論文 / 著書情報
Article / Book Information

論題(和文)	
Title(English)	CMOS Power Amplifier in 65nm Technology
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出典(和文)	, , , pp. 104
Citation(English)	2010 年電子情報通信学会エレクトロニクスソサイエティ大会, , , pp. 104
発行日 / Pub. date	2010, 9
URL	http://search.ieice.org/
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CMOS Power Amplifier in 65nm Technology

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1 Introduction

Nowadays, with the aggressive scaling down of gate length in CMOS technology, break down voltage is also reducing. This fact makes the CMOS power amplifier designing more challenging. In this paper we will describe our method for overcoming the breakdown voltage issue in CMOS devices.

2 Circuit topology and results

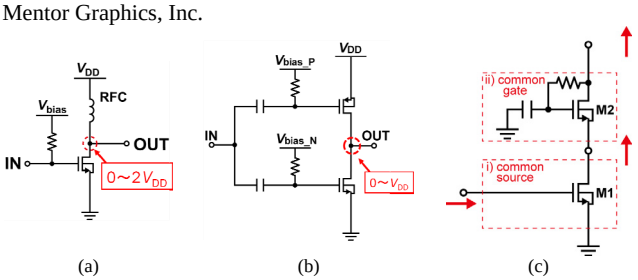
It's a rule of thumb that if the voltage of a device is low, in order to get high power we need to increase the current. But unfortunately, increasing power has its own problems. First, the device size will be enlarged with current. The other problem is the existence of parasitic elements; for example if there is a parasitic resistor in the source of the CMOS device, since the current is high, the voltage drop on this resistor will highly degrade the power amplifier performance. In the conventional power amplifier which is shown in Fig. 1 (a), the output power and efficiency is high at the expense of the low reliability because of $2V_{DD}$ voltage across the V_{DS}. Shown in Fig. 1 (b), In order to achieve more reliable circuit in term of breakdown voltage, CMOS inverter topology in which V_{DS} will be at most V_{DD}, can be used. It also will occupy smaller chip area but has the drawbacks of low output power and efficiency. In this topology for making it more linear, bias voltages applied to gates of MOS devices will be adjusted. Finally, instead of each MOS device in the inverter circuit, the cascode stage which is using self-biased technique and shown in Fig. 1 (c) will be used. The proposed method in this paper uses cascode technique to lower the voltage on each CMOS. In other words, we will increase the voltage of power amplifier stage while keeping the voltage on each CMOS as low as satisfying the breakdown voltage condition. The proposed circuit schematic is shown in Fig. 2. The power supply used in the output stage is 5 times of V_{DD} which is set to be 1.2V. The 1st and 2nd stages are for pre-amplification. Simulated results are shown in Fig. 3 and Fig. 4. From the Fig. 4, the output power can be as high as 23dBm which means the output voltage (8.9 V_{pp} in 50Ω system) is much higher than the breakdown voltage and obviously the proposed circuit has done its job. V_{bias} in Fig. 4 is the bias voltage adjusted at the gates of M_{3j}, M_{2d} and M_{1d}.

3 Conclusion

The proposed method for CMOS power amplifier design, divides the power supply voltage which is much higher than breakdown voltage across the output transistors and therefore satisfies breakdown voltage condition on each transistor while achieving high power at the output of the power amplifier.

Acknowledgment

This work was partially supported by STARC, MIC.SCOPE, KAKENHI, NEDO, Special Coordination Funds for Promoting Science and Technology, and VDEC in collaboration with Agilent Technologies Japan, Ltd., Cadence Design Systems, Inc., and Mentor Graphics, Inc.



(a) (b) (c)

Fig. 1 The basic idea of increasing power supply voltage while keeping the breakdown voltage condition at each transistor

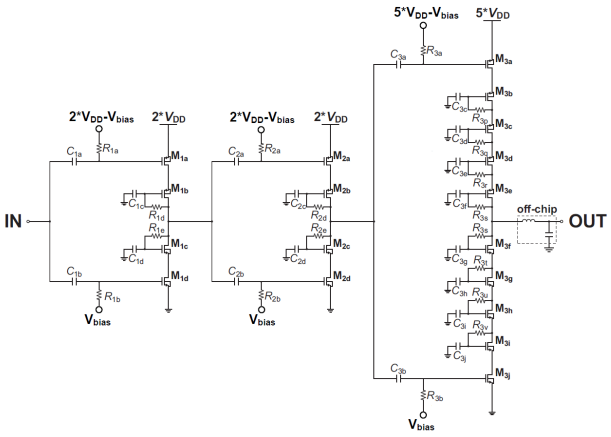


Fig. 2 The schematic of the proposed circuit

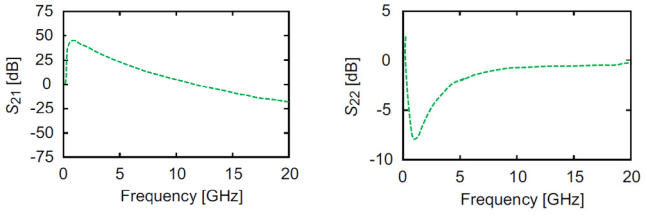


Fig. 3 Simulated S parameters of power amplifier at 2.5 GHz

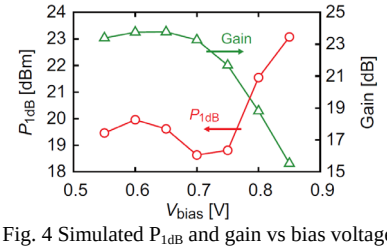


Fig. 4 Simulated P_{1dB} and gain vs bias voltage