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# A Study of Inverter-based RF CMOS Low Noise Amplifier Scalability in CMOS Process

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## 1　Introduction

Recently, small-sized and wide-band low noise amplifier (LNA) with low power consumption in RF circuits have been immensely developed. Today, electronic devices contain multiple RF front-end chips for various kind of wireless communications. Proportionally with the CMOS technology scaling, smaller size, higher cut-off frequency and lower power consumption are among the advantages obtained. However, passive devices such as inductors and capacitances consume large area despite of the developing scaling technology. Therefore, we study the scalability of CMOS inverter-based LNA.

## 2　Scalable Wideband LNA Design

Figure 1 shows the schematic of our LNA circuit. We applied Cherry-Hooper technique and active gain peaking technique to our inverter based LNA to enhance the bandwidth. With Cherry-Hooper technique, Miller effect that usually limits bandwidth is reduced, and effective input capacitance for the first stage is defined as

$$C_{\text{in}} = C_{\text{gs1}} + C_{\text{gs2}} + (C_{\text{gd1}} + C_{\text{gd2}})[1 + (g_{\text{m1}} + g_{\text{m2}})Z_{\text{x}}] \quad (1)$$

Moreover, as CMOS gate width is scaled down, parasitic capacitances such as $C_{\text{gs}}$ and $C_{\text{gd}}$ are reduced and this further enables improvement in the bandwidth expansion.

Second method for bandwidth enhancement is by implementing inverter feedback to the cascaded inverters. Instead of implementing the commonly used capacitance or inductive peaking technique to broaden the bandwidth, we used an active peaking technique using scalable CMOS inverter. With feedback inverter, the feedback is negative at low frequency, and as the frequency increases, the feedback changes to positive.

Finally, in the end of the proposed design, an additional low-resistance feedback amplifier is added to provide high load impedance to the voltage amplifier and better 50 Ω output matching. Since no passive device was used in the entire circuit, this design promises scalability in size.

## 3　Scalability Results

The circuit was fabricated with 40 nm, 65 nm, 90 nm and 180 nm CMOS process. Chip micrographs (65 nm, 90 nm 180 nm) and layout (40 nm) of our designed LNAs are shown in Fig 2 with size comparison. The scalability of the circuit in size, power consumption, noise figure, and bandwidth of each process when gain is above 15 dB and S11<-10 dB are shown in Fig 3. 40 nm LNA is currently under fabrication, thus simulation result is presented.

## 4　Conclusion

In this work, we proposed wideband scalable inverter-based RF CMOS LNA. Based on the results obtained, our LNA is highly potential in scalability as we achieved higher bandwidth and smaller size accordingly to the CMOS scaling. For future work, we are going to investigate methods on how to improve circuit linearity and minimize noise figure for our designed LNA.

## Acknowledgments

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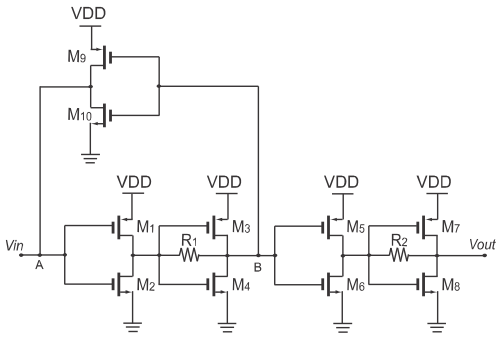


Fig. 1　Proposed LNA schematic

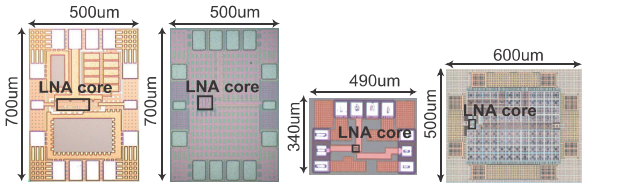


Fig. 2　Fabricated chips' micrographs and layout

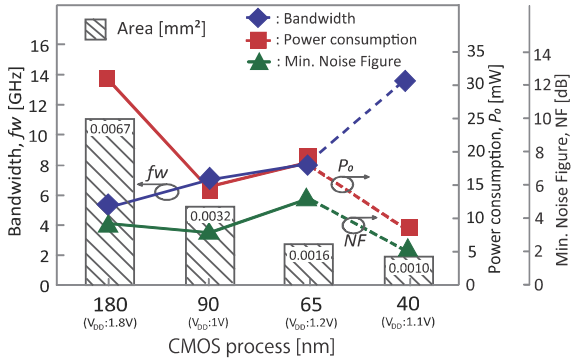


Fig. 3　LNA scalability


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