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RF signal generator using time domain harmonic suppression technique in 90 nm CMOS

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Abstract: This paper proposes an RF signal generator using a time domain harmonic suppression technique based on Fourier series analysis. The circuit consists of four differential ring voltage control oscillators (VCO's) with phase differences and the pulse signal summing circuit. By summing pulse signals from VCO's with appropriate phase differences determined by Fourier series in time domain, the third and fifth harmonics can be cancelled without filters. To confirm the validity, a prototypal RF signal generator was fabricated in 90-nm CMOS technology. As a result, we succeeded in generating an RF signal from digital pulse signals. The frequency range is from 1.1 to 3.7 GHz with 1-V power supply. The suppression of both the third and fifth harmonics are below −48 dBc at 1.1 GHz and −42 dBc at 3.7 GHz.

Keywords: RF signal generator, time domain, ring oscillator

Classification: Integrated circuits

References

[1] Y. Zhou and J. Yuan, "A 10-Bit Wide-Band CMOS Direct Digital RF Amplitude Modulator," *IEEE J. Solid-State Circuits*, vol. 38, no. 7, pp. 1182–1188, July 2003.

[2] X. Geng, F. F. Dai, J. D. Irwin, and R. C. Jaeger, "An 11-bit 8.6 GHz Direct Digital Synthesizer MMIC With 10-Bit Segmented Sine-Weighted DAC," *IEEE J. Solid-State Circuits*, vol. 45, no. 2, pp. 300–313, Feb. 2010.

[3] M. E. Heidari, M. Lee, and A. A. Abidi, "All-Digital Outphasing Modulator for a Software-Defined Transmitter," *IEEE J. Solid-State Circuits*, vol. 44, no. 4, pp. 1260–1271, April 2009.

[4] J. A. Weldon, R. S. Narayanaswami, J. C. Rudell, L. Lin, M. Otsuka, S. Dedieu, L. Tee, K. Tsai, C. Lee, and P. R. Gray, "A 1.75-GHz Highly Integrated Narrow-Band CMOS Transmitter With Harmonic-Rejection Mixers," *IEEE J. Solid-State Circuits*, vol. 36, no. 12, pp. 2003–2015, Dec. 2001.

[5] Z. Ru, E. A. M. Klumperink, G. J. M. Wienk, and B. Nauta, "A Software-defined Radio Receiver Architecture Robust to Out-of-Band Interference," *ISSCC Dig. Tech. Papers*, pp. 230–231, Feb. 2009.

[6] K. Nakano, S. Amakawa, N. Ishihara, and K. Masu, "RF Signal Generator

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Received December 25, 2011
Accepted January 21, 2012
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Based on Time-to-Analog Converter in 0.18 μm Complementary Metal Oxide Semiconductor," *Japan J. Applied Physics*, vol. 49, pp. 04DE12-1–04DE12-4, April 2010.

1 Introduction

To generate analog signals from digital pulse data used in RF data processing, a digital-to-analog converter (DAC) is used generally. However, high-speed and high-resolution characteristics, that make the circuit complex and large-scale, are necessary to generate low-distortion RF signals. For example, in order to obtain RF signals with low distortion of less than -50 dBc, more than 10-bit resolution is required [1, 2]. Thus, the circuit scale and the power consumption become large. Furthermore, as allowable power supply voltage becomes small in the finer CMOS process, getting high voltage domain resolution is particularly difficult. Therefore, the use of the conventional DAC for the RF signal generation is not practical. To reduce the circuit scale and the power consumption, a digitally controllable RF circuit technique is demonstrated [3]. In addition, a harmonic suppression using the multi voltage step signal generation has been proposed [4, 5]. And we also suggested the time-to-analog conversion (TAC) technique for RF signal generation using the time domain resolution instead of the voltage domain resolution [6]. This technique is useful for low-voltage operation other than reduction of circuit scale and power consumption. However, to obtain low-distortion RF signals, the circuit scale also become large because high time domain resolution is required, similar to the conventional voltage domain DAC.

In this paper, an RF signal generator using time domain harmonic suppression technique that does not require large circuit scale was clarified based on Fourier series analysis. Validity was confirmed by fabricating a prototypal RF signal generator in 90-nm CMOS process technology.

2 RF signal generator for harmonic suppression

In RF communication systems, RF signal harmonics cause adjacent channel interference by mutual interference and thus degrade RF communication quality. In particular, reducing the odd number harmonics is one of the important issues in RF systems. To generate a low-distortion signal, LC resonant circuit is generally used but the LC circuit occupies large chip area, resulting in high cost. Therefore, RF signal generation from digital pulse signal is desired, but the rectangular digital pulse data consists of fundamental and odd harmonics as shown in the following Fourier series.

$$f(t) = \frac{4}{\pi}\left(\frac{\cos\omega t}{1} - \frac{\cos 3\omega t}{3} + \frac{\cos 5\omega t}{5} - \cdots\right). \quad (1)$$

where the Fourier series of the function $f(t) = 1$ for $-T/4 < t < T/4$ and $f(t) = -1$ for $-T/2 < t < -T/4$ and $T/4 < t < T/2$. t is time value, T is the

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period of signal. The third and fifth harmonic levels are easily calculated as −9.5 dBc and −14 dBc, respectively. RF systems cannot accept these values.

If the rectangular signal is converted to a triangular signal, the triangular signal becomes near to the sinusoidal RF signal. Fourier series for the triangular signal is given by following equation.

$$f(t) = \frac{8}{\pi^2}\left(\frac{\cos\omega t}{1^2} + \frac{\cos 3\omega t}{3^2} + \frac{\cos 5\omega t}{5^2} + \cdots\right). \quad (2)$$

where the Fourier series of the function $f(t) = 1 - (4t/T)$ for $0 < t < T/2$ and $f(t) = 1 + (4t/T)$ for $-T/2 < t < 0$.

Compared with the rectanglar signal, the third and fifth harmonic levels are reduced to −19 dBc and −28 dBc. However, these values are not small enough for RF systems that require a level of less than −50 dBc. To get high suppression, it is necessary to configure the high time resolution to generate the RF signal as close as sinusoidal signal. In order to solve this problem, we introduce the third and fifth harmonic suppression technique into the RF signal generator by the sum of delay signals as a method to reduce the resolution. Fig. 1 (a) shows a RF signal generator consisting of a differential ring oscillator to generate the stepped triangular signal (G1 in Fig. 1 (b)). The stepped triangular signal includes the third and fifth harmonic components. The τ is the delay time of the ring oscillator outputs in Fig. 1 (a). At first to suppress the fifth harmonics, the signal delayed by the half period of the fifth harmonic component (G2 delayed by $T/10$ from G1) is generated and summed to G1. The fifth harmonics is cancelled by summing two signals (G1+G2). To cancel the third harmonics in the same way, the signal delayed for the half period of the third harmonic component (G3 delayed by $T/6$ from G1) is generated and summed to G1. A signal (G4) delayed by $T/10$ from G3 is generated to cancel the fifth harmonics in G3. By summing signals from G1 to G4, the third and fifth harmonics can be cancelled. Fig. 1 (c) shows the generated RF signal spectrum simulated when a 2-bit stepped triangular signal is assumed from G1 to G4. The main signal is not canceled. The third and fifth harmonics are reduced to less than −50 dBc effectively. This technique can also be used for the rectangular signal directly from Eq. (1). However, as the harmonics of the triangular signal are smaller than those of the rectangular signal, subtractions can be made effectively from the triangular signal.

3 Chip fabrication result in 90-nm CMOS process technology

We designed the broadband RF signal generation circuit. Circuitry is shown in Fig. 2 (a). To get four sets of 2-bit stepped triangular signals (G1-G4), four differential ring oscillators consisting of inverters with latching connection are used. To produce the delays between four triangular signals, ring oscillators are connected through tunable delay cells consisting of simple inverters. By tuning the delay between triangular signals, canceling operation can be observed. When the output frequency of four triangular signals are ω_0, The delay time ($\Delta t1$) between G1 and G2, and $\Delta t3$ between G3 and G4 are set

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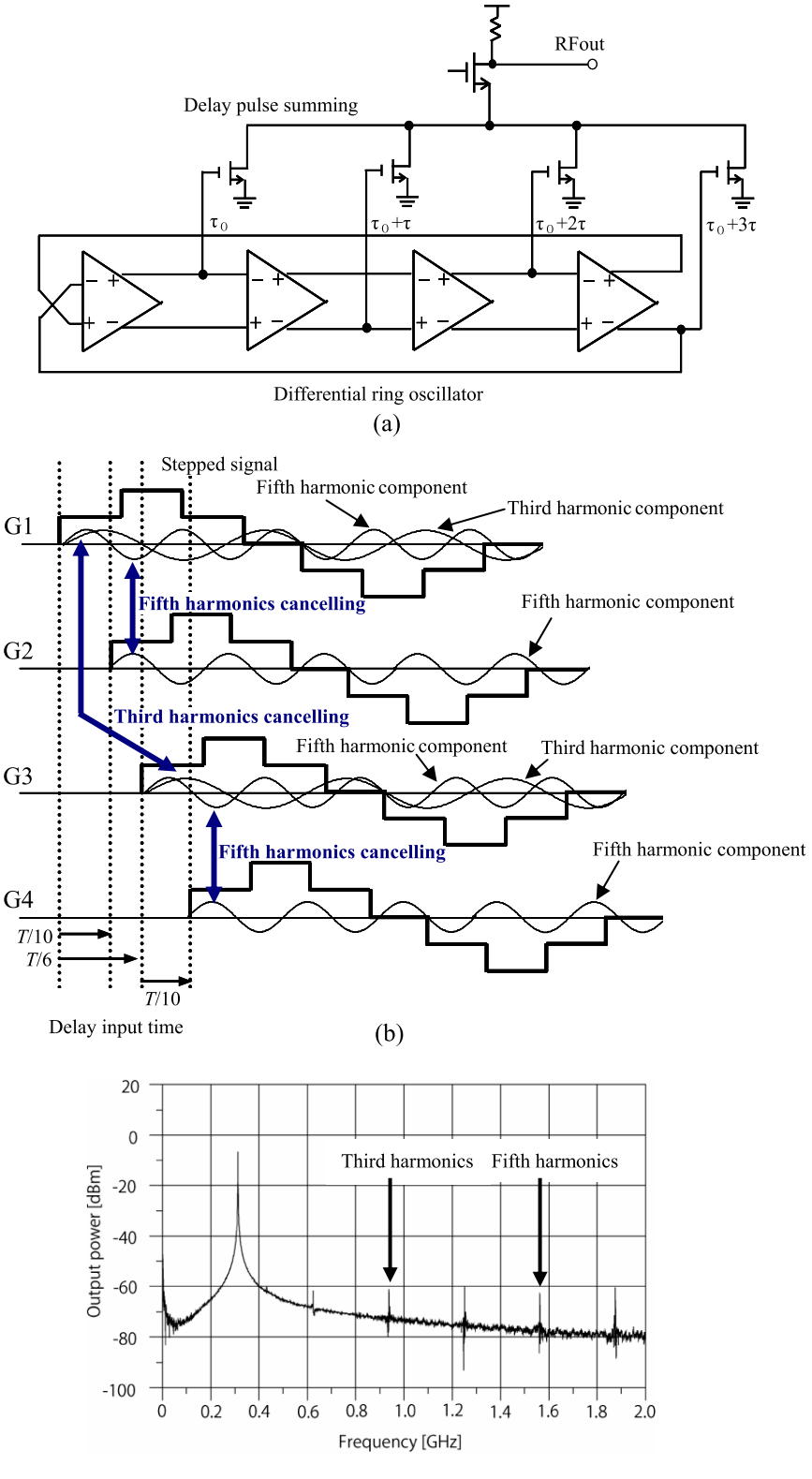

Fig. 1. (a) RF signal generator, (b) Method of third and fifth harmonic suppression, (c) Simulated signal spectrum of third and fifth harmonic suppression.

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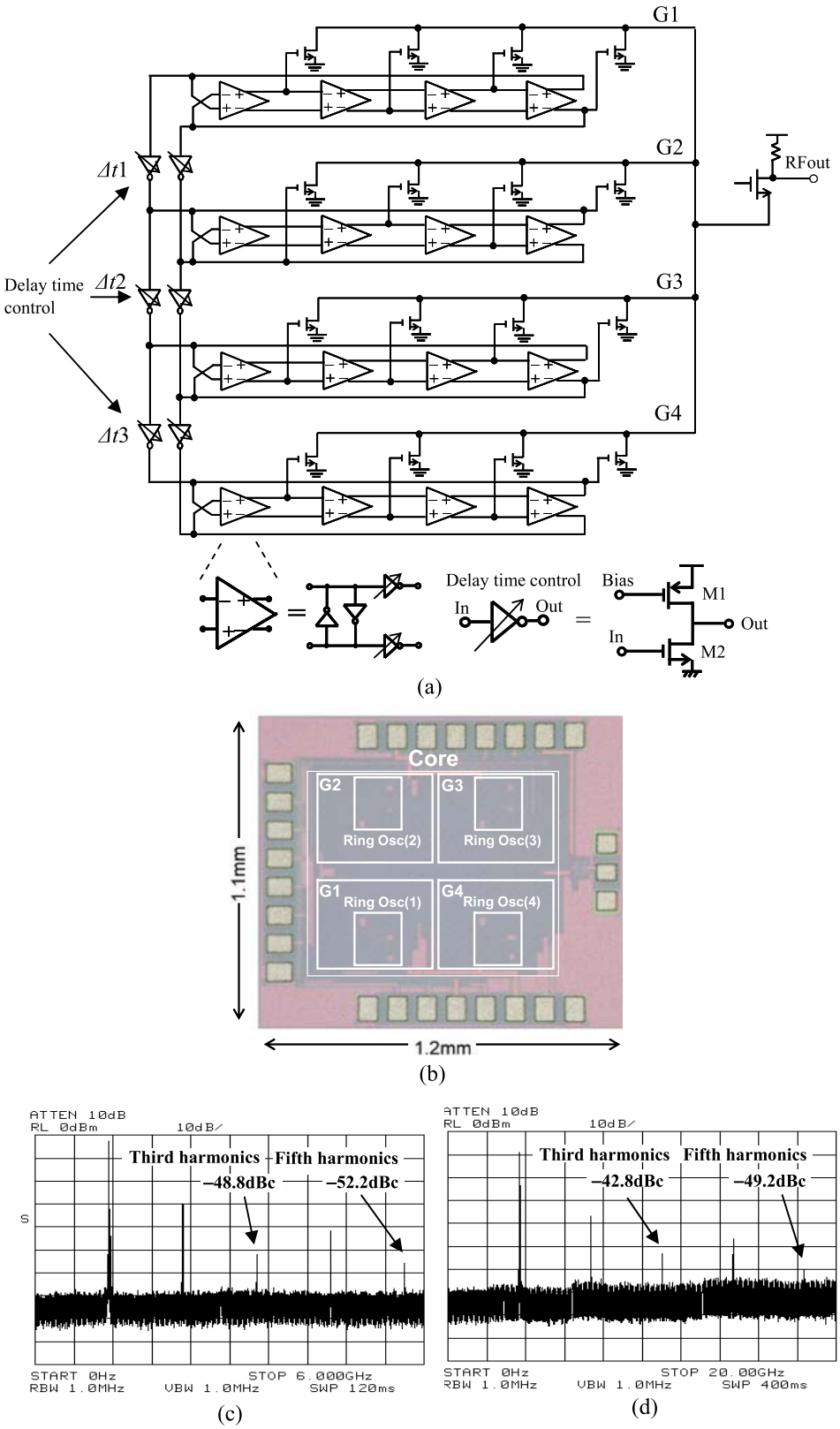

Fig. 2. (a) Block diagram of the RF signal generator, (b) Chip micrograph, (c) Measured ou tput spectrum with third and fifth harmonic suppression at 1.1 GHz, (d) Measured output spectrum with third and fifth harmonic suppression at 3.7 GHz.

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up $\pi/(5\omega_0)$, The delay time ($\Delta t2$) between G2 and G3 is set up $2\pi/(15\omega_0)$. Thus the third and fifth harmonics can be suppressed. The circuit is also designed so that oscillation frequency can be controlled by changing the load resistance value of each differential delay cell. The delay cell in this design uses M1 and M2. M1 is a pMOS transistor, and M2 is an nMOS transistor. The delay time can be controlled by bias control of M1.

To confirm the effectiveness of this circuit, a test chip was designed and fabricated using a 90-nm CMOS technology. A chip photo-micrograph is shown in Fig. 2 (b). The core size of the chip is 0.82 mm × 0.70 mm. The fabricated chip could generate from 1.1 GHz to 3.7 GHz RF signals. The power supply is 1.0 V. Fig. 2 (c) and (d) show measured RF output signal spectrum when the output frequency was 1.1 GHz and 3.7 GHz, respectively. The output main signal level was −1.4 dBm, the third harmonics was −48.8 dBc and the fifth harmonics was −52.2 dBc at 1.1 GHz, and at 3.7 GHz, the output main signal level was −5.4 dBm, the harmonics of the third and fifth were −42.8 dBc and −49.2 dBc. We confirmed the reduction of both the third and fifth harmonics effectively with the simple RF signal generator. Here, large even-order harmonics are observed. We think this is caused by the influence of an output buffer circuit and that it can be cancelled by taking the differential topology in the RF signal generator. As the remaining problem is the appropriate delay tuning between triangular signals, we are studying how to control the delay automatically.

4 Conclusion

An RF signal generator using harmonics suppression technique that does not require large circuit scale was clarified based on Fourier series analysis. By fabricating the chip in 90-nm CMOS process technology, we succeeded in generating RF signal from digital pulse suppressing the third and fifth harmonics less than −48 dBc at 1.1 GHz and −42 dBc at 3.7 GHz.

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