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Silicon double quantum dots with charge sensors for spin-based quantum information devices

A thesis submitted

In fulfillment of the requirements for the degree of

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by

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to the

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Contents

Chapter 1: Introduction

In this chapter, quantum computer, a new kind of information device, is explained as a research background and current situation of charge and electron spin qubits in semiconductor and coupled silicon quantum dot device are introduced. Finally, research purpose and constitution of this work are shown.

1.1. Background

1.1.1. Quantum computer

The semiconductor industry has been remarkably developing and achieving the high-speed, low electric consumption, and high-density integration, by scaling law. Because of the development of the nano-scale fabrication technology, semiconductor quantum dot (QD) structure can be fabricated, in which electrons are confined in zero dimension regime [1,2]. The various characteristics about the electrons of quantum dots have been studied recently. The research about the quantum computer with logical operation with quantum characteristics of few-electron in the QD has attracted [3]. The attached shows the basic theory of the quantum computer.

The research about the quantum computer has been studied since 1960's, but at that time, just the logic one had been done because the calculation ability of the computer doubted whether it was higher than the classical one or not. However, Peter W. Shor in the Bell laboratory proved that quantum algorithm could solve prime factorization extremely quickly with small error probability [4], which changed that situation. The factorization of large number of digits within the realistic time scale is impossible even for the best supercomputer in the world, and then it ensures safety of public key algorithm, for example RSA. If the quantum computer were realized, the factorization would be done at high speed and the safety of cipher would be destroyed, which would give a terrible influence to the society. Therefore, the experiment of the quantum computer in the real physical science has been advanced.

1.1.2. Semiconductor charge qubit and electron spin qubit

Bits of the quantum computer are called qubits. Qubits should have a possibility to be a candidate as a physical system of quantized two states. During the operation in the two-state condition, keeping the quantum states is necessary (coherent operation), which has been researched. The system which could prove many coherent operations concerning qubits uses nuclear spins in molecule, and the demonstration of the prime factorization of integer 15 was performed by solution NMR [5].

However, making further more qubits is extremely difficult because the molecular structure decides the number of qubits in this system. Therefore, for the accumulation in the future, the research with solid-state is advanced, and the qubits confining electric charge in a quantum dot has attracted.

One charge qubit, which is one of the examples of qubit systems confining electric charge in serially coupled two QD, is considered as one qubit. Quantum calculation is operated by superposition of the existence probability of the confined electron in the DQD. The coherent operation of one qubit is already reported in the research with using the two dimensional electron gas in heterostructure of compound semiconductor (GaAs/AlGaAs)[6]. For the charge qubits, the control of the coupling strength between two QDs is very important because the coupling within qubits decides the speed of the coherent operation [7]. Furthermore, for the realization of the quantum computer, the analysis of two-qubit behavior is extremely important because it is possible to build an arbitrary quantum circuit with the coherent operation of one qubit and CNOT gate of two qubits [8]. For the integration of qubits, the analysis of the electrostatic interaction in the device structure, which is corresponding to two qubits and the coherent operation have been achieved with compound semiconductor charge qubits [9, 10].

However, charge qubits has a problem, which means the destruction of quantum states for very short time, few nano-seconds. On the other hand, spin qubits [11] using the electronic spin confined in qubits is expected the longer time of quantum state than charge qubits, a few micro-seconds [12,13], and then, various approaches are tried. The coherent operation of single electron-spin in the QDs with compound semiconductor has been achieved by using electron spin resonance (ESR) with oscillating magnetic field led by strip line on the QDs [14]. In this experiment, the double QD (DQD) is used as the system to confine the electron spin. An effect of current suppression caused by Pauli exclusion, called Pauli spin blockade (PSB), has an important role for readout of the electron spin [15,16]. On the other hand, the coherent operation of the electron spin by using only electric field, not local magnetic field, has been reported in the similar structure of DQD. Electric field does not directly interact with the spin, but it controls the spin through various mechanisms: spin-orbit interaction [17], hyperfine interaction [18] and slant magnetic field by integrated micro magnet to the structure [19, 20]. Furthermore, the coherent operation with two electron spin, corresponding to two qubits, has achieved by using QDs with compound semiconductor [21]. The control of the coupling between the DQD is also important for this electron spin qubit system. The control of the strength of the coupling between the QDs plays the important role for qubit operations, for example, both single qubit and two qubit operation are shown by the same device structure with different coupling strength, and the speed of the coherent operation of electron spin is modulated by the strength [22].

1.1.3. Silicon coupling quantum dots

The research shown the above mainly has been done with two dimensional electron gas in heterostructure, especially GaAs/AlGaAs. This system has a small effective mass

m^* ($m^* = 0.067\ m_0$, m_0: mass of free electron), and so the size to obtain clear quantum effect is easy to fabricate with electron beam lithography, and is appropriate research object for basic physics. However, the causes destroying the coherence of electron spin has been proved with the progress of the research of quantum operation by compound semiconductor [12]. The most important point is the limitation of relaxation time of the spin by hyperfine interaction between electron spin and nuclear spin. According to one research, the relaxation time is dramatically extended by a polarization of the nuclear spin with pumping by flip-flop of the electron spin and nuclear spin [23] for controlling the spin relaxation by hyperfine interaction [24].

In the main current of such research, the other research with the material which has almost no nuclear spin such as IV semiconductor has been remarkable. For example, the research with carbon, carbon nano tube [25, 26, 27, 28, 29] and graphene [30, 31], and that with silicon, Si nanowire [32, 33, 34, 35] , two dimensional electron gas with a heterostructure of Si/SiGe [36, 37] and Ge/Si core shell nanowire [38] have been done. We focus on silicon, since there is almost no hyperfine interaction because 95% of natural silicon has no nuclear spin. Moreover, it is possible to completely remove the interaction with the perfect control of isotope. The coherence time becomes long because of small spin-orbit interaction (Rashba spin-orbit interaction [39]) and the inexistence of piezo-electric electron-phonon interaction. Recently, silicon is highly attractive as the object for the research of quantum information, and it is profitable for the integration of the qubits in the future because it is very adjustable with the existing silicon CMOS (Complementary Metal-Oxide-Semiconductor) fabrication process. Characteristics of electron transport in the coupled QDs of silicon has been researched in various structures: QDs in silicon narrow line controlled with top gate bias [40, 41], Si:P QDs fabricated by ion implantation of phosphorus [42], QDs controlled by top gate bias in Ge/Si core shell nanowire [43], Si/SiGe two dimensional electron gas [44]. The electron-spin coherence time T_2^* of phosphorus in natural and isotope-controlled Silicon is measured as longer than 1 ms and 1 s [45], and then, the electron spin qubit with Silicon becomes more promising. There is no report of Si spin qubit while there are T_1 measurement with Si:P QDs[46] and the coherent rotation of electron spin with exchange interaction in Si/SiGe substrate [46]. One reason is that the small splitting of the quantized levels in Silicon because of larger effective mass of electron (along minor axis $m^* = 0.19m_0$, along major axis $m^* = 0.916m_0$ in constant-energy surface) than that in GaAs. The small splitting results in the large number of electrons in the QD and unexpected superposition of charge and/or spin states. To obtain the large splitting, the Si QD size should be smaller than 50 nm.

Electron-spin control by using spin-orbit interaction and/or hyperfine interaction, which are the decoherence source, is already achieved in III-V semiconductor [48], while the control by those interactions is difficult in Silicon. Exchange interaction also control the electron spin, however, three coupled QDs are necessary to make an exchange-only qubit [49]. Integration technique of qubits is another challenge for quantum computation because many qubits should be integrated for quantum calculation. Therefore, the development of the system which operates each qubit independently and includes many qubits is necessary.

1.2. Research purpose

From the discussion in above background, we focus on the development of element technologies for Si spin qubits as follows in this work:

1. Development of the integration technology of Si QDs. Many gate electrodes and sensors should be used for one spin qubits, which becomes a problem for the integration.
2. Design the Si QDs device to develop the technology of the single electron-spin control. Especially, we focus on ESR method with RF wave which is suitable for future spin-qubits integration.

The Si QDs used in this work are defined lithographically and its shape is flexibly changed by the change of the design pattern of the lithography. For the actual quantum information processing in the future, Si spin qubits not only one qubit but also further integration of many qubits should be achieved. Therefore, development of the technology of the single electron-spin control with Si QDs fabricated by Si-MOSFET compatible process is another aim of this work.

1.3. Outline of the thesis

Chapter 1 Introduction

Chapter 1 presents the motivation for this work and over all literature review of semiconductor charge and spin qubits.

Chapter 2 Theory of Electron Transport in Quantum Dot Devices

Chapter 2 gives explanations theories of electron transport through QDs to analyze the characteristics in this work and electron-spin resonance. Derivation of electrostatic energy in the system of N conductor, principles of single electron tunneling, single QD and coupled QD structure and principle of the electron spin resonance are explained.

Chapter 3 Experimental Techniques

Chapter 3 gives detail introduction of main equipment and fabrication process which are used in this work.

Chapter 4 Analysis of Charge Modulation in Si DQD

Chapter 4 gives analyses of dependence of charge distribution on gate bias and temperature in Si QDs. Reduction of the number of the charges for electron-spin resonance is also discussed.

Chapter 5 Detection of Single Electron Transport in various Si DQD Structures

In chapter 5, coupled QDs device with a sensor to readout electron position, which is used to also detect electron spin, are fabricated and its transport characteristics are discussed. Device structures to obtain high tunnel rate through the QDs are also discussed.

Chapter 6 Dual Function of Charge Sensor: Charge Sensing and Gating

In chapter 6, a gating function of the integrated sensor in chapter 5 with its sensing function is developed for the first time. The gating function is also applied to self-modulation for wide-range charge detection. Integration of QDs for quantum information processing is discussed for the future.

Chapter 7 Analysis of Electron Spin Resonance with Ferromagnets and Si DQD

In chapter 7, electron-spin control by electron spin resonance with local magnetic field by ferromagnets and micro wave is analyzed for our Si QDs. Frequency of electron spin resonance is estimated as faster ~1 order of magnitude than similar QDs device in GaAs by calculated magnetic field, which is generated by ferromagnets and equipment. From the measurement of the DQD device with ferromagnet, the blockade region in several bias triangles is observed. From the magnetic field dependence of the leakage current in the blockade region, the blockade region is by valley-spin blockade. We also mention about the magnetic field and RF dependence at the blockade region. Furthermore, the method to resonance without magnetic field applied by equipment is analyzed by the optimization of the device structure.

Chapter 8: Conclusions

Chapter 8 summarizes this work.

Chapter 2: Theory of Electron Transport in Quantum Dot Devices

Abstract

In this chapter, theories of electron transport through QDs to analysis the characteristics in this work and electron-spin control by oscillating magnetic field are explained. In particular, derivation of electrostatic energy in the system of N conductor, principles of single electron tunneling, single QD and coupled QDs structure and electron spin resonance are explained.

2.1. Electrostatic energy in N conductors

There are capacitive coupling between every conductors and ground, an electrical reference, in an electrical circuit. A total number of the capacitance in the system consisted from N conductors is

$$N+\sum_{k=1}^{N}\frac{k-1}{2}=\frac{N(N+1)}{2} \quad . \tag{2.1}$$

Total charge Q_j in conductor j is showed as sum of the charges in the other conductors which is coupled to itself,

$$\begin{aligned} Q_j &= \sum_{k=0}^{N} q_{jk} = \sum_{k=0}^{N} c_{jk}\left(V_j - V_N\right) \\ &= c_{jk}\left(V_j - V_0\right) + c_j\left(V_j - V_1\right) + \cdots + c_{jN}\left(V_j - V_N\right) \\ &= -c_{jo}V_0 - c_{j1}V_1 - \cdots - c_{j(j-1)}V_{j-1} + \sum_{k=0,k\neq j}^{N} c_{jk}V_j - c_{j(j+1)}V_{j+1} - \cdots \\ &\qquad - c_{jN}\,V_N \end{aligned} \quad , \tag{2.2}$$

when c_{jk} and q_{jk} are the capacitance and charge between the conductor j and k, V_j is an electrostatic potential of the conductor j and electrostatic potential of the ground $V_0 = 0$. This equation is also expressed as a capacitance matrix

$$\vec{Q} = C\vec{V} \quad , \tag{2.3}$$

when

$$\vec{Q}=\begin{pmatrix} Q_0 \\ Q_1 \\ \vdots \\ Q_N \end{pmatrix}, \vec{V}=\begin{pmatrix} V_0 \\ V_1 \\ \vdots \\ V_N \end{pmatrix}, \qquad C=\begin{pmatrix} C_{00} & C_{01} & \cdots & C_{oN} \\ C_{10} & C_{11} & \cdots & C_{1N} \\ \vdots & \vdots & \ddots & \vdots \\ C_{N0} & C_{N1} & \cdots & C_{NN} \end{pmatrix} \quad , \tag{2.4}$$

and

$$C_{jj} = \sum_{k=0,k\neq j}^{N} c_{jk}\,, C_{jk} = C_{kj} = -c_{jk} \quad . \tag{2.5}$$

An electrostatic energy $\vec{U}$ is a sum of the charged energy in the N (N + 1) / 2 capacitances as

$$\vec{U} = \frac{1}{2}\vec{V}\cdot C\vec{V} = \frac{1}{2}\vec{V}\cdot\vec{Q} = \frac{1}{2}\vec{Q}\cdot C^{-1}\vec{Q} \quad . \tag{2.6}$$

A power supply can be added as a node with the capacitance C_p to the ground to this system. There is an enough charge Q_p in the power supply, and then the its voltage V_p is shown as $V_p = Q_p / C_p$. The charge of this system is calculated by using the capacitance submatrices

$$\begin{pmatrix} \vec{Q}_c \\ \vec{Q}_p \end{pmatrix} = \begin{pmatrix} C_{CC} & C_{CP} \\ C_{VC} & C_{PP} \end{pmatrix} \begin{pmatrix} \vec{V}_c \\ \vec{V}_p \end{pmatrix} \quad , \tag{2.7}$$

when the vector of the charge and voltage of the conductor (power supply) nodes are $\vec{Q}_{\mathrm{c(p)}}$ and $\vec{V}_{\mathrm{c(p)}}$. Therefore, by inverse matrix of the C_{CC}, $\vec{V}_c$ is derived as

$$\vec{V}_c = C_{CC}^{-1}\left(\vec{Q}_c - C_{CV}\vec{V}_p\right) \quad , \tag{2.8}$$

and the electrostatic energy of the conductor nodes $\vec{U}_c$ is calculated the same way as eq. (2.6))

$$\vec{U}_c = \frac{1}{2}\vec{V}_c \cdot C_{cc}\vec{V}_c = \frac{1}{2}\vec{V}_c \cdot \left(\vec{Q}_c - C_{CP}\vec{V}_p\right) \quad . \tag{2.9}$$

2.2. Tunnel junction: Coulomb blockade

At first, we think a junction with a capacitance C. Electron cannot transport through a potential barrier in classical theory, and then charge $Q = CV$ and electrostatic energy $U = Q^2 / 2C$ are accumulated when a voltage V is applied to the junction. The energy $U(N)$ with the accumulated N electrons at the junction is

$$U(N) = \frac{(-N|e|)^2}{2C} = N^2 \times \frac{|e|^2}{2C} \quad , \tag{2.10}$$

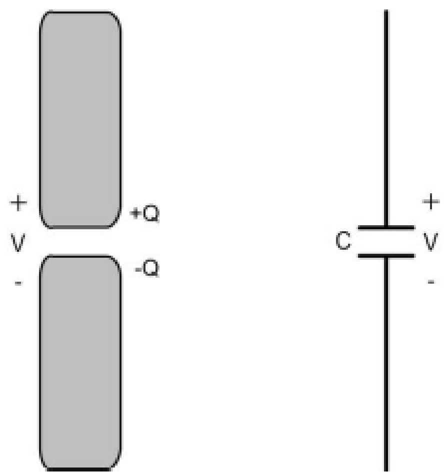


Fig2.1: Single junction

when $|e| = 1.6 \times 10^{-19}$ is elementary charge. However, the electron can tunnel through the junction with a tunnel rate Γ because of a broadening of its wave function. Such a junction is called tunnel junction. $U(N)$ is changed when one electron tunnel through the junction, and the difference of the energy $\mu(N)$ is represented as

$$\begin{aligned}\mu(N) &= U(N) - U(N-1) \\ &= (N^2 - (N-1)^2)\frac{|e|^2}{2C} \\ &= (2N-1)\frac{|e|^2}{2C}\end{aligned} \quad . \tag{2.11}$$

The μ is called as electrochemical potential, which is defined as energy to add Nth electron to the system. Next, we think a system which the charge is not accumulated at the tunnel junction and voltage V_{sd} is applied to it by the voltage source. The current does not flow through the junction when the electrochemical potential of the electrode voltage $\mu = |e|V_{sd}$ is smaller than the potential for the single-electron tunneling $\mu(1)$. The phenomenon such as the prohibition of the tunneling is called Coulomb Blockade in the regime,

$$\begin{aligned}\mu_L &< \mu(1) \Leftrightarrow \\ |e|V_{sd} &< \frac{|e|^2}{2C} \Leftrightarrow \\ V_{sd} &< \frac{|e|}{2C}\end{aligned} \quad . \tag{2.12}$$

On one hand, the junction is regarded as a resistor with a tunnel resistance R_T when $V_{sd} > |e|/2C$ and then the current flows. On the other hand, when $V_{sd} < 0$, we think the virtual voltage $V'_{sd} = -V_{sd}$ is connected instead of V_{sd} for the simplify. The comparison of the electrochemical potential μ_R and $\mu(1)$ declares the condition for the Coulomb blockade,

$$\begin{aligned}\mu_R &< \mu(1) \Leftrightarrow \\ |e|V'_{sd} &< \frac{|e|^2}{2C} \Leftrightarrow \\ -|e|V_{sd} &< \frac{|e|^2}{2C} \Leftrightarrow \\ V_{sd} &> -\frac{|e|}{2C}\end{aligned} \quad . \tag{2.13}$$

From eq. (2.12)) and (2.13)), the total condition for the Coulomb blockade with the single junction is assembled as

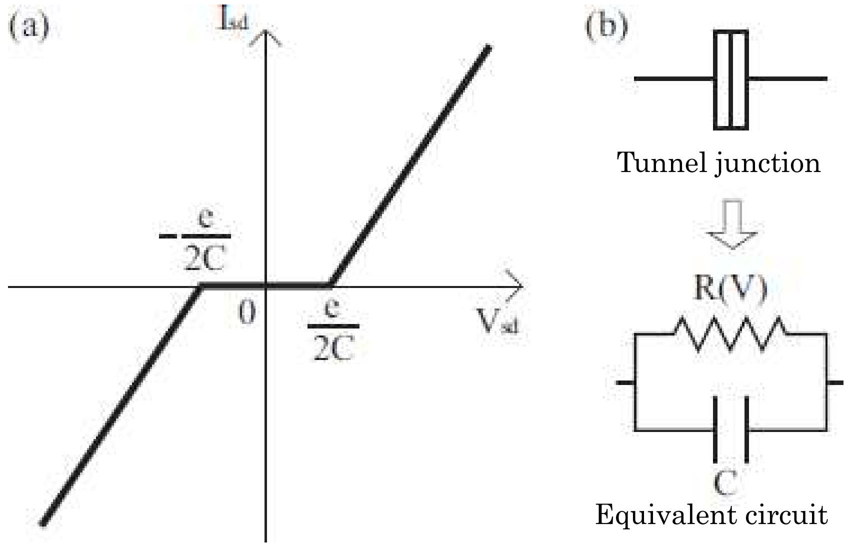


Fig. 2.2: (a) I_{sd}- V_{sd} characteristic of Coulomb blockade. (b) Equivalent circuit of tunnel junction in classical model.

$$-\frac{|e|}{2C} < V_{sd} < \frac{|e|}{2C} \quad . \tag{2.14}$$

Characteristics of ideal Coulomb blockade is shown as Fig.2.2(a). A width of the Coulomb blockade regime is called as Coulomb gap. The tunnel junction and the equivalent circuit can be depicted as Fig. 2.2(b) when

$$R(V) = \begin{cases} \infty \left(|V_{sd}| < \frac{|e|}{2C} \right) \\ R_T \left(|V_{sd}| > \frac{|e|}{2C} \right) \end{cases} \quad . \tag{2.15}$$

To observe the Coulomb blockade experimentally, below conditions should be satisfied;

A. Fluctuation by thermal energy

Coulomb blockade is not observed when the thermal fluctuation of the system $k_B T$ (k_B: Boltzmann constant) is larger than the Coulomb gap $2\mu(1)$ because electron can tunnel through the junction even V_{sd} = 0. Therefore, Coulomb blockade should be observed when the condition is needed as below;

$$2\mu(1) = \frac{|e|^2}{2C} \gg k_B T \quad . \tag{2.16}$$

The capacitance C for the blockade at the room temperature (T = 300 K) is

$$C \ll \frac{|e|^2}{k_B T} \sim 6[\mathrm{aF}] \quad . \tag{2.17}$$

Extremely fine structure is necessary to obtain such as the very small C. For example, the area of the parallel plate capacitor S with a gap $d \sim 1$ nm is

$$S \ll \frac{dC}{\epsilon_0} \sim 25 \times 25\ [\mathrm{nm}^2] \quad . \tag{2.18}$$

Techniques of a high level fabrication, for small d and S, and of a measurement at low temperature, for small T, are important to observe Coulomb blockades experimentally.

B. Tunnel resistance with uncertainly principle

The tunnel resistance should follow the below equation,

$$R_T \gg R_K = \frac{h}{|e|^2} \sim 25.8[\mathrm{k\Omega}] \quad , \tag{2.19}$$

when R_{K} is called resistance standard, which is derived by time and energy uncertainly. A time constant of relaxation by the tunneling through the tunnel junction τ is written by the tunnel capacitance C and tunnel resistance R_{T} as $\tau = CR_T$. The energy of the system is fluctuated $\sim h/CR_T$ by the uncertainly principle. Coulomb gap should be wider than the fluctuation to be observed, therefore,

$$\frac{h}{CR_T} \ll \frac{|e|^2}{C} \Leftrightarrow R_T \gg \frac{h}{|e|^2} \quad . \tag{2.20}$$

C. Coupling with environment

The tunnel junction is coupled with environment in real setting. We assume that the impedance of the environment $Z(\omega)$ is connected between the junction and voltage source serially. Equation (2.12)) can be applied when $Z(\omega)$ is higher than the quantum resistance and the T is extremely low [50].

2.3. Single quantum dot (QD)

Next, we consider double junction system which is described as Fig.2.3(a). The coupling of a region, called "island", from the environment which is connected the two junctions become weak and Coulomb blockades can be observed easily. The number of charges in the island is modulated by an integration of other gate electrodes which are capacitive coupled with the island. A single quantum dot (QD) with the tunnel coupled source and drain electrodes, and capacitive coupled gate electrode is used to observe Coulomb blockades experimentally.

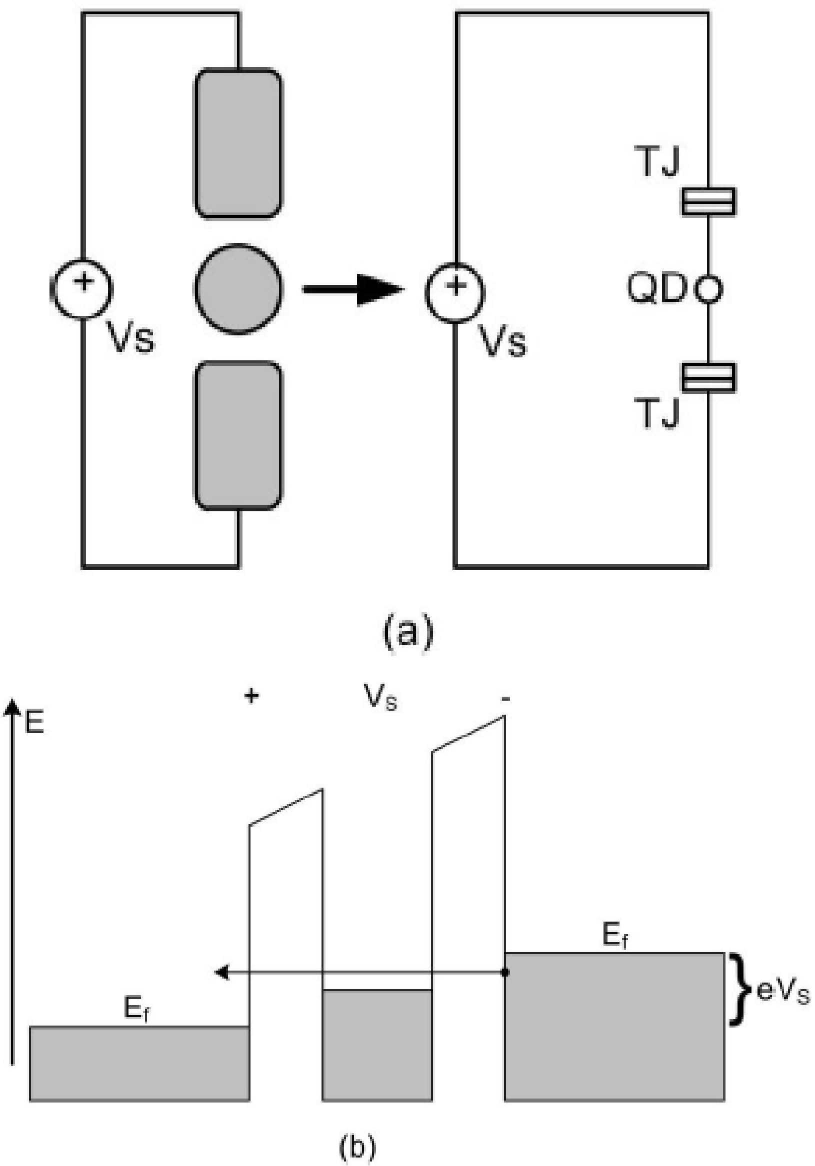


Fig.2.3: (a) Double junction system and equivalent circuit model. (b) Energy diagram of a quantum dot (QD) coupled to leads with voltage V_S.

The accumulated charges in the single QD is

$$Q_1 - C_L(V_1 - V_L) + C_R(V_1 - V_R) + C_g(V_1 - V_g) \Leftrightarrow$$
$$Q_1 + C_L V_L + C_R V_R + C_g V_g = C_1 V_1 \quad . \tag{2.21}$$

when $C_1 = C_L + C_R + C_g$. Also, the electrostatic energy $U(N_1)$ is,

$$U(N_1) = \frac{1}{2} V_1 \cdot C_1 V_1$$
$$= \frac{\left[-(N_1 - N_0)|e| + C_L V_L + C_R V_R + C_g V_g\right]^2}{2C_1} \quad . \tag{2.22}$$

$$
\begin{aligned}
&= \frac{1}{2}(N_1 - N_0)^2 E_{C1}^2 \\
&\qquad - (N_1 - N_0)\left(\frac{C_L}{C_1}|e|V_L + \frac{C_R}{C_1}|e|V_R + \frac{C_g}{C_1}|e|V_g\right) \\
&\qquad + f(V_L, V_R, V_g)
\end{aligned}
$$

when $Q_1 = -(N_1 - N_0)|e|$ (N_0: the number of electrons at initial state, N_1: the number of electrons at stable state), $E_{C1} = |e|^2/C_1$ and $f(V_L, V_R, V_g) = (C_L^2 V_L^2 + C_R^2 V_R^2 + C_g^2 V_g^2 + 2C_L C_R\, V_L V_R + 2C_L C_g\, V_L V_g + 2C_R C_g\, V_R V_g)/2C$. Therefore, the electrochemical potential $\mu(N_1)$ is

$$
\begin{aligned}
\mu(N_1) &\equiv U(N_1) - U(N_1 - 1) \\
&= \left(N_1 - N_0 - \frac{1}{2}\right)E_{C1} - \frac{C_L}{C_1}|e|V_L - \frac{C_R}{C_1}|e|V_R - \frac{C_g}{C_1}|e|V_g \quad . \qquad (2.23)
\end{aligned}
$$

If $V_L = -V_{sd}$ and $V_R = 0$, eq. (2.23)) becomes

$$
\mu(N_1) = \left(N_1 - N_0 - \frac{1}{2}\right)E_{C1} - \frac{C_L}{C_1}|e|V_{sd} - \frac{C_g}{C_1}|e|V_g \quad . \qquad (2.24)
$$

The condition to observe Coulomb blockade with the single quantum dot is derived by a comparison of the electrochemical potential of the electrodes and the dot. When $V_{sd} > 0$, electrons tunnel from left to right, and then, the condition is calculated in the same way as eq. (2.12)) and (2.13)),

$$
\begin{aligned}
&\mu(N_1) > \mu_L \Leftrightarrow \\
&\left(N_1 - N_0 - \frac{1}{2}\right)E_{C1} + \frac{C_L}{C_1}|e|V_{sd} - \frac{C_g}{C_1}|e|V_g > |e|V_{sd} \Leftrightarrow \qquad (2.25) \\
&V_{sd} < \frac{-C_g}{C_R + C_g}V_g + \left(N_1 - N_0 - \frac{1}{2}\right)\frac{|e|}{C_R + C_g} \quad ,
\end{aligned}
$$

and

$$
\begin{aligned}
&\mu(N_1) < \mu_R \Leftrightarrow \\
&\left(N_1 - N_0 - \frac{1}{2}\right)E_{C1} + \frac{C_L}{C_1}|e|V_{sd} - \frac{C_g}{C_1}|e|V_g < 0 \Leftrightarrow \qquad (2.26) \\
&V_{sd} < -\frac{-C_g}{C_L}V_g - \left(N_1 - N_0 - \frac{1}{2}\right)\frac{|e|}{C_L} \quad .
\end{aligned}
$$

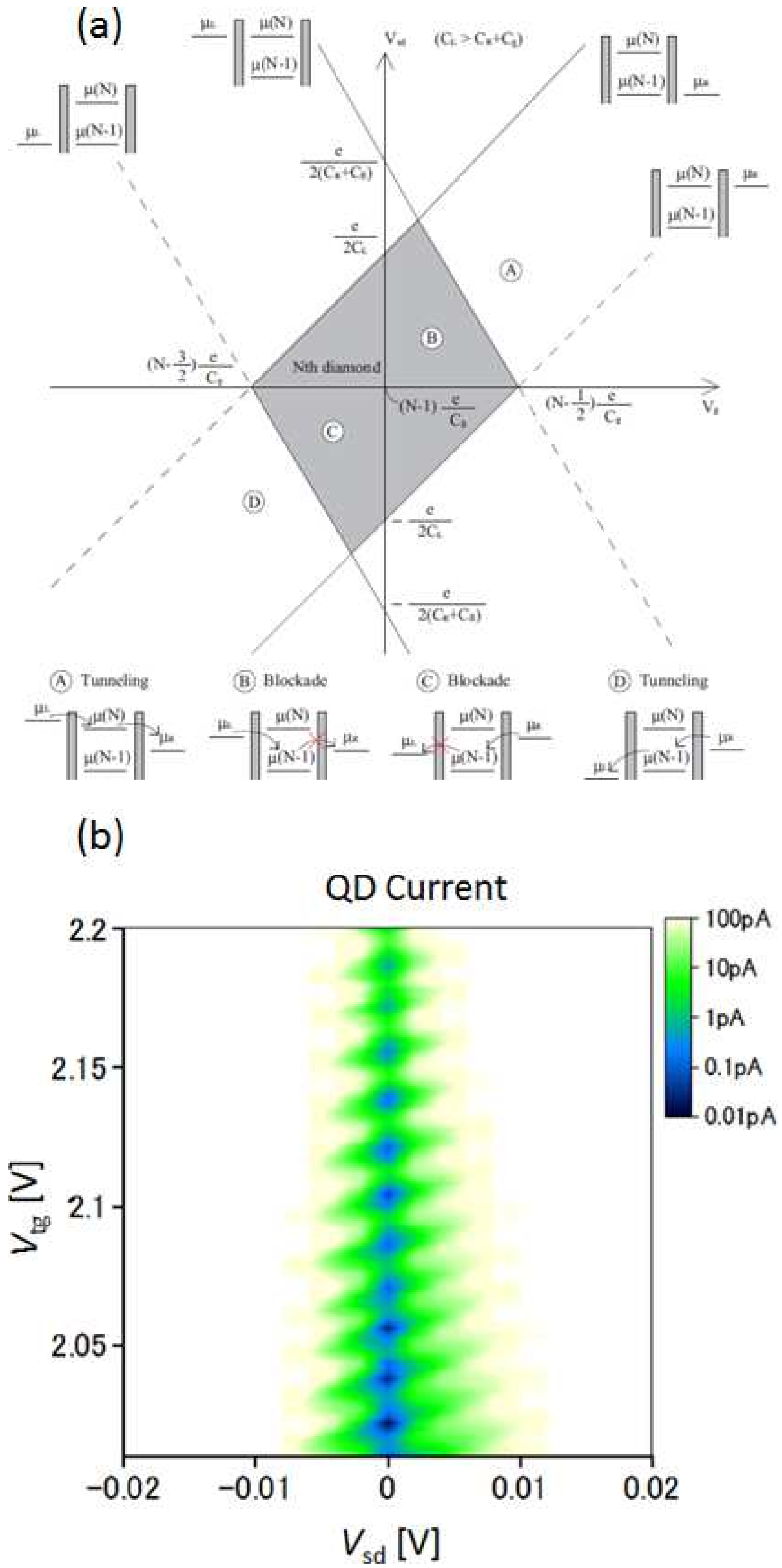


Fig.2.4: (a) Energy diagram of one Coulomb diamond. (b) V_{tg}-V_{sd} characteristics of Si single QD. In black and blue region, QD current is blockade.

When $V_{sd} < 0$, just inequality sign should be reversed because the tunneling is occurred from right to left. This characteristic is drown as Fig.2.4(a) with the schematics of the potentials in the region A, B, C and D and at the each interface. The shape is called “Coulomb Diamond”. Coulomb blockade is occurred in the gray region in Fig.2.4(a) with N electrons. Figure 2.4(b) shows V_{tg}- V_{sd} characteristics of Si single QD. Many diamonds are observed.

When$V_{sd} \approx 0$, characteristic oscillations, which is called as “Coulomb Oscillation”, is observed with sweeping the gate bias [Fig.2.5(a)]. Figure 2.5(b) is an image of scanning electron microscope (SEM) which is used to obtain the I_d- V_g of Fig.2.5(a).

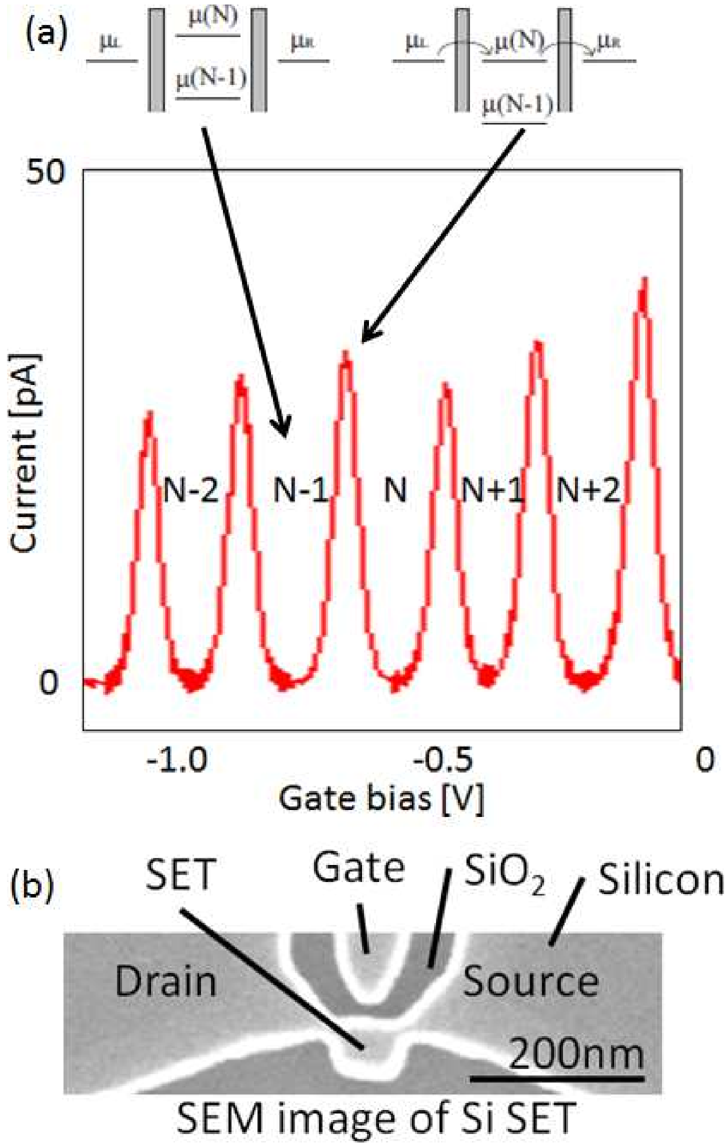


Fig. 2.5 (a): I_d- V_g characteristics and energy levels at Coulomb peak and blockade region. (b): SEM image of lithographically Si SET. Current flows from source and drain electrode, and modified by gate electrode.

The device, which is also called as "Single-Electron Transistor" (SET), like Fig 2.5(b) is widely researched because the current is controlled and switched between ON and OFF state by the gate bias. From eq.(2.23)), the gap between N_1 and N_1+1 peaks in the Coulomb oscillation becomes

$$\mu(N_1;V_g)=\mu(N_1+1;V_g+\Delta V_g)\Leftrightarrow \Delta V_g=\frac{e}{C_g} \quad . \qquad (2.27)$$

The gate capacitance C_g is estimated from the frequency of the Coulomb oscillation. When the source-drain bias and gate bias are constant, the difference of the electrochemical potential by addition of one electron is

$$\mu(N_1+1)-\mu(N_1)=E_{C1} \quad . \qquad (2.28)$$

E_{C1}, called as charging energy, can be also treated as an energy to add N_1+1th electron to the island since N_1th electron comes in.

When two gate electrodes are integrated with the QD [Fig. 2.6], the electrochemical potential $\mu(N_1)$ is represented as follows:

$$\mu(N_1)=\left(N_1-N_0-\frac{1}{2}\right)E_{C1}-\frac{C_{g1}}{C_1}|e|V_{g1}-\frac{C_{g2}}{C_1}|e|V_{g2} \quad , \qquad (2.29)$$

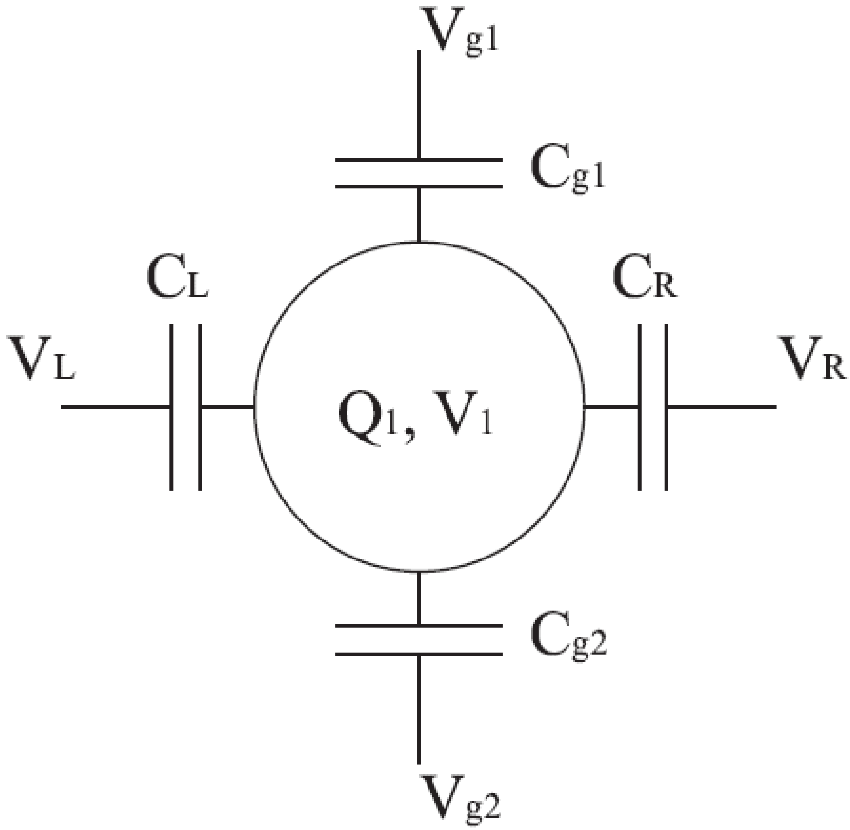


Fig. 2.6: Schematic of double gated SET

with $V_L = V_R \simeq 0$ and $N_0 = 0$ for simplify. If $\mu(N_1) = 0$,

$$V_{g2} = -\frac{C_{g1}}{C_{g2}} V_{g1} + \left(N_1 - \frac{1}{2}\right)\frac{|e|}{C_{g2}} \quad . \tag{2.30}$$

Figure 2.7 shows an electron stability diagram which is calculated from eq.(2.30). The numbers and the black lines are in Fig.2.7 is the number of electrons and the peaks of Coulomb oscillation in the QD. The peak lines are parallel each other.

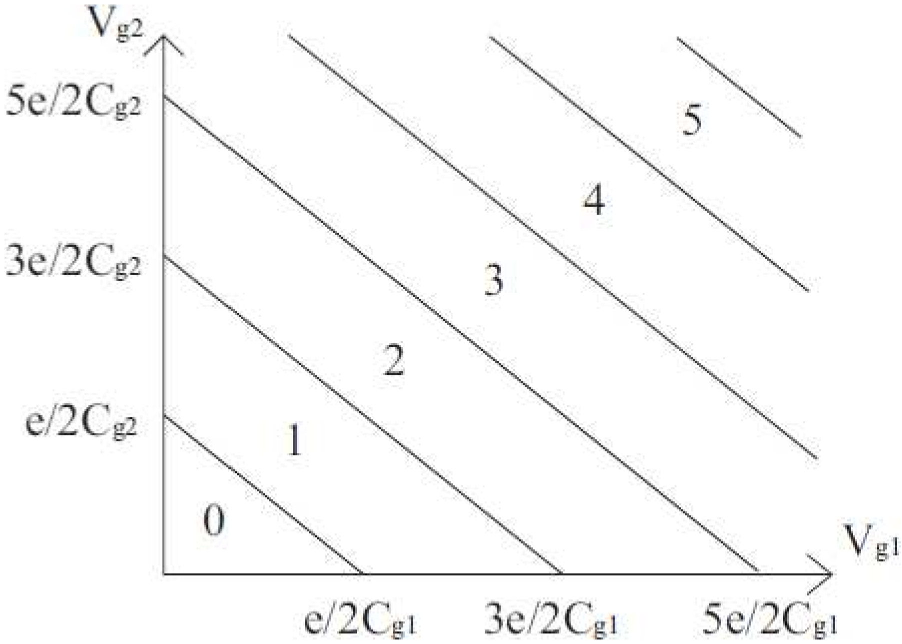


Fig. 2.7: Schematics of Coulomb oscillation with V_{g1} and V_{g2}. The numbers in each area is the number of electrons in the SET.

The discussion above uses classical model with the electron tunneling through the potential barrier. However, de Broglie wave length in semiconductor is larger than that in metal, and then, the energy levels in the QD is drastically quantized by the quantum confinement with the nano-scale device structure. The electrostatic energy with the quantized energy level $U(N_1)$ is calculated as follows:

$$U(N_1) = U^*(N_1) + \sum_{p=1}^{N_1} E_p \quad , \tag{2.31}$$

When $U^*(N_1)$ is the electrostatic energy from classical model and E_p is an energy to occupy pth level. The equation (2.31) derives the electrochemical energy $\mu(N_1)$ as

$$\begin{aligned} \mu(N_1) &= U(N_1) - U(N_1 - 1) \\ &= \mu(N_1) + E_{N1} \end{aligned} \quad . \tag{2.32}$$

The additional energy $\mu(N_1 + 1) - \mu(N_1)$ becomes

$$\mu(N_1+1)-\mu(N_1) = E_{C1} + \left(E_{N_1+1} - E_{N_1}\right) \\ = E_{C1} + \Delta E \quad , \tag{2.33}$$

when ΔE is the gap between the quantized levels. The gate bias to add N_1+1th electron $\Delta V_g = V_{gN_1+1} - V_{gN_1}$ is represented from eqs. (2.23)and (2.33) as follows:

$$\Delta V_g = \frac{e}{C_g} + \frac{C_1}{|e|C_g}\Delta E \quad . \tag{2.34}$$

The quantized level are clearly observed when thermal energy of the system is enough small ($k_B T \ll \Delta E$). When source-drain bias is increased with the fixed gate bias, an extra electron can contribute to the electron transport though the QD [Fig. (2.8)]. Figure 2.8 (a) shows Nth and N+1th ground states GS(N) and GS(N+1), and Nth and N+1th excited states ES(N) and ES(N+1) in the quantum dot. When the relaxation is faster than the tunnel rate through the SET, the transports with ES(N) and ES(N+1) can be observed, then the spectrum of the tunnel current gives informations of the relaxation. Figure 2.8(b) shows an electrostatic potential $\mu(N+1)$ corresponding to Fig. 2.8(a). The potential of $ES(N) \leftrightarrow GS(N+1)$ is smaller than that of $GS(N) \leftrightarrow GS(N+1)$. Figure 2.8 (c) shows the Coulomb diamond with Fig. 2.8(b). Excited lines (yellow and blue) are shown at higher V_{sd} than the edge of diamonds.

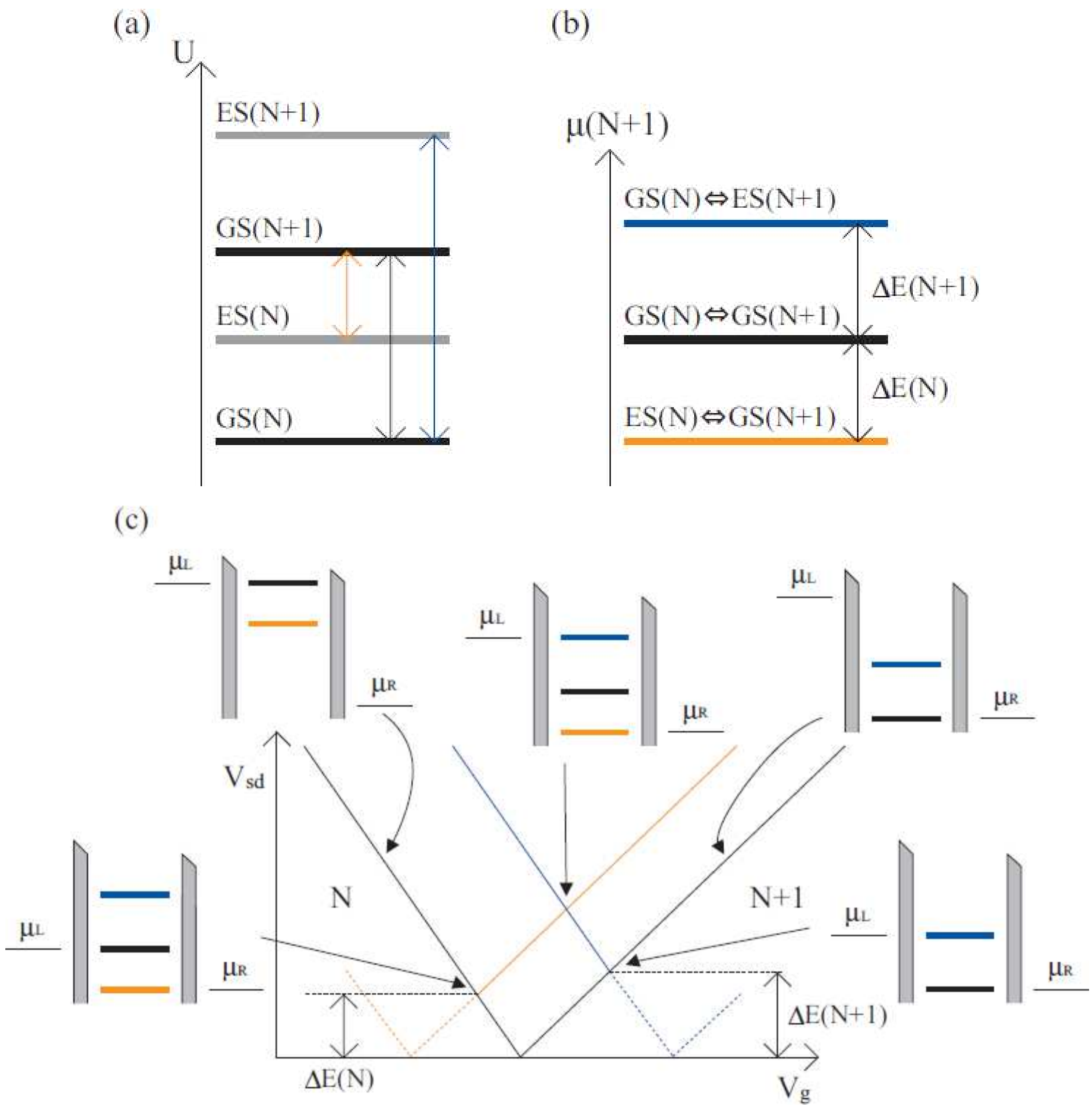


Fig. 2.8: Schematics of Coulomb diamond with excited states

2.4. Double quantum dot in series (DQD)

Similar to the SET, serially-coupled dot is modeled as a network of resistors and capacitors as depicted in Fig. 2.9.

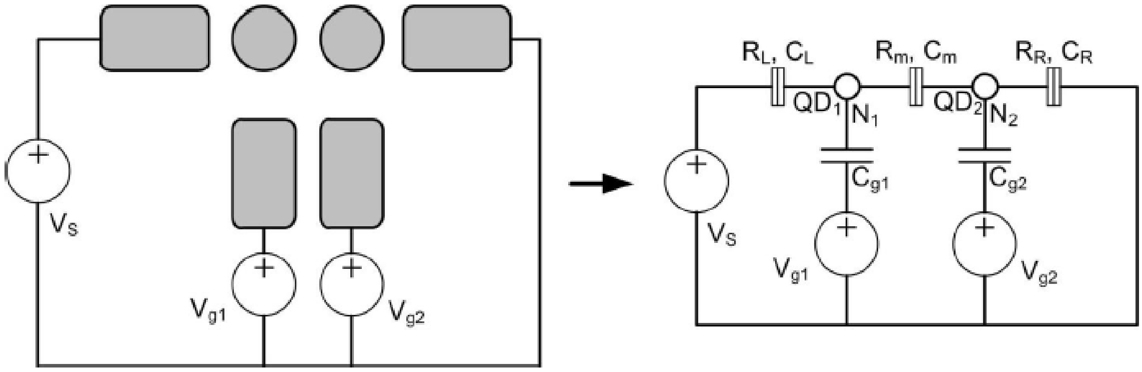


Fig. 2.9: Equivalent circuit model of serially coupled QD as a network of resistors and capacitors

Each dot is capacitively coupled to a gate voltage V_{g1} and V_{g2} through a capacitor C_{g1} and C_{g2}, respectively; and to the source (S) or drain (D) contact through a tunnel barrier represented by a resistor R_L or R_R, and a capacitor C_L or C_R connected in parallel. The dots are coupled to each other by a tunnel barrier, represented by a resistor R_m and a capacitor C_m in parallel. The number of electron in QD_1 and QD_2 is N_1 and N_2, respectively. The bias voltage, V_S is applied to the source contact with the drain contact grounded (asymmetric bias). In this section we consider the linear transport regime, i.e. $V \approx 0$. Assuming the cross-capacitances (such as between Vg1 and QD_2 or vice versa), and other voltage sources and stray capacitances are negligible. The total charge on each dot can be expressed as the sum of charges on all capacitor,

$$\begin{aligned} Q_1 &= C_L(V_1 - V_L) + C_{g1}(V_1 - V_{g1}) + C_m(V_1 - V_2) \\ Q_2 &= C_R(V_2 - V_R) + C_{g2}(V_2 - V_{g2}) + C_m(V_2 - V_1) \end{aligned} \quad . \tag{2.35}$$

The voltage on the charge nodes then

$$\begin{aligned} V_1 &= \frac{C_2(Q_1 + C_L V_L + C_{g1}V_{g1}) + C_m(Q_2 + C_R V_R + C_{g2}V_{g2})}{C_1 C_2 - C_m^2} \\ V_2 &= \frac{C_m(Q_1 + C_L V_L + C_{g1}V_{g1}) + C_1(Q_2 + C_R V_R + C_{g2}V_{g2})}{C_1 C_2 - C_m^2} \end{aligned} \quad . \tag{2.36}$$

Where

$$\begin{aligned} C_1 &= C_L + C_{g1} + C_m \\ C_2 &= C_R + C_{g2} + C_m \end{aligned} \quad . \tag{2.37}$$

For the case $V_L = V_R = 0$, $Q_1 = -N_1$, and $Q_2 = -N_2$, the electrostatic energy of the double dot can be expressed as

$$E_{ES}(N_1, N_2) = \frac{1}{2}N_1^2 E_{C1} + \frac{1}{2}N_2^2 E_{C2} + N_1 N_2 E_{Cm} + f(V_{g1}, V_{g2}) \quad . \tag{2.38}$$

$$f(V_{g1}, V_{g2}) = \frac{1}{-|q_e|}\{C_{g1}V_{g1}(N_1E_{C1} + N_2E_{Cm}) + C_{g2}V_{g2}(N_1E_{Cm} + N_2E_{C2})\}$$
$$+ \frac{1}{q_e^2}\left\{\frac{1}{2}C_{g1}^2V_{g1}^2E_{C1} + \frac{1}{2}C_{g2}^2V_{g2}^2E_{C2} + C_{g1}V_{g1}C_{g2}V_{g2}E_{Cm}\right\}$$

Here, E_{C1} and E_{C2} is the charging energy of the QD_1 and QD_2, respectively; and E_{Cm} is the electrostatic coupling energy, which is the change in the energy of one dot when an electron is added to the other dot. In terms of capacitance, these energies can be expressed as

$$E_{C1} = \frac{q_e^2}{C_1}\left(\frac{1}{1-\frac{C_m^2}{C_1C_2}}\right), E_{C2} = \frac{q_e^2}{C_2}\left(\frac{1}{1-\frac{C_m^2}{C_1C_2}}\right), E_{Cm} = \frac{q_e^2}{C_1}\left(\frac{1}{\frac{C_1C_2}{C_m^2}-1}\right) \quad . \qquad (2.39)$$

C_1 and C_2 is the sum of all capacitances attached to QD_1 and QD_2, respectively. When C_{Cm}= 0 and hence E_{Cm} = 0, eq. (2.38)) reduced to

$$E_{ES}(N_1, N_2) = \frac{\left(-N_1|q_e| + C_{g1}V_{g1}\right)^2}{2C_1} + \frac{\left(-N_2|q_e| + C_{g2}V_{g2}\right)^2}{2C_2} \quad , \qquad (2.40)$$

which is the sum of the energies of two independent dots. In case of a strongly coupled DQD, C_m become dominant as $\frac{C_m}{C_{1,2}} \to 1$, the electrostatic energy is given by

$$E_{ES}(N_1, N_2) = \frac{\left[-(N_1 + N_2)|q_e| + C_{g1}V_{g1} + C_{g2}V_{g2}\right]^2}{2(C_1 + C_2 - 2C_m)} \quad , \qquad (2.41)$$

In this case, strong coupling between the DQD leads to one big dot. The electrochemical potential is defined as the energy needed to add the Nth electron to a dot, while having N electrons on the dot. Using the expression of total energy eq. (2.38), the electrochemical potentials of the dots are

$$\mu_1(N_1, N_2) = \left(N_1 - \frac{1}{2}\right)E_{C1} + N_2E_{Cm} - \frac{1}{|q_e|}\left(C_{g1}V_{g1}E_{C1} + C_{g2}V_{g2}E_{Cm}\right) \quad , \qquad (2.42)$$

$$\mu_2(N_1, N_2) = \left(N_2 - \frac{1}{2}\right)E_{C2} + N_1E_{Cm} - \frac{1}{|q_e|}\left(C_{g2}V_{g2}E_{C2} + C_{g1}V_{g1}E_{Cm}\right) \quad , \qquad (2.43)$$

The change in $\mu_1(N_1, N_2)$at fixed gate voltages, N_1 is changed by one, $\mu_1(N_1 + 1, N_2) - \mu_1(N_1, N_2) = E_{C1}$, is called the addition energy of QD_1, and similarly for QD_2.

From the electrochemical potentials in eqs. (2.42) and (2.43), we can construct a charge stability diagram, giving the equilibrium electron number N_1 and N_2 as a function of V_{g1} and V_{g2}. We define the electrochemical potentials of the left and right leads to be zero if no bias voltage is applied, $\mu_L = \mu_R = 0$. Hence, the equilibrium charges on the dots are the largest values of N_1 and N_2 for which both $\mu_1(N_1, N_2)$ and $\mu_2(N_1, N_2)$ are less then zero. If either is larger than zero, electrons escape to the leads.

For completely uncoupled dot, the diagram looks as in Fig. 2.10 (a). If the coupling between the DQD is increased, the domains become hexagonal as shown in Fig. 2.10 (b), while if the coupling is strong, the triple point separation become maximum as depicted in Fig. 2.10 (c). In this case, the DQD behaves as a single big dot with total charge $N = N_1 + N_2$. In Fig. 2.11, two kind of such triple points are distinguished, (•) and (o), corresponding to different charge transfer process. At triple point (•), the dots cycle through the sequence $(N_1, N_2) \rightarrow (N_1 + 1, N_2) \rightarrow (N_1, N_2 + 1) \rightarrow (N_1, N_2)$ while at triple point (o) the dots cycle through sequence $(N_1 + 1, N_2 + 1) \rightarrow (N_1 + 1, N_2) \rightarrow (N_1, N_2 + 1) \rightarrow (N_1 + 1, N_2 + 1)$.

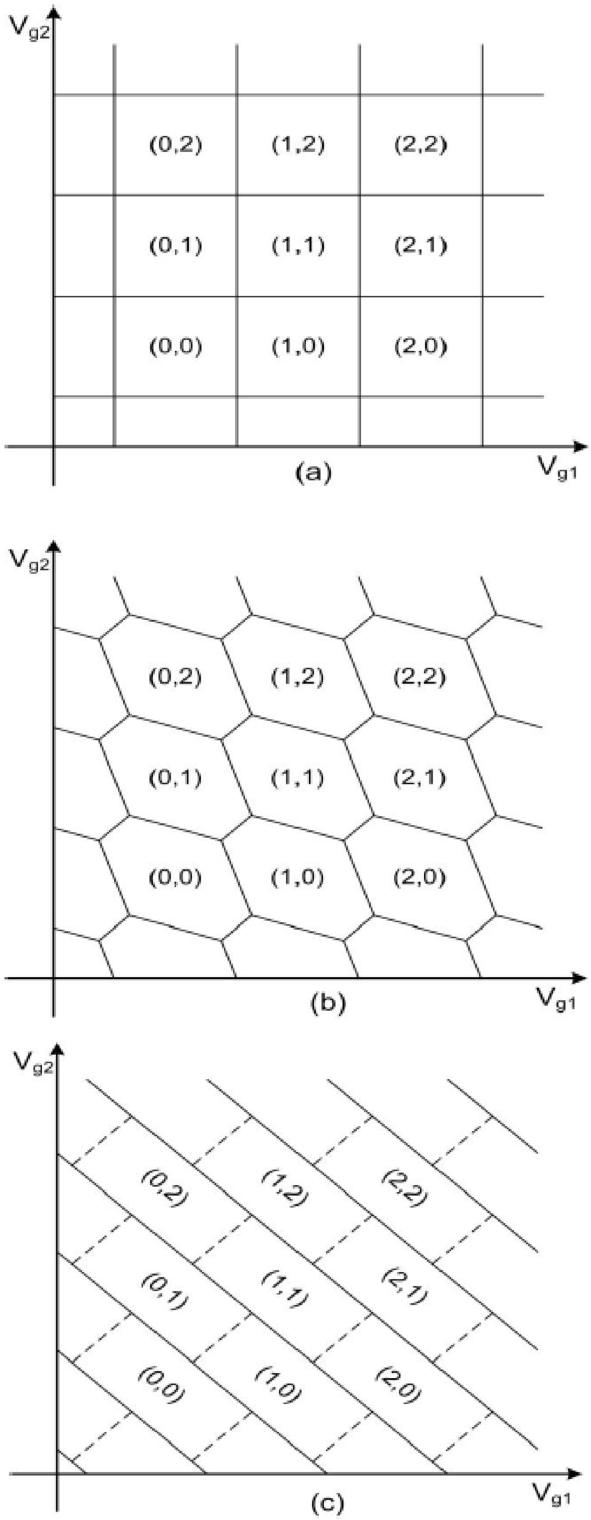


Fig. 2.10: Schematic stability diagram of the double-dot system for (a) small, (b)intermediate, and (c) large inter-dot coupling. The equilibrium charge on each dot in each domain is denoted by (N_1,N_2).

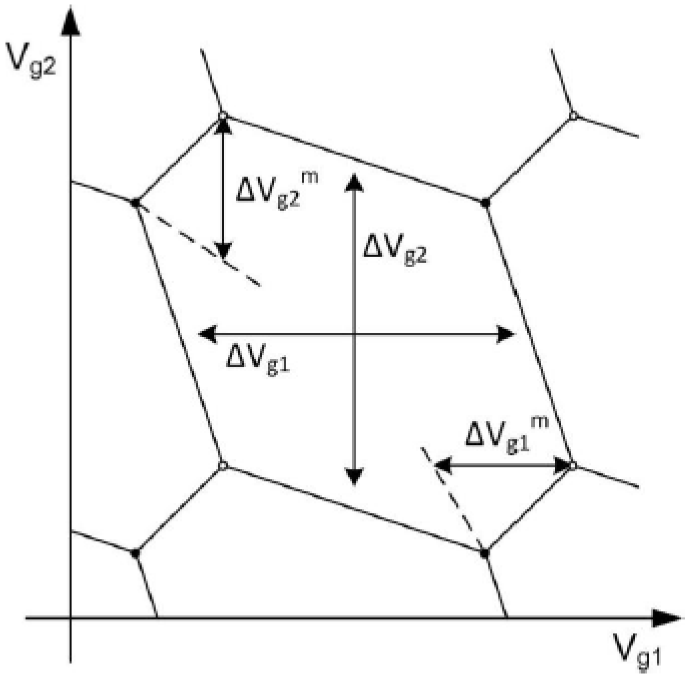


Fig. 2.11: Schematic stability diagram showing the Coulomb peak spacing given in eqs. (2.44) and (2.45). These spacing can be determined experimentally by connecting the triple-points

The dimension of the honeycomb cell can be related to the capacitances using (2.64), and we can obtain

$$\Delta V_{g1} = \frac{|q_e|}{C_{g1}}, \Delta \mathrm{V}_{\mathrm{g2}} = \frac{|q_e|}{C_{g2}} \qquad , \qquad (2.44)$$

$$\Delta V_{g1}^{m} = \frac{|q_e| C_m}{C_{g1} C_{g2}} = \Delta \mathrm{V}_{\mathrm{g1}} \frac{C_m}{C_{g2}}, \Delta V_{g2}^{m} = \frac{|q_e| C_m}{C_{g2} C_{g1}} = \Delta \mathrm{V}_{\mathrm{g2}} \frac{C_m}{C_{g1}} \qquad , \qquad (2.45)$$

2.5. Principle of electron spin resonance (ESR)

ESR is a method to control electron spin with resonance between the electron spin and electromagnetic waves. When a static magnetic field is applied to QDs, the electron spin degeneracy in the QD is lifted and the electron absorbs or emits photons of energy differences from micro wave. That is why ESR is occurred in the QD.

Separation of spin degeneracy level by a magnetic field

When configuring a magnet with magnetization M in a magnetic field with magnetic flux density B_0, the magnetic energy ε will be

$$\varepsilon = -\boldsymbol{M} \cdot \boldsymbol{B}_0 \qquad , \qquad (2.46)$$

$$= -MB_0 \cos\theta$$

θ is the angle formed by magnetization M and magnetic flux density B_0. The electrons have magnetic moment μ_S complying with spin angular momentum, while they also have magnetic moment μ_L according to their orbital angular momentum in an atom and a molecule. Since magnetization M is the summation of magnetic moment μ that exists in a unit volume, the energy of magnetic moment μ can be calculated with M replaced by μ in the equation (2.46).

Spin magnetic moment $\hat{\mu}_S$ can be calculated with operator of electron spin angular momentum $\hat{s}$ as follows:

$$\hat{\mu}_S = -g_e \mu_B \widehat{\boldsymbol{S}} \quad , \tag{2.47}$$

g_e is an invariable called g factor of an electron. Without relativistic corrections, g_e = 2, and with relativistic corrections, g_e = 2.0023193. μ_B is called Bohr magneton, and is a unit of magnetic moment of an electron. The size of μ_B is

$$\mu_B = \frac{e\hbar}{2m_e} \tag{2.48}$$
$$= 9.2740154 \times 10^{-24}\ \mathrm{JT^{-1}} \quad ,$$

Thus, Hamiltonian $\widehat{H}_{SH}$ indicating interaction between electron spin and a magnetic field will be

$$\widehat{H}_{SH} = -g_e \mu_B \hat{s} \cdot B_0 \quad . \tag{2.49}$$

Electron spin has spin quantum number s = 1/2, and spin magnetic quantum number m_s, which determines its component z, could take ±1/2. Provided spin eigenfunction to be $|\alpha\rangle = |s = 1/2, m_s = +1/2\rangle$, $|\beta\rangle = |s = 1/2, m_s = -1/2\rangle$, eigenvalue of these equations will be +1/2, -1/2 (Please note that the unit here is $\hbar$). Hence, when component z of spin angular momentum operator interacts with $|\alpha\rangle, |\beta\rangle$, we have

$$\widehat{s_z}|\alpha\rangle = \left(+\frac{1}{2}\right)|\alpha\rangle \quad , \tag{2.50}$$

$$\widehat{s_z}|\beta\rangle = \left(+\frac{1}{2}\right)|\beta\rangle \quad . \tag{2.51}$$

Applying B_0 of the component z of $\hat{S}_Z$ and B_0, the equation (2.48) can be read

$$\widehat{H}_{SH} = -g_e \mu_B \widehat{S}_z B_0 \quad , \tag{2.52}$$

Based on the equation (2.49), (2.50), and (2.51), energy eigenvalue ε in the above equation (2.52) will be

$$\varepsilon_\alpha = \langle\alpha|\widehat{H}_{SH}|\alpha\rangle$$
$$= \left(+\frac{1}{2}\right) g_e \mu_B B_0 \quad , \tag{2.53}$$

$$\varepsilon_\beta = \langle \beta | \hat{H}_{SH} | \beta \rangle = \left(-\frac{1}{2}\right) g_e \mu_B B_0 \quad . \tag{2.54}$$

Therefore, energy splitting Δε caused by magnetic field B_0 equals to

$$\delta\varepsilon = |\varepsilon_\alpha - \varepsilon_\beta| = g_e \mu_B B_0 \quad . \tag{2.55}$$

Suppose frequency of the absorbed ray (electromagnetic wave) to be ν, we get

$$h\nu = g_e \mu_B B_0 \quad . \tag{2.56}$$

The equation (2.56) is called the Resonance Condition Equation. As mentioned in the beginning, this only applies to free electrons, and the resonance condition equation within a material will be more complex.

Selection rules of magnetic dipole transition

Electron spin transits between two levels, absorbing and releasing oscillating magnetic field B_1 (micro wave), which is shown in eq. (2.56). Now I will discuss the selection rule of direction and transition of oscillating magnetic field. All the transition is magnetic dipole transition regarding ESR. Hence, transition probability is calculated with transition spin Hamiltonian of magnetic dipole transition

$$\widehat{H_1} = -\mu \cdot B_1 = -B_1 \hat{\mu}_{B1} \quad , \tag{2.57}$$

μ indicates all the magnetic moment including electron spin. $\mu_B 1$ shows the B_1 component of μ. When beginning with $|\phi_0\rangle$, with the final state of $|\phi_1\rangle$, probability of magnetic dipole transition is viewed as $\left|\langle \phi_0 | \hat{H}_1 | \phi_1 \rangle\right|^2$ (squae of the transition moment). We suppose here that the beginning and the final state to be $|\phi_0\rangle = m_S, m_I\rangle$ and $|\phi_1\rangle = |m_S', m_I'\rangle$ respectively, including magnetic quantum number of nuclear spin. When B1 and B0 are orthogonal as in regular ESR set-ups, $\hat{H}_1 = -\mu \cdot B_1 = -B_1 \hat{\mu}_{B1} = g_e \mu_B B_1 \hat{S}_x$. S means spin composed. Transition moment becomes as follows, on condition that $B_1 \parallel x$:

$$\begin{aligned} &\langle \phi_0 | \hat{H}_1 | \phi_1 \rangle \\ &= \langle m_S, m_I | \hat{H}_1 | m_S', m_I' \rangle \\ &= g_e \mu_B B_1 \langle m_S, m_I | \hat{S}_x | m_S', m_I' \rangle \\ &= g_e \mu_B B_1 \langle m_S | \hat{S}_x | m_S' \rangle \langle m_I | m_I' \rangle \quad . \end{aligned} \tag{2.58}$$

Only when $m_S' = m_S \pm 1, m_I' = m_I$, the equation (2.58) becomes unequal to 0. $B_1 \perp B_0$ also applies to this experiment.

Spin Hamiltonian

The equation (2.56) is only valid i_{th} free electrons. Electrons, however, is subjected to various interactions within a material. The equation can be established with spin component being perturbations, as in (2.59).

$$\hat{H} = \hat{H}_0 + H\hat{}' \quad , \quad (2.59)$$

$\hat{H}'$ is the Hamiltonian of the spin component. Suppose that wave function without the perturbations being $|\Psi\rangle = |\psi_{\mathrm{Ln}}\psi_S\rangle$ times trajectory component multiplied by spin component, and the eigen energy being $\varepsilon_n^{(0)}$. Under the premise, basic energy with perturbation ε_0 and spin-type energy without trajectory component ε_S can be formulated as follows, when we use as much as the secondary perturbation term.

$$\begin{aligned}\varepsilon_S &= \varepsilon_0 - \varepsilon_0^{(0)} \\ &= \langle\Psi_0|\hat{H}'|\Psi_0\rangle - \sum_{\mathrm{n}\neq 0}\frac{\langle\Psi_0|\hat{H}'|\Psi_n\rangle\langle\Psi_n|\hat{H}'|\Psi_0\rangle}{\varepsilon_n^{(0)} - \varepsilon_0^{(0)}} \quad ,\end{aligned} \quad (2.60)$$

Formula (2.60) can also be written as $\langle\psi_S|\hat{H}_S|\psi_S\rangle$, when integrating the trajectory component alone. As a result, the new Hamiltonian ˆHS can be calculated as follows:

$$\hat{H}_S = \langle\Psi_{L0}|\hat{H}'|\Psi_{L0}\rangle - \sum_{\mathrm{n}\neq 0}\frac{\langle\Psi_{L0}|\hat{H}'|\Psi_{Ln}\rangle\langle\Psi_{Ln}|\hat{H}'|\Psi_{L0}\rangle}{\varepsilon_n^{(0)} - \varepsilon_0^{(0)}} \quad , \quad (2.61)$$

$$\hat{H}_S|\psi_{S0}\rangle = \varepsilon_S\psi_{S0} \quad . \quad (2.62)$$

Here $\hat{H}_s$ is called effective spin Hamiltonian. ψ_{S0} is spin wave function in the ground state. Effective spin Hamiltonian takes in the wave function of the trajectory component as an expectation value of location r and as an expectation value of angular momentum L.

Overall Hamiltonian can be broken down into the equation (2.63))

$$\hat{H} = \hat{H}_{el} + \hat{H}_{cr} + \hat{H}_{LS} + \hat{H}_{ex} + \hat{H}_{SS} + \hat{H}_{Ze} + \hat{H}_{hf} + \hat{H}_{Zn} + \hat{H}_{II} + \hat{H}_Q \quad , \quad (2.63)$$

$\hat{H}_{el}$ is Hamiltonian that can be calculated by adding kinetic energy of an electron to Coulomb potential energy. $\hat{H}$ indicates, for instance, Coulomb potential from neighboring atoms which surround the central atom.

$\hat{H}_{ex}$ indicates exchange interaction. This appears when two unpaired electrons are closed by. Even if electron 1 and electron 2 have changed places, it cannot be distinguished from the earlier state. That is why the conditions before and after the exchange appears to be degenerating. When we take the Coulomb interaction between two electrons into account, the degeneracy disappears to be separated to 2 states. One of them degenerates to 3 layers and the total of electron 1 and 2 is in the state 1 (triplet). The other does not degenerate and the total spin comes to the state of 0 (singlet). Energy of spin triplet will be smaller than that of the singlet. Apparently, exchange interaction can be handled as interaction between spin and spin.

$$\hat{H}_{ex} = -2JS_1 \cdot S_2 \quad , \quad (2.64)$$

$2J$ is the energy difference between singlet and triplet. $\hat{H}_{LS}$ represents spin obit interaction, $\hat{H}_{Ze}$ indicates Zeeman interaction of an electron, and $\hat{H}_{SS}$ is spin-spin interaction. Each of them can be found as in the followings:

$$\widehat{H}_{LS} = -\lambda\hat{L}\cdot\hat{S} \quad , \tag{2.65}$$

$$\widehat{H}_{Ze} = -\mu_B\left(\hat{L} + g_e\hat{S}\cdot B_0\right) \quad , \tag{2.66}$$

$$\widehat{H}_{SS} = \hat{S}\cdot D\cdot\hat{S} \quad , \tag{2.67}$$

D represents tensor. If we replace spin orbit interaction and Zeeman interaction with spin Hamiltonian by regarding both interactions as perturbations, we get

$$\mu_B\hat{S}\cdot g\cdot B_0 + \hat{S}\cdot D\cdot\hat{S} \quad . \tag{2.68}$$

Value g, which is proportional to magnetic flux density will become tensor g, bringing anisotropy to Zeeman term, which corresponds to magnetic flux density B. Then, the secondary term gets to have the same configuration as spin-spin interaction. $\hat{S}\cdot D\cdot\hat{S}$ will appear when $S \geq 1$, and separates the levels without having an external magnetic field. Specifically speaking, paramagnetic term unaffected by temperature change exists. It, however, gives only little effect to spin energy, and will not be taken into account here.

$\widehat{H}_{hf}$ is called hyperfine interaction, or hf, which indicates interaction between electron spin and nuclear spin. When put into spin Hamilton, it reads

$$\widehat{H}_{hf} = \hat{S}\cdot A\cdot\hat{I} \quad , \tag{2.69}$$

on condition that

$$A = A_{dip} + A_0 1 \quad , \tag{2.70}$$

A here is tensor and is called hyperfine coupling constant. A tensor can be divided into anisotropic term A_{dip} and isotropic term $A_0 1$ (1 = unit matrix). Anisotropic term A_{dip} is called dipolar term. Isotropic term $A_0 1$ appears when the wave function spreads through to nucleus location $r = 0$, namely, when $\psi \neq 0$.

$\widehat{H}_{Zn}$ represents nuclear Zeeman term, $\widehat{H}_{II}$ implies nuclear spin-nuclear spin magnetic dipolar interaction, and $\widehat{H}_{Q}$ is called nuclear quadruple interaction.

Chapter 3: Experimental Techniques

Abstract

In this chapter, equipment and process conditions for device fabrication are introduced. Cleanliness of the equipment and the order of the process have a huge effect to the electron transport characteristics of the QDs device in semiconductor nanofabrication, especially in silicon.

3.1. Introduction

Fabrication of nano-scale Silicon devices is complicated process. The major steps in the fabrication of Silicon QDs devices are thermal oxidation, lithography, dry etching, insulator and top gate deposition, ion implantation and metal deposition. The fabrication process of devices is adjusted and modified for different purposes. In this chapter, the details for device fabrication will be described in each section concerning each different experimental purpose.

3.2. Device fabrication techniques

3.2.1. Substrate cleaning

Substrate cleaning is one of most important process for silicon devices. If dusts ore contamimations are remaind in the sample, the silicon device process will not exactly works. Therefore, the first process is always wafer cleaning. The wafer cleaning process is described below.

1. Ultrasonication in pure water to remove large dusts and particles (1 min)
2. $H_2SO_4 : H_2O_2 = 1 : 1$ (SPM 1:1) to remove organic contamination (120 °C, 10 min)
3. Pure water flowing to remove SPM 1:1 (5 min)
4. $NH_3 : H_2O_2 : H_2O = 1 : 5 : 27$ (SC1) to remove Silicon particle with slow wet etching (150 °C, 10 min)
5. Pure water flowing to remove SC1 (5 min)
6. 1.5 % HF to remove surface SiO_2 (3 min)
7. Pure water flowing to remove HF (30 s)
8. $HCl : H_2O_2 : H_2O = 1 : 1 : 5$ (SC2) to remove metal contaminatins (150 °C, 10 min)
9. Pure water flowing to remove SC2 (5 min)

Ratio of SPM 1:1 is changed 3:1 when photo or electron beam resist is remained on the surface and SC1 and its rense processes are skipped when the cleaning is not after initial wafer cut because SC1 etchs the sample surface slowly.

3.2.2. Thermal oxidation

During the thermal process, thermal uniformity is important to obtain good reproducibility and good uniformity to each sample. Figure 3.1 shows the schematic image of thermal oxidation furnace. To get uniform temperature distribution, this furnace is separated to three zones. Each zone has a heater controlled by the thermo controller depending on the temperature measured by each thermo couple. The sample are put on the quartz plate vertically and loaded into the furnace. By this equipment, N2 and O2 gases are available. In this study, O2 gas is used for oxidation, and N2 gas is used for drive in and recrystallization.

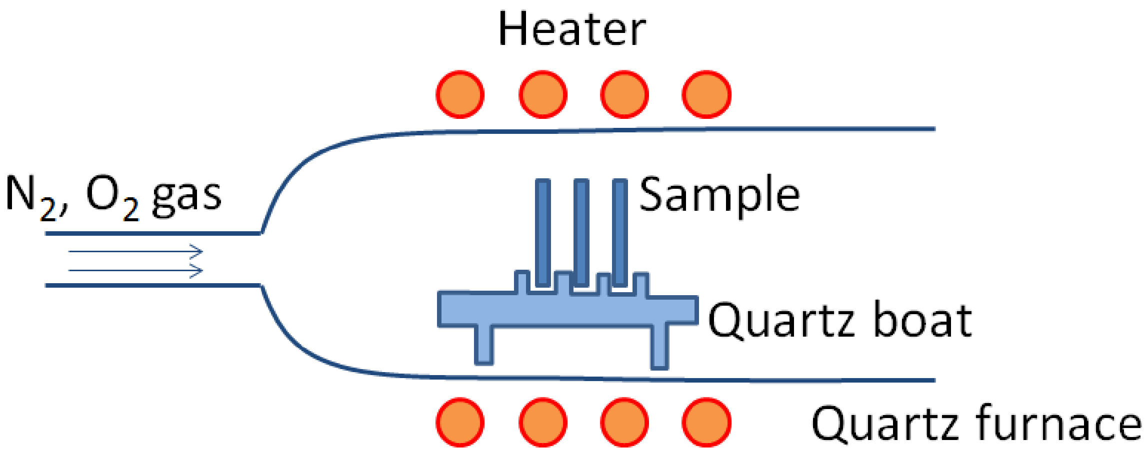


Fig. 3.1: schematics of thermal oxidation furnace

Figure 3.2 shows the thermal oxidation system. The clean level of the furnace is also important to make clean Silicon dioxide without contamination. Once contamination (expecially metal) is heated in the furnace, the contamination diffuses to the furnace from the sample or quartz boat, and then, all samples after that will be affected the contamination. Therefore, the thermal oxidation process shold be operated carefully and be checked the furnace is kept clean.

Fig. 3.2: Image of the thermal oxication system

3.2.3. Electron beam lithography (EBL)

3.2.3.1. Introduction

Electron beam lithography (EBL) provides a mean to reduce image resolution below 100 nm by using accelerated electrons instead of photons. Electron, like photon, has particle and wave properties. When electrons accelerate, the wave length is acquired by the electron can be approximated by [51]

$$\lambda = \frac{1.23}{\sqrt{V}} \quad , \tag{3.1}$$

where λ is in nm and V is the accelerating voltage in Volts. Hence, for electrons accelerated at 50 kV the equivalent wavelength will be 0.0055 nm, several orders of magnitude smaller than that of wavelength of ultraviolet light. Moreover accelerated electrons can be focused to a spot size of few nm in diameter and easily deflected by electrostatic or electromagnetic fields. For these regions accelerated electron beams are widely used for sub-micron imaging such as scanning electron microscopy and transmission electron microscopy. EBL is very similar to the scanning electron microscopy. Scanning electron microscopy is to observe some images. On the other hand, EBL system is to write some images in the resist layer. The advantage of EBL is the achievement of minimum feature size of ≤ 10 nm and a pattern positioning accuracy of ≤ 50 nm. However, due to its low throughput this system cannot use in large-scale device fabrication with the highest its resolution.

3.2.3.2. Electron beam exposure system: JBX-6300

The electron beam exposure system is one of most important fabrication equipment to form Silicon DQD. Table 3.1 shows main spec of JBX-6300. Because of small beam size and high field position accuracy, < 10nm pattern can be drown. Figure 3.3 shows an image of JBX-6300 and Fig. 3.4 shows schematic of the optics system. Many parameters are optimized for best performance.

Table 3.1: Main spec of JBX-6300

Electron gun	ZrO/W
Accelerate voltage	25 kV / **50 kV** / 100 kV
Beam current	30 pA ~ 20 nA
Beam size	> 8 nm / > 5 nm / > 2 nm
Field position accuracy	0.6 nm
Drawing area	150 mm × 150 mm

Fig. 3.3: Image of JBX-6300

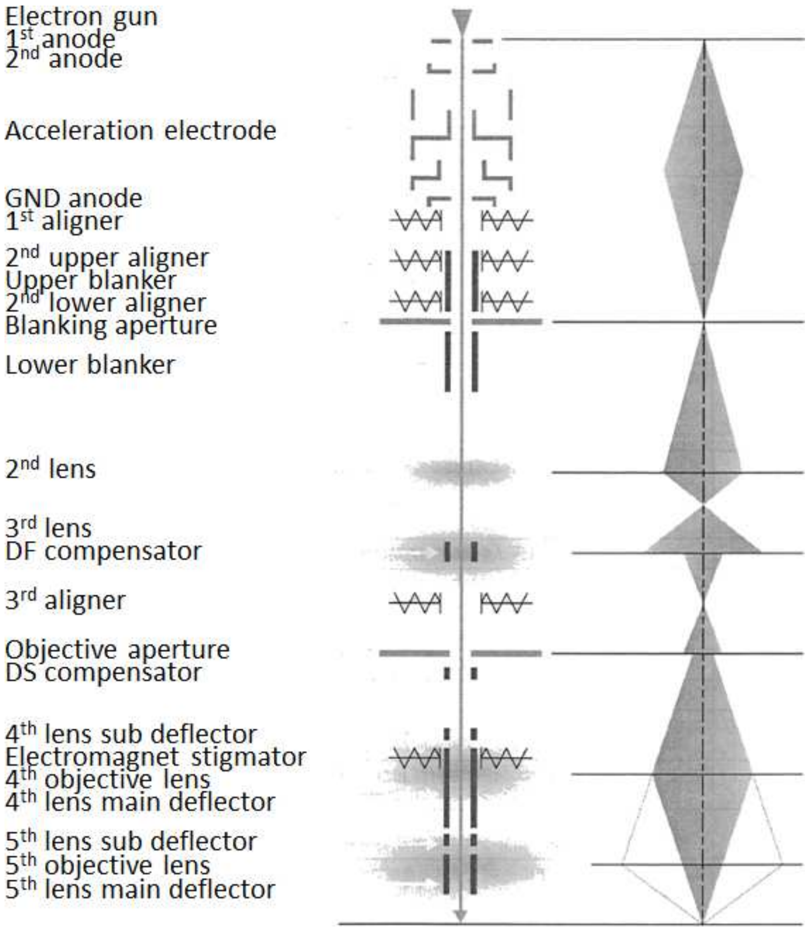


Fig. 3.4: Optics system of JBX-6300

3.2.3.3. Proximity effect

Unlike optical lithography, in case of electron beam lithography the minimum feature size is not limited by diffraction limit. However, there are other parameters which restrict the resolution of EBL, notably forward scattering of electrons in the resist layer and back scattering of electrons from substrate. Fig. 3.4 shows the schematic image of forward scattering and back scattering when electron beam is traveled through the resist layer by collisions with different atoms in the resist layer. An elastic collision causes electron to deviate from their incident direction, while inelastic collisions results in loss of electron energy. Electron beam broaden after touch to one point on resist layer. This effect is called forward scattering. On the other hand, some electrons are scattered of over ninety degree in resist or substrate layer and then go back to the direction to return. This effect is called back scattering. The forward scattering is negligible for thin resist layer (100 nm) at higher acceleration voltages (50 keV). However, at high beam voltages the range of secondary electrons varies from few microns to few tens of microns. It is important to use high voltage energy beam and thin resist layer for reduction of the effect of forward scattering and back scattering.

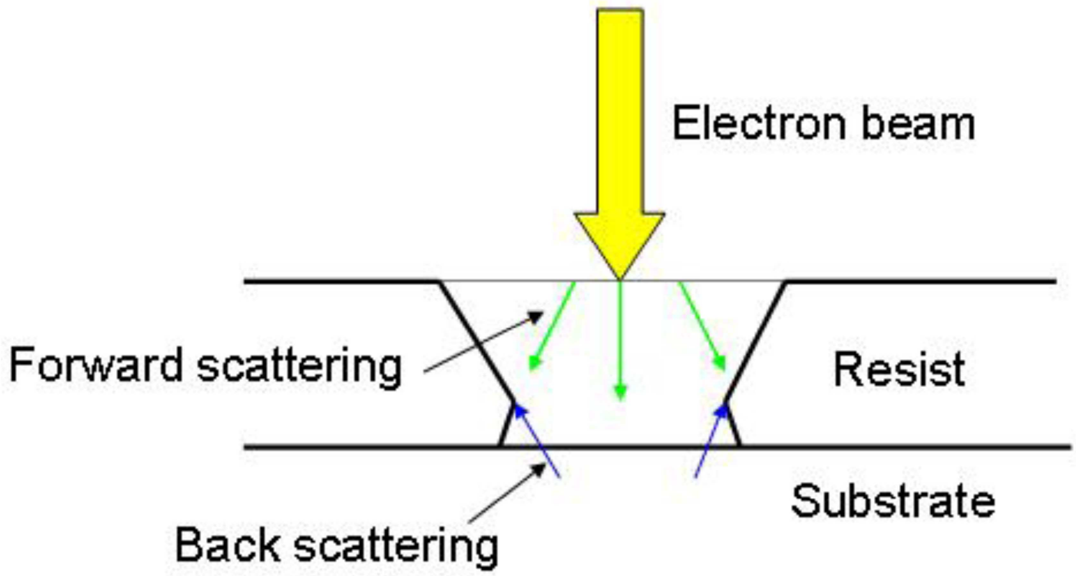


Fig. 3.5: schematic of proximity effect

3.2.4.Dry etching

Dry etching is also importatnt fabrication process for lithographically-defined QDs devices. There are kinds of dry etching, however we explain only reactive ion etching (RIE) which is used for this work. RIE equipment etchs Silicon anisotropically and has good etching ratio of resist and Silicon, then nano-scale pattern can be formd.

To etch anisotropically, we use Cl_2 and SF_6 gases are used. The RIE system with Cl_2 is in charge of Tsutsui Lab.. Cl_2 gas emits volatile by-product, and then, surface cleaning such as O_2 ashing is not necessary after etching. However, many materials included in metals are etched by other labratories with the RIE, the anisotoropy is not stable. The instability may cause fluctuation of the QDs pattern. On the other, SF_6 gas emits non-volatile by-product with Silicon etching, then O_2 ashing is necessary to remove it. However, the RIE equipment is used only for Silicon etching, the ratio and anisotropy is probably stable. Figure 3.5 shows one of RIE system which is in charge of Misumoto Lab..

Fig. 3.6: Image of RIE system with SF_6 gas

3.2.5.Metal deposition

3.2.5.1. Introduction

Metal deposition for devices was performed by mask lift-off process. In this process a resist mask is dissolved in some adequate solvent (acetone was used in this work). As a result the metal on top of the resist mask gets lifted off. Lift-off was used for fabrication of electrode.

The resist mask was prepared by EBL or photolithography. The thicknesses of metals are 90 nm - 300 nm. To make sure of the success of lift off process, the thickness of metal should be less than 50 percentage of the thickness of the resist. After metal deposition samples were kept in acetone to perform lift-off.

3.2.5.2. Electron beam (EB) evaporator

There are two kinds of equipment can be used for metal materials deposition. One is thermal evaporator, which are used for deposition of metallic thin film for electrodes. The thermal evaporator is easy to deposit Aluminum, however it is not best system to deposit fine metal pattern because of a distortion of the resist by high temperature from the source. The other one is EB evaporator, which is used to deposit many kinds of metals, such as Al, Co, Au and other refractory metals under a very high vacuum condition. The equipment usually has thickness monitors. In addition, more than two kinds of metals such as Co and Au can be deposited subsequently without load sample out from the vacuum chamber. The deposition rate highly depends on the values of current. EB gun for evaporation has different shape from the standard EB gun. To keep away from evaporated material flow, EB is emitted from below the hearth and passes through the magnetic field. This EB is bended to the hearth by magnetic field and hits to the source materials on the hearth. The source materials are heated and evaporated by this EB.

Figures 3.7 and 3.8 show the image and schematic of the EB evaporator. In this equipment, load lock chamber is attached on the evaporation chamber separated by gate valve. The pumps of the load lock chamber are turbo molecular pump (TMP) and rotary pump (RP). Evaporation chamber is vacuumed by another TMP and another RP and ultimate vacuum is about 1×10^{-6} Pa. Three kinds of materials can be set on the hearth liner with this EB gun, and the target materials are heated by electron beam emitted by EB gun (CANON ANELVA Corp., Co., LTD., XTM/2) attached around the sample holder. This thickness monitor is quartz transducer type monitor using MODELOCKTM method, and its operating temperature limit is 0-50 °C. The substrate and the source materials are separated by the shutter. Therefore, we can evaporate desired thick metals by using both thickness monitor and the shutter.

Fig. 3.7: Image of EB evaporator

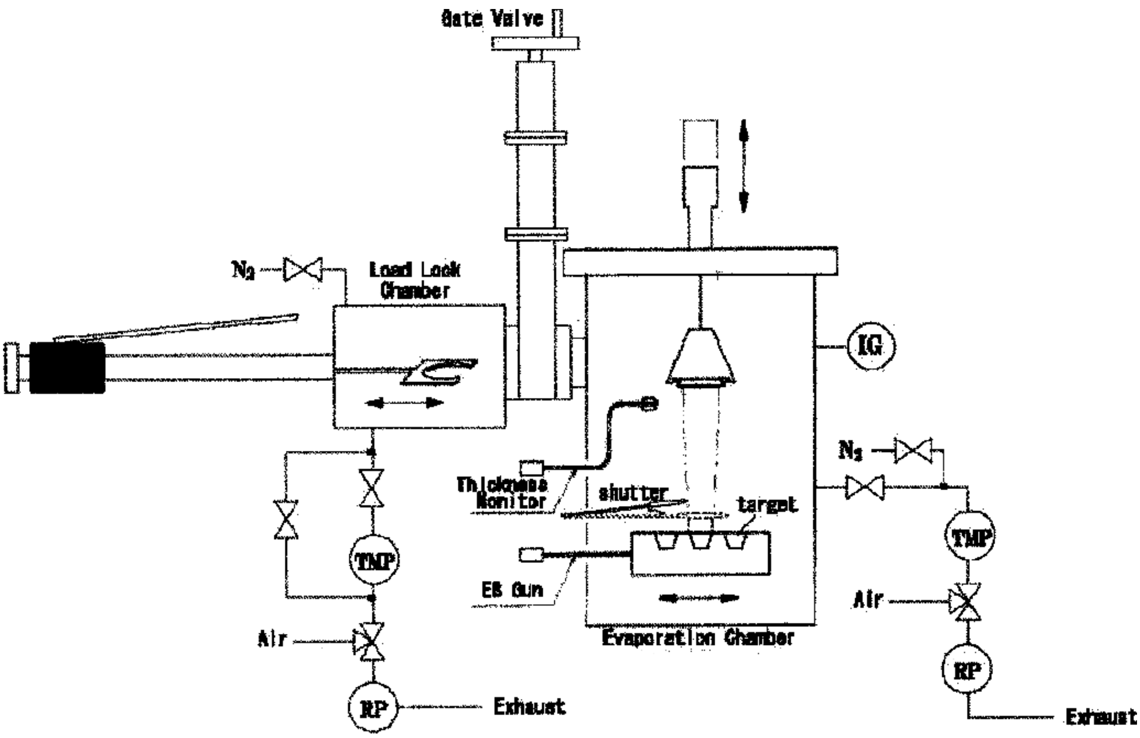


Fig. 3.8: vacuum system of EB evaporator

3.2.6.Scanning electron microscopy (SEM)

A scanning electron microscopy (SEM) is a type of electron microscope that images a sample by scanning it with a high-energy beam of electrons in a raster scan pattern. The electrons interact with the atoms that make up the sample producing signals that contain information about the sample's surface topography, composition, and other properties such as electrical conductivity.

The SEM (HITACHI. Inc., S-5000, S-4500) is used for observation of the shape of electrode pattern, Silicon QDs, ferromagnets and misalignment of those. In charge of S-5000 is Oda laboratory, and in charge of S-4500 is Mizumoto laboratory. In the case of S-5000, the sample should be cut to because max size of sample holder is small less than 1 cm × 1 cm. On the other hands, maximum sample size is 2 cm × 2 cm for S-4500. Therefore, we should use S-4500 during our fabrication process. Figure 3.9 shows the image of S-4500. The accelerate voltage of electron is very high, then we should take care the sample especially using photo or electron beam resist. With the voltage is high and magnification is high, the high energy electrons break the shape of the resist and deposit many hydro-carbon contamination. Therefore, we set the voltage as 10 or 15 keV when observe the sample.

Figure 3.9 Image of S-4500

3.3. Device fabrication process

Silicon QDs devices are fabricated by following condition (Table 3.2). Schematics of the device after fabrication processes *1~*5 are shown in Fig. 3.10-14.

Table 3.2: Fabrication process of the Si QDs device

SOI substrate		
SOI layer thickness	100 nm or 200 nm	
Buried oxide (BOX) layer thickness	200 nm or 380 nm	
Thinning *1		
Temperature	1100 °C	
Thinned SOI thickness	~40 nm	
Passivation		
Temperature	900 °C	
Duration	5 min	
EB resist coating		
Resist	ZEP 520A : ZEP A= 1:3 with C_{60}	
Spin coating	1000 / 3000 rpm, 5 / 60 s	
Pre beak	180 °C, 10 min by oven	
EB exposure		
Dose quantity	~490 μC	
Development		
Developer	MIBK : IPA = 1 : 1	
Duration time	90 s	
Rinse	IPA	
Duration time	30 s	
Dry etching		
Gas	Cl_2	SF_6
Micro wave power	50 W	20 W
Duration time	~60 s	~88 s
O_2 ashing	Not used	15 s
Resist removal *2		
Remover	SPM 3:1	
Duration	15 min ~30 min, 120 °C	
Gate oxidation *3		

Temperature	1000 °C	
Duration	Varied	
SiO_2 deposition		
Thickness	~50 nm by Hiramoto Lab. In Tokyo Univ.	
Poly-Si deposition *4		
Gas	Si_2H_6 0.3 sccm, PH_3 7 sccm	
Temperature	500 °C	
Duration time	40 min	8 min
Thickness	~200 nm	~ 50 nm
Photo resist coating		
Resist	HMDS and S1818	
Spin coating	1000 / 2000 rpm, 5 / 30 s and 1000 / 3000 rpm, 5 /60 s	
Pre beak	Not used and 1 min by hot plate	
Photolithography		
Mask	Metal mask	
Dose quantity	~100 mJ	
Development		
Developer	MF320	
Duration time	90 s	
Rinse	Pure water	
Duration time	30 s	
Poly-Si etching by plasma etcher		
Gas	CF_4 and O_2	
Duration time	1 ~ 2 min	
Ion implantation		
Acceleration voltage	Varied	
Dose quantity	1×10^{15} / cm^3	
Source	PH^3	
Resist removal *5		
Remover	SPM 3:1	
Duration	15 min ~30 min, 120 °C	
Drive in and recrystallization		
Temperature	1000 °C	
Duration time	20 min	

Photo resist coating	
Resist	HMDS and S1818
Spin coating	1000 / 2000 rpm, 5 / 30 s and 1000 / 3000 rpm, 5 /60 s
Pre beak	Not used and 1 min by hot plate
Photolithography	
Mask	Metal mask
Dose quantity	~130 mJ
Development	
Hardener	Dichlorobenzene
Duration time	2 min 15 s
Developer	MF320
Duration time	90 s
Rinse	Pure water
Duration time	30 s
Metal deposition	
Metal	Aluminum
Thickness	~ 300 nm
Lift off	
Solution	Acetone
Duration time	~ half day
Forming gas anneal	
Gas	$N_2 : H_2 = 95 : 5$
Temperature	400 °C
Duration time	20 min

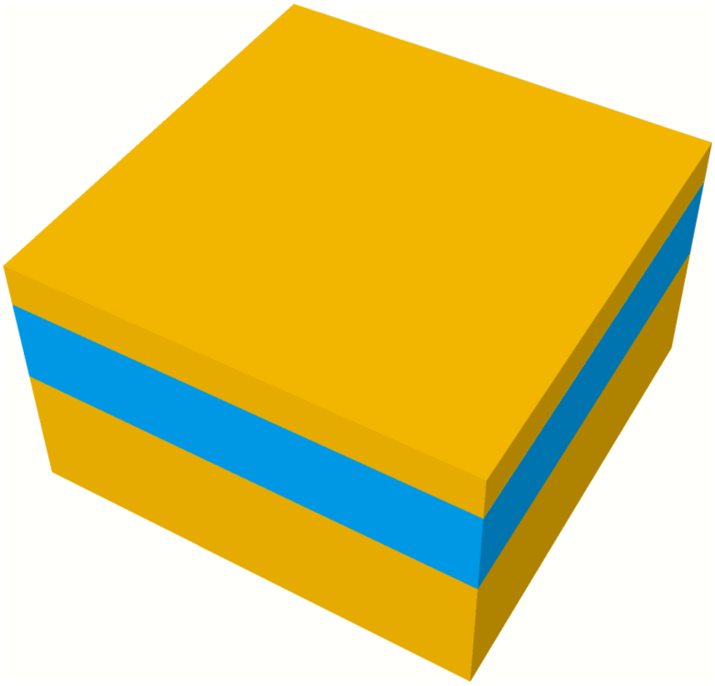


Fig. 3.10: schematic of the device after thinning process

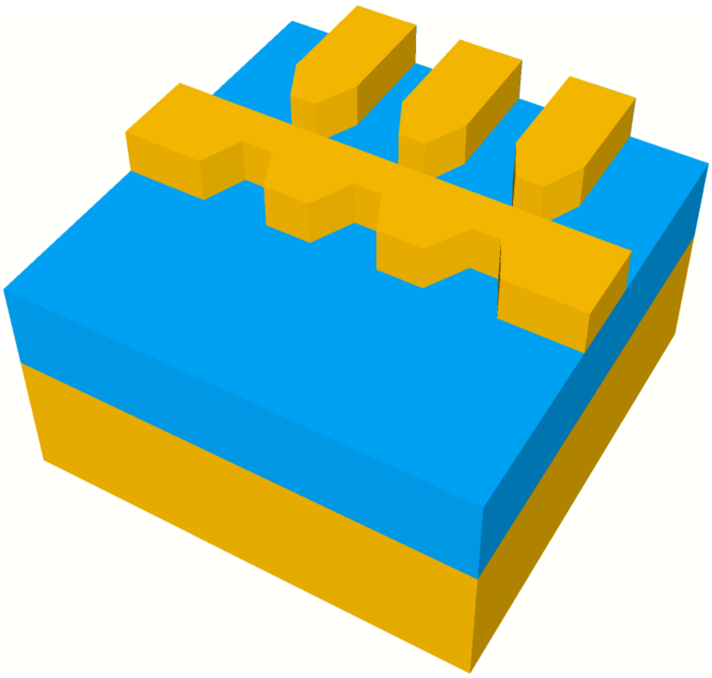


Fig. 3.11: schematic of the device after resist removal of dry etching

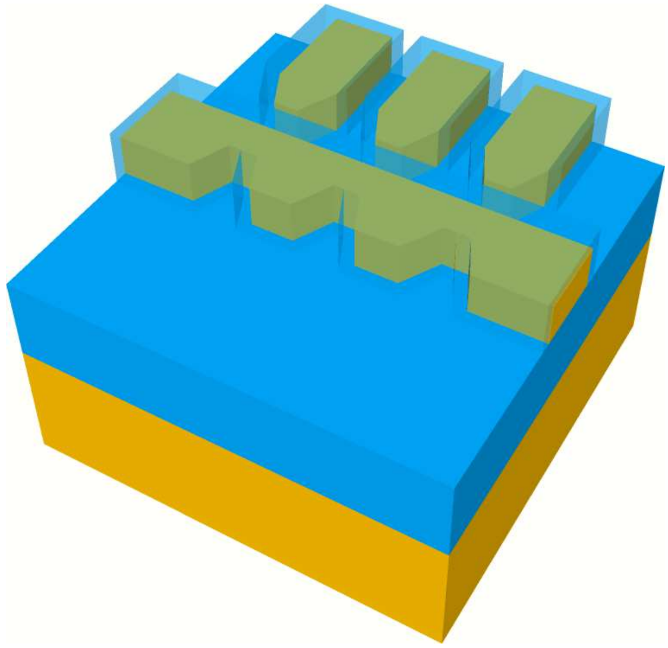


Fig. 3.12: schematic of the device after gate oxidation

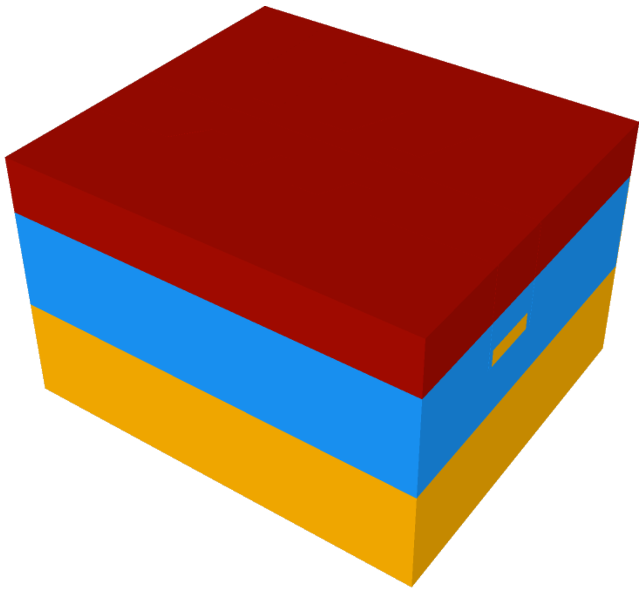


Fig. 3.13: schematic of the device after poly-Si depostion

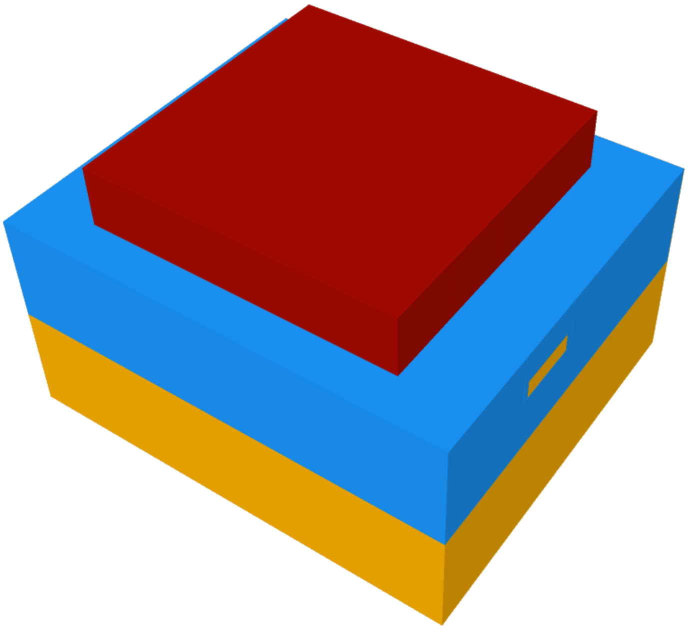


Fig. 3.14: schematic of the device after resist removal of ion implantation

Chapter 4: Analysis of Charge Modulation in Si DQD

Abstract

In this chapter, we have calculated the electron states in Si DQD device. Electrons are confined near the upper interface in the SOI layer by a top gate and side gates voltages. Charge density at 4 K in DQDs is evaluated using the experimental data of the temperature dependence of the density in a MOS) transistor at 100 K and 4 K. With optimum side gates bias, electrons are confined in QDs and a coupling between QDs is controlled in a few-electron regime. We have also proposed that a charge sensor is required to read out the few-electron regime because no current flows in the DQD device.

4.1. Introduction

In this chapter, we study a DQD device where a few-electron regime can be achieved using a device simulator with a classical model. In a few-electron regime, a coupling between QDs is modified by side gate voltages. We propose a DQD device structure integrated with a charge sensor to read electron states in a few-electron regime where drain current is too small to measure.

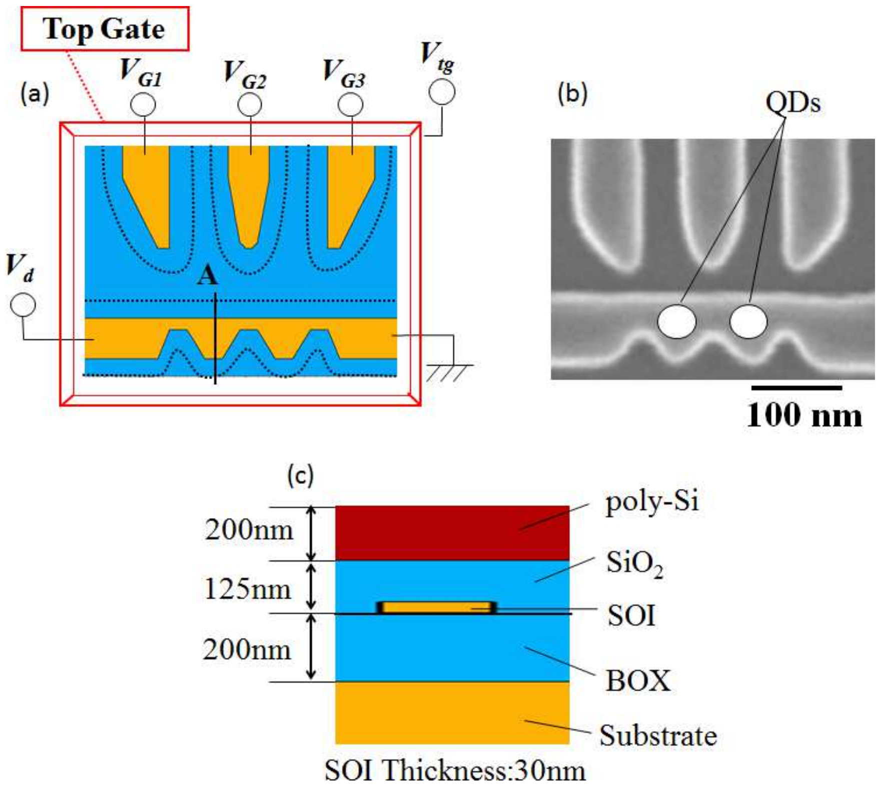


Fig. 4.1(a): Device model used for simulation. Si DQDs and side gates (G1, G2, and G3) are covered with deposited SiO_2 and BOX. The top gate, which is formed after the SiO_2 deposition, is shown as a red transparent rectangle. (b) SEM image of Si DQD device after dry-etching of SOI layer. The Si QDs are schematically indicated by ovals. (c) Cross-section of device structures along the line A in (a). The thicknesses of the poly-Si, SiO_2, SOI, and BOX are 200, 125, 30, and 200 nm, respectively.

4.2. Simulation method

We used a device simulator "ATLAS" from Silvaco Inc. to calculate electrical potentials in the Si DQD device as shown in Fig. 4.1(a) [52]. The device simulator solves Poisson equation to calculate electrical potentials and electron concentrations. We used an incomplete ionization model for calculation of electron concentrations at a temperature higher than 100 K [53]. In order to estimate a surface charge density of QDs at 4 K, we used a simulation result at 100 K and measurement results of a metal-oxide-semiconductor (MOS) transistor at 100 K and 4 K.

The side gates and DQD regions are formed with thermal oxidation after fabricating the structure with EBL and dry etching. Figure 4.1(b) shows a SEM image of the device before deposition of the top gate. The Si DQD is schematically indicated by ovals. The dotted lines in Fig. 4.1(a) are boundaries between the SiO_2 formed with thermal oxidation and that deposited with low-pressure chemical vapor deposition (CVD). The potential barriers are formed at constricted regions, which are made less than 10 nm wide. Figure 4.1(c) shows a cross-section of the device structure along line A in Fig. 4.1(a). The thicknesses of the SOI layer and BOX are 30 nm and 200 nm, respectively.

A top gate layer, deposited after thermal oxidation and CVD SiO_2 formation, is made of heavily doped poly-Si, and used to induce a 2DEG at the Si/SiO_2 interface, much like a gate layer of a MOS transistor. The side gates are used for controlling the potential of each QD and modifying the tunneling rates through potential barriers. Figure 4.2 shows the electrical potential distribution of the upper interface in the SOI layer when voltages are applied to the top gate (V_{tg}) and the side gates (V_{G1}, V_{G2}, and V_{G3}). The bottom curve indicates the potential along the line B, which shows two local minimums between the constrictions, leading to the formation of two QDs.

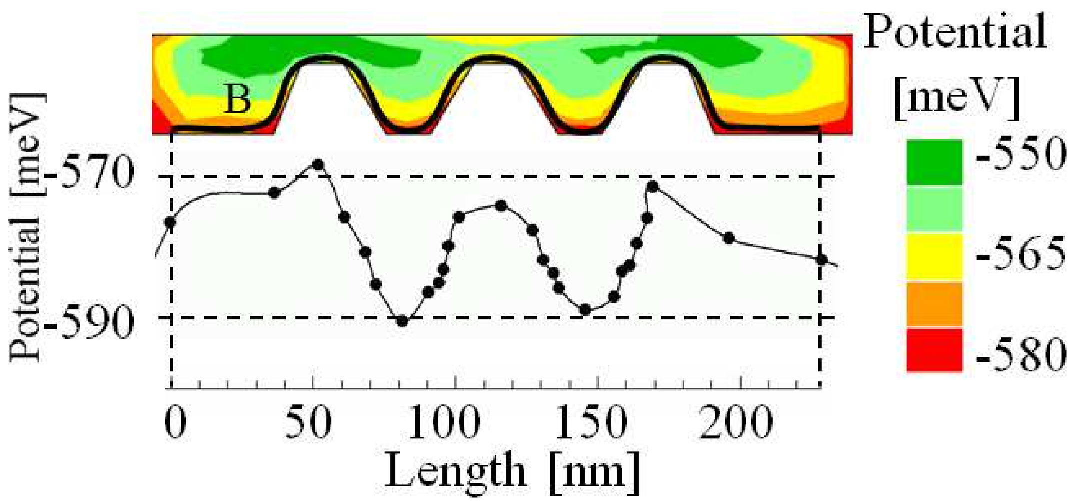


Fig. 4.2: Distribution of electrical potential in the region of QDs when V_{tg}= 2 V, V_{G1}= V_{G3}= -1.5 V, and V_{G2}= 0 V. The bottom curve indicates the potential along the line B.

4.3. Results and discussion

A few-electron regime in QDs confined into a thin layer is required for the goal of spin manipulation. First, V_{tg} dependence on the thickness of QDs at 100 K is studied. Electrons are induced with positive V_{tg} [Figs. 4.3(a) and 4.3(b)]. When V_{tg} is lower than 1 V, electron concentration is too low.

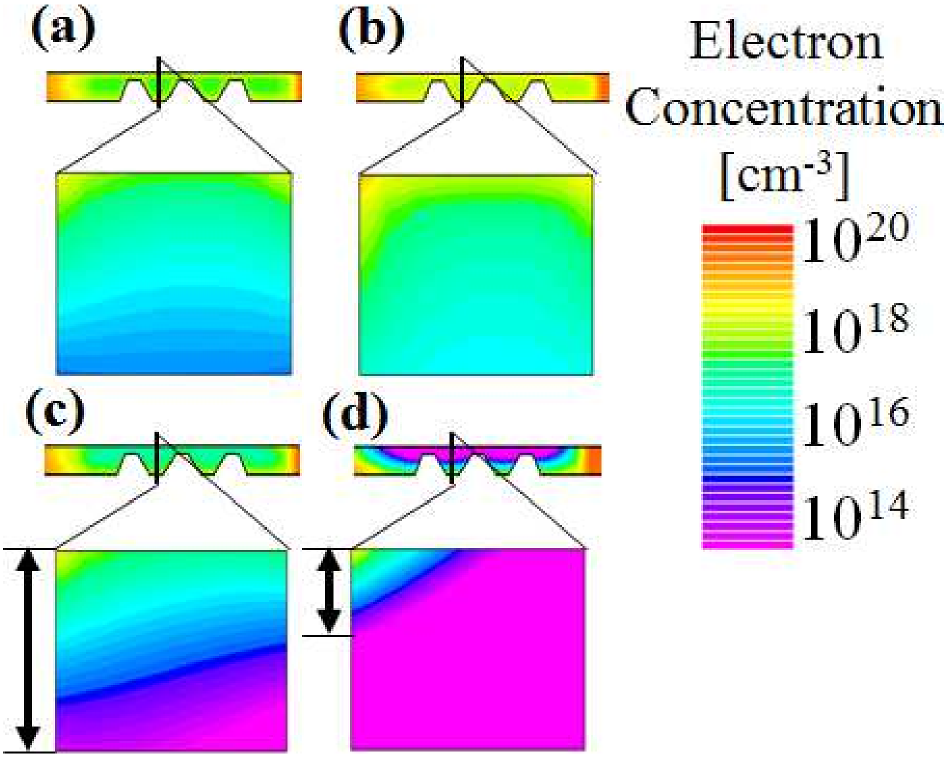


Fig. 4.3. Top views and cross-sections of the electron concentration in DQD part of device at 100K. The numbers of electrons are calculated by integration of the electron concentration in a QD. (a) V_{tg} = 1.0 V and V_{G1} = V_{G2} = V_{G3} = 0 V. Electrons are strongly induced especially near the upper interface in the SOI layer. (b) V_{tg} = 2.0V, V_{G1} = V_{G2} = V_{G3} = 0 V. Electron concentrations are higher than those in (a) in the whole SOI layer. (c) V_{tg} = 1.0V, V_{G1} = V_{G3} = -0.6 V and V_{G2} = 0 V. There is one electron in each QD. Electron concentration is spread widely, which forms the thick QDs. (d) V_{tg} = 2.0 V, V_{G1} = V_{G3} = -2.4 V, V_{G2} = 0 V. There are two electrons confined in each QD.

Therefore, DQDs cannot be formed even when V_{G1} = V_{G2} = V_{G3} = 0. With a high V_{tg}, the electron concentration becomes high, especially near the upper interface in the SOI layer. Thus, the thickness of QDs is varied by controlling V_{tg}, V_{G1}, V_{G2}, and V_{G3} while the few-electron regime is maintained [Figs. 4.3(c) and 4,3(d)]. Here the definition of the

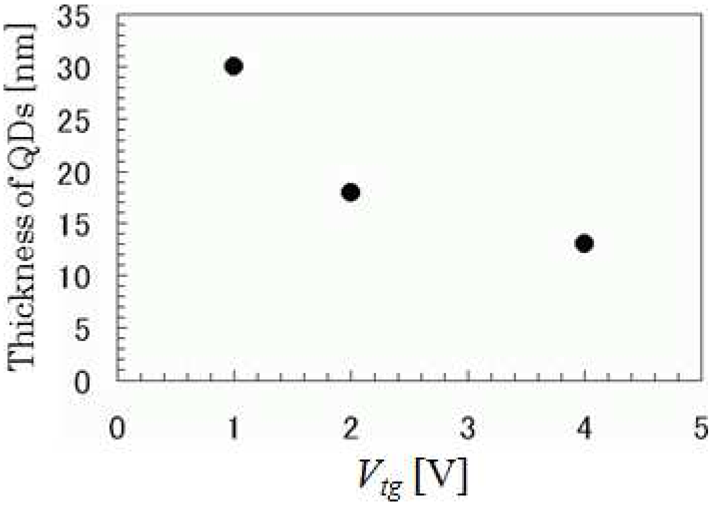


Fig. 4.4: V_{tg} dependence of the thicknesses of QDs.

thickness of QDs is the depth of the region with the electron concentration higher than 10^{14} cm^{-3} on the far side from side gates (indicated by arrows). Figure 4.4 shows V_{tg} dependence on the thickness of the QDs in the few-electron regime. Here the regions with electron concentrations less than 10^{14} cm^{-3} are ignored when we estimate the thickness. V_{tg} dependence of the thickness is small when V_{tg} is higher than 2 V, where electron concentration is too high to achieve a few-electron regime. Therefore in later discussion, V_{tg} is fixed at 2 V.

When we consider the number of electrons in QDs, temperature becomes important. Potential distributions depend on temperature [Figs. 4.5(a) and 4.5(b)].

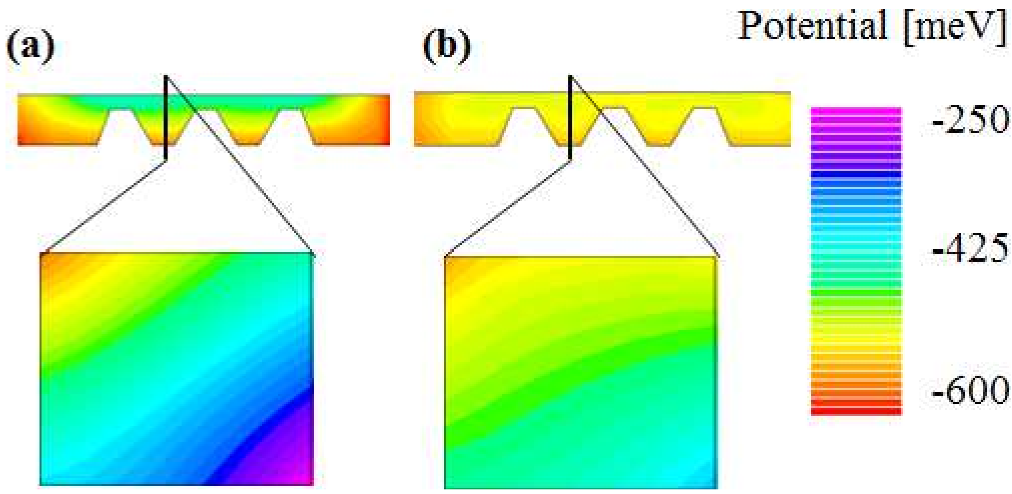


Fig. 4.5: Top views and cross-sections of potential distribution in QDs. Here V_{tg}= 2 V, V_{g1}= V_{g3}= -1.5 V, and V_{g2}= 0 V. Temperatures are 200 (a), and 100 K (b), respectively. Electrical potential of lower right region at 100 K (b) is higher than that at 200 K (a).

However, it becomes more difficult to get convergence as the temperature drops, especially below 10 K. Intrinsic carrier concentration n_{ie} is given by:

$$n_{ie} = \sqrt{N_C N_V} \mathrm{F}_{1/2}^2 \left(\frac{-E_g}{kT_L}\right). \tag{4.1}$$

Here N_C and N_V are the effective density of states for electrons and holes, $\mathrm{F}_{1/2}(x)$ is the Fermi-Dirac integral of order 1/2, E_g is the band-gap energy of Si, k is Boltzmann's constant and T_L is a lattice temperature. By decreasing T_L, n_{ie} also decreases drastically. Therefore n_{ie} and surface charge density, N_S, at ultra-low temperature cannot be calculated using only the simulator.

In this chapter, the number of electrons in the DQD device at 4 K is estimated by experimental data of N_S in an MOS transistor. Figure 4.6 shows the temperature dependence of N_S of the MOS transistor based on simulation and measurement. With gate oxide thickness of 6 nm, N_S is calculated by a split C-V method using V_{tg}= 150 mV. The incomplete ionized model is used to account for impurity freeze-out at low temperature [53]. However, it cannot explain the reason why N_S of the measurement result is drastically reduced less than 20 K.

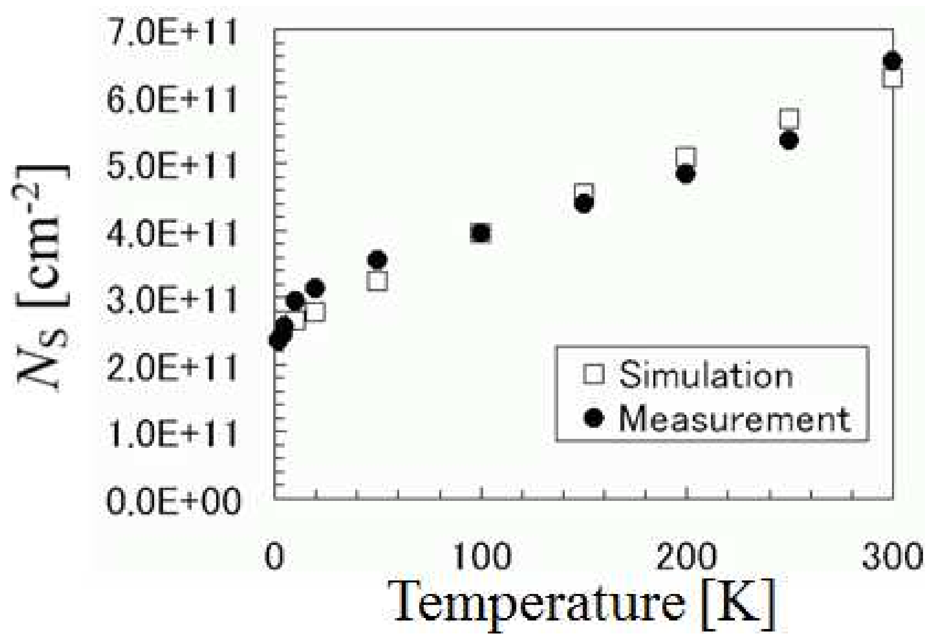


Fig. 4.6: Temperature dependences of N_S in MOS transistor obtained by simulation (indicated by square), and by measurement (indicated by circle), respectively. The difference in N_S between simulation and measurement is within $\pm$ 10% when the temperature is higher than 50K.

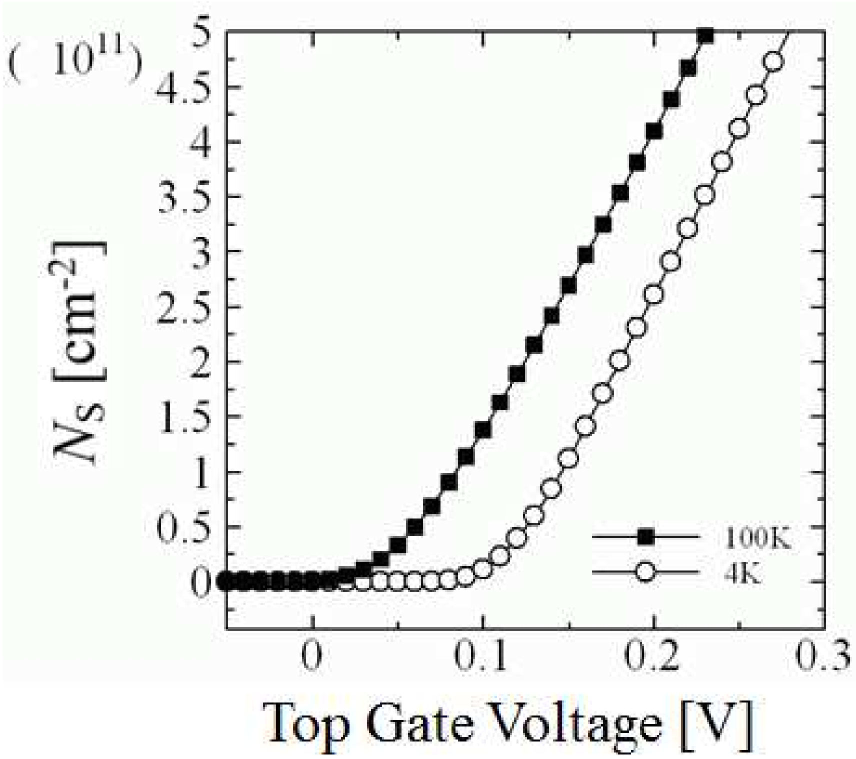


Fig. 4.7: Top gate voltage dependences on N_S of MOS transistor measured at 4 K (indicated by circle), and at 100 K (indicated by square), respectively.

The top gate voltage dependences on N_S of MOS transistor measured at 100 K and 4 K are shown in Fig. 4.7. Since the DQD device structure has a top gate electrode to induce electrons and multiple side gate electrodes to create local depletion regions, distribution of electrical potentials are different from simple MOS transistor case. However, in order to estimate N_S and number of electrons in QDs, a region near the upper interface of SOI layer is dominant. Therefore, we can estimate N_S of QDs at 4 K using experimental data of the MOS transistor [Fig. 4.7].

By using the method, few-electron DQDs at 4 K are formed with optimized side gate voltages as shown in Figs. 4.8(a) and 4.8(b). When V_{tg}= 2 V and V_{G1}= V_{G2}= V_{G3}= -1V, the number of electrons in each QD becomes one [Fig. 4.8(a)]. In this condition, the coupling between the QDs is very weak because there are no electrons in the center constriction. On the other hand, the inter-dot coupling becomes strong when V_{G1} = V_{G3} = -1.5 V and V_{G2} = 0 V [Fig. 4.8(b)]. In this device we can form few-electron DQDs and modulate inter-dot coupling by changing side gates voltages.

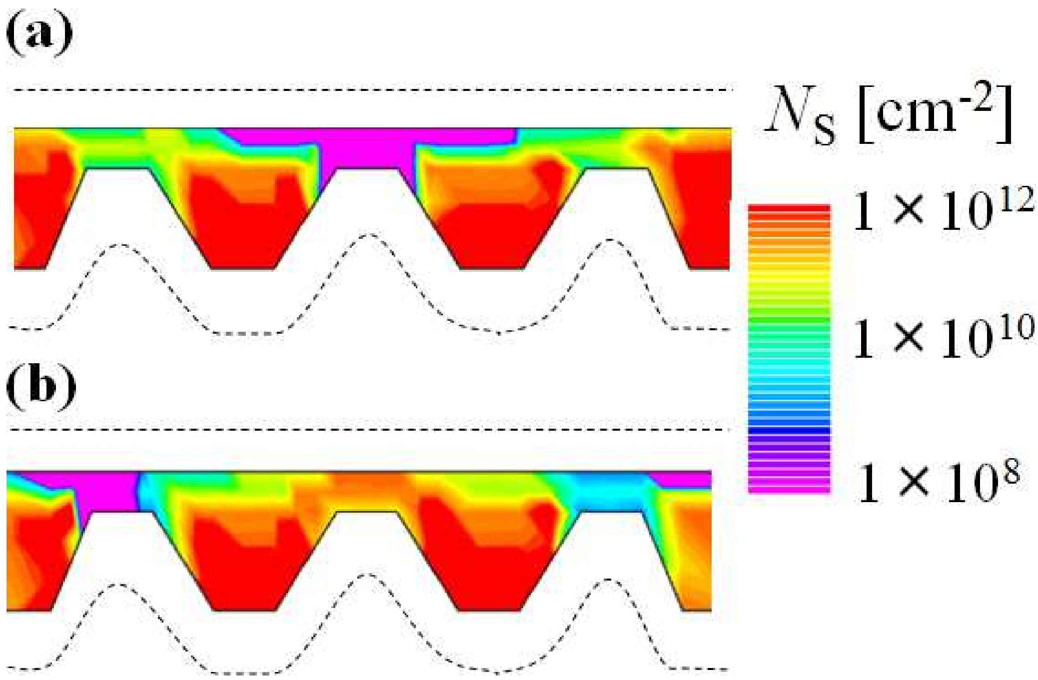


Fig. 4.8. Distribution of N_S in few-electron DQDs. (a): Weakly coupled DQD. (V_{tg} = 2.0 V, V_{G1} = V_{G3} = -1 V, V_{G2} = -1.3 V). (b): Strongly coupled DQD. (V_{tg} = 2.0 V, V_{G1} = V_{G3} = -1.5 V, V_{G2} = 0 V). In both cases, there is a single electron in each QD.

However, there are no electrons in the constrictions between two QDs [Fig. 4.8(a)] or between a QD and a lead [Fig. 4.8(b)]. As a result, it is difficult to obtain the source-drain current I_d through the DQD in these conditions. Therefore, a charge sensor, such as a single-electron transistor (SET) integrated near the DQD, is required to monitor electron states in a few-electron regime, instead of measuring I_d [54]. Figure 4.9 shows an SEM image of the structure fabricated with EBL and dry etching. The upper side of the structure, consisting of a DQD and gates, is the same as the model used for the device simulation. An SET was integrated in the vicinity of the DQD. By measuring the current through the SET, electron states in a few-electron regime can be observed.

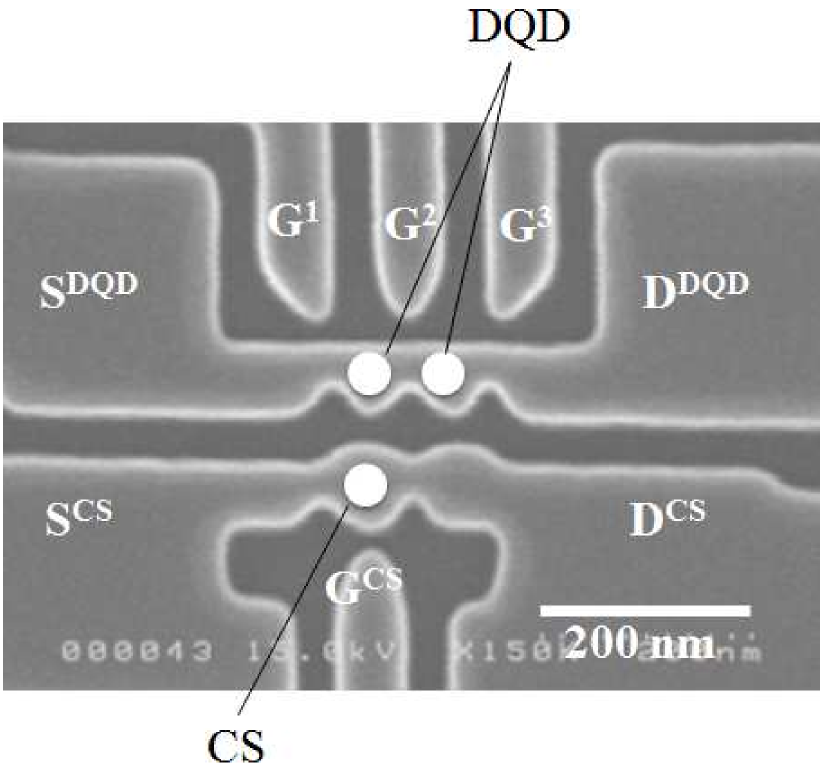


Fig 4.9. SEM image of DQD device integrated with SET as CS. The DQD and CS are schematically indicated by circles. The electron states in the DQD can be read out using an SET.

4.4. Conclusions

In this chapter, we calculated the electron concentration in a DQD device at 100 K using a device simulator within a classical regime. The profile of the surface charge density in the DQD device at low temperature was obtained using the experimental data of the MOS transistor. The DQDs in a few-electron regime at 4 K were formed by controlling the top gate and the three side gate voltages. The coupling between two QDs was modulated by the side gate voltages while the number of electrons in QDs was kept constant. We proposed the device structure integrated with an SET as a CS for monitoring charge states in few-electron DQDs.

Chapter 5: Detection of Single Electron Transport in various Si DQD Structures

Abstract

In this chapter, DQDs device with the CS to readout electron position, which is used to also detect electron spin, are fabricated and its transport characteristics are analyzed. Device structures to obtain high tunnel rate through the QDs are also discussed.

5.1. Introduction

In previous chapter, the electron density at the constriction by the effect of the applied gate bias to achieve few-electron regime with the calculated DQD device. The low density means high and/or thick potential barrier at each constriction. Therefore, the tunnel rate of electron from the source electrode to the drain electrode will becomes low, and it is difficult to observe the source-drain current in real device. In this chapter, the charge sensor to measure the electron transport in the DQD without the DQD current is integrated to the DQD, and the characteristics of the transport of the DQD and CS are shown. In order to keep high tunnel rate, the position of the constrictions, gate electrodes, and the sensor of the device structure is optimized.

Electrons are confined at near the interface of SOI and the gate oxide layer when the electrons are induced by the top gate bias. The confined electrons at the upper interface tend to be affected by the defects of the interface of the thermal oxidation and the edge shape of the DQD formed by dry etching. In this chapter, the DQD is also formed at the bottom interface of SOI and BOX layer by the back gate bias, and its electron transport is measured.

5.2. Charge sensing of DQD

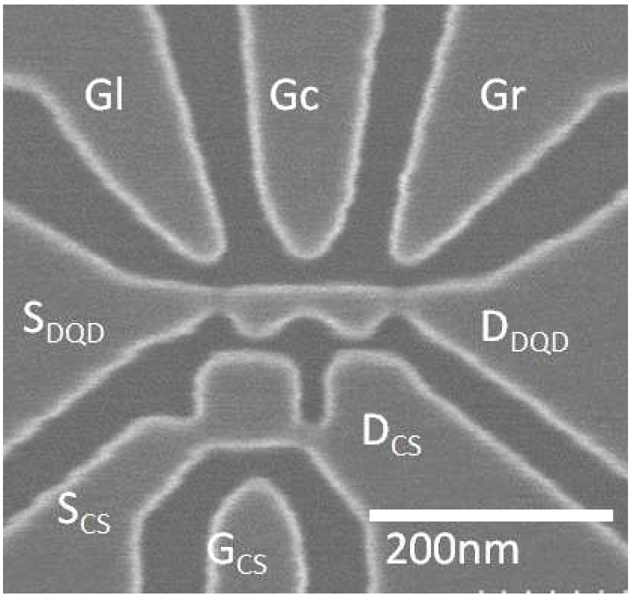


Fig. 5.1: SEM image of DQD with SET as a CS

As above discussion, the DQD device structure which is integrated with a CS is fabricated. Fabrication process is not changed but different EB pattern is drawn before dry etching. The CS works as a SET with Coulomb oscillation in I_{dCS}-G_{CS} characteristics. The DQD is capacitively coupled to the close CS as well as other gate electrodes. The electric field from the DQD to the CS depends on the number of electrons in the DQD, and then, the gate voltage from the DQD is changed rapidly when the number of electron is changed [Fig. 5.2(a)]. When the gate bias coupled to both the DQD and CS is swept, a smooth Coulomb oscillation and kinks in the result of I_{CS} [Fig. 5.2(b)] because of the another gate, the DQD.

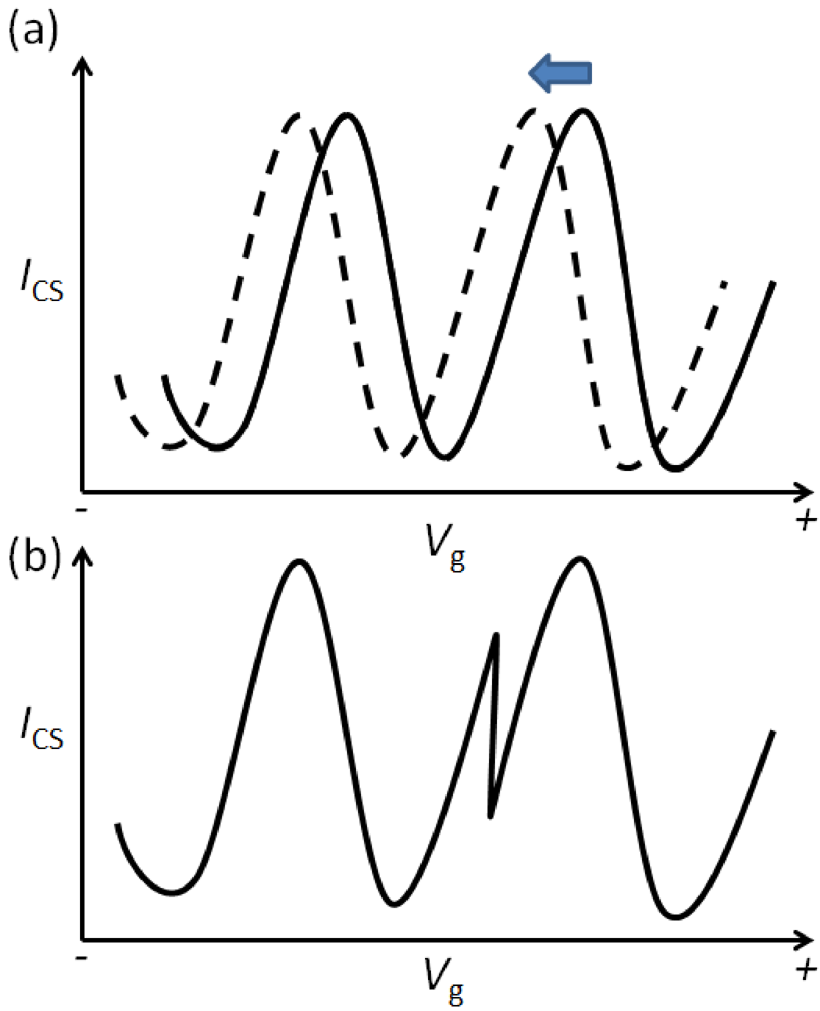


Fig. 5.2: Schematics of I_{CS}- V_g. (a) Before (dashed line) and after (solid line) of changing the number of electron in capacitively-coulpled DQD. (b) Measured current when The number of electrons are changed in sweeping V_g.

Figure 5.3 shows $I_{DQD,CS}$- V_{gl} characteristics of the DQD device with sweeping V_{gl} of the DQD device of Fig. 5.1. The position of the Coulomb peaks of I_{dDQD} is the same as that of the kinks in the Coulomb oscillation of I_{dCS}. Because the number of electrons of the DQD is stable in the region between each Coulomb peak, the kinks are the signal of the single-electron transition in the DQD. Furthermore, the kinks are obtained in whole region of I_{dCS} with large value ~ 1 nA, while the Coulomb peaks of the I_{dDQD} are not observed in the left side in Fig. 5.3. This means that the number of electrons of the DQD is changed, however, Coulomb peaks are not observed because of too low tunnel rate between the source and drain.

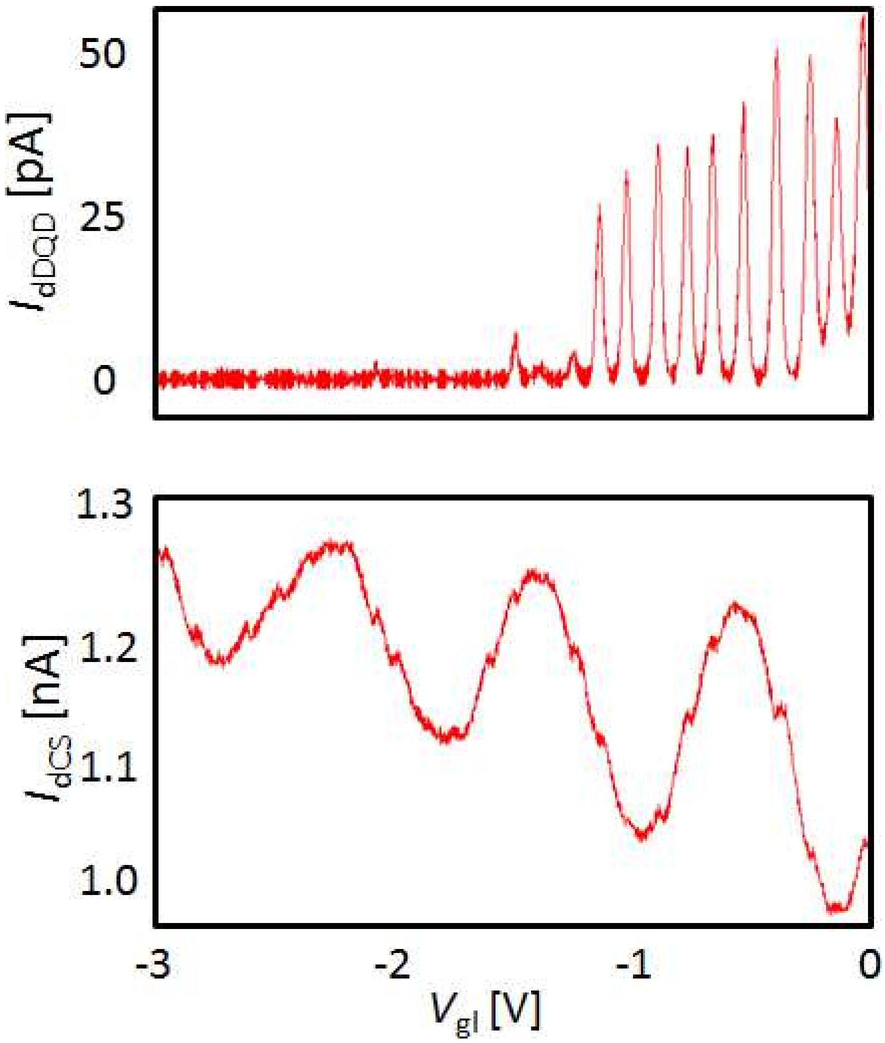


Fig. 5.3: $I_{dDQD,dCS}$- V_{gl} characteristics of the device of Fig. 5.1. Positions of the Coulomb peaks of I_{dDQD} and kinks of I_{dCS} which are charge sensing signals. The kinks are clearly observed whole region of I_{dCS} when I_{dDQD} = 0 A.

Figure 5.4 shows the charge stability diagrams of the DQD and CS with sweeping V_{gl} and V_{gr}. The distinctive honeycomb structure of the DQD is observed in the diagram of the DQD [Fig. 5.4 (a)]. There is no current in the left side of Fig. 5.4 (a), then it looks the characteristics of the few-electron regime. In the diagram of the CS, in addition to thick stripes colored by blue, white and red in whole regime, the honeycomb structure, whose shape is completely the same as that of the DQD [Fig. 5.4 (a)], is clearly shown. The observed honeycomb structure is the result of reading out of the single-electron transition of the DQD, and the honeycomb is also observed in the region of $V_{gl} < 0.3$ V.

Therefore, as the discussion in the chapter 4, the observation of the few-electron regime with only the direct current through the DQD is the challenge. However, the relative change of the number of electrons in each QD is now read out by the integration of the CS. In addition to that, the number of the electron in each QD is stable in the region surrounded by one Honeycomb. From these results, the technique to control the position of the single electron in the DQD by the gate biases and the integrated CS is developed. This technique is also useful to read out the electron-spin information from the DQD system.

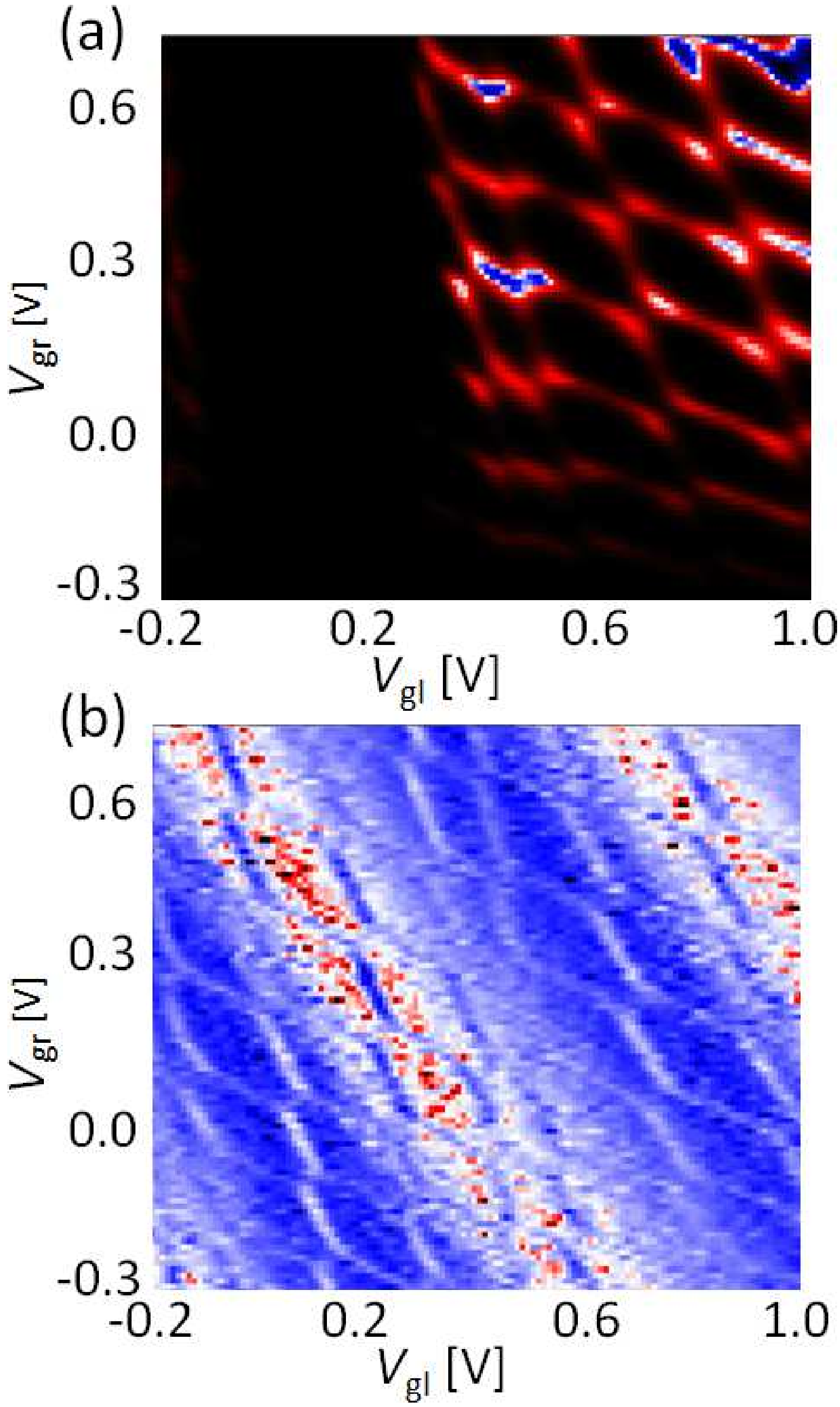


Fig. 5.4: (a) Charge stability diagram of the DQD with V_{tg} = 5.55 V and V_{bg} = 0 V. Honeycomb structure is clearly observed at right side, but no signal at left side. (b) Differential conductance of the integrated CS. The same honeycomb structure as that of the DQD is observed in whole region. Each honeycomb line shows that single electron escapes/enters from/to the DQD.

5.3. DQD formed by back gate bias

To reduce the number of electrons in the QDs, good quality QDs formation is also an important technology. Impurities and defects in Si crystal or the oxide layer of the QDs vicinity form a trap, which give negative effects such as a shot noise or an unintentional QD formation. Therefore, we form the DQD by the inducing the electrons with positive V_{bg} and V_{tg} = 0 V in the same device of Fig. 5.4 [Fig. 5.5].

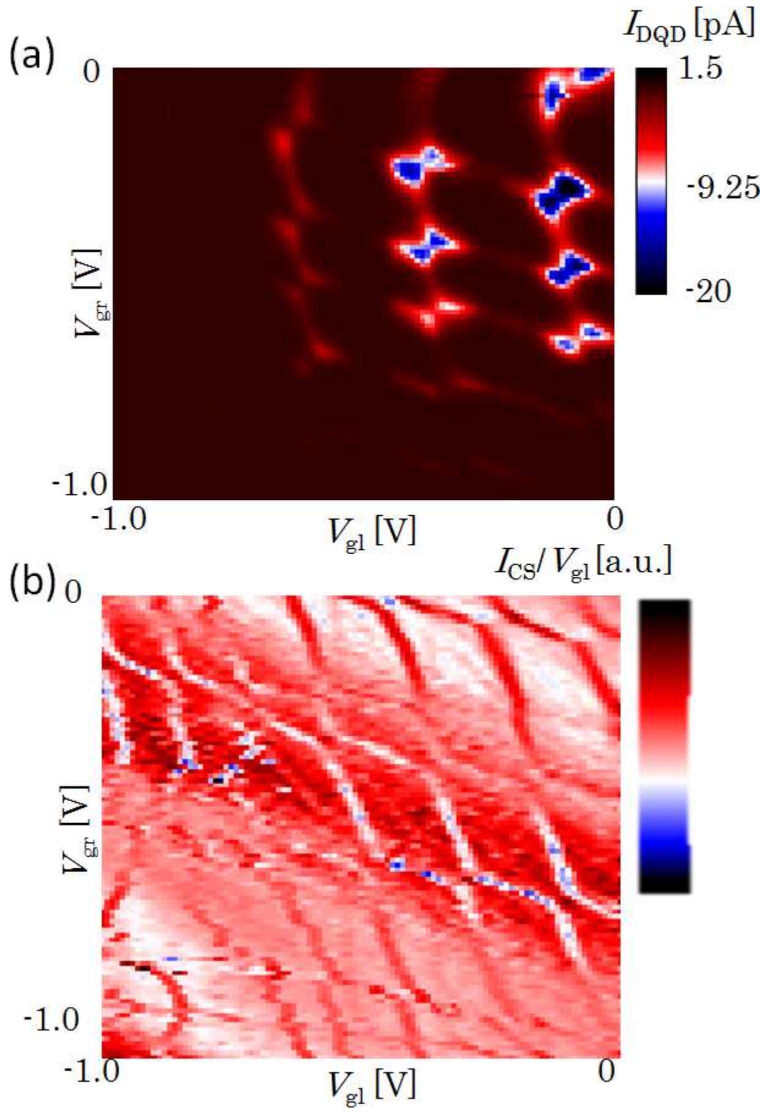


Fig. 5.5: Charge stability diagram of the same device as that of Fig. 5.4 with V_{tg} = 0 V and V_{bg} = 4.5 V. (a) The electrons forms DQD and clear honeycomb structure is observed. (b) Differential conductance of CS. Sensing lines are fluctuated at left side because of low tunnel rate though the DQD.

The induced electrons are confined near the clean interface of SOI-BOX layer. The DQD which is formed by V_{bg} may have less the additional dots and potential barriers than that formed by V_{tg}. On the other hand, the sensing lines of the CS are unclear and unstable in the region of $V_{gl,r} < -0.5$ V [Fig. 5.5 (b)]. The fluctuated lines means that any potential barrier of the DQD becomes thick by the high negative $V_{gl,r}$, and then, tunneling rate of the electrons is lowered significantly. Therefore, the timing of the single-electron transition in the DQD is shifted. From these results, the only DQD formed by V_{bg} does not solve the problem of the controlling the height of the potential barrier for the electron number reduction.

5.4. Modification of constrictions and gate electrodes positions

When the high biases are applied for the electron number reduction of the DQD, the potential barriers become high, then tunneling rates become low because the gate electrodes are coupled to the constrictions as well as the QDs. I_{DQD} cannot be observed with the low tunneling rate, but when the tunneling rate is further decreased, the DQD is isolated from the lead completely, which means no more electrons are excluded. We fabricate the DQD device with changing the positions of the constrictions to maintain the large tunneling rate of the DQD [Fig. 5.6 (a)]. The capacitance of the gate electrodes and the constrictions between the leads and QDs are reduced by the gate electrodes away from the constrictions. However, since the tunnel coupling of left and right QDs is preferred to be adjusted, the G_C is placed near the center constriction. Figure 5.6 (b) shows the charge stability diagram of the DQD. I_{DQD} flows even with high negative V_{gl} and V_{gr}, which means the tunneling rates of the DQD is kept high in Fig. 5.6 (b). However, even in this structure, the specific characteristics of the few-electron regime are not observed. One reason of that is considered as that the gate electrodes are not still close enough to the QDs and/or that the size of the QD is not small enough. Because of the limit of our fabrication techniques, the closer gate electrodes and more reduction of the QDs size with this shape is a big challenge.

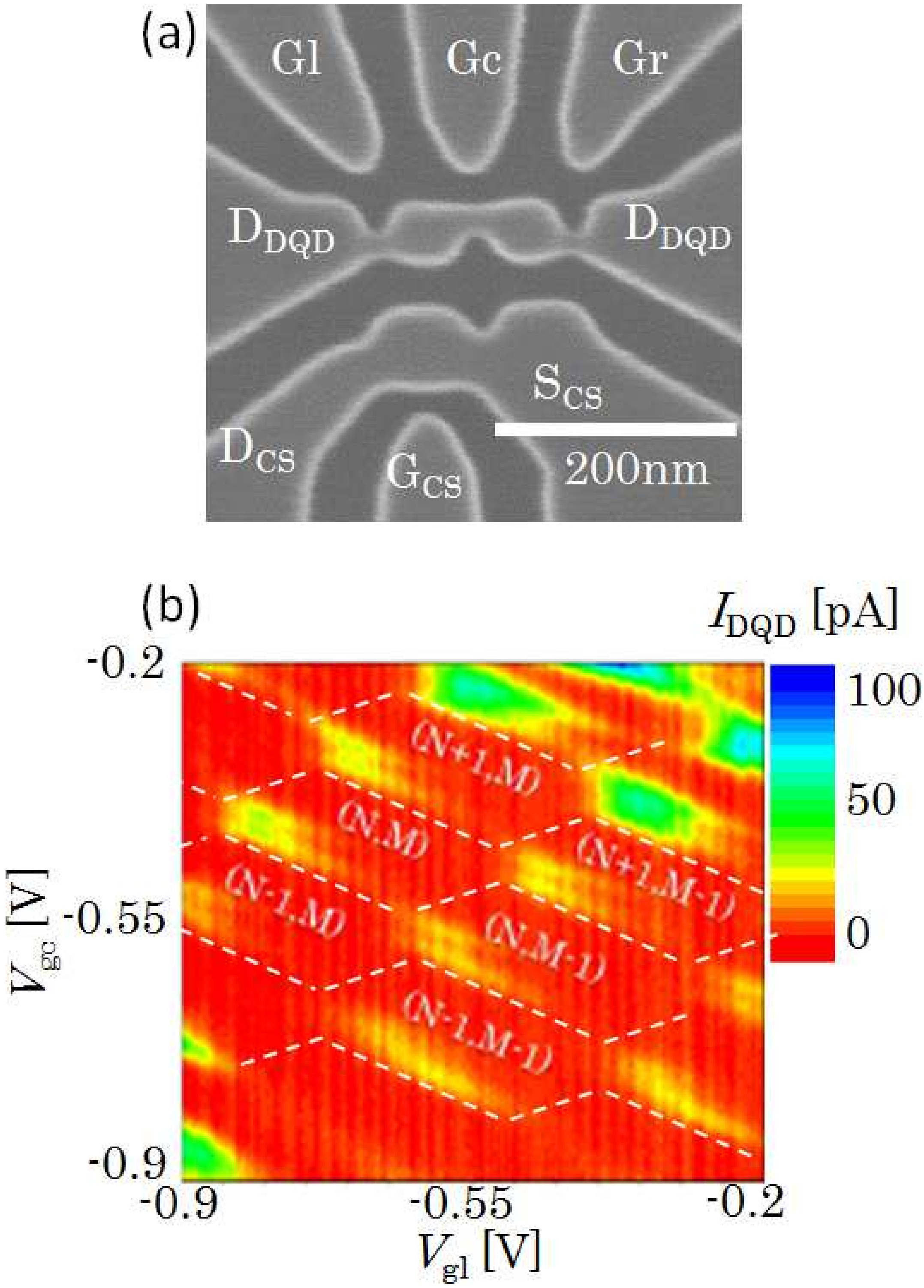


Fig. 5.6: (a) SEM image of the DQD with modification of constrictions between dot-lead. Gl and Gr become far from the constriction to avoid pinch off the potential barriers. (b) Charge stability diagram of the DQD. Triple points are clearly observed in whole region.

5.5. Modifications of charge sensor and gate electrodes positions

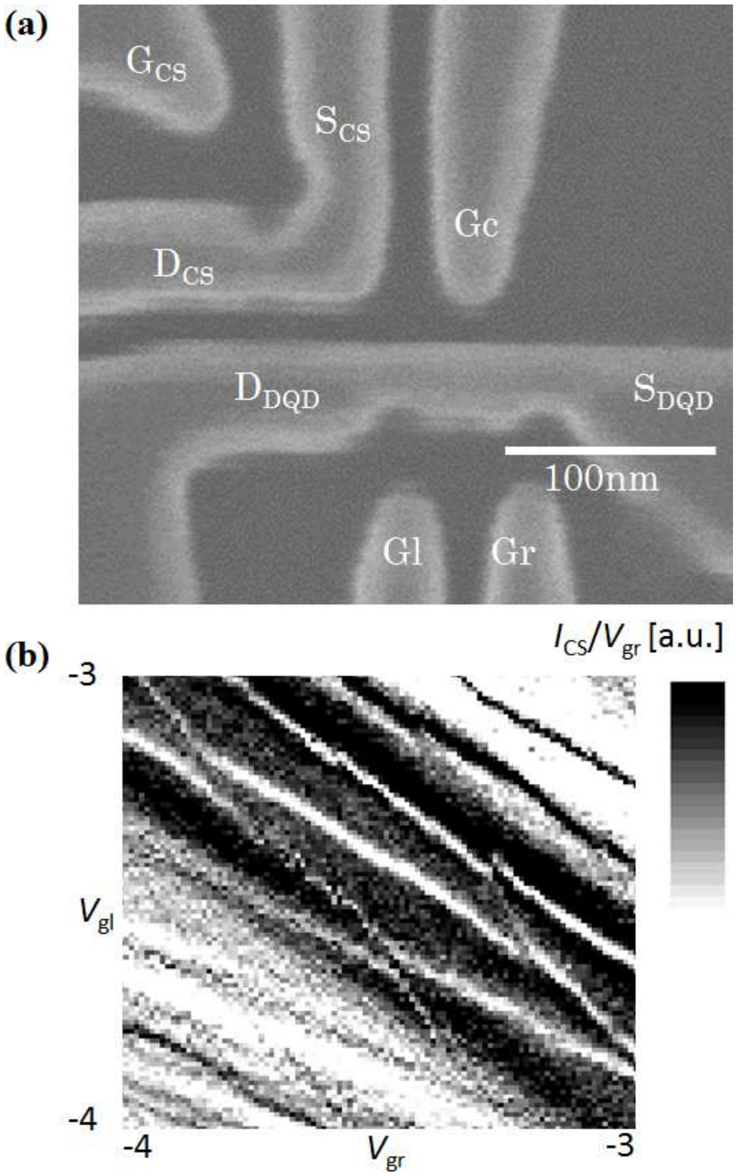


Fig.5.7: (a)SEM image of small DQD device. The QDs size is 35×26 nm^2 measured from scale bar. The position of Gl, Gr and CS is changed to change the QDs potential effectively without pinch off. (b) Differential conductance of the CS. Honeycomb structure is detected, however, the signal of the transition in right QD is weaker than that of left QD.

For the closer gate electrodes and smaller DQD, the device whose positions of the gate electrodes and charge sensor are changed is fabricated [Fig. 5.7 (a)]. The DQD device is fabricated without depositing the top gate electrodes for the simple fabrication and Gl and Gr, which modulates the potential of the QDs, are positioned the small DQD vicinity. Figure 5.7 (b) shows the charge stability diagram of the CS. The single-electron transition in the DQD is successfully read out as before devices. The sensing signal from the right QD is small and unclear because the right QD is away from the CS, which means the capacitance becomes low. From these results, we succeeded in controlling the number of electrons in the reduced size DQD. However, few-electron regime is not observed because of the low tunneling rate again. Because the DQD size is approaching the limit of the dry etching and EBL techniques for fabricating the device with high reproducibility, the fine modulation of the structure is challenging. Therefore, other ways than the reduction of the QDs size should be considered to reduce the number of electrons of the DQD.

5.6. Conclusions

In this chapter, we demonstrate the reading out of the electron number change of the DQD by the current through the CS integrated next the DQD. This technique is used to measure the single-electron position in the DQD and even the spin information in the DQD in the future. We also demonstrate the formation of the DQD by applying V_{bg} instead of V_{tg}. The device structure is one of the promising structures to form the DQD without any additional dot because of the clean interface of the SOI-BOX layer. The DQD without the top gate electrode is also fabricated its charge stability diagram is measured. The device structure is feasible to integrate other structures on the DQD such a magnetic or metal materials for the ESR and DQD integration; We also succeed in the fabrication of the small DQD with changing the constrictions, CS and gate electrode positions. However, few-electron regime is not observed with either device mainly because of the low tunnel rate.

Toward few-electron regime of the DQD which is originally targeted, the structure for excluding the electrons while maintaining high tunneling rate is required. Another problem is difficulty to detect the change in the number of electrons in the QDs apart. Therefore, we have to develop the technique to reduce the number of electrons by not only the QDs size reduction. We also note that the structure tends to be unstable from the environmental fluctuations because of no electromagnetic shielding by the top gate electrode.

Appendix: Electron temperature in QDs

To obtain the long coherence time of the charge and spin qubit using QDs, "electron temperature", which is the temperature of the electron in the QD, should be low. The presence probability of the electron is distributed in the levels of two or more at the same time when the energy level spacing of the QD is smaller than the thermal energy of electrons. Therefore, the high electron temperature becomes a major factor of the decoherence in the charge qubits. In the spin qubit, since the transition between the levels is limited not only by the energy level spacing but also the spin degree of freedom, the effect of the decoherence from the high electron temperature is small. However, the decoherence would occur indirectly by the effects such as the electron spin flip due to the spin-orbit interaction. Therefore, the measurement of the electron temperature in our QDs device is important for both the charge and spin qubits.

In this appendix, we measured the electron temperature of the QD by using the relationship of the Coulomb peak width and set temperature by the cryostat. Figure 5.8 shows a schematic of electron transport in the SET at the absolute zero and finite temperature.

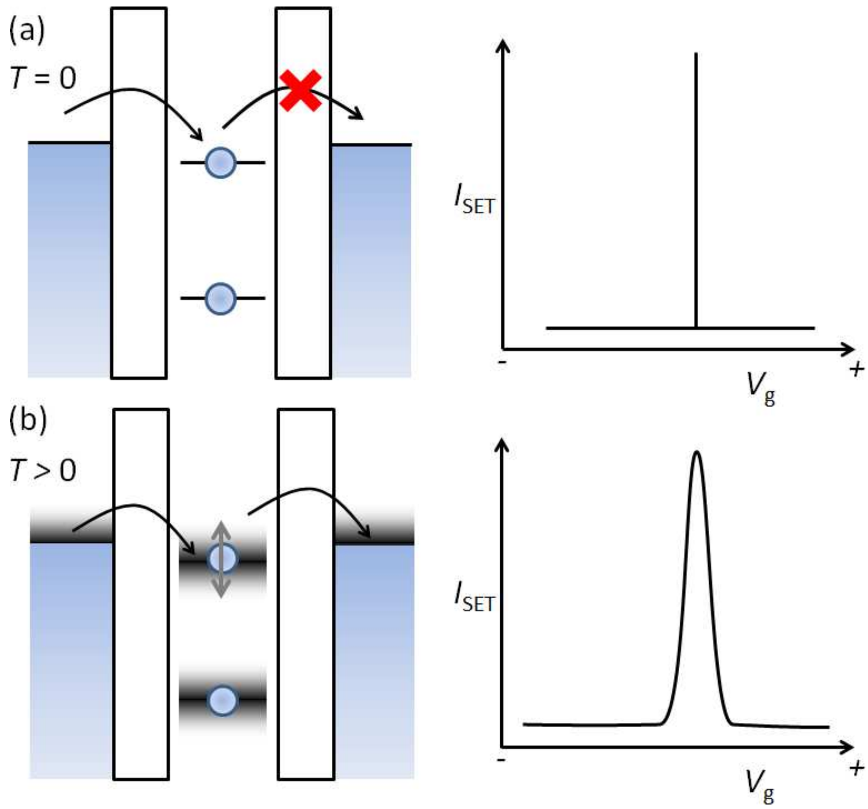


Fig. 5.8: energy diagram and I_{CS}-V_g of CS at (a) T =0 K and (b) T > 0 K. Because of fluctuation by thermal energy, Coulomb peak becomes broad at T > 0 K.

When $V_{ds} \simeq 0$ V at 0 K, I_{SET} flows only when the potential of the SET is the same as the Fermi energy of the leads and Coulomb peak becomes Δ function dependent on V_g [Fig. 5.8 (a)]. At finite temperature, I_{SET} flows in the region where the broaden level of the SET by the thermal energy is matched with Fermi energy of the leads [Fig. 5.8 (b)]. Therefore, the QDs device cooling by cryostat, the electron temperature does not always fall to the set temperature due to the coupling with the environment and electrons in the leads [55].

Figure 5.9 shows Coulomb peak with the base temperature from 0.3 K to 0.7 K by using the device of Fig. 5.1 [Fig. 5.9]. For clarity, an offset is given to each trace.

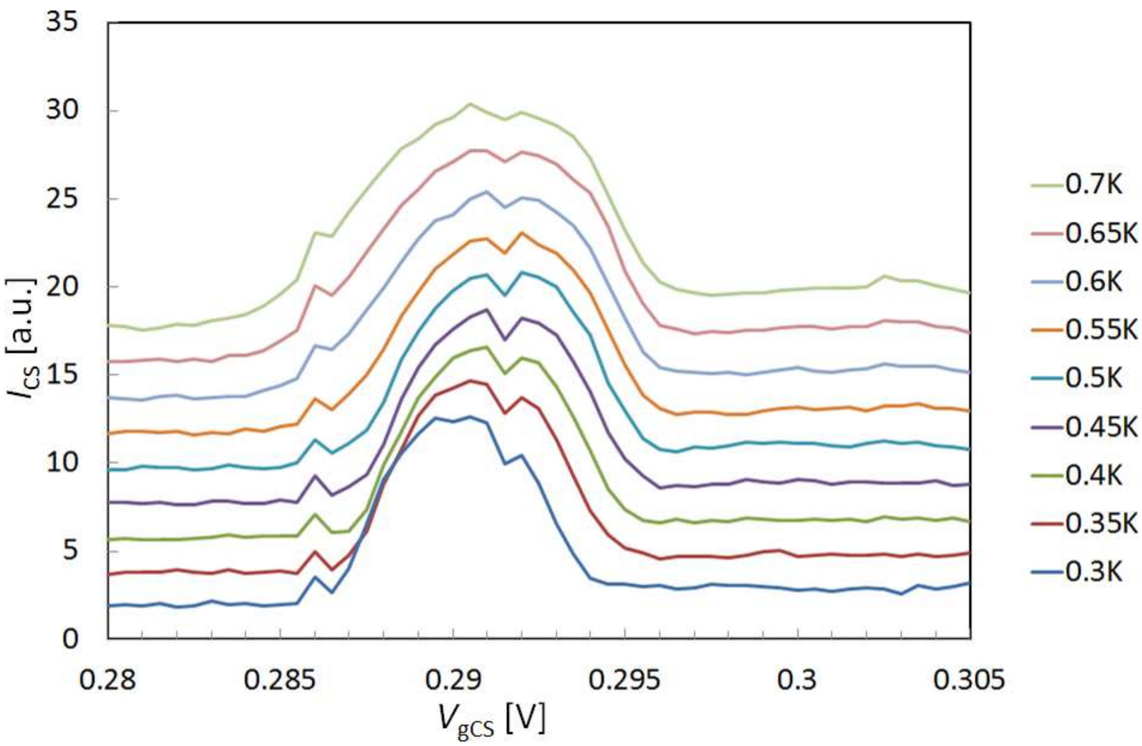


Fig. 5.9: I_{CS}-V_{gCS} characteristics with various base temperatures. The traces are given an offset for clarity. The Coulomb peak broadens with temperature increasing.

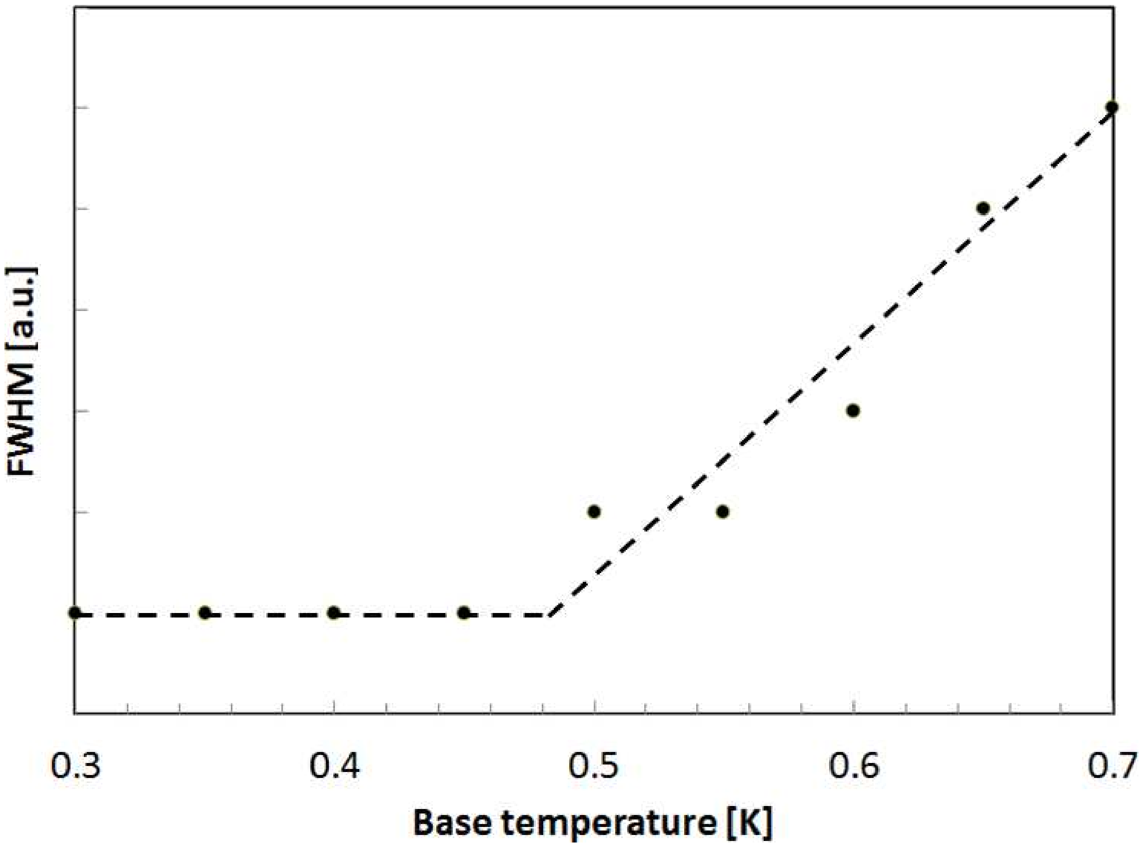


Fig. 5.10: Full width at half maximum (FWHM) versus base temperature to read out the temperature dependence of Coulomb peak. FWHM is increased over ~ 480 mK.

Figure 5.10 shows the full width at half maximum (FWHM) of the Coulomb peak at each base temperature. FWHM is increased at the temperature higher than ~ 480 mK, which means that the lowest electron temperature is 480mK. This measurement cannot be applied to the DQD because the shape of the current is strongly affected by the coupling strength. However, the electron temperature will be also the same, ~ 500mK because the coupling to the environment of the DQD may be approximately the same as the CS. The temperature is about the same as another Si QD, therefore, the value is reasonable [56].

Chapter 6: Dual Function of Charge Sensor: Charge Sensing and Gating

Abstract

In this chapter, we demonstrate gating and charge sensing functions of the lithographically defined QD. The electrochemical potential of the QD is modulated by applying a voltage to both the source and drain electrodes. The QD integrated with the DQD as a CS works as a gate electrode for the DQD. Charge transitions in the DQD are detected by the CS through its charge sensing function.

6.1. Introduction

Recently, qubits with semiconductors have been studied by many researchers because of their long coherence time of the electron spin. One or two qubits have already been achieved by several groups [14,19,21,57,58]. Many QDs are integrated to be used for not only qubits but also CSs to identify the position of an electron [58]. In addition to such QDs, many gate electrodes should be integrated to a qubit device to control the electrochemical potential of each QD and tunnel barriers between the QDs. However, the qubits and CSs also occupy a large space in the device. Such a large structure for qubits would be a problem in the integration of many QDs to achieve a quantum information processor. Therefore, technological development of QDs by multifunctionalization is required to reduce the number of gates and integrate many QDs.

In this chapter, we demonstrate gating and charge sensing functions of a lithographically defined QD. The electrochemical potential of integrated QDs is modulated by applying a voltage to both their source and drain electrodes independently. Since the modulation of the potential of a QD also changes the potential of another capacitively coupled QD, the QD works as a gate electrode for the other one. In addition, charge transitions in a DQD are successfully detected by the integrated QD through its charge sensing function.

6.2. Device Structure and Measurement Method

6.2.1. Device structure

The device structure we measured is shown in Fig. 6.1(a) as a bird's-eye view. Si DQD, CS, and gates are fabricated by electron beam lithography, dry etching, and thermal oxidation [59-61]. Constricted regions between QDs and reservoirs work as potential barriers for the DQD and SQD. The BG is used to induce two-dimensional electron gas at the lower Si/SiO_2 interface in the SOI layer, which acts as a gate of a MOSFET structure. The induced electrons flow from the source electrode to the drain electrode through the potential barriers and the QDs. Figure 6.1(b) shows a SEM image of a device with the same design as that measured in this experiment. The DQD and CS are schematically indicated by ovals. The thickness of the SOI layer is 30 nm, and that of the buried oxide layer is 145 nm.

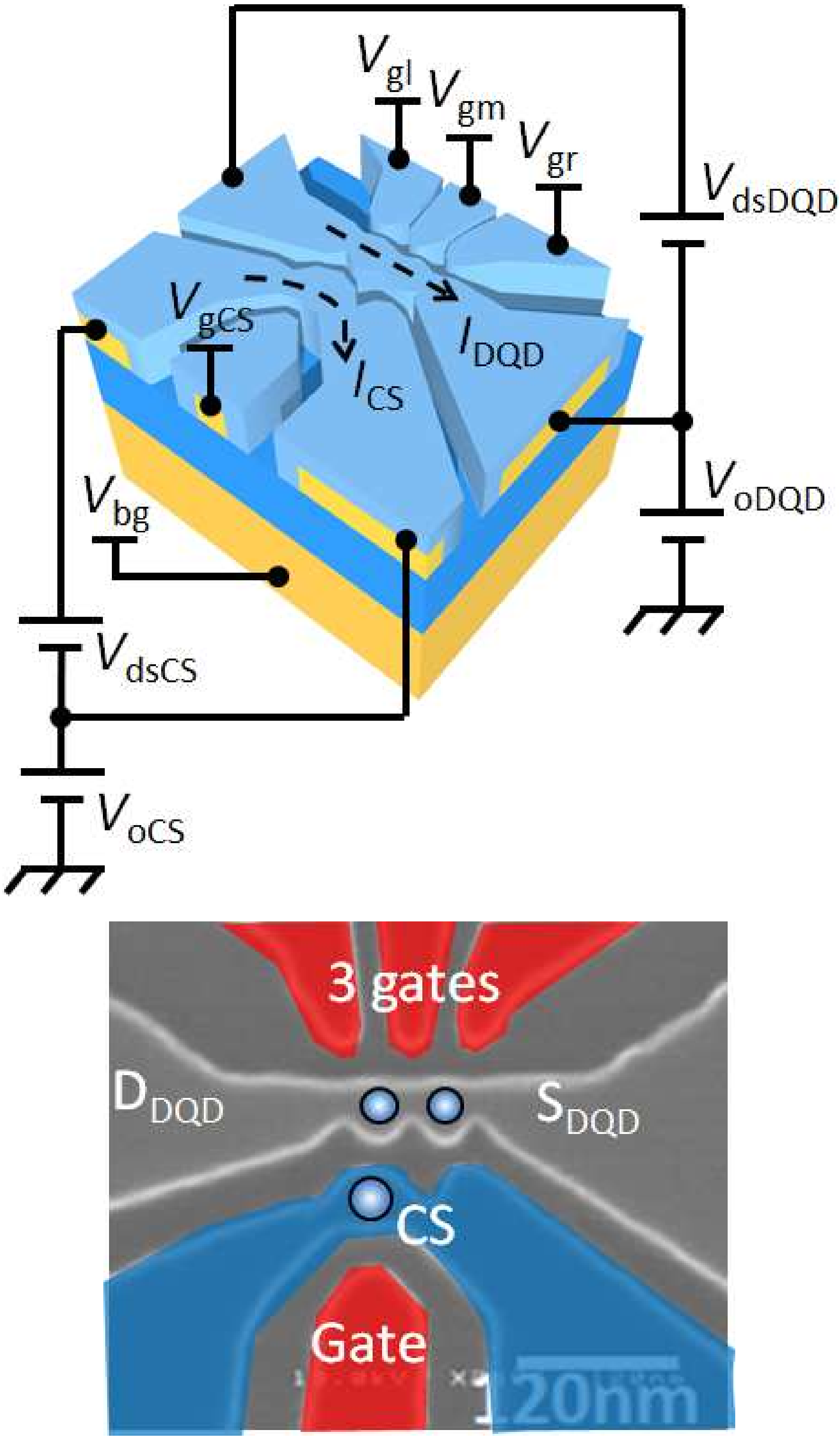


Fig. 6.1: (a) Schematic structure of QD device on SOI wafer. DQD, CS, and gates are insulated by dry etching and covered with the thermally oxidized SiO_2 and buried oxide. (b) SEM image with the same design as that measured. The DQD and CS are schematically indicated by ovals.

6.2.2.Measurement method

The voltages applied to the gates (V_{gl}, V_{gm}, V_{gr}, V_{gCS}, and V_{bg}) control the electrochemical potential of each QD and modify the tunnel rate of each potential barrier [59,60]. In a typical case, source voltages of all QDs are applied at a ground level for use as a reference voltage. On the other hand, in this study, we apply offset voltages of the DQD (V_{oDQD}) and CS (V_{oCS}) to tune the performance of each QD. V_{oDQD} (V_{oCS}) is applied to both the source and drain electrodes of the DQD (CS) [Fig. 6.1(a)]. Currents through the DQD (I_{DQD}) and CS (I_{CS}) flow from their drain to source electrodes, as indicated by dashed arrows. There is no leakage current between the QDs when different offset biases are applied because each QD is isolated by dry etching, thermal oxidation, and buried oxide. Source-drain voltages of the DQD (V_{dsDQD}) and CS (V_{dsCS}) remain constant during V_{oDQD} or V_{oCS} sweeping. The base temperature in this experiment is 250 mK.

6.3. Results and Discussion

6.3.1.Self-modulation by offset bias

Working all QDs on the same chip in good condition is difficult when they are driven by a common gate because the gate has different capacitances to all QDs in the device [59]. In addition to that, threshold voltages of the QDs are often different because of their shape difference due to the design of the QDs and/or a fluctuation in their fabrication process [Figs. 6.2(a) and 6.2(b)]. Applying a different offset voltage to each QD modulates the energy band bending of the QD itself and the number of induced electrons [Fig. 6.2(c)].

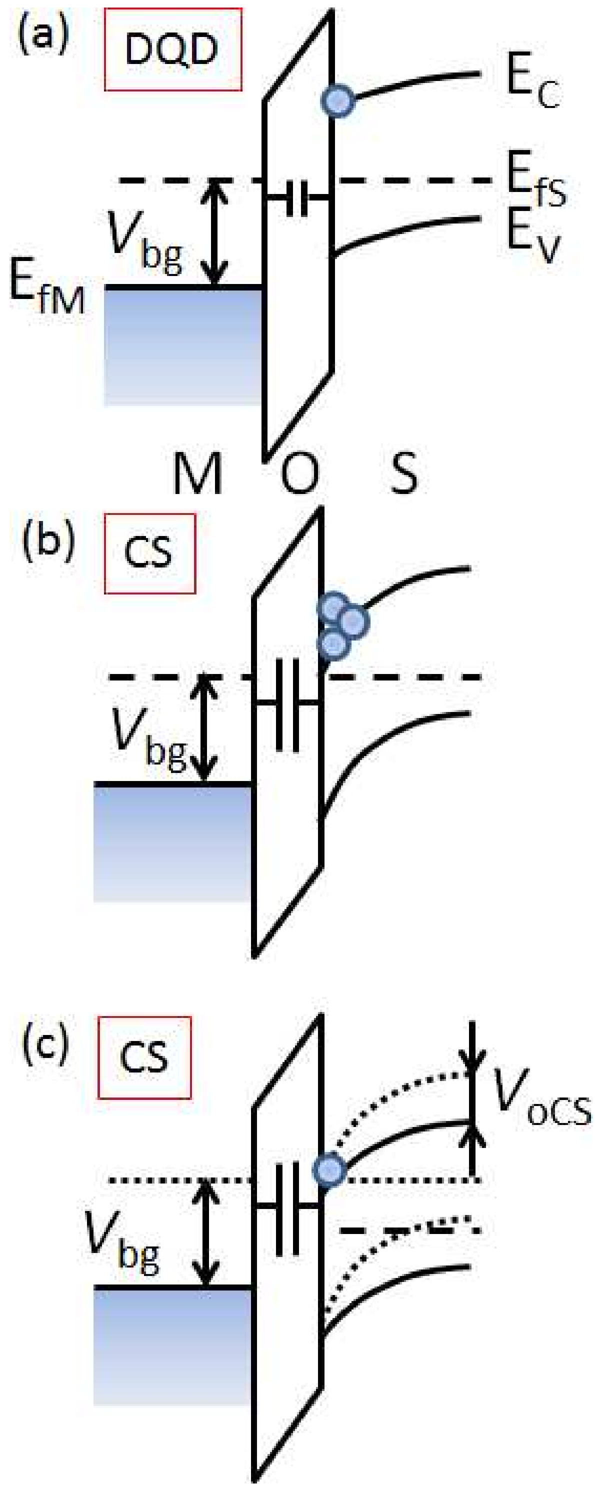


Fig. 6.2: Energy band schematics of the DQD (a) and CS (b, c). (a) A few electrons are induced in the DQD by V_{bg}. (b) More electrons are induced in the CS when the same V_{bg} as that of (a) is applied because the BG has a larger capacitance to the CS than to the DQD. (c) The number of electrons in the CS is reduced by applying V_{oCS}. The bending of the band in the SOI layer is modulated by each offset bias with the same V_{bg} to all QDs.

To confirm the effect of this technique, modulations of the Coulomb oscillations are measured [Figs. 6.3(a) and 6.3(b)]. Figure 6.3(a) shows the measured current traces of the CS as a function of the left and right gate voltages (V_{gl} and V_{gr}, respectively) with a change in V_{oCS} as a parameter. There are few small Coulomb peaks when V_{oCS} = 0 mV because of the low tunneling rate through the CS. When a negative V_{oCS} is applied, the potentials of the CS and the barriers relatively decrease because such potentials are defined by the difference between the applied voltages of the BG (V_{bg}) and V_{oCS}. Therefore, many large Coulomb peaks are observed when V_{oCS} = -150 mV [Fig. 6.3(a)]. Figure 6.3(b) shows a similar measurement of the DQD with the same applied V_{bg} as that in Fig. 6.3(a). The Coulomb peaks of the DQD are modulated by applying a negative V_{oDQD} in Fig. 6.3(b). From these results, we demonstrate the technique of activating the CS and DQD independently with the application of different offset voltages.

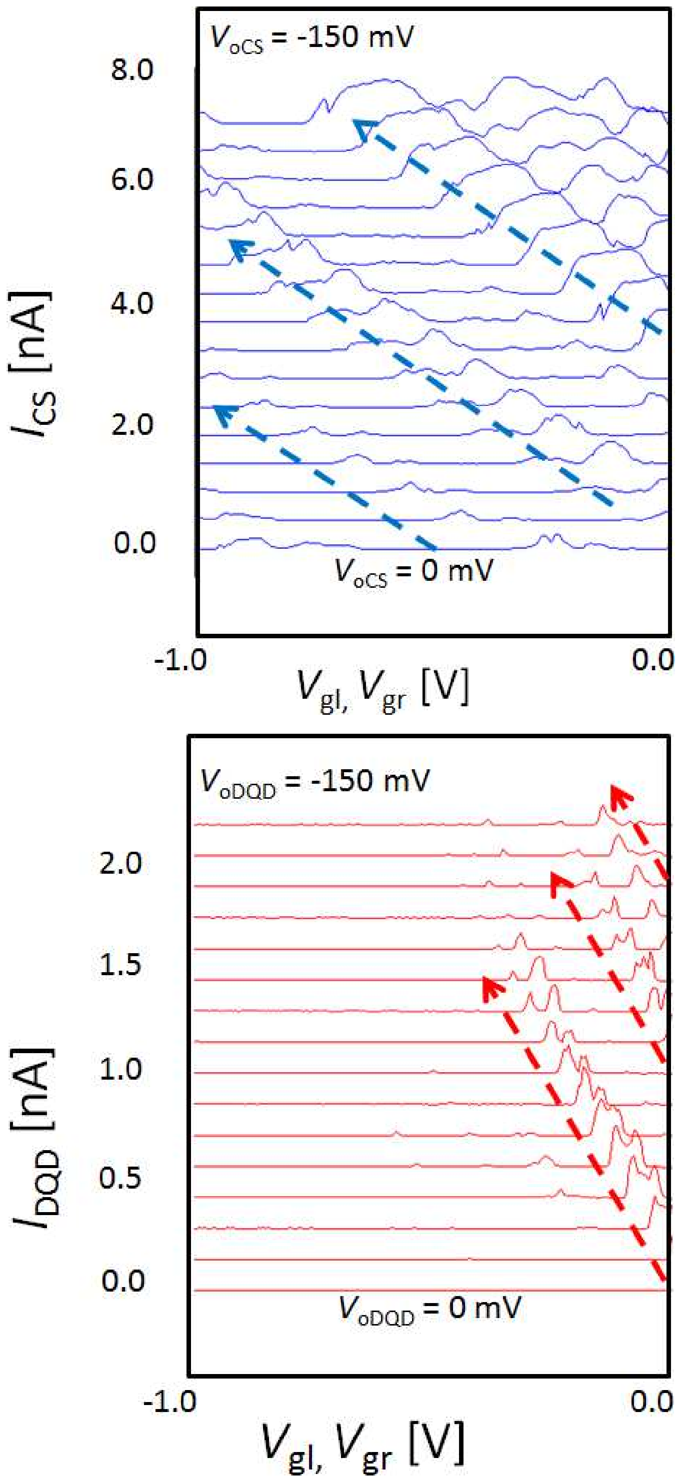


Fig. 6.3(a) $I_{CS} - V_{gr}$, V_{gl} characteristics for V_{oCS} between 0 mV (bottom trace) and -150 mV (top trace). The traces are given an offset for clarity. (b) $I_{DQD} - V_{gr}$, V_{gl} characteristics for V_{oDQD} between 0 mV (bottom trace) and -150 mV (top trace). The traces are given an offset for clarity.

6.3.2. Gating function of CS

Integrated G_l, G_m, G_r, and G_{CS}, which are fabricated with SOI, are used as gate electrodes for the DQD and CS. Electrons in the gates are induced by V_{bg} in the same way as the QDs and their number is modulated by changing the Fermi level of the gate. This means that QDs work as gate electrodes when an offset voltage is applied to the source and drain electrodes. Figure 6.4 shows the measured current traces of the DQD as a function of V_{gl} and V_{gr}. Here, from top to bottom, V_{oCS} increases from 70 to 260 mV in 8 mV steps. V_{dsDQD} = 5 mV and V_{dsCS} = 10 mV are fixed in all traces. An inter dot coupling of the DQD is so strong that the DQD behaves like an CS because of the low negative bias of the gates in Fig. 5.4 [62]. The Coulomb oscillation of the strongly coupled DQD shifts depending on the CS potential. As a result, the gate function of the CS is successfully demonstrated. We calculated the ratio of the capacitances of G_l and G_r (C_{glrDQD}) and the CS (C_{CSDQD}) to that of the DQD for comparison. $C_{CSDQD}/C_{glrDQD} = (e/\alpha\Delta V_{oCS})/(e/\alpha\Delta V_{glr})) = \Delta V_{glr}/\Delta V_{oCS} = 0.97$ is obtained, where α is the lever arm and ΔV_{oCS} and ΔV_{oglr} are the distances between the Coulomb peaks in Fig. 6.4 [63]. This gating effect of the CS, as well as those of the other gates, is sufficiently large to use.

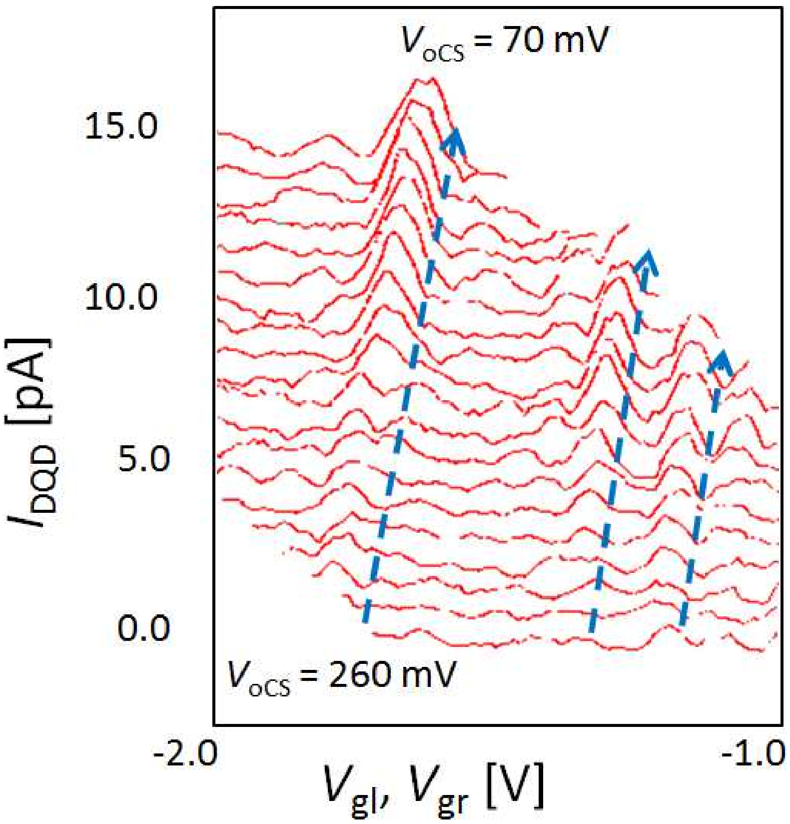


Fig. 6.4: Measured current traces of the DQD for V_{oCS} between 260 mV (bottom trace) and 70 mV (top trace). The traces are given an offset for clarity. Gray (red) arrows are used as visual guides. Positions of the Coulomb peaks are shifted by changing V_{oCS}.

6.3.3.Dual function of CS

The CS is useful for both charge sensing and gating functions because it is normally integrated next to the DQD to detect the charge transition sensitively [44,59,64]. Figure 6.5(a) shows a charge stability diagram of the DQD with the applied V_{oCS} = -0.2 V. A large current flows in several points. The points indicate triple points that are typical of a serially coupled DQD [60,65]. White dashed lines in Fig. 6.5(a) indicate the points where the number of electrons in the left or right QD of the DQD is changed. Figure 6.5(b) shows the differential conductance of the CS in the same measurement.

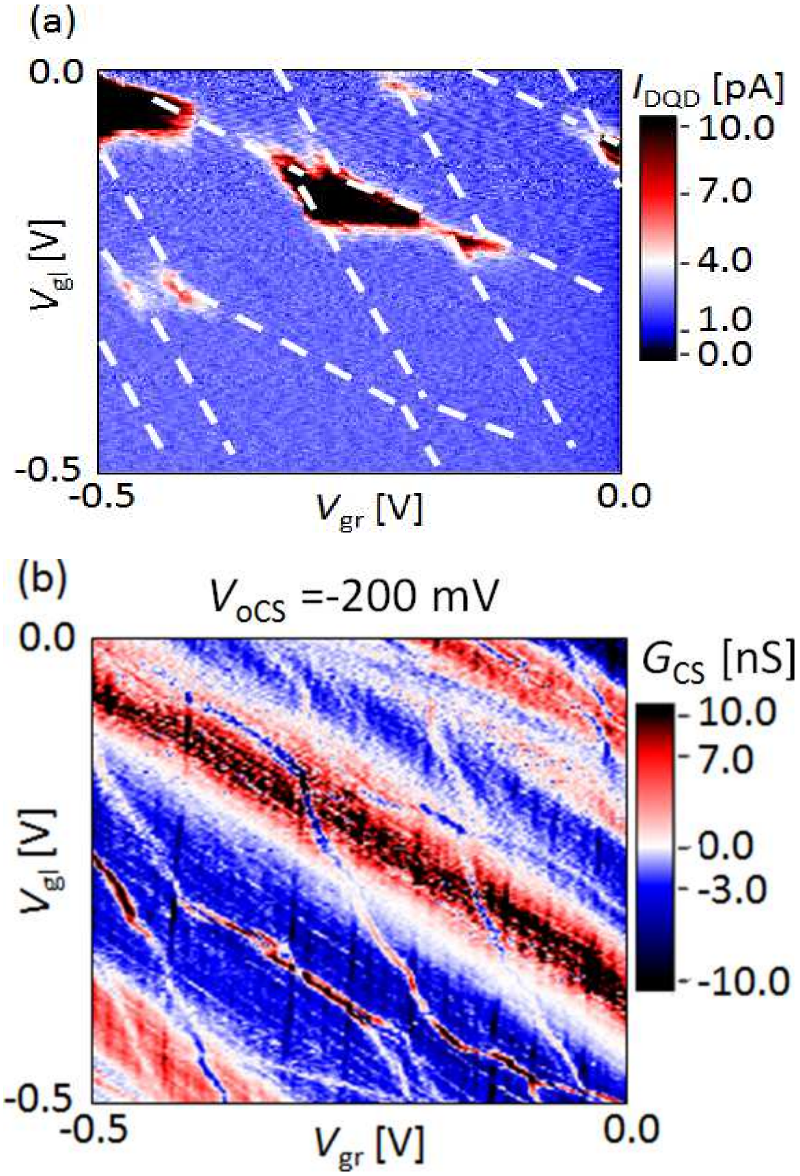


Fig. 6.5 (a) Charge stability diagram of the DQD. White dashed lines show the same lines in (b). (b) Differential conductance of the CS. The charge detection lines are clearly observed with V_{oCS} = -200 mV.

When the electron number in the DQD is changed, the differential conductance is changed simultaneously because of the electric field from the DQD [43,66]. To obtain the large signal of charge detection, we should set the potential of the CS where its Coulomb oscillation is sharp and large. By applying a low negative V_{oCS}, the charge sensing lines become unclear [Figs. 6.6(a)-6.6(c)]. V_{oCS} set the CS to the best condition for charge detection by its charge sensing function and the formation of the DQD by its gating function [Fig. 6.5(b)].

To integrate many QDs, many gates and CSs should also be integrated in the same device [67]. This multifunctional QD will save space in the device and enable a large-scale integration for the quantum calculation [Fig.6.7].

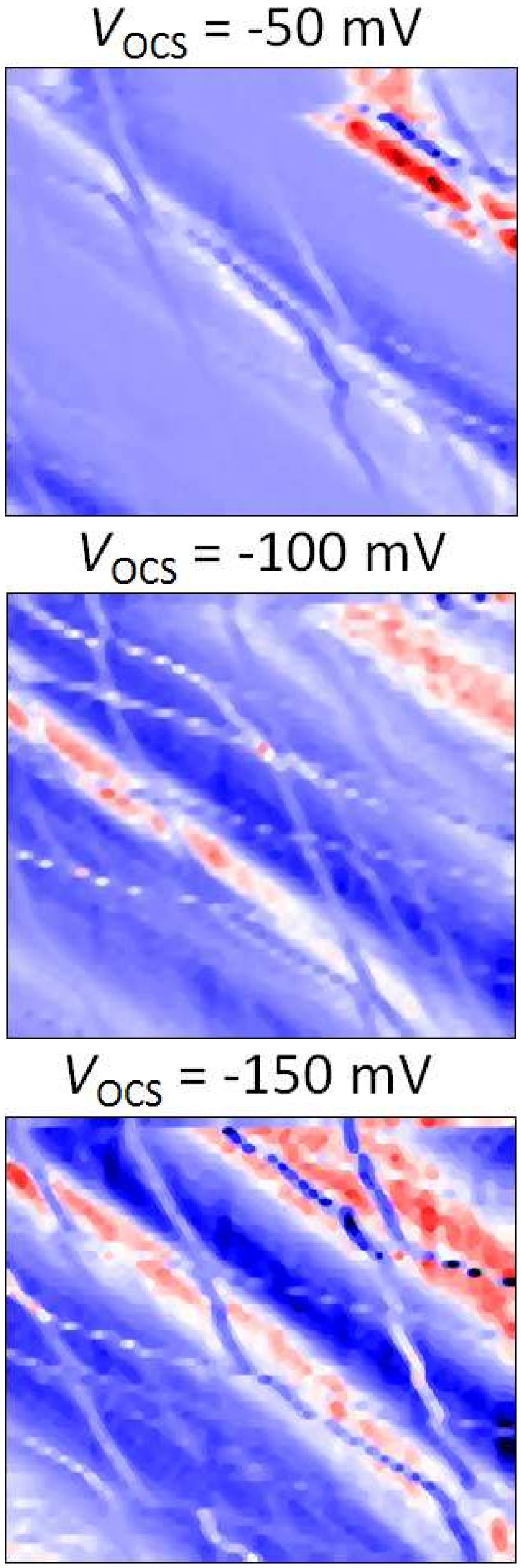
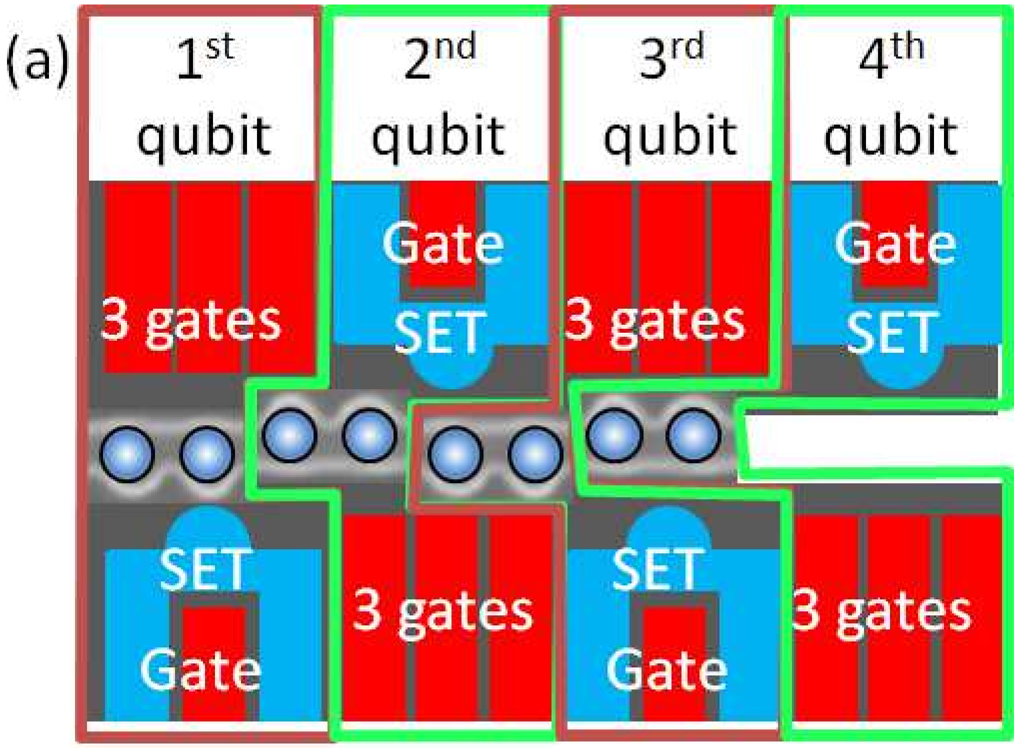


Fig. 6.6 (a-c) Differential conductances of the CS with different V_{OCS} values of -50 (a), -100 (b), and -150 mV (c). The charge sensing lines are less clear than that in Fig. 6.5(b).



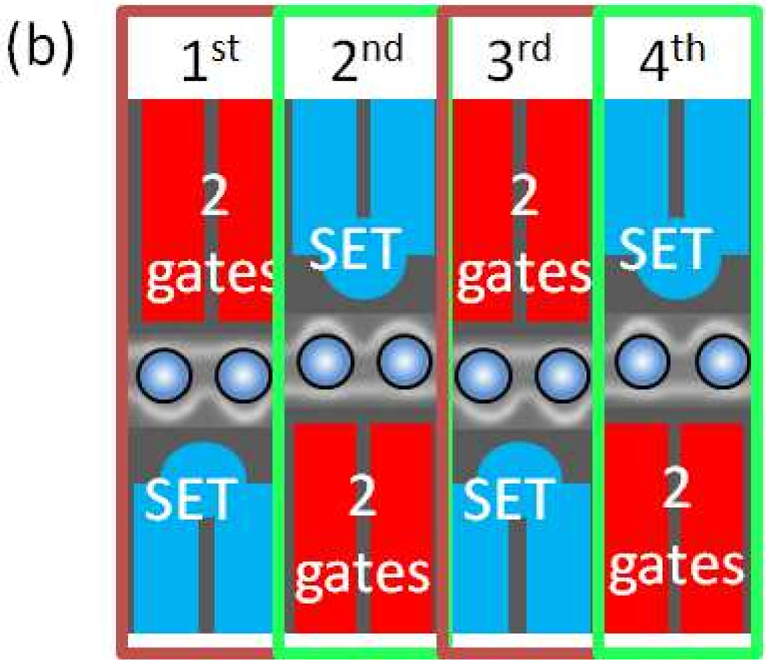


Fig. 6.7: (a) QDs integration with 4 gate electrodes and an SET for the CS. The potential modulation for each QD is impossibile. (b) QDs integration with decreased gate electrodes because of the gating function of the CS. The integration is feasible with the DQD device used in this work.

6.4. Conclusions

In this chapter, we demonstrated a modulation of Coulomb oscillations of the lithographically defined DQD and CS by applying offset biases. The modulation technique is used to set the condition of each QD independently. We also developed the gating function of the CS to actively control the electrochemical potential of the integrated DQD for the first time. The CS isolated by dry etching shows this additional function. Finally, the detection of the charge transitions in the serially coupled DQD by the CS using its gating function is successfully demonstrated. This multifunctional QD is a useful device for not only flexible measurements in various QD devices but also the integration of qubits with a small number of gate electrodes for a quantum computer.

Chapter 7: Analysis of Electron Spin Resonance with Ferromagnets and Si DQD

This chapter is non-disclosure because the data will be published.

Chapter 8: Conclusions

The main results of this study can be summarized as follows:

1. Develop the Si coupled QDs device for single spin qubit and its integration
2. Design and fabricate the Si DQD for ESR and observe blockade region

About the 1st result, the CS is integrated with the Si DQD to read out the position of electrons in the DQD, and the single-electron transition in the DQD is actually measured by the transconductance of the CS. The gating function of the CS with its charge sensing function is also developed. The dual functionality enables the reduction of the number of electrons of the DQD and gate electrodes, and the integration of the multiple quantum dots. The offset bias of the CS modulates the operating bias of the CS itself, and then, the charge sensing is available in the preferable region of the DQD.

About the 2nd result, we discuss about that the ESR method by using the ferromagnets is suitable in the Si DQD device using in this work and investigate the device structure for actual spin qubits device. As a result, by thinning the top gate electrode thickness, 7 MHz Rabi frequency and the small difference of the RF frequency for the resonance in the left and right QD are calculated. The difference of the RF frequency becomes larger than 200 MHz, which is easy to distinguish and Rabi frequency becomes 5 MHz by optimizing the shape of the structure.

From the measurement of the DQD device with ferromagnet, the blockade region in several bias triangles is observed. From the magnetic field dependence of the leakage current in the blockade region, the blockade region is by valley-spin blockade. By applying RF to the gate electrode in the current hot spot, distant current peaks are observed. The center frequency of the peaks agrees well with the expectation from the magnetic field calculation, which suggests the current peaks are by ESR.

The ESR is occurred by the strong local magnetic field even when the external magnetic field is zero because of the large remnant magnetization of the anisotropic ferromagnets. This new ESR technology with only the local magnetic field has a potential of long coherence time because the decoherence by spin-orbit interaction induced by the magnetic field is strongly suppressed.

These results are significant progresses to implement the Si spin-based qubit and its integration. The Si DQD devices for the development of the element technologies in this work are still fabricated in the range of conventional Si-MOSFET process. Thus, these developed technologies are useful to make the actual quantum information processing.

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Publications

Journal Publications

1. **T. Kambara**, T. Kodera, Y. Arakawa, and S. Oda, “Dual Function of Single Electron Transistor Coupled with Double Quantum Dot: Gating and Charge Sensing,” *Jpn. J. Appl. Phys.*, vol. 52, p. 04CJ01, Feb. 2013.

2. **T. Kambara**, T. Kodera, T. Takahashi, G. Yamahata, K. Uchida, and S. Oda, “Simulation Study of Charge Modulation in Coupled Quantum Dots in Silicon,” *Jpn. J. Appl. Phys.*, vol. 50, no. 4, p. 04DJ05, Apr. 2011.

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1. **T. Kambara**, T. Kodera, G. Yamahata, K. Uchida, S. Oda, “Simulation study of charge modulation in coupled quantum dots in silicon” Solid State Devices and Materials Conference, Extended Abstracts September 2010 Tokyo

2. **T. Kambara**, T. Kodera, Thierry Ferrus, Alessandro Rossi, K. Horibe, Yasuhiko Arakawa, David Williams, and Shunri Oda, “Charge detection techniques in Si double quantum dots”, G-COE PICE International Symposium and IEEE EDS Minicolloquium on Advanced Hybrid Nano Devices: Prospects by World’s Leading Scientists, October 2011 Tokyo

3. **T. Kambara**, T. Kodera, S. Oda, “Dual Function of Charge Sensor: Charge Sensing and Gating”, Solid State Devices and Materials Conference September 2012 Kyoto

4. **T. Kambara**, T. Kodera, Yukio Kawano, Yasuhiko Arakawa and S. Oda, “Micro

magnets on lithographically-defined Si double quantum dots for electron spin resonance", IEEE EDS WIMNACT-37 February 2013 Tokyo

5. T. Kodera, G. Yamahata, **T. Kambara**, T. Ferrus , D. Williams, S. Oda, Y. Arakawa, "Improvements of transport properties in silicon quantum dots", International Symposium on Quantum Nanophotonics and Nanoelectronics (ISQNN 2009), ThP-4, pp.76, Tokyo, Japan (November 2009)

6. T. Kodera, G. Yamahata, **T. Kambara**, T. Ferrus, D. A. Williams, K. Uchida, Y. Arakawa, S. Oda, "Fabrication and characterization of silicon double quantum dots towards spin qubits", G-COE PICE International Symposium on Silicon Nano Devices in 2030: Prospects by World's Leading Scientists October 2009 Tokyo

7. T. Kodera, **T. Kambara**, K. Horibe, G. Yamahata, K. Uchida, and S. Oda, "Silicon Quantum Dots for Spin-Based Quantum Information Processing", 2nd Japanese-Russian young scientists conference on nano-materials and nano-technology, Tokyo, Japan, (September 2010)

8. T. Kodera, G. Yamahata, **T. Kambara**, K. Uchida, C. M. Marcus, and S. Oda," Magnetic field dependence of a leakage current in Pauli-spin blockade regime of silicon double quantum dots", School and conference on Spin-based quantum information processing, A48, Konstanz, Germany, (August 2010)

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11. G. Yamahata, **T. Kambara**, K. Uchida, C. M. Marcus, S. Oda ,T. Kodera, "Pauli spin blockade in a lithographically-defined silicon double quantum dot", International Symposium on Quantum Nanostructures and Spin-related Phenomena March 2010

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13. K. Horibe, T. Kodera, **T. Kambara**, K. Uchida, S. Oda , "Fabrication of few-electron silicon quantum dot devices based on an SOI substrate with a top gate contact", G-COE PICE International Symposium and IEEE EDS Minicolloquium on Advanced Hybrid Nano Devices: Prospects by World's Leading Scientists, October 2011 Tokyo

14. T. Kodera, K. Horibe, **T. Kambara**, G. Yamahata, K. Uchida, Y. Arakawa, S. Oda, "Observation of few-electron regime and suppression of inter-dot tunneling in silicon quantum dots", the International Conference on Quantum Information Processing and Communication 2011 (QIPC 2011), CS-8, September 2011 Zurich Switzerland

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17. T. Kodera, K. Horibe, W. Lin, **T. Kambara**, T. Ferrus, A. Rossi, K. Uchida, D. A. Williams, Y. Arakawa, and S. Oda, "Charge Detection in Silicon Quantum Dots Coupled in Parallel", IEEE Silicon Nanoelectronics Workshop June 2011 Kyoto

18. T. Kodera, K. Horibe, **T. Kambara**, G. Yamahata, K. Uchida, Yasuhiko Arakawa, Shunri Oda, "Observation of Pauli-Spin Blockade and Single-Electron Regime in

Silicon Coupled Quantum Dots", 7th International Nanotechnology Conference on Communication and Cooperation (INC7) May 2011 Albany

19. K. Yamada, T. Kodera, **T. Kambara**, Y. Kawano, S. Oda, "Fabrication and Characterization of p-Channel Si Double-Quantum-Dot Structures", Solid State Devices and Materials Conference September 2012 Kyoto

20. T. Ferrus, A. Rossi, T. Kodera, **T. Kambara**, W. Lin, S. Oda, and D.A. Williams, "Microwave manipulation of electrons in silicon quantum dots", IEEE Silicon Nanoelectronics Workshop June 2012 Honolulu

21. K. Horibe, T. Kodera, **T. Kambara**, Y. Kawano and S. Oda, "Two-electron silicon double quantum dots fabricated for spin-based qubit application", IEEE EDS WIMNACT-37 February 2013 Tokyo

22. Ko Yamada, T. Kodera, **T. Kambara**, Yukio Kawano and S. Oda, "Observation of Few-Hole Regime through p-channel Si Double Quantum Dots", IEEE EDS WIMNACT-37 February 2013 Tokyo

Domestic conference

1. **蒲原知宏**，小寺哲夫，山端元音，内田建，小田俊理, "サイドゲートとトップゲートを用いたシリコン二重結合量子ドット形成シミュレーション", 第 71 回応用物理学会学術講演会, September 2010 長崎市

2. **蒲原知宏**，小寺哲夫，山端元音，内田　建，小田俊理, "ダブルトップゲートを有するシリコン量子ドットのシミュレーションと作製", 第 57 回応用物理学関係連合講演会 March 2010 平塚市

3. **蒲原知宏**，小寺哲夫，小田俊理, "バックゲートとソース/ドレイン電圧印加による各量子ドットの電気化学ポテンシャル制御", 第 73 回応用物理学会学術講演会 September 2012 松山市

4. **蒲原知宏**，小寺哲夫，Thierry Ferrus，Alessandro Rossi，堀部浩介，荒川泰彦，David Williams，小田俊理, "シリコン 2 重結合量子ドットの少数電子領域観測へ向けた構造

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