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Doctoral Thesis

A Study on Semiconductor Interfaces with Rare Earth Oxide and Ni Silicides for High Performance InGaAs MOSFETs

A Dissertation Submitted to the Department of

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A Study on Semiconductor Interfaces with Rare Earth Oxide and Ni Silicides for High Performance InGaAs MOSFETs

Daryoush Hassan Zadeh

Abstract

The extreme advances in electronic technology is mainly been made possible due to continuous scaling of Si-based MOSFETs. However, it is getting ever more difficult to enhance MOSFET performance on Si platform due to inherent limitations of Si material. Various booster technologies, together with new device designs have been proposed to extend the Si roadmap, however the uncertainty of Si-device lifetime has sparked a wave of research on new channel material with superior transport properties. InGaAs in particular has been identified as a suitable candidate due to the beneficial qualities it can offer in terms of, transport properties, immunity to short channel effects and band to band leakage current, and maturity of fabrication. On the Other hand, in order to realize InGaAs-based devices in industrial level, various issues must be tackled. Among these issues, achieving a high quality high-k/InGaAs interface can be named as one the most important ones. InGaAs has greatly benefited from the introduction of high-k material since InGaAs does not possess a natural high quality oxide similar to Si. Various high-k materials have been tried on InGaAs but so far only atomic layer deposited Al_2O_3 has been able to provide a high quality interface necessary with small density of defects at the interface. Although the Al_2O_3 has enabled InGaAs-based device demonstration in various designs, the small k-value of Al_2O_3 (k~9) will make it inevitable to replace it with oxides with higher k-value in order to increase the gate controllability over channel charge in quasi-ballistic device regime of 10 nm or smaller. Therefore, it is still necessary to investigate a high-k oxide which is able to achieve a high quality interface with InGaAs and simultaneously leave the prospects for its application in ultra-scaled structures open.

In this thesis, the interface characteristics of $La_2O_3/In_{0.53}Ga_{0.47}As$ are studied. La_2O_3 is a rare-earth oxide with a high k-value (~24). It was found that an amorphous interfacial layer is formed reactively at the $La_2O_3/In_{0.53}Ga_{0.47}As$ interface in the form of $LaInGaO_x$. The thickness, composition and thermal stability of this interfacial layer were found to be controllable through the supply of oxygen. A careful selection of gate metal (TiN/W) with balanced control supply, resulted in the formation of high quality interface with excellent electrical characteristics. Near ideal *CV* characteristics (high-frequency), and interface state density in the order of 10^{11} ($eV^{-1}cm^{-2}$) which is lower than other reported high-k/InGaAs interfaces, was achieved. A gate stack with La-silicate structure formed by intermixing La_2O_3 and thin Si layer is also proposed. Upon process optimization excellent thermal stability (up to 620^oC) and an effective k-value of 19 was obtained.

Another critical issue facing the InGaAs-based MOSFETs is the formation of low resistance Source/Drain (S/D) regions. Conventional doping methods are reported to be insufficient and ineffective for short channel InGaAs devices. Commonly, a Ni-InGaAs alloy contact is used to form metallic contacts for S/D regions of InGaAs MOSFET. However, small thermal stability and difficulty in controlling alloy composition would make its application difficult for future nodes. In this thesis a $NiSi_2$/InGaAs Schottky contact is introduced. A non-alloyed interface with high thermal stability and good electrical properties was achieved. Finally, InGaAs-MOSFET operation with high-k gate stack and metal S/D is confirmed.

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Chapter 1

Introduction

Chapter 1 Introduction

1.1 The Scaling of MOSFET Transistors

The phenomenal advances in modern society have largely been made possible due to our ability to send/receive, process and store large volumes of information which is unprecedented in human story. The innovation of computers, cell phones, internet, etc. is all a testimony to humans' insatiable desire to analyze the world around them and communicate their findings, feelings and thoughts with others. At the heart of these technologies, is the fundamental building block of any circuitry, Metal-Oxide-Semiconductor Field Effect Transistors (MOSFET). It's the miniaturization, i.e. "Scaling", of field effect transistors that has led to continuous progression in the performance of electronic devices. The scaling rule which was first published by R. Dennard [1.1] is very simple, it states that if the device dimensions and supply voltage of MOSFETs are reduced by a factor of α, then the circuit operation speed is increase by the same factor α. (Figure 1.1) Also the power dissipation of the circuit is reduced by a factor of α^2.

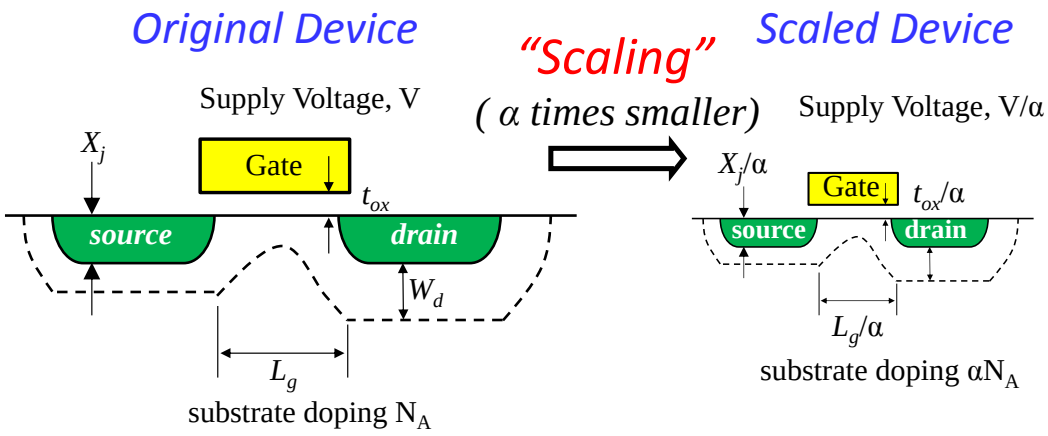

Figure 1.1 Principles governing scaling rule.

Following this guideline has allowed increased functionality per unit chip-area, increased performance, reduced device switching power and most importantly reduced cost per device year after year. Figure 1.2 shows the scaling trend of MOSFETs [1.2]. Every two years, the number of transistors packed to unit chip area is doubled, accompanied by almost 50% reduction in the cost of each transistor. This trend is universally known as "Moore's Law".

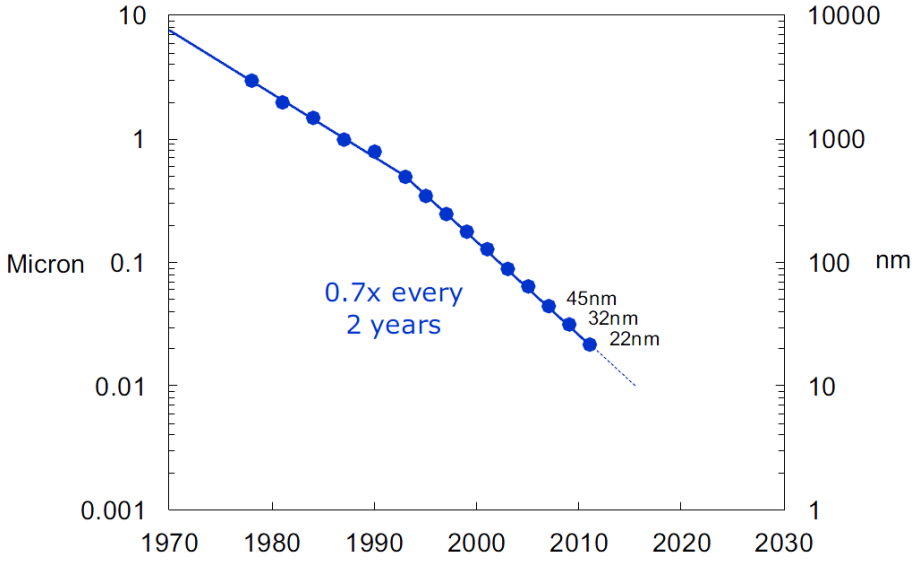

Figure 1.2 Device scaling according to Moore's law [1.2].

Traditionally Silicon dioxide (SiO_2) was used as the MOSFET gate dielectric, since it is possible to achieve an almost ideal interface with Si with very low defects at the interface and a very good thermal stability. The thickness of SiO_2 was also reduced in each generation of MOSFETs in accordance with the scaling law; however as the SiO_2 thickness reached about 1.2 nm, which is only a few atomic layers of SiO_2 molecules, new set of issues were faced [1.3]. At this level of thickness, carriers within the Si substrate (electrons) start to flow through SiO_2 due to tunneling effect, rendering insulating properties of SiO_2 seriously hindered. As a result, a dramatic increase in gate leakage current and a subsequent increase in both active and standby (passive) power consumption of the circuits, as illustrated in Figure 1.3, were not negligible [1.4].

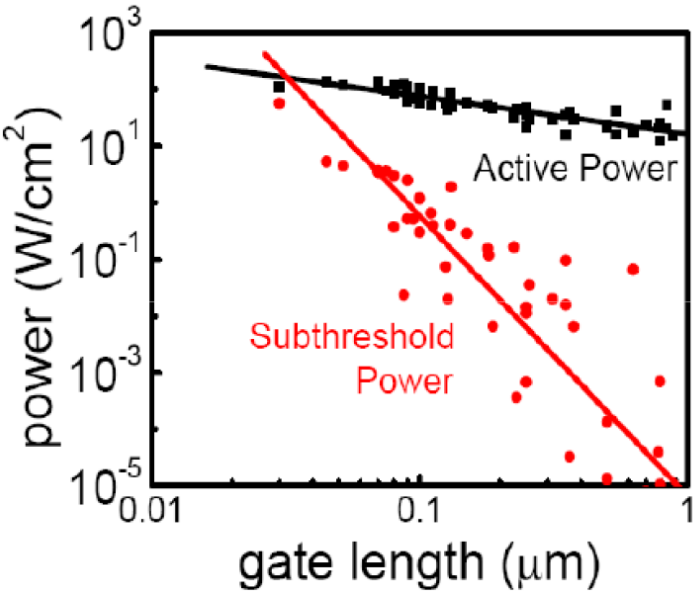

Figure 1.3 Power density of device as a function of gate length [1.4].

This huge obstacle in scaling trend, sparked a massive research amongst engineers and physicists to find a suitable gate dielectric which could replace SiO_2. High dielectric constant materials (high-*k*) were proposed as a solution to this crisis [1.5]. By using high-*k* materials as gate dielectrics, the physical thickness of dielectric could be increased while preserving a large gate capacitance. The increase in dielectric thickness could resolve the direct tunneling problem, thus relaxing the power consumption crisis.

Meanwhile, poly-Si gate electrode, which was also traditionally used as the MOSFET gate electrode, was replaced by metal electrode such as TaN, TiN, W, in order to suppress the depletion layer in the poly-Si gate at scaled gate lengths. The formation of the depletion layer increases the equivalent oxide thickness (EOT) of the gate insulator.

Figure 1.4 shows the schematic illustration and real device example for replacement of Poly-Si/SiO_2 with high-k/metal gate.

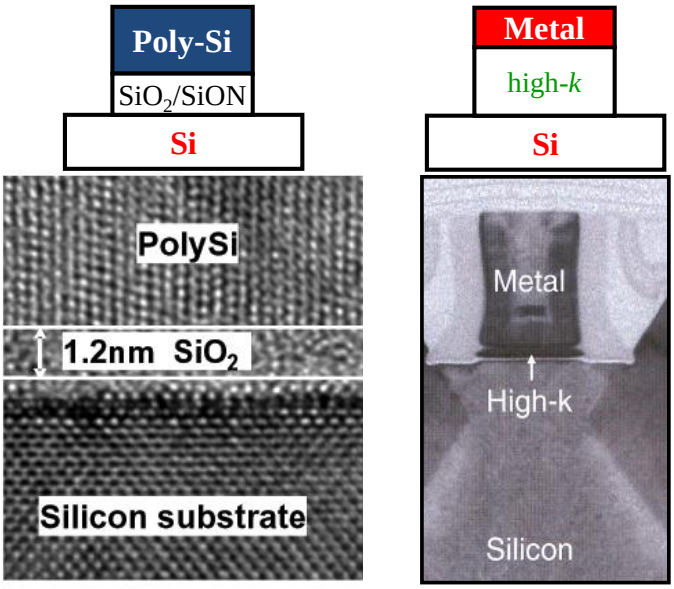

Figure 1.4 Replacement of SiO_2 and poly-Si at gate dielectric and gate electrode (left) with high-*k* and metal material (right) respectively [1.3],[1.5].

Reducing the EOT of MOSFET gate stacks in accordance with gate length scaling, is of outmost importance due to appearance of two physical phenomena as the scaling becomes aggressive. These two effects are Drain Induced Barrier Lowering (DIBL) and Short-Channel Effect (SCE) [1.6]. Both of these effects need to be suppressed so that the desired performance from a scaled device can be derived.

The requirements for selecting a high-*k* dielectric as the new oxide are:

1- A dielectric constant value high enough to allow for scaling to continue for several generations

2- Thermal stability

3- A large band gap, band offset of over 1 eV with semiconductor is necessary to minimize carrier injection from semiconductor to the oxide

4- High quality interface with semiconductor channel

Dielectric constant and band gap of an oxide has a reverse relationship that must be considered in order to apply a dielectric in a MOSFET gate stack structure. Higher dielectric constant material have smaller band gap, which means the potential barrier for carriers at oxide/semiconductor becomes smaller allowing them to penetrate through the oxide. The relationship between the band gap and dielectric constant value of several high-*k* oxides is shown in Figure 1.5 [1.7].

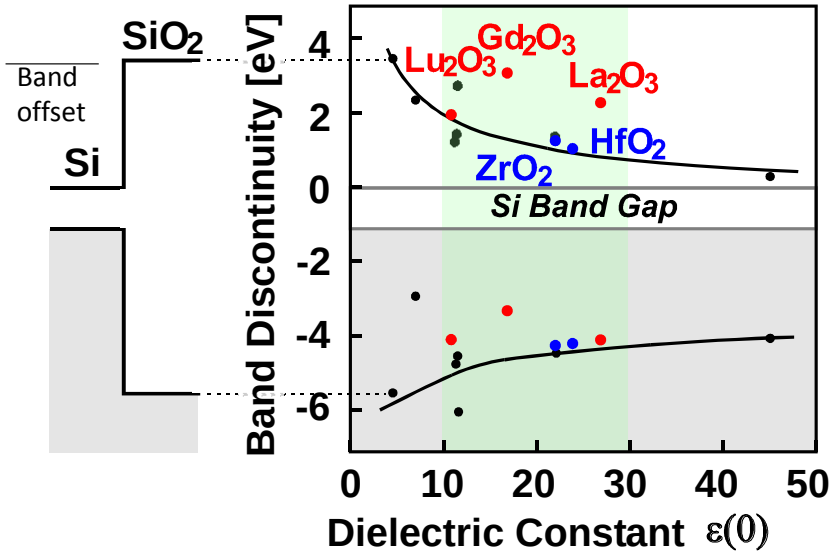

Figure 1.5 Dielectric constant versus band offset for various high-k gate dielectrics [1.7].

The oxides within the green zone are the ones with acceptable band gap and dielectric constant trade off. The successful implementation of high-*k* metal gate stack in an industrial level was first announced by Intel in 2007 in 45 nm production, using HfO_2-based gate insulator.

1.2 Limits of Scaling Beyond 20 nm Node

As mentioned in the previous chapter, device scaling was fundamentally the main factor for improving the transistor performance. However, miniaturization of the device inherently creates trade off relationships between three main areas of MOSFET

performance as well. These three main areas are 1- MOSFET drive current (I_{ON}), 2- power consumption and 3- short-channel effects.

The relationship between drain current and gate voltage (I_{ds} -V_g) of MOSFETs is shown in Figure 1.6.

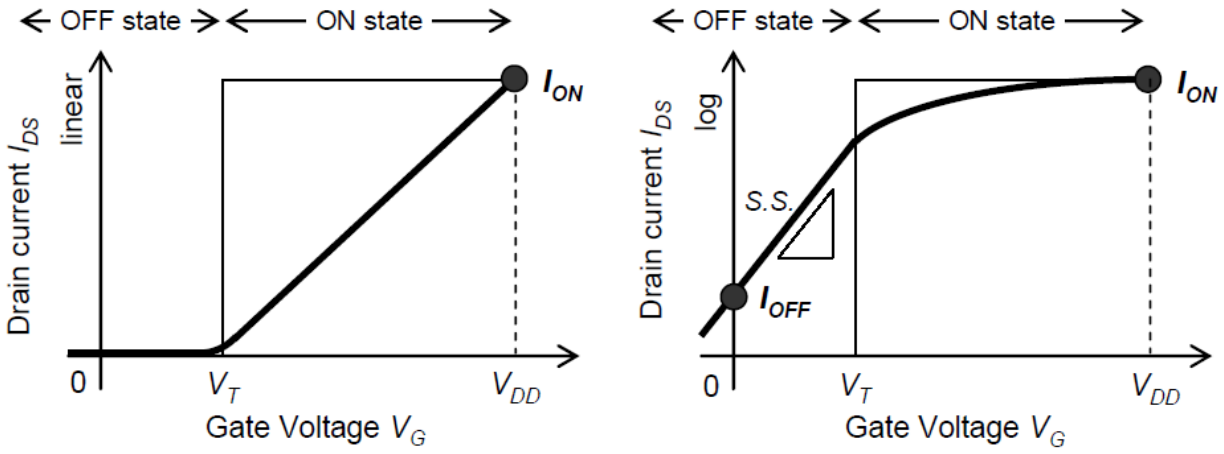

Figure 1.6 (a) linear, and (b) logarithmic I_{ds}-V_g characteristics of an nMOSFET

The total power consumption in a CMOS circuit can be separated to two components, dynamic power (when the transistor is ON) and static power (when the device is OFF). Power consumption and drive current (I_{ON}) of a MOSFET can be related to device parameters approximately by the following equations [1.8]:

$$P_{consumption} \approx afC_{load}V_{dd}^2 + I_0.10^{\frac{V_{th}}{S}}.V_{dd} + I_{leak}.V_{dd} \quad (1.1)$$

$$I_{ON} \approx C_g(V_{dd} - V_{th}).\upsilon(V_{dd}) \quad (1.2)$$

Here a is a constant value, f is the operating frequency, C_{load} is the load capacitance, I_0 is the drain current at V_g of V_{th}, S is the subthreshold swing factor, I_{leak} is the total leakage current, C_g is the gate capacitance and υ is the electron velocity near the source region.

The static power consumption component is represented by the third section of Equation (1.1) and is dominated by leakage current. The second part of Equation (1.1) is due to the momentary pass of current that is created as a result of necessary time for one transistor to switch off in an inverter circuit. The first part of Equation (1.1) is the active power which is drawn from the power supply when the transistor is operating at a clock frequency of f. From Equation (1.1) it can be derived than in in order to realize low-power MOSFETs, lower V_{dd}, higher V_{th}, smaller S (higher immunity to short-channel effects), and lower I_{leak} are necessary. However, according to Equation (1.2) lowering V_{dd} and increasing V_{th} leads to drastic reduction in I_{ON}. Furthermore, even with the application of high-k material at the gate oxide, the thickness of the gate oxide (T_{ox}), should be large enough to reduce the gate leakage current which conflicts with the need for increasing I_{ON}. As a consequence, satisfying a high performance and low power consumption device with good device characteristics based on only traditional scaling methods is becoming increasingly difficult and might become impossible at 20 nm node gate length. Figure 1.7 shows the device performance degradation per power density at

ultra-scaled MOSFET gate length [1.9].

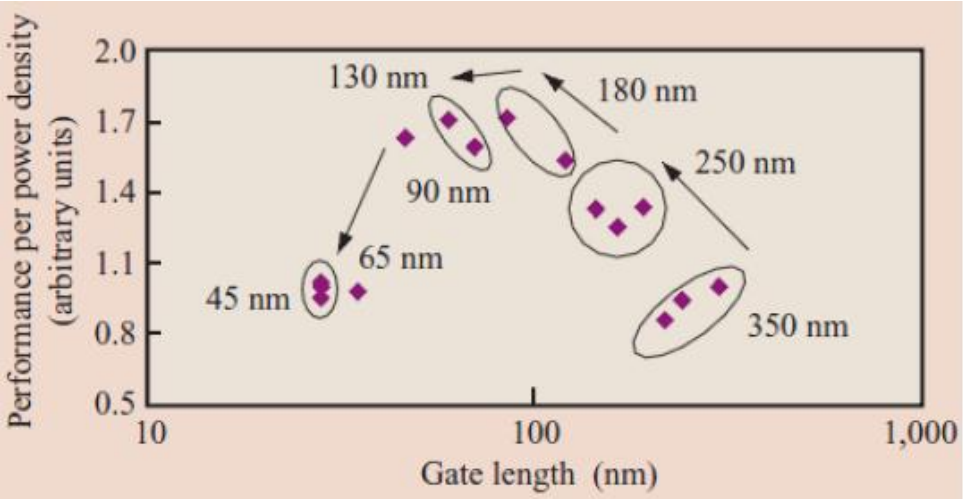

Figure 1.7 Relation between device power density and device gate length [1.9].

1.3 New Material for Enhanced Carrier Transport

In order to make both requirements of low power consumption and high performance compatible, new device technologies are introduced. These technologies, which are stated in the International Technology Roadmap for Semiconductors (ITRS) [1.10], include high-*k*/metal-gate technologies, high-carrier-mobility/high-carrier-velocity channels, ultrathin-body (UTB) structures, multi-gate structures, and metal source/drain.

Among these technologies, new channel material with high carrier mobility are considered to be very important since their superior carrier properties, if utilized fully,

would directly result in achieving higher I_{ON}, or reduce V_{dd} under a constant value of I_{ON}. This means that the active or standby power could be reduced. The enhancement effect of implementing new material with higher carrier mobility on drain current and gate voltage characteristics of a MOSFET is shown in Figure 1.8 [1.11].

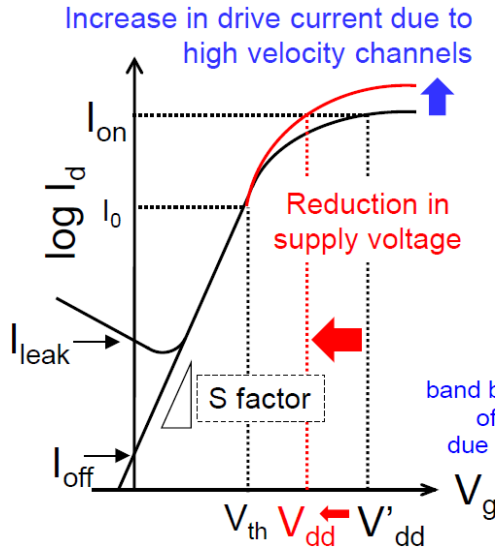

Figure 1.8 Effect of carrier mobility on MOSFET transfer characteristics [1.11].

The drive current of a MOSFET can be described by the following equation [1.12]:

$$I_{ON} \approx qN_s^{source}.v_s \quad (1.3)$$

Where N_s^{source} is the surface carrier concentration near the source edge, v_s is the carrier velocity near the source edge and q is the elemental charge.

Carrier concentration can be modulated by the applied electric field to the channel which is done through gate voltage (V_g) and oxide capacitance (C_{ox}). On the other hand υ_s is determined by intrinsic (material) as well as extrinsic (device parameters) mechanisms. At ultra-scaled devices where the channel length is close to 20 nm, the transport mechanism of carriers becomes quasi-ballistic. This transport mechanism first proposed by Lundstrom is represented by[1.13]

$$I_{ON} = qN_s^{source}.\upsilon_{inj}\frac{1-\gamma}{1+\gamma} \quad (1.4)$$

where υ_{inj} is the injection velocity at the top of the barrier near the source edge, and γ is the backscattering rate near the source region. Figure 1.9 shows the quasi-ballistic concept in a MOSFET band structure.

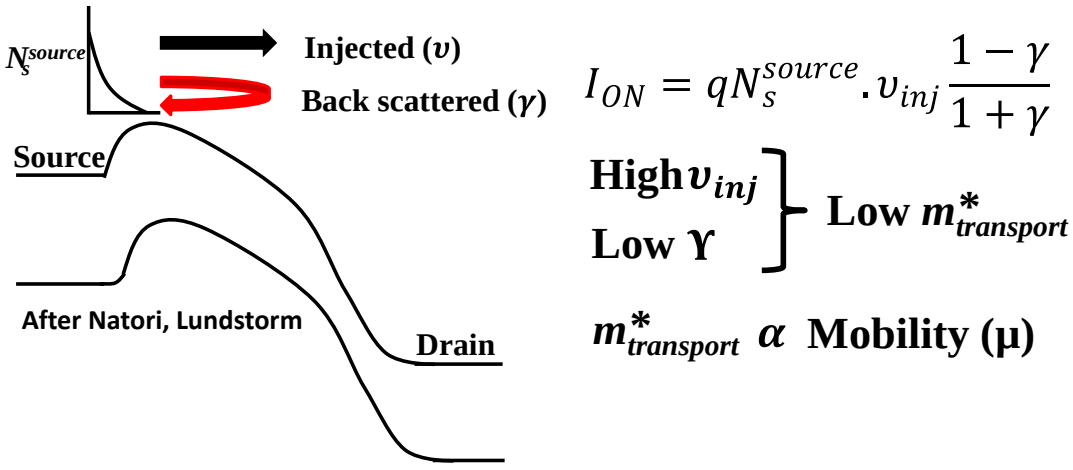

Figure 1.9 Schematic of quasi-ballistic carrier transport mechanism

If the channel length is further reduced to 10 nm, all scattering events in the channel become negligible and Equation (1.4) becomes [1.14]

$$I_{ON} = qN_s^{source}.\upsilon_{inj} \quad (1.5)$$

which is called the fully ballistic transport. Thus, the enhancement of υ_{inj} is necessary to increase I_{ON} in ultra-scaled MOSFETs with ballistic transport as the main carrier transport mechanism. υ_{inj} is an intrinsic material property which can be represented by the following equation [1.14]

$$\upsilon_{inj} = \frac{4}{3\pi}\sqrt{\frac{4N_s}{m_x D_{2D}}} \quad (1.6)$$

Here m_x is the effective mass parallel to the current flow direction and D_{2D} is the density of states (DOS) of the 2-D subband. In both low and high N_s region, υ_{inj} increases with a decrease in m_x and, therefore, reduction in the effective mass along the current-flow direction is the key parameter in increasing υ_{inj} and enhancing I_{ON} under ballistic transport.

1.4 Choice of New Material for MOSFET Channel Region

As it was stated in the previous chapter, enhancing the mobility of semiconductor would lead to higher gains in MOSFET drive current, and enable achieving low power/high performance device. Table 1 summarizes the bulk electron and hole mobility, the electron and hole effective mass, the band gap and the permittivity of Si, Ge, and main III–V semiconductors.

	Si	Ge	InP	GaAs	$In_{0.53}Ga_{0.47}As$	InAs
electron mob. (cm^2/Vs)	1600	3900	5400	9200	10000	40000
electron effective mass ($/m_0$)	m_t:0.19 m_l:0.916	mt:0.082 mt:1.467	0.08	0.067	0.041	0.026
hole mob. (cm^2/Vs)	430	1900	200	400	250	500
hole effective mass ($/m_0$)	m_{HH}:0.49 m_{LH}:0.16	m_{HH}:0.082 m_{LH}:0.044	m_{HH}:0.45 m_{LH}:0.12	m_{HH}:0.45 m_{LH}:0.082	m_{HH}:0.45 m_{LH}:0.052	m_{HH}:0.57 m_{LH}:0.35
band gap (eV)	1.12	0.66	1.34	1.42	0.74	0.36

Table 1. Summary of Si, Ge and compound semiconductors physical properties

The electron mobility of the III–V materials is quite high, and the enhancement factor of the electron mobility against Si can reach up to 3–50 in the bulk. This high mobility is basically attributed to the light effective mass. However, most high mobility materials

also have a significantly smaller band gap compared to Si, leading to a very high band-to-band tunneling (BTBT) leakage currents, which could limit their scalability. BTBT leakage current, which is caused by coupling of valence band and conduction band due to thermal lattice vibration of the semiconductor, can become the dominant off-state leakage current in small band gap semiconductors, thus negating the efforts to reduce the static power dissipation of the device.

InGaAs is a very promising candidate for future nFETs, because it allows for a very good tradeoff between the excellent transport properties of InAs and the low leakage of GaAs. Figure 1.10 shows the simulation results relationships between delay and $I_{OFF,BTBT}$ for thin body nMOSFETs for different materials at a fixed subthreshold leakage current of 0.1μA/μm. The supply voltage is varied from 0.3V to 0.7V and the oxide thickness is set to be T_{ox}= 0.7 nm. The best material should show small delay and low $I_{OFF,BTBT}$ at the same time. Overall, among all the unstrained III-V materials InGaAs and InP exhibit the best performance- high I_{ON}, low delay and low $I_{OFF,BTBT}$ compared to Si [1.15].

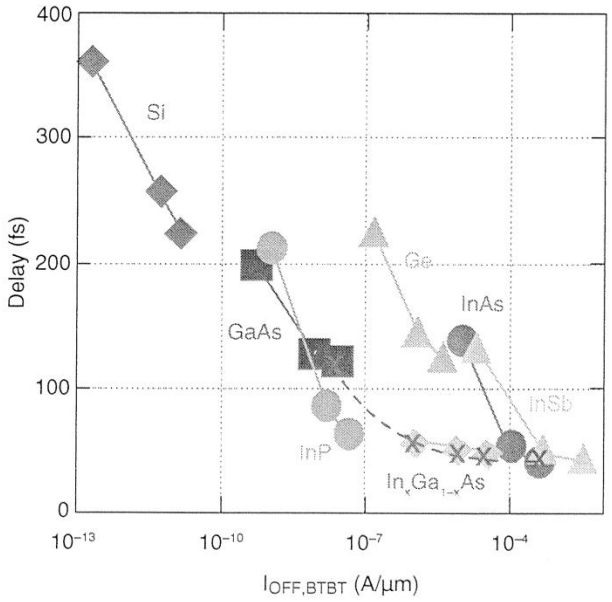

Figure 1.10 Intrinsic delay *vs* $I_{OFF,BTBT}$ trade-off in various materials [1.15].

A comparison between the projected performances of emerging device structures at 11nm technology node are shown in Figures 1.11 and 1.12. According to the results of both experimental data and simulations, emerging devices such as $In_{0.7}Ga_{0.3}As$ MOSFETs and TFETs both provide better energy-delay tradeoff for certain delay target ranges [1.16]. Resolving other manufacturing obstacles (discussed in next chapter) for InGaAs-based devices, could enable a new generation of low-powered high performances devices that surpass those of their Si counterparts.

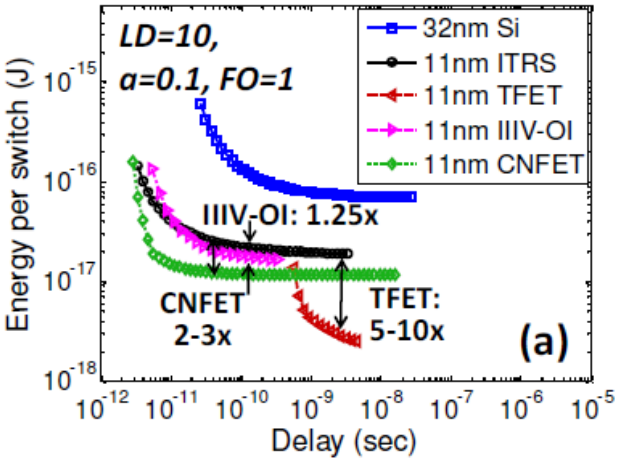

Figure 1.11 Projected minimum E_{tot} *vs* delay for various MOSFET technologies [1.16].

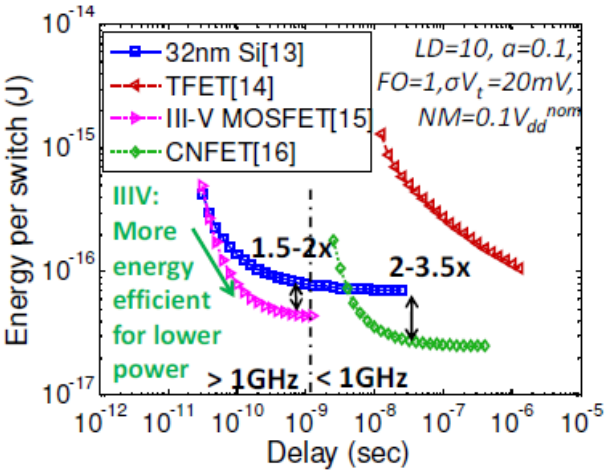

Figure 1.12 Minimum E_{tot} *vs* delay for best available experimental results [1.16].

1.5 Conclusions

Utilizing high mobility III-V channel material could provide a viable solution for the insatiable demand for low-power/high-performance devices, especially in sub-20nm regime where projected limitations of devices on Si-platform is of major concern. Ternary III-V materials, such as $In_xGa_{1-x}As$ are recognized as attractive candidates for high performance, low power devices thanks to their superior carrier transport properties.

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Chapter 2

Current Status and Issues of III-V MOS Devices

Chapter 2 Current Status and Issues of III-V MOS Devices

2.1 Introduction

From the III-V compound semiconductor family, GaAs has the longest history and GaAs metal-oxide-semiconductor field-effect transistors MOSFETs have been a subject of study for several decades. However, unlike Si, III-V semiconductors are not blessed with a stable native oxide like SiO_2 and numerous efforts to realize high quality interface with deposited oxides were failed to produce gate stacks with acceptable gate controllability. Thus, the main obstacle to realizing a GaAs MOSFET technology with commercial value was the lack of high-quality, thermodynamically stable gate dielectric insulators on GaAs that could match device criteria similar to SiO_2 on Si. In recent years the research for alternative material [2.1], which has inherently better transport properties than Si, has sparked a renewed interest in III-V compound semiconductors. These alternative channel materials are sought for application in CMOS technology beyond the 22 nm node and even to replace traditional Si or strained Si. In chapter 1, it was stated that high-*k* material had to be introduced to the gate stack in order to alleviate the gate leakage crisis. Ironically, this step has been a very fortunate one for III-V

family since the introduction of high-*k* dielectrics effectively ended the rule of native oxides (oxides which consist from substrate elements) in device technology. In this chapter a brief overview on the history of III-V MOSFET research is provided. The complications and common issues of high-*k*/InGaAs interface that face the researchers are discussed and finally the purpose of this study is introduced.

2.2 History and Current Status

The advantage of GaAs MOSFET over its Si counterpart has long been recognized because the electron mobility (transport efficiency) in GaAs is five or more times higher than that in Si. The first GaAs MOSFET work was reported by H. Becke et al. by the Radio Corporation of America in 1965 [2.37]. Although deposited SiO_2 is used as the gate dielectric with a large amount of interface traps, the devices were successfully operated in the several-hundred megahertz frequency range showing the feasibility of this approach. It was quickly realized that SiO_2 is not the right gate dielectric for GaAs, which encouraged an enormous research effort in the following decades with a search for a low-defect, thermal-dynamically stable gate dielectric for GaAs. The efforts can be divided into two sceneries: deposited oxide and native oxide. A variety of dielectrics

and techniques have been investigated.

The well-studied dielectrics on GaAs include pyrolytically deposited silicon dioxide [2.1], silicon nitride [2.2], silicon oxynitride [2.3], and aluminum oxide [2.4]. All these processes require relatively high temperatures ranging from 350 to 600 °C. The chemical reaction between GaAs and oxygen in gas ambient is expected to form Ga oxide, As oxide, and even a large number of vacancies due to the high volatility of As. As a result, it became apparent that a low-temperature process is believed to be essential for obtaining a high-quality interface [2.5]. Plasma-enhanced deposition with the process temperature lower than 200 °C was attempted [2.6], though it could potentially induce more defects or fixed charges on the GaAs surface or interface due to the induction of plasma.

In addition to conventional physical vapor deposition and chemical vapor deposition (CVD), Molecular Beam Epitaxy (MBE) approach was also used to form insulating films on GaAs after it began to be widely used to grow III–V compound semiconductor heterostructures at the end of 1970s. For example, high-resistive AlGaAs [2.7] or low-temperature-grown GaAs [2.8] were used as an insulating layer for the GaAs channel. However, relatively high gate leakage current limits the wide application of these approaches. To improve the barrier heights at the heterojunction interface, thermal

oxidation of AlAs epilayers grown on GaAs using MBE were also investigated. [2.8] The difficulty of this approach is to control the oxidation process to terminate at the AlAs–GaAs interface, though the large difference exhibits in the rate of oxide formation of AlAs and GaAs. The research in this direction is still currently active. [2.9]

Motivated by the success of thermally oxidized SiO_2 on Si, using native oxides on GaAs as gate dielectrics was also intensively studied at the very beginning. Some representative approaches include thermal oxidation [2.10], wet-chemical anodization [2.11, 2.12], dc and RF plasma oxidation [2.13], laser-assisted oxidation [2.14], vacuum ultraviolet photochemical oxidation [2.15], and photo-wash oxidation [2.16]. However it turned out that none was optimistic as a feasible approach leading to a commercial GaAs MOSFET technology. One general observation is that the native oxide is not stable, mostly leaky with low dielectric breakdown strength, and cannot be biased beyond a few volts. All these studies are essential to enrich the understanding of chemistry and physics properties of III–V interfaces.

Although some controversies exist within much experimental data, there is consensus that a significant amount of As_2O_3, As_2O_5, and elemental As in native oxides pin the Fermi level of GaAs and are not favorable for an ideal gate dielectric.

Spicer’s extensive experiments which were published in 1980, concluded that the

Schottky-barrier formation on III–V semiconductorsis due to defects formed near the interface by deposition of the metal or any chemisorption of oxygen [2.17]. This model also applies to the formation of states at III–V oxide interface states. Fermi-level position in GaAs is pinned at the mid-gap whether or not it is a metal/semiconductor or oxide/semiconductor interface.

Fermi-level pinning in III–V semiconductors dampened the enthusiasm among III–V researchers to compete with Si in large-scale integrated circuits. However, significant progress was made on high-performance microwave GaAs metal-semiconductor field-effect transistors, pioneered by Hooper and Lehrer [2.18] using a GaAs Schottky barrier directly.

The development of MBE and metal-organic CVD technologies in the 1970s made heterojunctions, quantum wells, and superlattices practical. GaAs HEMT eventually became a commercialized technology, finding broad applications in the communication, and aerospace industries today. GaAs MOSFET research did not continue on a large scale after the successful introduction of GaAs HEMT.

The search for suitable dielectrics or passivation layers on GaAs continues. In 1987, researchers at Bell Labs discovered that a class of sulfides (e.g., Li_2S, $(NH_4)_2S$, $Na_2S{\cdot}9H_2O$) was able to passivate the GaAs surface and provide excellent electronic

properties to GaAs surfaces [2.19- 2.20]. The work generated new interest in GaAs MOSFETs using sulfur passivation before dielectric deposition. Hundreds of papers were published related to GaAs sulfur passivation. However, sulfur passivation did not become a technology because sulfur is an unstable material with very low thermal budget. Nevertheless, it is still very scientifically interesting. Sulfur, as a group VI element next to oxygen, has the same electron number in its outer shell as oxygen, but is less chemically reactive. A few monolayers of sulfur can passivate the GaAs surface in certain conditions and prevent GaAs from oxidation to form As oxides. Sulfur passivation is still used in today's research. Other work on effective passivation of GaAs using hydrogen or nitrogen plasma was also reported by the IBM group [2.21]. Another interesting approach uses a very thin amorphous or crystalline Si layer as an interfacial control layer (ICL) between GaAs and SiO_2 or Si_3N_4 [2.22- 2.23- 2.24]. This approach was intensively studied in the 1990s and was recently adopted to integrate with high-*k* HfO_2 gate dielectrics on GaAs.

In 1995, M. Passlack and M. Hong at Bell Labs reported that *in-situ* deposition of $Ga_2O_3(Gd_2O_3)$ dielectric film on a GaAs surface by electron-beam evaporation from single-crystal $Ga_5Gd_3O_{12}$ produced MOS structures on GaAs with a low interface trap density (D_{it}) [2.25]. UHV scanning tunneling microscopy reveals that the unpinning of

the GaAs Fermi level results from Ga_2O restoring the surface As and Ga atoms to near bulk charge [2.26].

The strong investment in research on deposited high-*k* dielectrics for Si CMOS technologies began in the late 1990s. High-*k* research has since flourished, in particular, the use of ALD method for fabricating Si-based high-*k* MOS devices. At the end of 2001, P. D. Ye and E. Wilk at Bell Labs/Agere Systems started to work on ALD high-*k* Al_2O_3 and HfO_2 on GaAs and other III–V materials. A series of *D*-mode MOSFETs on GaAs, InGaAs, and GaN using ALD Al_2O_3 as gate dielectrics was demonstrated [2.27]. ALD is an *ex situ*, robust, and manufacturable process that attracts wider interest in academia and industry. High-performance inversion-mode III–V MOSFETs were demonstrated with unprecedented drain current as high as 1.05 A/mm and transcondcutance as high as 0.35 S/mm [2.28- 2.29- 2.30]. This was the first surface-channel device in III–V with drain current beyond 500 mA/mm. In-rich InGaAs is identified as the potential channel material for the future 22 nm technology node or beyond with higher effective mobility and manageable band gap for low drain voltage.

2.3 Issues of high-*k*/InGaAs Interface

Recently, there have been reports on experimental demonstration of non-planar InGaAs MOSFETs, which show much enhanced electron injection velocities and high drive current at smaller supply voltage [2.31]. However, various challenges remain to enable commercialization of high mobility channel MOSFETs. One of the key challenges is demonstration of a high quality high-*k*/InGaAs (III-V in general) interface. The high-*k*/InGaAs gate stack also needs to be scalable since for sub-16 nm nodes, highly scaled gate length devices would require very low EOT to maintain electrostatic control of the channel. This requires elimination of low-*k* layer (native oxides) at the interface of III-V and gate dielectric. It is reported that an all *in-situ* process with InGaAs growth followed by high-*k* deposition can suppress the formation of native oxides [2.32], however from the manufacturing point of view, an ex-situ process flow is more desirable.

The ability of MOSFET to switch on and off is described by sub-threshold slope (SS). The value of SS is dependent not only on the accumulation capacitance, but also on the capacitance due to interface state density (D_{it}). In order to improve the switching capability (reduce passive power dissipation), it is imperative to reduce the effect of

parasitic capacitance by reducing D_{it} at high-*k*/InGaAs interface.

Numerous high-*k* dielectrics have been investigated on InGaAs substrate with various In (Indium) contents. Dielectrics such as HfO_2, ZrO_2, TaSiOx, $SrTa_2O_6$ and Al_2O_3 have been tried and electrically characterized. Dielectrics such as HfO_2 have higher dielectric constant than Al_2O_3 and are preferable for gate stack for scaling purposes; however generally these dielectrics have high D_{it} values at their interface with InGaAs which make their application in device structures very difficult. A typical Capacitance-Voltage (*CV*) characteristic of $HfO_2/In0_{.53}Ga_{0.47}As$ interface is shown in Figure 2.1.

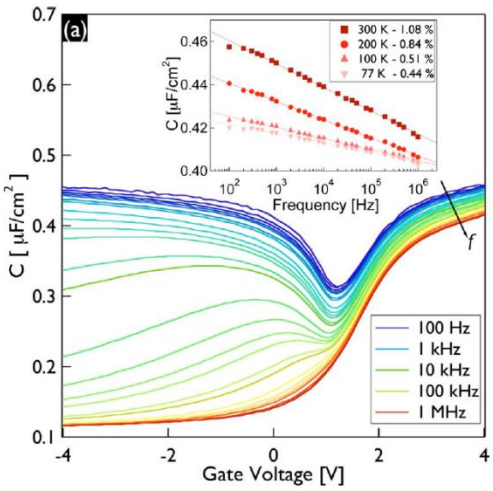


Figure 2.1. *CV* characteristics of HfO_2(35 nm)/InGaAs as a function of frequency measured at 300k [2.33]

Significant frequency dispersion is observed in all ranges of the gate voltage bias. The mechanism of dispersion in each region is different. The effect of high levels of mid-gap D_{it} (~10^{13} eV^{-1} cm^{-2}) can be seen as the capacitance response in lower measurement frequencies in the inversion condition (negative gate bias in this case). Also, the thermal stability of HfO_2 gate stack is usually lower than 500^{o}C. Formation of an interfacial layer $fO_2/In0_{.53}Ga_{0.47}As$ interface is commonly reported even at low annealing temperatures, which degrades the *CV* characteristics of the capacitor (Figure 2.2 [2.34] and 2.3 [2.35]).

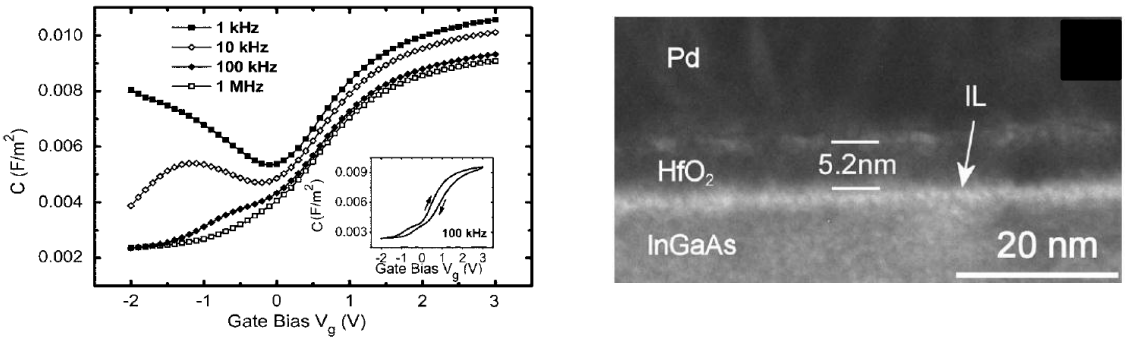


Figure 2.2 *CV* characteristics and TEM image of ALD HfO_2/InGaAs MOS devices with 1.9 nm IL [2.34]

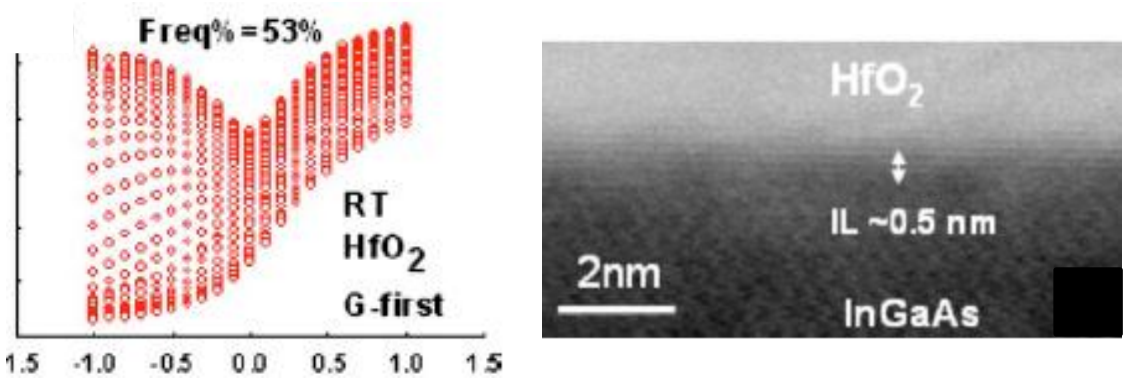


Figure 2.3 *CV* characteristics and TEM image of TaN/HfO_2/InGaAs MOS capacitor at a Gate First process [2.35]

High quality and atomically flat dielectric/InGaAs interfaces have been reported by using Al_2O_3. By using Atomic Layer Deposition (ALD) method for synthesizing Al_2O_3 films on InGaAs, mid-gap D_{it} (~10^{12} eV^{-1} cm^{-2}) has been demonstrated. The improvement in interface is attributed to so called "self-cleaning effect" of trimethylaluminum (TMA) gas which is used as the precursor gas for ALD-Al_2O_3 deposition. This effect refers to removal of As-oxide species by exposing the InGaAs substrate to TMA gas during the first cycle of ALD deposition.

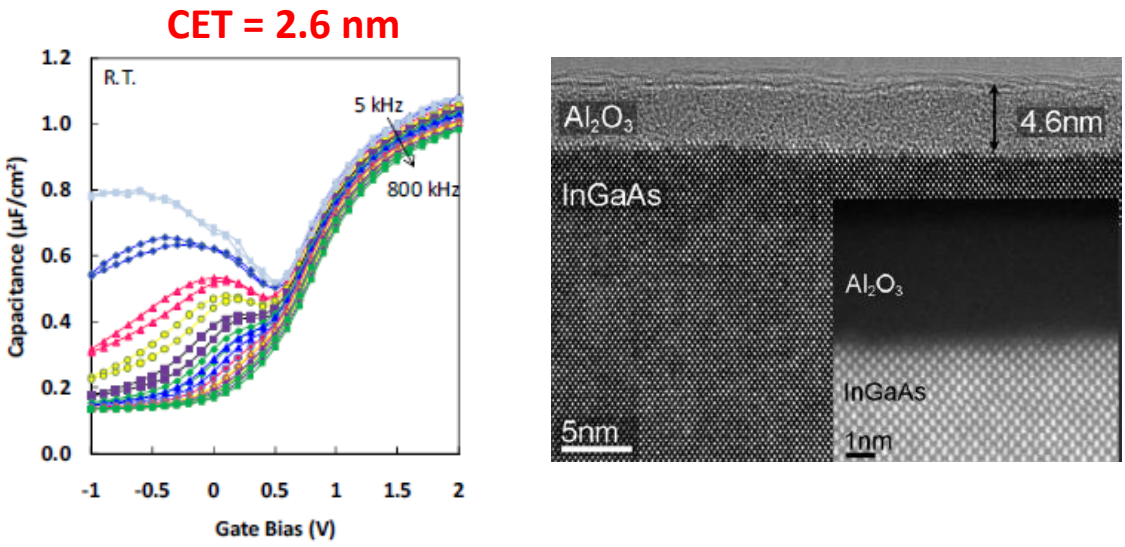


Figure 2.4 *CV* characteristics and TEM image of Pt/ALD-Al_2O_3/InGaAs MOS devices with no IL [2.36]

Although in the recent publications, Al_2O_3 commonly is used as the gate dielectric for InGaAs-based device performance demonstrations, the relatively low dielectric constant of Al_2O_3 (k≈9) and the low thermal budget of Al_2O_3/InGaAs interface (~400 ^oC) will make it inevitable to replace Al_2O_3 with a high-*k* dielectric with better or at least equal level of interface quality.

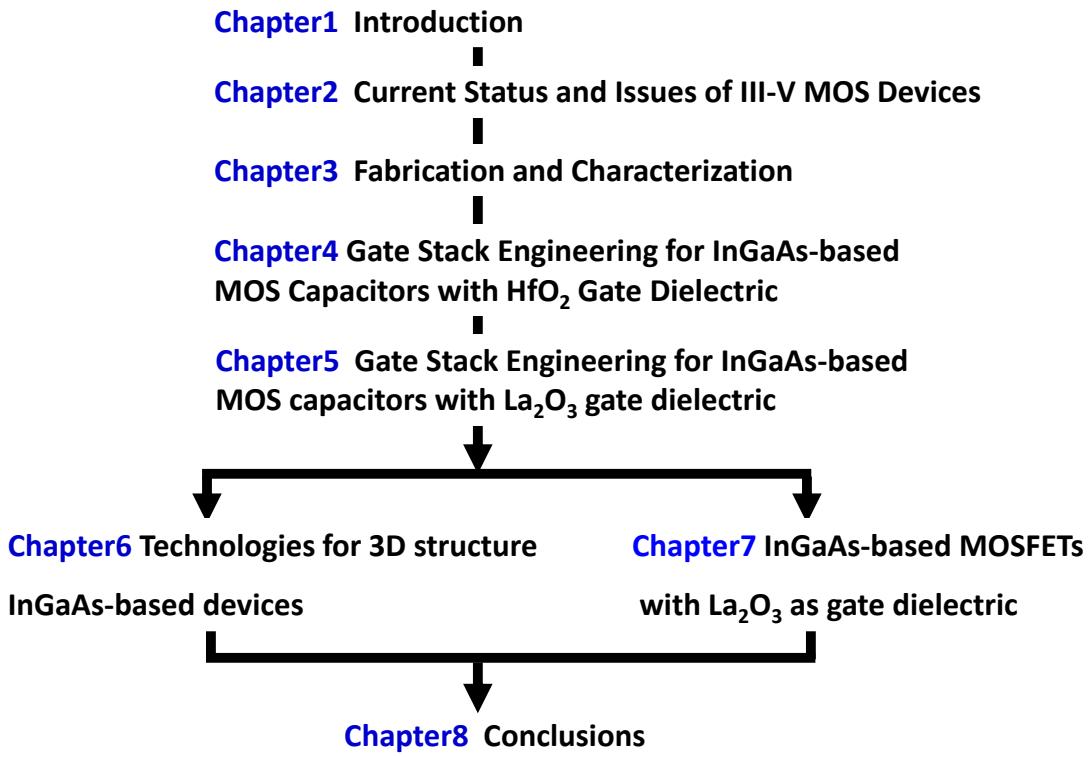
2.4 Purpose and Organization of this Study

This thesis focuses on investigating La_2O_3 as a gate dielectric with great potential for InGaAs-based gate stacks. The majority of work in various research groups has been conducted on application of HfO_2 and Al_2O_3 to InGaAs. The issues regarding both of these materials were described in section 2.3, however in this thesis the fundamental difficulties of HfO_2/InGaAs are evaluated under a new proposal. Therefore, the general purpose of this thesis is to improve the La_2O_3/InGaAs interface properties, by reducing the defects at the interface, reducing the gate stack EOT while improving its thermal stability, and finally evaluating La_2O_3-based InGaAs MOSFET operation.

This thesis consists of eight chapters. Chapter 1 describes the background of MOSFET scaling history and the emergence of new channel material with higher carrier transport properties, such as III-V compound semiconductors and in particular InGaAs. Chapter 2 states the history and current status of III-V based devices and the issues facing the commercial application of such devices with a focus on gate-stack technology as the main determinant for device success. The common experimental scheme used throughout this study, is described in Chapter 3. In Chapter 4, properties of HfO_2/InGaAs interface is investigated and a temperature manipulation method during

HfO_2 deposition is proposed to compensate the formation of defects at the bulk of InGaAs. Chapter 5 focuses on applying La_2O_3 as a gate dielectric to InGaAs substrate and is divided to four sections. The first section describes the difference between the reactivity of La_2O_3 and HfO_2 with InGaAs. Formation of $LaInGaO_x$ layer at La_2O_3/InGaAs interface is proposed and the issues that need to be resolved in order to improve La_2O_3/InGaAs electrical properties are described. The following section purposes a novel passivation method of InGaAs surface, based on self-assembled monolayer formation of Si-containing elements to improve the electrical properties of La_2O_3/InGaAs interface. The third section describes the application of La-silicate structure on InGaAs. Excellent thermal stability of silicate structures was utilized for to manufacture gate stacks with Capacitance Equivalent Thickness (CET) of 0.7 nm which correspond to an EOT< 0.5 nm considering the quantum effects. In the final chapter, the reaction between La_2O_3 and InGaAs was controlled by controlling the amount of oxygen diffusion through the choice of metal gate. Compositional and thickness control of the resultant interfacial layer yielded one of the lowest D_{it} levels in the literature even compared to that of Al_2O_3/InGaAs interface. Chapter 6 deals with requirements for future node 3D structure devices on InGaAs platforms and purposes solutions for two of the critical obstacles (gate stack and source/drain regions). The chapter is divided to two

sections, each section dealing with gate stack and source-drain regions separately. The first section describes synthesizing La_2O_3 film by Atomic Layer Deposition (ALD) method, the second section offers a novel stacked Ni/Si structure for forming highly stable $NiSi_2$/InGaAs without forming any alloy at the interface. In chapter 7, InGaAs MOSFET operation with La_2O_3 as high-k gate dielectric and Ni/InGaAs as metal source and drain, is demonstrated. Finally, in chapter 8, conclusions and prospects for future work are described. Chapter structure in this thesis is summarized in the following chart.



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Chapter 3

Fabrication and Characterization

Chapter 3 Fabrication and Characterization

3.1 Device Fabrication Methodology

The basic device fabrication flow, used throughout this thesis to process MOS devices with high-k gate dielectrics, is illustrated in Figure 3.1. *n*- or *p*- type $In_{0.53}Ga_{0.47}As$ (*100*) substrates epitaxially grown on InP substrate with impurity concentration of 1×10^{16} cm^{-3} or 2×10^{17} cm^{-3}, were used in this study. All substrates were first cleaned by acetone/ethanol. Next, concentrated HF (20%) was used to remove surface oxides. A subsequent surface S-passivation was conducted by dipping the substrates in $(NH_4)_2S$ solution (concentration 7%) at room temperature for 20 min.

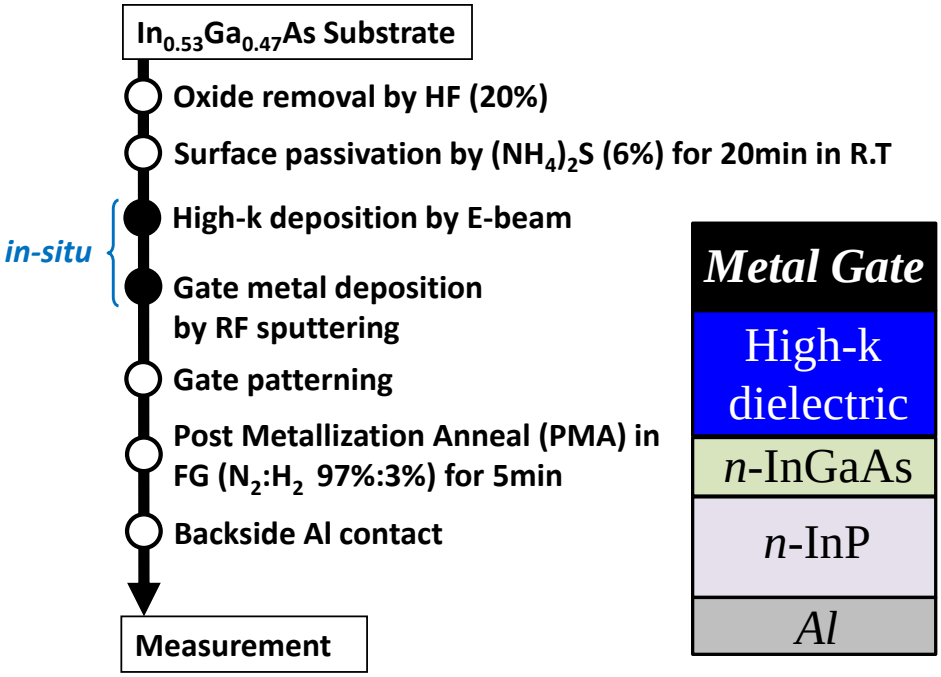


Figure. 3.1 *Fabrication flow for MOS devices*

In order to deposit high-*k* thin films, substrates were loaded into a multi-chamber system equipped with electron-beam (EB) gun, RF sputtering and Chemical Vapor Deposition (CVD) chambers, where samples can be transferred between each chamber in base vacuum pressure of 10^{-7} Pa as shown in Figure 3.2.

The gate electrodes were patterned by lithography and dry-etched by Cl_2/Ar based Reactive Ion Etching (RIE). Post-Metallization annealing (PMA) was performed in a Rapid Thermal Annealing (RTA) chamber in forming gas (FG) (N_2/H_2: 97%:3%) ambient for 5 min. 50-nm Al films were deposited by evaporation to form back side contacts of the samples.

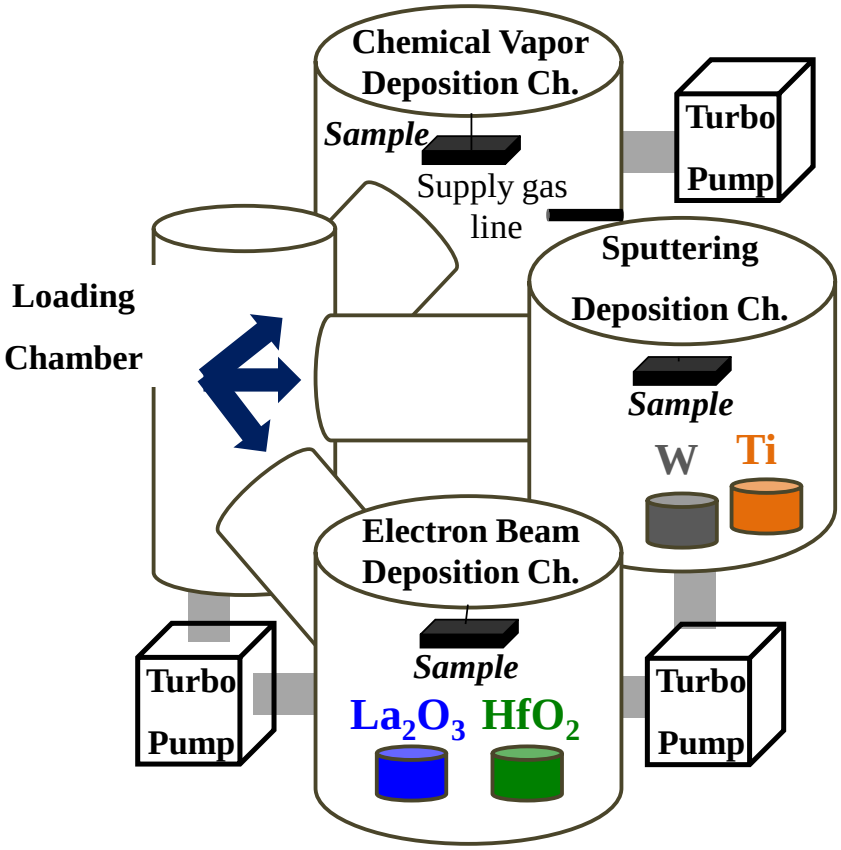


Figure. 3.2 *Schematic illustration of e-beam evaporation, CVD and RF sputtering system.*

3.2 Admittance Characterization of MOS Capacitors

Interface state density (D_{it}) of the high-*k*/InGaAs interface in this study is extracted by measuring the impedance of MOSCAPs as a function of voltage, frequency, and temperature of high-*k*/semiconductor interfaces. Figure 3.3 shows a schematic energy band diagram of an *n*-type MOSCAP in depletion condition.

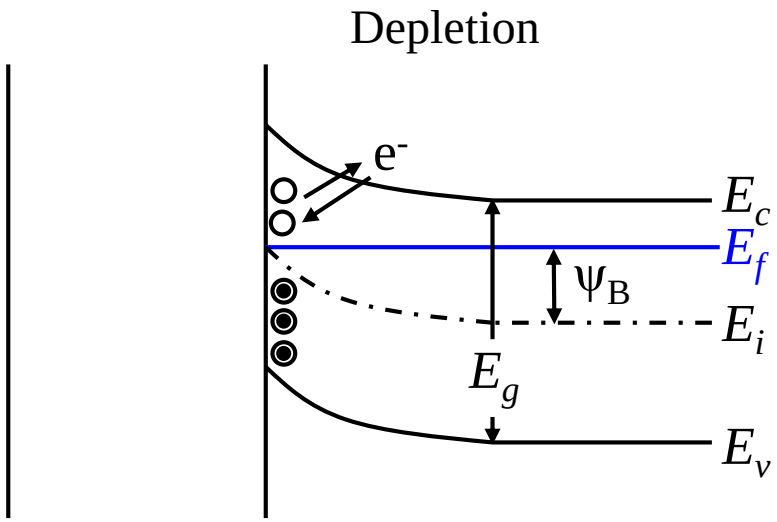


Figure. 3.3 Band diagram of the semiconductor in depletion condition with majority carriers trapping and de-trapping at interface state sites

A dc gate bias, V_g, with an ac signal (amplitude:25 mV and frequency *f*: 1 kHz~ 1 MHz) superimposed to it, is applied to the metal gate. The dc voltage modulates the position of the Fermi level at the interface while the superimposed ac signal causes the Fermi level to oscillate around that energy level. As a result, the traps within the Fermi level proximity are charged and discharged, creating a parasitic capacitance which is related to the interface trap density by $C_{it} = qD_{it}$, where q is the elemental charge. The equivalent circuit model used for extracting the admittance of dielectric/semiconductor interface is shown in Figure 3.4, assuming that the minority carrier contribution in

depletion condition is negligible.

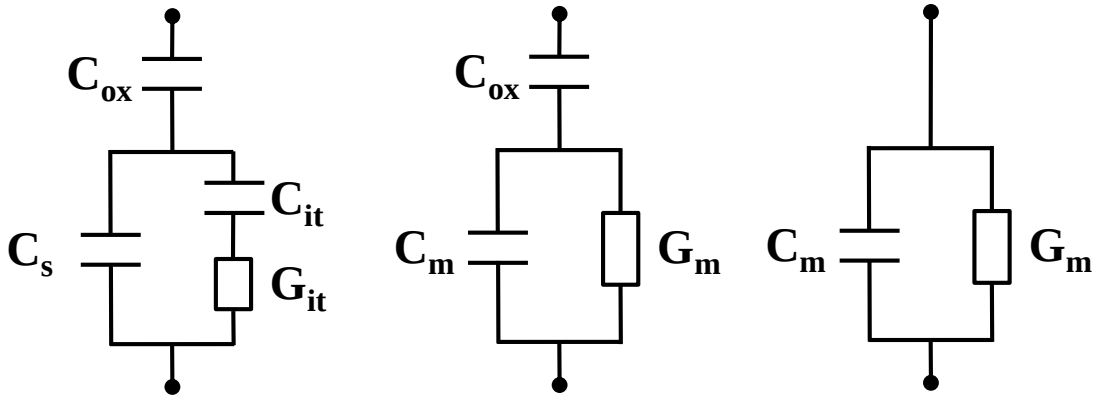


Figure. 3.4 Equivalent circuit diagram of the MOS capacitance used in conductance measurements

The conductance method is based on analyzing the loss that is caused by the change in the trap level charge state (3.1). The equivalent parallel conductance G_p is related to the measured impedance G_m by:

$$G_p = \frac{\omega^2 C_{ox}^2 G_m}{G_m^2 + \omega^2 (C_{ox} - C_m)^2} \quad (3.1)$$

Interface traps in the proximity of Fermi level can change their occupancy. Maximum loss occurs when interface traps are in resonance with the applied ac signal frequency. Assuming that surface potential fluctuations can be neglected, the D_{it} is estimated from the normalized parallel conductance peak, $(G_p/\omega)_{max}$:

$$D_{it} \approx \frac{2.5}{Aq}\left(\frac{G_p}{\omega}\right)_{max} \quad (3.2)$$

where A is the device area. Typically the portion of the band gap that can be probed by conductance measurement is from flatband to weak inversion.

An accurate measurement of C_{ox} is needed in order to use the conductance method for interface trap evaluation. However, in contrast to Si, using the accumulation capacitance to estimate C_{ox} is not possible for n-type channels, because of the low conduction band DOS of III-V semiconductors. In this thesis, C_{ox} is estimated by fitting the experimental results to theoretical ideal *CV* curve.

3.3 Ideal CV Characteristics of oxide/$In_{0.53}Ga_{0.47}As$ Interface

Figure 3.5 shows the schematic band structure of $In_{0.53}Ga_{0.47}As$ at room temperature (T=300k) using the parameters from Ref. 3.2.

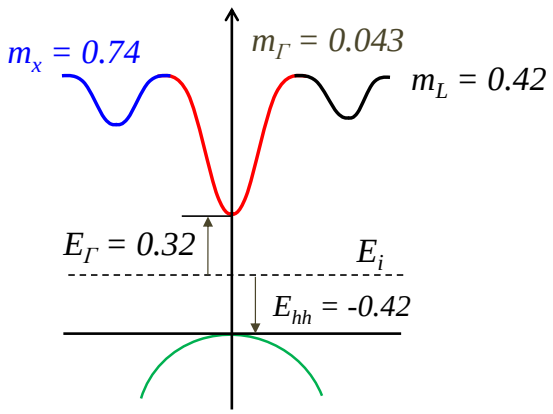


Figure. 3.5 Band structure of $In_{0.53}Ga_{0.47}As$ at room temperature

The small electron effective mass of $In_{0.53}Ga_{0.47}As$ results in small conduction band density of states (DOS) which causes the Fermi level move into conduction band at large electric fields. This means that for calculating electron density, the related equation for degenerate semiconductors must be used. Also the nonparabolicity of the lowest conduction band valley (Γ) should be taken into account to allow for an accurate evaluation of band bending within the semiconductor. The ideal *CV* calculation is driven by solving the Poisson equation:

$$\frac{d^2V(x)}{dx^2} = E(x)\frac{dE(x)}{dV(x)} = -\frac{e[N_d - N_a + p(x) - n(x)]}{\varepsilon_s} \quad (3.3)$$

Where N_d and N_a are the donor and acceptor concentrations in the semiconductor, *n(x)* and *p(x)* are the electron and hole densities and ε_s is the dielectric constant. The electric field *E(x)* inside the semiconductor can be calculated by integrating Equation (3.3) from the bulk of semiconductor to depletion region.

The electron density equation assuming only Γ valley occupations is given by:

$$n[V(x)] = \frac{2\sqrt{\pi}}{kT^{3/2}} N_C \int_{E_C}^{\infty} \frac{(E - E_C)^{1/2}}{1 + e^{[E-V(x)]/kT}} dE \quad (3.4)$$

Where E_c is the conduction band edge energy, N_c is the effective density of states in the semiconductor conduction band and T is the temperature. If the higher lying conduction band valleys (X and L) are also taken into account for ideal *CV* calculations, a small upturn of capacitance in accumulation region at higher gate voltages is observed. This

can be attributed to occupation of these valleys with electrons at high electric fields, however an upturn of capacitance in accumulation condition, in experimental data has never been observed. Therefore, only the occupation of Γ valley is assumed for calculation of the ideal *CV* curve in this thesis.

Total charge Q_s per unit area inside the semiconductor can be obtained by Applying Gauss's law and integrating Equation (3.4),

$$Q_s(\Phi_s) = -2\text{Sign}(\Phi_s) \times \sqrt{\int_{\psi_B}^{\Phi_s} -e\varepsilon_s\{N_d - N_a + p[V(x)] - n[V(x)]\}dV(x)} \quad (3.5)$$

The ideal capacitance therefore can be expressed by:

$$C_s(\Phi_s) = -\frac{dQ_s(\Phi_s)}{d\Phi_s} \quad (3.6)$$

The gate voltage causing the band bending ψ_s, is calculated from

$$V_g = \Phi_s + \Delta\phi_{ms} - \frac{Q_s(\Phi_s)}{C_{ox}} \quad (3.7)$$

An example of the calculated ideal *CV* for oxide/*n*-$In_{0.53}Ga_{0.47}As$ interface with a doping concentration of 1×10^{16} cm^{-3} and considering the InGaAs band structure, is shown in Figure 3.6. The capacitance equivalent thickness (CET) is taken to be 2 nm, where accumulation capacitance is lower than the oxide capacitance (C_{ox}) for the assumed CET value.

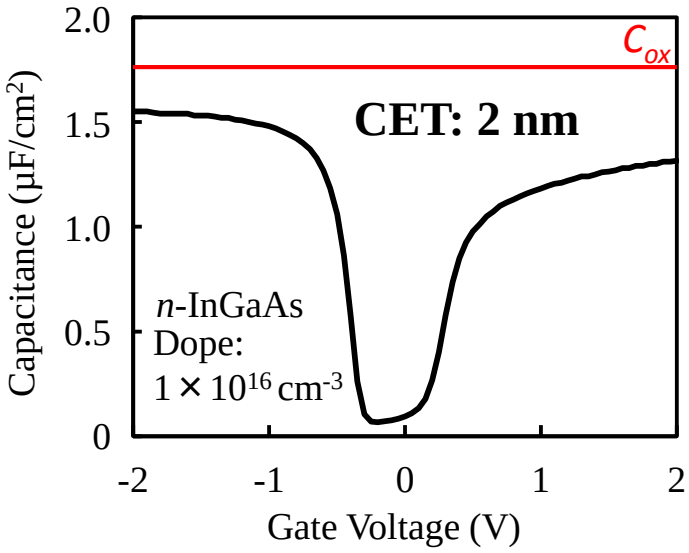


Fig. 3.6 Simulation of ideal *CV* characteristics for InGaAs MOS at room temperature.

3.4 References

[3.1] Y. Taur and T. Ning, Fundamentals of Modern VLSI Devices, Cambridge, 1998

[3.2] http://www.ioffe.ru/SVA/NSM/Semicond/GaInAs/index.html

[3.3] I. Vurgaftman, J. R. Meyer, and L. R. Ram-Mohan, "Band parameters for III–V compound semiconductors and their alloys," *J. Appl. Phys.*, vol. 89, 5815, 2001

Chapter 4

Gate Stack Engineering for InGaAs-based MOS Capacitors with HfO_2 Gate Dielectric

Chapter 4 Gate Stack Engineering for InGaAs-based MOS Capacitors with HfO_2 Gate Dielectric

4.1 Introduction

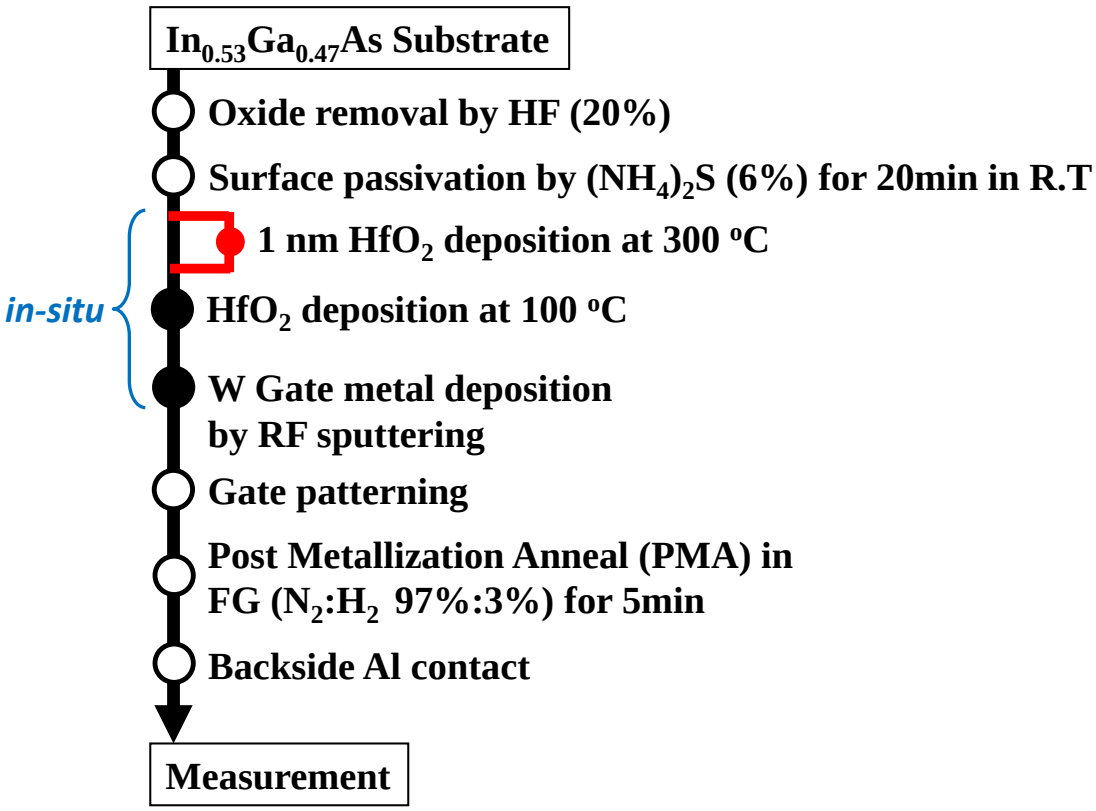
As it was previously described in Chapter 1, Hafnium dioxide (HfO_2) was chosen for SiO_2 replacement to resolve excessive gate leakage problem, caused by aggressive scaling of the gate oxide. Excellent thermal stability of HfO_2 and its band offset values against Si band gap, were some of the main reasons for its selection. However, the HfO_2/InGaAs interface is more complicated and not studied as deeply or as widely as Si. A common theme that is commonly reported in literature for not only HfO_2/InGaAs interface but in general for high-*k*/InGaAs interface, is the non-ideal behavior of capacitance-voltage (C-V) measurements, such as frequency dispersion in accumulation region [4.1, 4.2], irrespective of the surface treatment method and deposited gate oxide. This dispersive behavior is complex and cannot be explained by conventional interface states or parasitic series resistance effects [4.3]. Clarifying the physical origins causing the capacitance dispersion in accumulation condition, could help resolve the source of electrical behavior abnormalities and therefore improve the device performance. In this

chapter, the charge trapping mechanisms of InGaAs-based capacitors with high-*k* gate stack is measured and analyzed by multi-temperature admittance measurements. The results are compared with the non-ideal admittance behaviors observed on Si and Ge with same device fabrication flow. A simple and straightforward model is proposed to identify the dominant defect mechanisms responsible for observed capacitance-voltage or conductance-voltage behavior at various gate bias range. These results provide a guideline for the high-*k*/InGaAs interface requirements, in order to achieve optimum electrical characteristics for MOS capacitors.

4.2 Experimental Procedure

Capacitors were fabricated on (*100*)-$In_{0.53}Ga_{0.47}As$ epitaxially grown on InP substrates (*n*-type). Substrates were degreased by acetone- ethanol followed by a three step pre-deposition cleaning process: native oxide was removed using concentrated HF (20%) and *ex-situ* surface passivation was performed using $(NH_4)_2S$ solution. The samples were then immediately loaded to e-beam chamber and were heated at 450^oC for 30 min in vacuum to remove any residual oxides. HfO_2 layer was deposited in two different conditions by e-beam evaporation. For a control sample (sample A) the

substrate temperature was kept at 100^{o}C during the HfO_2 deposition. For sample B, 1-nm HfO_2 was deposited while the substrate temperature was kept at 300^{o}C, and the rest of the deposition was continued after the substrate temperature was lowered to 100^{o}C. 50 nm W gate electrode was in situ deposited by RF magnetron sputtering and SF_6 ion etching was used to pattern the gates. Post-metallization anneals (PMA) were carried out in forming gas (F.G.) (N_2:H_2= 97:3%) ambient for 5 minutes. Al contact layer on backside of the substrates was deposited by thermal evaporation. Figure 4.1 shows the flow for experimental methodology. Electrical characterization was performed on MOS capacitors using Agilent 4156C semiconductor parameter analyzer for room temperature and Agilent 4284A semiconductor parameter analyzer for low temperature measurements.



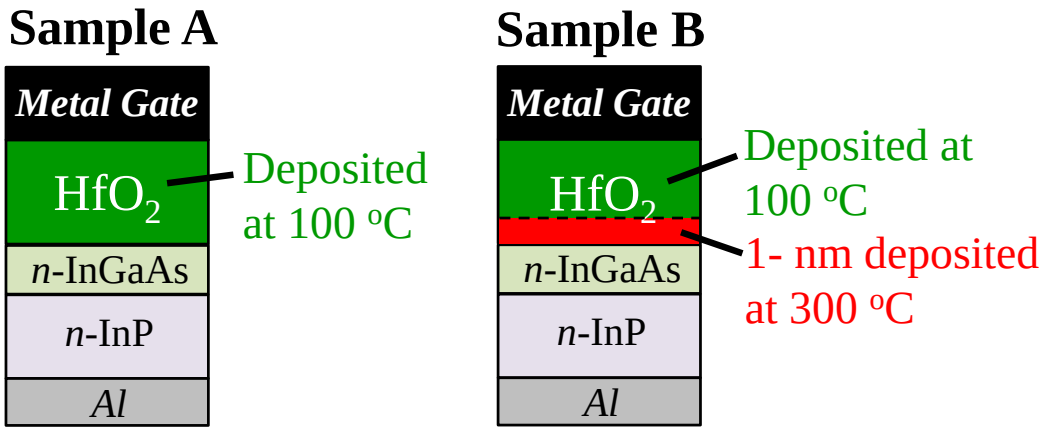


Figure 4.1 Experimental flow for fabrication of Samples A and B

4.3 Impact of Manipulating Substrate Temperate During HfO_2 Deposition

Figures 4.2 and 4.3 show the *CV* characteristics of samples A and B with 14-nm thick HfO_2 gate dielectric respectively. Samples were annealed in FG at 420 ^oC and measured at a frequency range of 1 kHz ~ 1 MHz at room temperature. Qualitative comparison of the *CV* characteristics for the two samples point to an improved interface for sample B. Frequency dispersion in accumulation and depletion condition is reduced for sample B and the capacitance response in negative bias occurs in lower frequencies. Furthermore, the lower upturn capacitance value (highest value of C_{min}) in sample B indicates smaller minority carrier response due to the presence of interface trap states.

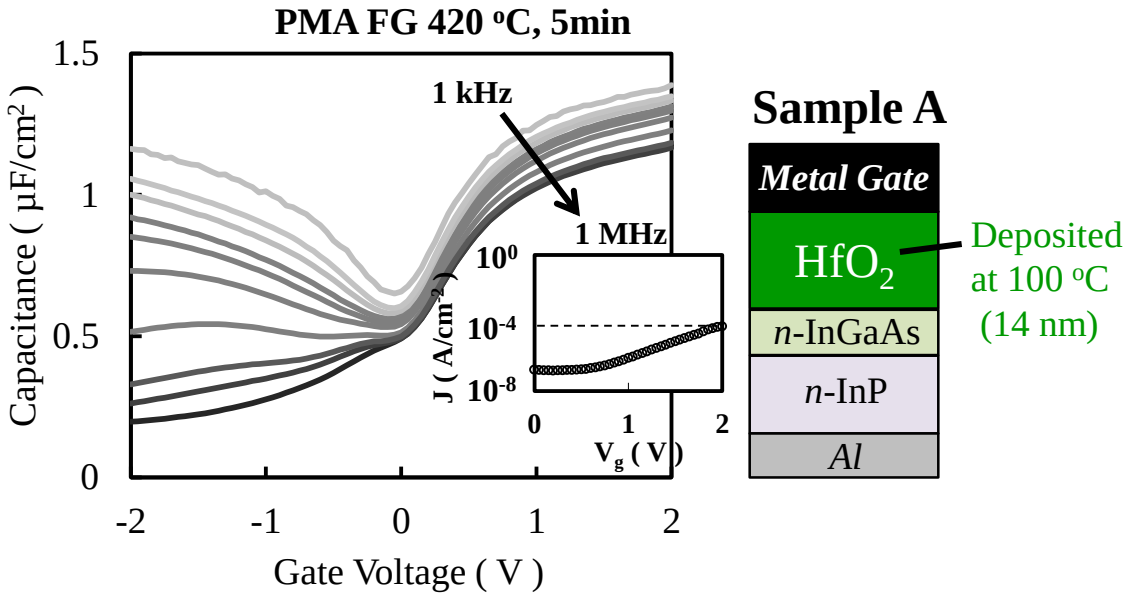


Figure 4.2 *CV* characteristics of sample A (HfO_2 = 14 nm) in room temperature, inset shows the gate leakage characteristics

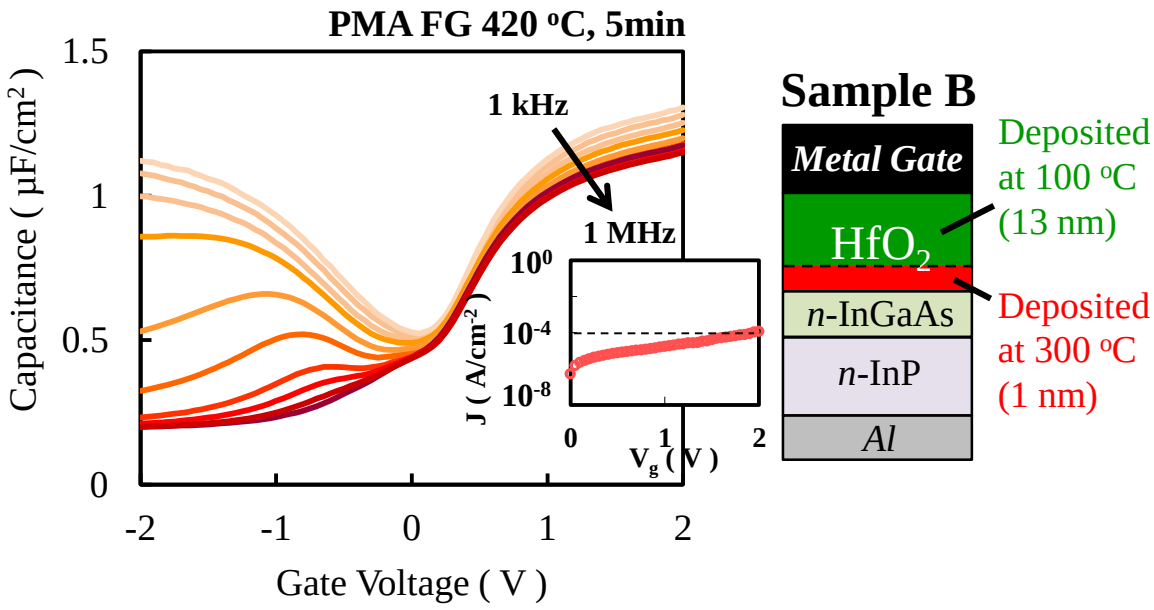


Figure 4.3 *CV* characteristics of sample B (HfO_2 = 14 nm) in room temperature, inset shows the gate leakage characteristics

In order to see the effect of temperature manipulation during gate oxide deposition, on thinner HfO_2 layer during deposition, samples with 7-nm HfO_2 as gate dielectric were fabricated. Figures 4.4 (a) and (b) show the *CV* characteristics of samples A and B with 7-nm thick HfO_2. The measurement results carried out at room temperature and 100 K is included for both samples. Sample B shows improved *CV* behavior, less affected by the leakage current and less dominated by the high interface trapping states. The abrupt increase of accumulation capacitance at lower frequencies for sample I, is due to higher ac leakage current, which generally occurs for currents over 0.1 A/cm^2. Given that both samples have the same dielectric thickness (Figure 6), suggests that the integrity of dielectric for Sample B is better preserved after annealing.

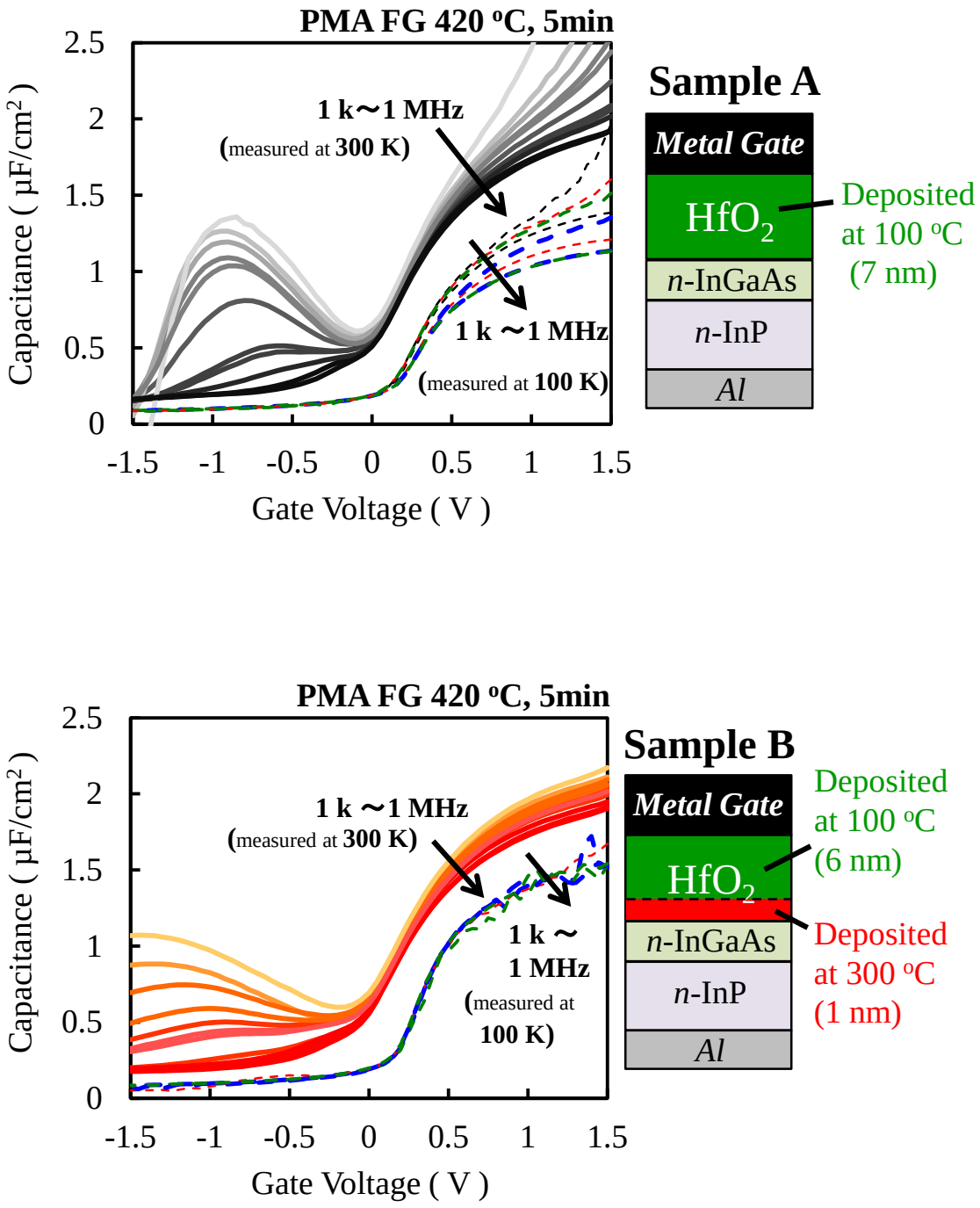


Figure 4.4 *CV* characteristics of (a) sample A (HfO_2 = 7 nm) in room temperature and 100K, and (b) sample B (HfO_2 = 7 nm) in room temperature and 100K

Also it has been reported that the presence of low band gap native oxides at the high-*k*/InGaAs interface would result in an increase in the gate leakage current. This becomes especially more evident when the thickness of high-*k* oxide is reduced [6]. As can be seen from Figures 4.2 and 4.4 (a), the frequency dispersion in sample A (substrate temperature fixed at 100 ^{o}C during HfO_2 deposition) is not affected by changing the HfO_2 thickness, thus oxide border traps or leakage current caused by trapping events in mid-gap interface states, as is proposed elsewhere [4.4], could not be the main reason for the dispersive behavior of the capacitance in accumulation condition. Capacitance response of both samples is completely resolved for the low temperature measurements. This is due to the decrease of minority carriers at lower temperatures and slower characteristic time response of mid-gap interface states [4.5]. The decrease in inversion capacitance would cause the total capacitance to be noticeably lower at 100 K measurement compared to room temperature measurement [4.6].

Interface states of the samples were quantitatively compared by the conductance method [4.7]. Figure 4.5 shows the interface state distribution of the samples, in the upper half of the band gap, after FG anneal at 420 °C. The D_{it} value is smaller for sample B in both majority carrier band edge and mid-gap than that of sample A. The lowest value obtained was 1.6×10^{13} $eV^{-1}cm^{-2}$ for sample B with 7-nm HfO_2.

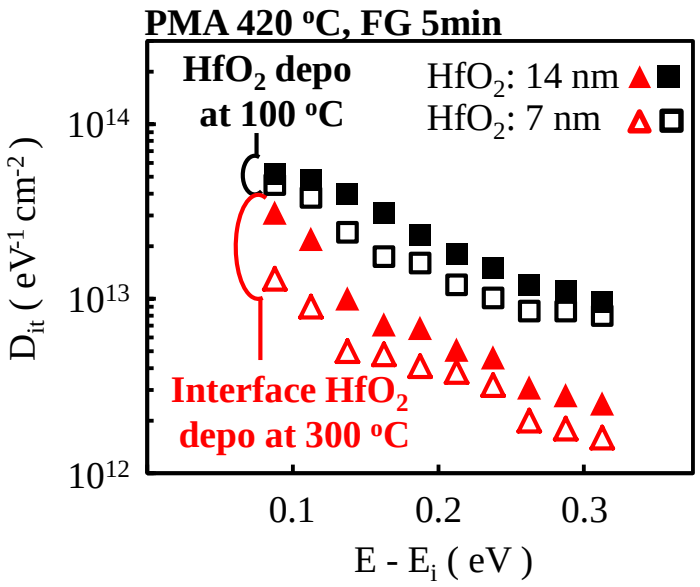


Figure 4.5 Interface state density (D_{it}) distribution of samples A and B with HfO_2:7 and 14 nm

In order to investigate the frequency dispersion behavior seen in both samples with different oxide thicknesses, the capacitance of samples at a frequency range of 1 kHz ~ 1 MHz in accumulation condition (when surface potential ψ_s is 0.1 eV) is shown in Figure 4.6. A stronger dependence of capacitance on measurement frequency is observed for Sample A, especially for device with 14-nm HfO_2 as the gate dielectric. Examining the G_p/ω versus frequency plots for both samples with 7-nm HfO_2, reveals the existence of peaks for a voltage sweep from flat band voltage to accumulation condition (Figure 4.7). A significant number of peaks is observed at higher measurement frequencies are for sample A, indicating existence of fast trapping states

[4.8].

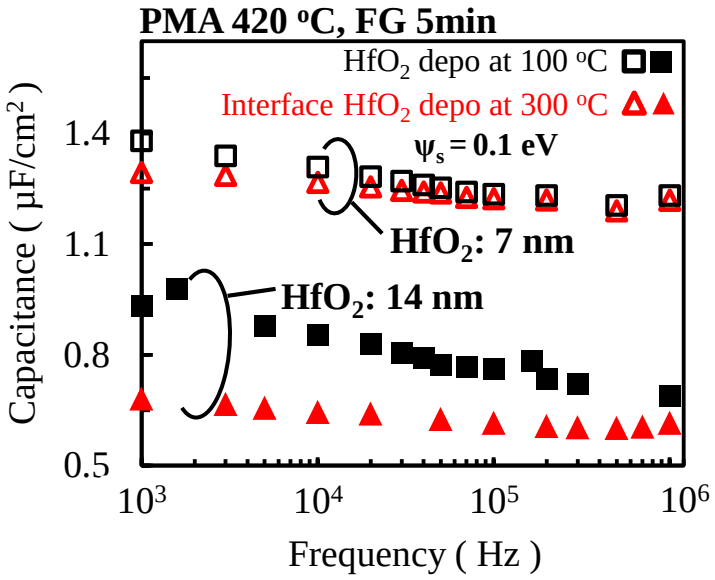


Figure 4.6 Capacitance vs frequency characteristics of samples A and B with HfO_2:7 and 14 nm in accumulation condition

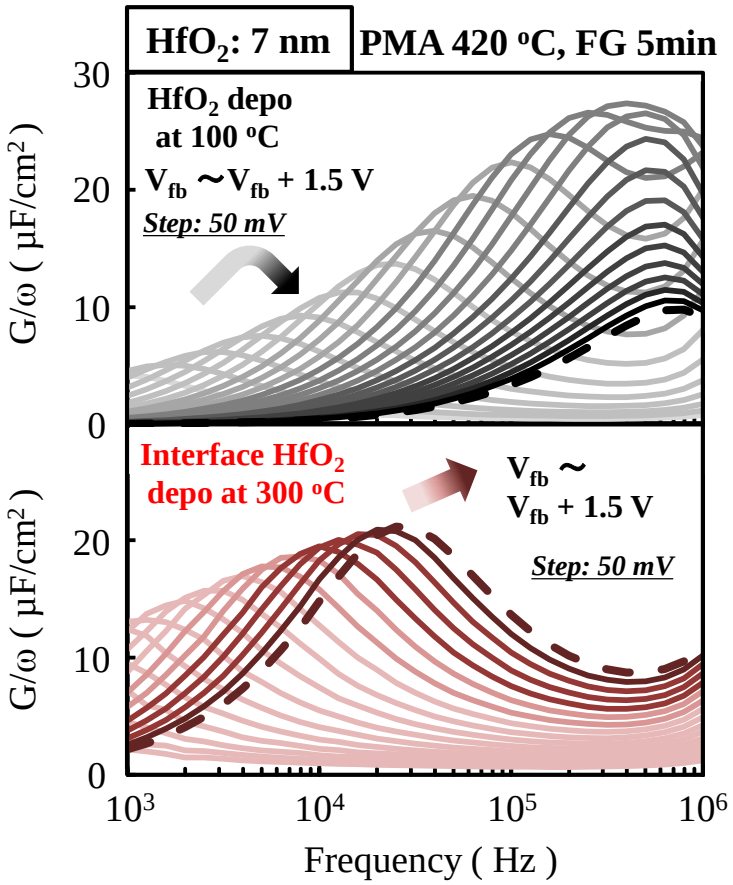


Figure 4.7 Conductance vs frequency characteristics of samples A and B with HfO_2:7 and 14 nm in accumulation condition

4.4 Theoretical Modeling of high-*k*/InGaAs Interface

The models proposed so far, for explaining the frequency dispersion behavior in III-V capacitors, include series resistance, oxide border traps and carrier trapping in mid gap interface states due to leakage current. However, these models are not universally accepted yet since they cannot explain many of the experimental data published in the

literature. Frequency dispersion due to series resistance would account only for a few percent of the total dispersion seen in most InGaAs capacitors, oxide traps should not cause any conductance loss (appearing as conductance peaks in accumulation condition), furthermore frequency dispersion in accumulation is a thermally activated phenomena thus oxide trap activation which is caused by tunneling current should not be responsible for the dispersive behavior since tunneling current does not depend on temperature. A correlation between oxide thickness and frequency dispersion is not always seen to validate leakage current argument.

Here we purpose a model based on the existence of traps within the bulk of the InGaAs substrate, which could explain the dispersive behavior in accumulation in our results and we also purpose a guideline to prevent this problem.

CV characteristics of W/HfO_2/InGaAs MOS capacitor at room temperature on both *n*- and *p*- type substrates are shown in Figure 4.8. It should be noted here that HfO_2 deposition method for these samples is the same as Sample B, described in section 4.2. The gate leakage current of each capacitor is shown in the inset of each graph. Dielectric constant of HfO_2 after annealing at 420 ^oC was estimated to be around $k \approx 19$ using the thickness series method as is shown in Figure 4.9.

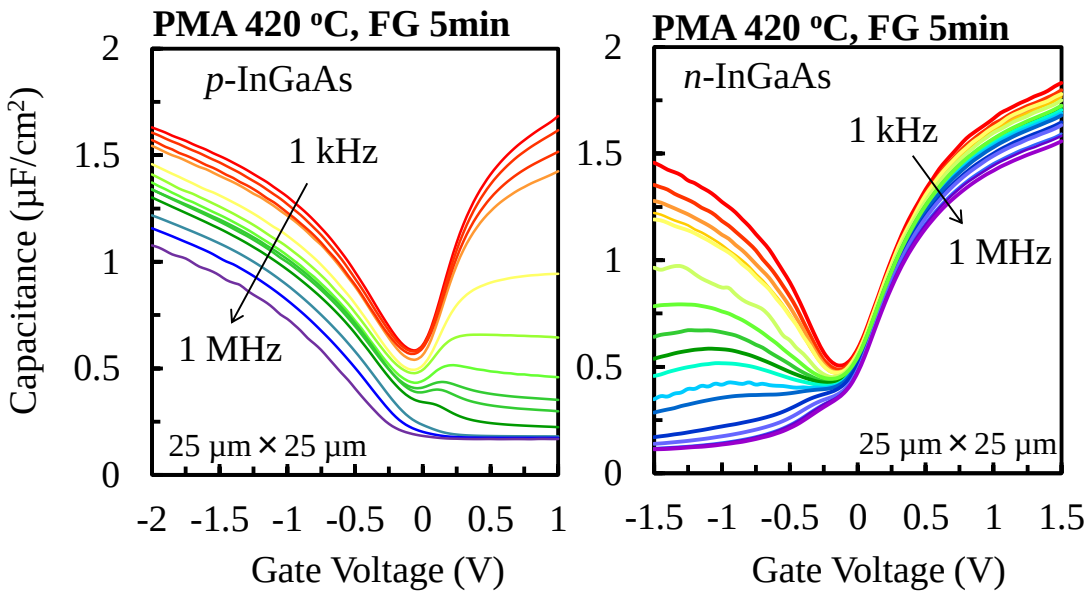


Figure 4.8 *CV* characteristics of W/HfO_2/InGaAs capacitors on *p*- and *n*- type InGaAs

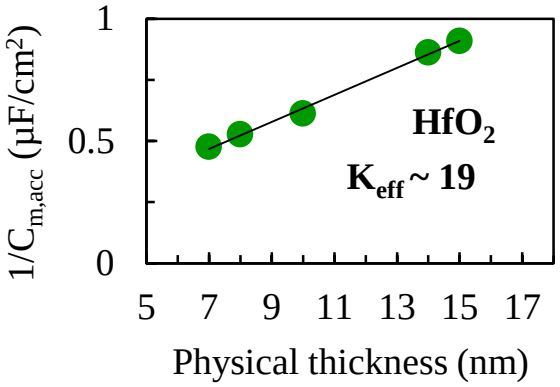


Figure 4.9 Effective *k*-value of HfO_2 obtained from thickness series

Peak D_{it} value estimate by conductance method at 50 kHz for both *n*- and *p*-type, show a higher interface state density for *p*-type substrate (Figure 4.10).

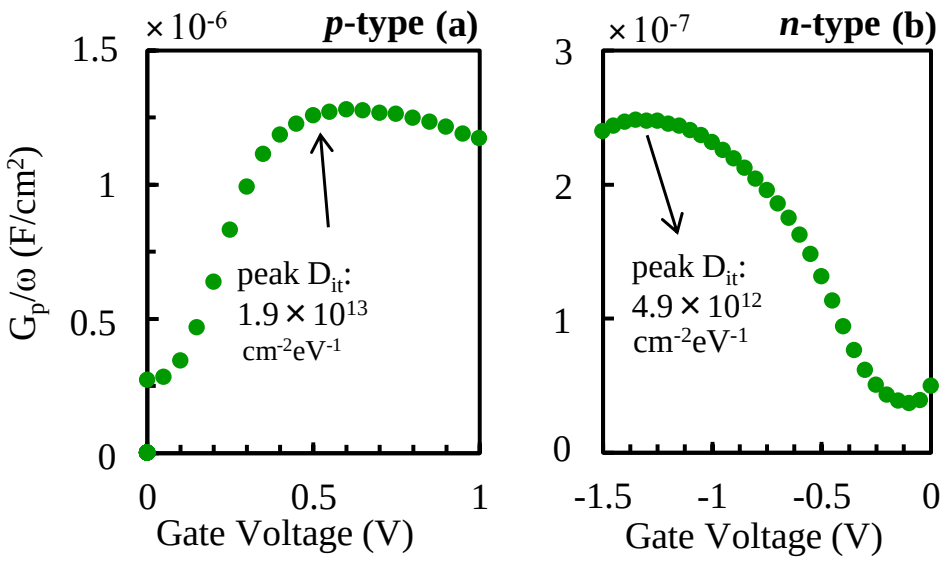


Figure 4.10 Peak conductance value for W/HfO_2/InGaAs capacitors on (a) *p*- and (b) *n*- type InGaAs

Various traps could exist within the gate dielectric in a MOS structure and all of these defects could act as trapping sites for carriers within the semiconductor and disturb the ideal electrical properties, which are expected from a capacitor.

Schematic in Figure 4.11 shows theses defect mechanisms in the gate-stack. The traps from the bulk of the semiconductor are also included. The effect of these traps is categorized by comparing the measurement results on Si and Ge MOS capacitors with InGaAs MOS capacitors.

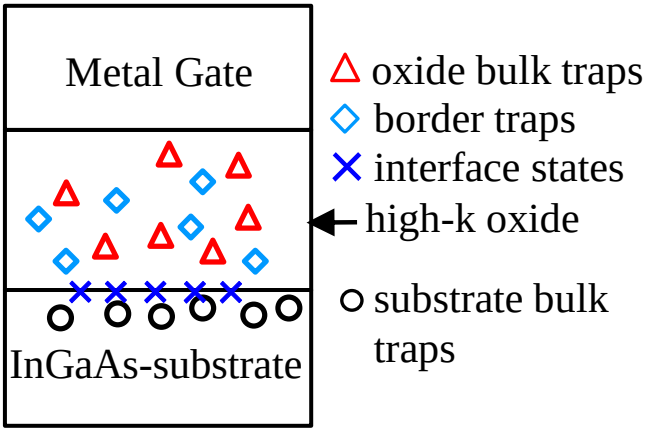


Figure 4.11 Schematic illustration of defect mechanisms in gate stack

CV characteristics of high-*k*/Si interface, is shown in Figure 4.12. The small hump in depletion region, which appears at low measurement frequencies, is observed in numerous papers and is a typical characteristic of high-*k* dielectrics. *CV* curves of a high quality, thermally grown SiO_2/Si interface is also shown in the same figure for comparison.

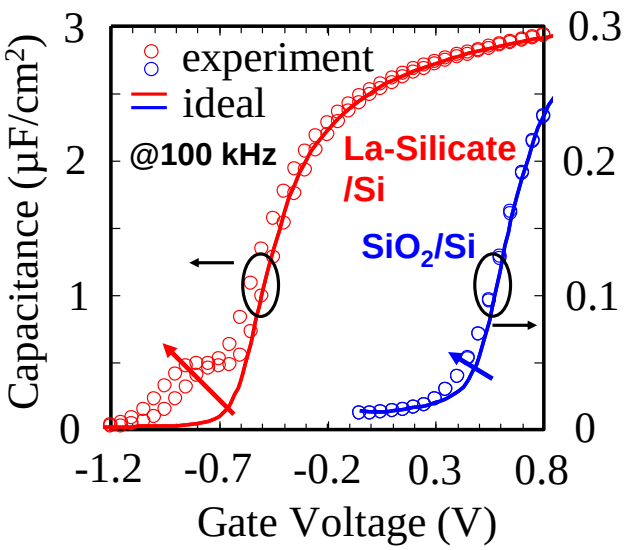


Figure 4.12 *CV* characteristics comparison of La_2O_3/Si and SiO2/Si interfaces

Contrasting the conductance measurement results for both of these devices (with SiO_2 and high-*k* gate dielectric) reveals a conductance peak for the high-*k*/Si interface at lower frequency range, shown if Figure 4.13. These low-frequency conductance peaks share several characteristics; 1- their height (amplitude) remains constant under varying gate bias and 2- their peak occur outside of the response frequency range of Si dangling bonds which is outside the response frequency range of Si dangling bonds [4.9].

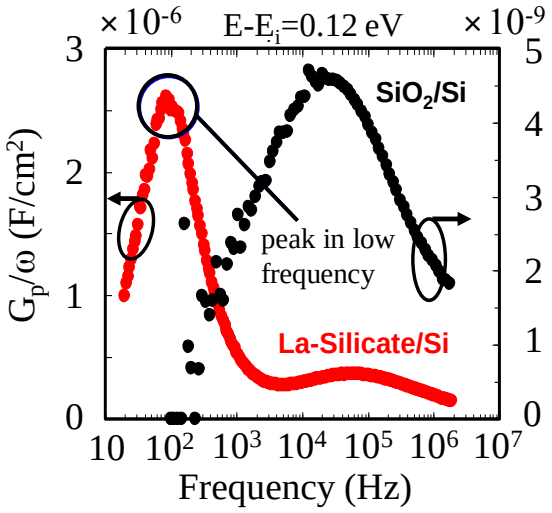


Figure 4.13 Conductance peak comparison of La_2O_3/Si and SiO_2/Si interfaces

It has been shown that oxide traps (bulk and border), which possess long time constants, can exchange charge with majority carriers through tunneling. Thus two trapping mechanisms based on conductance time constants (long and short), can be separated for high-*k*/Si capacitors (Figure 4.14).

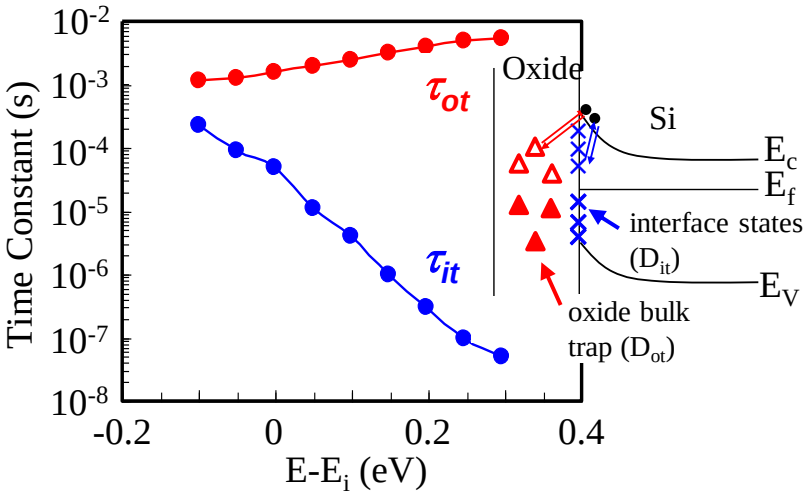


Figure 4.14 Trap time constant comparison of La_2O_3/Si and SiO_2/Si interfaces

The traps that have shorter time constant and depend on their position within the band gap are related to interface states, and the traps with slower time constant and almost constant throughout the band gap are related to the traps within the bulk of the oxide.

Figure 4.15 (a) and (b) shows the conductance over frequency measurements conducted on W/HfO_2/n-InGaAs MOS capacitor at 300K. Two distinctive peak types in depletion and accumulation conditions can be observed.

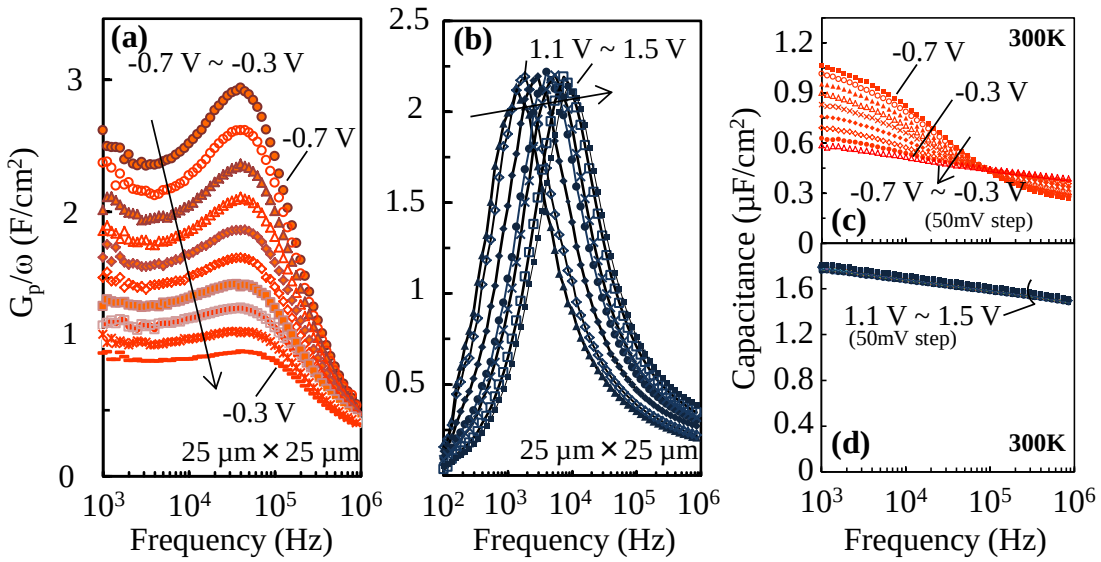


Figure 4.15 Conductance peak of HfO_2/InGaAs at (a) depletion and (b) accumulation condition. (c) and (d) show the capacitance at frequency range 1 kHz ~ 1 MHz

Compared to the depletion condition, the peaks in accumulation condition appear over a broader frequency range (1 kHz ~ 30 kHz) and the peak values are two orders of magnitude larger than depletion. Measured capacitance (Figure 4.15 (c) and (d)) begin a linear decrease trend at voltages higher than -0.3 V (depletion region).

Broad temperature (77K ~ 400K) conductance measurements were conducted to change Fermi level position and evaluate the interface admittance behavior. Figure 4.16 (a)~(d) shows that as the measurement temperature is lowered and the Fermi level is moved closer to the conduction band, the peaks in accumulation condition appear in higher frequencies at the corresponding gate biases while the peak size decreases.

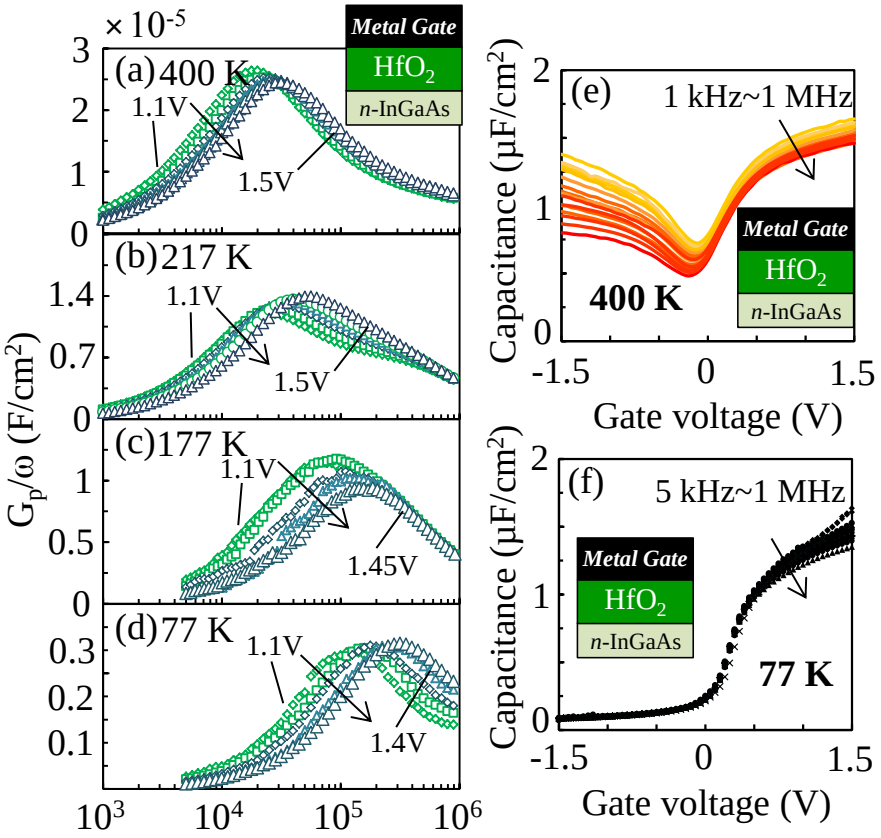


Figure 4.16 Temperature dependent conductance peak of HfO_2/InGaAs at (a) 400K, (b) 217K, (c) 177K, and (d) 77K. (e) and (f) show the *CV* characteristics at 400K and 77K

The *CV* characteristics of the MOS capacitors at 77K and 400K are shown in Figure 4.16 (e) and (f). The smaller peaks at higher frequencies for lower measurement temperatures trend, can also be observed in *p*-InGaAs as well, with accumulation peaks shifting to higher frequencies as the temperature is lowered (Figure 4.17).

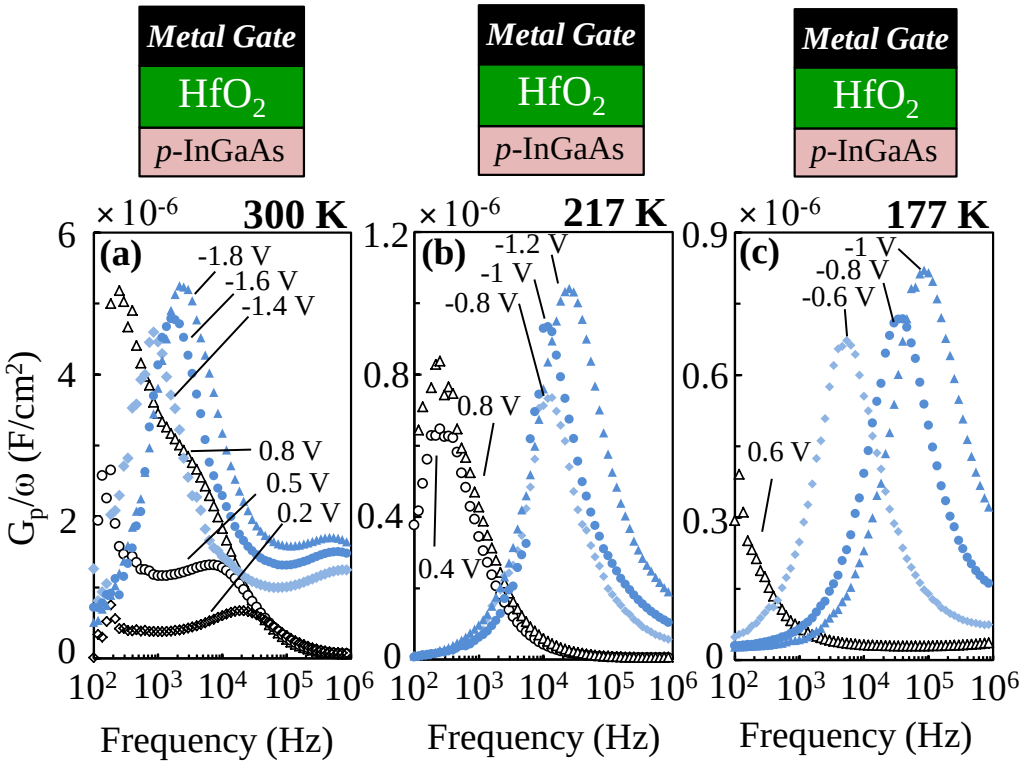


Figure 4.17 Temperature dependent conductance peak of HfO_2/*p*-InGaAs at (a) 300K, (b) 217K, and (c) 177K

Trapping time constants extracted from accumulation condition peak frequency across the band gap by varying the measurement temperature are summarized in Figure 4.18. It is evident that time constant across the band edges are smaller but increase around the mid-gap. This behavior can be explained by assuming a trap energy level between the conduction band edge and Fermi level. Since the trapping sites respond to higher frequency at lower temperature, the trapping energy level can be assumed within the bulk of the semiconductor.

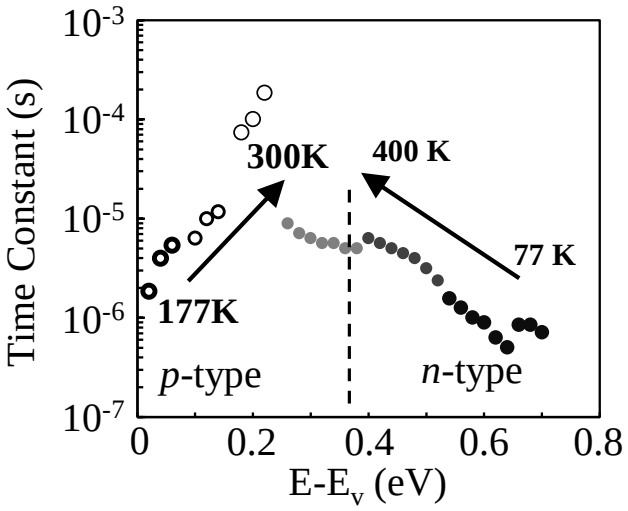


Figure 4.18 Trap time constant of HfO_2/InGaAs interfaces extracted from *n*- and *p*- InGaAs MOS capacitors

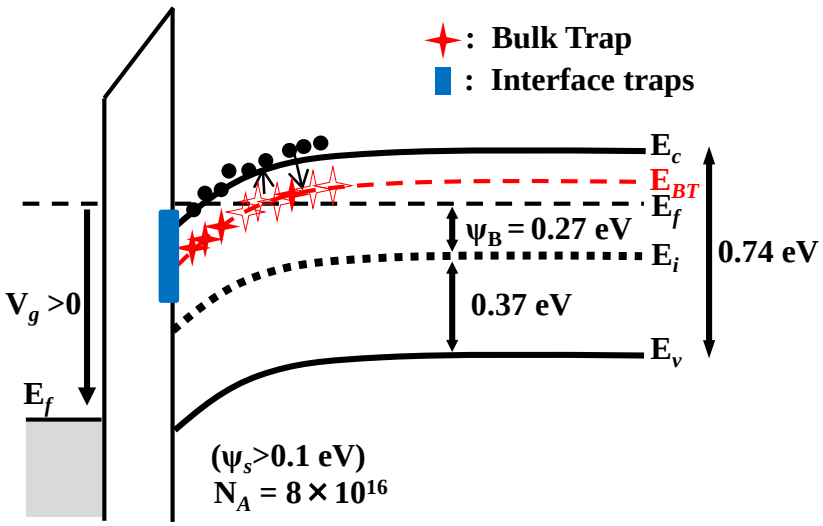


Figure 4.19 Illustration of InGaAs band diagram of incorporating a trap energy level within the bulk of InGaAs

Cross-sectional TEM images of the W/HfO_2/*n*-InGaAs gate stack shows void like defects at the interface (Figure 4.21). The density of InGaAs at these defect sites is lighter than the rest of the substrate.

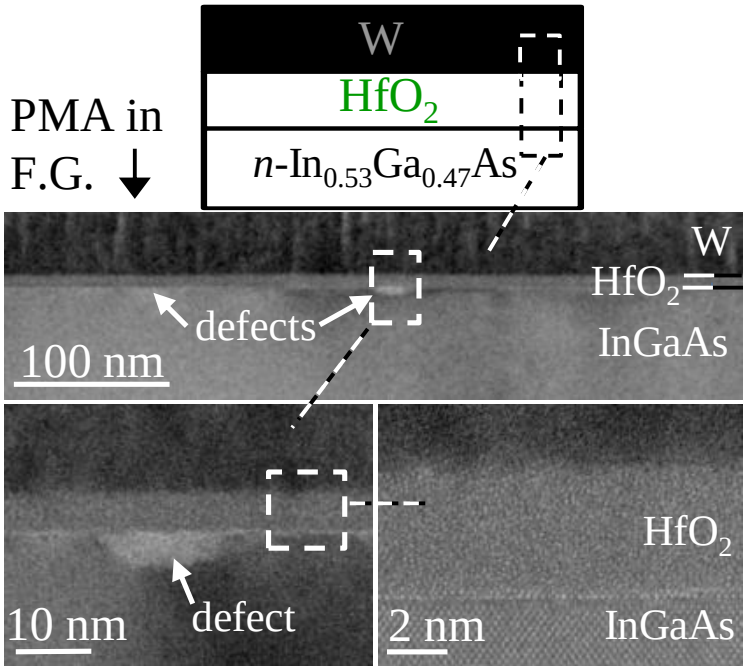


Figure 4.20 Cross-sectional TEM image of W/HfO_2/InGaAs MOS capacitor

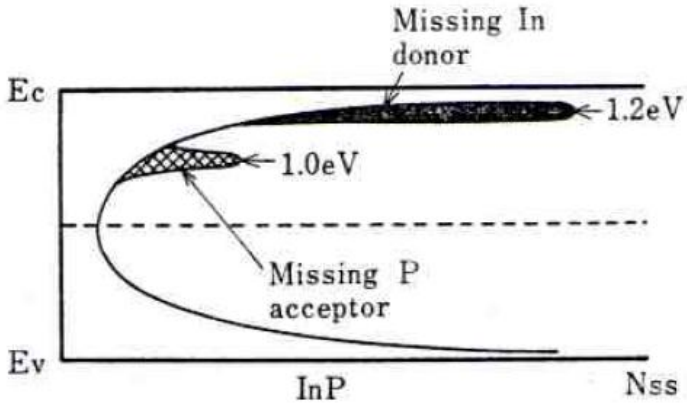


Figure 4.21 Band diagram of GaAs showing the energy level creating by missing In donors [4.10]

It has been reported that In-containing compound semiconductors such as InP, loose some of In atoms from their surface upon thermal annealing (Figure 4.21). These defects can act like depletion centers that would trap and emit charges from the band edges. Based on these results, a summary of defect mechanisms and their effect on *CV* measurements are proposed in Figure 4.22 and Table 4.1.

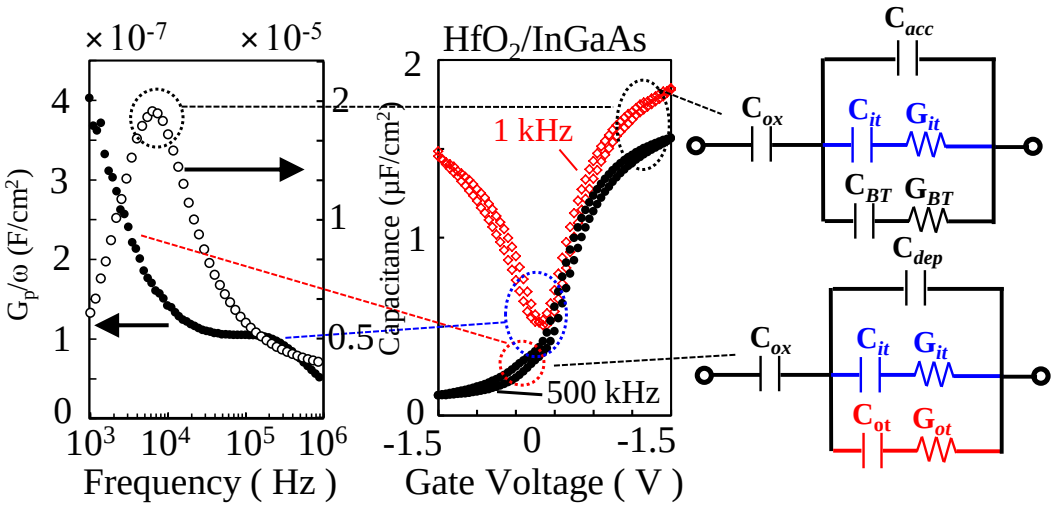


Figure 4.22 Equivalent circuits contributing to the capacitance and conductance characteristics of oxide/semiconductor interface

	Oxide (bulk or border)	Interface states	Semiconductor bulk
Hump	○	△	—
hysteresis	△	—	—
Strech-out	—	○	—
Accumulation frequency dispersion	△	—	○

Table 4.1 Summary of trapping mechanisms and their effect on *CV* characteristics

4.5 Conclusions

The effect defects at the bulk of InGaAs for HfO_2/InGaAs interface on electrical properties of MOS capacitors was investigated. Diffusion of elements from the substrate cause void like defects at the interface that can act like depletion centers causing frequency dispersion in *CV* characteristics of the MOS capacitor. It was shown that although high temperature deposition of HfO_2 can reduce the defect formation through compensation of missing substrate elements, more effective methods are required to prevent the diffusion of elements from the substrate into gate dielectric.

4.6 References

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Chapter 5

Gate Stack Engineering for InGaAs-based MOS Capacitors with La_2O_3 Gate Dielectric

Chapter 5 Gate Stack Engineering for InGaAs-based MOS Capacitors with La_2O_3 Gate Dielectric

5.1 Fundamental Properties of La_2O_3 Gate Dielectric

5.1.1 Introduction

Low standby power (LSTP) technology requirements in the near term years according to the International Technology Roadmap for Semiconductors (ITRS) are listed in Table 5.1 [5.1]. As can be seen, more aggressively scaled Equivalent Oxide Thickness (EOT) is required in order to reach the specifications beyond 22 nm node.

		2018	*2020*	*2022*	*2024*	*2026*
L_g (nm)		**14**	**11.7**	**9.3**	**7.4**	**5.8**
V_{dd} (V)		**0.63**	**0.61**	**0.58**	**0.56**	**0.54**
EOT (nm)		**0.68**	**0.62**	**0.56**	**0.50**	**0.45**
Mobility enhancement factor due to channel material	III-V	**8**	**8**	**8**	**8**	**8**
	Ge	**4**	**4**	**4**	**4**	**4**
C_g Ideal (fF/μm)	III-V	**0.28**	**0.24**	**0.20**	**0.16**	**0.13**
	Ge	**0.41**	**0.36**	**0.30**	**0.25**	**0.21**
$V_{t,sat}$ (mV)	III-V	**229**	**230**	**238**	**245**	**251**
	Ge	**230**	**231**	**241**	**249**	**254**
CV/I (ps)	III-V	**0.13**	**0.11**	**0.09**	**0.07**	**0.06**
	Ge	**0.21**	**0.17**	**0.13**	**0.10**	**0.08**

Table 5.1 *ITRS requirements for III-V technology*

This leads to stringent control of interfacial oxide layer, either by reducing its thickness or by increasing its *k*-value. A good interface requires either that the oxide is amorphous, or that it is epitaxial and lattice-matched to the underlying semiconductor substrate. Amorphous oxides are the key for a low-cost solution; nonetheless the challenge is to keep these materials amorphous even after post-deposition high temperature processing in order to avoid increased surface roughness and additional leakage current due to the formation of grain boundaries, as shown in many investigations [5.2].

A silicate formation is known to occur when a rare earth oxide is in contact with a Si-containing dielectric or a silicon substrate in the presence of oxygen [5.3]. La_2O_3 is a rare-earth high-*k* oxide with properties that can fulfill the requirements for next generation device dielectrics. *n*MOSFET operation with scaled EOT using La_2O_3 has been reported [5.4]. Annealing La_2O_3/Si stack, results in the formation of La-silicate layer at the interface which is amorphous, has a high *k*-value and is thermally stable.

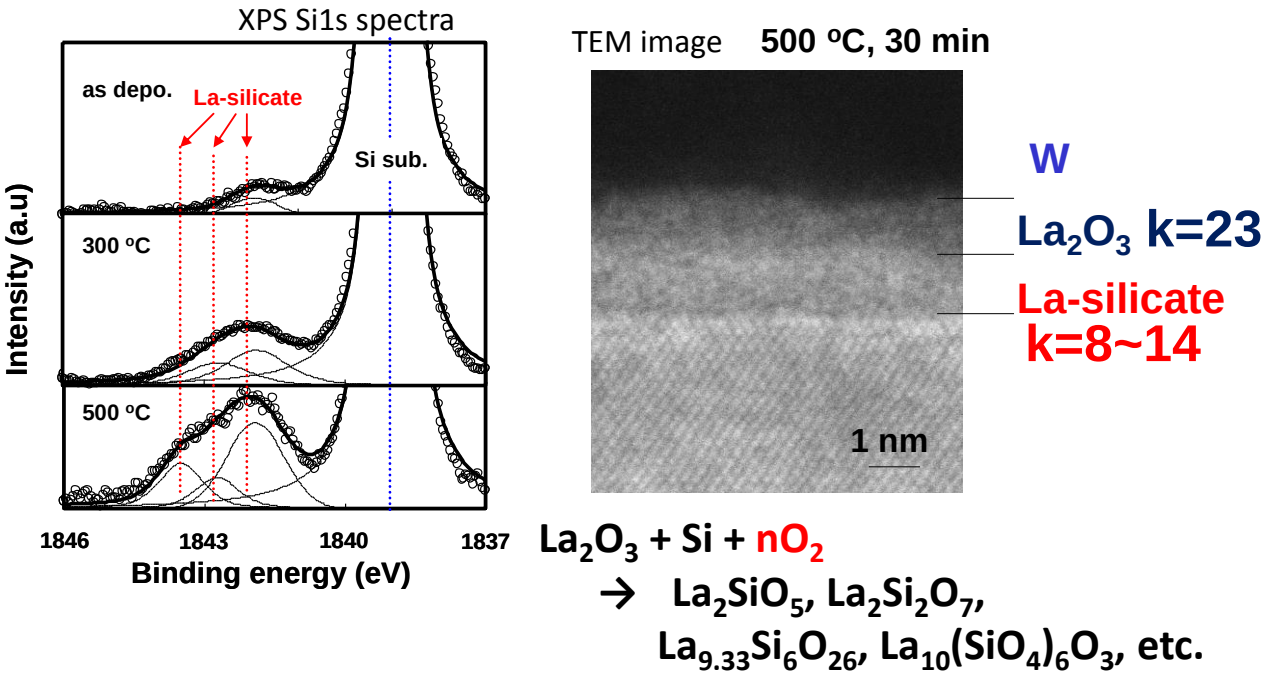


Figure 5.1 La-Silicate formation at Si interface

Figure 5.1 shows the cross-sectional TEM image and XPS analysis of La_2O_3 MOS capacitors. The formation of La-silicate can be confirmed by both methods and a *k*-value of 8~14 is estimated for the interfacial La-silicate layer [5.5]. The ability of La-atoms to create bonds with both Si and oxygen atoms, is the underlying mechanism of silicate formation at the oxide/Si interface. In fact it is the half full *d*-orbital of rare-earth metals that makes them active in formation of bonds with neighboring atoms. In order to investigate the bonding properties of La_2O_3 with InGaAs substrate, InGaAs-based MOS capacitors with both La_2O_3 and HfO_2 were fabricated separately and evaluated.

5.1.2 Experimental Procedure

Figure 5.2 shows the fabrication process of MOS capacitors. MOS capacitors with both La_2O_3 and HfO_2 as gate dielectric were fabricated in order to compare their characteristics. The La_2O_3 and HfO_2 films were deposited using e-beam evaporation in an ultra-high vacuum chamber, followed by *in-situ* metal deposition by RF sputtering. For both samples 50-nm Tungsten (W) metal gate was used as the gate electrode. The samples were post-metallization annealed in forming gas ambient (N_2:H_2 = 97%:3%) for 5 mins. Finally, Al was deposited on the back side of the InGaAs/InP substrate to form the back contact. Hard x-ray (7.94 keV photons) excited photoelectron spectra arising from As $2p_{3/2}$, Ga $2p_{3/2}$, and In $3d_{5/2}$ core levels of the MOS capacitors with 10-nm HfO_2 or La_2O_3 as gate dielectric, were measured at photoelectron take-off angle of 80^o with energy resolution of 100 meV at beam line (BL46XU) using high resolution electron energy analyzer R-4000. For XPS measurements, the gate metal thickness was reduced from 50-nm to 10-nm to enable probing interface reaction.

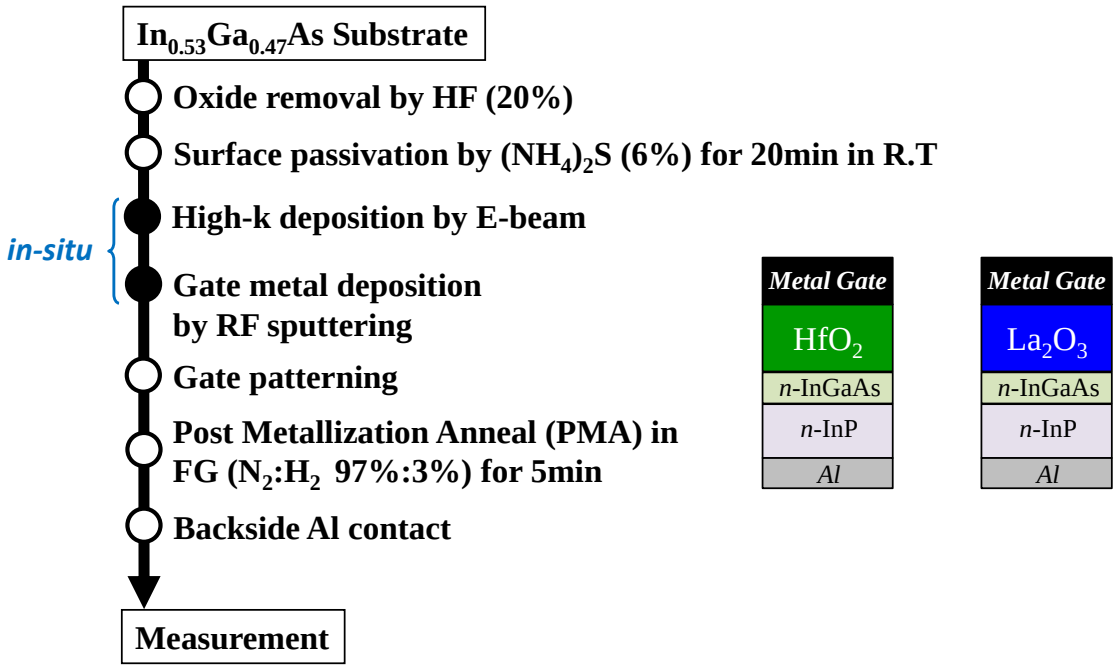
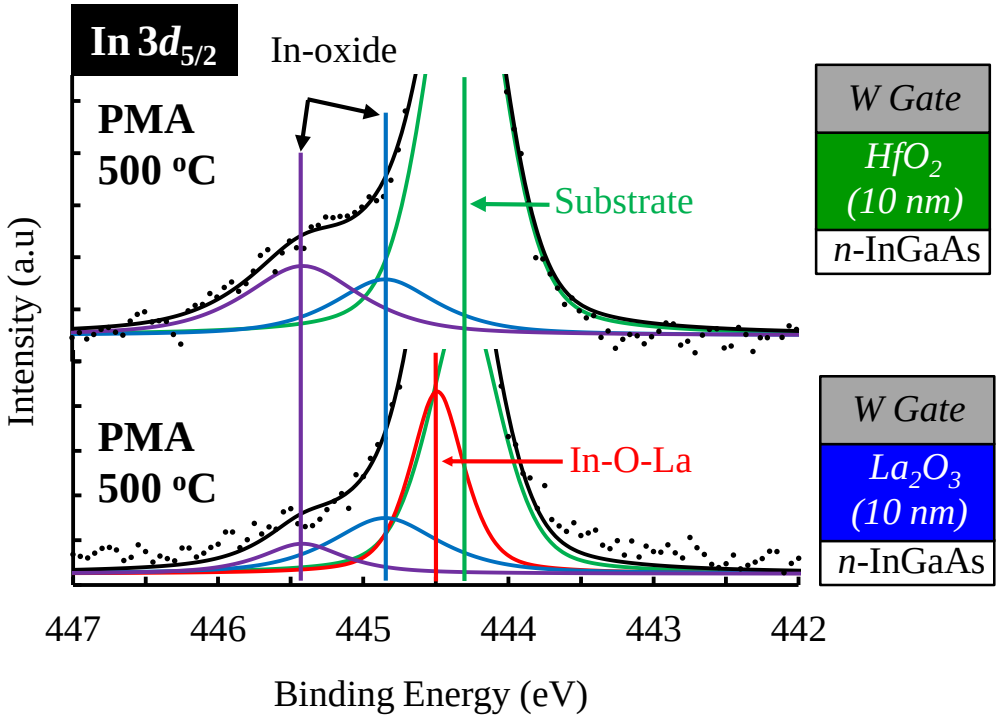


Figure 5.2 Experimental flow for MOS capacitors fabrication

5.1.3 Comparing HfO_2 and La_2O_3 Reaction at InGaAs Interface

Figures 5.3 (a) and (b) show the XPS results for the two samples after PMA in FG at 500 ^{o}C for 5 min. Intermixing of La_2O_3 with the substrate through the formation of Ga-O-La and In-O-La bonds can be observed for the W/La_2O_3/InGaAs samples. At the same time the Ga and In sub-oxides form in a much smaller amount for La_2O_3 sample compared to the HfO_2 case.



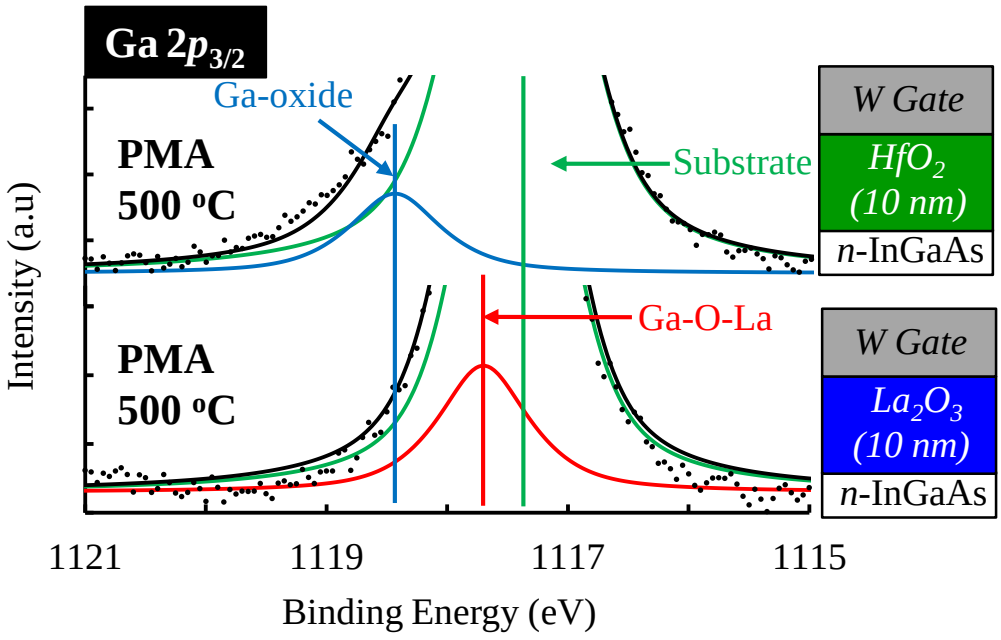


Figure 5.3 Hard-XPS spectra of La_2O_3/InGaAs and HfO_2/InGaAs

Comparing the XPS results for As $2p_{3/2,}$ shows that although a significant amount of AsO_x remain after annealing the sample with HfO_2, no detectable amount of the same AsO_x species can be observed for the sample with La_2O_3 as is seen in Figure 5.4.

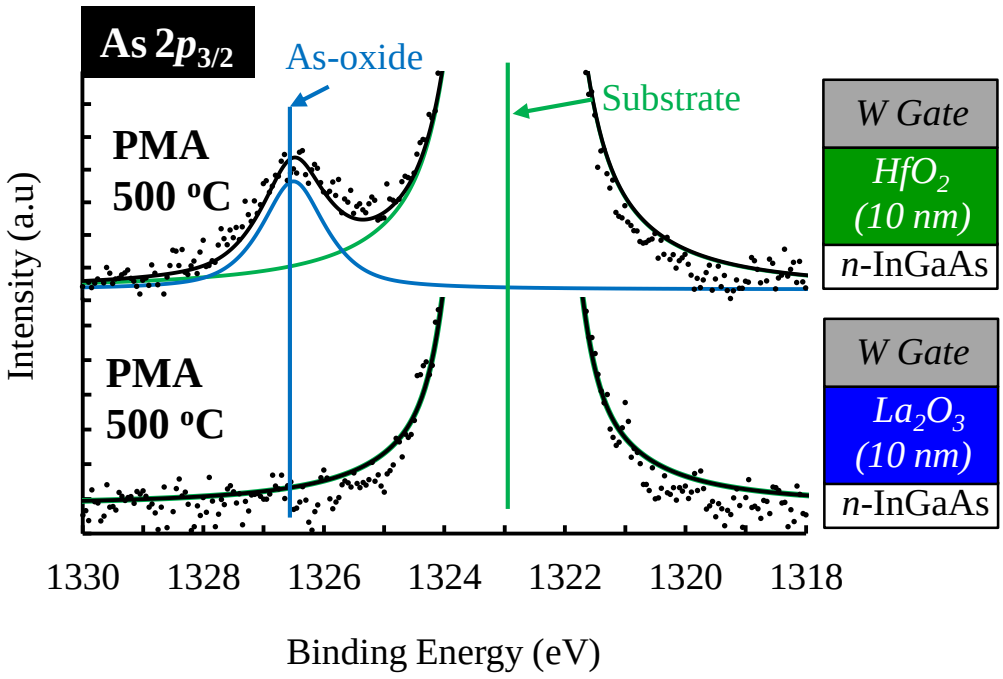


Figure 5.4 Hard-XPS spectra of La_2O_3/InGaAs and HfO_2/InGaAs

The As-oxides are the most unstable of the oxides and are easily removed or converted to the more stable Ga oxides, in particular Ga_2O_3. It is reported that the stability of this oxide state makes it difficult to remove during chemical processing, however the ability of La atoms to form bonding states with GaO_x species can suppress the formation of Ga_2O_3 compared to HfO_2 sample.

Cross-sectional TEM image of W (50 nm)/ La_2O_3 (7 nm)/ InGaAs MOS capacitor is shown in Figure 5.5 (a). In order to evaluate compositional structure of the stack, four points are chosen for Energy-dispersive X-ray spectroscopy (EDX) measurements and the results are summarized in Figures 5.5 (b) and (c).

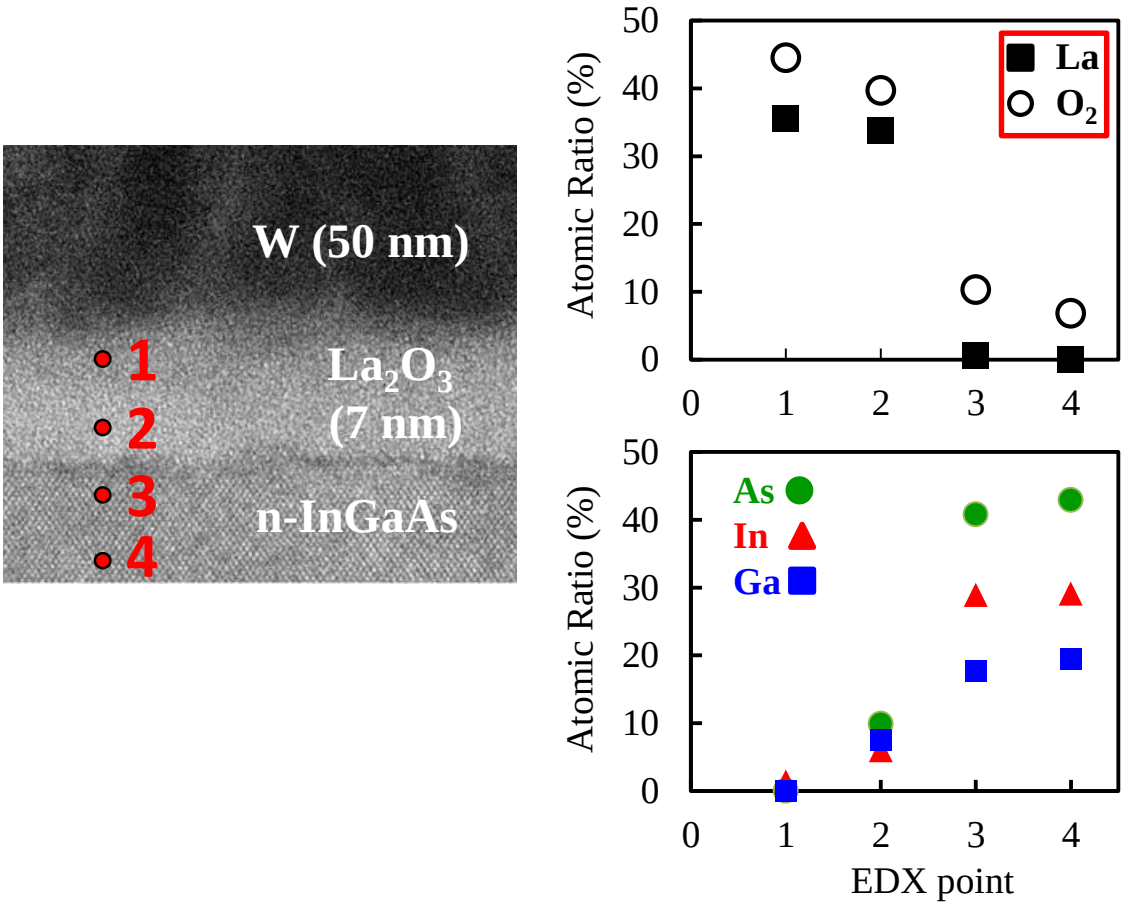


Figure 5.5 Cross-sectional TEM image and EDX analysis of W/La_2O_3/InGaAs gate stack

Two of the points are chosen within the La_2O_3 gate dielectric, and two are chosen within the substrate. Roughly same amount of atomic ratio for the three substrate elements (In, Ga, and As) is detected at point 2 which is close to the interface of oxide/InGaAs. This fact hints to a uniform intermixing of La-oxide with InGaAs substrate. However no amount of In, Ga, or As elements were detected close to the W metal gate. Also the atomic ratio of the three substrate elements, remain constant within the bulk of the substrate. Although a slight decrease in the atomic ration of O_2 is observed from point 1 to 2, the atomic ratio of La atoms remains the same throughout the dielectric. These results are in agreement with XPS measurements which predicted the formation of La bonds with oxygen and elements from the substrate. Based on these results a model to express the difference between La_2O_3/InGaAs and HfO_2/InGaAs is proposed which is shown in Figure 5.6.

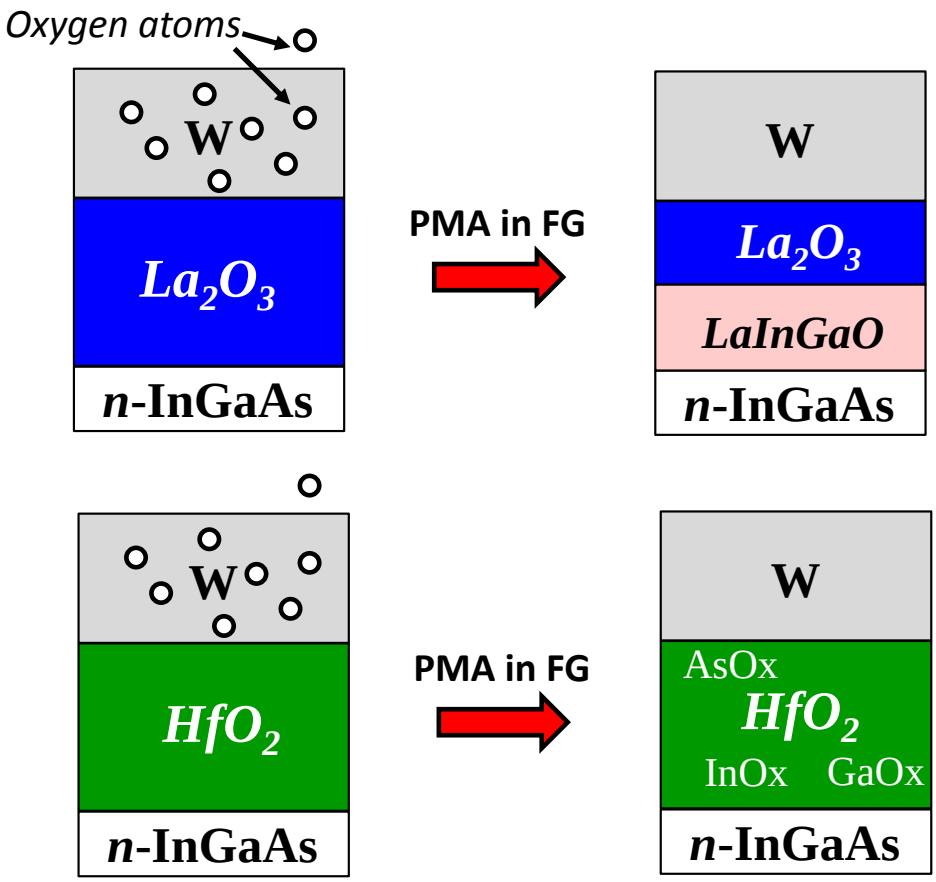


Figure 5.6 Comparison between La_2O_3/InGaAs and HfO_2/InGaAs reaction difference

It was reported that the sputtered W contains large amounts of oxygen [5.6], the supply of oxygen from W and its diffusion to the gate dielectric upon annealing, triggers the reaction at the interface resulting in the formation of IL layer. On the other hand, diffusion of substrate elements into HfO_2, results in the formation of As, In and Ga oxides. These oxides are unstable in high annealing temperatures and create interface states through the creation of As-antisites and Ga dangling bonds upon their

disintegration [5.7]. *CV* characteristics of W (50nm)/La_2O_3 (10 nm)/InGaAs MOS capacitor at the measurement frequency range of 5 kHz ~ 1 MHz after annealing in FG at 370 ^oC is shown in Figure 5.7.

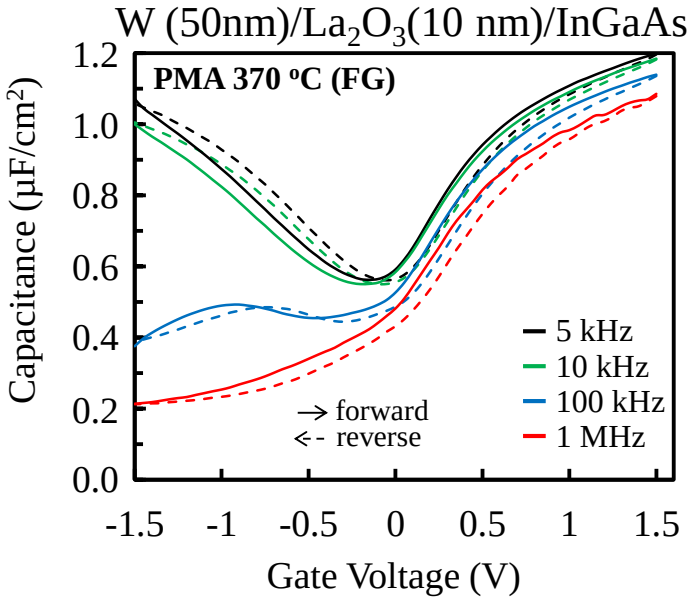


Figure 5.6 *CV* characteristics of W (50 nm)/La_2O_3 (10 nm)/InGaAs MOS capacitor

The capacitance response at lower frequencies is typical of high-*k*/InGaAs interfaces with very high interface state density (usually in the order of 10^{13} $eV^{-1}cm^{-2}$) which is commonly reported in the literature. Furthermore, a comparison between the 1 MHz *CV* curve with the ideal *CV*, shown in Figure 5.7, reveals a large stretch out and a failure to reach depletion capacitance. These results are indicative of Fermi level pinning which is

the inability of Fermi level to effectively sweep through the InGaAs band gap from the conduction band to the valance band.

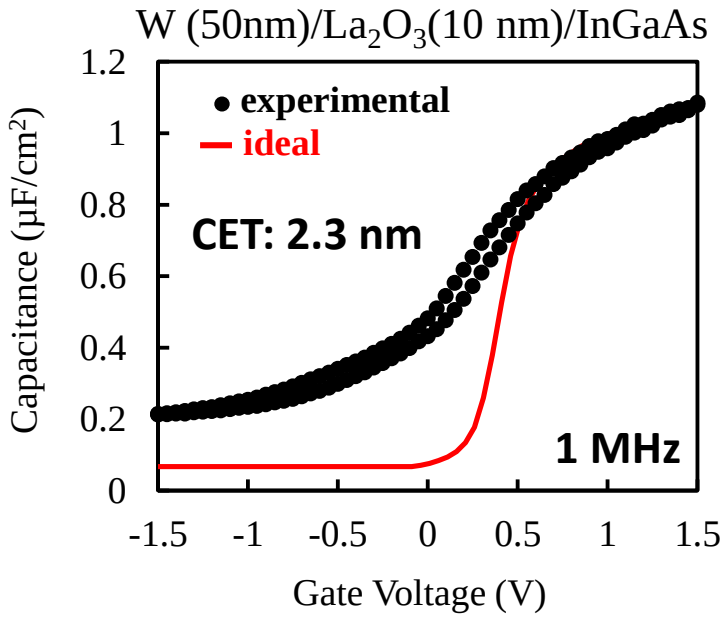


Figure 5.7 Comparison of 1 MHz *CV* characteristics of W (50 nm)/La_2O_3 (10 nm)/InGaAs MOS capacitor to the ideal *CV*

The gate leakage dependence of La_2O_3-based MOS capacitors on annealing temperature at CET= 2.3 nm is shown in Figure 5.8. The leakage current at 500 ^oC, already surpasses 1 A/cm^2 which is the limit that *CV* characteristics can be measured without being affected by the excessive leakage current.

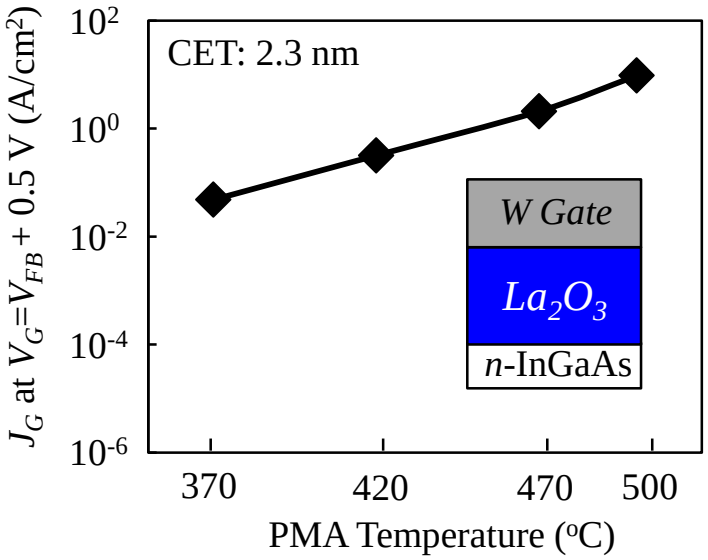


Figure 5.8 PMA dependence of W (50 nm)/La_2O_3 (10 nm)/InGaAs MOS capacitor gate leakage

As a result scaling La_2O_3/InGaAs gate stack by simply reducing the thickness of La_2O_3 film is not achievable unless the interface quality is improved and the increase in gate leakage current is resolved.

5.1.4 Conclusions

In this sub-chapter the fundamental difference of interfacial reaction between HfO_2 and La_2O_3 at InGaAs interface was described. The diffusion of elements from the substrate (In, Ga, and As) to HfO_2, result in the formation of unstable oxides at the surface of the substrates as well as within in the dielectric, and defects within the substrate. On the other hand, a reactive amorphous layer in the form of LaInGaOx is formed at La_2O_3/InGaAs interface through the intermixing of La atoms with substrate elements. Judging from TEM and EDX analysis, this amorphous layer seems to block excessive diffusion of elements from the substrate to the gate dielectric. However, the electrical characteristics of the W/La_2O_3/InGaAs MOS capacitors show that it is necessary to control the composition and thickness of this IL in order to improve the interface quality and realize the scalability potential of La_2O_3 as a high-*k* dielectric for InGaAs-based devices.

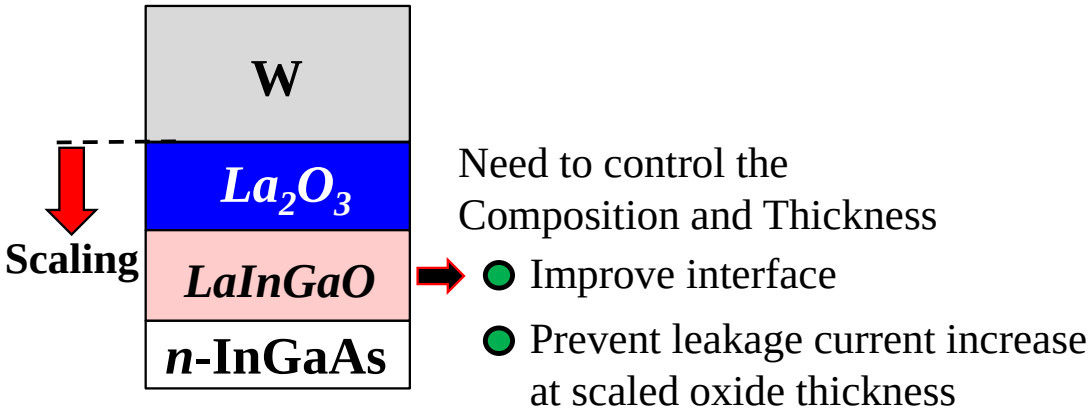


Figure 5.9 Schematic showing the required approach for improving

La_2O_3/InGaAs interface

In the following sections of chapter 5, new methods to improve the La_2O_3/InGaAs interface are introduced. Diffusion of Oxygen into gate dielectric is controlled through various methods and their efficiency are compared and discussed.

5.2 Self-Assembly- Monolayer Surface Passivation

5.2.1 Introduction

$In_{0.53}Ga_{0.47}As$ has been the focus of research as an alternative channel material since it offers a very good trade-off between the superior transport properties of InAs and the low leakage properties of GaAs [5.8, 5.9]. However, achieving high permittivity (high-*k*) gate dielectrics/III-V interface with low interface trap densities (D_{it}), which is necessary for high performance MOSFETs is extremely difficult when ex-situ deposition methods are applied. Therefore, careful treatment of substrate surface prior to gate dielectric deposition is required. To lower the interface trap density at the high-*k*/III-V semiconductor interface, sulfur passivation and Si layer insertion have been widely studied as means of surface treatment [5.10, 5.11]. The incorporation of Si into gate stack, is reported to improve the high-*k*/III-V interface significantly [5.12]. However, the increase in capacitance equivalent thickness (CET) resulting from this Si layer remains a problem.

In previous section the limitation of $W/La_2O_3/InGaAs$ structure due to excess of IL formation was discussed. In this section the effect of InGaAs surface passivation by

Si-monolayer is described. In order to form a Self-Assembled Monolayer (SAM) of Si atoms on InGaAs substrate, hexamethyldisilazane (HMDS) which contains Si atoms is used. The molecular structure of HMDS forces the molecules to attach to the substrate through the oxygen bond. Once the entire surface of the substrate is covered by HMDS molecules, the process should stop since the saturated CH3- molecules cannot form any new bonds. This would result in the formation of a mono-Si layer on the substrate's surface. A schematic of a surface, passivated by HMDS is shown in Figure 5.10.

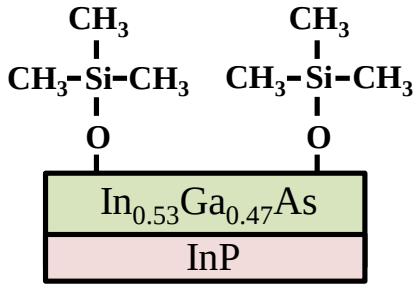


Figure 5.10 Schematic of InGaAs surface passivation by HMDS

HMDS passivation effects have been reported on thin film transistors before; however, to our knowledge, no published results are available for its application on III-V based substrates. After HMDS treatment, InGaAs substrates were used to fabricate $W/La_2O_3/In_{0.53}Ga_{0.47}As$ capacitors. The electrical characteristics of these capacitors were compared with capacitors prepared with widely-used aqueous sulfur passivation

method.

5.2.2 Experimental Procedure

InGaAs capacitors were fabricated on n-type $In_{0.53}Ga_{0.47}As(100)$ substrates epitaxially grown on *n*-type InP substrates with Si doping concentration of 1×10^{17} cm^{-3}. Substrates were initially degreased by acetone/ethanol and native oxides were removed by concentrated (20%) HF for 2 min. Next, one set of substrate was immediately dipped in a $(NH4)_2S$ solution (concentration 7%) at room temperature for 30 min to acquire a sulfur passivated surface. Another set was put in a beaker filled with HMDS vapor for 3 min at 100 ^oC in order to form an HMDS layer on the substrate surface. These samples prepared with three different treatment methods are referred to as sample I, sample II, and sample III throughout section 5.2 and are summarized in Table 5.1.

	Sample I	Sample II	Sample III
Oxide removal	HF (20 %) 1 min	HF (20 %) 1 min	HF (20 %) 1 min
Surface treatment	-	$(NH_4)_2S$ 30 min	HMDS vapor 3 min

Table 5.1. Summary of the samples and the applied surface treatment method

After the initial surface treatment, all samples were immediately transferred to the deposition chamber to avoid any extra re-oxidation of the substrate surface because of the prolonged air exposure. 7-nm La_2O_3 layer was deposited by e-beam evaporation at room temperature at a deposition rate of 0.2 nm/min in 10^{-6} Pa. A 50-nm-thick W layer as the gate electrode was deposited *in situ* by RF magnetron sputtering and gates were patterned by SF_6 reactive ion etching. Capacitors were post-metallization annealed (PMA) in a rapid thermal annealing (RTA) furnace in forming gas (FG) (N_2:H_2= 97:3%) ambient. Al contact layer on the backside of the substrates was deposited by thermal evaporation. Figure 5.11 shows the schematic cross-sectional view of the capacitor structure.

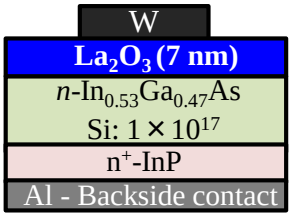


Figure 5.11 Schematic of the W (50 nm)/La_2O_3 (7 nm)/InGaAs MOS capacitor

5.2.3 Comparison Between Wet Surface Passivation Methods

Figure 5.12 shows the *CV* characteristics of sample I (only treated by HF (20%)) after annealing in FG at 500 ^{o}C. The measurements are conducted at 1 kHz ~ 1 MHz frequency range at room temperature.

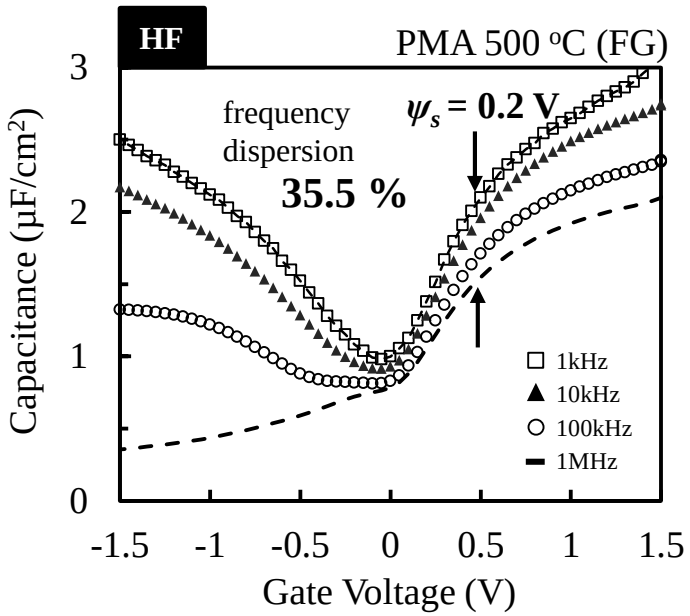


Figure 5.12 *CV* characteristics of W (50 nm)/La_2O_3 (7 nm)/InGaAs MOS capacitor with only HF treatment

The *CV* curves of MOS capacitors with surface passivation, samples II and III, are shown in Figures 5.13 (a) and (b) respectively.

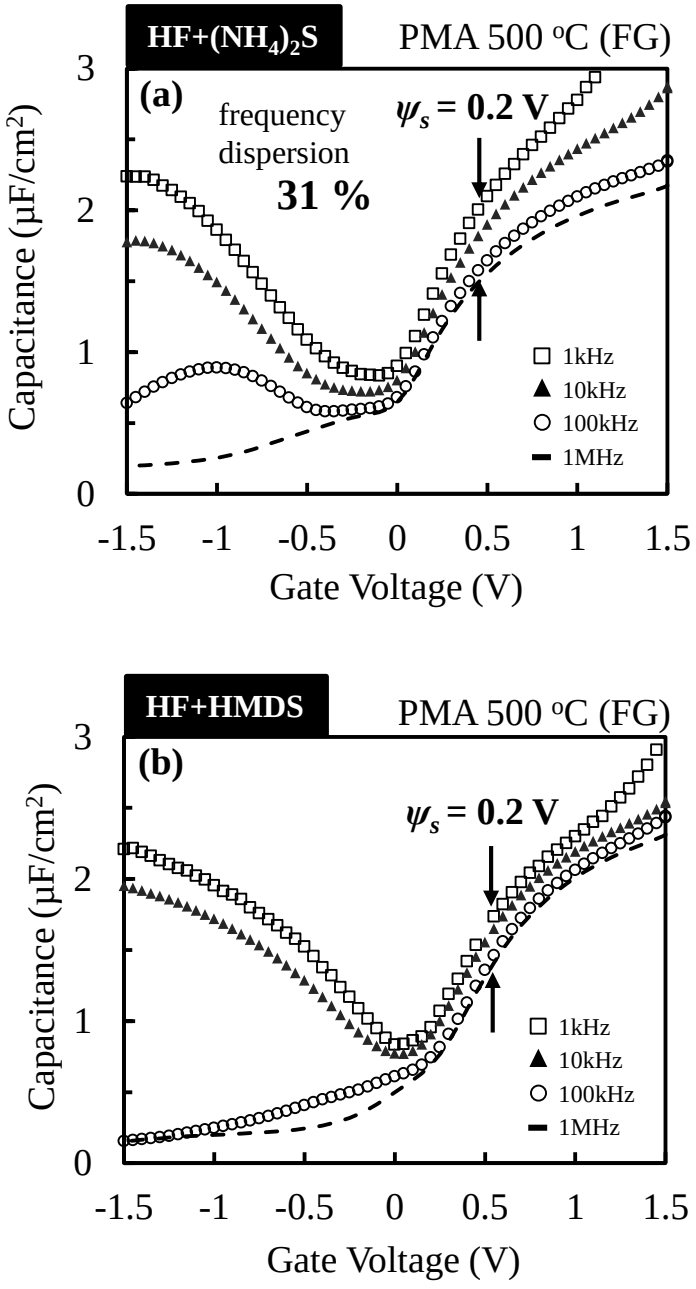


Figure 5.13 *CV* characteristics of W (50 nm)/La_2O_3 (7 nm)/InGaAs MOS capacitor with (a) $(NH_4)_2S$ and (b) HMDS treatment after HF treatment

A qualitative comparison of these figures points to an improved interface property of sample III, which is treated by HMDS. Frequency dispersion [defined as ($C_{1\ kHz} - C_{1\ MHz}$) / $C_{\ 1\ MHz}$ ×100 %] of the samples at gate voltage of roughly 0.5 V is shown in each figure. A surface band bending of 0.2 V at this bias voltage is sufficient to probe the depletion to accumulation region without capacitance response being affected by the up-turns due to leakage current [5.13]. The dissipation factor (D) of the capacitors at this voltage and frequency range is below 1.0 which should ensure a less than 4% error in measurement accuracy [5.14]. It should be noted here that the physical dielectric thickness and deposition conditions are the same for the three samples; thus, HMDS treatment of the surface allows for the deposition of smaller La_2O_3 thickness by improving the interface quality. The large frequency dispersion of 35% in sample I (treated with only HF) is effectively suppressed to 18% in sample III, treated with HMDS. The 1MHz curve in sample III is not dominated by mid-gap D_{it} response which appears as a hump in negative gate voltages and a failure to reach the depletion capacitance [5.15]. The CET of the samples, shown in Figure 5.14, were estimated by fitting the accumulation capacitance at 1 MHz (D<1) to the ideal *CV*.

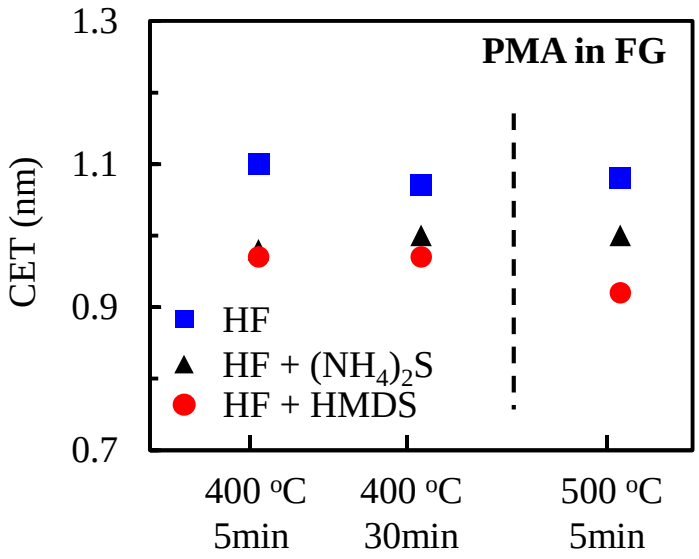


Figure 5.14 CET of W (50 nm)/La_2O_3 (7 nm)/InGaAs MOS capacitor with various surface treatment methods

The Annealing condition was varied between the annealing temperature and time to evaluate the effect of both parameters on electrical characteristics of the samples.

Although increasing annealing temperature generally causes thicker CET, the *CV* response of the capacitors suffers from greater hysteresis and frequency dispersion in lower annealing temperatures. Figure 5.15 shows the 1 MHz *CV* curve hysteresis of the capacitors against PMA condition, measured at a bias voltage range of -1.5 to 1.5 V with 50 mV intervals.

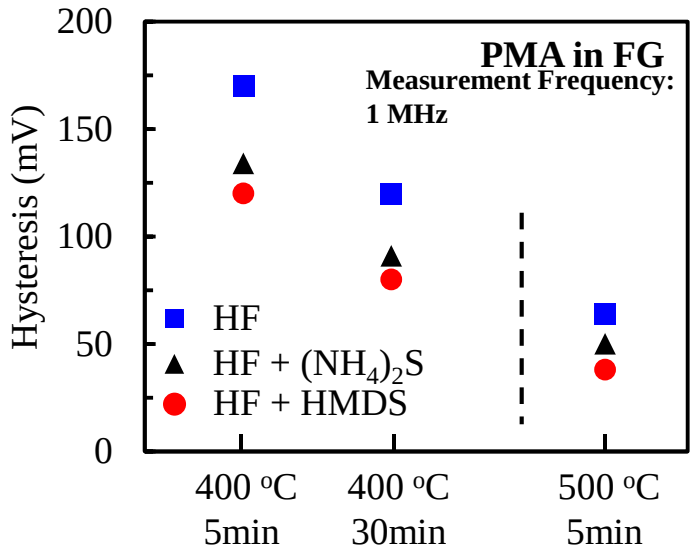


Figure 5.15 Hysteresis of W (50 nm)/La_2O_3 (7 nm)/InGaAs MOS capacitor with various surface treatment methods

A steady decrease of hysteresis with higher annealing temperatures and time for all samples is observed, regardless of the applied surface treatment method; however sample III exhibits the minimum hysteresis value of 30 mV. Thus by HMDS-treatment of InGaAs surface prior to La_2O_3 deposition, a more stable interface can be obtained, which is evident from a smaller CET with improved hysteresis and frequency dispersion at higher annealing temperatures. [5.16]

The influence of surface preparation on interface states density was quantitatively compared by the conductance method. The peak conduction measurements as a function of the gate voltage for all three samples are shown in Figure 5.16 (a) and (b).

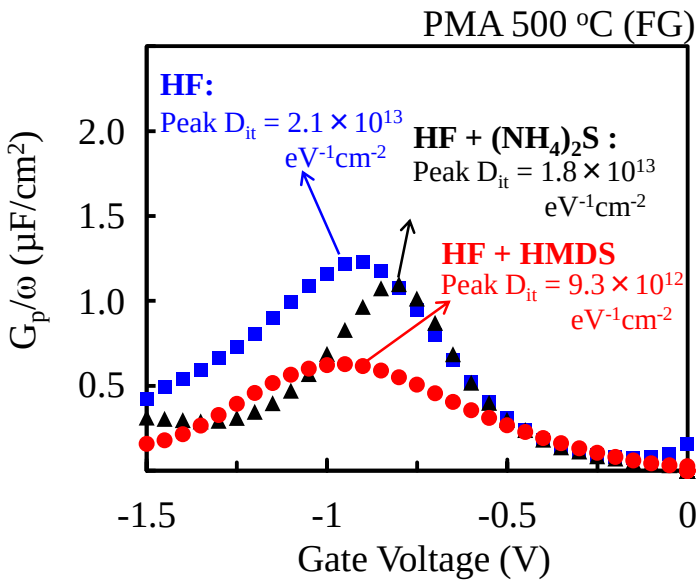


Figure 5.16 Peak conductance of W (50 nm)/La_2O_3 (7 nm)/InGaAs MOS capacitor

with various surface treatment methods

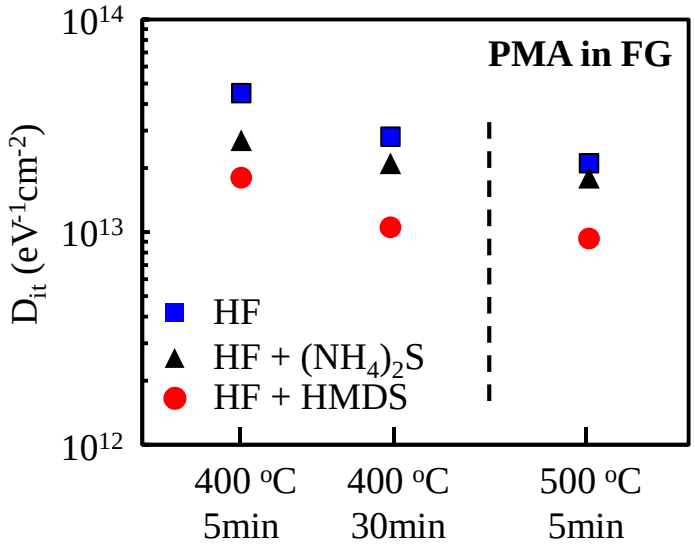


Figure 5.16 peak D_{it} of W (50 nm)/La_2O_3 (7 nm)/InGaAs MOS capacitor

with various surface treatment methods

The capacitor treated with HMDS (sample III) shows an equivalent parallel conductance loss that is smaller than that of samples I and II by a factor of 0.44 and 0.51, respectively. Furthermore, annealing at 500 ^{o}C improves the interface states for all samples and a minimum value of peak D_{it} ~ 9.3×10^{12} eV^{-1}cm^{-2} obtained for sample III.

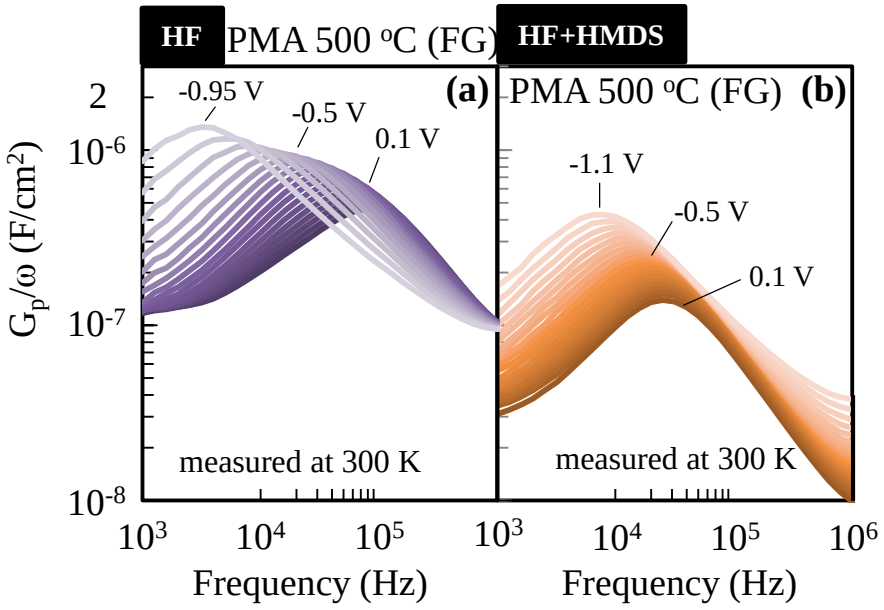


Figure 5.17 Conductance peak distribution of W (50 nm)/La_2O_3 (7 nm)/InGaAs MOS capacitor with HMDS treatment on HF only treatment

The conductance as a function of frequency and voltage for samples I and III (PMA 500 ^{o}C) in Figs. 8(a) and 8(b) shows larger and wider G_p/ω peaks for sample I compared to sample III over the same voltage range. This would reflect in the energy distribution of the interface states indicating a lower D_{it} at band-edges for HMDS treated sample.

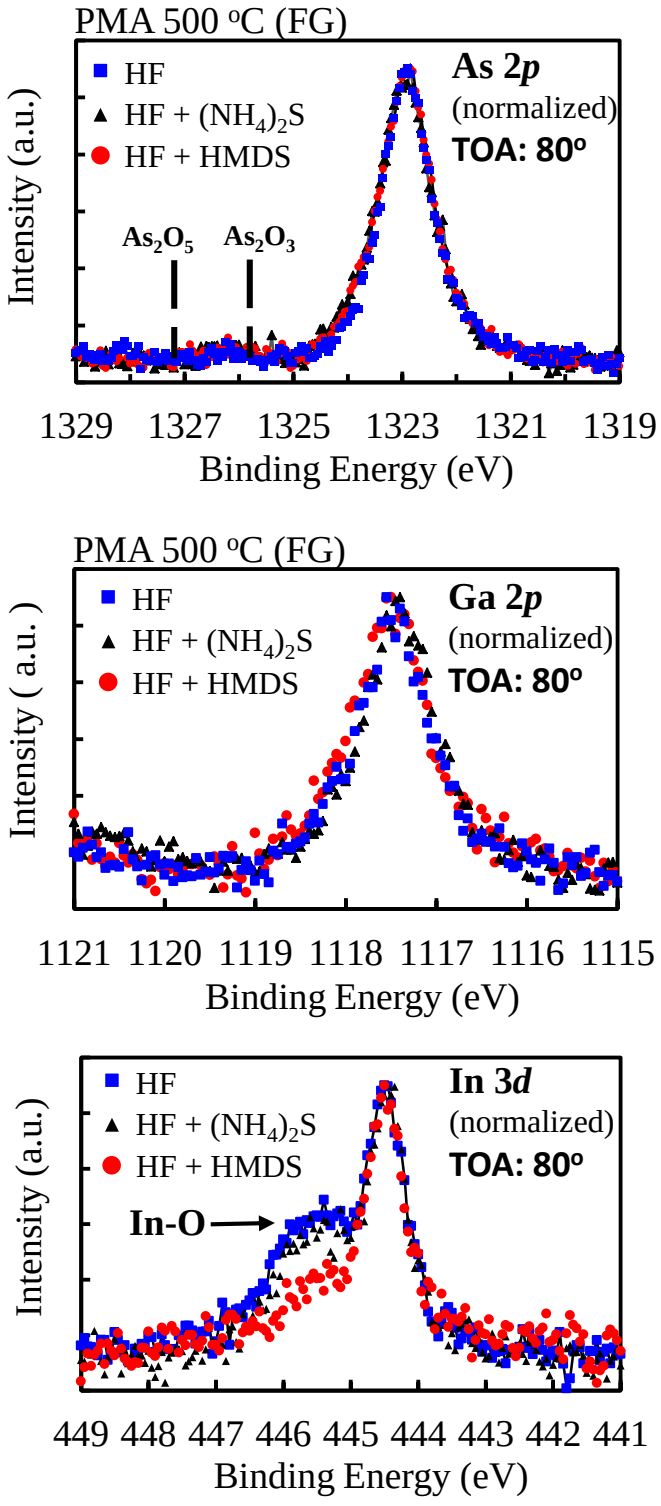


Figure 5.18 XPS spectra of W (5 nm)/La_2O_3 (7 nm)/InGaAs MOS capacitor

with various surface treatment methods

X-ray photoelectron spectroscopy (XPS) measurement was conducted for all three samples to clarify the nature of interface modifications. The formation of both As and Ga sub-oxides were sufficiently suppressed regardless of the applied surface treatment method. On the other hand, formation of In suboxides (In-O) was considerably reduced by using HMDS treatment.

5.2.4 Conclusions

The effects of the post metallization annealing and the modification of high-*k*/$In_{0.53}Ga_{0.47}As$ interface with sulfur or HMDS cleaning and passivation by measuring the electrical characteristics of W/La_2O_3/*n*-$In_{0.53}Ga_{0.47}As$ capacitors were investigated. Experimental results showed that HMDS treatment of $In_{0.53}Ga_{0.47}As$ surface prior to high-*k* oxide deposition, results in reduced frequency dispersion and interface state densities of W/La_2O_3/$In_{0.53}Ga_{0.47}As$ capacitors without sacrificing capacitance value in accumulation condition. This was due to the passivation effect of HMDS by forming a mono-layer of Si on InGaAs surface and changing the sub-oxide formation at the La_2O_3/*n*-$In_{0.53}Ga_{0.47}As$ interface.

5.3 Applying La-Silicate Structure to InGaAs-based Capacitors

5.3.1 Introduction

Interfacial passivation layers (e.g., amorphous Silicon) between the dielectric and III-V semiconductor have been explored previously [5.17]. It is shown that presence of a thin Si layer (1.2 nm) at the interface could substantially suppress the frequency dispersion of GaAs MOS capacitors. A complete absence of As-oxides due to either the ALD "self-cleaning" phenomenon [5.18] or the reducing effect of reaction between Si with surface oxides to form Si-O species, it is reported that presence of Si at the interface, dramatically reduces the presence of Ga 3+ oxidation states. The transfer properties of InGaAs-based MOSFETs are also consistent with the CV results, showing a significant improvement as a result of Si insertion at the interface. On the other hand, introducing the Si interfacial layer, is at the cost of increasing the overall EOT of the gate stack. From the point of view of implementing high mobility channel materials, such as InGaAs, in future generation nodes, it is imperative to increase the C_{ox} (or reduce the EOT) of the gate stack and thus improve the gate controllability over the carriers in channel region [5.19]. Therefore, direct application of Si at the interface does

not offer a definitive solution for the InGaAs-based gate stacks. As stated in section 5.1.1, La_2O_3 has the property to intermix with Si, forming an amorphous layer in the form of La-silicate. La-silicate benefits from a high *k*-value with very promising results for gate stack scaling purposes. The k-value of La-silicate, is determined by the ratio of Si and La atoms in the final silicate composition [5.2]. Therefore, application of this material as a gate dielectric to InGaAs can help with scaling and thermal stability of InGaAs-based gate stacks, provided that the silicate/InGaAs interface is carefully controlled. In this section, methodology for fabricating highly scalable and thermally stable La-silicate layer as a gate dielectric for InGaAs-based devices as well as electrical characteristics of MOS capacitors has been investigated.

5.3.2 Experimental Procedure

The experimental methodology for fabricating La-silicate structure on InGaAs is similar to the previous sections. Substrates were cleaned by acetone/ethanol, followed by HF (20%) and $(NH_4)_2S$ treatment for oxide removal and sulfur passivation, respectively. Substrates were then loaded into an ultra-high vacuum chamber. Before the deposition of high-*k* film, first a thin layer of Si was deposited by RF- sputtering on

InGaAs substrates. The thickness of Si film was varied between 0.5 nm to 2 nm. Depending on the experiment, the temperature of the substrate was then raised to 300 ^{o}C, and a nitrogen radical beam gun was used to nitridize the Si layer. The power of nitrogen gun, the N_2 flow and the nitridation time were all optimized to achieve the best data possible. La_2O_3 films were *in-situ* deposited using e-beam evaporation followed by *in-situ* metal deposition by RF sputtering. A TiN (45 nm)/ W(5 nm) film structure was deposited to form the metal gate electrode for samples with Si incorporation, A W(50 nm) gate was used for samples without Si incorporation. The samples were post-metallization annealed in forming gas ambient (N_2:H_2 = 97%:3%) for 5 mins. Finally, Al was deposited on the back side of the InGaAs/InP substrate to form the back contact. Figure 5.19 shows the experimental flow used for fabricating the samples.

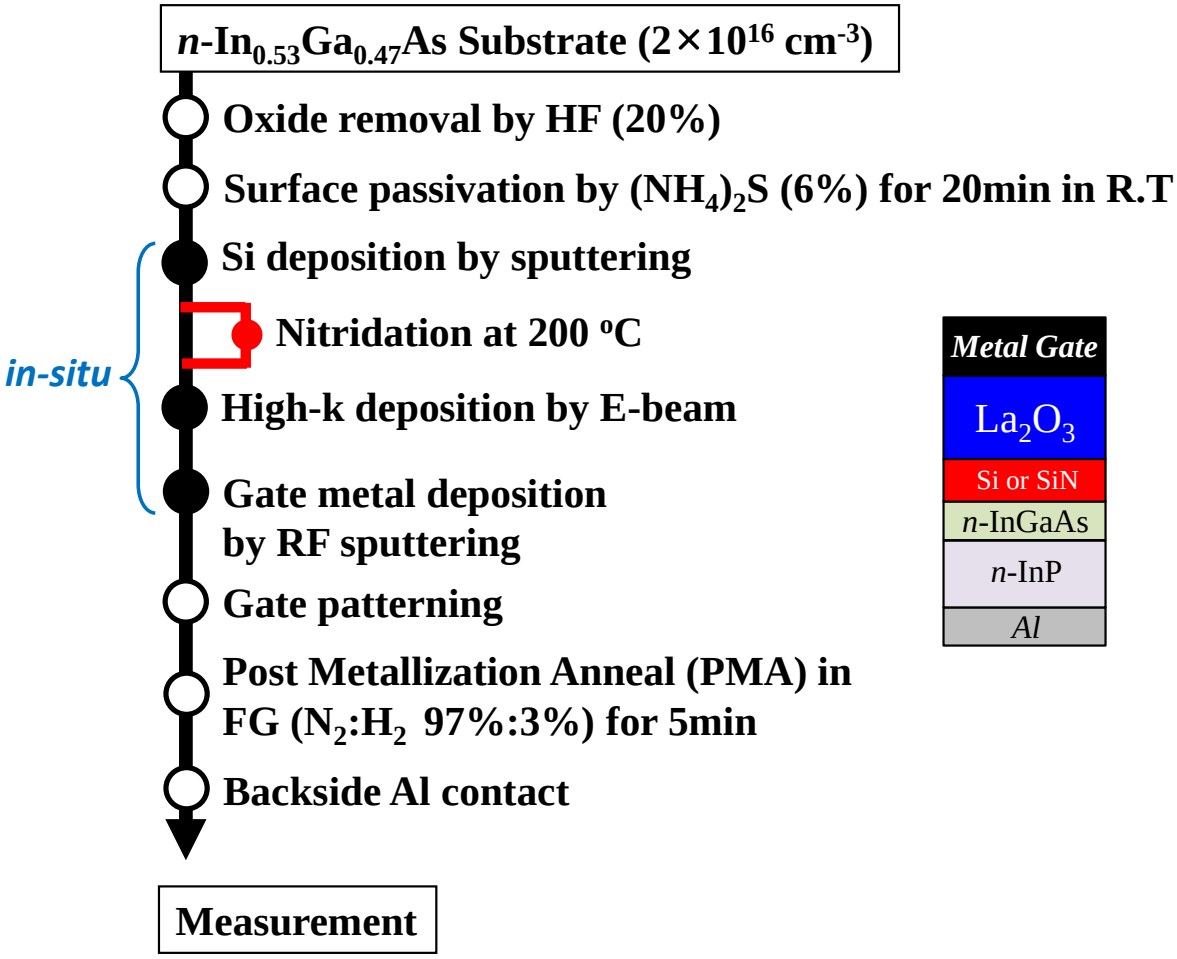


Figure 5.19 Experimental procedure flow for MOS capacitor fabrication process

5.3.3 Effect of Nitridated-Si on Silicate Structure

As stated in the previous section, La_2O_3 can readily react with Si and form a silicate structure. However, the composition of silicate structure affects its *k*-value [5.2]. A La-rich possess a higher *k*-value whereas a Si-rich silicate structure has a lower *k*-value. In order to investigate the quality of silicate layer and its *k*-value on InGaAs substrate,

thickness of the deposited Si was varied from 0.5 nm to 2 nm and the Capacitance Equivalent Oxide (CET) of the capacitors was compared at various annealing temperatures. The nitridation condition is the same for all the samples and is described in section 5.3.2. The results are summarized in Figure 5.20.

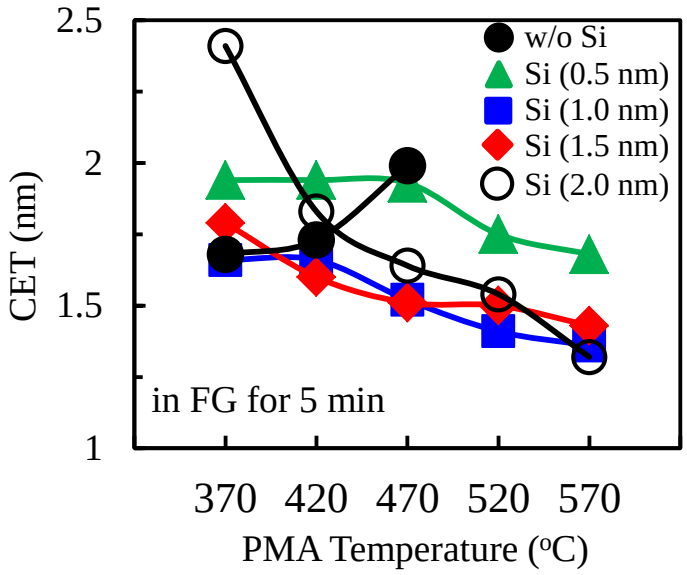


Figure 5.20 CET dependence of MOS capacitors on initial Si layer thickness

It is seen that if the Si thickness is more than 0.5 nm, the difference of CET between the capacitors is negligible, especially at higher annealing temperatures. This is in contrast to the capacitor with no Si layer, where a sudden increase in CET occurs at annealing temperature over 420 ^{o}C. Therefore, it can be assumed that *k*-value of the silicate structure is roughly the same if the Si incorporation is more than 1 nm. Higher

k-value is obviously more desirable since it would allow for further scaling of the gate stack. The effect of nitridated Si layer (LaSiON) is contrasted to non-nitridated (LaSiO) Si layer in Figure 5.21.

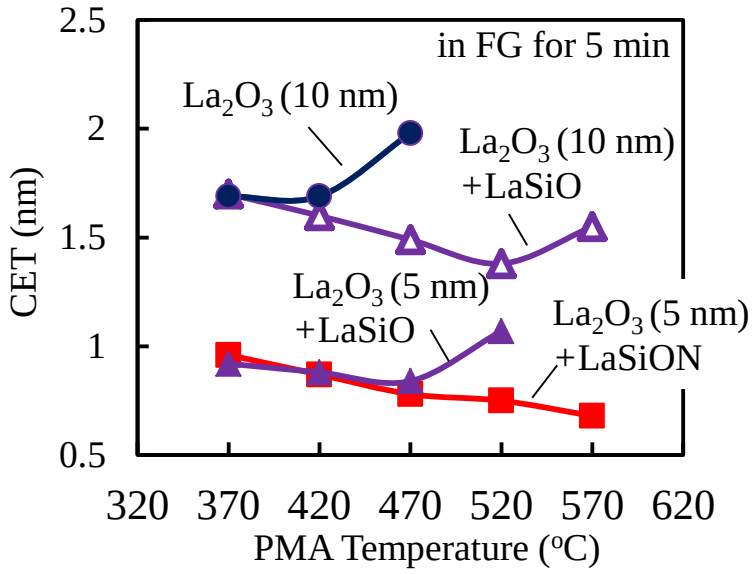


Figure 5.21 Effect of initial Si layer nitridation on CET of MOS capacitors

It is evident that nitridation of Si layer, before depositing La_2O_3, increase the thermal stability of the gate dielectric. The difference becomes more noticeable as the thickness of La_2O_3 is scaled. At La_2O_3= 5 nm , the increase in CET (or lowering of *k*-value) is suppressed by least 100 ^oC. Furthermore, The CET of MOS capacitor with La_2O_3= 5 nm+LaSiON is around 0.7 nm at PMA 570 ^oC, which is one of the lowest reported values in literature [5.20]. Including the quantum effect, the equivalent oxide thickness

(EOT) of the device, is expected to be around 0.4 nm. These results point to the fact that Nitridation of Si layer, to form a silicate structure is more suitable for scaling purpose.

Cross-sectional TEM image of the MOS capacitor with La_2O_3= 5 nm+ Nitridated- Si (1 nm) after annealing in 520 ^oC for 5 min is shown in Figure 5.22.

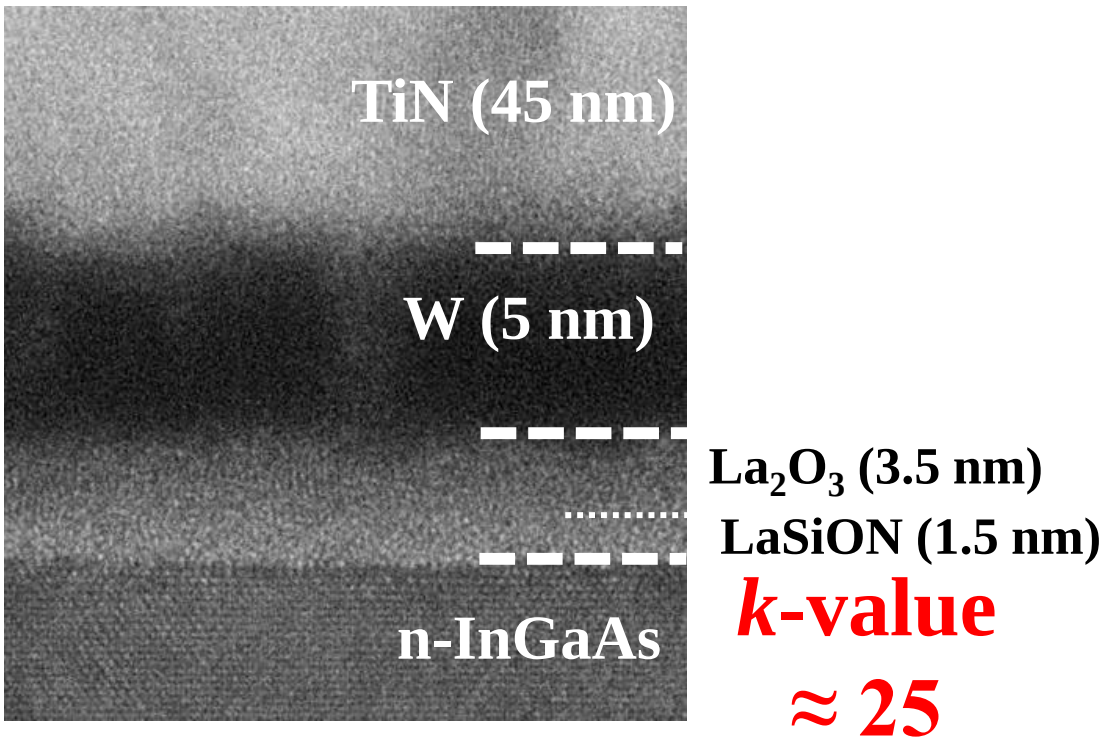


Figure 5.22 Cross-sectional TEM image of La_2O_3 (5 nm)/ Nitridated Si (1 nm)/InGaAs after PMA in FG at 520 ^oC

Two distinct layers can be separated in the TEM image, a 1.5 nm layer close to the substrate and a 3.5 nm close to the metal gate electrode. The total thickness of gate

dielectric layer is reduced after annealing, compared to the deposited total thickness. This means that the inserted Nitridated-Si layer intermixes with the La_2O_3 layer. The total k-value of the dielectric layer is estimated to be 25, which is almost 3 times higher than Al_2O_3 (≈ 9). The schematic in Figure 5.23, illustrates the change that the gate dielectric undergoes upon annealing. The resultant dielectric layer has amorphous structure with no signs of crystallization in the TEM image.

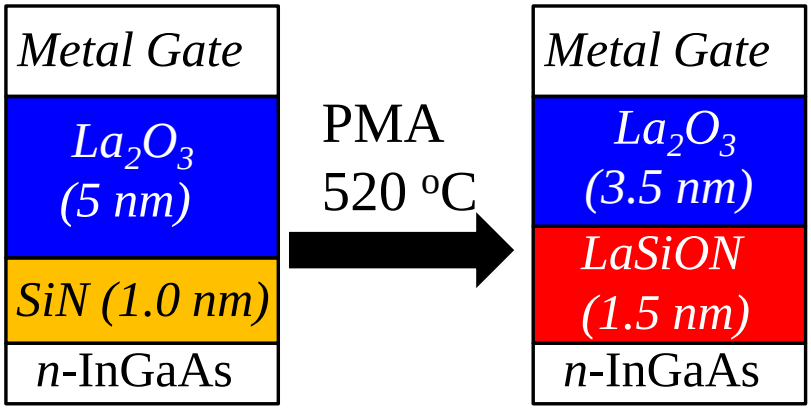


Figure 5.23 Schematic illustration of PMA effect on La_2O_3 / Nitridated Si/InGaAs

It was stated that the thickness of deposited layer, if more than 0.5 nm, does not affect the *k*-value of dielectric layer. However, the quality of interface must also be compared to achieve an optimized the device performance. Peak interface state density (D_{it}) of capacitors with various Si thicknesses, are measured by conductance method and are compared in Figure 5.24.

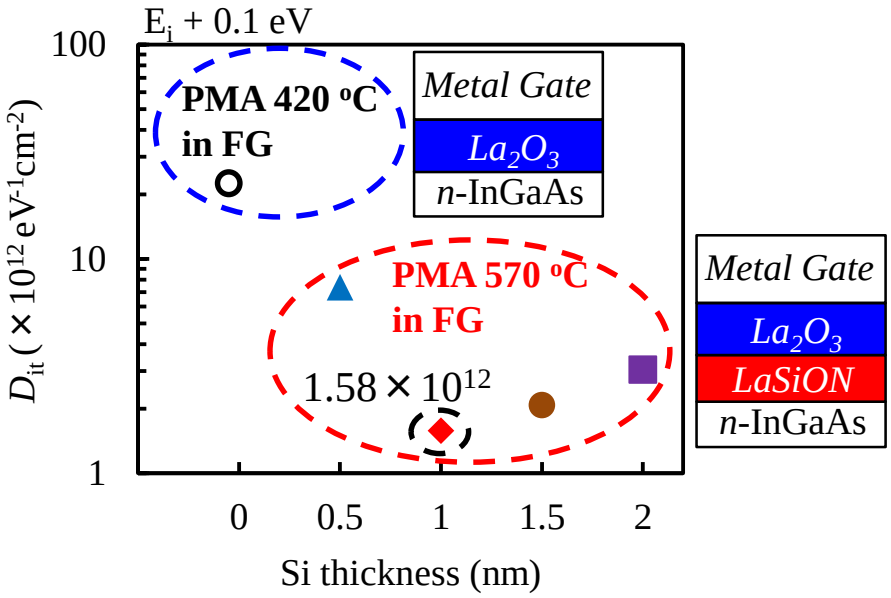


Figure 5.24 Initial Si layer thickness effect on peak D_{it} value of LaSiON/InGaAs interface

The lowest value is obtained for the sample with initial Si thickness of 1 nm indicating a better interface quality. Thus by controlling the composition of LaSiON layer through initial Si thickness, and nitridation condition, both improving the *k*-value and interface quality targets can be met.

Figure 5.25 shows the effect of reducing initial La_2O_3 thickness on Capacitance-Voltage (*CV*) characteristics of the MOS capacitors at a measurement frequency of 100 kHz. The thickness of the nitridated Si is constant at 1nm and the PMA temperature is 520 ^{o}C.

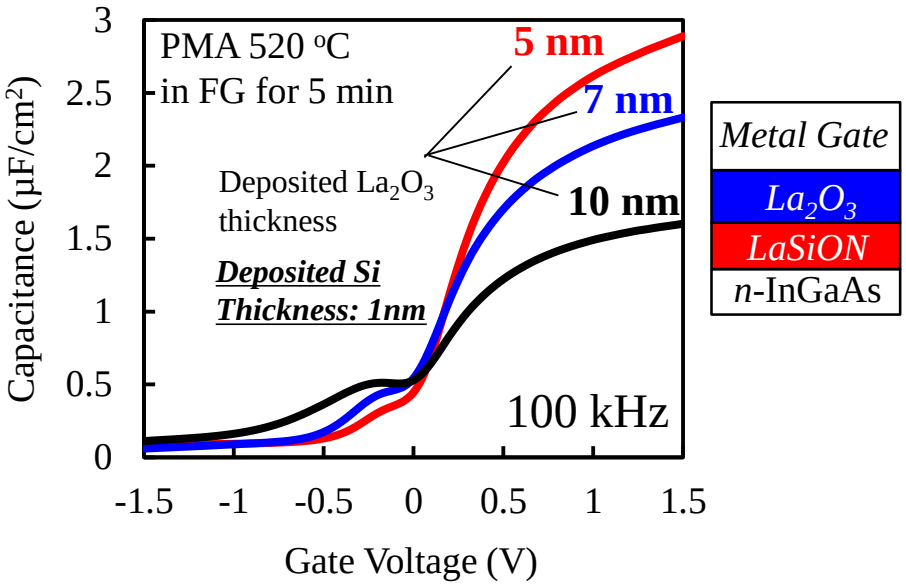


Figure 5.25 CV characteristics of W/La_2O_3/LaSiON/InGaAs gate stack with various La_2O_3 thicknesses

The linear increase in capacitance value for smaller La_2O_3 thickness, points to the uniformity of LaSiON layer and to its potential for scalability.

The dependence of La_2O_3/LaSiON stack on deposited La_2O_3 thickness and annealing temperature is shown in Figure 5.26. Higher annealing temperature leads to lower CET regardless of the deposited La_2O_3 thickness. Changes in the composition of LaSiON layer or crystallization of La_2O_3 layer which might occur at high annealing temperatures could be contributing factors for these results. Although no signs of crystallization were observed at an annealing temperature of up to 520 ^oC from the TEM image. Unlike La_2O_3, La-silicate structure does not crystalize in high annealing temperature.

Controlling silicate structure on Si-substrate is easier compared to InGaAs-substrate since on Si-substrate, Sian be readily be supplied from the substrate. However, on an InGaAs substrate providing enough Si for forming La-rich silicate which is immune to crystallization effect in high temperature is challenging and needs more physical analysis of the dielectric layer.

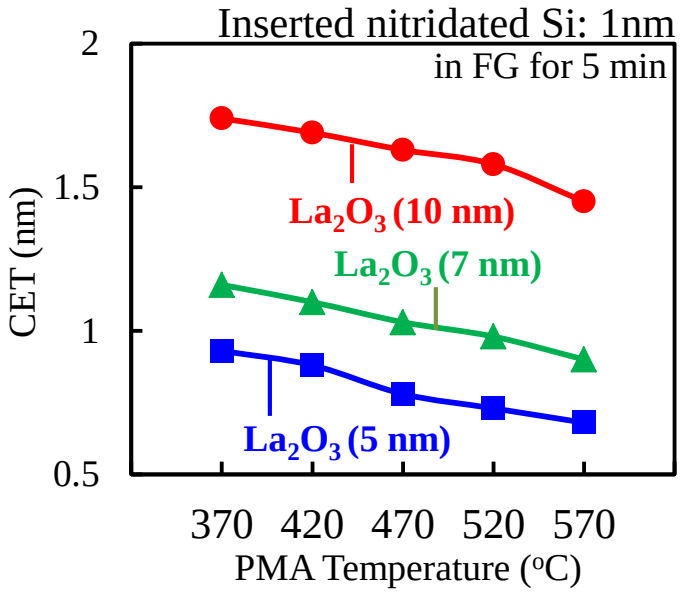


Figure 5.26 CET dependence of W/La_2O_3/LaSiON/InGaAs gate stack on PMA temperature with various La_2O_3 thicknesses

A closer view on the effect of PMA temperature on *CV* characteristic of devices at a measurement frequency of 100 kHz is shown in Figure 5.27. A clear increase in the

capacitance value of the MOS capacitors without any degradation in the *CV* curves is visible.

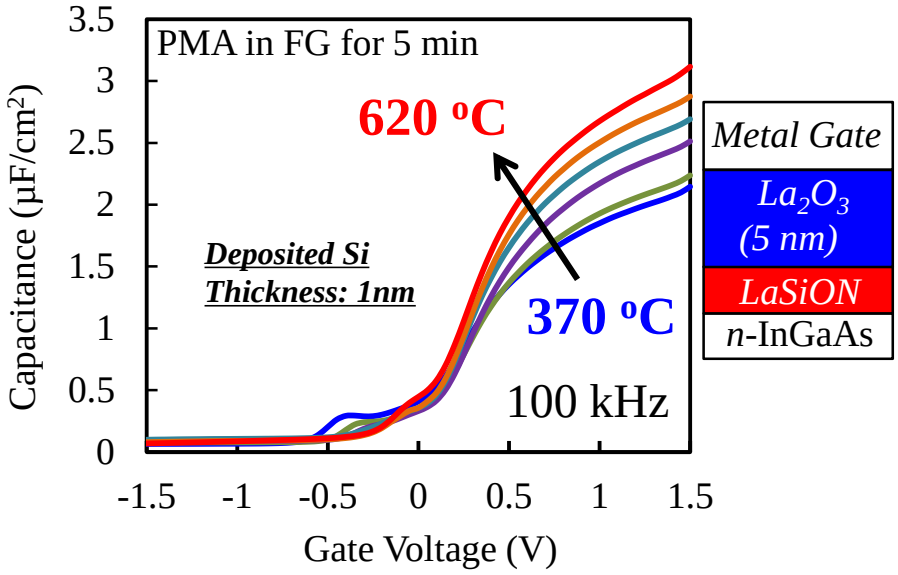


Figure 5.27 PMA temperature effect on CET of TiN/W/La_2O_3 (5 nm)/LaSiON/InGaAs gate stack

For successful scaling, it is important not only to increase the maximum capacitance, but only to decrease the gate leakage current. The effect of annealing temperature on gate leakage current of La_2O_3 (5 nm)/ Nitridated Si (1 nm) samples is shown in Figure 5.28 (a) and (b). The leakage behavior in accumulation condition is shown in Figure 5.28 (a) and the leakage current value at a gate bias voltage of V_{FB} + 0.5 V is shown in Figure Figure 5.28 (b).

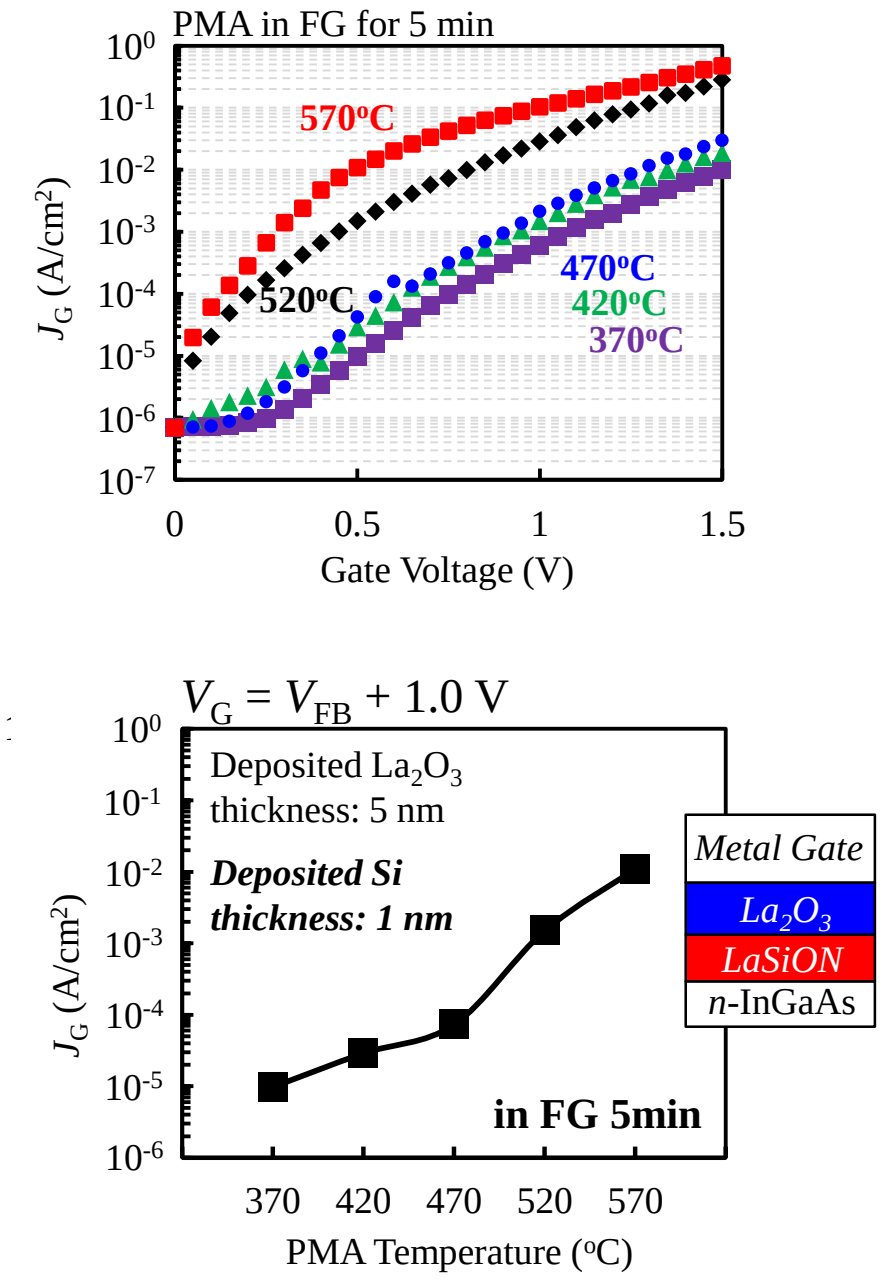


Figure 5.28 PMA temperature effect on gate leakage current of of TiN/W/La_2O_3 (5 nm)/LaSiON/InGaAs gate stack

The increase in leakage current as the annealing temperature increases is not unexpected. Formation of oxygen vacancies, diffusion of elements from the substrate and gate metal might all contribute to the increase in gate leakage current. However a comparison between these experimental results and some of the most up-to-date available data for leakage current at scaled gate stacks (Figure 5.29) shows the superiority of La_2O_3/LaSiON stack at suppressing gate leakage current.

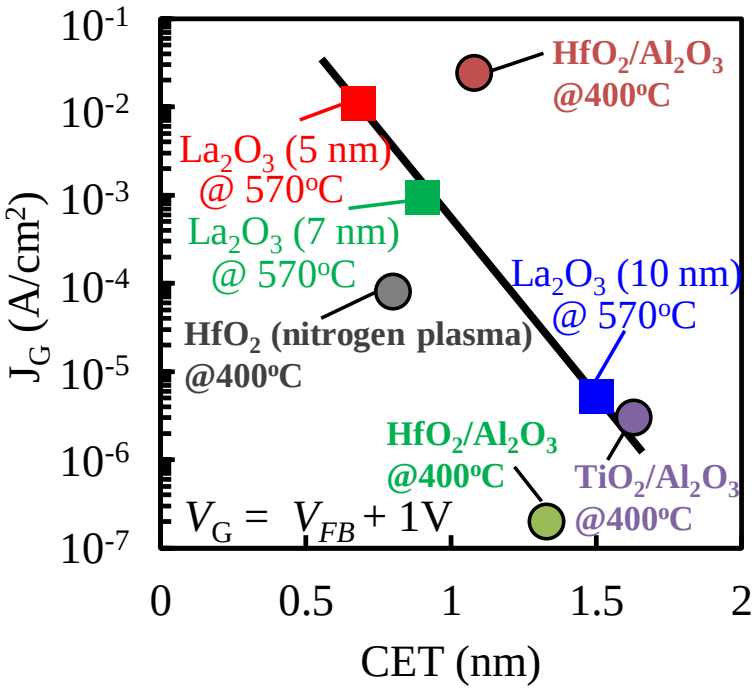


Figure 5.29 Gate leakage current comparison of La_2O_3/LaSiON/InGaAs

The effect of PMA temperature on interface quality of LaSiON/InGaAs interface can be easily judged by comparing the Capacitance-Voltage (*CV*) response of the samples in various annealing temperatures. Figure 5.30 focuses on the *CV* characteristics of the LaSiON/InGaAs structure in the depletion condition. The effect of high density of interface states would manifest as high depletion capacitance and failure to fit the ideal *CV* profile.

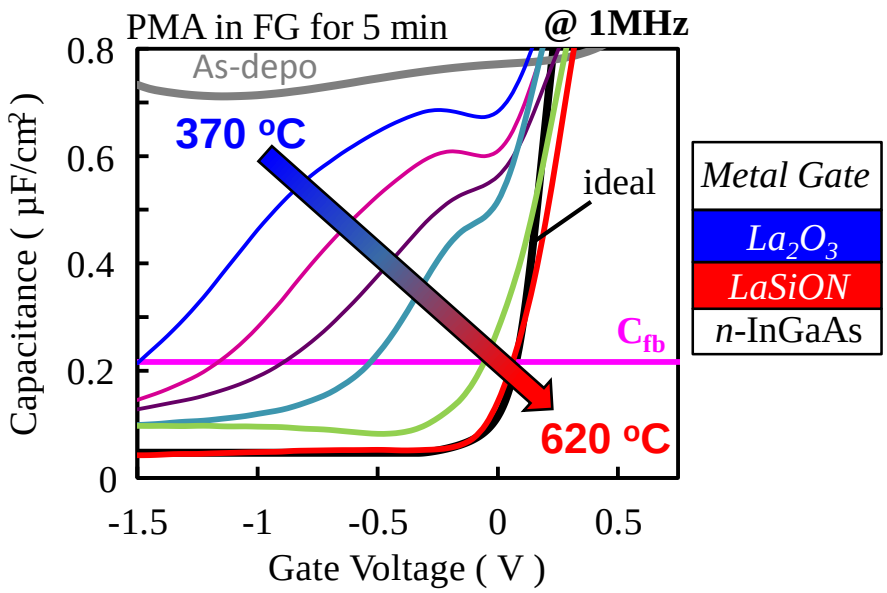


Figure 5.30 PMA temperature effect on depletion capacitance of 1 MHz *CV* curves of La_2O_3/LaSiON/InGaAs

It is clear from Figure 5.30, as the PMA temperature increases, the *CV* response of the device, gets closer to the ideal *CV* curve. At 620 ^{o}C, a very close fitting to the ideal

CV profile is possible.

The effect of scaling La_2O_3 thickness on interface state density of metal/ La_2O_3/LaSiON/InGaAs gate stacks is evaluated for annealing temperature range of 370 ^oC to 620 ^oC and shown in Figure 5.31. Almost identical D_{it} values is obtained for La_2O_3= 5nm and 10nm pointing to an excellent scalability potential. Although 620 ^oC annealing temperature results in the minimum D_{it} value, the effect of leakage current must also be considered for scaled devices. For precise admittance characterization, the leakage current should be kept lower than ~1 A/cm^2, otherwise the error in measured capacitance and conductance cannot be neglected. Several methods for evaluating very-leaky, highly scaled gate stacks for Si-based devices has been proposed, however it is best to keep the leakage current low for accurate admittance evaluation. The effect of high gate leakage current, manifests as capacitance upturn in low measurement frequencies. Higher measurement frequencies (higher than 100 kHz) are not as much affected by leakage current unless the leakage current is extremely high (above 10~100 A/cm^2).

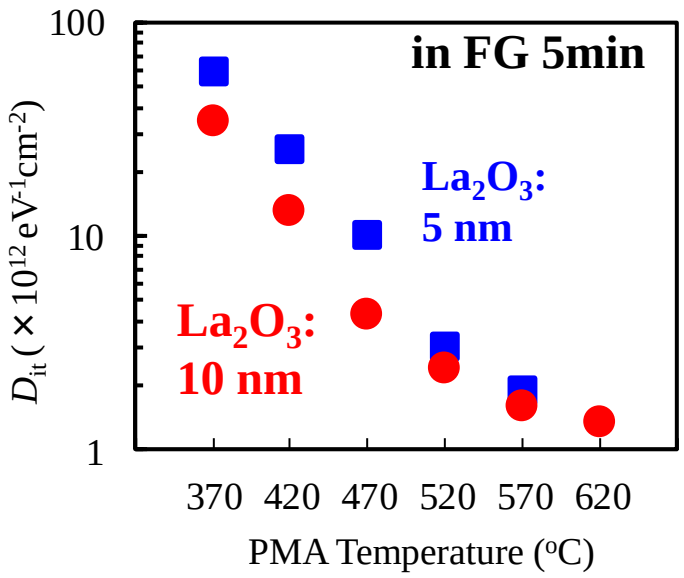


Figure 5.31 PMA temperature effect on interface state density (*D*it) of La_2O_3/LaSiON/InGaAs

The Capacitance-Voltage (*CV*) characteristics of the La_2O_3 (3.5nm)/LaSiON (1.5 nm)/InGaAs gate structure at PMA 520 °C , corresponding to the TEM image in Figure 5.22, is shown in Figure 5.32. Well behaved *CV* response with CET= 0.73 nm is obtained. As previously mentioned, factoring in the quantum effect, the EOT of this gate stack would be below 0.5 nm. Although the leakage current causes slight capacitance upturn in measurement frequencies lower than 10 kHz, it should be reiterated that CET of these samples are extracted from fitting the 100 kHz, which is not affected by the leakage current.

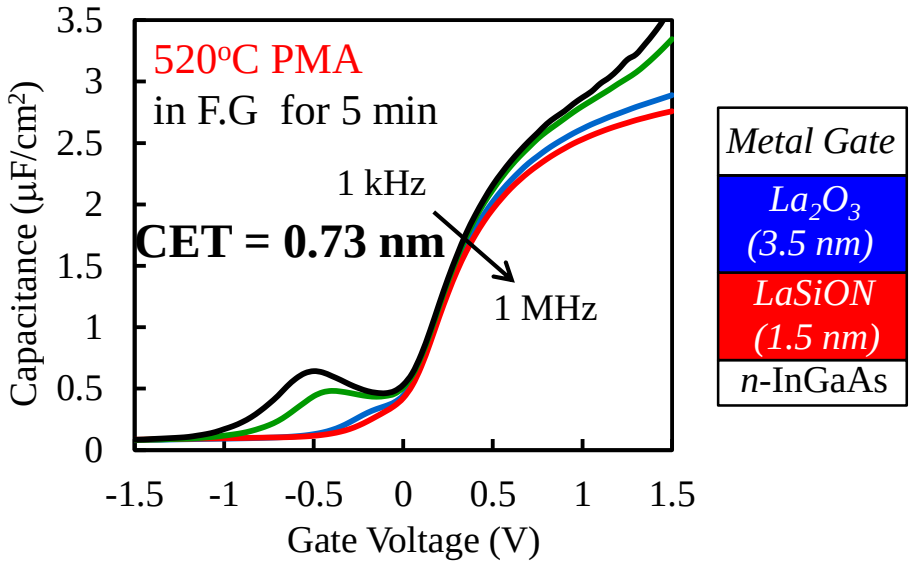


Figure 5.32 *CV* characteristics of TiN/W/La_2O_3/LaSiON/InGaAs gate stack after FG PMA at 520 ^{o}C for 5min.

5.3.4 Conclusions

Thermally robust gate stack with CET as low as 0.7 nm at 620 ^{o}C was achieved by forming La-silicate structure on InGaAs. Incorporation of nitridation step to the initial Si layer could add to the stability and interface quality of La-silicate/InGaAs gate stack. Composition of the silicate can be modified by amount of incorporated N and Si. LaSiON could be promising dielectric with high *k*-value for ultra-scaled gate stacks.

5.4 Impact of Gate Metal Selection on La_2O_3/InGaAs Interface

5.4.1 Introduction

As it was stated in previous chapters, one of the paramount challenges that InGaAs-based devices have continuously faced, is to find a suitable gate dielectric to achieve a high quality oxide/InGaAs interface with low interface state density (D_{it}). Achieving low interface state of density is of outmost importance since the standby power dissipation and lifetime of a device is directly related to the amount of interface state density. The dielectric used for InGaAs should also have a dielectric constant (*k*-value) high enough to allow for capacitance equivalent thickness (CET) scaling with suppression of gate leakage current. Although, various gate oxides (high-k) have been examined on InGaAs substrates, similar electrical characteristics are persistently and most commonly observed regardless of the employed high-*k* oxide; high D_{it} values at or close to conduction band, capacitance frequency dispersion at accumulation and up-turn of capacitance in inversion region [5.21, 5.22]. Most of these undesirable effects are considered to originate from unstable native/thermal oxides, particularly Ga and As oxides, which are formed prior to or during high-*k* deposition at high-*k*/InGaAs

interfaces. A number of passivation techniques including sulfur passivation [5.11], As layer capping followed by desorption technique [5.18], hydrogen-based plasma passivation [5.21], are used to suppress the formation of unstable oxides. However, reported D_{it} values are still above 10^{12} cm^{-2}/eV.

Among high-*k* oxides, HfO_2 and Al_2O_3 have attracted great attention as gate dielectric materials for InGaAs substrates. HfO_2 having a higher dielectric constant (k~22) than Al_2O_3 (k~9) is preferable since it would allow further capacitance equivalent thickness (CET) scaling. However, as the interface quality of HfO_2/InGaAs is worse than Al_2O_3/InGaAs, it is difficult to apply HfO_2 directly on InGaAs substrates for device performance, therefore a thin layer of Al_2O_3 is commonly inserted underneath the HfO_2 layer to overcome the interface issue [5.22]. The reasons for better Al_2O_3/InGaAs interface quality are reported to arise from the fact that Al_2O_3 to a large extent prevents the formation of InGaAs sub-oxides with low temperature thermal annealing process. Thus one of the Al_2O_3 issues is that the thermal processing window of Al_2O_3/InGaAs interfaces remains below 400 ^oC due to degradation in interface properties at higher temperatures.

On the other hand, it was shown in previous chapters that La_2O_3 can be a promising high-*k* material for CET scaling. In section 5.1 it was stated that La_2O_3 can react with

InGaAs substrates and form an intermixed interface layer . It was also mentioned that excess growth of the layer results in the increase of CET. The thickness of intermixed interface layer is dependent on the oxygen partial pressure during the annealing step, and TiN capping on the metal electrode is reported to be effective to suppress the diffusion of oxygen atoms into the gate dielectric [5.3].

In this section, the effect of gate metal selection on the changes it induces on La_2O_3/InGaAs interface after post-metallization annealing (PMA) is investigated by examining both physical and electrical properties of MOS capacitors. It is demonstrated that by controlling the reaction at La_2O_3/InGaAs interface through the choice of gate metal, superior capacitance-voltage (*CV*) characteristics with low D_{it} and leakage current, stable up to 620 ^{o}C can be obtained.

5.4.2 Experimental Procedure

For this study, 500 nm thick *n*-type $In_{0.53}Ga_{0.47}As$ (100) substrates epitaxially grown on *n*-type InP substrates with S doping concentration of 1×10^{16} cm^{-3} were used to fabricate MOS capacitors. After substrate cleaning described in chapter 3, samples were transferred to a multi ultra-high vacuum chamber for gate dielectric and metal

deposition. A 10 nm La_2O_3 layer was deposited by e-beam evaporation in room temperature at a deposition rate of 0.2 nm/min in 10^{-6} Pa. Two sets of capacitors were fabricated with W (50 nm) gate or TiN/W (45 nm/ 5 nm) gate by *in situ* RF magnetron sputtering. The TiN layer was reactively deposited using a Ti target with a mixed gas of Ar and N_2. Gate electrodes were patterned using an inductively coupled plasma reactive ion etching (ICP-RIE) system at a Cl_2:Ar concentration of 30:10 sccm. PMA was conducted in FG as has been the case throughout this thesis. Figure 5.33 shows the schematic cross-sectional view of both capacitor structures. For x-ray photoelectron spectra (XPS) measurements, samples were fabricated in the same way except for the change in thickness of metal gate, from 50 to 13 nm, and patterning steps. Hard x-ray (7.94 keV photons) excited photoelectron spectra arising from As $2p_{3/2}$, Ga $2p_{3/2}$, and In $3d_{5/2}$ core levels of the samples were measured at photoelectron take-off angle (TOA) of 80^o with energy resolution of 100 meV at beam line (BL46XU) using high resolution electron energy analyzer R-4000. For XPS measurements, the gate metal thickness was reduced to W:13 nm and TiN/W: 10 nm/3 nm to enable probing interface reaction.

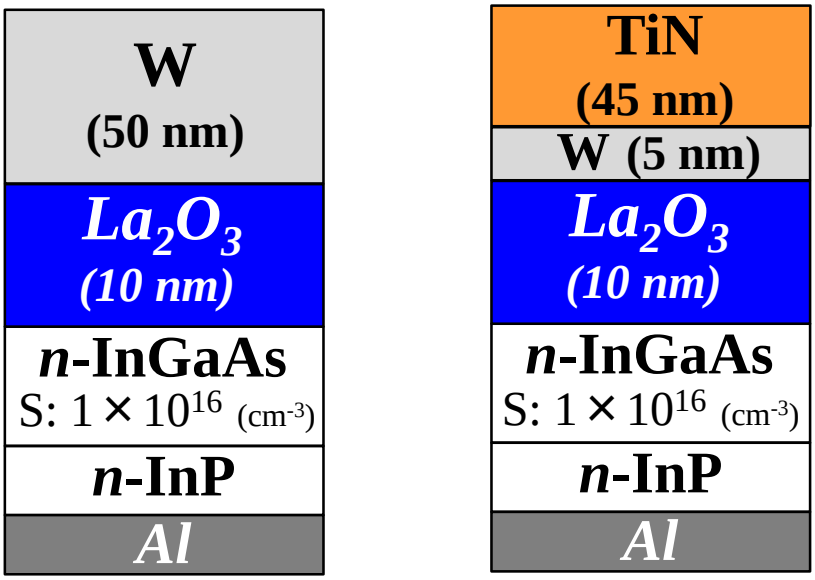


Figure 5.33 Schematic of the fabricated MOS capacitors

5.4.3 Oxygen Supply Control Through Gate Metal Selection

Cross-sectional TEM image of sample with TiN/W gate is shown in Figure 5.34.

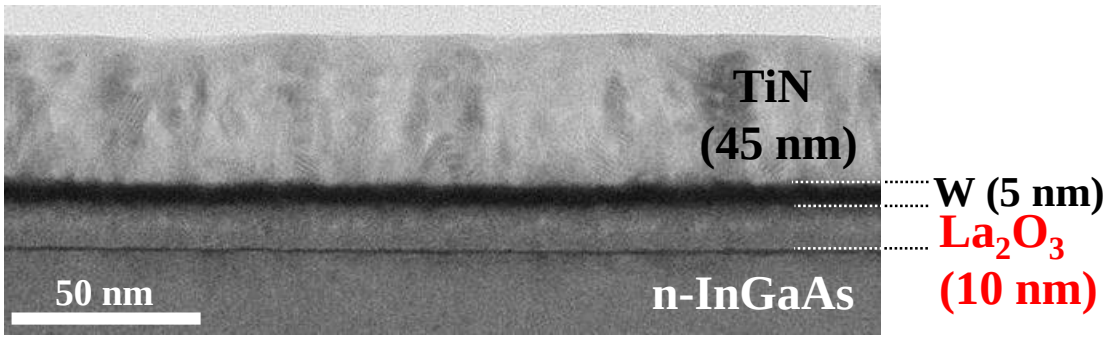


Figure 5.34 Cross-sectional TEM image of TiN(45 nm)/W(5 nm)/La_2O_3 (10 nm)/$In_{0.53}Ga_{0.47}As$ capacitor after FG PMA in 420 ^oC.

A sharp La_2O_3/InGaAs interface can be observed with no void-like defects as was seen for HfO_2/InGaAs interface in chapter 4. EDX measurements of 4 points within the gate stack were carried out. Points 1~3 inside the gate dielectric and for comparison point 4 at the bulk of InGaAs (Figures 5.35 (a)). A Summary of atomic ratio for In, Ga, As, La and O_2 at these 4 points are shown in Figures 5.35 (b) and (c). No trace of elements from the substrate, were detected at points 1 and 2 which are away from the interface.

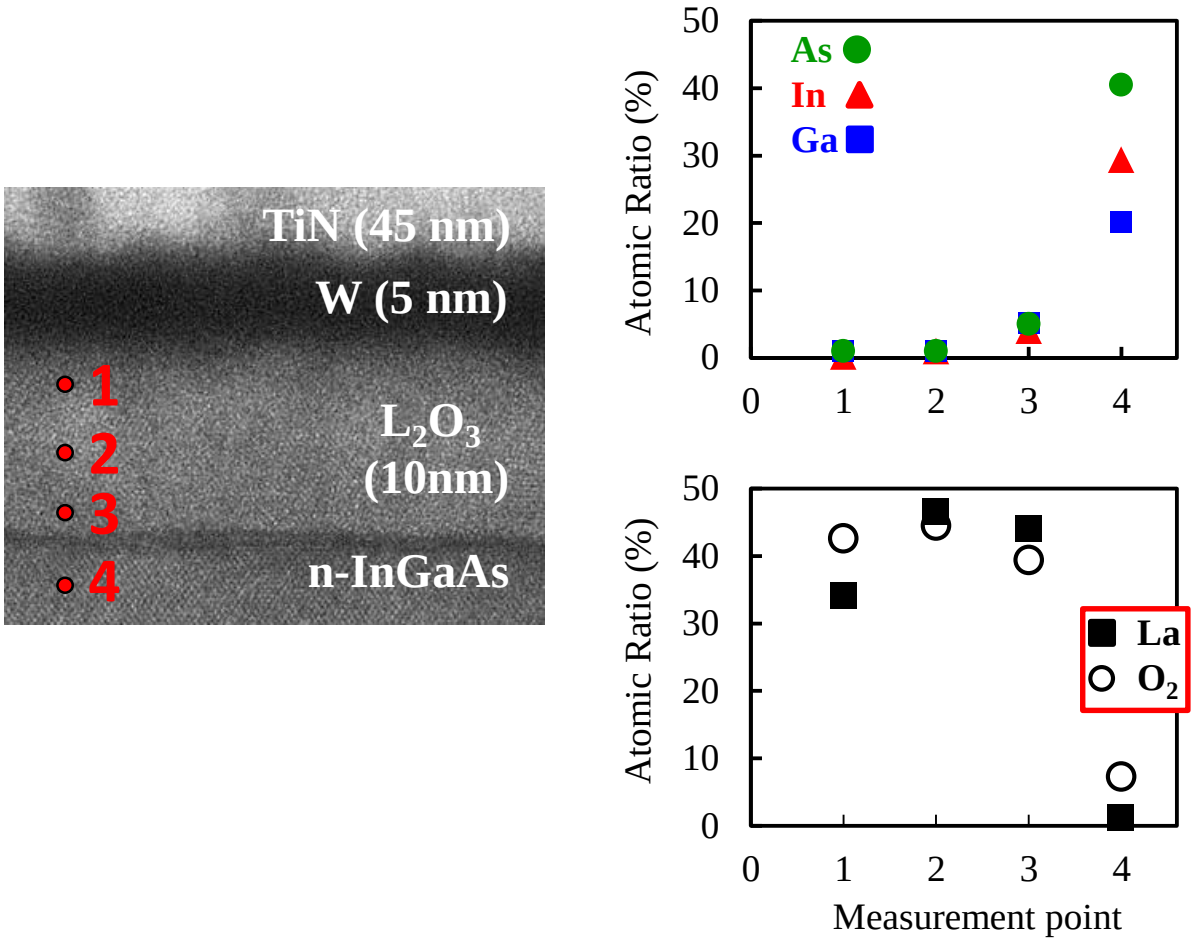


Figure 5.35 Cross-sectional TEM image of TiN(45 nm)/W(5 nm)/La_2O_3 (10 nm)/$In_{0.53}Ga_{0.47}As$ capacitor after FG PMA in 420 ^{o}C. with point-EDX analysis of the stack.

However, slight amount of In, Ga and As is seen at interfacial point 3. This is in agreement with the hypothesis from section 5.1 which predicts the intermixing of La_2O_3 and InGaAs and forming $LaInGaO_x$ layer. Interestingly the atomic ratio of La and O_2 is relatively the same within the gate dielectric which points to a high quality oxide composition.

Comparing the detected levels of In, Ga and As atomic ratio, at an interfacial point (within the La_2O_3 layer) it becomes evident that a larger amount of mixing La_2O_3 and InGaAs mixing occurs for W (50 nm) gate compare to TiN (45nm)/W (5 nm) gate. Figure 5.36 shows an almost 50% decrease in the amount of detected elements from InGaAs substrate.

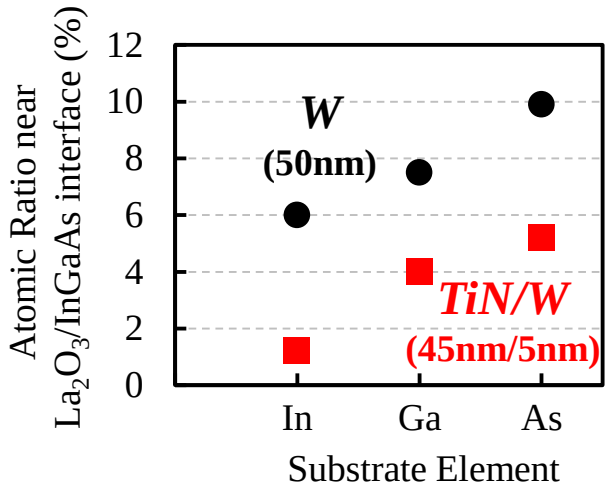


Figure 5.36 Comparison of atomic ratio of substrate elements at La_2O_3 (10 nm)/$In_{0.53}Ga_{0.47}As$ interface (dielectric side) with W and TiN/W gate

To evaluate the physical changes that occur in MOS interface by applying different metal gates, XPS study on the La_2O_3/InGaAs interface with and without metal gate was performed after annealing the samples in FG at 420 ^{o}C. Figure 5.37 shows the As $2p_{3/2}$,

Ga $2p_{3/2}$ and In $3d_{5/2}$ photoelectron spectra for (a) La_2O_3 (1.5 nm)/InGaAs structure and La_2O_3 (10 nm)/InGaAs MOS capacitors with (b) W (13 nm) and (c) TiN (10nm)/W (3 nm) metal gate.

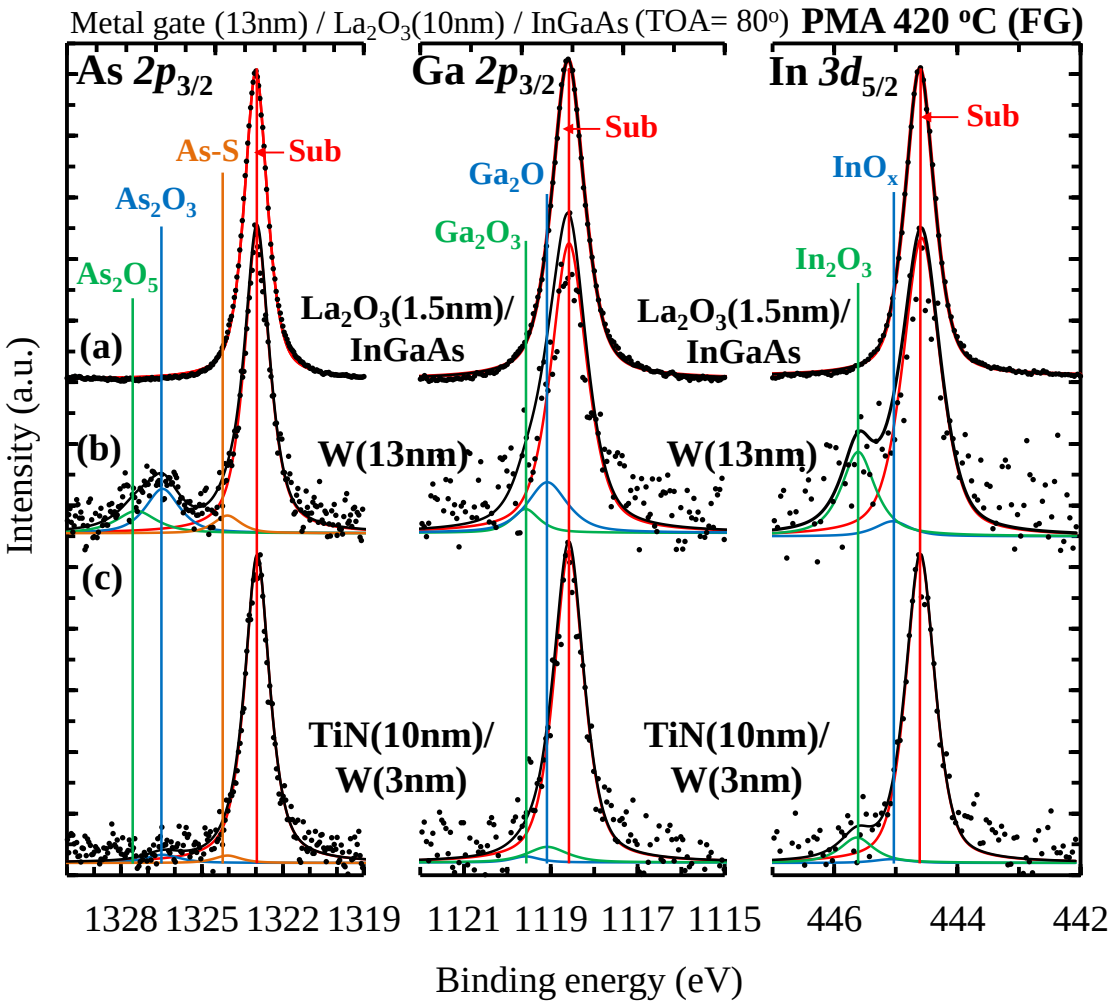


Figure 5.37 As $2p_{3/2}$, Ga $2p_{3/2}$ and In $3d_{5/2}$ HAXPS spectra for (a) La_2O_3 (1.5 nm)/$In_{0.53}Ga_{0.47}As$ (b) W(13 nm)/ La_2O_3 (10 nm)/$In_{0.53}Ga_{0.47}As$ and (c) TiN (10nm)/W(3 nm)/ La_2O_3 (10 nm)/$In_{0.53}Ga_{0.47}As$ MOS capacitors after annealing in FG at 420 °C.

It can be noticed in the spectra of row (a) that a solitary post-deposition anneal (PDA), does not result in the formation of In, Ga or As oxides. However, the spectra undergo a notable change for a PMA process. The W-gated sample, shown in row (b), reveals clear oxidation peaks for all three substrate elements especially for those of As^{3+} (~3.3eV chemically shifted from the substrate peak) and In^{3+} (~1.05eV chemically shifted from the substrate peak) suggesting diffusion of oxygen atoms through the W gate metal. Formation of these oxide states however, is significantly suppressed when W gate metal is replaced by TiN/W as is shown in row (c).

The ratio of In^{3+}, Ga^{1+} and As^{3+} states peak intensity to un-oxidized substrate peaks are shown in Figure. 5.38 By changing the gate material from W to TiN/W, both In^{3+} and Ga^{1+} peak intensities have reduced by 65%, whereas As^{3+} peak intensity is lowered by 82%.

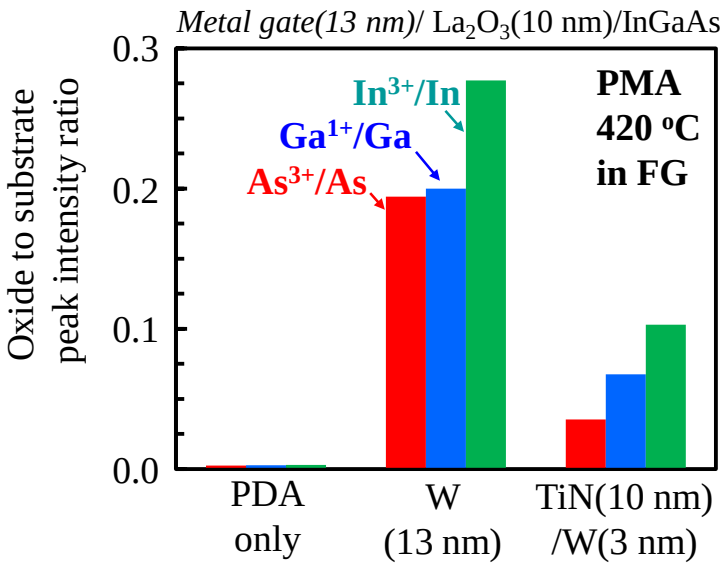


Figure 5.38 Measured intensity ratio of oxides for three samples.

This large decrease in As^{3+} peak intensity could be due to suppression of As out-diffusion into the gate stack of TiN/W-gated sample [5.23]. As the Gibbs free energies predict, the oxygen could be converted to more stable Ga and In states in the system.

The formation of $LaInGaO_x$ interfacial layer as a result of La_2O_3 intermixing with InGaAs substrate as was described in section 5.1, can be explained by the model shown in Figure 5.39. Gate metal acts as an oxygen supply mechanism, which triggers the reaction at La_2O_3/InGaAs interface. The composition and thickness of the $LaInGaO_x$ can be controlled by the choice of gate metal. Since W metal contains a significant amount of Oxygen atoms, reducing W thickness and capping it with TiN, decreases the

diffusion of Oxygen from the gate metal.

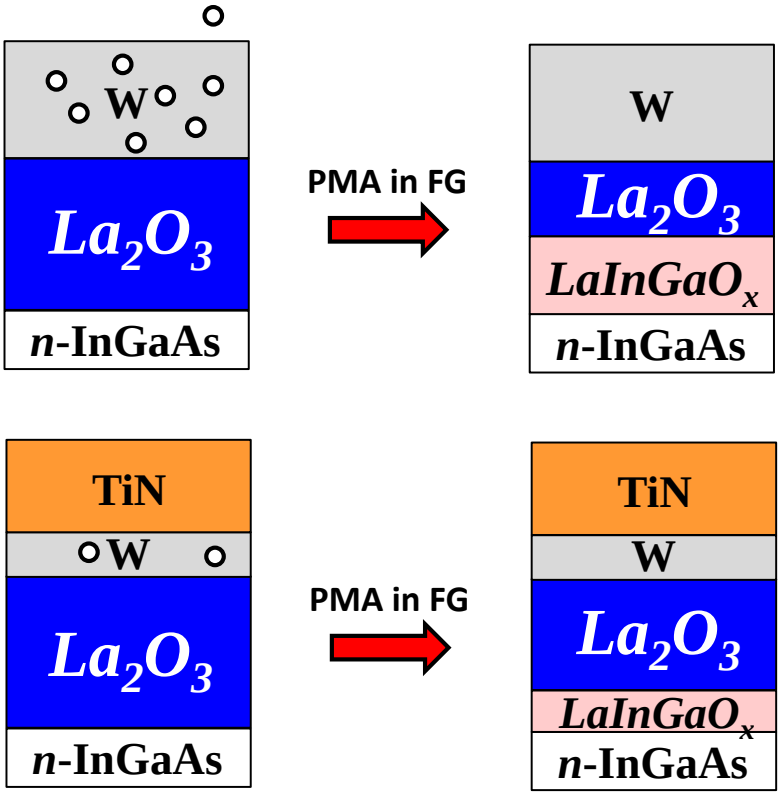


Figure 5.39 Schematic illustrating the effect of W gate electrode on thickness of the interfacial layer at La_2O_3 (10 nm)/$In_{0.53}Ga_{0.47}As$ interface

Figures 5.40 (a) and (b) show the room temperature *CV* characteristics of La_2O_3 (10nm)/InGaAs capacitors with W and TiN/W gate electrodes, respectively. Both capacitors are annealed in forming gas at 370 ^{o}C for 5min.

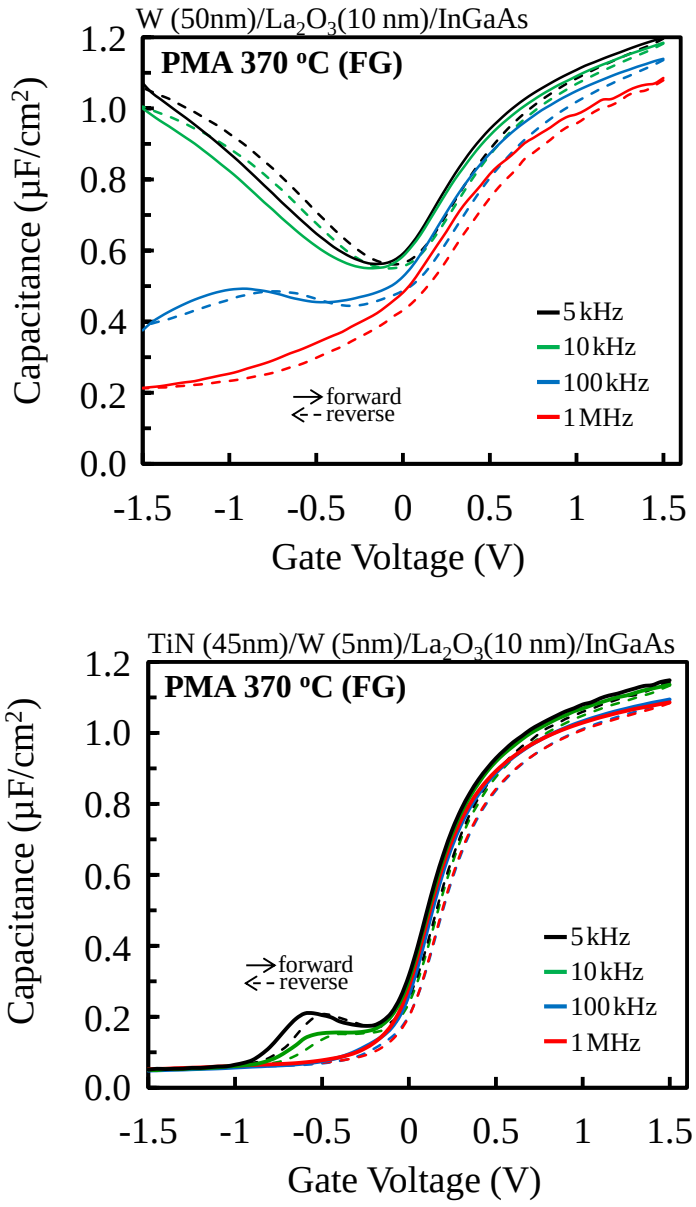


Figure 5.40 *CV* characteristics of La_2O_3 (10 nm)/$In_{0.53}Ga_{0.47}As$ capacitors with (a) W gate and (b) TiN/W gate. Samples are annealed in forming gas (N_2:H_2= 97:3%) at 370 ^oC for 5 min.

A very different capacitance response is obtained between the two MOS capacitors. The TiN/W-gated sample shows a superior *CV* response with significant reduction in

stretch-out and frequency dispersion in the entire voltage sweep range. Moreover, the capacitance bumps in inversion region even at low frequencies are resolved compared with W-gated sample. The dependence of capacitance on frequency and gate voltage in strong inversion region for W-gated capacitor, is indicative of high mid-gap interface state density [5.24]. This is because the surface potential (ψ_s) is not able to effectively sweep the InGaAs band gap due to the presence of interface states, therefore the inversion layer cannot be formed and the depletion capacitance is affected by the gate voltage.

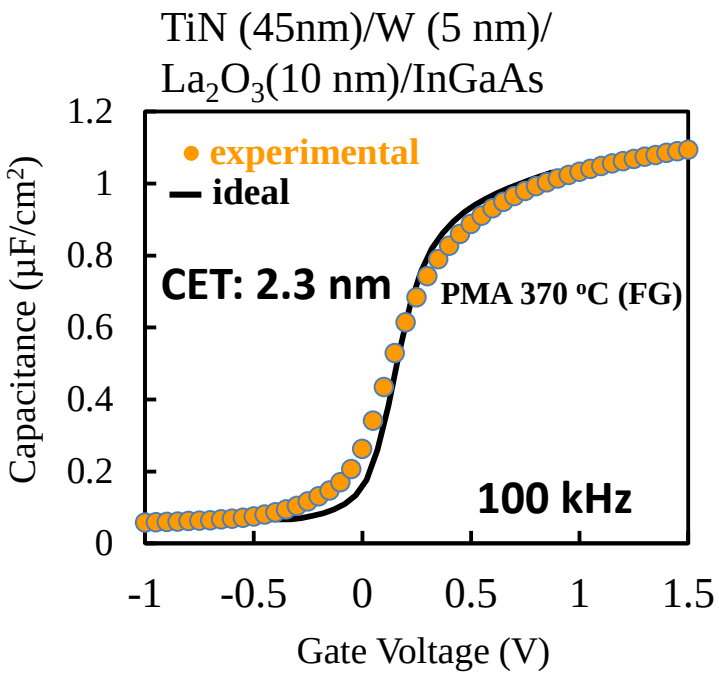


Figure 5.41 100 kHz *CV* curves of TiN/W/La_2O_3 (10 nm)/$In_{0.53}Ga_{0.47}As$ capacitors against ideal *CV* curve

The *CV* response of the sample with TiN/W gate at a measurement frequency of 100 kHz is contrasted to the ideal *CV* curve in Figure 5.41. Experimental and ideal depletion capacitances are matched and a very small stretch out in the *CV* is observed.

The gate voltage dependent capacitance behavior is particularly apparent for W-gated capacitors without any annealing (as-deposited) as is shown in Figure 5.42 (a). Increasing the annealing temperature, results in a smaller bump in 100 kHz *CV* curves, accompanied by a reduction in the maximum accumulation capacitance. However at annealing temperature over 470 ^{o}C, accurate *CV* measurement is not possible due to increase in gate leakage current.

Figure 5.42 (b) shows the effect of annealing on 100 kHz *CV* curves of TiN/W-gated samples. In this case the annealing temperature is elevated from 370 to 620 ^{o}C in 50 ^{o}C steps. The clear stretch-out observed in as-deposited *CV* response is mostly eliminated by performing annealing; furthermore in contrast to W-gated capacitors the decrease in accumulation capacitance is effectively suppressed even by annealing up to 620 ^{o}C.

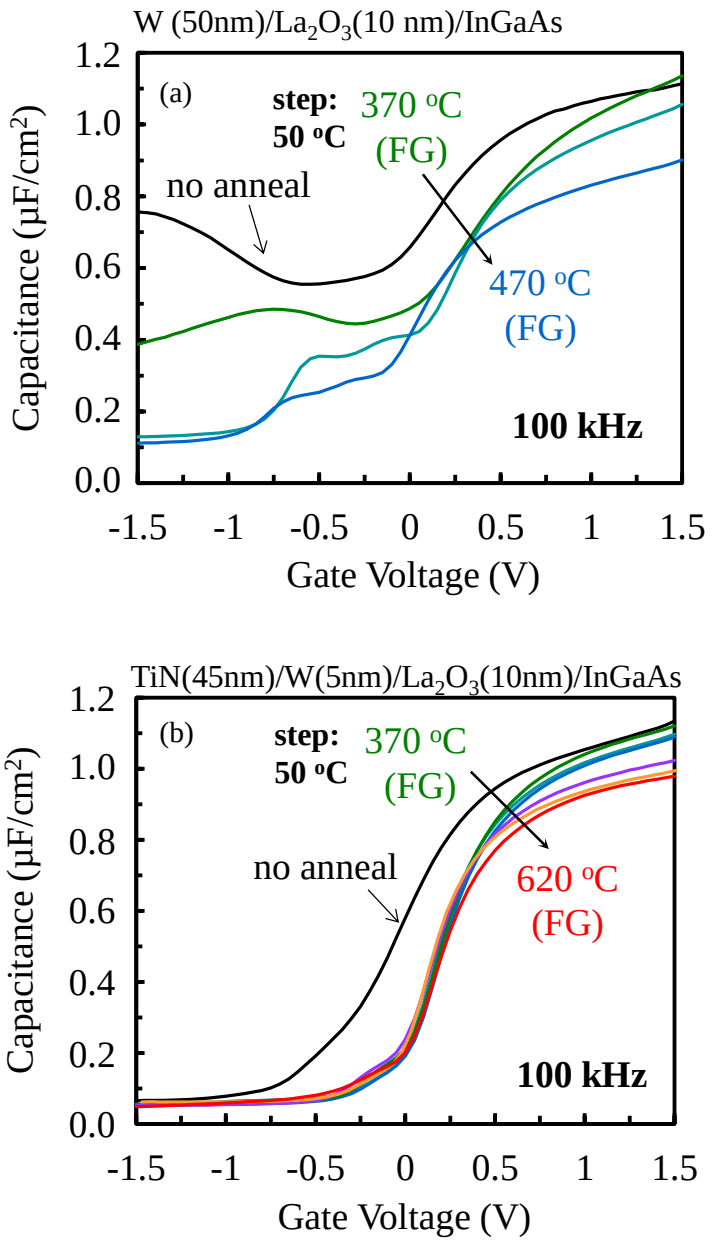


Figure 5.42 Effect of increasing PMA temperature on 100 kHz *CV* curves of (a) W gate and (b) TiN/W gate in La_2O_3 (10 nm)/$In_{0.53}Ga_{0.47}As$ capacitors. PMA temperature is increased from 370 °C in 50 °C steps.

Figure 5.43 (a) shows the capacitance tolerance of the W-gated and TiN/W gated

samples by comparing their CET against the annealing temperature. Since different oxide states response to ac signal, can increase the measured capacitance at low frequencies [5.25], CET is estimated from fitting 100 kHz curves to the ideal *CV* curve, without considering the quantum effect. A 36% rise in CET of W-gated capacitors is observed when annealing temperature is increased from 370 to 470 ^{o}C, while that value is lowered to 25% for TiN/W-gated capacitors at a much wider annealing temperature range of 370 to 620 ^{o}C.

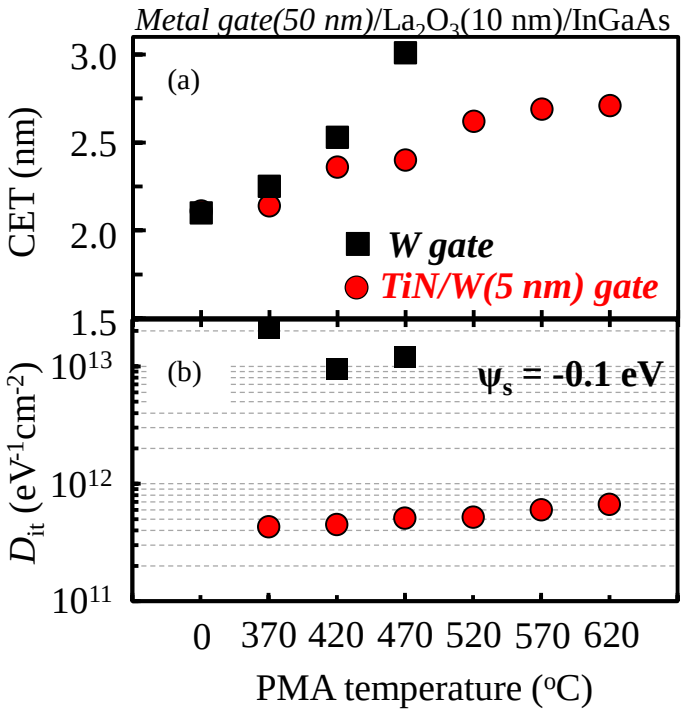


Figure 5.43 Effect of increasing PMA temperature on (a) CET and (b) D_{it} of La_2O_3 (10 nm)/$In_{0.53}Ga_{0.47}As$ capacitors with W or TiN/W gate metal.

The D_{it} for MOS interfaces was evaluated by the conductance method including the effects of surface potential fluctuation. Figure 5.43 (b) compares the D_{it} of both samples at a ψ_s of -0.1 eV (0.25 eV below the conduction band). The ψ_s value is chosen to probe mid gap states while minimizing the contribution from weak inversion response in $In_{0.53}Ga_{0.47}As$. TiN/W-gated capacitor has a minimum D_{it} of 4.6×10^{11} $eV^{-1}cm^{-2}$, and increases only slightly as the annealing temperature is increased from 370 ^{o}C to 620 ^{o}C. The D_{it} value for W-gated capacitor on the other hand, exceeds 10^{13} $eV^{-1}cm^{-2}$ at an annealing temperature of 370 ^{o}C. The lowest D_{it} for W-gated sample is obtained at 420 ^{o}C with a value of $\sim9.2\times10^{12}$ $eV^{-1}cm^{-2}$, still over an order of magnitude higher than TiN/W-gated capacitor. The As and Ga oxidation states are known to be volatile and result in interface states on the upper half of the InGaAs band gap by creating Ga dangling bonds and As anti-bonding states [5.26, 5.27], which is also in agreement with the XPS results previously presented in this study. Hence, the amount of IL formed at La_2O_3/InGaAs should be controlled to optimize the interface quality and reduce maximum capacitance loss at the same time. The significant improvement in *CV* characteristics of TiN/W-gated capacitor and its tolerance to higher annealing temperature could be related to oxygen blocking effect of TiN layer. As a result, the diffusion of oxygen atoms from annealing ambient and/or metal gate itself into the

La_2O_3 gate dielectric is suppressed (shown in Figure 5.39). Consequently, the development of excessive IL and oxidation states are suppressed. The composition of intermixed interface layer might be the critical factor for improving both D_{it} and CET.

Figure 5.44 (a) and (b) summarize the leakage current behavior of the two samples at various annealing temperatures. Although both samples have the same leakage current at the as-deposited state due to equal initial physical thickness of La_2O_3 (10 nm), the difference becomes more apparent as the annealing temperature increases. At 470 ^oC, the gate leakage current at W-gated capacitor already reaches the limits that would allow for accurate *CV* measurement, while the capacitor with TiN/W gate structure shows a more robust behavior. For comparison, the leakage current density at a gate voltage of V_{flatband} +1 V is shown in Figure 5.44 (b) for both samples. The small increase in leakage current of TiN/W-gated samples at an annealing temperature window of 250 ^oC (from 370 to 620 ^oC) points to the stable quality of La_2O_3/InGaAs interface.

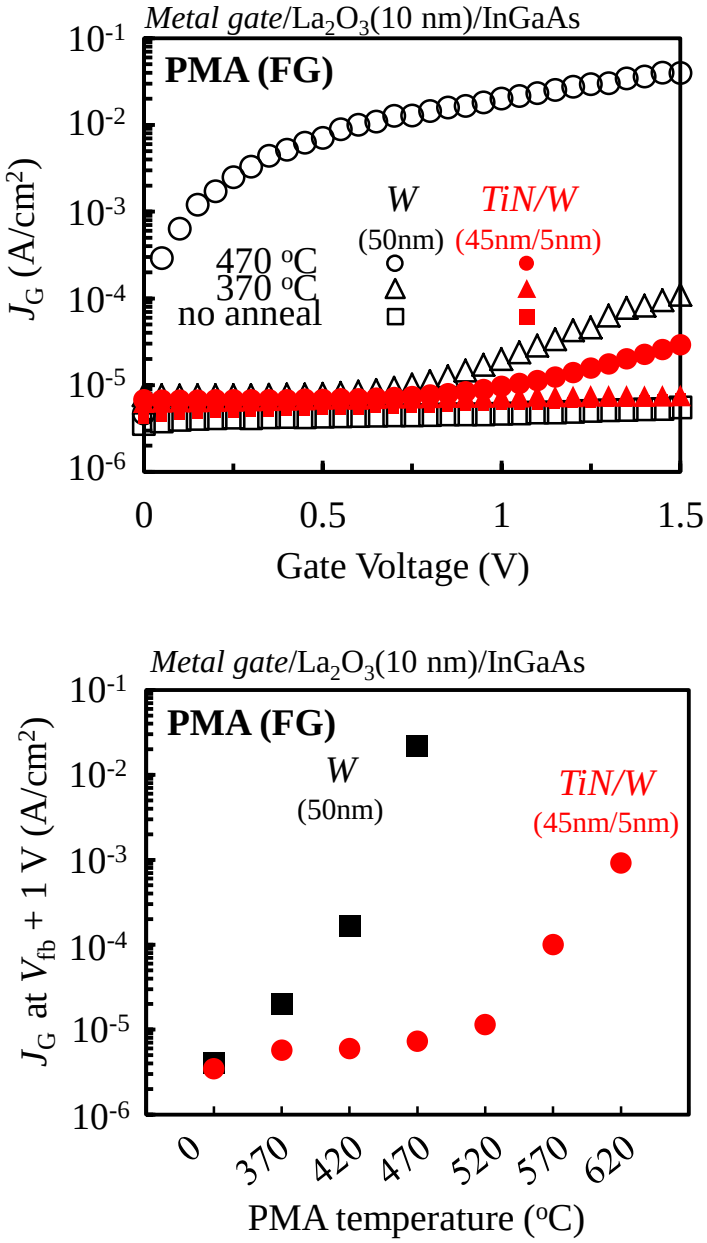


Figure 5.44 (a) Gate leakage current of La_2O_3 (10 nm)/$In_{0.53}Ga_{0.47}As$ with W (50nm) or TiN (45nm)/W (5nm) gate electrode at two annealing temperatures. (b) Effect of PMA temperature on gate leakage current at the gate voltage of V_{fb}+ 1 V.

These results demonstrate the reaction at the La_2O_3/InGaAs interface, triggered by oxygen diffusion from the gate metal with PMA, has a major impact on the integrity of La_2O_3/InGaAs MOS capacitors. The thermal stability of CET, leakage current and low D_{it} of TiN/W/La_2O_3/InGaAs gate stacks, promise scalability potential for La_2O_3-based oxides on InGaAs through the choice of appropriate gate metal.

5.4.4 Conclusions

The effect of gate metal on La_2O_3/InGaAs interface after PMA was studied by HXPS measurement and electrical characterization of MOS capacitors with W and TiN/W as gate electrode. Well behaved *CV* characteristics with low D_{it} and leakage current at annealing range from 370 to 620 ^{o}C were obtained by using TiN/W gate electrode. The improved MOS capacitor performance could be attributed to the reduction of oxygen diffusion through the gate dielectric, leading to a controlled IL formation at La_2O_3/InGaAs interface.

5.5 Conclusions

The fundamental properties of La_2O_3/InGaAs interface were investigated. It was found that La_2O_3 can intermix with InGaAs and create LaInGaO interfacial layer. The composition and thickness of this IL is a determinant factor for the electrical properties of La_2O_3/InGaAs gate stacks. Three approaches were taken in order to control and/or manipulate the interfacial reaction. Self-assembled Si monolayer passivation by vapor HMDS treatment of the InGaAs substrate prior to La_2O_3 deposition could reduce the interface state density without increasing CET of the gate stack. La-silicate structure was successfully implemented to obtain high quality, thermally stable gate stacks with CET as low as 0.73 nm in 600 ^oC. It was shown that oxygen diffusion through the gate metal is the trigger for formation of IL LaInGaO, thus the IL composition can be controlled through the gate metal selection. By TiN capping of W/La_2O_3/InGaAs gate stack low D_{it} value of 6×10^{11} $eV^{-1}cm^{-2}$ was obtained.

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Chapter 6

Technologies for 3D structure InGaAs-based Devices

Chapter 6 Technologies for 3D structure InGaAs-based Devices

6.1 Overview of 3D Device Structures

In 2007, the first commercially available transistor with high-*k* gate dielectric was announced by Intel. The Hf-based dielectric films used for the 45-nm node MOSFETS, instead of being grown by an oxidation process, which was the case for SiO_2, were deposited using atomic layer deposition (ALD). At the same time, new device structures based on 3D designs are attracting more attention since they allow for the scaling trend to follow Moore's law for several more device generations. In 2011, Intel for the first time implemented a 3D structured, 32-nm node transistor in their new microprocessors [6.1]. Intel refers to this transistor as Tri-Gate, although in the literature it is referred to as Fin-FET. This non-planar transistor structure consists of a Si arc around wrapped around by gate dielectric layer and the gate electrode. The evolution of transistors in a microchip from planar structure to 3D structure is illustrated in Figure 6.1. The 3D scaling approach facilitates the miniaturization of the footprint of the transistor while keeping the gate surface area approximately constant. This transition to 3D structure is inevitable since the high-*k*/metal gate stack with even low EOT cannot

control the source to drain leakage once the gate length is aggressively scaled and the source-drain extension regions approach each other. FinFET on the other hand, by design, are fully depleted so that the entire available silicon underneath the gate electrode is depleted of carriers before the threshold condition is reached [6.2]. These features significantly improve sub-threshold slope (standby power) and short channel effects of the device.

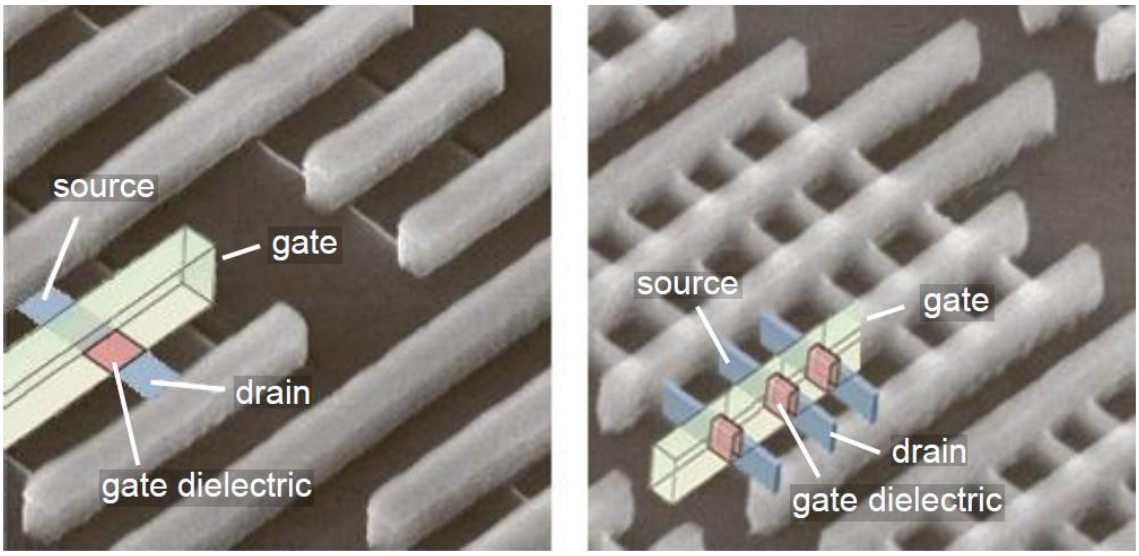

Figure 6.1 Evolution of MOSFET from planar (left) in 32 nm node to FinFET structure (right) in 22 nm node [6.1].

In order to fabricate 3D transistors, not only should the gate dielectric have high quality, but also the growth control during deposition at different directions

(conformality) should be precise and the deposition should be uniform across the complete wafer. These are all requirements that can be fulfilled by ALD. The quest for faster, more power efficient devices will make integrating 3D structures to III-V channel material, inevitable as well. In fact Intel has already announced both Fin-FET and Quantum well FET(QWFET) structures on InGaAs platforms [6.3]. (Figure 6.2).

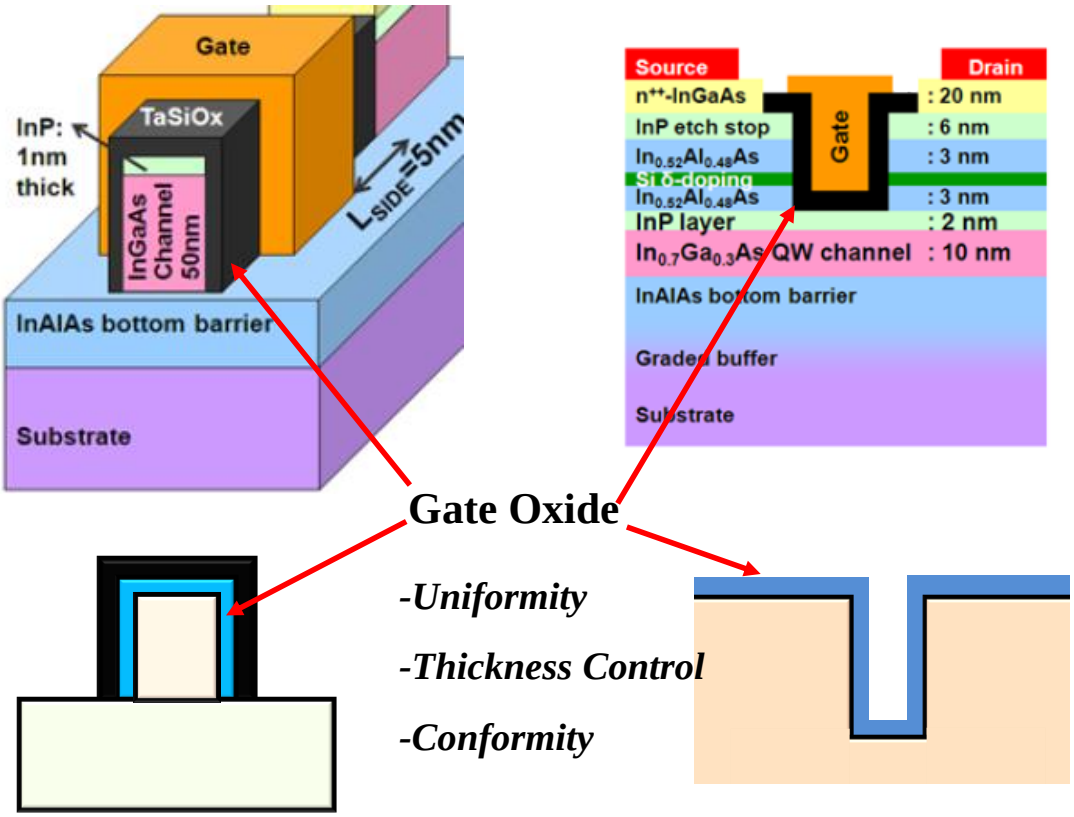

Figure 6.2 FinFET and quantum-well structure devices on InGaAs requiring ALD-deposited oxide for precise and uniform thickness at all angles and surfaces [6.3].

In this chapter, gate dielectric and source.drain fabrication techniques which would be of interest in 3D InGaAs-based devices, are discussed.

6.2 Atomic Layer Deposition (ALD) of La_2O_3

6.2.1 Introduction

ALD is a vapor-phase deposition technique in which (ultra-)thin films can be deposited sub-monolayer by sub-monolayer by repeating supply and purge cycles [6.4]. In the first part of the cycle, a precursor (typically a vapor carrying the main element of the film material) is supplied which reacts with the elements on the starting surface. The precursor is not reactive with the surface formed by its own elements, and consequently the surface reactions stop occurring when all surface groups have reacted (known as self-limiting reaction). Then, a pump and/or purge step is executed with an inert gas (typically Ar) during which the volatile reaction by-products are removed from the reactor along with the excess of precursor. In the second half of the cycle, the surface is exposed to a co-reactant (typically a gas, such as O_2 or NH_3, or a vapor such as H_2O) which reacts with the surface which is now covered with the elements from the

precursor, again in a self-limiting manner. After a pump and/or purge step to remove the reaction by-products and the excess of co-reactant from the reactor, one ALD cycle is completed and the surface groups are equal to those with which the cycle started.

During ALD, the surface reactions typically occur by elevating the substrate temperatures to 150 ~ 350 ^{o}C). In this thesis, La(^{i}PrCp)$_3$ is used as the metal source and H_2O as the co-reactant (oxidant) gas to synthesize La_2O_3 films. Figure 6.3 illustrates the deposition cycle for synthesizing La_2O_3 films.

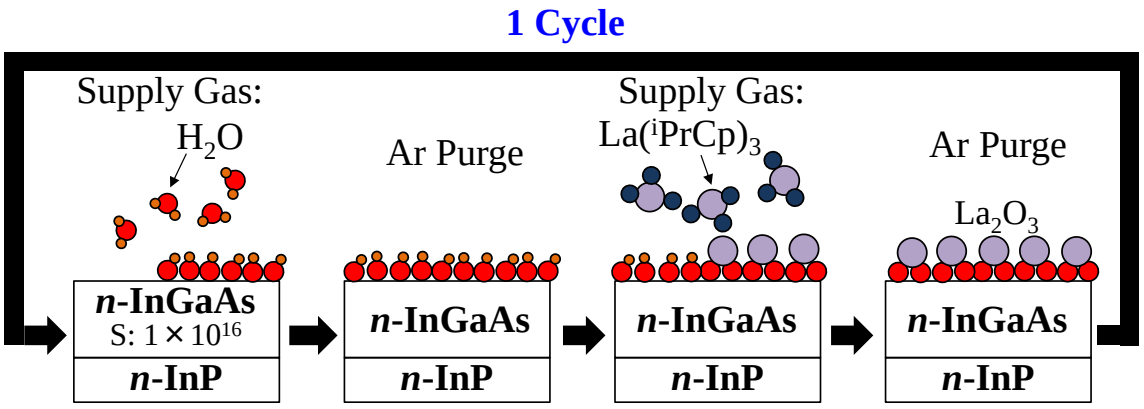

Figure 6.3 Schematic of 1-full cycle of ALD process for La_2O_3 deposition

6.2.2 Experimental Procedure

After initial surface treatment, the substrates were loaded to ALD chamber for La_2O_3 films synthesis, followed by *in-situ* metal deposition by RF sputtering. A TiN (45 nm)/W (5 nm) metal gate was used as the gate electrode. The samples were post-metallization annealed in forming gas ambient (N_2:H_2 = 97%:3%) for 5 mins. Finally, Al was deposited on the back side of the InGaAs/InP substrate to form the back contact. The gas feed times and exhaust times were investigated for optimal electrical performance of the capacitors. The growth conditions and schematic of the MOS capacitor structure are shown in Figure 6.4 (a) and (b) respectively.

(a)

	$La(^iPrCp)_3$	H_2O	Ar
Supply time (sec.)	5	5	10
Exhaust time (sec.)	20	50	30

(b)

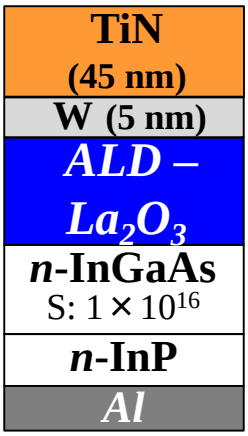

Figure 6.4 (a) Optimized and modified supply and exhaust time table for ALD-La_2O_3 deposition, (b) Capacitor structure with ALD-La_2O_3 as gate dielectric

6.2.3 Experimental Results

The effect of substrate temperature during ALD cycles, on CET of the TiN/W/La_2O_3/InGaAs capacitors is shown in Figure 6.5. Controlling the substrate temperature below 180 ^oC results in relatively similar values of CET, increasing the growth temperature to 180 ^oC and over on the other hand, shows a sudden increase in the CET. This could be due to changing the deposition mode to chemical vapor deposition (CVD), which results in larger deposition thickness and subsequently a larger CET value.

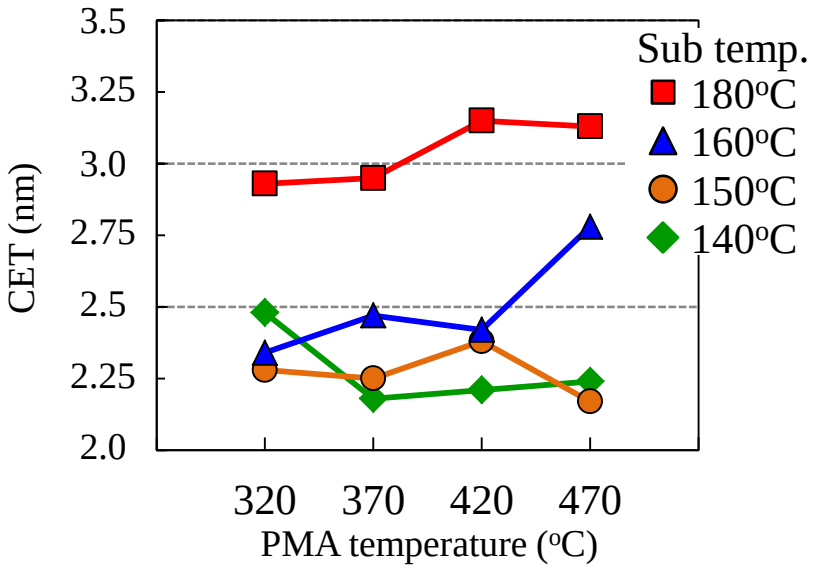

Figure 6.5 CET vs PMA of TiN/W/ALD (75 cycle)-La_2O_3/InGaAs capacitors

Establishing a deposition temperature window is necessary in order to prevent excessive growth of the intended film. In ALD process, the reaction occurs on the substrate surface and the reaction is self-limiting, therefore the synthesized film would only depend on the number of cycles. In contrast in a CVD process, the reaction is predominantly at the chamber and not specifically surface of the substrate, thus it is not a self-limiting process.

Hysteresis for the *CV* characteristics of the capacitors, are compared as a function of ALD growth temperatures for various PMA temperatures, in Figure 6.6. It is found that lowest hysteresis values can be achieved for growth temperature of 140 and 150 ^{o}C. A minimum hysteresis value of 5 mV is obtained for the capacitor with La_2O_3 ALD growth temperature of 150 ^{o}C and PMA at 320 ^{o}C in FG. A higher growth temperature however, causes a sharp increase in the hysteresis.

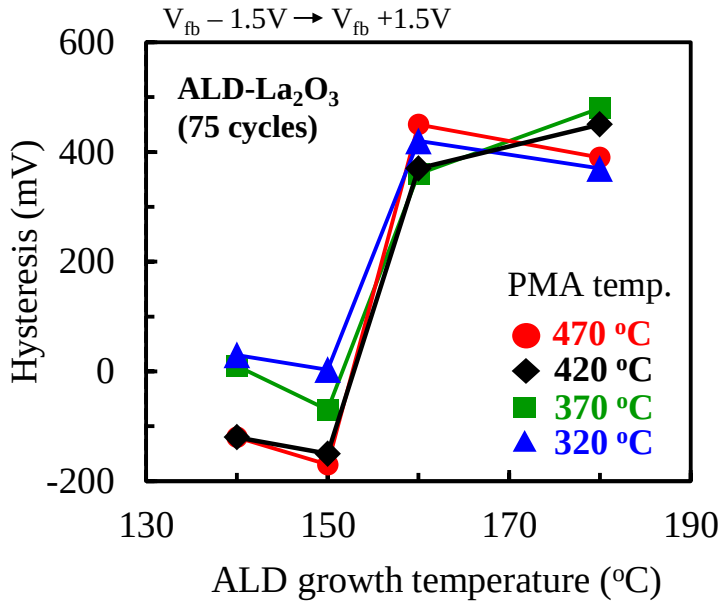

Figure 6.6 Hysteresis dependence of TiN/W/ ALD-La_2O_3(75 cycles)/InGaAs MOS capacitors at 100 kHz, on growth temperature as a function of PMA temperature

The increase in hysteresis has been attributed to formation of elemental As at the interface of dielectric/InGaAs. Oxide species of As (AsO_x) are the easiest to form, but are also very unstable and disintegrate to more stable GaO_x and elemental As, when annealing the capacitors [6.5]. This is an important factor that should be noted for chemical-based deposition of dielectric on InGaAs substrates. The growth temperature should be kept in a range that formation of As oxide species is prevented or minimized. The so called self-cleaning effect of TMA gas used for synthesizing Al_2O_3, is its ability to reduce AsO_x formed at the surface of InGaAs.

Figure 6.7 shows the XPS spectra for (a) As 2 $p_{3/2}$, (b) Ga2 $p_{3/2}$, and (c)In 3$d_{5/2}$ for a TiN (8 nm)/W (3 nm)/La_2O_3 (75 cycles, 150 ^{o}C)/InGaAs MOS capacitors at as deposited and also after PMA 320 , 420 ^{o}C. Formation of all species of As and Ga oxides is effectively suppressed from as-deposited condition to annealing temperature up to 420 ^{o}C. Small amounts of In-O bonds on the other hand, are detected for PMA at 420 ^{o}C. Although InO_x species are reported to be stable and do not degrade interface quality, they might contribute to increase in gate leakage current at scaled gate stacks.

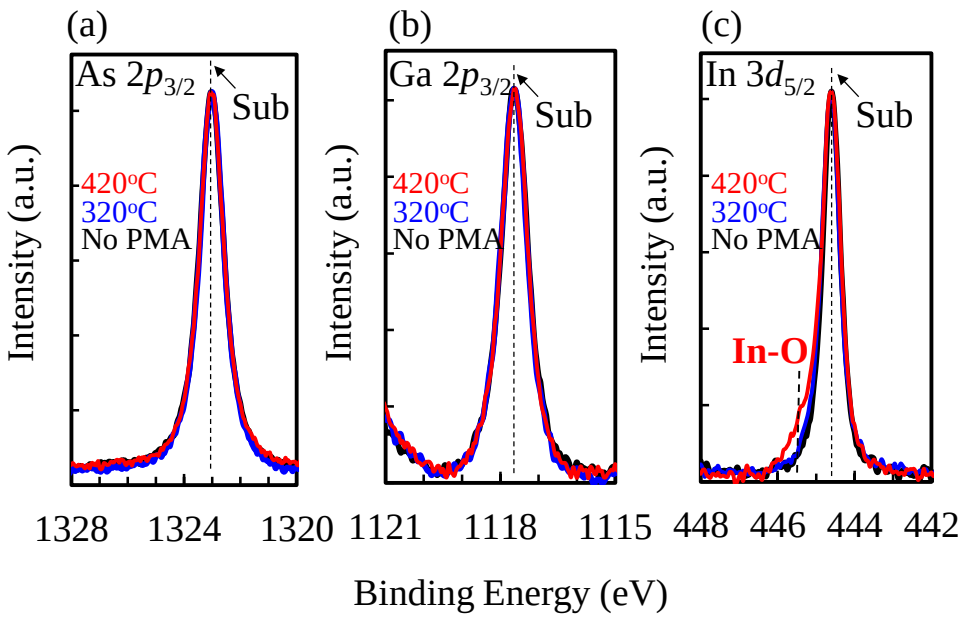

Figure 6.7 XPS spectra of (a) As 2 $p_{3/2}$, (b) Ga2 $p_{3/2}$, and (c)In 3$d_{5/2}$ of TiN/W/ ALD-La_2O_3(75 cycles)/InGaAs MOS capacitors

The La_2O_3 deposition thickness at growth temperature of 150 ^oC, is calculated from La $3d_{5/2}$ peak intensity for 10 and 20 cycles of deposition (Figure 6.8). Same deposition rate of ~0.85 nm/cycle is obtained regardless of the surface treatment method. The effect of sulfur passivation on electrical characteristics of ALD-deposited is subject to further research.

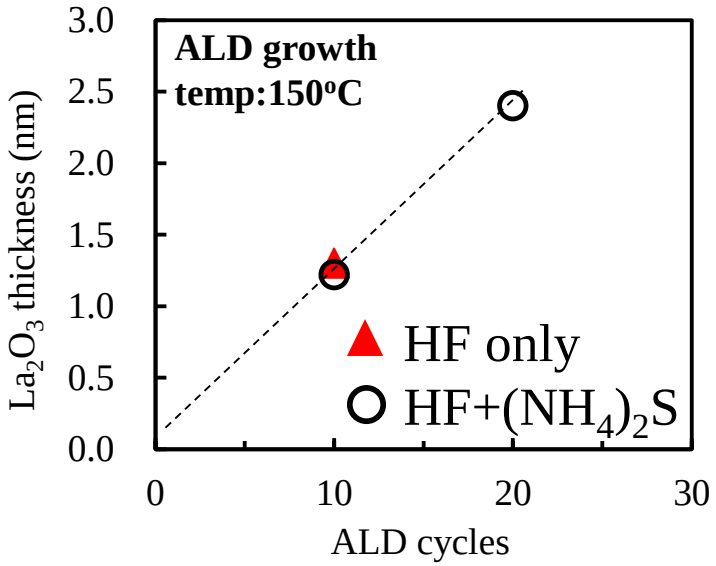

Figure 6.8 La_2O_3 deposition rate for growth temperature of 150 ^oC with and without Sulfur treatment

Conductance method was used to quantitatively evaluate the interface state density of samples at various growth temperatures and the results are shown in Figure 6.9 and 6.10. The increase in D_{it} value for higher annealing temperatures is the similar to EB

deposited samples. However a sharper increase for ALD case is observed. The smaller D_{it} values for lower annealing temperatures could be due to the presence of residual Carbon (C) atoms within the synthesized dielectric film which diffuses towards the interface as the annealing temperature increases. Further physical analysis of the film is necessary to accurately characterize the quality of film and its impurity level. Adjusting the purge and exhaust time during deposition cycles, has been reported to be effective in reducing the impurity levels within the dielectric layer [6.6], therefore further optimization of experimental procedure is required.

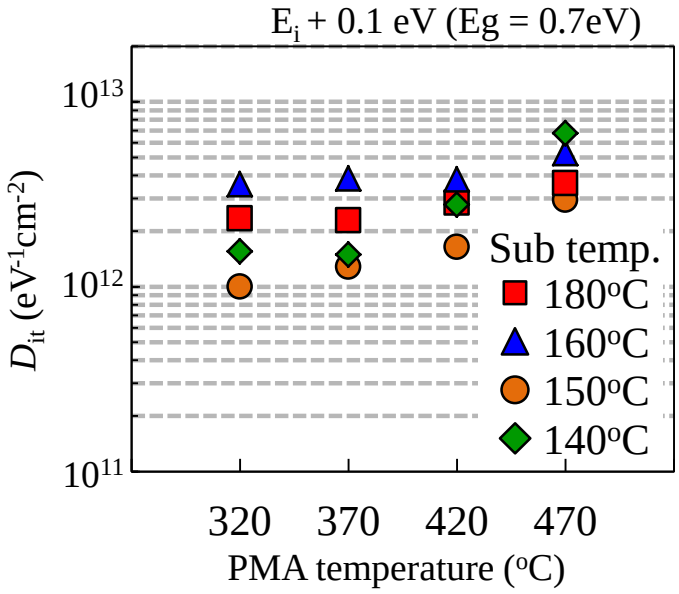

Figure 6.9 Growth temperature effect on D_{it} of TiN/W/ ALD-La_2O_3(75 cycles)/InGaAs MOS capacitors as a function of PMA temperature

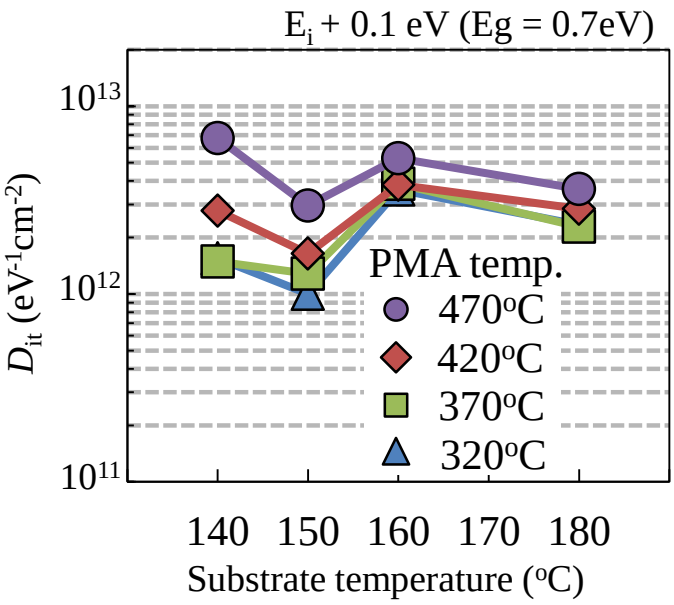

Figure 6.10 D_{it} of TiN/W/ ALD-La_2O_3(75 cycles)/InGaAs MOS capacitors as a function of growth temperature at various PMA.

The *CV* characteristics of TiN (45 nm)/W (5 nm)/La_2O_3/InGaAs capacitors with ALD synthesized La_2O_3 film after PMA 320 ^oC is shown in Figure 6.11. ALD is performed for 75 cycles and the substrate temperature is set to 150 ^oC during the deposition.

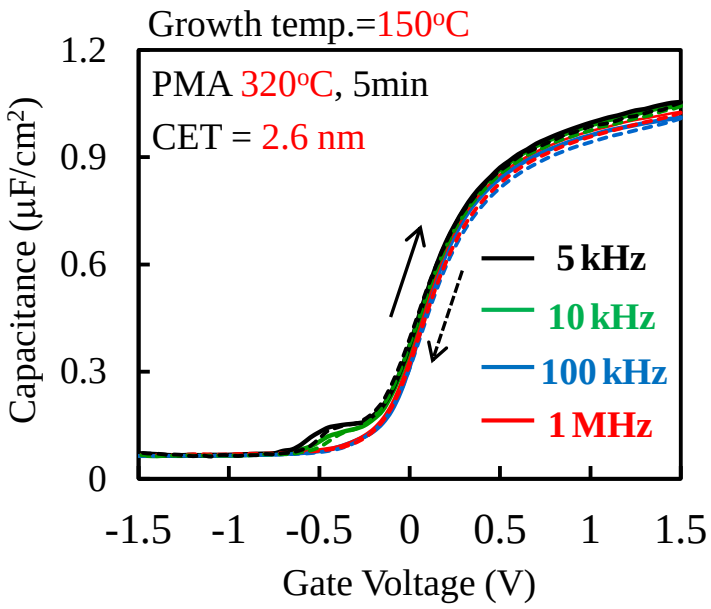

Figure 6.11 *CV* characteristics of TiN/W/ ALD-La_2O_3(75 cycles)/InGaAs MOS capacitor after PMA in FG at 320 ^oC for 5 min.

A healthy *CV* is observed with very small frequency dispersion in all gate bias conditions. Figure 6.12 compares the *CV* characteristics of ALD-La_2O_3 and EB- La_2O_3 capacitors at 100 kHz. The capacitance value is normalized to C_{max}. Identical *CV* characteristics for both ALD and EB deposited capacitors indicate the formation of high quality of interface. A benchmark of interface state density (D_{it}) as a function of CET between capacitors fabricated in this thesis with other recently reported results is shown in Figure 6.13.

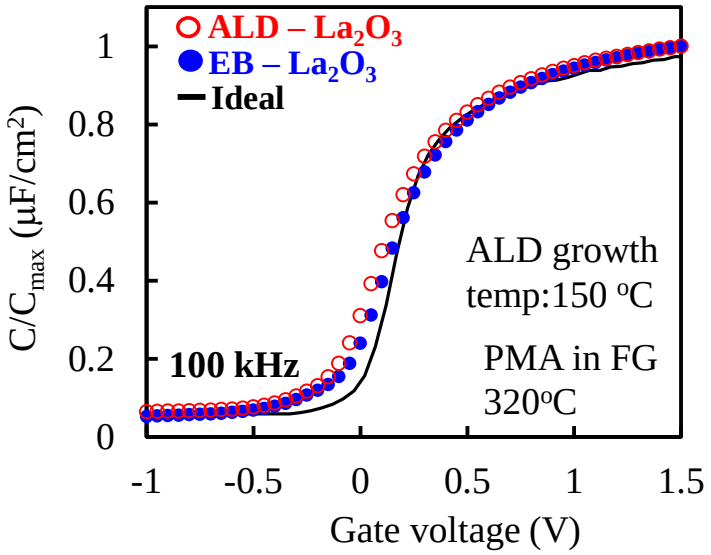

Figure 6.12 Comparison between the normalized 100 kHz *CV* curves of ALD-deposited and EB-deposited TiN/W/La_2O_3/InGaAs MOS capacitor against the ideal curve

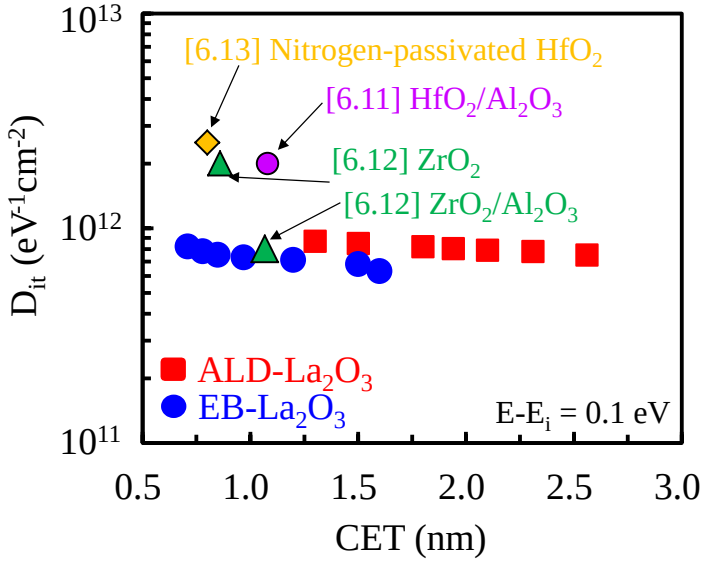

Figure 6.13 D_{it} vs CET benchmark of capacitors in this work with recent published results

6.2.4 Conclusions

TiN/W/La_2O_3/InGaAs MOS capacitors were fabricated by atomic layer deposition of La2O3 film. It was shown that substrate temperature during film synthesis significantly affects the electrical properties of the capacitors, in particular *CV* hysteresis. Hysteresis value as small as 5 mV can be achieved by keeping the substrate temperature below 150 ^{o}C. Formation of AsOx species and their disintegration to elemental As during PMA could cause the increase in hysteresis. The interface state density and leakage current of the EB and ALD deposited La_2O_3 films are comparable at lower PMA temperatures. Further process modification to inhibit the impurities in the synthesized film, could improve thermal stability of the layer.

6.3 Non-alloyed Ni Silicide/InGaAs Contact

6.3.1 Introduction

One of the challenges that need to be resolved in order to benefit from the InGaAs's superior transport properties is fabricating a low resistance self-aligned source/drain access regions suitable for CMOS logic. The access resistance includes the source/drain (S/D) sheet resistance, the metal-semiconductor contact resistance and the metal sheet resistance. High thermal budget that is required for dopant activation in ion implantation method, is shown to be a limiting factor for this approach [6.7]. Furthermore, low dopant solubility of compound semiconductors, makes high doping levels required for scaled channel lengths difficult. Selective epitaxy of in-situ doped InGaAs S/D regions has also been carried out by molecular beam epitaxy (MBE) and metal-organic vapor phase epitaxy (MOVPE) [6.8], achieving a high carrier density in a self-aligned gate-first scheme. These two approaches require the III-V substrate to be etched down until an etch-stop layer before regrowth. This is not compatible with a potential extremely-thin III-V-on-insulator (ET-III-V-OI) integration scheme which is predicted to be needed for the 11 nm node and beyond. A salicide-like (self-aligned silicide)

process on InGaAs has been developed using an (Ni)-InGaAs alloy structure [6.9]. This structure suffers from a high off-state drain current due to the absence of a channel-to-S/D p-n junction.

Moreover, at ultra-scaled device sizes (beyond 11 nm) and 3D FinFET, Nanowire structures, it is critical to achieve abrupt and shallow junctions at S/D region in order to suppress the short channel effects. Achieving an abrupt junction, requires controlling the intermixing (reaction) of metal and III-V semiconductor at metal/III-V interface and prevent alloy formation.

It has been shown that thick Ni films (> 30 nm) can mix with InGaAs even from the deposition stage, and form Ni-InGaAs alloy (Figure 6.11). However, for scaled metal S/D MOSFETs (Lg < ~50 nm) with suppressed short channel effects, sufficiently thin layers (< ~10 nm) is required.

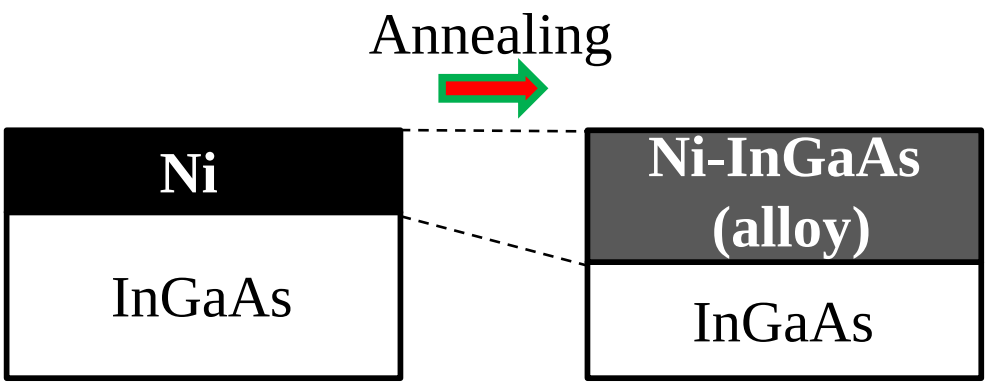

Figure 6.11 Schematic showing the Ni-InGaAs alloy formation

Several issues arise from simply thinning the deposited Ni-film on InGaAs. Figure 6.12 (a) [6.10] shows the cross-sectional TEM image of 4-nm Ni film on InGaAs substrate after annealing at 200 ^{o}C. The high reactivity of Ni and InGaAs has resulted in a 8-nm thick alloyed layer. Although at low annealing temperature it is possible to achieve thin films, increasing the annealing temperature [Figure 6.12 (b)], severely degrades both the interface and surface of Ni-InGaAs alloy.

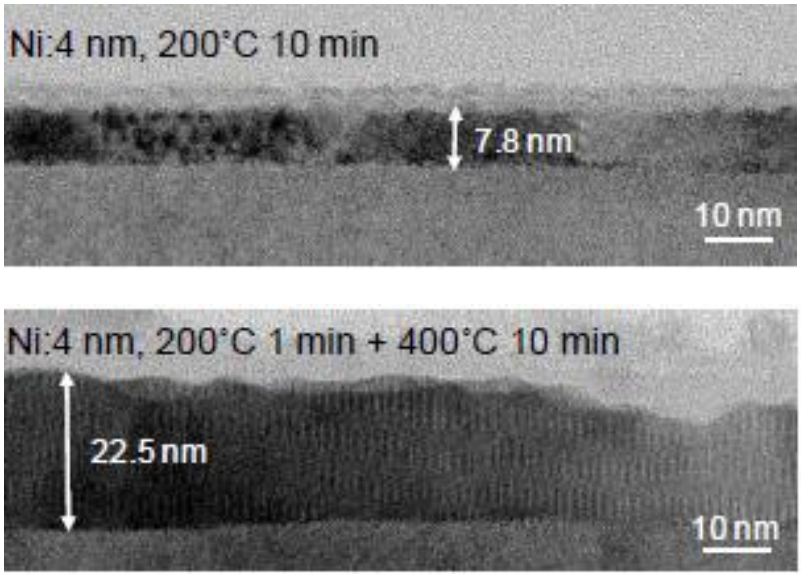

Figure 6.12 Figure 6.12 Cross-sectional TEM image for Ni/InGaAs with low and high temperature PMA. [6.10]

In this section, a novel Ni/Si stacked silicidation process is proposed to achieve thin metal contact with InGaAs control the Schottky interface. It is shown that by using

stacked $NiSi_2$/InGaAs structure, an atomically flat and non-alloyed interface with stable physical and electrical properties can be achieved in a wide range of process temperature window. The proposed process has high potential for application in metal S/D of scaled 3-dimensional devices. Furthermore, in this section the composition of Ni-InGaAs alloy and the changes that Ni-InGaAs alloy goes through upon annealing, has been analyzed by XPS analysis.

6.3.2 Experimental Procedure

The fabrication process for diodes is summarized in Figure 6.13. *p*- type $In_{0.53}Ga_{0.47}As$ (100) substrates epitaxially grown on InP substrate with doping concentration of 2×10^{17} cm^{-3}, were cleaned by acetone/ethanol followed by surface oxide removal by concentrated HF (20%). A 400 nm protective SiO_2 layer was deposited by chemical vapor deposition (CVD) using Tetraethyl orthosilicate (TEOS) gas. The SiO_2 layer was patterned and etched away by BHF to create diode contact areas. Substrates were then transferred to an RF sputtering chamber and Ni and Si was deposited. The remaining metal layers were removed by lift-off process. Samples were then annealing in N_2 and finally Al layer for back contact was deposited.

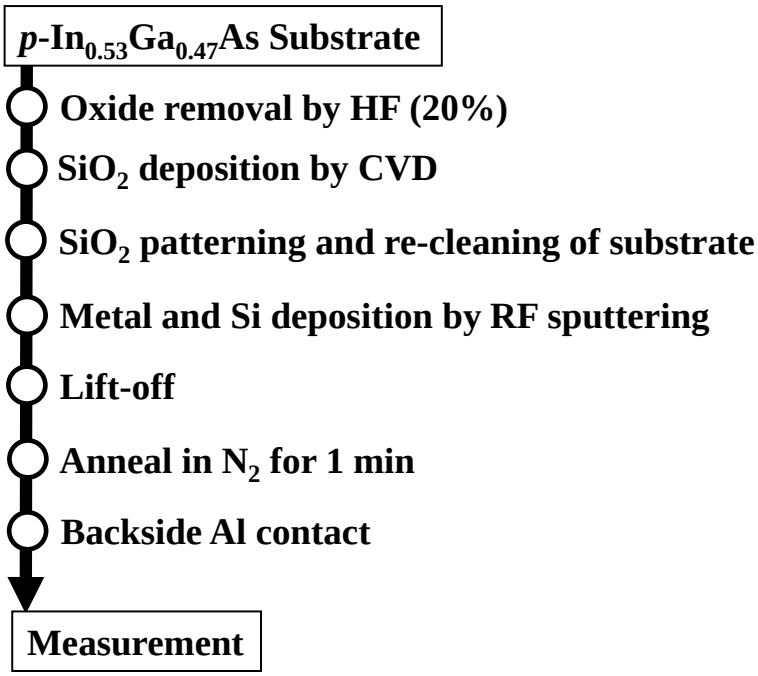

Figure 6.13 Fabrication process for metal/InGaAs junction

Two types of diodes were fabricated. For Ni/InGaAs contacts, a 10-nm Ni film was deposited on InGaAs substrate (Figure 6.14 (a)). The Ni/Si stacked structure was made by depositing Ni: 0.5 nm and Si: 1.9 nm in cycles for a total of 16 cycles (Figure 6.14 (b)). The thicknesses of Ni and Si films were optimized to target an atomic ratio Ni:Si of 1:2.

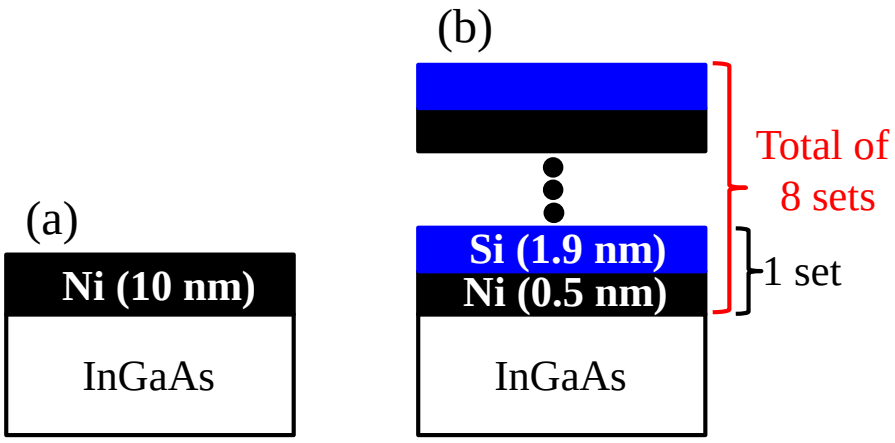

Figure 6.14 Schemactic of Ni/InGaAs and $NiSi_2$/InGaAs contacts

6.3.3 Comparison of metal/InGaAs Interfaces

Cross-sectional TEM image of Si (1.9 nm)/ Ni (0.5 nm) stack structre (illustrated in Figure 6.14 (b)) on *p*-InGaAs after annealing in N_2 at 400 ^{o}C, is shown in Figure 6.15 (b) and (c). A uniform film with atomically flat interface and no observable defects in substrate or metal side, is obtained. The size reduction of multi-layer film's total thickness after annealing to ~ 11 nm is indicative of a $NiSi_2$ composition, where no consumption from the substrate has taken place. The possibility of alloy formation and intermixing of substrate elements with the post-annealed Ni/Si multi-layer, was examined Energy-dispersive X-ray spectroscopy (EDX) measurement of the deposited layer was carried out. The EDX point, shown in Figure 6.15 (c) was chosen close to the

interface. Only Ni and Si elements were detected as can be confirmed in Figure 6.15 (d), thus no sign of substrate and deposited layer could be seen.

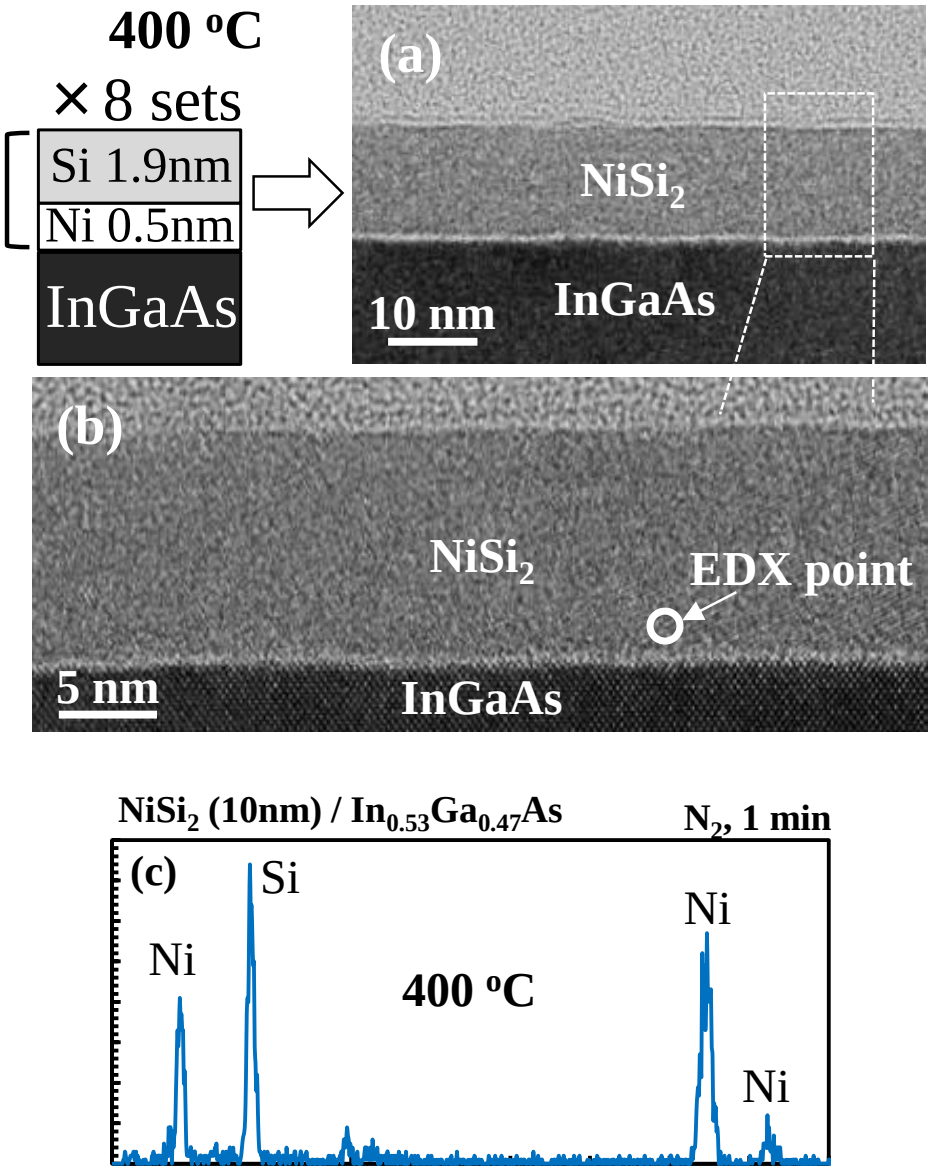

Figure 6.15 (a), and (b) Cross-sectional TEM image of Ni/Si stacked structure on InGaAs after RTA in 400 ^{o}C, (c) EDX analysis of near interface layer

The effect of annealing temperature on the composition of stacked Ni/Si multi-stack structure and Ni layer on InGaAs substrate was analyzed in detail by Hard X-ray photoelectron spectroscopy (XPS) measurements. The measurements were carried out at SPring-8 with BL46XU using an x-ray light source of 7940 eV at a take-off angle of 80^{o}. (Figure 6.16 (a)). An R-4000 high-resolution electron energy analyzer modified for HX-PES was used.

Ni $2p_{3/2}$ core-level spectra obtained from Ni/Si multi-stack structure corresponding the to the TEM image in Figure 6.16 (b) shows a 1.5 eV shift to the higher energy level as a result of annealing.

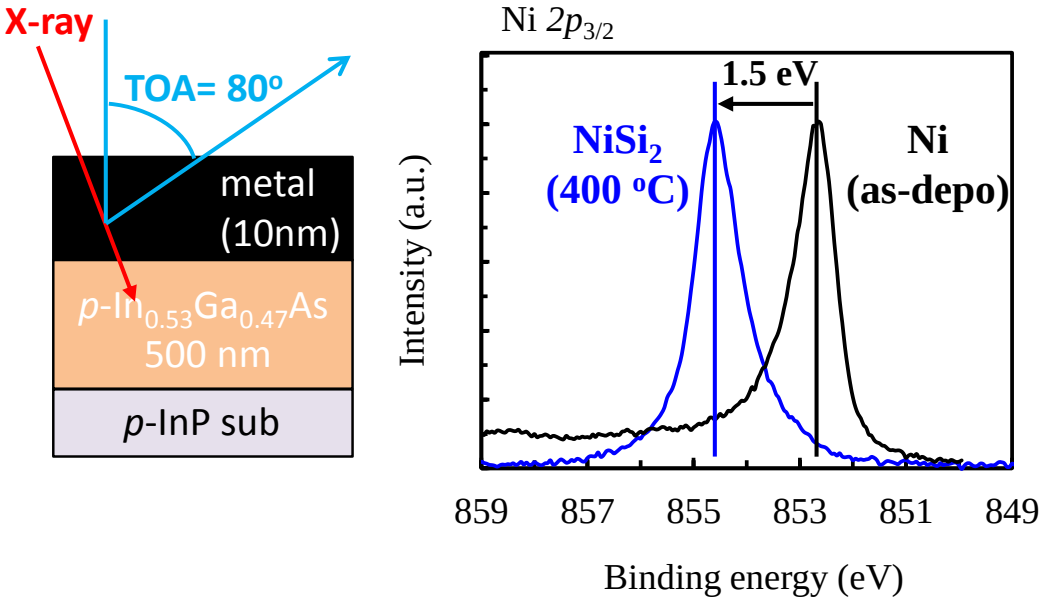

Figure 6.16 Ni2$p_{3/2}$ XPS spectra of $NiSi_2$/InGaAs for before and after PMA at 400 oC.

It has been reported that this amount of shift indicates the formation of $NiSi_2$ where Ni $2p_{3/2}$ peak appears at more than 1 eV higher energy position. Therefore, the stacked Ni/Si structure is referred to as $NiSi_2$ stack in the remaining of this thesis.

Although many papers on Ni-InGaAs alloy have been published, the exact composition of the alloy and the annealing temperature effect on its structure is not well studied yet. In this section, comprehensive XPS anlysis are conducted to clarify the physical nature of Ni and InGaAs reaction. As $2p_{3/2}$, Ga $2p_{3/2}$ and In $3d_{5/2}$, core-level spectra obtained from Ni (10 nm)/$In_{0.53}Ga_{0.47}As$ sample at various annealing temperatures are shown in Figure 6.17. The annealing temperature is varied from as-deposited (no thermal treatment) to 500 ^{o}C. Two distinctive peaks can be separated for all three elements from InGaAs at all of the annealing conditions. One is originating from the substrate, and the other arising from the Ni-InGaAs alloy. As the annealing temperature is increase, the alloyed layer increases in thickness since more of the substrate is consumed by Ni. This corresponds to the weakening of the signals from the substrate and a subsequent intensification of the signals from the alloy. Examining the Ga $2p_{3/2}$ state, shows the formation of the most stable oxidation state of Ga, Ga_2O_3. The intensity of Ga_2O_3 peak increases at higher annealing temperatures pointing to a larger concentration of the oxide at the surface of the alloyed layer.

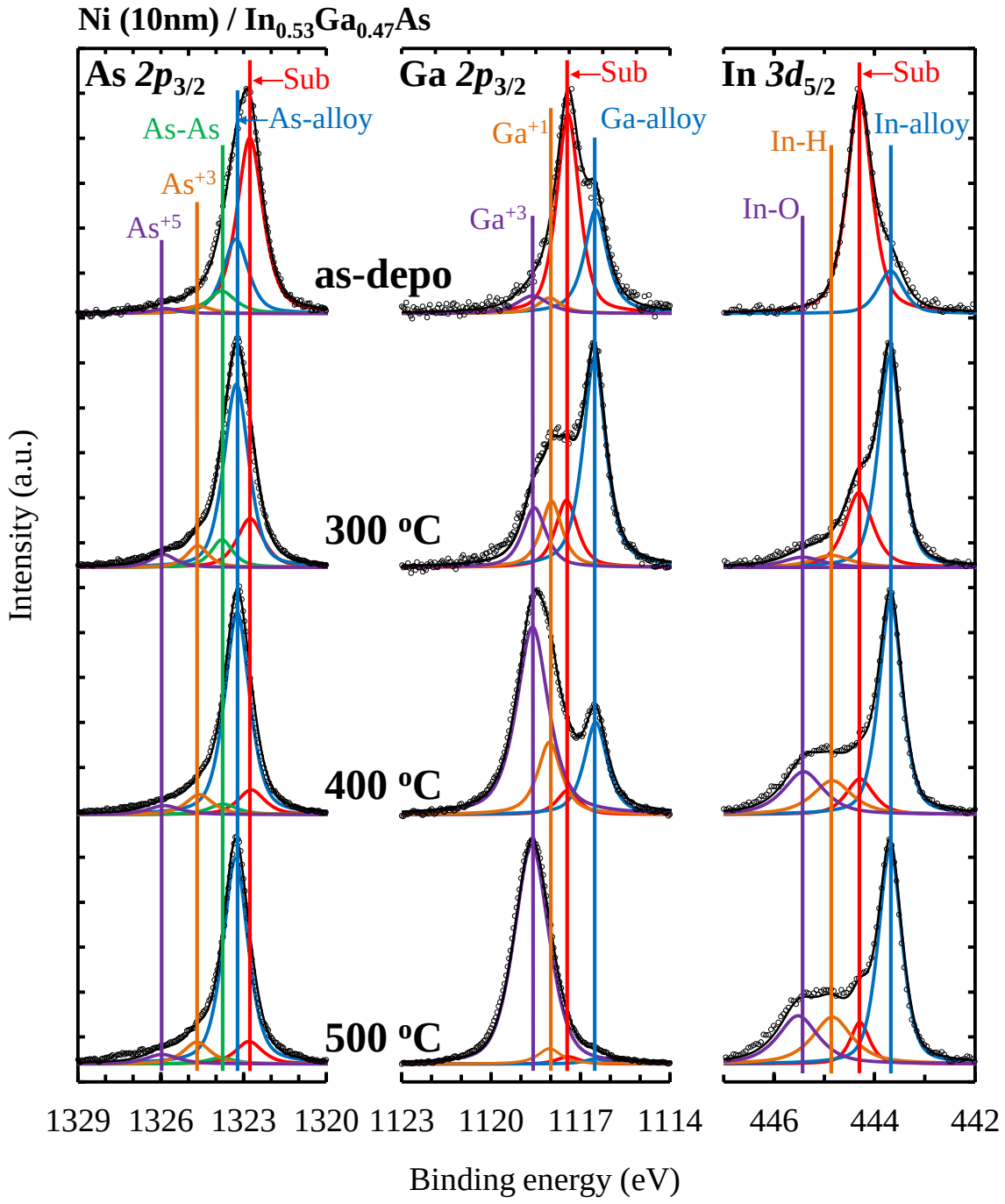

Figure 6.17 HAXPS spectra for As $2p_{3/2}$, Ga $2p_{3/2}$, and $In3d_{5/2}$ of Ni/InGaAs at different PMA temperatures in N_2 for 1 min.

The intensity ratio of the three In, Ga and As elements from the substrate, measured from normalized XPS peaks, at annealing temperature from 300 ,400 and 500 ^{o}C compared to the as-deposited condition are shown in Figure 6.18. A uniform decrease in the peak intensities for all elements is observed at elevated annealing temperatures, which is in agreement the thickening of Ni-InGaAs alloy layer.

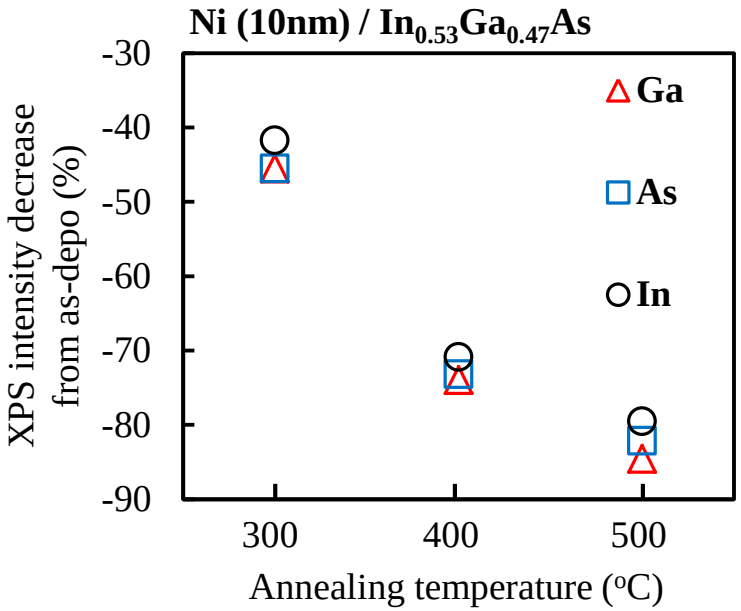

Figure 6.18 Relation between substrate elements peak intensity and PMA temperature

Figure 6.19 shows the As $2p_{3/2}$, Ga $2p_{3/2}$ and In $3d_{5/2}$ peaks for $NiSi_2$ (11 nm)/InGaAs sample at 400, 500 and 600 ^{o}C. It is clear that the alloy and oxide species, observed in Ni/InGaAs interface, are not detectable in $NiSi_2$/InGaAs structure. This is in agreement

with TEM and EDX results. The XPS spectra remain unchanged for annealing temperature up to 600 ^{o}C.

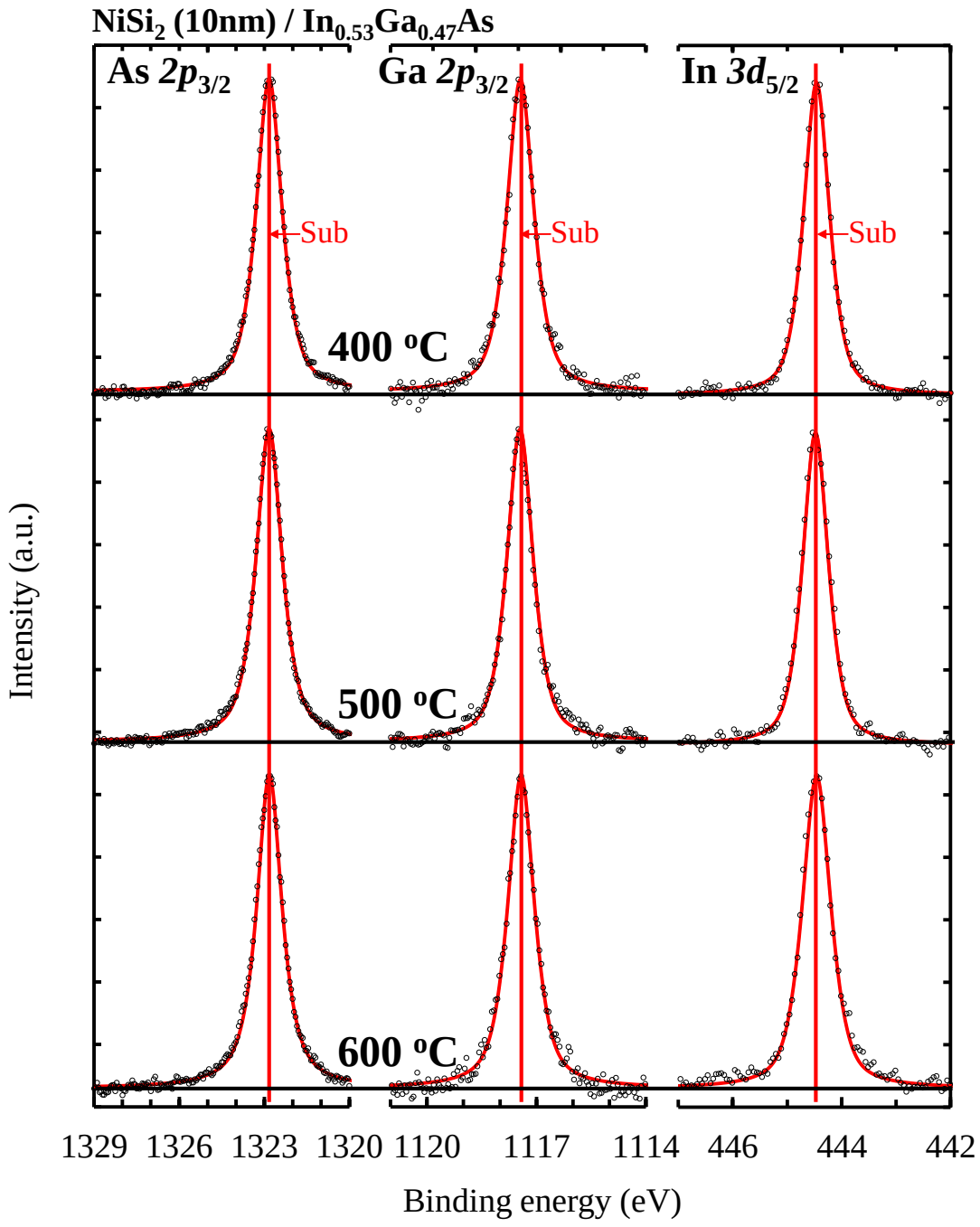

Figure 6.19 HAXPS spectra of $NiSi_2$/InGaAs at different PMA temperatures in N_2 for 1 min.

To confirm the elemental balance of the $In_{0.53}Ga_{0.47}As$ at $NiSi_2$/InGaAs interface, the peak intensity of the three In, Ga and As elements in relation to one another at 400, 500 and 600 ^oC is evaluated and shown in Figure 6.20. The ratio of elements remains almost constant regardless of the annealing temperature, implying a high thermal stability for $NiSi_2$/InGaAs stack.

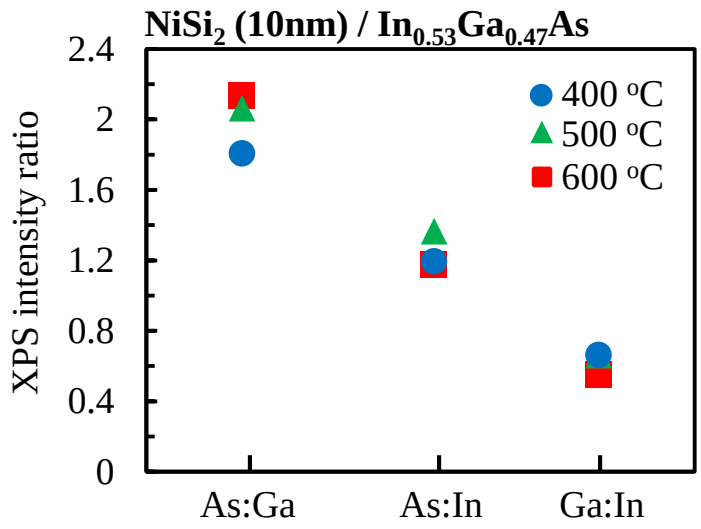

Figure 6.20 Relation between substrate elements peak intensity and PMA temperature

The electrical properties of both Ni/InGaAs and $NiSi_2$/InGaAs diode structures were compared by measuring the Current density-Voltage (*JV*) characteristics of the samples.

Figure 6.21 shows the *JV* characteristics for both diodes at 400 ^{o}C. Although well-behaved Schottky characteristicsis can be obtained in both cases the ON/OFF ratio for $NiSi_2$ stack is two oders of magnitude larger.

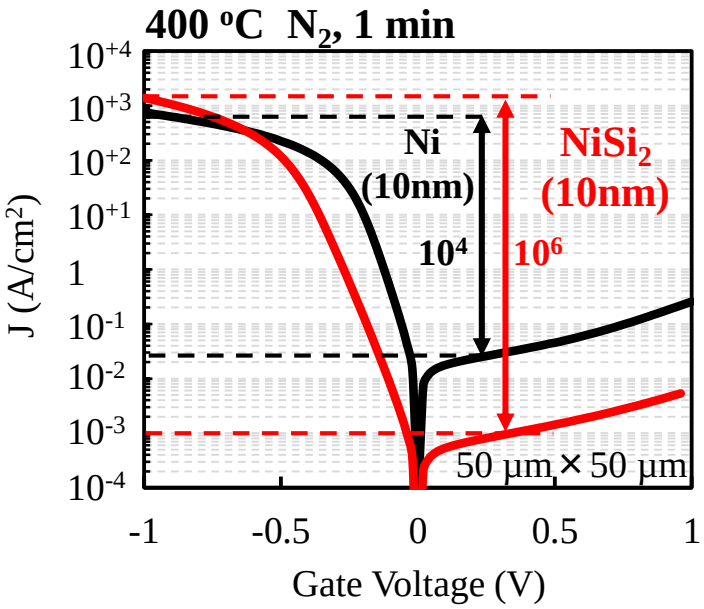

Figure 6.21 *JV* characteristics for Ni (10 nm)/InGaAs and $NiSi_2$/InGaAs.

The comparison between the *JV* characteristics for Ni and $NiSi_2$ diodes at a PMA windown of 400 ~ 600^{o}C is shown in Figure 6.22. A consistent 10^6 ON/Off ratio is achieved for $NiSi_2$ diode, whereas a significant increase in the reverse current fo Ni diode is observed by increasing the PMA temperature. This indicates a range of potential difficutlties Ni contacts could face for gate last process where several thermal

treatments are necessary.

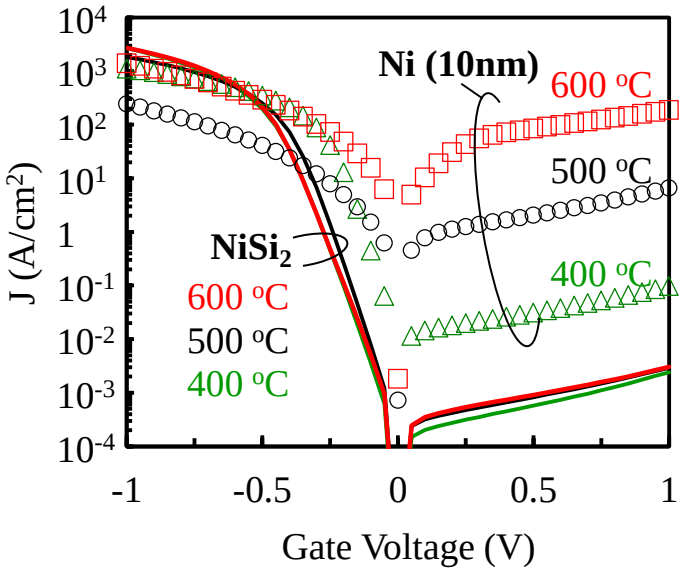

Figure 6.22 *JV* characteristics for Ni (10 nm)/InGaAs and $NiSi_2$/InGaAs at various PMA.

The reports on the value of Richardson constant for InGaAs are scarce and not well agreed upon, therefore for accurate assessment of Schottky Barrier Height (SBH) of $NiSi_2$/InGaAs, multi-temperature *JV* measurements were carried out. The results are shown in Figure 6.23.

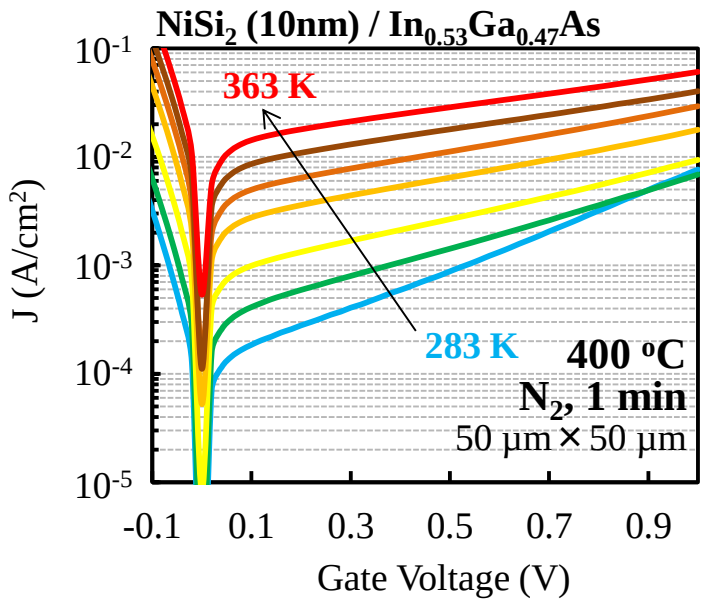

Figure 6.23 Temperature dependent *JV* characteristics for $NiSi_2$/InGaAs.

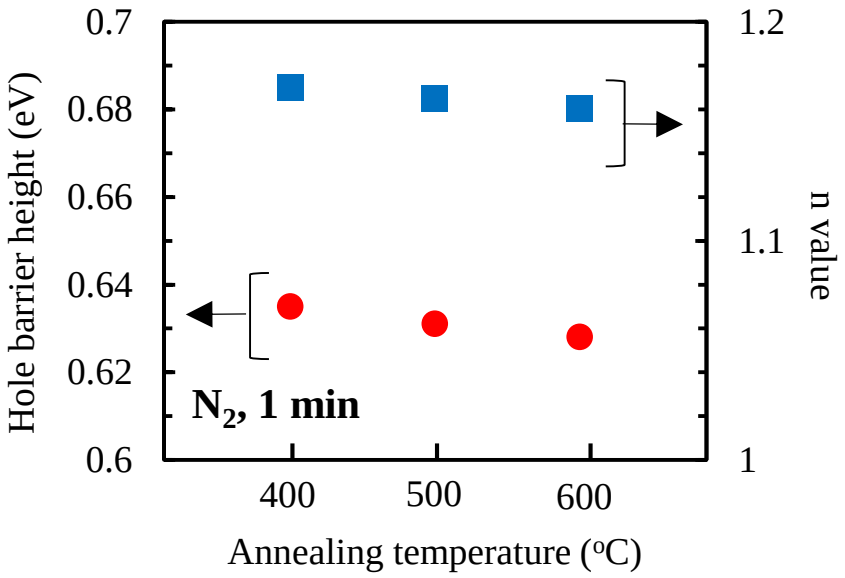

Figure 6.24 Hole barrier height and ideality factor (n) for $NiSi_2$/InGaAs junction at various annealing temperatures.

The barrier height for holes and the ideality factor of $NiSi_2$/InGaAs diodes extracted from *JV* characteristics, are summarized in Figure 6.24. The barrier height for holes is close to the reported values for Ni/InGaAs interface which point to the pinning of Fermi level at the interface of metal/InGaAs. More experiments are necessary to enable modulation of barrier height through silicidation process.

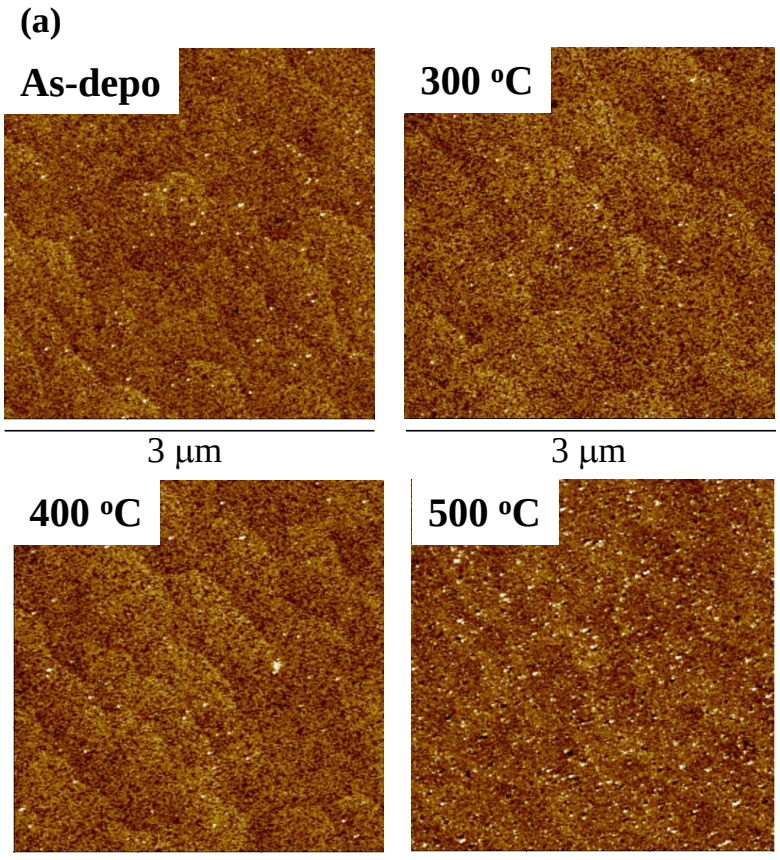

Figure 6.25 AFM images for $NiSi_2$ surface on InGaAs after PMA.

By using physical analysis, it was shown that a thermally stable $NiSi_2$/InGaAs interface can be achieved by Ni/Si stacked structre. However, it is also important for the metal contact to have a smooth surface to reduce parasitic resistance in device structre. Atomic Force Microscopy (AFM) measurements of $NiSi_2$ surface, deposited on InGaAs show a smooth surface with roughness of ~1 nm in annealing temperatures of up to 500 ^oC (Figure 6.25 and 6.26).

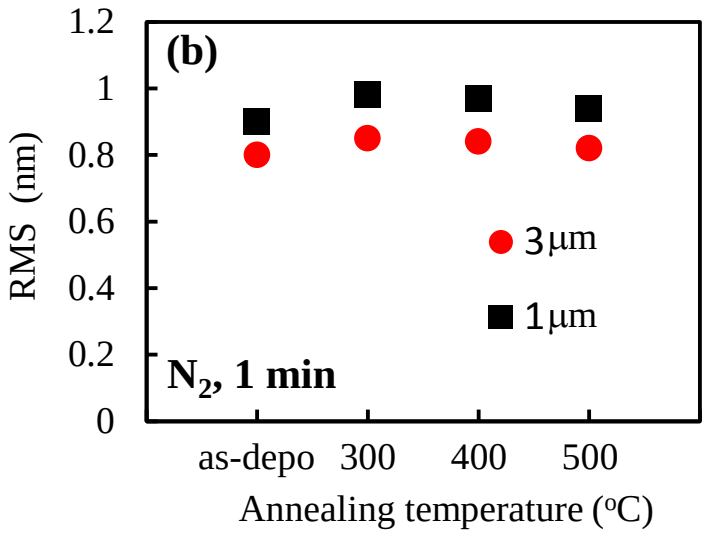

Figure 6.26 RMS values for $NiSi_2$ surface on InGaAs after PMA.

6.3.4 Conclusions

Thermally stable NiSi2/InGaAs contacts were fabricated by a multi-layer stack structure. The $NiSi_2$/InGaAs junctions exhibit near ideal Schottky characteristics with ideality factor (n) of 1.1 for annealing temperatures as high as 600 ^{o}C. In contrast to Ni/InGaAs contacts, both the surface of $NiSi_2$ and its interface with InGaAs, show high thermal tolerance and remain flat.

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Chapter 7

InGaAs-based MOSFETs with La_2O_3 as gate dielectric

Chapter 7 InGaAs-based MOSFETs with La_2O_3 as gate dielectric

7.1 Introduction

Integration of high-mobility channels such as InGaAs is envisaged for beyond 14-nm node devices. Majority of device demonstrations, overwhelmingly use Al_2O_3 as gate dielectric, which benefits from good interface properties [7.1]. Consequently scaling of InGaAs-based gate stacks has been limited due to low k-value (~9) of Al_2O_3. This is in contrast to the requirements for high C_{ox} values in quasi-ballistic regime of 10-nm node and beyond, which is necessary to minimize the effect of high semiconductor capacitance in InGaAs-based devices [7.2]. In previous chapters, La_2O_3/InGaAs interface properties were described and various methods including metal selection and ALD process for improving the interface quality were proposed. In this section, the InGaAs MOSFET operation with ALD-La_2O3 gate stack and Ni as metal source/drain has been demonstrated.

7.2 Experimental Procedure

The fabrication process for InGaAs-based transistors is summarized in Figure 7.1. *p*-type $In_{0.53}Ga_{0.47}As$ (100) substrates epitaxially grown on InP substrate with doping concentration of 2×10^{17} cm^{-3}, were cleaned by acetone/ethanol followed by surface oxide removal by concentrated HF (20%). A 400 nm protective SiO_2 layer was deposited by chemical vapor deposition (CVD) using Tetraethyl orthosilicate (TEOS) gas. The SiO_2 layer was patterned and etched away by BHF to create diode contact areas. Substrates were then transferred to an RF sputtering chamber for Ni depositioin. After the 10 nm of Ni deposition samples were annealed in N_2 at 250 ^oC to form Ni-InGaAs alloy at the contact areas. The samples were then subjected to BHF and HF 10% to remove metal and SiO_2 simultaneously from non-contact regions in a lift-off process and thus form the Source/Drain contact regions. A second SiO_2 layer with TEOS was subsequently deposited and patterned to create field isolation. Channel area was cleaned and passivated by $(NH_4)_2S$ as described in previous sections. The substrates were the loaded to ALD chamber for La_2O_3 films synthesis at 150^oC for 75 cycles, followed by *in-situ* metal deposition by RF sputtering. A TiN (45 nm)/W (5 nm) metal gate was used as the gate electrode. The samples were post-metallization annealed

in forming gas ambient (N_2:H_2 = 97%:3%) for 5 mins. After Source/Drain contact formation, Al was deposited on the back side of the InGaAs/InP substrate to form the back contact.

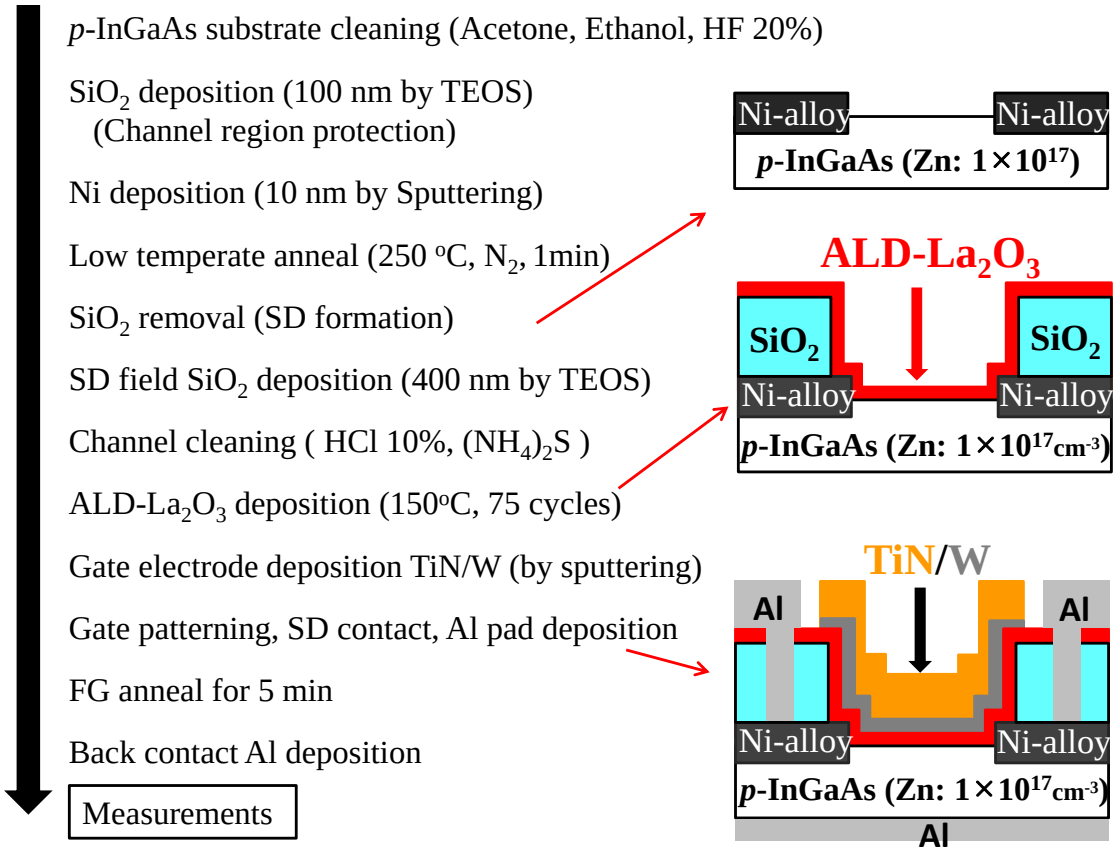

Figure 7.1 Process flow for InGaAs-MOSFET fabrication.

7.3 Experimental Results

Figure 7.2 shows drain current- drain voltage (I_d-V_d) characteristics of TiN(45 nm)/W (5 nm)/ALD-La_2O_3 (75 cycles at 150 ^oC)/p-InGaAs after PMA 320 ^oC. Well-bahved MOSFET operation is confirmed albeit the apparent high contact resistance at source/drain.

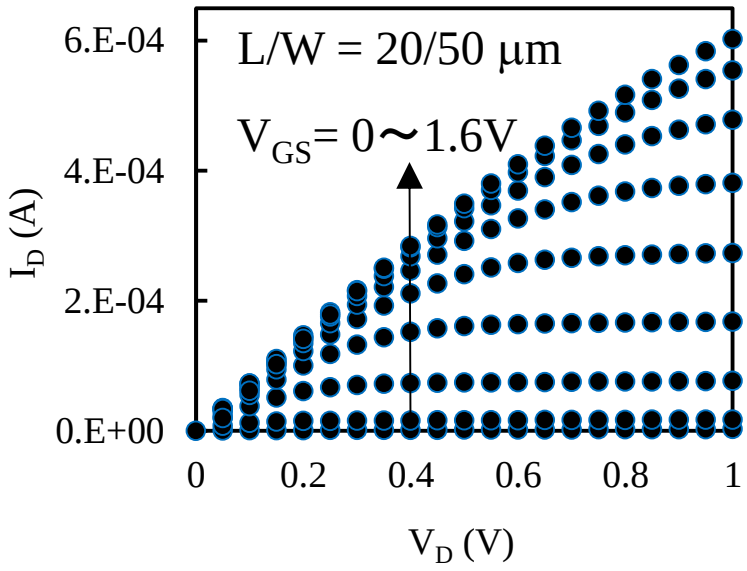

Figure 7.2 I_D-V_D characteristics of TiN(45 nm)/W (5 nm)/ALD-La_2O_3 (75 cycles at 150^{o}C)/p-InGaAs after PMA 320^{o}C.

I_d-V_g chracteristics of the same MOSFET at a linear and saturation drain voltage (V_d) of 50 mV and 1 V are shown in Figure. 7.3. A substhreshold slope (SS) of ~ 139 mV/dec is

exctracted which is roughly similar to the reported values for Al_2O_3 gate stacks on planar InGaAs MOSFETs [7.3], indicating a high quality of high-*k*/InGaAs interface.

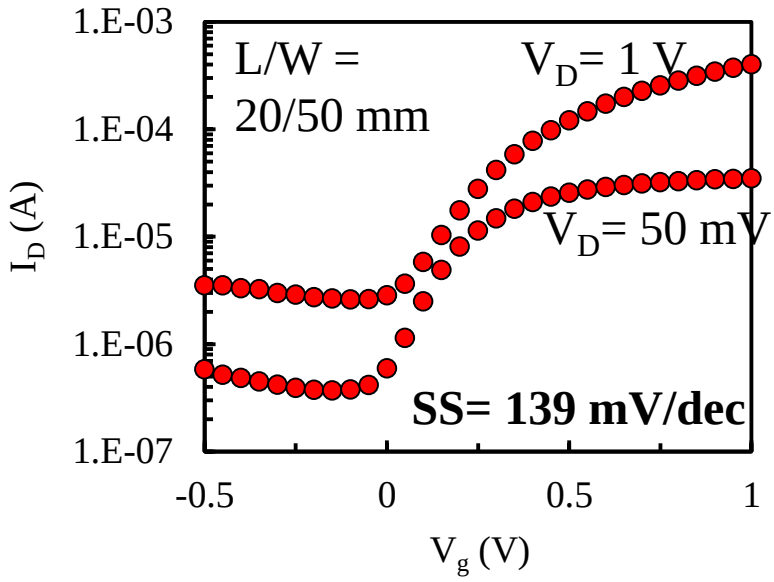

Figure 7.3 I_d-V_g characteristics of TiN(45 nm)/W (5 nm)/ALD-La_2O_3 (75 cycles at 150^{o}C)/p-InGaAs after PMA 320^{o}C.

Effective mobility (μ_{eff}) was calculated by split *CV* method using the capacitance response at 100 kHz and is shown in Figure 7.5. The gate to channel CV characteristics of MOSFET in 100 kHz is shown in Figure 7.4. The CET= 1.1 nm is extracted by fitting the curve to the ideal *CV* as described in chapter 3.

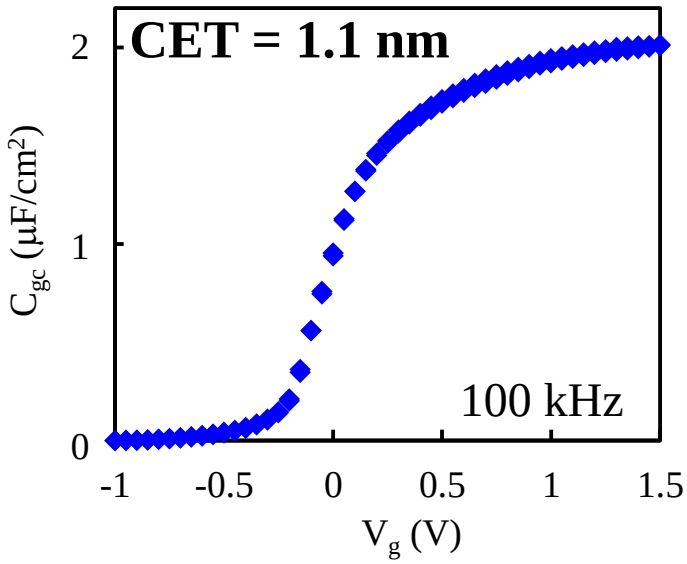

Figure 7.4 100 kHz split C-V characteristics of Ni-SD InGaAs MOSFET with ALD-La_2O_3.

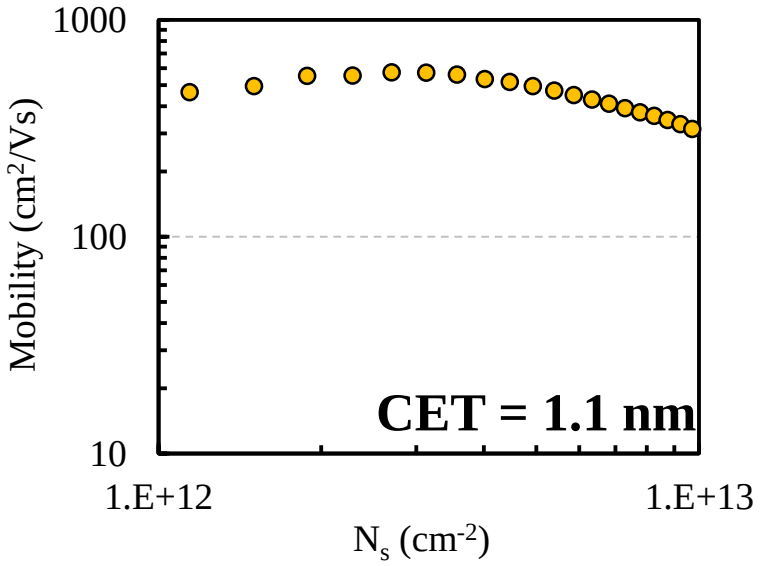

Figure 7.5 Mobility characteristic of InGaAs MOSFET with ALD-La_2O_3.

Figure 7.6 shows the high field mobility mobility vs. CET plot for various

high-*k*/InGaAs planar n-MOSFETs.

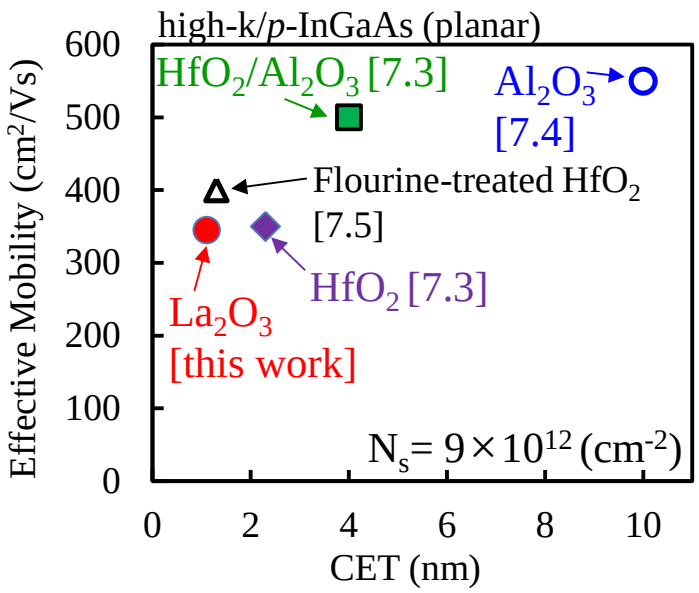

Figure 7.6 High field mobility vs. CET plot for various planar n-MOSFETs high-*k*/InGaAs.

Although a higher effective mobility can be obtained for Al_2O_3/InGaAs, there is a severe CET penalty. At smaller CET where the effective thickness reaches ~1.0 nm region, La_2O_3 layer with no complicated passivation technique, achieves high electron mobility comparable to HfO_2/InGaAs at $N_s= 9\times10^{12}(cm^{-2})$.

In table 7.1, list of recent results on various gate stack and junction technologies used on InGaAs platform, as well as the results from this thesis is summarized. The scalability, low D_{it}, and thermal stability of La_2O_3/InGaAs interface, combined with robust $NiSi_2$/InGaAs junction indicate a great potential for their application in future

device technology nodes.

Table 7.1 Comparison of gate stack and SD properties in this thesis with recent reported results

	Gate stack			junction		
Reference	Gate dielectric	D_{it} ($eV^{-1}cm^{-2}$)	CET / Process temp.	Structure	Process Temp.	Interface condition
[7.6] S. Takagi *et al.*, 2012 *IEDM*	Al_2O_3 & HfO_2/Al_2O_3	$2.0x10^{12}$ $2.0x10^{12}$	1.08nm / 400°C	Ni	< 400°C	Alloy Formation
[7.7] X. Gong *et al.*, 2012 *VLSI*	HfO_2/SiO_2 and Si Cap	$1.9x10^{12}$	1.26nm (EOT) / 400°C	Implant [2]	700°C [2]	-
[7.8] N. Goel *et al.*, 2008 *IEDM*	ZrO_2	$2.0x10^{12}$	0.78nm / -	Implant	700°C	-
This thesis	**La_2O_3**	**$8.0x10^{11}$**	**0.73nm / 570°C**	**$NiSi_2$**	**600°C**	**Small reaction (R_a=0.47nm)**

7.4 Conclusions

InGaAs MOSFET operation with ALD-La_2O_3 as high-*k* gate dielectric with CET= 1.1 nm and Ni as metal source/drain has been demonstrated. Well behaved MOSFET transfercharacteristics were achieved although the high contact resistance at source/drain regions contribute to smaller I_{on}/I_{off} ratio of drain current. Reducing the contact resistance and using material such as $NiSi_2$ (discussed in chapter 6) which has 10^2 higher on/off ratio could improve the SS and subthreshold characteristics of the transistor. The effective mobility at high surface carrier concentration was found to be

equal or surpassing the best reported results with HfO_2 as gate dielectric. However, further research on process conditioning to improve the low field mobility with ALD dielectric by optimizing deposition conditions is required.

7.5 References

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Chapter 8 Conclusions

8.1 Conclusions of This Study

In this thesis, various problems related to the high-*k*/InGaAs interface engineering described in chapter 2, are experimentally investigated and effective solutions to those problems are proposed. .

In Chapter 8, the results and summary of the studies in this thesis is and their importance on improving high-*k*/InGaAs interface is described.

a) Gate Stack Engineering for InGaAs-based MOS Capacitors with La_2O_3 Gate Dielectric (Chapter 4)

In chapter 4, the interface issues of HfO_2/InGaAs were investigated. An experimental solution to suppress and compensate for the defects created at the interface was proposed. In depth electrical characterizations were carried out to identify the carrier trapping mechanisms of these defects and their effect on electrical characteristics of HfO_2-based InGaAs MOS capacitors. The main findings of this chapter are summarized below.

(1) Thermal treatment of HfO_2/InGaAs gate stacks result in the formation of void-like defects at InGaAs substrate. These voids which have lighter density than the substrate are caused by out-diffusion of substrate elements, especially In, into the dielectric.

(2) Increasing substrate temperature during initial HfO_2 layer deposition, reduces the void formation at the interface by supplying In, Ga, As elements from the bulk of the substrate. The reduction of defects, lead to improved *CV* characteristics with less frequency dispersion and lower interface state density.

(3) Multi-temperature admittance measurements revealed that void-like defects at HfO_2/InGaAs interface, act as depletion centers that cause parasitic capacitance in accumulation condition contributing to frequency dispersion in accumulation condition. The energy level of these defects within InGaAs band gap, correspond to the energy level created by missing In atoms.

(4) An amorphous high-*k* dielectric or interfacial layer is required, to effectively prevent the void formation at the bulk of InGaAs.

b) Gate Stack Engineering for InGaAs-based MOS Capacitors with HfO_2 Gate Dielectric (Chapter 5)

In chapter 5, La_2O_3 as gate dielectric for InGaAs was experimentally investigated. The fundamental properties of La_2O_3/InGaAs were manipulated and controlled to achieve high quality and ultra-thin La_2O_3/InGaAs gate stacks with very low density of interface states. The main findings of this work are summarized below.

(1) It was found that an amorphous interfacial layer (IL) is formed at La_2O_3/InGaAs interface. This IL is created due to reactive intermixing of In and Ga from the substrate with La_2O_3 and creating a structure in the form of $LaInGaO_x$. The thickness and composition of this IL, however, needs to be carefully controlled to prevent excessive increase of interface state density and capacitance equivalent thickness (CET). Three approaches were investigated to address this issue. (a) Application of a mono-layer Si passivation method, (b) applying La-silicate structure at La_2O_3/InGaAs interface, and (c) controlling the formation of IL through gate metal selection

(2) A mono-layer Si passivation method by using vapor hexamethyldisilazane

(HMDS) was found to be effective for reducing interface state density W/La_2O_3/InGaAs MOS capacitors and improving its overall electrical characteristics by preventing As oxide species.

(3) InGaAs-based MOS capacitors with lowest reported CET (0.65 nm) and small interface state density (~10^{12} $eV^{-1}cm^{-2}$) were fabricated by using La-silicate as gate dielectric. A thin Nitridated Si layer (1.0 nm) was deposited at La_2O_3/InGaAs interface in order to form La-silicate structure. High k-value of ~19, which is much higher than conventionally used Al_2O_3 k-value ~9, was obtained through careful process control. The high quality amorphous nature of La-silicate layer, drastically improved the thermal stability of gate stack up to 620^oC. La-silicate application in gate-last processes where annealing temperature around 600^oC for SD activation is required can be expected.

(4) Formation of $LaInGaO_x$ IL at La_2O_3/InGaAs interface is triggered by diffusion of oxygen through the gate metal electrode. It was found that composition and thickness of $LaInGaO_x$ can be improved by reducing W gate electrode thickness and capping it with TiN. Record low mid gap interface state density (~8×10^{11} $eV^{-1}cm^{-2}$) with excellent thermal stability was achieved for TiN/W/La_2O_3/InGaAs MOS capacitors.

c) Technologies for 3D structure InGaAs-based devices (Chapter 6)

In chapter 6, atomic layer deposition (ALD) method with ($La(^{i}PrCp)_3$ and H_2O) for La_2O_3 film synthesis, as well as a non-alloyed $NiSi_2$/InGaAs contacts were investigated. These technologies are expected to be necessary for transition of InGaAs from bulk to other device structures in short gate lengths. The main findings of this work are summarized below.

(1) It was shown that near ideal *CV* characteristics with low density of interface state ($\sim 9\times10^{11}$ $eV^{-1}cm^{-2}$) can be obtained for TiN/W/ALD-La_2O_3/InGaAs MOS capacitors. It was found that controlling the substrate temperature (~150^{o}C) during La_2O_3 synthesis was essential for prevention of substrate oxidization during deposition.

(2) A multi stack structure composed of Ni and Si layers was proposed to form $NiSi_2$ on InGaAs substrate at a relatively low temperature (400^{o}C). It was found that $NiSi_2$/InGaAs contact is not alloyed even at annealing temperature as high as 600^{o}C which is in contrast to widely used Ni/InGaAs contact. XPS, TEM and AFM analysis showed that $NiSi_2$ film morphology remains constant up to 600^{o}C. The diode electrical

characteristics of $NiSi_2$/InGaAs showed roughly 10 times higher (10^6) on/off ratio than Ni/InGaAs. This type of non-alloyed contact can be applied to SD regions in short channel 3D structures where SD interaction with channel region needs to be minimized.

d) InGaAs-based MOSFETs with La_2O_3 as gate dielectric (Chapter 7)

In chapter 7, InGaAs MOSFET operation with Ni as metal SD and La_2O_3 as gate dielectric was demonstrated. Effective electron mobility at high surface carrier concentration region (N_s: 9×10^{12} cm^{-2}) was comparable to reported HfO_2-based InGaAs MOSFETs at CET ~ 1.0 nm.

8.2 Prospects for Further Study

Based on the results of this study, further research topics for InGaAs high-*k*/metal gate stacks with La_2O_3 as gate dielectric is proposed.

Sulfur passivation is used as a common substrate cleaning step for InGaAs substrate before high-*k* deposition. This approach is applied throughout this study as well. Although the process condition for sulfur passivation is optimized in this study, a clear mechanism of Sulfur atoms in regard to the reactive interfacial layer of $LaInGaO_x$ after thermal treatment of La_2O_3/InGaAs is unclear. Taking advantage of chemically activated ALD process together with the formation of $LaInGaO_x$ interfacial layer, might altogether render the use of sulfur passivation for InGaAs high-*k*/metal gate stacks with La_2O_3 as gate dielectric completely unnecessary. This in turn would have great implications on industrial point of view for InGaAs-based devices.

Given the superior interface quality of La_2O_3/InGaAs interface, it is possible to achieve MOSFET operation with better results than those of reported for Al_2O_3-based InGaAs MOSFETs. Low subthreshold value (~60mV) is necessary to utilize low power/high performance benefits of InGaAs-based devices. Further process optimization of ALD-deposited La_2O_3 is necessary to improve subthreshold value and

achieve high mobility in gate stack with smaller equivalent oxide thickness

In conclusion, the reactive interfacial layer at high-*k*/InGaAs interface and non-alloyed metal/InGaAs concepts proposed in this thesis, could provide useful guidelines for high-quality high-k/metal gate systems on InGaAs platform leading to high-performance and low-power MOSFETs. The dielectrics used in this thesis and extracted MOS characteristics are summarized in the following table.

MOSCAP / Dielectric	*Interface State Density (D_{it}) $cm^{-2}eV^{-1}$ (E-Ei=0.1eV)	**Capacitance Equivalent Thickness (nm)	***Thermal Stability (°C)
(1)EB-HfO_2	1×10^{13}~	~ 1.5	~ 400
(2)Enhanced EB-HfO_2	5×10^{12}~	~ 1.0	~ 470
La-silicate	2×10^{12}~	~ 0.73	~ 620
EB-La_2O_3	7×10^{11}~	~ 0.78	~ 620
(3)ALD-La_2O_3	9×10^{11}~	~ 1.2	~ 470

(1) Electron beam deposition
(2) Deposited at 300 °C
(3) Atomic Layer Deposition

* Lowest interface at smaller CET
** Extracted from 100 kHz CV curve at leakage current < 0.1Acm^{-2}
*** Maximum post metallization annealing temperature for leakage current <0.1Acm^{-2}

Publications and Presentations

Peer Reviewed International Journals (fist author)

1- D. H. Zadeh, H. Oomine, Y. Suzukia, K. Kakushima, P. Ahmet, H. Nohira, Y. Kataoka, A. Nishiyama, N. Sugii, K. Tsutsui, K. Natori, T. Hattori, H. Iwai "$La_2O_3/In_{0.53}Ga_{0.47}As$ metal–oxide-semiconductor capacitor with low interface state density using TiN/W gate electrode" *Solid-State Electronics*, vol. 82, p. 29, 2013.

2- D. Zade, T. Kanda, K. Kakushima, K. Yamashita, P. Ahmet, K. Tsutsui, A. Nishiyama, N. Sugii, K. Natori, T. Hattori, H. Nohira and H. Iwai "Capacitance-Voltage characterization of La_2O_3 metal-oxide-semiconductor structures on $In_{0.53}Ga_{0.47}As$ substrate with different surface treatment methods" *Japanese Journal of Applied Physics* 50, 10PD03, 2011.

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Invited Talk

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