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| 著者(和文) | LeeHyunui |
| Author(English) | Hyunui LEE |
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# Study of Multi-Stage Analog to Digital Converters using Interpolation Technique

A PhD Dissertation by

Hyunui Lee

in partial fulfillment of the requirements for the degree of

Doctor of Philosophy (Ph.D.)

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TOKYO INSTITUTE OF TECHNOLOGY
GRADUATE SCHOOL OF SCIENCE AND ENGINEERING
DEPARTMENT OF PHYSICAL ELECTRONICS

*To my family*

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## Abstract

In this thesis, design and analysis of multi-stage ADCs using interpolation technique are proposed. The interpolation technique is very effective to realize high-speed and high-resolution ADC using recent scaled technology. By introducing the interpolation technique, the multi-stage ADC does not require a high-gain amplifier which is a bottleneck of high-resolution ADC design. As a result, the ADC becomes free from large amount of calibrations to compensate non-idealities caused by insufficient amplifier's gain.

As an implementation method for the interpolation, CDAC and RDAC in subranging ADC are compared in settling time, power consumption, and noise. Since CDAC shows better performance, it is utilized to ADCs in the thesis. Also, mismatch analysis on CDAC is performed for ADC design. Furthermore, effect of gate-weighted interpolation technique to ADC's performance, such as comparator's offset calibration ability at each interpolation point are examined. The subranging ADC using CDAC and gate-weighted interpolation technique achieves FoM of 250 fJ/conv., which is the world lowest result. And, a new interpolation method to reduce CDAC in half is suggested. These analyses become basics for multi-stage ADC design using interpolation.

Extension of ADC's resolution from subranging ADC, interpolated pipeline ADC is designed and analyzed. In the interpolated pipeline ADC, the most important characteristic for amplifier is linearity, not gain. In this thesis, relation between amplifier's linearity and the ADC's performance is analyzed. Also, effect of MDAC stage's noise, mismatch between amplifiers, ADC's optimized operation frequency with amplifier's current are analyzed. And, optimized 1st stage resolution in each ADC is suggested. A 12-bit interpolated pipeline ADC based on the previous analysis and body voltage controlled amplifier for low-power consumption and wide output swing range is demonstrated. The 12-bit ADC achieves 10-bit of ENOB at 300 MS/s with low-frequency input. The result is competitive with other top-performance 12-bit ADCs although the proposed ADC does not incorporate MDAC calibration and any kind of special process and layout technique.

In this thesis, three types of amplifiers are introduced for interpolated pipeline ADC design, such as source degeneration, cascode (body voltage control), and gm-cell. Also, Open- and closed-loop topologies are utilized to the ADC design. The performance comparison of those proposed topologies are shown in this thesis to choose the suitable topology for various ADC target specifications. Finally, this thesis is concluded with prospection of interpolation technique and relationship between interpolation and calibration techniques.

## List of Abbreviations

| | | |
|---|---|---|
| ADC | : | Analog to Digital Converter |
| ADSL | : | Asymmetric Digital Subscriber Line |
| BIST | : | Built-In Self Test |
| BOST | : | Built-Out Self Test |
| BW | : | Band Width |
| CAL | : | Calibration |
| CD | : | Compact Disc |
| CDAC | : | Capacitive Digital to Analog Converter |
| CMFB | : | Common-Mode Feedback |
| CMOS | : | Complementary Metal-Oxide Semiconductor |
| CT | : | Continuous-Time |
| DAC | : | Digital to Analog Converter |
| DNL | : | Differential Nonlinearity |
| DSP | : | Digital Signal Processing |
| DT | : | Discrete-Time |
| DVD | : | Digital Versatile Disk |
| ENOB | : | Effective Number of Bit |
| FFT | : | Fast Fourier Transform |
| FoM | : | Figure of Merit |
| $F_S$ | : | Sampling Frequency |
| FVF | : | Flipped Voltage Follower |
| GSM | : | Global System for Mobile communications |
| GS/s | : | Giga Sample Per Second |
| HDD | : | Hard Disk Drive |
| IF | : | Intermediate Frequency |
| IP | : | Interpolation |
| INL | : | Integral Nonlinearity |
| ITRS | : | International Technology Roadmap for Semiconductors |
| LMS | : | Least Mean Square |
| LNA | : | Low Noise Amplifier |
| LPE | : | Layout Parasitic Extraction |
| LSB | : | Least Significant Bit |
| MD | : | Mini Disc |
| MDAC | : | Multiplying Digital to Analog Converter |
| MIFG | : | Multiple Input Floating Gate |
| MIM | : | Metal-Insulator-Metal |

| | | |
|---|---|---|
| MOS | : | Metal-Oxide Semiconductor |
| MSB | : | Most Significant Bit |
| MS/s | : | Mega Sample Per Second |
| NA | : | Not Announced |
| NMOS | : | N-channel Metal-Oxide Semiconductor |
| OTA | : | Operational Transconductance Amplifier |
| OP-AMP | : | Operational Amplifier |
| PCB | : | Printed-Circuit Board |
| $P_D$ | : | Power Dissipation (consumption) |
| PMOS | : | P-channel Metal-Oxide Semiconductor |
| PVT | : | Process-Voltage-Temperature |
| RDAC | : | Resistive Digital to Analog Converter |
| RF | : | Radio Frequency |
| RNMC | : | Reversed Nested Miller Compensation |
| SAR | : | Successive Approximation Register |
| S/H | : | Sample and Hold |
| SC | : | Switched Capacitor |
| SFDR | : | Spurious Free Dynamic Range |
| SNDR | : | Signal to Noise and Distortion Ratio |
| SNR | : | Signal to Noise Ratio |
| SoC | : | System on Chip |
| THD | : | Total Harmonic Distortion |
| TI | : | Time-Interleaved |
| T/H | : | Track and Hold |
| TV | : | Television |
| $V_{DD}$ | : | Supply Voltage |
| $V_{GS}$ | : | Gate-Source Voltage of transistor |
| $V_{TH}$ | : | Threshold Voltage of transistor |
| VDSL | : | Very high bit-rate Digital Subscriber Line |
| W/L | : | Aspect Ratio |
| WLAN | : | Wireless Local Area Network |

# Table of Contents

# 1. Introduction

## 1.1 Research Background

It has been almost 10 years passed after turning of the 20th century. At this point, the semiconductor technology downscaling is still progressing. Even though Moore's Law [1.1] - [1.2] - which indicates that the density of transistors in the microprocessor has doubled every 18 months - is looked like to close the limit, the technology downscaling seems continuing for a while. By the diminution of the channel length of the transistor, the digital circuit benefits many points, such as core area, degree of integration, and processing speed. As a result, the digital circuit has been substitute many function of the analog circuit in the SoC and the DSP, because high-integration becomes the most important characteristic of the recent developed SoC.

On the contrary, the analog circuit suffers from decrease of the transistor's intrinsic gain and reduced supply voltage, which are caused by the technology downscaling. For low-cost and highly-integrated SoC realization, the analog and the digital circuits have to be fabricated in the same technology (wafer). Therefore, the problems by the technology downscaling cannot be avoidable to the analog circuits, and it causes increase of difficulty of the analog circuit design. The simplest way to solve this problem is substitution of the analog circuit to the digital circuit as much as possible. However, even though the digital circuits occupy the traditional analog signal process domain, some analog circuits are not alternative due to its unique functionality. Among the analog circuits, the ADC is one of the most important circuits because it realizes the interface between the real world (analog domain) and the digital world (digital domain) as shown in Figure 1.1. The ADC has to be placed in many applications, such as image processing, communication system, measurement instrument, and consumer electronics.

Due to the analog circuit and the digital circuit are designed in the same technology for low-cost and highly-integrated SoC, performance requirement to the analog circuit has been increasing because the digital circuit is getting better and better by the technology

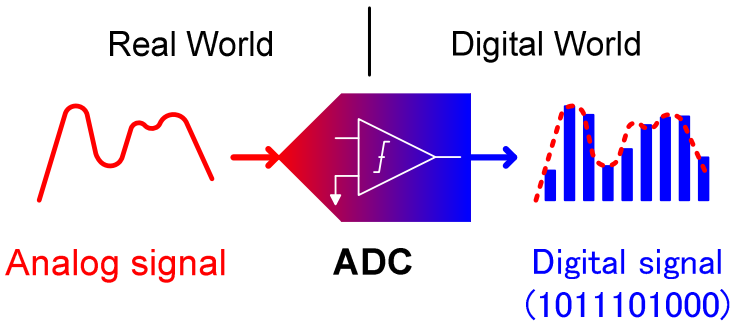


Figure 1.1 Concept of analog to digital conversion.

downscaling. For the ADC, the performance requirement is different by the application. For example, the communication system for radio station requires high-resolution and high-speed ADC to realize high order modulation. On the other hand, the mobile communication system requires low-power consumption and small core area due to limited space and battery operation.

Figure 1.2 shows the ADC performance and ADC topologies in terms of ADC's resolution and sampling frequency [1.3]. In Figure 1.2, the subranging ADC and the pipeline ADC can be categorized in multi-stage ADC because they are consisted of series connected multiple-stages. According to Figure 1.2, the multi-stage ADC covers from 6 to 12-bit resolution and from several MS/s up to GS/s. The multi-stage ADC's specific applications are depicted as HDD and DVD (disc read channel), VDSL and ADSL (communication system), and digital TV and digital camera (consumer electronics). Detailed block diagrams of the application will be shown in the following sub-chapter.

Figure 1.3 shows detailed categorization of ADC's resolution vs. sampling frequency in terms of ADC topologies. According to Figure 1.3, the subranging ADC covers from several tens to hundreds MS/s and until 8-bit resolution. On the other hand, the pipeline ADC can be utilized for 8 to 12-bit resolution and from several tens MS/s to several GS/s. Figure 1.3 is a guideline to choose a suitable ADC topology for their target specification. However, the categorization in Figure 1.3 is not a mandatory. Recently, the boundary in Figure 1.3 is collapsed by several techniques. For example, in [1.4], a 10-bit two-step (similar to subranging) ADC is presented with high-precision comparator. Also, improved timing calibration technique allows using of multiple-interleaving and it increases sampling frequency of the ADC even the single channel of the ADC operates in low-speed. As a result, a

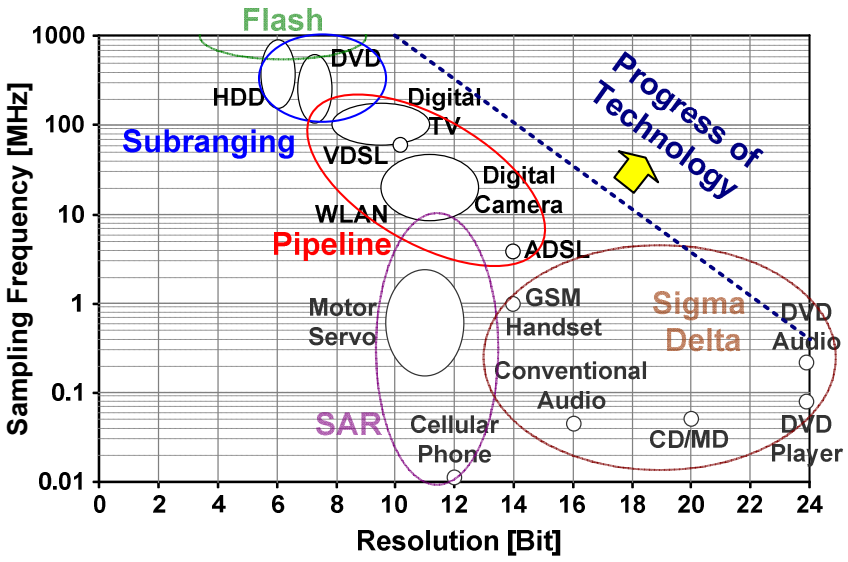


Figure 1.2 Recent ADC performance needs for important product classes.

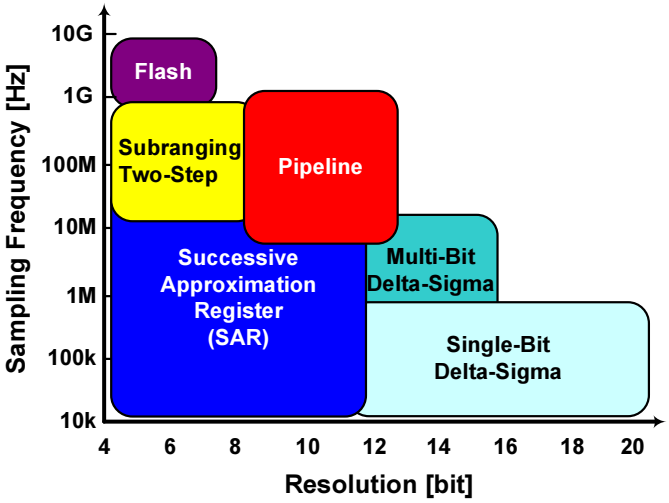


Figure 1.3 Resolution vs. sampling frequency in terms of ADC topologies.

2.8 GS/s SAR ADC [1.5] is realized by 24-way time interleaving using 120 MS/s single channel ADC.

## 1.2 High-speed / Medium to High-resolution ADC Application

A disk drive system is an example of the high-speed medium-resolution ADC application. Figure 1.4 shows a block diagram of the disk read channel path. As storage density of the disk and the read channel operation speed is increased, the speed and the resolution requirements to the ADC are also increased. Also, increased data storage requires high dynamic range of the ADC. Therefore, increasing ADC's speed and resolution are very important for the disk drive system.

High-speed and medium to high-resolution ADCs are desired in many applications; for example, communication system and disk drive front-end. Figure 1.5 shows super-heterodyne receiver architecture. This kind of system uses down-conversion signal processing which relaxes the ADC's performance requirement because the signal processing is performed in the baseband frequency domain. However, this kind of system is not suitable for the recent communication system because the system requires large area due to some

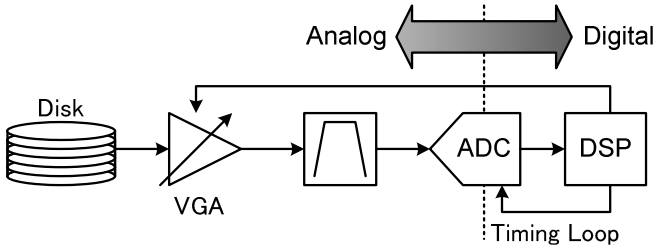


Figure 1.4 Disk read channel path.

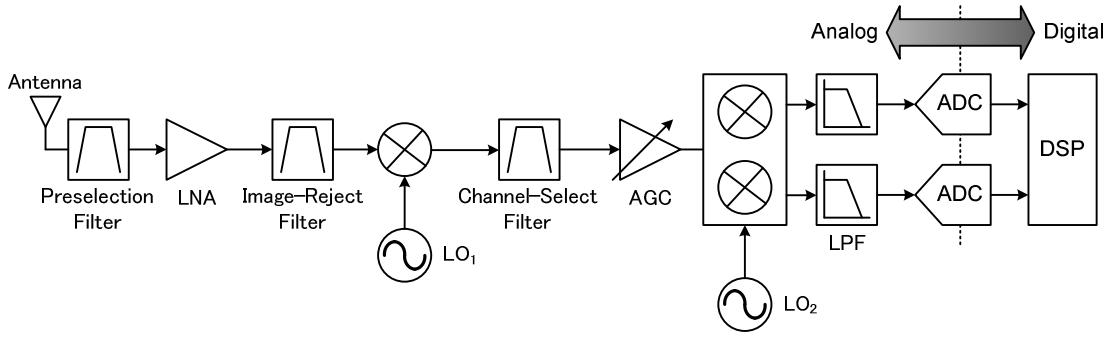


Figure 1.5 Conventional super-heterodyne receiver architecture.

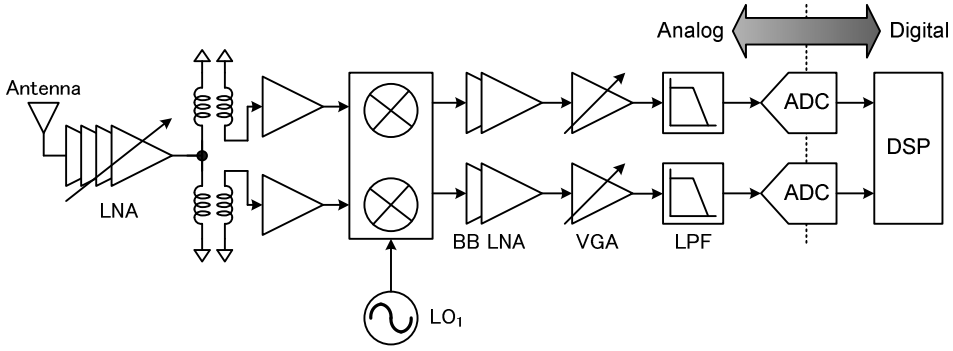


Figure 1.6 60 GHz direct-conversion receiver architecture.

components, such as image-reject filter. On the other hand, the direct conversion receiver can be realized in smaller area because there is no image-reject filter. Figure 1.6 shows an example of 60 GHz direct conversion receiver architecture. Even though the direct conversion system can save the core area, high-speed ADC is required for direct IF signal conversion and it makes the ADC design difficult.

## 1.3 ADC Design with Scaled CMOS Technology

The improvement of the CMOS technology scaling pushes the recent SoC to high-integration. Also, advance of the mobile system drives SoC towards low-supply voltage system. These recent CMOS technology trends (high-integration and low-supply voltage) benefit for the SoC in small core area and low-power consumption.

In the SoC, the digital circuit has benefits by the recent CMOS technology improvements, which mean the digital circuit becomes smaller, faster, and more energy efficient. However, these trends cause severe problems to the analog circuit. For example, scaled CMOS technology reduces transistor's intrinsic gain. The reduced transistor's intrinsic gain is a crucial for some analog circuits which require high-gain amplifier. Also, reduced supply voltage makes difficult to maintain analog circuit's precision because the signal range is shrunk.

Figure 1.7 shows the CMOS technology scaling roadmap for the high-performance

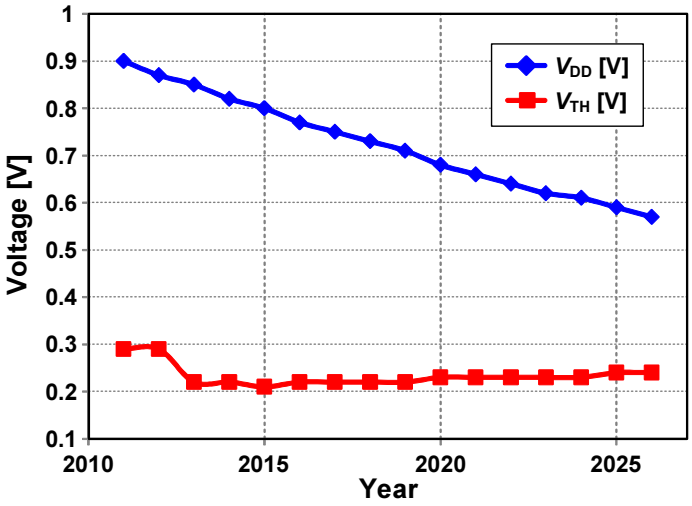


Figure 1.7 CMOS technology scaling roadmap for high-performance logic [1.6].

logic technology, as predicted by ITRS [1.6]. As shown in Figure 1.7, supply voltage is expected to reduce from 0.9 V to 0.55 V through 15 years. Because SNR of the analog circuit is proportional with the supply voltage, it is expected that the SNR also reduced with supply voltage. The transistor's threshold voltage ($V_{th}$) makes this problem more crucial. As shown in Figure 1.7, even though the supply voltage is reduced, the threshold voltage is barely changed. For the proper analog circuit operation, transistor has to secure overdrive voltage ($V_{gs}$- $V_{th}$) as voltage headroom. Therefore, almost constant $V_{th}$ is another reason of poor SNR in the recent scaled CMOS technology. To maintain SNR with scaled CMOS technology, additional circuit technique is required, such as calibration circuit which is introduced in the following chapter.

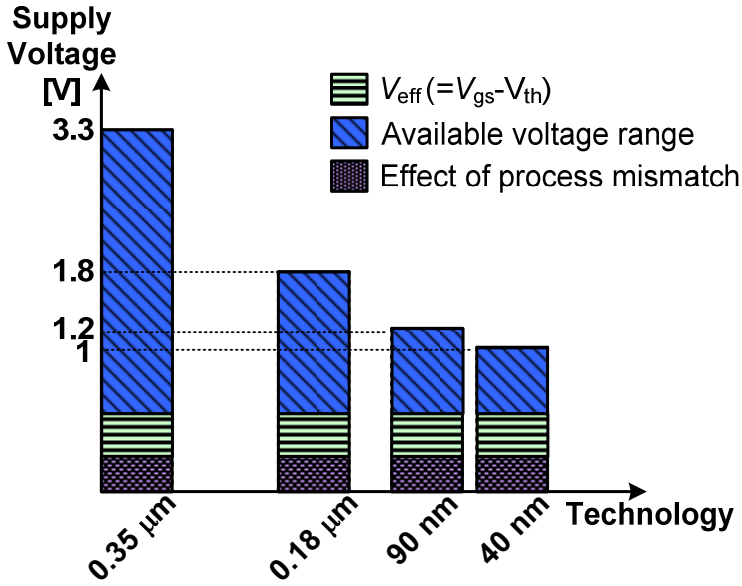


Figure 1.8 Supply voltage with technology scaling.

Figure 1.8 shows the CMOS technology vs. the supply voltage. According to Figure 1.8, the supply voltage is decreased with the technology scaling. For example, the supply voltage is 3.3 V with 0.35 μm technology. However, the supply voltage is decreased to 1 V when the technology is scaled down to 40 nm. As described in above paragraph, the threshold voltage almost constant during the recent technology downscaling. Therefore, the overdrive voltage ($V_{eff}$), which is necessary for the analog circuit operation, is also constant. Furthermore, the signal swing margin for the process mismatch also does not reduced, because the mismatch characteristic is not improved in the recent scaled technology. According to the above reasons, available signal swing is reduced and it decreases the SNR of the ADC.

Figure 1.9 shows transistor's drain-source voltage ($V_{DS}$) vs. early voltage ($V_A$) with several CMOS technologies. The relationship between $V_A$ and the transistor's gain ($G$) can be defined as below,

$$G = \frac{2 \cdot V_A}{V_{eff}}. \tag{1.1}$$

In (1.1), $V_{eff}$ means overdrive voltage the same as chapter 1.3. According to (1.1), $V_A$ has a proportional relationship with $G$. Therefore, to realize the high gain circuit, large $V_A$ is mandatory. However, $V_A$ is also decreased with the technology scaling as shown in Figure 1.9. Therefore, design of high-gain circuit in scaled technology is very tough challenge. For example, a cascode amplifier using 350 nm technology at $V_{DS}$ of 0.3 V can achieve 52-dB gain. When the technology is scaled to 90 nm, the gain is reduced to 40-dB at the same amplifier topology and $V_{DS}$ voltage.

For the reason of the described problems above, the design of high-speed and high-resolution ADC becomes difficult in recent scaled process. Especially higher than 10-bit resolution ADC, the ADC realization using traditional circuit architecture without error

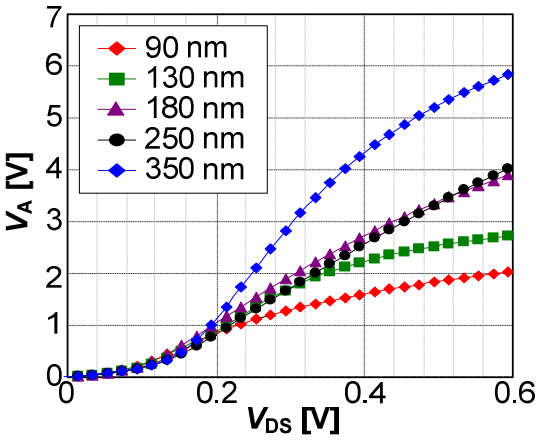


Figure 1.9 $V_A$ vs. $V_{DS}$ in several technologies.

correction (calibration) technique is almost impossible. As a result, the calibration circuit becomes essential for the recent ADC design. However, the calibration circuit increases the core area and the power consumption. Also, complex calibration logic needs long calibration time which increases the test cost. Therefore, high-speed and high-resolution ADC design without calibration is one challenge in recent ADC development. The calibration techniques are explained in the following chapter.

## 1.4 Research Purpose

The main purpose of this research is a proof of practicability of interpolation technique by realization of high-speed and high-resolution ADC using recent scaled technology. To achieve this purpose, three steps of research are proposed.

1. Performance analysis on ADC using the interpolation technique.
2. Design of ADC using the interpolation technique based on analysis of step 1.
3. Performance verification of designed ADC in comparison of other recent published ADCs.

Through these three steps, it is expected that the practicability and the effectiveness of the interpolation technique for ADC design are verified.

## 1.5 Organization of Thesis

This paper is organized in 8 chapters. This chapter presents the overview of the ADC topologies and applications. Also, this chapter describes the characteristics of the recent scaled technology and how those problems affect to the recent ADC design.

Chapter 2 will explain the interpolation technique. Because the interpolation technique is incorporated to ADCs in this research as the key-technique, it is better to draw principle and characteristic of the interpolation technique before introducing the proposed ADCs. The interpolation technique has been developed for a long time and used in many applications including ADCs. The implementation examples of the interpolation are shown first. Also, the usage of the interpolation in ADC design is shown. After that, the characteristic of the pipeline ADC using interpolation technique is explained with comparison of the conventional pipeline ADC structure. And, calibration techniques for recently developed high-resolution ADCs are introduced. The principle, examples, pros and cons of calibration technique explains trend of the recent ADC design and suggests what is necessary to improve the ADC performance in the future development.

Chapter 3 will present a 6-bit subranging ADC using interpolation technique. Introducing interpolation technique to the subranging architecture brings several advantages, such as elimination of S/H circuit and consistence of the signal range between

the fine and the coarse stages. In chapter 3, the comparison of CDAC and RDAC is shown in settling time, power consumption, and noise. Also, effect of the CDAC's mismatch to the ADC's performance and the characteristic of the offset calibration with interpolation technique are explained. The chapter also includes circuit implementation and measurement results.

Chapter 4 will present another 6-bit subranging ADC with new interpolation technique. The previous interpolation method (in chapter 3) utilizes two CDAC, which causes large core area and high-power consumption. The proposed ADC in chapter 4 utilizes only one differential signal and two DC voltages to realize the interpolation. Therefore, the CDAC can be reduced in half. Consequentially, the core area and the power consumption are reduced. The principle of the new interpolation technique and the proposed ADC using new interpolation technique will be explained in chapter 4. Also, simulation results and caution in ADC design will be shown.

Chapter 5 will address design of the interpolated pipeline ADC using low-gain open-loop amplifier. By introducing the interpolation technique, high-gain amplifier is not required for the high-resolution pipeline ADC design. In the interpolated pipeline ADC design, the amplifier's linearity becomes crucial than the amplifier's gain. In chapter 5, the issues of the interpolated pipeline ADC are introduced first. Also, the effect of the amplifier's characteristics to the ADC's performance is described, especially the linearity. After that, the MDAC stage's noise characteristic is examined. The ADC's operation speed and ENOB degradation with the amplifier's current is analyzed. The performance comparison with the multi-bit pipeline ADC is also suggested. Lastly, the determination of the pipeline stage resolution and design flow is suggested to help the interpolated pipeline ADC design.

Chapter 6 will present a 12-bit, 300 MS/s interpolated pipeline ADC using body voltage controlled amplifier. Basically, the ADC has the same structure as the interpolated pipeline ADC in chapter 5. However, the low-gain open-loop amplifier such as SD amplifier cannot be accepted to the 12-bit resolution due to the linearity issue. To address the linearity issue, the proposed ADC utilizes a cascode amplifier with feedback loop. A body voltage controlled amplifier is proposed to low-power consumption and wide output swing range. Chapter 6 also includes the simulation results and measurement results of the amplifier and the proposed ADC including analysis of the measurement results.

Chapter 7 will present a 12-bit, 200 MS/s, 600 MHz input frequency interpolated pipeline ADC using $g_m$-cell. By introducing the $g_m$-cell, the linearity requirement is satisfied without feedback loop. The schematic and the operation of the $g_m$-cell and the ADC are introduced. Also, the simulation results of the ADC are shown in the chapter. Chapter 7 discusses amplifier usages (open-loop and closed-loop) and amplifier topologies (SD amplifier, body voltage controlled amplifier, $g_m$-cell) to make clear that what is the most suitable topology for interpolated pipeline ADC.

Chapter 8 will concludes the thesis with the prospect of the interpolation technique and the future relation of the interpolation technique and the calibration technique.

Appendixes will provide explanations of the formulas in which introduced in the thesis. It consists of the derivation of the effect of the CDAC's gain degradation to the subranging ADC's performance; the derivation of the comparator's offset with input common-mode voltage level, and the derivation of the ENOB calculation in the interpolated pipeline ADC structure. Also, the measurement results of the temperature variation using 10-bit interpolated pipeline ADC is shown to prove the robustness for the temperature variation.

The important issues and solutions in each chapter of this thesis are described in the Figure 1.10 except the introduction and conclusion.

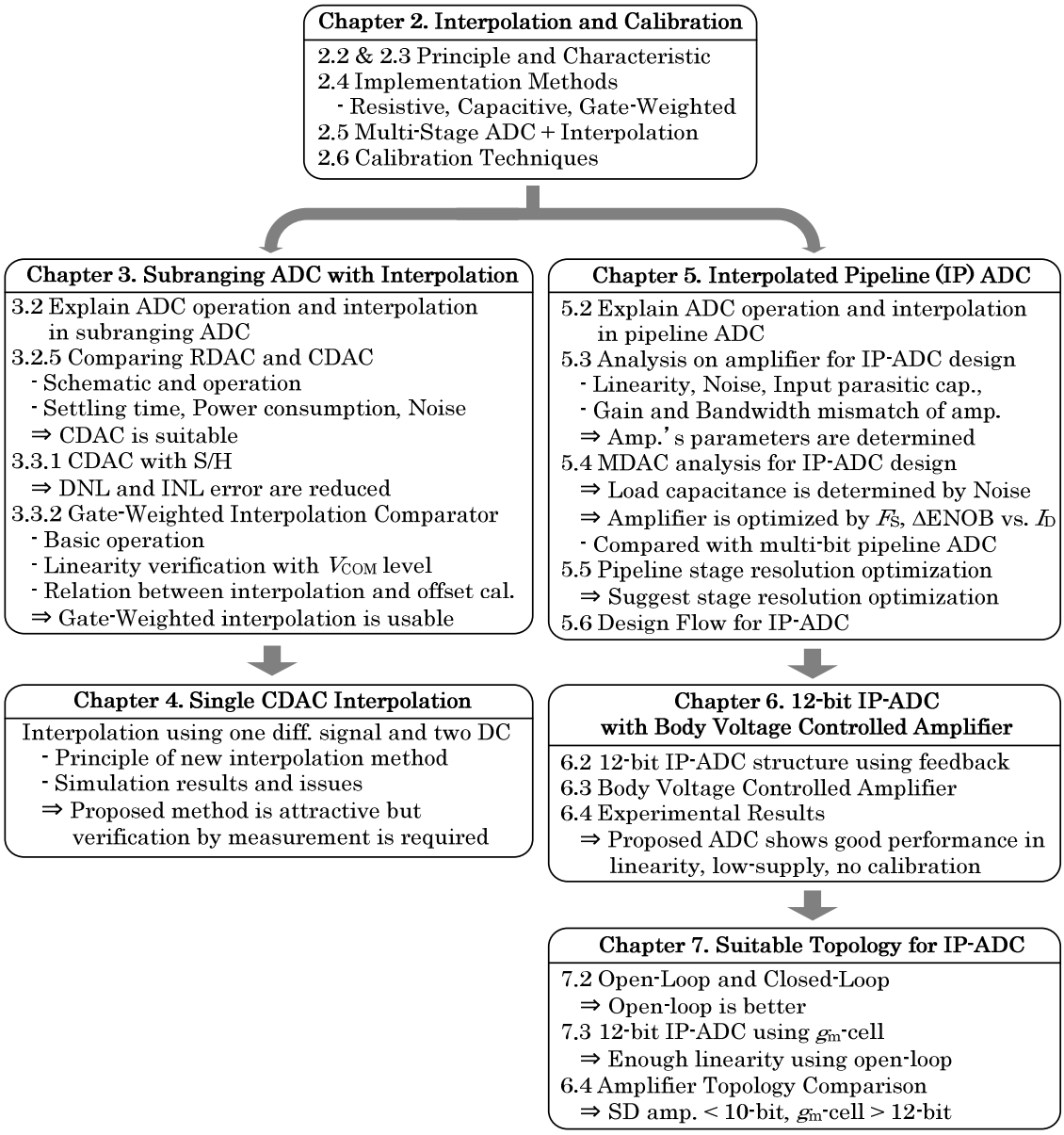

Figure 1.10　Composition of the thesis.

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# 2. Interpolation and Calibration Techniques

## 2.1 Introduction

The interpolation technique has been used in the analog circuit design for a long time. The interpolation technique has many implementation methods and many applications. The ADCs in this research incorporate the interpolation technique as a key-technique to solve the problems which are caused by recent scaled technology.

In this chapter, the principle and the characteristics of the interpolation technique are explained. Also, the representative methods to realize the interpolation are introduced, such as resistive interpolation, capacitive interpolation, and gate-weighted interpolation. After that, the realization of the interpolation in the multi-stage ADC is shown because circuit implementation is different from the conventional pipeline ADC. By virtue of the interpolation technique, high-resolution (> 10-bit) ADC can be realized without calibration circuit. Therefore, to understand the advantage of the elimination of the calibration circuit, the calibration techniques are discussed. For example, principle, examples, pros and cons are explained including test cost.

## 2.2 Principle of Interpolation and Extrapolation Technique

The principle of interpolation and extrapolation is generating new signal by using weight control of source signals. If new signal is generated between source signals, it called interpolation. On the other hand, if new signal is generated outside of source signals, it called extrapolation. The location of the generated signal is determined by the ratio of interpolation (extrapolation). The source signals can be voltage or current. Figure 2.1 shows the conceptual diagram of the interpolation and the extrapolation. In Figure 2.1, the $signal_1$ and the $signal_2$ are the source voltages for the interpolation or the extrapolation. And, $a_1$ ($b_1$) and $a_2$ ($b_2$) means the interpolation (extrapolation) ratio. For example, if the $signal_1$ and the $signal_2$ are interpolated with the ratio of $a_1 : a_2$, the red colored signal can be generated. The location of the interpolated signal can be changed by the $a_1 : a_2$. The same operation can be performed in the extrapolation. The generated signal by the extrapolation is drawn by the blue color in Figure 2.1. The formula of the interpolation and the extrapolation are represented as below,

$$\text{Interpolation} = \frac{\boldsymbol{a}_1 \times \boldsymbol{Signal}_1 + \boldsymbol{b}_1 \times \boldsymbol{Signal}_2}{\boldsymbol{a}_1 + \boldsymbol{b}_1} \tag{2.1}$$

$$\text{Extrapolation} = \frac{\boldsymbol{a}_2 \times \boldsymbol{Signal}_1 - \boldsymbol{b}_2 \times \boldsymbol{Signal}_2}{\boldsymbol{a}_2 - \boldsymbol{b}_2} \tag{2.2}$$

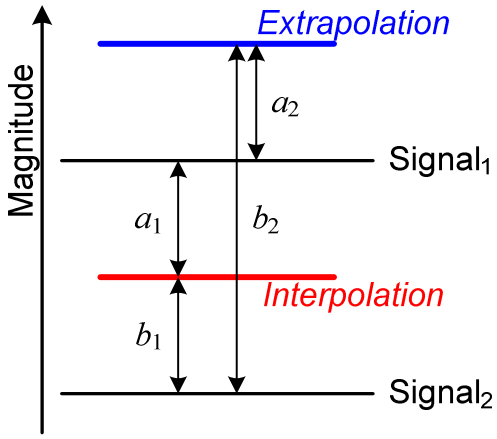



Figure 2.1 Conceptual diagram of interpolation and extrapolation.

In (2.1), the interpolation is realized by addition. However, as shown in (2.2), the extrapolation is realized by subtraction. In the analog circuit design, the addition can be realized by the passive component, such as capacitor or resistor. However, the realization of the subtraction is difficult by the passive components. The subtraction can be realized by the active components, for example, operational amplifier. However, the high-precision subtraction requires high-gain amplifier which is not easy to realize in recent scaled technology. Also, the active component consumes static power, in which increases the power consumption of the system. Therefore, it is reasonable to introduce the interpolation technique to the ADC design.

## 2.3 Characteristics of Interpolation Technique

The interpolation technique has many characteristics, not only advantages but also disadvantages. In this sub-chapter, those characteristics are explained.

### 2.3.1 Reduction of Circuit Components

The interpolation technique has several advantages. One advantage is reduction of the circuit components. Figure 2.2 shows block diagram of a conventional flash ADC. The flash ADC samples the input voltage and compares the sampled input voltage with the reference voltage. Therefore, the conventional flash ADC has an equal number of S/H circuits and reference voltages. To generate reference voltages, resistor ladder is usually used. However, if the circuit incorporates the interpolation technique, the number of the S/H circuits and the reference voltage generators can be reduced.

Figure 2.3 shows the block diagram of the components reduction. As mentioned in chapter 2.2, the interpolation technique can generate a signal using two source signals. This means the reference voltage also can be generated by interpolation technique. In Figure 2.3,

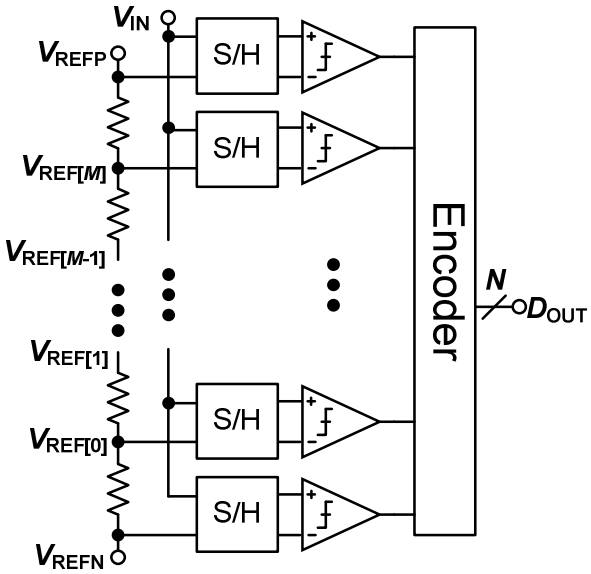



Figure 2.2 Block diagram of flash ADC architecture.

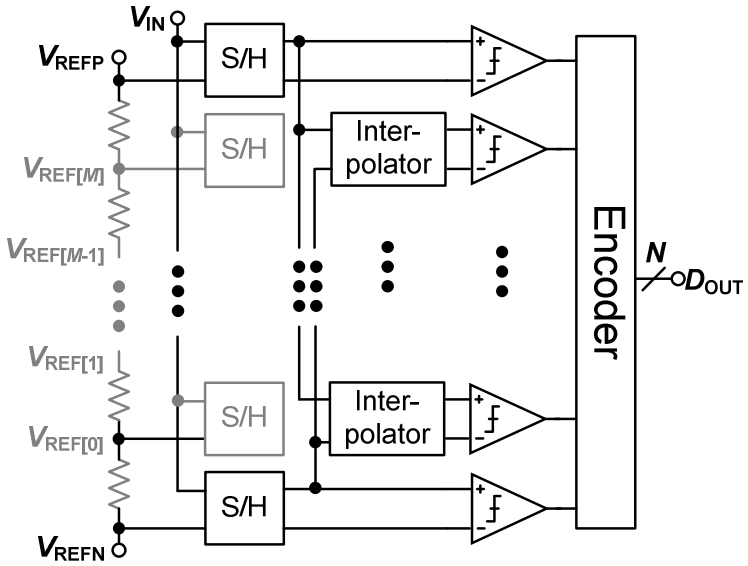



Figure 2.3 Conceptual diagram of components reduction.

the gray colored components are removed components by the interpolation. Assume that the flash ADC in Figure 2.3 has 3-bit resolution. If the flash ADC uses conventional topology, 9 S/H circuits are required. However, by using interpolation technique, the number of S/H circuits can be reduced to only 2. Even though the interpolator circuit is added to the flash ADC, the interpolator does not consume high power. Furthermore, the interpolator can be realized in small area. Therefore, the low-power consumption and small area can be achieved by the interpolation technique by the result of the components reduction.

The interpolation technique has another merit for the sampling capacitance

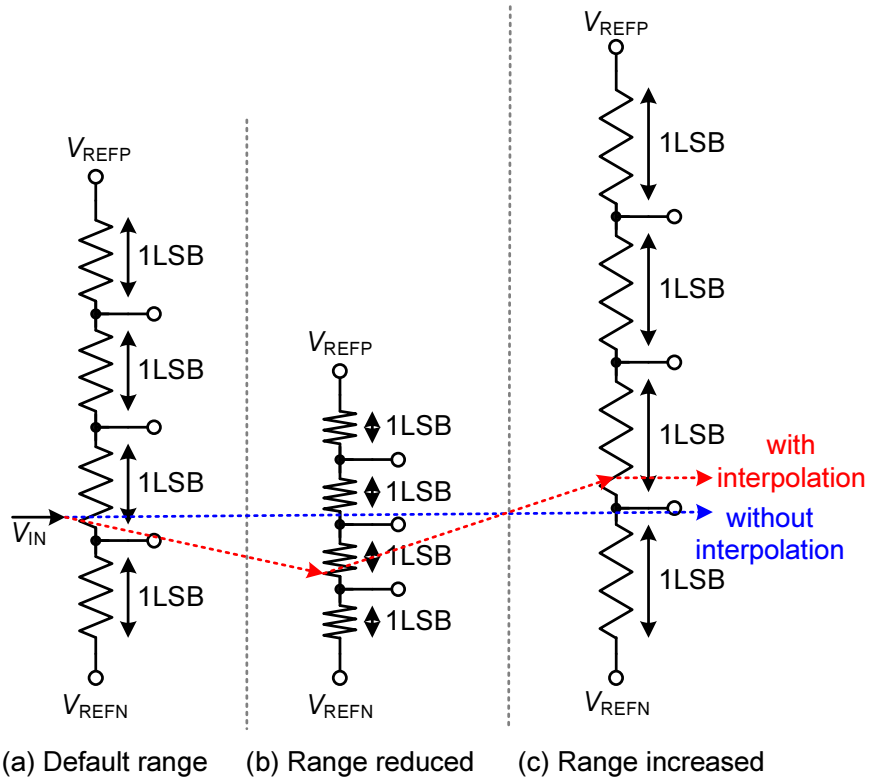



Figure 2.4 Conceptual diagram of mitigation of DNL error.

reduction. Because the numbers of S/H circuits are reduced, the number of sampling capacitors is also reduced. Basically, the total sampling capacitance of the ADC is determined by the number of S/H circuits. Therefore, by introducing the interpolation technique, the total sampling capacitance can be reduced. And, this means that the performance requirement of the ADC input driver is relaxed. However, the sampling capacitance determines the thermal noise and the input signal gain. Therefore, the total sampling capacitance has to be determined with consideration of the effect to the ADC performance.

### 2.3.2 Mitigation of DNL Error

Another merit of the interpolation is the mitigation of the DNL error. There are many reasons of the degradation of the DNL. In this chapter, the DNL degradation by the reference voltage variation is considered.

The ADC usually converts its analog input signal within the reference range. Because the A/D conversion results are determined by the comparison of the input signal and reference voltages, the reference voltage variation causes the A/D conversion error. Especially in the multi-stage ADC, matching of reference range between stages is very important. Because the reference range is different between stages, the A/D conversion result also becomes different even though the analog input is equal. The interpolation technique relaxes the required accuracy for the reference range.

Figure 2.4 shows the conceptual diagram of the reference voltage variation with and without interpolation technique. As shown in Figure 2.4, the conventional comparison makes error when the reference range is changed because it causes the reference voltage variation (also size of LSB). However, by introducing the interpolation technique, the input signal is also changed with the reference range. It means that the A/D conversion result does not depend on the absolute reference voltage. The detailed operation will be explained in later part of this chapter and also in chapter 3. Even though the reference range variation does not become a problem by interpolation technique, the reduced reference range is easily affected by noise and mismatch. Therefore, the signal reduction has to be considered in the ADC design.

### 2.3.3 Interpolation Range

There are several methods to realize the interpolation in circuit design. If the interpolation is implemented by passive components, the interpolation range is not problematic. However, if the interpolation is implemented by active components, such as an amplifier or transistor's size ratio, the interpolation range becomes a problem. Because the interpolation is performed using two source signals, the source signals should not include distortion and nonlinearity which are related with the signal swing range.

Figure 2.5 shows an interpolation example using amplifier's output signal. A flash ADC is depicted as an example in Figure 2.5 (a). The amplifiers are utilized to suppress the

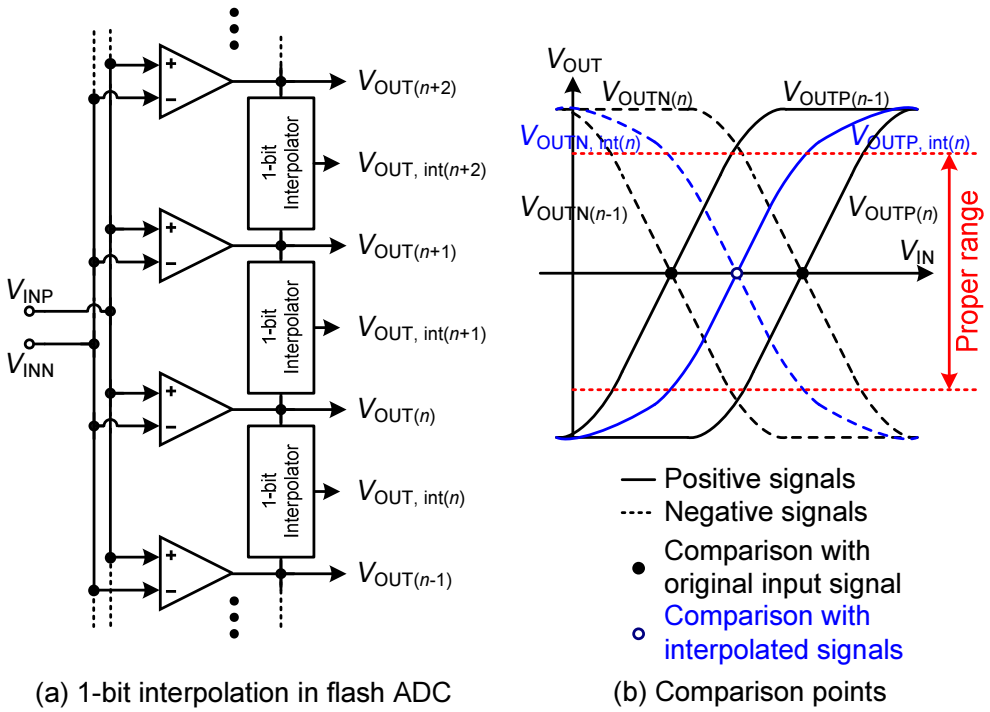



Figure 2.5 Relation with interpolation range and nonlinearity.

offset voltage of the comparators. Because the amplifier's linearity characteristic is inversely proportional with signal swing range, the interpolation has to be performed within proper range. The Figure 2.5 (b) explains this characteristic. If the interpolation is performed output of the proper range, the interpolated signals include distortion and it causes A/D conversion error. The linearity characteristic is different by circuits; therefore, circuit's linearity characteristic and signal range has to be concerned.

## 2.4 Implementation of Interpolation

There are several methods to realize the interpolation. In this chapter, three famous implementation methods are introduced, which are resistive interpolation, capacitive interpolation, and gate-weighted interpolation. More information for those interpolations is included in chapter 3.

### 2.4.1 Resistive Interpolation

The resistive interpolation can be realized by series connected resistors. Figure 2.6 depicts block diagram of the resistive interpolation. In Figure 2.6, the resistive interpolation is implemented with amplifiers. The resistive interpolation is very easy to understand because it just divides two voltages by using series connected resistors. The resolution of the interpolation can be controlled by the number of resistors in the interpolator. The resistor has better mismatch characteristic in comparison with other components; therefore, it can generate more accurate interpolated signals. In addition, if the resistive interpolation is implemented as shown in Figure 2.6, the interpolator averages the amplifiers' mismatch and it increases the ADC's performance. However, the interpolator affects to the output impedance of the amplifier and it causes the amplifier's gain and bandwidth variation. Also, static current in resistive interpolator usually increase the total power consumption of the circuit.

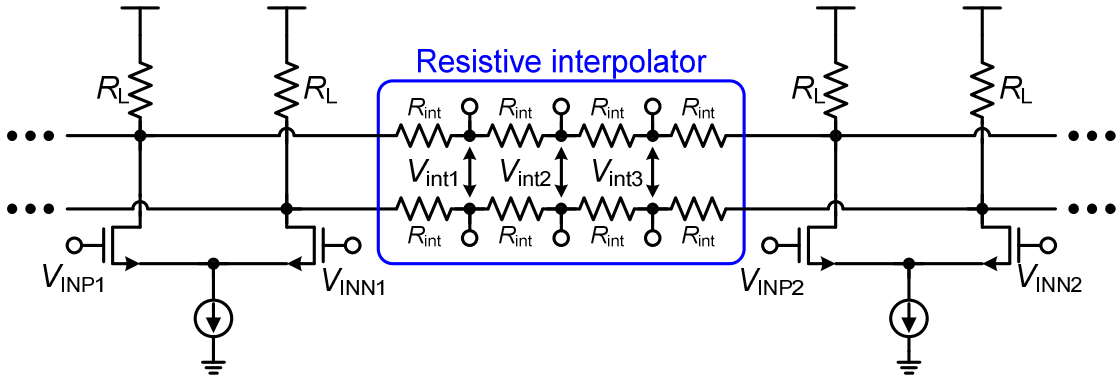



Figure 2.6 Example of resistive interpolation.

### 2.4.2 Capacitive Interpolation

Figure 2.7 [2.1] and Figure 2.8 [2.2] show two examples of the capacitive interpolation. In Figure 2.7, the capacitors divide between two voltages the same method as resistive interpolation. Contrary to the resistive interpolation, multiple stages are necessary to realize multi-bit interpolation. Figure 2.8 shows the interpolation using charge redistribution. The interpolated signal's location (interpolation ratio) is controlled by the ratio of the capacitors which are connected to $V_{REFP}$ or $V_{REFN}$. Basically, the capacitive interpolation requires clock signals to realize interpolation because the circuits utilize capacitors and switches.

There is no static current in the interpolator using capacitors; therefore, the capacitive interpolation can achieve low-power consumption than resistive interpolation. However, circuit implementation is usually complicate due to the increase of the switches and the capacitors. Also, the mismatch between capacitors and the signal coupling by parasitic capacitance should be checked carefully.

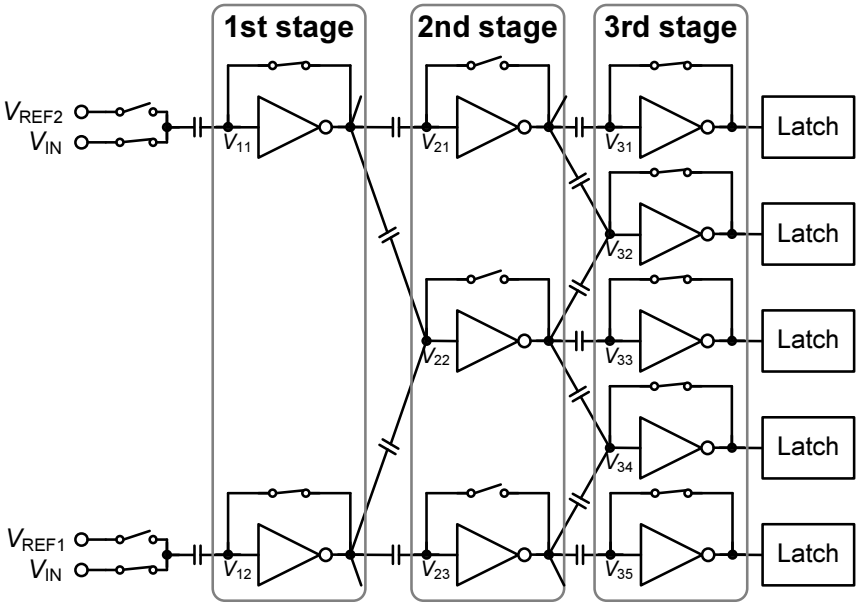



Figure 2.7 Example of capacitive interpolation using voltage division [2.1].

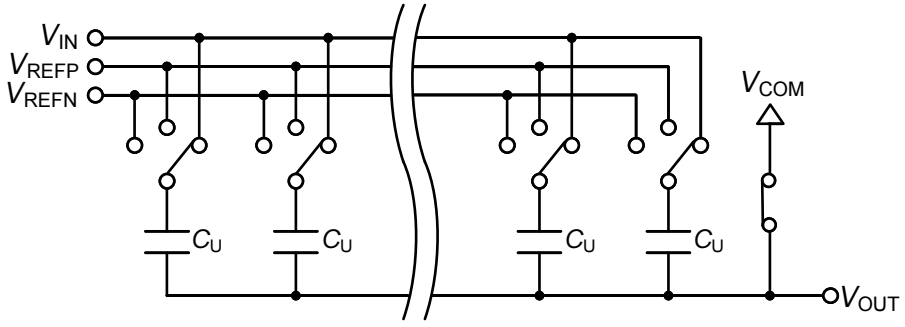
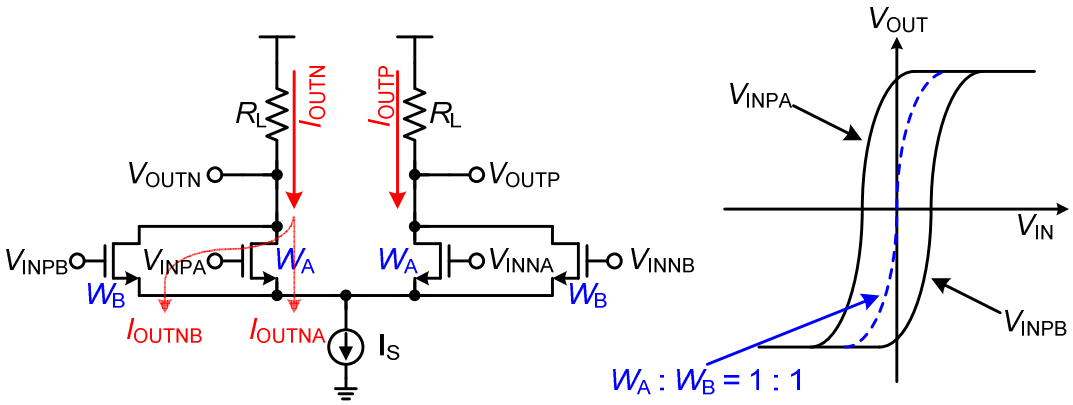



Figure 2.8 Example of charge redistribution interpolation [2.2].

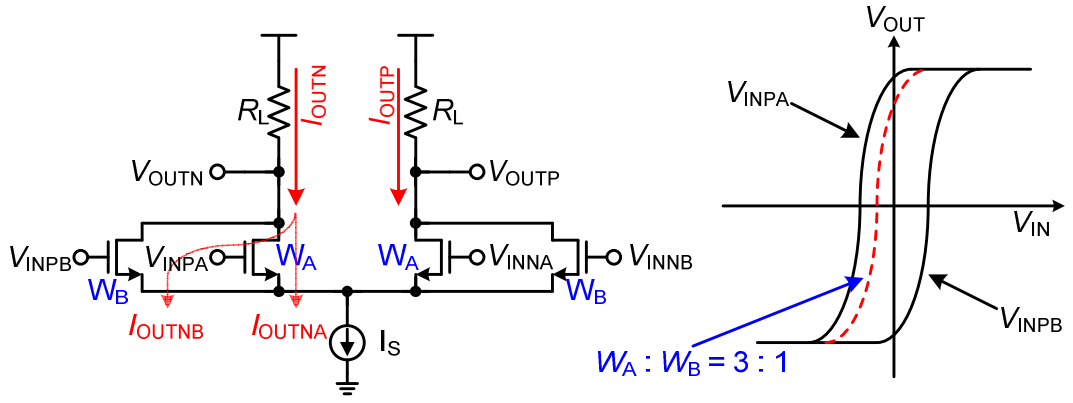
### 2.4.3 Gate-Weighted Interpolation

The resistive and the capacitive interpolator consist of the passive components, resistors and capacitors. There is another interpolation implementation method which utilizes active component. Figure 2.9 shows the gate-weighted interpolation technique. Contrary to the previous two interpolation techniques, the gate-weighted interpolation is performed by the only input signals. This interpolation is usually utilized in the comparator to make the comparison without reference voltages [2.2]. The circuits in Figure 2.9 are used as pre-amplifier for the comparator.

To realize the gate-weighted interpolation, the circuit requires 4-input transistors, 2 for $V_{INP}$ and 2 for $V_{INN}$. Also, input signals with offset are also required, such as $V_{INPA}$ and $V_{INPB}$. Assume that the input transistors have the same width as shown in Figure 2.9 (a). And $V_{INPA}$ and $V_{INPB}$ are connected in each transistor. Then, the averaged current of the $M_A$ and $M_B$, $I_{OUTP}$ flows in the load resistor, $R_L$. It means that the interpolated voltage with the size ratio of 1:1 is generated in the $V_{OUTP}$ node, as shown in the right side of Figure 2.9 (a). The same operation is performed in the negative side. The interpolation ratio can be changed by the transistors width ratio. For example, if the width ratio of $M_A$ and $M_B$ is assigned to 3:1,




(a) 1:1 interpolation




(b) 3:1 interpolation

Figure 2.9 Gate-weighted interpolation.

the interpolated signal is changed as shown in Figure 2.9 (b).

By using the interpolated signals, the comparator can make the comparison like the conventional comparator without reference range (it is explained in chapter 3 in detail). For example, by the composition of the CDAC interpolation and the gate-weighted interpolation, the reference-free multi-stage ADC can be realized. The gate-weighted interpolation utilizes the transistors; therefore, the linearity (signal range) and the transistor mismatch should be concerned. Also, the effect of input signal common-mode level is considered because it affects to the transistor's operation.

## 2.5 Realization of Interpolation in Multi-Stage ADCs

Multi stage ADC means that the ADC consists of more than two stages. In the multi stage ADC, each stage performs A/D conversion with the assigned stage's resolution. Here is a brief explanation of the multi-stage ADC's operation.

Firstly, the 1st stage samples the input signal. The stage performs A/D conversion and the sampled analog signal is added / subtracted based on the A/D conversion result (using DAC). The calculated signal is usually called the residue signal. After that, the residue signal is transferred to the followed stage. At that time, the transferred signal is usually amplified by the residue amplifier in the stage. The followed stage performs the same operation as the previous stage, sampling, A/D conversion, residue calculation, and transferring with amplification. Those operations are divided into two phases, the sampling phase and the amplifying phase. Usually, the sampling phase includes sampling and A/D conversion. And the amplifying phase is including residue calculation and transfer. After transfer the residue signal, the stage samples the next input signal and continue the same operation repeatedly. When the final stage finishes the A/D conversion, the ADC collects the each stage's A/D conversion results and generates the ADC result. As explained above, the ADC can perform the A/D conversion in every clock cycles; therefore, it can achieve high-speed operation. Also, the multi-stage ADC can achieve high-resolution by increasing

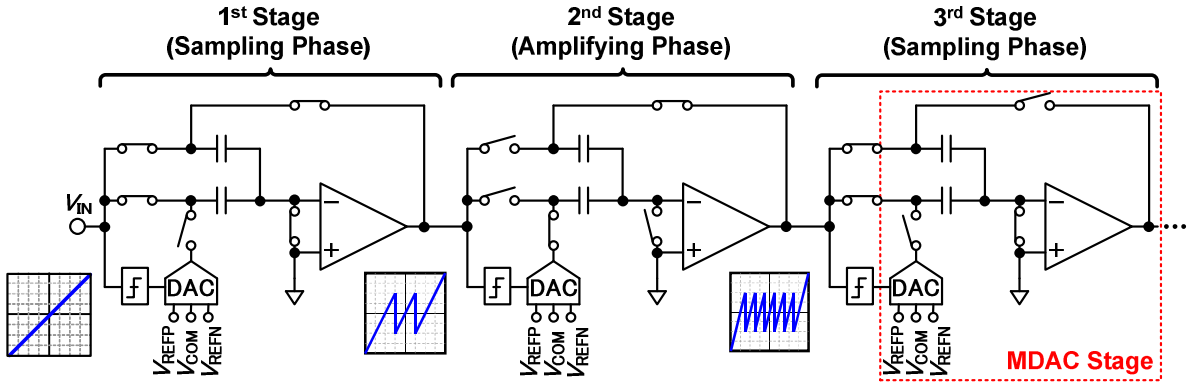



Figure 2.10 Block diagram and signal transfer of conventional pipeline ADC.

the number of the stage. The representative architectures of the multi-stage ADC are the pipeline ADC and subranging ADC.

Figure 2.10 shows block diagram and residue signal transfer of the conventional pipeline ADC. Each stage consists of capacitors, sub-ADC, DAC, and amplifier. The composition of MDAC stage is also depicted in Figure 2.10. The blue colored curve at the output of the stage means the amplified residue signal. The residue signal's slope becomes larger due to the amplification of each stage. As shown in Figure 2.10, the conventional pipeline utilizes the one differential signal (only shown single side signal in Figure 2.10).

Figure 2.11 shows block diagram and residue signal transfer of the interpolated pipeline ADC. The composition of the interpolated pipeline stage is basically same with the conventional pipeline ADC. The 'sample & CDAC' block in the 1st stage includes capacitors and DAC. Also, the 'Int. Caps' block in the 2nd and 3rd stage means CDAC including interpolation function. The most difference between the conventional pipeline ADC and the interpolated pipeline ADC is the number of single paths. As explained in chapter 2.4, the two differential signals (only shown single side signal in Figure 2.11) are required for the interpolation. Therefore, there are two signal paths (two circuits) in the interpolated pipeline ADC. The slope of the transferred curves becomes large due to the amplification, as well as the conventional pipeline ADC. As shown in Figure 2.11, there is no reference signal from the 2nd stage. The ADC selects signal range by using interpolation technique. Because there is no defined reference range, the signal ranges in each stage are different. The detailed operation of the interpolated pipeline ADC is covered in the following chapters.

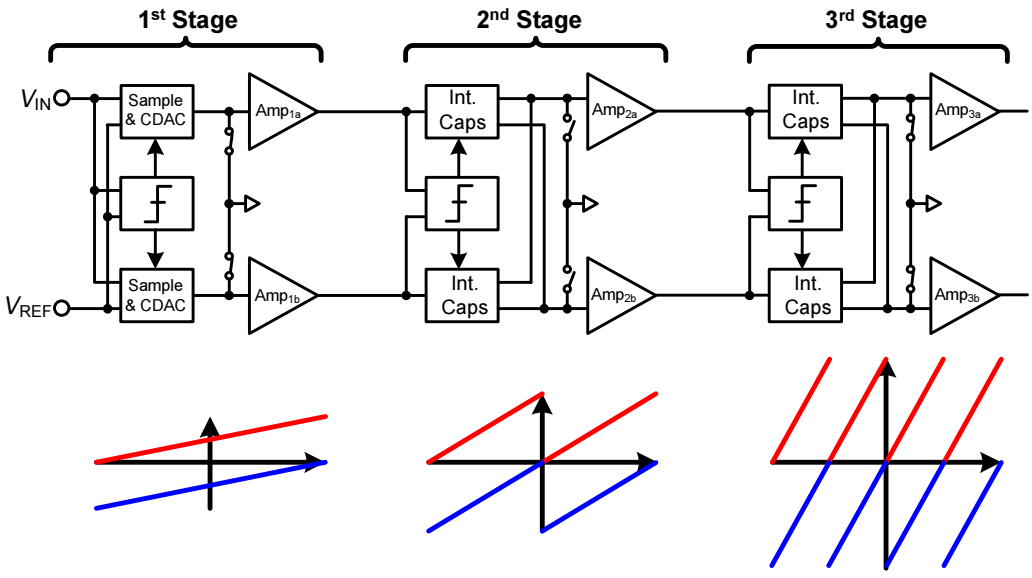



Figure 2.11 Block diagram and signal transfer of interpolated pipeline ADC.

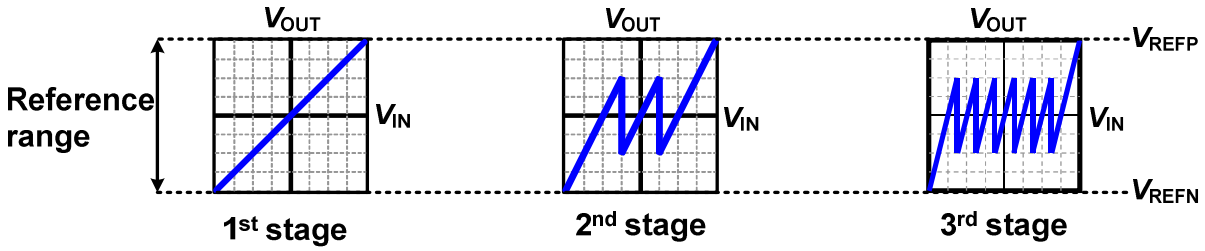



Figure 2.12 Signal transfer and reference range in conventional pipeline ADC.

### 2.5.1 Reference Range in Multi-Stage ADC

As explained in chapter 2.5, the multi-stage ADC consists of series connected multiple stages. Therefore, the reference ranges have to be matched between stages. To match the reference ranges between stages, each stage must realize the accurate relative gain. For example, in the pipeline ADC, well matched capacitors and high-gain amplifier are required to realize the accurate gain. Figure 2.12 shows the concept of reference range and amplified signal transfer in the conventional pipeline ADC. In Figure 2.12, the blue signal is analog signal which is amplified and transferred to the following stage. As shown in Figure 2.12, the start-point and the end-point of the analog signal have to meet to $V_{REFN}$ or $V_{REFP}$, respectively. If the analog signal does not meet to those reference voltages, the linearity error is occurred in the ADC's output code.

Among the requirements for the accurate gain, the capacitor matching can be achieved with proper capacitor size and careful layout. However, the high-gain amplifier realization is difficult in recent scaled technology as described in chapter 1.3. The relation of the ADC's error and the amplifier's gain is written as below [2.3],

$$\varepsilon_{[LSB]} = \frac{3 \times 2^N}{G} \tag{2.1}$$

where $\varepsilon$ means error of the ADC, $N$ means the ADC's resolution, and the $G$ means the amplifier's gain. By the (2.1), the error of the ADC is inversely proportional with the amplifier's gain.

Figure 2.13 shows an example of the effect of the reference range mismatch when the amplifier's gain is not high enough. In Figure 2.13 (a), the red colored line means sufficient amplifier's gain and the blue colored line means insufficient gain. If the amplifier of the stage does not have sufficient gain, the gain of the stage is reduced and also the reference range of the amplified signal is shrunk from the original $V_{REFP}$ and $V_{REFN}$. As a result, the ADC's output code includes missing codes as shown in Figure 2.13 (b). These missing codes degrade the ADC's linearity. The amplifier's required gain can be estimated as below [2.4],

$$G = 6N + 10\,[\mathrm{dB}]. \tag{2.2}$$

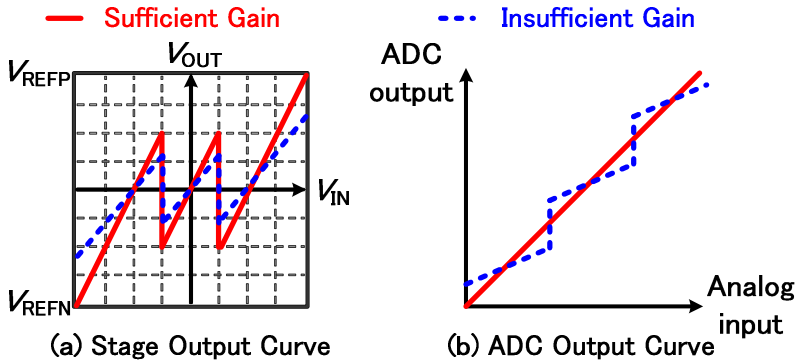



Figure 2.13 Effect of reference range mismatch (insufficient amplifier's gain).

In (2.2), $G$ means the required gain of the amplifier and $N$ means the ADC's resolution. For example, to realize 10-bit pipeline ADC, 70-dB gain amplifier is required. For 12-bit pipeline ADC, the required amplifier's gain is increased to 82-dB. This gain is very high to realize in recent scaled technology.

In Figure 2.13, the problem of the insufficient amplifier's gain is drawn. Actually, the gain requirement of the amplifier is the most crucial in the high-resolution multi-stage ADC development using amplifier, such as pipeline ADC. Also, the component mismatch and poor linearity of the amplifier are problematic. Recent developed multi-stage ADCs usually solve these problems by introducing the calibration technique.

### 2.5.2 Comparison with Interpolation Technique in Pipeline ADC

Before moving to the calibration technique, more specific explain for the interpolation in the multi-stage ADC is described in this sub-chapter. This sub-chapter focuses on the A/D conversion in the multi-stage ADCs, in comparison of the conventional pipeline ADC and the interpolated pipeline ADC.

Before explain the comparison using interpolation technique, the operation of the conventional pipeline ADC is described first to understand the advantage of the interpolation technique. Figure 2.14 depicts the A/D conversion of the conventional pipeline ADC. Only the amplifier and the comparators are drawn because those circuits have the charge of the A/D conversion. In the conventional comparison, each comparator has its own reference voltage. If the input signal of the comparator is higher than its reference voltage, the comparator outputs high. On the other hand, if the input signal is lower than the reference voltage, the comparator outputs low. Because the comparison is performed by the reference voltage, the result is affected by the amplifier's gain. As shown in Figure 2.14, if the amplifier's gain is varied, the amplifier's output signal is also varied from $V_O$ to $V_O$'. At that time, the input signal of the $CMP_3$ is moved from below the reference voltage to above the reference voltage. This variation causes $CMP_3$'s comparison error because its output is changed from low to high

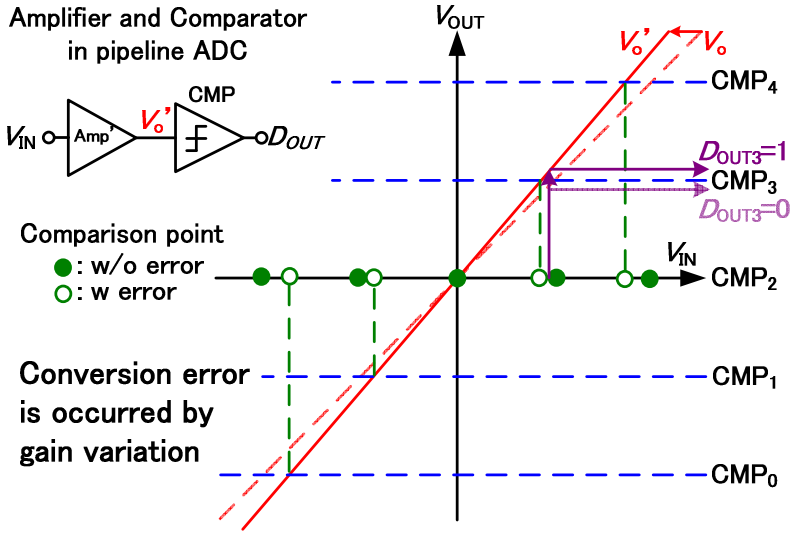



Figure 2.14 A/D conversion in conventional pipeline ADC.

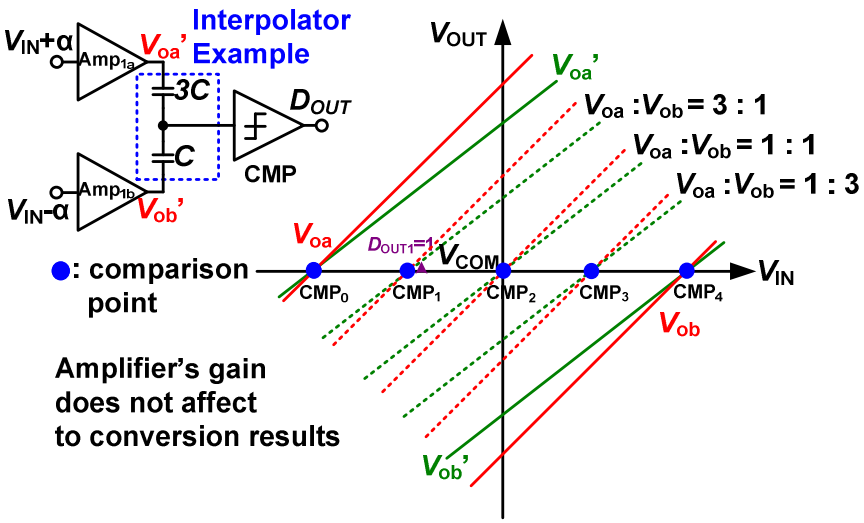



Figure 2.15 A/D conversion in interpolated pipeline ADC.

although the input (amplifier's input) does not changed. This is the reason of the amplifier's gain variation causes the ADC's error in the conventional pipeline ADC.

On the other hand, the interpolation technique solves this amplifier's gain variation error easily. Figure 2.15 shows the A/D conversion of the interpolated pipeline ADC. Because the interpolation technique requires two signals, the input signals with +/- α offset are applied to two amplifiers. Those amplifiers' output is connected to the interpolator. In Figure 2.15, the capacitive interpolator (CDAC) is utilized. However, the resistive interpolator also can be used. The interpolator outputs the interpolated signal with assigned ratio. The interpolated signals are also shown in Figure 2.15. After that, the comparator compares the interpolated signal with a common mode voltage level, such as $V_{COM}$. This is because the example is single signal comparison. By using the differential signal, the comparison can be

done without $V_{COM}$ -. If the interpolated signal is higher than $V_{COM}$, the comparator outputs high. For the comparison using the interpolation technique, the comparator's output does not changed although the amplifier's gain is changed as shown in Figure 2.15. For example, in Figure 2.15, $CMP_1$'s output is still 1 after amplifier's gain is changed. Consequently, the amplifier's gain does not affect to the ADC performance. This is the reason of the interpolated pipeline ADC becomes free from the high-gain amplifier. There are many considerations to realize the interpolation. The analysis on the interpolation technique are described in following chapters.

## 2.6 Calibration for Multi-Stage ADCs

As introduced in chapter 1.3, recently developed high-speed / high-resolution ADCs usually utilize calibration technique. However, introducing calibration technique not only increases the ADC's performance but also accompanies several disadvantages. One of the merits of the interpolation techniques is elimination of the calibration circuit from high-performance ADC.

The calibration technique for the multi-stage ADCs can be categorized by foreground / background calibration. Also, each calibration methods can be sub-categorized by algorithm. Each calibration has advantages and disadvantages. In this chapter, calibration methods are introduced for the multi-stage ADCs. The principle, examples, pros and cons are described for further understanding of not only the calibration but also the ADC using interpolation.

### 2.6.1 Error Sources of Conventional Pipeline ADC

Before investigating calibration techniques, explanation of the error sources in the ADC is necessary to understand the operation of the calibration. The conventional pipeline ADC is picked up as an example of the multi-stage ADC as well as previous chapters.

There are three major error sources in the conventional pipeline ADC. The gain error caused by insufficient amplifier's gain, the DAC error caused by the unit capacitor's mismatch, and the linearity error caused by the amplifier's nonlinearity are the major error sources. Figure 2.16 shows the ideal outputs and the non-ideal outputs of the pipeline stage. It is assumed that the stage has 4-bit resolution. Therefore, there are 16 reference ranges in Figure 2.16. Among the error sources, required calibration time for the gain error is assigned as 16 clock cycles because the stage has 16-times gain. Also, required calibration time for the linearity error also assigned 16 clock cycles because the 16-times gain expands signal swing range and wide swing range degrades linearity characteristic. For the DAC error is different from the previous two errors. The reason of the DAC error is due to the capacitor mismatch. Because the mismatch of each capacitor is different, it is necessary to calibrate using different amount for each capacitor. Therefore, the calibration time is increased with the stage's resolution (reference ranges), 16 clock cycles in this example.

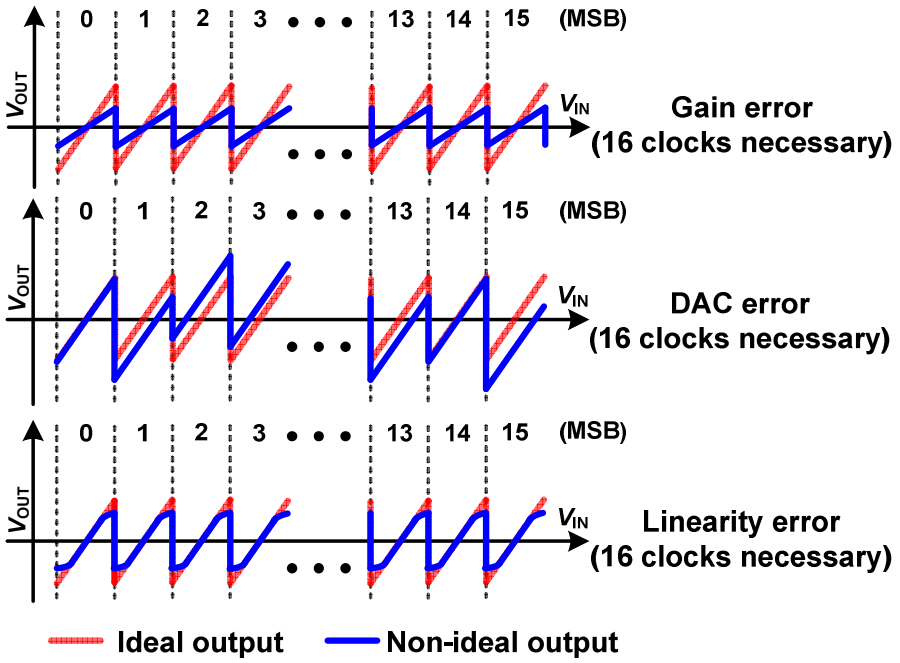



Figure 2.16 Three major error sources of conventional pipeline ADC.

The error sources and the necessary calibration times in Figure 2.16 are simplified for explanation. The actual error sources and calibration times are much more complicate and hence it requires much longer calibration time. Especially, the amount of required calibration is proportional with the ADC's resolution. Therefore, the high-resolution ADC's calibration time becomes extremely long.

### 2.6.2 Foreground Calibration

Figure 2.17 shows principle of foreground calibration [2.5]. The foreground calibration performs calibration process before start of the ADC operation. During calibration, already known input sequence is applied to the ADC. Since the output of the ADC under ideal condition can be expected (by already known input sequence); the amount of ADC's error can be measured and corrected.

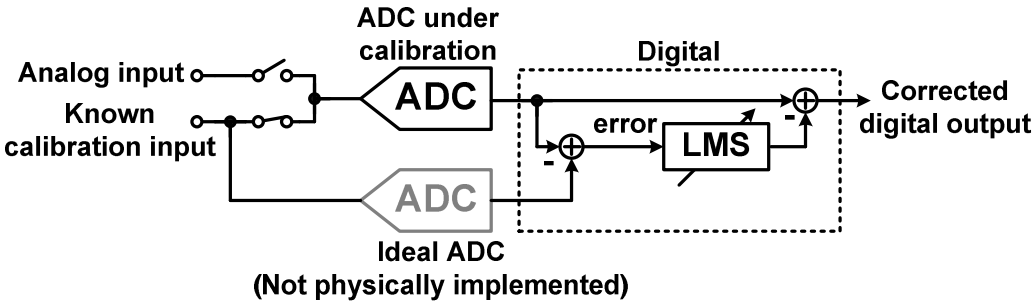



Figure 2.17 Principle of foreground calibration [2.5].

The required calibration time of foreground calibration is determined by the algorithm of the calibration. Usually, the foreground calibration takes long time [2.6] – [2.7]. Some calibration techniques reduce the calibration time effectively [2.8] – [2.10]. It is possible because the error source in the ADC and the ADC's output is highly correlated. However, that kind of short time calibration also has limitations, such as applicable ADC resolution is low or applicable operation speed is slow. Also, foreground calibration does not affect to the ADC operation because the calibration process is already finished before the ADC's operation. However, foreground calibration has severe disadvantage. To perform the calibration, the ADC is required to be taken offline. This kind of operation cannot be allowed in some application, which means foreground calibration's application is limited. Also, foreground calibration cannot adjust the calibration coefficient with the change of the ADC status automatically. For example, the temperature of SoC is usually increased after the begging of the operation. Because the characteristics of circuit components are changed with the temperature variation, such as mobility and threshold voltage, the coefficient for the calibration is also apart from the proper value. It means the ADC should run the calibration again. This makes the huge problem of the ADC, because the ADC cannot work during calibration.

A pipeline ADC using foreground calibration technique has been introduced [2.6]. The calibration in [2.6] estimates MDAC stage's gain error, amplifier's nonlinearity, and capacitor mismatch by the LMS engine, which is a name of calibration algorithm. Block

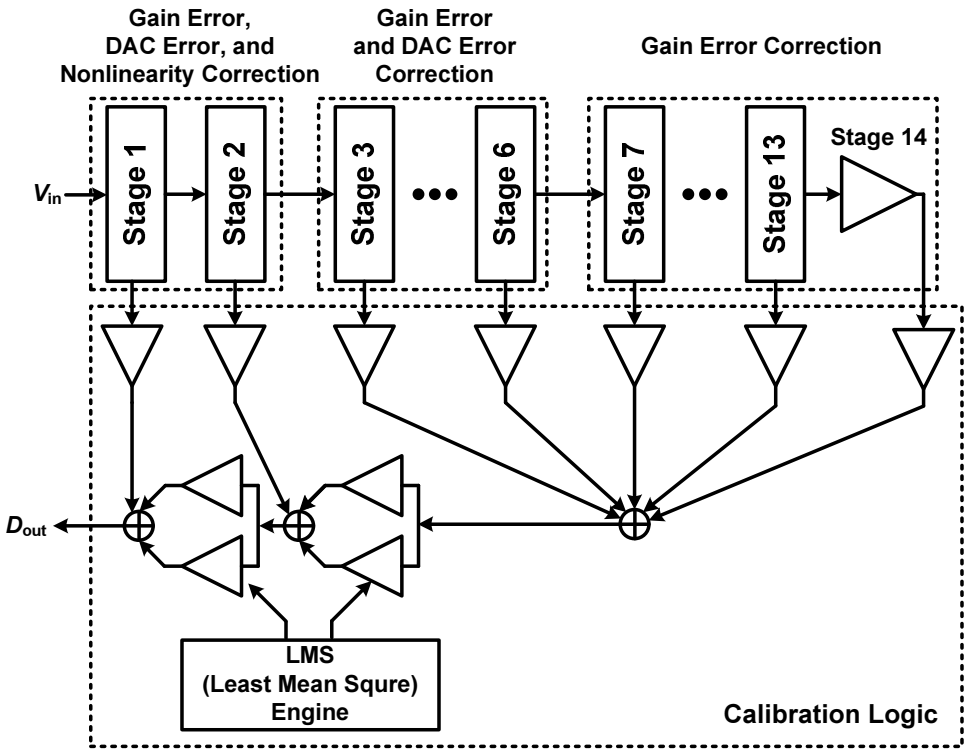



Figure 2.18 Example of foreground calibration using LMS engine [2.6].

diagram of the pipeline ADC in [2.6] is depicted in Figure 2.18. As shown in Figure 2.18, the calibration logic (LMS) collects all stages' digital output and compensates error. The amount of compensation is reduced with later stages. This is because the previous stages are more important in the pipeline ADC. After collecting digital outputs, the LMS engine calculates the errors and determines coefficients for calibration. Those coefficients are applied to the pipeline stages' output and the errors are eliminated. By the proposed calibration, the analog circuit in the MDAC stage can be designed simply because most of errors are cancelled by calibration circuit. However, the calibration method in [2.6] usually requires long calibration time. For example, the calibration in [2.6] requires thousands of clocks for calculation, which increases the test time and test cost.

Simple foreground calibration also has been presented. The work in [2.8] introduces another foreground calibration. As shown in Figure 2.10, the conventional pipeline ADC's stage gain is realized by the ratio of the sampling capacitance and the feedback capacitance. Figure 2.19 shows capacitors and op-amp of the pipeline ADC in [2.8]. Since the gain of MDAC stage is determined by feedback capacitance, the gain error which is caused by insufficient amplifier's DC gain can be compensated by the feedback capacitance adjustment. The calibration in [2.8] prepares extra capacitors in the feedback loop. After the estimation of the MDAC stage gain, the extra capacitors are added to adjust MDAC stage gain. This method can reduce the calculation time effectively, such as 168 clocks which is very small in comparison with the calibration in [2.8]. However, the increased capacitance in the feedback loop limits amplifier's bandwidth. It causes the settling error and degrades the ADC's performance. Also, the calibration cannot compensate the amplifier's linearity; therefore, the amplifier should satisfy the linearity requirement. Moreover, the ADC's resolution in [2.8] is 10-bit; therefore, the calibration needs to examine before applying to the ADC higher than 10-bit resolution. The work in [2.9] also incorporates foreground calibration. The calibration in [2.9] realizes 12-bit resolution ADC with 2,304 * $m$ calibration cycles where $m$ means error

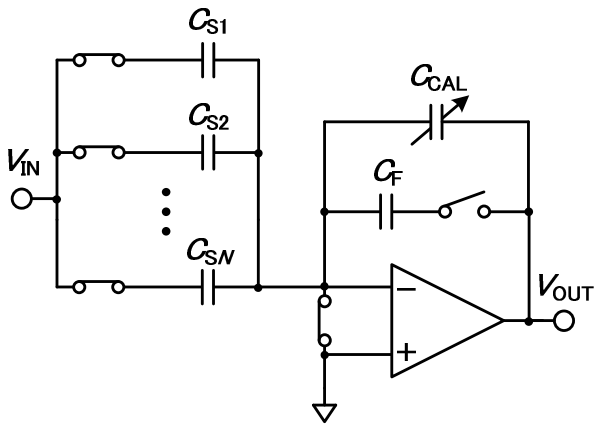



Figure 2.19 Conceptual diagram of gain calibration using feedback capacitance [2.8].

coefficient of the ADC. The calibration time is significantly reduced in comparison with [2.6]. However, if an ADC has large mismatch, the *m* is increased and the calibration time is also increased.

### 2.6.3 Background Calibration

In contrast of foreground calibration, background calibration is performed during ADC operation. It means the calibration logic continuously measures and corrects the error in an ADC. Therefore, the ADC does not need to be turned-off for the calibration.

Recently, a statistical calibration is utilized widely in background calibration [2.5]. Figure 2.20 shows a principle of background calibration using statistical method. For the statistical scheme, ADC's input signal is combined with a known pseudo-random sequence. Therefore, the output of the ADC is correlated with the pseudo-random sequence and the amount of the ADC's error can be measured. The pseudo-random sequence signal should be slow frequency and small amplitude to avoid significantly altering the ADC output spectrum and output code saturation.

Background calibration has a clear advantage which is non-necessity of turning-off the ADC for calibration. However, with statistics based background calibration schemes, a large number of clocks are required to accurately extract the pseudo-random sequence from the ADC output. This is because the output of the ADC is highly correlated with the analog input signal and weakly correlated with the pseudo-random sequence. Other background calibration algorithm, such as LMS engine, also has similar problem.

Some examples of background calibration are described below [2.11] - [2.14]. A 12-bit, 30 MS/s pipelined ADC has been presented [2.11]. Figure 2.21 depicts the block diagram of the ADC in [2.11]. It looks similar with the foreground calibration in [2.6]; however, the calibration algorithm is different. The ADC in [2.11] solves the reference range mismatch problem (insufficient amplifier's gain and nonlinearity) using background calibration, which is called the deterministic calibration which is a kind of statistical calibration. To perform the calibration, the ADC in [2.11] splits its timing into two phases, one is normal operation phases and another one is calibration phase. This calibration uses the sampling phase as

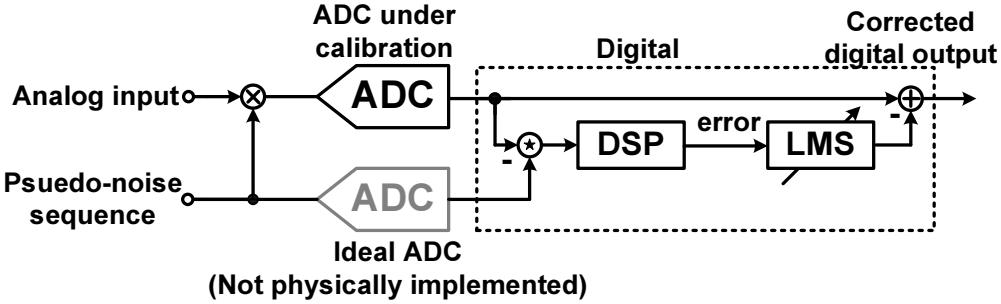



Figure 2.20 Principle of background calibration using statistical method [2.5].

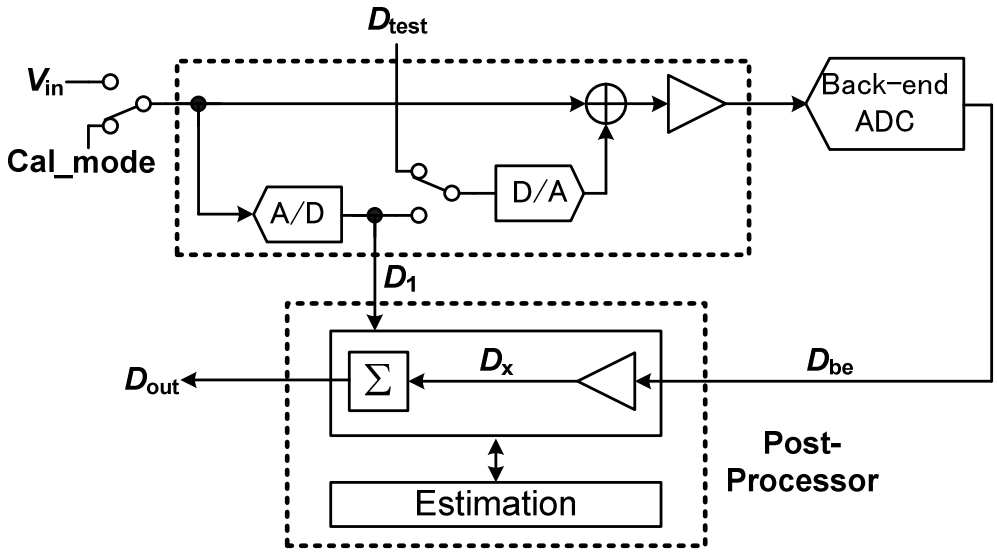



Figure 2.21 Block diagram of the deterministic background calibration [2.11].

calibration phase, which is the amplifier does not work during the phase. The calibration can compensate the insufficient gain and nonlinearity successfully. However, large amount of calculation increases the calibration circuit size and it becomes difficult to realize in on-chip. Due to the reason, the ADC incorporates the calibration circuit in off-chip, which is easier to examine the calibration and to modify the algorithm. Another disadvantage of the proposed background calibration is the ADC performance limitation by the calibration. Because the ADC cannot operate until the end of the calibration, the sampling frequency of the ADC is limited by the calibration time.

Another background calibration is introduced in [2.12]. Background calibration in [2.12] incorporates an auxiliary ADC to compensate amplifier's insufficient gain and nonlinearity. Figure 2.22 shows the principle of the calibration using auxiliary ADC. The chip and possibly slow ADC in Figure 2.22 indicates the auxiliary ADC. By introducing the auxiliary ADC, the calibration does not affect to the main ADC's operation timing. The calibration in [2.12] increases SFDR effectively in any temperature condition. However, the calibration utilizes additional ADC; therefore, it is easily expected that the power consumption and the core area are increased. Unfortunately, there is no specific information of the power consumption and the core area for the auxiliary ADC in [2.12]. However, the area of auxiliary ADC can be estimated by the chip micro photo. It looks almost 20% size of the main ADC. Also, the complex calibration method degrades its attractiveness.

There are many other background calibration methods. The ADCs in [2.13] - [2.14] utilize statistical background calibration. Those ADCs achieve high-resolution by the calibration, such as 15-bit and 12-bit, respectively. However, as written in the first paragraph in this sub-chapter, the statistical background calibration requires large number of calibration clock cycles. For example, [2.13] requires $2^{27}$ calibration clock cycles to realize

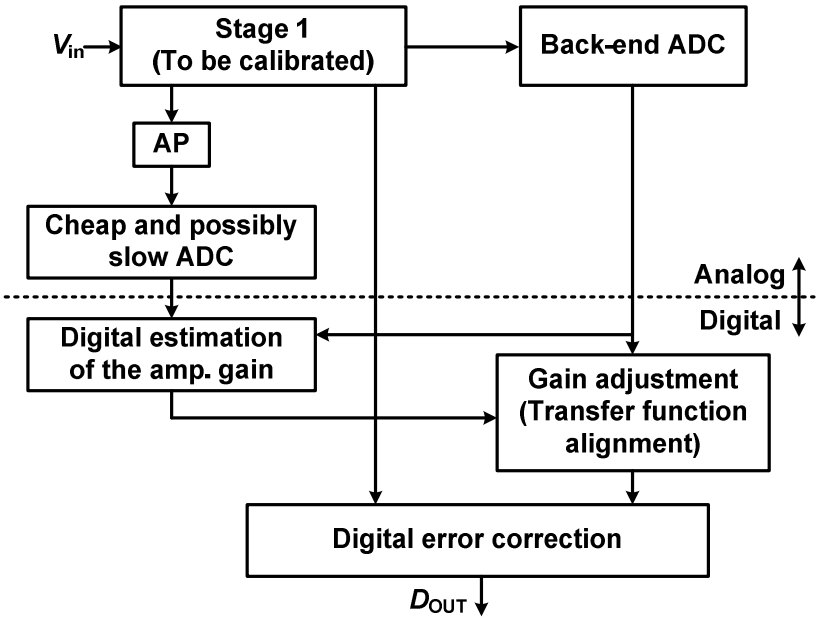



Figure 2.22 Principle of background calibration using auxiliary ADC [2.12].

15-bit resolution. The calibration [2.14] utilizes split ADC architecture to reduce calibration time. The required calibration clock cycles are reduced to 4,096 clocks; however, the ADC operation speed also decreased to 5 MS/s due to the calculation. Also, increased complexity is a disadvantage of [2.14].

### 2.6.4 Calibration Summary

Table 2.1 shows the comparison table of the several calibration methods which are introduced in chapter 2.6. Some references are not included in the Table 2.1 because they do not describe the specific information of the calibration in the ADC, such as [2.12].

The calibration techniques become an essential part of the high-resolution ADCs using recent scaled technology. Especially higher than 10-bit resolution, most of the ADCs include calibration circuit to achieve the target specification. However, calibration circuit accompanies several disadvantages. Both background and foreground calibrations usually increase the power consumption and the core area. Also, high-resolution ADCs require long calibration time which increases the test time and test cost, as shown in Table 2.1.

Furthermore, foreground calibration cannot track the circuit status variation by temperature variation. Especially, the linearity calibration is very sensitive to the temperature variation. Therefore, the temperature variation is very crucial for some applications in which cannot turn-off the ADC during the system's operation. To reduce the effect of the temperature variation using foreground calibration, high-gain amplifier is required, which means that it is putting cart before the horse [2.15].

On the other hand, the background calibration circuit usually limits the ADC's

Table 2.1 Comparison table of calibration methods.

| Ref. | Calibration Circuit | | | | | ADC | |
|---|---|---|---|---|---|---|---|
| | Cal. Type | On/Off chip | Time [cycle] | Area [$mm^2$] | Power [mW] | Resolution [bit] | $F_S$ [MS/s] |
| [2.6] | Foreground | Off | > 10,000 | 20,000 gates | 8 | 10 | 500 |
| [2.8] | Foreground | On | 2,304 * *m* | 16.7 | NA | 12 | 80 |
| [2.9] | Foreground | On | 168 | NA | NA | 10 | 320 |
| [2.11] | Background | Off | > 22,000 | NA | 3 | 12 | 30 |
| [2.13] | Background | On | $2^{27}$ (> 134e6) | 6 | NA | 15 | 50 |
| [2.14] | Background | Off | 4096 | NA | NA | 12 | 5 |

※ *m*: Error amount coefficient in ADC.

operation speed because the coefficient for the calibration has to be calculated during ADC operation. The effect by the background calibration to the ADC operation is also shown in Table 2.1.

In the industry, the test cost is one of the most important issues in circuit development. The test cost relates with test time deeply and the test time is increased by the calibration. Generally, the test cost can be defined as below,

$$\text{Test Cost} = \frac{\text{Tester Price} + \text{Managing Price}}{\text{Depreciation Cost}} + \text{Personnel Expenses} \qquad (2.3)$$

Because the analog tester is usually expensive than 10 billion dollar, reducing test time is important in the point of development cost. Several test methods are developed to reduced test time, for example, BIST and BOST [2.16]. For reducing the test cost, not only test method but also circuit design are important, such as small calibration required circuit. For example, an ADC requires 4,096 clock cycles for calibration, only 1.5 million chips are tested in 1 second. On the other hand, if an ADC requires only 168 clock cycles for calibration, 36 million chips can be tested.

The calibration technique is very effective method to realize high-resolution ADC with recent scaled technology. However, it also accompanies several disadvantages. Therefore, if it is possible, the elimination of the calibration circuit is the best for the ADC design. The interpolation technique is a good solution to realize the ADC without the calibration

technique. Therefore, the interpolation technique is valuable to be investigated. The effectiveness of the interpolation technique is explained in the following chapters. Also, the relation of the interpolation technique and the calibration technique in the future is suggested in chapter 8.

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# 3. Design of 6-bit Subranging ADC with Gate-Weighted Interpolation

## 3.1 Introduction

6 to 7-bit, several hundred MS/s to around 1 GS/s ADCs are required for disk drive front-ends, backplane and ultra-wideband receivers. Especially for embedded consumer SoCs, an ultra-low-power operation is the most important characteristic rather than high-resolution and high-speed for the conventional ADC cores. This is because total power reduction is very crucial for portable applications and also for addressing green IT regulation.

Conventionally, the flash architecture has been used for these targets because of an advantage to high-speed operation [3.1]. However, the flash architecture has an essential limitation in reducing conversion energy [3.2] - [3.3]. An open-loop pipelined ADC has been investigated to attain this target [3.4], however the power consumption is still large. The SAR architecture has been recognized as the most energy efficient architecture; however, it is not easy to increase the conversion rate up to the GS/s range [3.5] - [3.6]. An asynchronous SAR ADC with interleaving [3.7] achieves a relatively high conversion rate but design difficulty is increased. An extremely small FoM of 40 fJ/conv. steps has been attained in a 6-bit 2.2 GS/s ADC using dynamic pipeline architecture [3.8]. However, this ADC also introduced interleaving technique and the design becomes complicated.

The subranging architecture is a good solution for this target; however, the results have not been attractive. Although, [3.9] achieves 1 GS/s conversion rate, the power consumption is very large due to pre-amplifiers which are introduced to reduce offset voltages. Another subranging ADC [3.10] achieves 8-bit resolution and 770 MS/s conversion rate; however, large power consumption by pre-amplifiers and buffers are also problematic. A two-step architecture in [3.11] shows high-resolution, but large power consumption and low conversion speed reduces its attractiveness.

The work presented here is based on the subranging ADC using the CDAC, gate-weighted interpolation scheme, and digitally offset calibrated double-tail latched comparator [3.12] - [3.13]. This chapter is organized as follows: Chapter 3.2 introduces the ADC architecture, key schemes and techniques. Chapter 3.3 provides the implementation of the proposed subranging ADC. Chapter 3.4 details the experimental results, and this chapter is finally concluded in chapter 3.5.

## 3.2 ADC Architecture and Techniques

### 3.2.1 Conventional Subranging Architecture

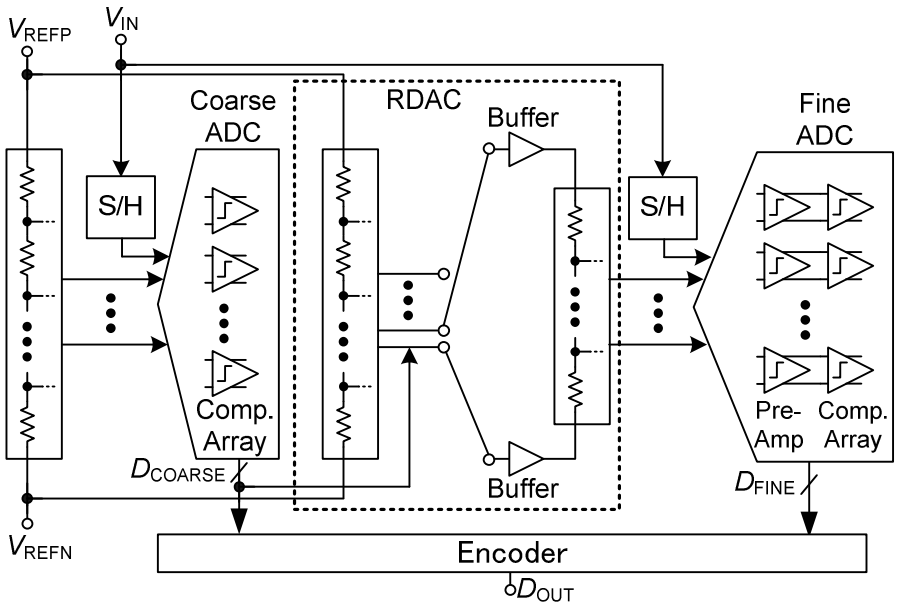


Figure 3.1 Conventional subranging architecture.

As introduced in chapter 3.1, the subranging architecture is an attractive solution for our target specification. However, a conventional subranging architecture has a couple of issues, especially the disadvantage of the power consumption.

The conventional subranging architecture is shown in Figure 3.1 [3.1]. There are two resistor ladders in Figure 3.1. Static current flows through the resistor ladder and this causes large power consumption. This current can be suppressed by increasing resistance of the resistor ladder. However, reducing the current causes speed degradation, which is not suitable for high-speed operation. The pre-amplifiers to reduce comparator's offset are another source of the power consumption. Furthermore, the buffers for the fine ADC consume static power.

Another issue of the conventional subranging ADC is the conversion precision in the fine ADC. Because the fine ADC decides the resolution of the ADC, it has to have a sufficiently fast settling time and a small offset voltage; therefore, the speed of the ADC is limited. Comparators in the fine ADC also have to satisfy the precision requirement of the ADC in the whole reference range.

### 3.2.2 Subranging ADC using CDAC

One effective solution to solve the large power consumption problem in the conventional subranging ADC is to introduce the CDAC for the reference selection. The subranging architecture using the CDAC is shown in Figure 3.2. By introducing the CDAC, S/H and buffers can be eliminated. Also, timing margin for settling is relaxed and fine reference range is fixed around common-mode voltage which is helpful for the gate-weighted interpolation in

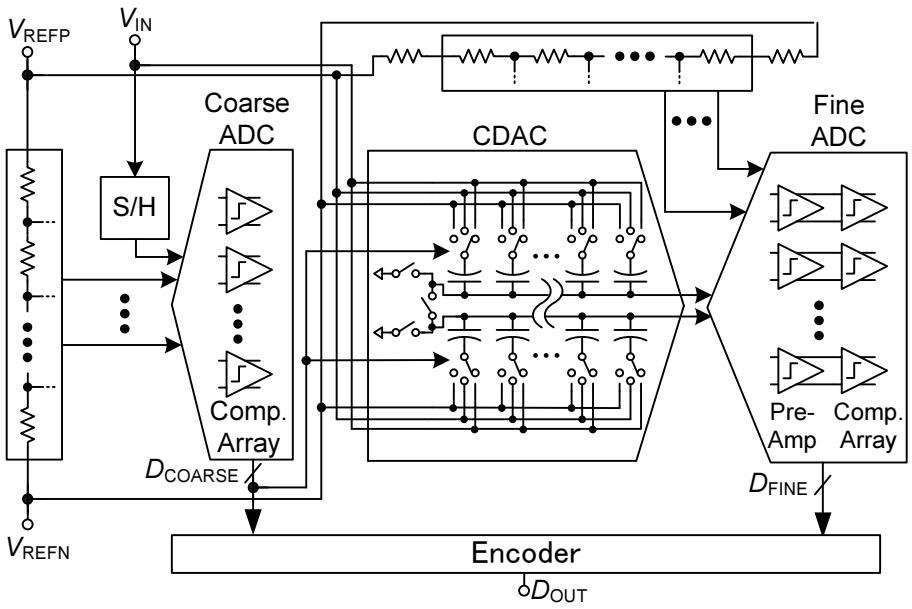


Figure 3.2 Subranging architecture using CDAC.

the fine stage. However, if there is a parasitic capacitance in the input of the fine ADC such as $C_{PI}$ in Figure 3.12, the input signal that is charged into the CDAC is reduced. This affects the ADC's performance. The RMS DNL error, which is caused by the parasitic capacitance, is represented in (3.1)

$$\boldsymbol{ERR}_{\mathrm{DNL\_RMS}}\,[\mathrm{LSB}] = \sqrt{2^{N-1}-1}\left(\frac{1-\boldsymbol{G}_{\mathrm{SIGNAL}}}{\boldsymbol{G}_{\mathrm{SIGNAL}}}\right) \tag{3.1}$$

where $N$ is resolution if the ADC and $G_{SIGNAL}$ is the gain of the CDAC. In the fine conversion range, DNL errors occur symmetrically with respect to the midpoint of the signal range. The amount of the error is represented as $2^{N-1}$-1 in (3.1). If there is no parasitic capacitance,

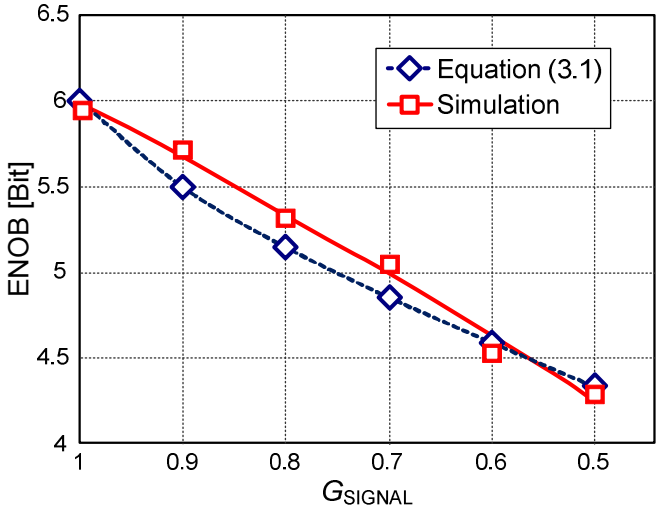


Figure 3.3 Effect of input signal reduction in fine ADC.

$G_{SIGNAL}$ is 1 and $ERR_{DNL\_RMS}$ becomes 0. However, by increasing parasitic capacitance, $G_{SIGNAL}$ decreases and $ERR_{DNL\_RMS}$ increases; therefore, the performance of the ADC is degraded.

Figure 3.3 shows the effect of the signal reduction by the parasitic capacitance in the input of the fine ADC vs. the ENOB of the 6-bit subranging ADC. The ideal model is utilized for the simulation. When the parasitic capacitance becomes half of the sampling capacitor, ENOB degrades about 1.7-bit.

The gain degradation problem might be addressed by introducing a gain error adjustment circuit. However, it is not easy to detect the amount of the gain error and guarantee sufficient linearity against PVT fluctuations. Furthermore, additional circuit causes an increase of the power consumption and core area.

### 3.2.3 Proposed ADC Architecture

To solve the previous issues, several techniques are introduced to the proposed ADC. First, the two-way fine ADC interleaving is incorporated to relax the timing margin for the fine conversion. Also, the CDAC is introduced instead of the RDAC to suppress static power consumption. The gain reduction problem, which is induced by the CDAC and the parasitic capacitance, is solved by the interpolation technique. A gate-weighted interpolation can realize good matching between the coarse and the fine conversion range, even if parasitic capacitances exist in the input of the fine ADC. Digital offset calibration using capacitors reduces the offset voltage of comparators effectively without introducing static power consumption.

Figure 3.4 shows the detailed block diagram of the proposed ADC. The coarse ADC consists of reference ladder, S/H, and 4×2-bit IP cells for 4-bit conversion. Each IP cell consists of 4 comparators that use gate-weighted interpolation technique. To realize the interpolation, the coarse ADC requires voltage shifter to generate two differential signal pairs because the input signal of the ADC is only one differential pair. In the coarse ADC, S/H

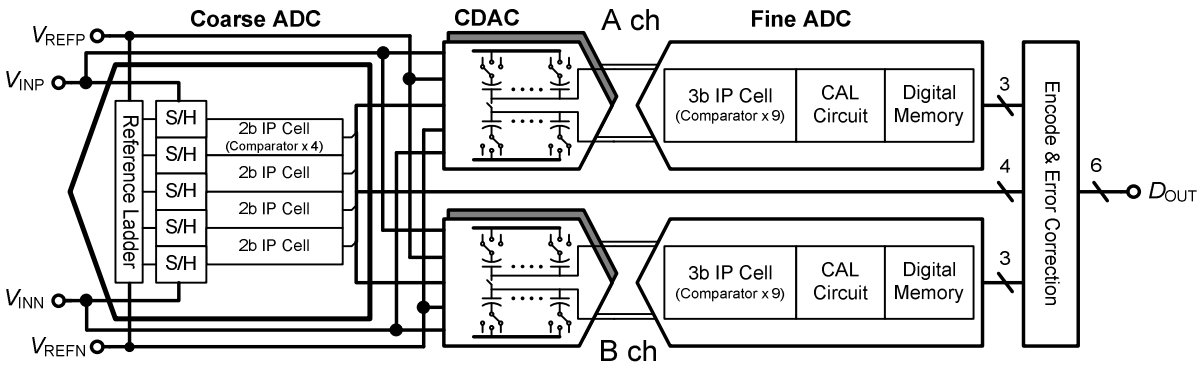


Figure 3.4 Proposed subranging ADC architecture.

circuit also performs voltage shifting. There is a resistor ladder in the coarse ADC. The total resistance of the resistor ladder is 1.7 kΩ. The resistor ladder consumes 0.3 mW power.

Two sets of the CDACs are used in the same way as in [3.11] to generate voltages for the fine conversion, instead of the conventional resistor ladder, in order to reduce the power consumption and the settling time, simultaneously. Furthermore, these CDACs act as S/H circuit like the CDAC in a SAR ADC.

The fine ADC consists of 9 comparators for 3-bit conversion which is illustrated as 3b IP cell in Figure 3.4. These comparators mainly determine the resolution of the ADC; therefore, it is necessary to reduce their offset voltages. Digital offset calibration is incorporated to the comparator instead of the conventional method, such as a pre-amplifier, for low-power consumption. In Figure 3.4, the CAL circuit and the digital memory blocks mean digital logic circuits and D flip-flops for the offset calibration. Two fine ADCs are interleaved to relax its operating frequency margin. Timing of each ADC is controlled by a clock timing controller which is not illustrated in Figure 3.4. Conversion results from the coarse and the fine ADCs are gathered in digital logics and corrected using one redundancy bit.

Figure 3.5 shows voltage transfer during conversion of the ADC. When the signal is applied to the ADC, the coarse ADC starts a conversion of 4-bit resolution. After the coarse conversion, two sets of differential signals are outputted from the CDACs for interpolation

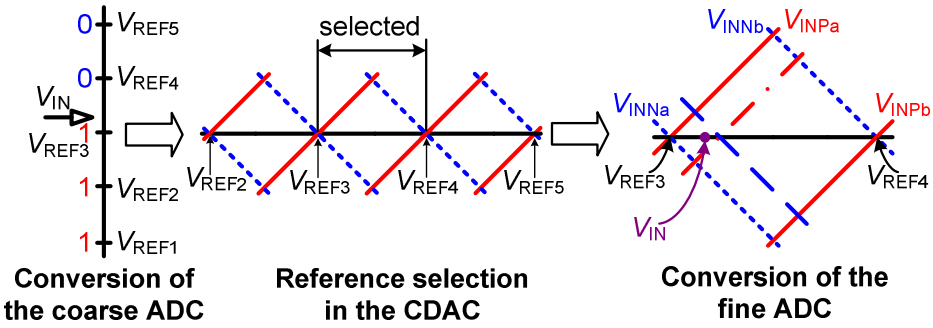


Figure 3.5 Conversion process of proposed subranging ADC.

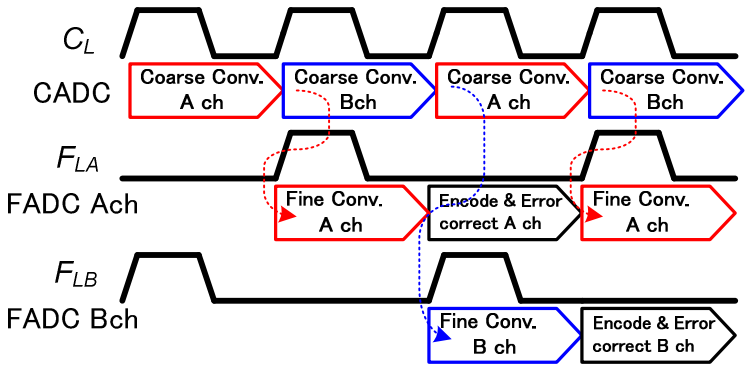


Figure 3.6 Timing chart of proposed subranging ADC.

according to the results of the coarse ADC. Finally, the fine ADC converts the input signal to the digital value in 3-bit resolution using the interpolation. The detailed explanation of the interpolation is shown in chapter 3.2.4.

Figure 3.6 shows a timing chart of the proposed subranging ADC. The coarse ADC operates at the same speed as the sampling frequency; however, the fine ADCs operate at half of the sampling frequency to relax the requirement for the settling time and the timing margins. The fine ADC does not consume any power when it does not convert; therefore, the power consumption does not increase although the circuit size is increased.

### 3.2.4 Interpolation in Subranging ADC

The proposed ADC addresses the gain reduction issue by using interpolation, which makes it possible to realize fine conversion without any reference voltages and to avoid the effect of the input parasitic capacitance of the fine conversion stages. To implement the interpolation, we introduce a gate-weighted interpolation scheme in the saturation region of MOS transistor to reduce the number of S/H circuits and input capacitance. The circuit implementation is described in chapter 3.3.2.

Figure 3.7 shows the 3-bit interpolation in the fine ADC of the proposed ADC. Two differential outputs from CDAC_a and CDAC_b are used to realize the interpolation. These output signals are shifted by 0.5 coarse LSB to realize one bit redundancy (half over range and half under range) for digital error correction [3.14].

The interpolated voltages $V_{Pi}$ and $V_{Ni}$ in Figure 3.7 can be represented as below,

$$V_{Pi} = \frac{(2^d - i)V_{INPa} + iV_{INPb}}{2^d} \tag{3.2}$$

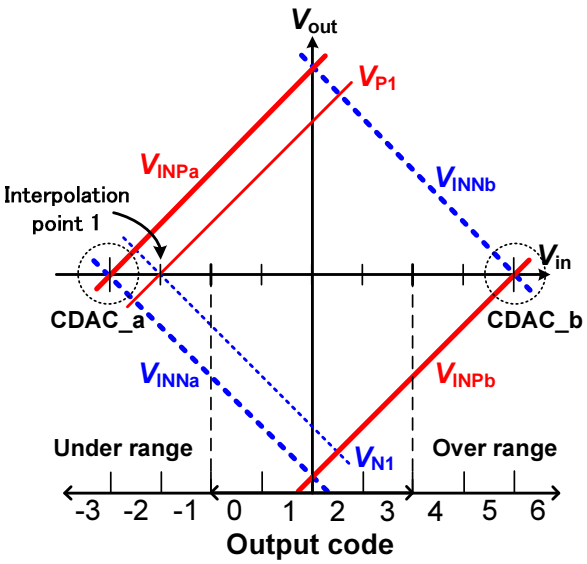


Figure 3.7 Interpolated voltages and output code in fine conversion.

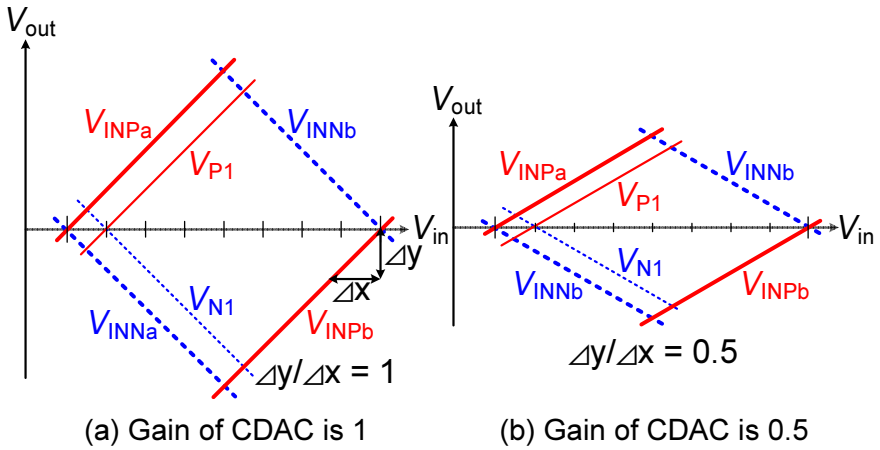


Figure 3.8 Mitigation of gain error by interpolation.

$$V_{Ni} = \frac{(2^d - i)V_{INNa} + iV_{INNb}}{2^d} \tag{3.3}$$

where $d$ is a resolution of the interpolation, $i$ is the number of the interpolated voltage, $V_{INPa}$ and $V_{INNa}$ are the differential output voltages from the CDAC_a, and $V_{INPb}$ and $V_{INNb}$ are the differential voltages from the CDAC_b. For example, at the interpolation point 1 (between -3 and -1), conversion is executed by using only $V_{P1}$ and $V_{N1}$. The other conversions are also realized by the interpolated signals. Therefore, reference voltages are not required for the fine conversion and consistency between the coarse and the fine conversion range is realized automatically.

Figure 3.8 shows the mitigation of the gain reduction error of the input signal for the fine ADC when using the interpolation (The principle is the same with chapter 2.3.2). Even though the signal gain is reduced, as long as the reduction ratio of two differential signals is the same, the comparison point does not change. Therefore, the proposed ADC does not require a gain error correction circuit to solve this problem.

### 3.2.5 Reference Selection

For the proposed subranging ADC, the CDAC is utilized instead of the RDAC. The reason of using CDAC is used is described in this sub-chapter.

Figure 3.9 shows the conceptual diagram of the CDAC and the RDAC. Both DACs basically consist of passive elements. The CDAC generates its output voltage using charge distribution of the capacitors and the RDAC generates its output voltage using voltage division of the resistor ladder.

The CDAC and the RDAC work in a very similar way. For example, during $\Phi_S$ (sampling phase), an input signal is charged to the capacitors, all of the unit capacitor, $C_U$ and sampling capacitor, $C_S$. After that, during $\Phi_H$ (holding phase) in the CDAC, one side of

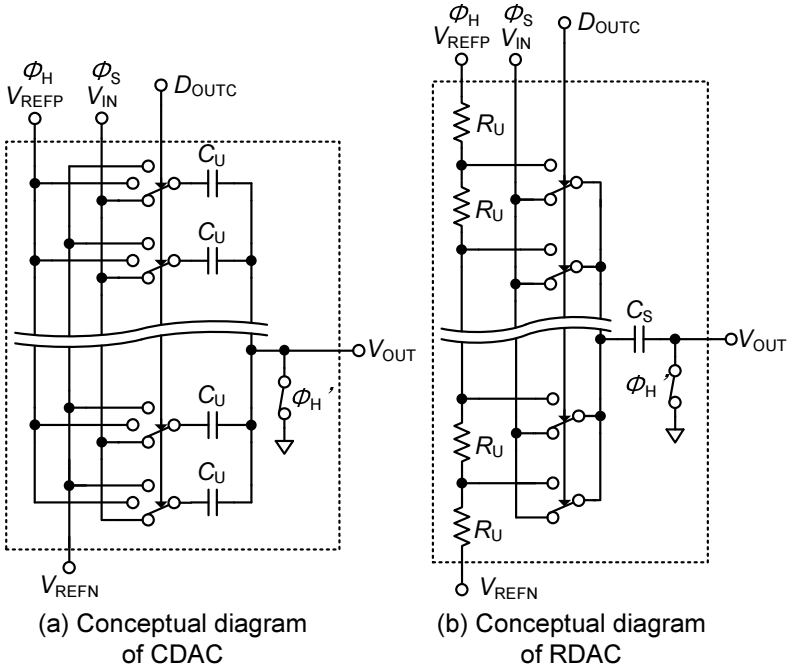


Figure 3.9 Conceptual diagram of CDAC and RDAC.

Table 3.1 Component values for analyses and simulation.

| $h$ | $C_U$ | $C_S$ | $C_{PI}$ | $R_{SW}$ | $R_U$ |
|---|---|---|---|---|---|
| 16 | 15 fF | 250 fF | 50 fF | 850 Ω | 10 Ω |

capacitors are connected to $V_{REFP}$ or $V_{REFN}$ depending on the results of the coarse conversion, and another side of the capacitors are connected to the input of the fine ADC. In the RDAC, one side of $C_S$, is connected to a certain node of the resistor ladder by the coarse comparison results. Another side of $C_S$ is connected to the fine ADC in the same way as the CDAC.

To compare the two DACs in detail, the analysis of settling time, power consumption and noise follows. Table 3.1 summarizes the components values for the analysis and the simulation. Those values of $C_U$ and $R_{SW}$ came from design parameters of the proposed subranging ADC [3.13]. In the CDAC, $R_{SW}$ is the resistance of PMOS or NMOS switch in the reference select circuit. In the proposed subranging ADC, the average resistance of PMOS and NMOS switch is about 850 Ω; therefore, $R_{SW}$ is assigned that value. $h$ is the number of unit capacitors (resistors). The total number of switches in both of the DACs is 16, which is the same value as $h$. For the RDAC, $C_S$ is the sum of $C_U$ and $R_{SW}$ is same as the CDAC. $C_{PI}$ is parasitic capacitance of the subsequent circuit, such as the fine ADC. The value of $C_{PI}$ is assumed to be 50 fF which is estimated from the proposed fine ADC [3.13].

In the RDAC, another resistive component $R_U$ exists. Basically, the value of $R_U$ is decided for the optimal power consumption and settling time with consideration of $R_{SW}$. However, in this comparison, $R_{SW}$ is decided first by the CDAC. When using that value of $R_{SW}$,

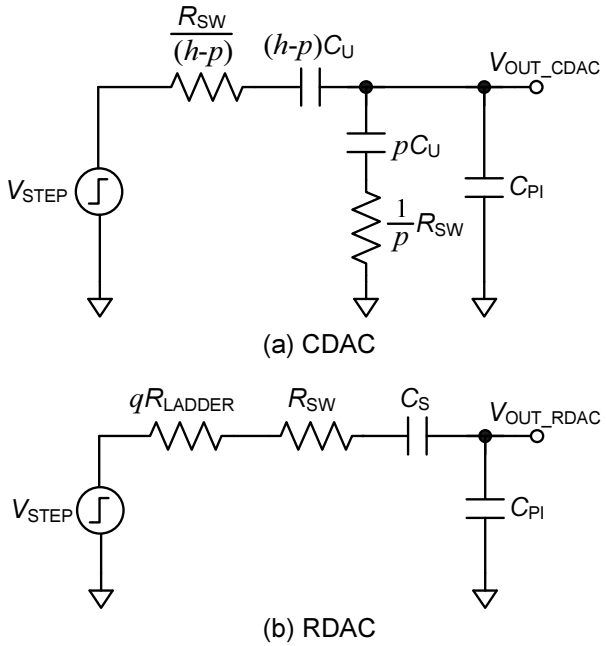


Figure 3.10 Circuit models for settling time analysis during holding phase.

even if $R_U$ is set to 0, the RDAC shows slower settling time than the CDAC. Although $R_U$ contributes only small portion of the settling time comparison, it also affects the power consumption and also settling time a little. Therefore, $R_U$ should be considered in the analysis and simulation.

In this comparison, $R_U$ is assigned to 10 Ω. For values less than 10, the power consumption of the RDAC increases drastically, but the settling time is only reduced by about 5 ps. More detail data is shown in chapter 3.2.5.2

### 3.2.5.1 Settling Time

To calculate settling time, we use the simplified models of the CDAC and the RDAC during holding phase. In Figure 3.10, $p$ is the number of parallel connection, $R_{LADDER}$ is the sum of resistance of the resistor ladder and $q$ is the variation coefficient by the connected position in the resistor ladder. We ignore parasitic capacitance in each node of the resistor ladder to simplify this analysis.

$$V_{OUT\_CDAC} = V_{STEP}\left(1-\frac{p}{h}\right)\frac{1}{1+\frac{C_{PI}}{hC_U}}\left(1-e^{-\frac{1+\frac{C_{PI}}{hC_U}}{\frac{R_{SW}}{h}C_{PI}}t}\right) \tag{3.4}$$

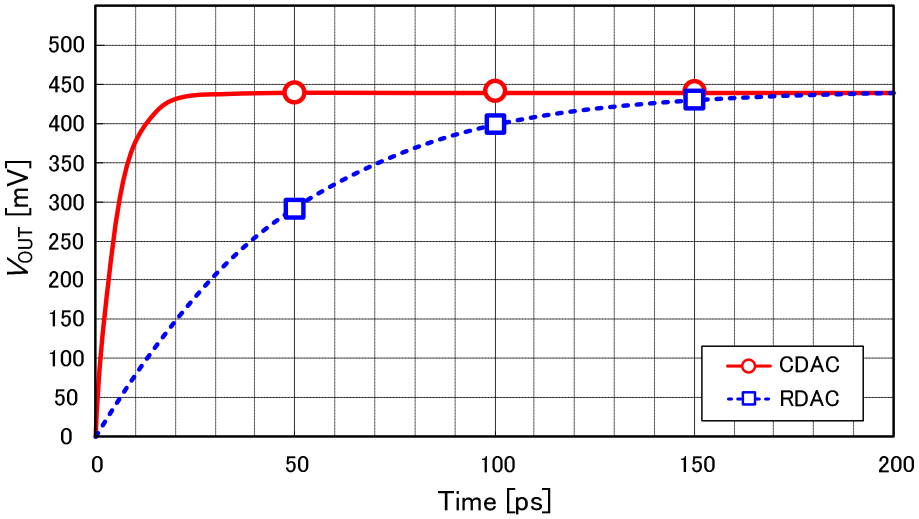


Figure 3.11 Simulation results of settling time.

$$V_{OUT\_RDAC} = V_{STEP} \frac{1}{1+\frac{C_{PI}}{C_S}} \left( 1 - e^{-\frac{1+\frac{C_{PI}}{C_S}}{(qR_{LADDER}+R_{SW})C_{PI}}t} \right) \tag{3.5}$$

Equation (3.4) and (3.5) represent the settling time of the CDAC and the RDAC, respectively. By these formulas, it is recognized that reducing resistance of the switch and the parasitic capacitance is important for faster settling time.

Simulation and analysis results are shown in Figure 3.11. The simulation results of circuits in Figure 3.10 and calculation results of (3.4) and (3.5) are matched almost perfectly. In Figure 3.11, only one line is drawn for each DAC for the clear figure drawing. According to the simulation and calculation results, the CDAC shows faster settling. The difference of the settling time between the two DACs is due to the difference of the resistance. In the CDAC, $R_{SW}$ is divided by $h$. However, in the RDAC, $R_{SW}$ is added with the resistance of the resistor ladder, $R_{LADDER}$.

In the RDAC, the settling time can be reduced by using a smaller $R_{LADDER}$; however, it results in an increase of the power consumption. Reducing $R_{SW}$ also contributes to faster settling time. However, it increases the parasitic capacitance of the switch; therefore, the settling time and the power consumption are increased.

### 3.2.5.2 Power Consumption

Figure 3.12 shows a mechanism of the power consumption in the CDAC and the RDAC during the holding phase. Assume that the input signal is already charged to $C_U$ and $C_S$ during the sampling phase and no leakage current flows in the DAC circuits.

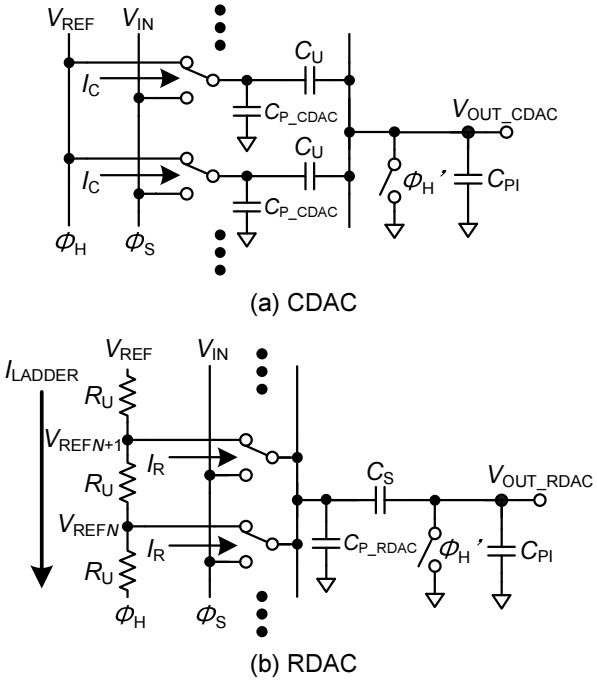


Figure 3.12 Mechanism of power consumption during holding phase.

$$P_{\mathrm{d\_CDAC}} = F_{\mathrm{S}}\left(C_{\mathrm{P\_CDAC}} + C_{\mathrm{PI}}\right)\left(V_{\mathrm{REF}} - V_{\mathrm{IN}}\right)^2 \tag{3.6}$$

$$P_{\mathrm{d\_RDAC}} = \frac{V_{\mathrm{REF}}^{\ 2}}{R_{\mathrm{LADDER}}} + F_{\mathrm{S}}\left(C_{\mathrm{P\_RDAC}} + C_{\mathrm{PI}}\right)\left(V_{\mathrm{REF\_}N} - V_{\mathrm{IN}}\right)^2 \tag{3.7}$$

Equation (3.6) and (3.7) represent the power consumption in the CDAC and the RDAC respectively. In (3.6) and (3.7), $F_s$ means sampling frequency of the proposed subranging ADC and $V_{\mathrm{REF\_N}}$ is $N$-th reference voltage in the resistor ladder. Equation (3.6) indicates that the

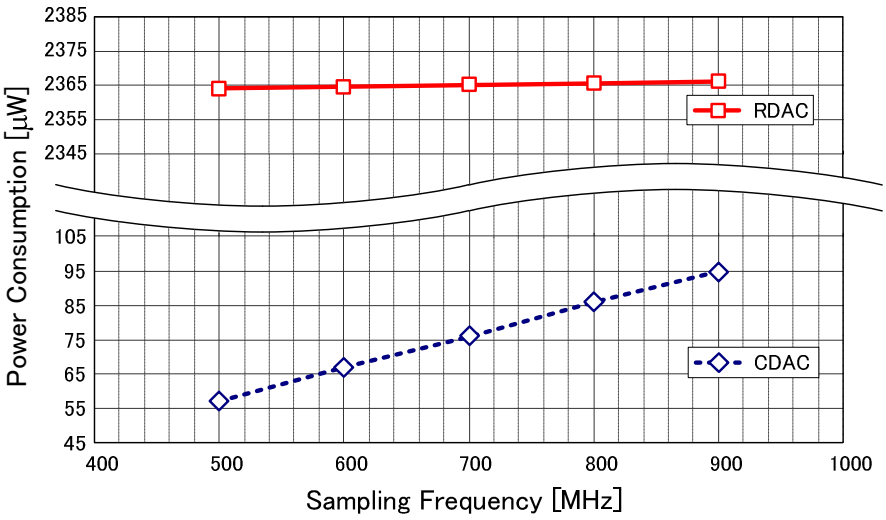


Figure 3.13 Simulation results of power consumption vs. sampling frequency.

power consumption of the CDAC is same as the digital circuit. On the other hand, (3.7) includes not only dynamic power consumption but also static power consumption caused by the resistor ladder in the RDAC.

Figure 3.13 shows simulation results of the power consumption vs. sampling frequency. In this simulation condition, the settling times of the CDAC and the RDAC are about 190 ps and 280 ps, respectively. For fair comparison, the settling time should be set to the same. However, as mentioned in chapter 3.2.5, adjusting settling time using only $R_U$ is quite difficult. Changing other parameters also affect to the CDAC and causes other issues, such as change of settling time.

There is a large difference of the power consumption between two DACs', such as 76

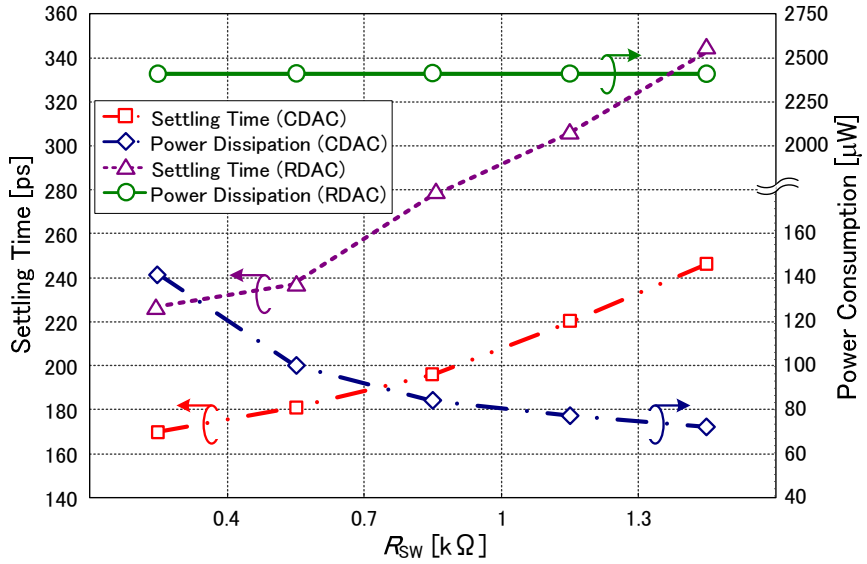


Figure 3.14 Simulation results of power consumption and settling time vs. $R_{SW}$.

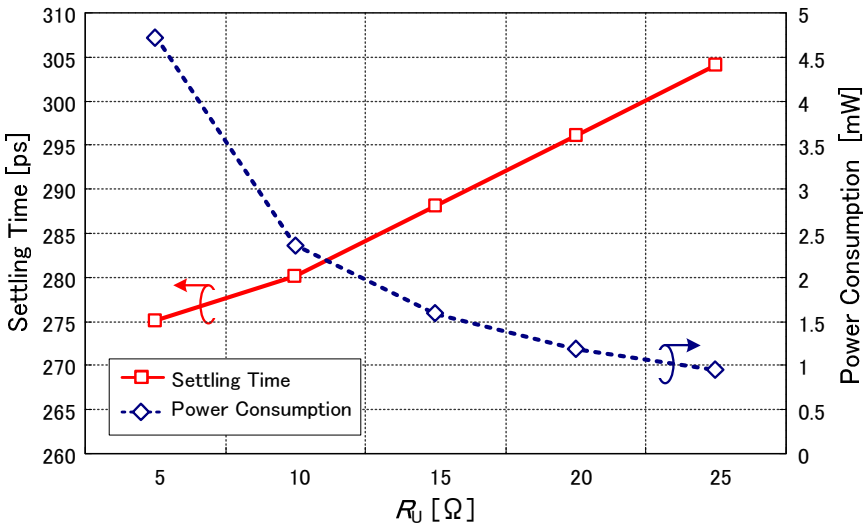


Figure 3.15 Simulation results of power consumption and settling time vs. $R_U$ in RDAC.

μW vs. 2.4 mW at 700 MHz sampling frequency. The power consumption of the CDAC is changed with sampling frequency because it works like a digital CMOS circuit. Although the RDAC partially consumes dynamic power, the main source of its power consumption is static current. Therefore, the power consumption in the RDAC barely changes with increasing the sampling frequency.

The simulation results of the power consumption and the settling time vs. $R_{SW}$ are shown in Figure 3.14. The CDAC shows faster settling by more than 60 ps under the same $R_{SW}$ condition. The settling times of the CDAC and the RDAC become faster with decreasing $R_{SW}$; however, power consumption also increases due to the parasitic capacitance. For the RDAC, the power variation is quite unnoticeable because the power consumption is dominated by the static current in the resistor ladder in RDAC.

The effect of $R_U$ to the power consumption and the settling time in the RDAC is shown in Figure 3.15. $R_U$ affects both of the power consumption and the settling time, especially the power consumption. However, even if $R_U$ is set to 5 Ω, the RDAC's settling time is still larger than that of the CDAC. According to Figure 3.15, 10 Ω to 15 Ω is reasonable value of $R_U$ in consideration of the settling time and the power consumption.

### 3.2.5.3 Noise

Contrary to the previous analysis, noise analysis has to consider both the sampling phase and the holding phase. Figure 3.16 shows the circuit models of the CDAC for noise analysis. During the sampling phase, all of $C_U$ charges noise. During the holding phase, each series

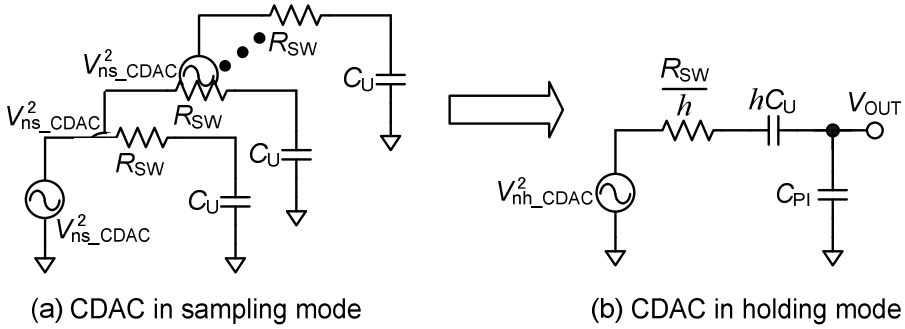


Figure 3.16 Circuit model of CDAC for noise analysis.

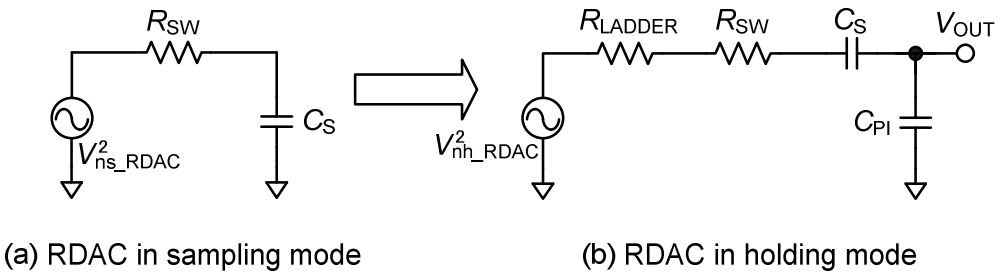


Figure 3.17 Circuit model of RDAC for noise analysis.

connected $R_{SW}$ and $C_U$ is seen as a parallel connection at node $V_{OUT}$, and the charged noise is distributed to $C_{PI}$. Finally, adding up the noise during two phases, the total noise is represented in (3.8).

$$V_{n\_CDAC}^2 = kT\left(\frac{1}{hC_U} + \frac{1}{C_{PI}\left(1+\frac{C_{PI}}{hC_U}\right)}\right) \tag{3.8}$$

Noise analysis for the RDAC is simpler than the CDAC since there is only one signal path as shown in Figure 3.17. During the sampling and the holding phases, circuits can be simplified to a RC network. Calculation result is represented in (3.9), which is identical to (3.8) when $h^* C_U = C_S$.

$$V_{n\_RDAC}^2 = kT\left(\frac{1}{C_S} + \frac{1}{C_{PI}\left(1+\frac{C_{PI}}{C_S}\right)}\right) \tag{3.9}$$

Although the noise calculation results of the CDAC and the RDAC are the same, it has to be considered that the difference of resistance between the two DACs. During the sampling phase, both of the DACs utilize the same switches; this means the charged noise are equal. The difference appears during the holding phase. $R_{SW}$ of the CDAC is divided by $h$ due to its parallel connection. On the other hand, $R_{SW}$ of the RDAC is shown as it is. Moreover, the RDAC incorporates resistor ladder, which is another noise source.

If noise bandwidth is considered to infinity, total noise of the two DACs becomes the same. However, the bandwidth is limited by the subsequent circuit, in this case, comparators in the fine ADC. Therefore, the accurate noise has to be analyzed with the bandwidth limitation by the comparators.

#### 3.2.5.4 Comparison Summary

In chapter 3.2.5, the CDAC and the RDAC are compared in settling time, power consumption and noise. The comparison results are organized in Table 3.2. Through the comparison, the

Table 3.2 Performance comparison table of CDAC and RDAC.

| | CDAC | RDAC |
|---|---|---|
| Settling time | **Fast** | Slow |
| Power consumption | **Low** | High |
| Noise | - | - |

CDAC shows better performance than the RDAC in settling time and power consumption. For noise, both of DACs show the same characteristics. The amount of noise is determined not the DAC circuit itself but the following circuit's parasitic capacitance. As the results, the CDAC shows better performance than the RDAC, especially, around several hundred of operating frequency. Therefore, it is reasonable to incorporate the CDAC for the proposed subranging architecture.

## 3.3 ADC Implementation

### 3.3.1 CDAC with S/H

The CDAC is composed of 17 unit capacitors ($C_U$) and one capacitor to make the offset voltage for one bit redundancy as shown in Figure 3.18, where one side of circuitry of differential scheme is illustrated. The unit capacitance is 15 fF and it samples and holds the input signal like the CDAC in a SAR ADC. Sampling switches use bootstrapping technique to reduce the on-resistance and the signal distortion.

When $\Phi_S$ goes high, $V_{IN}$ is sampled into the capacitors. Next, $\Phi_H$ goes high, capacitors are connected to $V_{REFP}$ or $V_{REFN}$ depending on the results of the coarse conversion. Considering parasitic capacitance $C_{PI}$, $V_{OUT}$ can be represented as below,

$$V_{OUT} = \frac{C_U\{(mV_{REFP} + nV_{REFN}) - (m+n)V_{IN}\} + C_{OFS}V_{OFS}}{C_U(m+n) + C_{PI}} \tag{3.10}$$

where $m$ and $n$ are the number of capacitors which connected to $V_{REFP}$ or $V_{REFN}$, respectively. $C_{OFS}$ and $V_{OFS}$ mean capacitor and reference voltage to generate offset voltage for one bit redundancy. Equation (3.10) indicates that $C_{PI}$ reduces $V_{IN}$ swing range, which causes the conversion range issue of the conventional subranging ADC. The proposed subranging ADC addresses this issue by introducing the interpolation technique.

#### 3.3.1.1 Mismatch of the CDAC

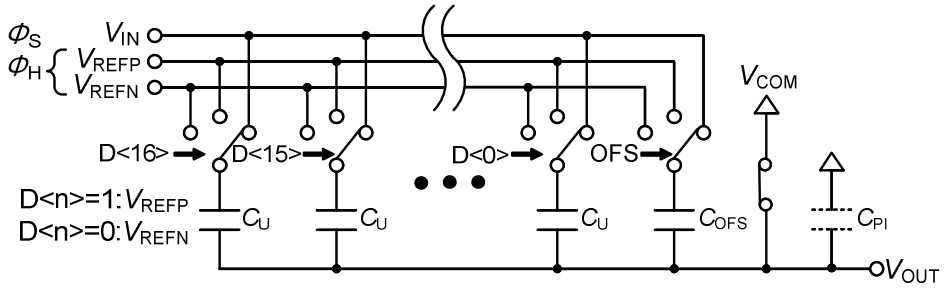


Figure 3.18 CDAC with S/H circuit.

The size of the unit capacitor has to be set with consideration of the mismatch error. Especially for the CDAC, the DNL error is affected by not only the capacitor mismatch but also the number of the unit capacitors.

The total capacitance of the CDAC is decided by noise of the circuit. Because the total capacitance is fixed, the unit capacitance and the number of capacitors are inversely proportion. Therefore, if the number of unit capacitors increase, the mismatch of the CDAC is also increased. The DNL error calculation result per sigma with consideration of the mismatch and the number of unit capacitors is represented in (3.11)

$$\boldsymbol{DNL}(\sigma)[\mathrm{LSB}] = 2^{N}\frac{\Delta C_{\mathrm{total}}}{C_{\mathrm{total}}}(\sigma)\frac{1}{\sqrt{\boldsymbol{h}}}\sqrt{1-\frac{1}{\boldsymbol{h}}} \tag{3.11}$$

where $N$ is the resolution of the ADC, $C_{\mathrm{total}}$ is the total capacitance of the CDAC, and $h$ is the number of capacitors in the CDAC. When the unit capacitance is decreased, the mismatch of the unit capacitance is increased with $\sqrt{h}$. However, in the CDAC, the output error caused by the mismatch of the unit capacitance is also suppressed by $1/h$, because the signal range is divided by $h$. Finally, DNL error is reduced by about $1/\sqrt{h}$. The maximum INL(σ) can be derived from DNL(σ) as below,

$$\boldsymbol{INL}_{\mathrm{MAX}}(\sigma)[\mathrm{LSB}] = \boldsymbol{DNL}(\sigma)\times\sqrt{\frac{\boldsymbol{h}}{2}}. \tag{3.12}$$

The calculation result of DNL(σ) is 0.011 LSB and the maximum INL(σ)is 0.03 LSB. See Appendix. A for more details.

Figure 3.19 shows the maximum INL(σ) simulation results with 100 times iteration. The averaged maximum INL(σ) is 0.0292 LSB, which shows good matching with the calculation. Target specifications of the INL & the DNL are less than 0.25 LSB each; therefore, the CDAC satisfies the requirements with plenty of margin.

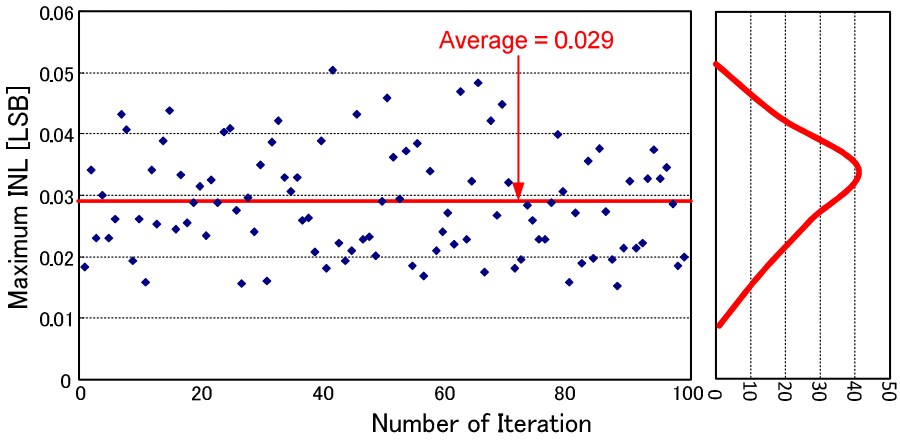


Figure 3.19 Simulation results of the maximum INL.

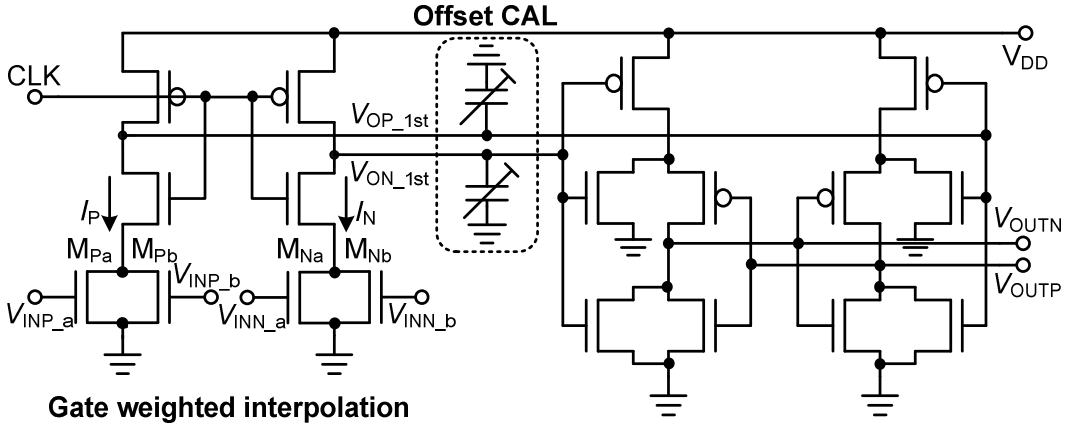


Figure 3.20 Double-tail latched comparator with interpolation and offset calibration.

### 3.3.2 Comparator with Gate-Weighted Interpolation

The double-tail latched comparator with gate-weighted interpolation shown in Figure 3.20 is employed in the proposed ADC. The comparator consists of 4 input MOS transistors for interpolation. The gate-weighted interpolation technique is very effective to reduce the power consumption by reduction of circuit components. The interpolation method which is incorporated in [3.15] utilizes the on-conductance of a transistor in the linear region. In contrast, the proposed ADC realized the interpolation in the saturation region.

Drain current in the saturation region of a classical long channel MOS transistor exhibits a square-law relationship to ($V_{GS}$- $V_{TH}$) and causes nonlinearity error when using for an interpolation. However, the drain current of the recent scaled MOS transistor is proportional to ($V_{GS}$- $V_{TH}$) due to the heavy velocity saturation effect. The drain current of the input transistor, $I_D$, can be expressed as

$$\boldsymbol{I}_{\mathrm{D}} \approx \alpha \boldsymbol{W} \left( \boldsymbol{V}_{\mathrm{GS}} - \boldsymbol{V}_{\mathrm{TH}}' \right) \tag{3.13}$$

where α is coefficient, $W$ is the gate width, and $V_{TH}$' is the effective threshold voltage. We used the value of 290 mV as the $V_{TH}$'.

In Figure 3.20, current $I_P$ is the sum of the currents in $M_{Pa}$ and $M_{Pb}$. Also, $I_N$ is the sum of the currents in $M_{Na}$ and $M_{Nb}$. The current $I_P$ is represented as below

$$\boldsymbol{I}_{\mathrm{P}} = \alpha \left\{ \boldsymbol{W}_{\mathrm{Pa}} \left( \boldsymbol{V}_{\mathrm{INP\_a}} - \boldsymbol{V}_{\mathrm{TH}}' \right) + \boldsymbol{W}_{\mathrm{Pb}} \left( \boldsymbol{V}_{\mathrm{INP\_b}} - \boldsymbol{V}_{\mathrm{TH}}' \right) \right\} \tag{3.14}$$

where $W_{Px}$ means the gate width of the MOS transistor $M_{Px}$. Equation (3.14) shows that $I_P$ can be controlled by changing gate width, $W_{Px}$, even if the input voltages are not changed. The ratio between $W_{Pa}$ and $W_{Pb}$ is set by the ratio of the interpolation. The $I_N$ is also

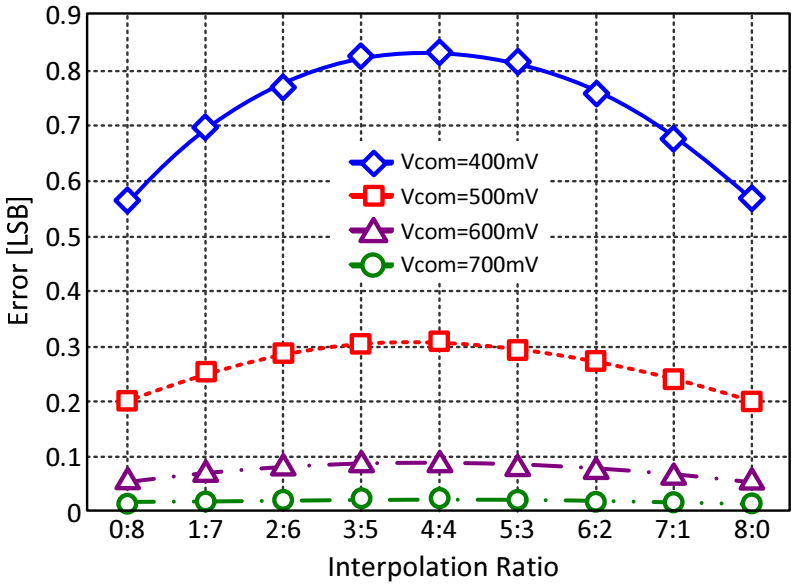


Figure 3.21 Simulation results of nonlinearity error in 3-bit interpolation.

calculated in the same way. Comparators in each interpolating points compare using each $I_P$ and $I_N$. This concept is shown in Figure 3.7.

The simulation results of the interpolation error using the same size of the input MOS transistor is shown in Figure 3.21. The simulated interpolation range is assigned $\pm$100 mV from $V_{COM}$ voltage. The interpolation error is less than 0.1 LSB when $V_{COM}$ voltage is higher than 600 mV. Therefore, in those $V_{COM}$ voltages, the gate-weighted interpolation can be realized with sufficient accuracy. However, it is difficult to realize the interpolation with $V_{COM}$ of less than 500 mV, due to the increase of nonlinearity.

### 3.3.3 Offset Calibration

An offset calibration technique by adjusting capacitance [3.16] is incorporated to the

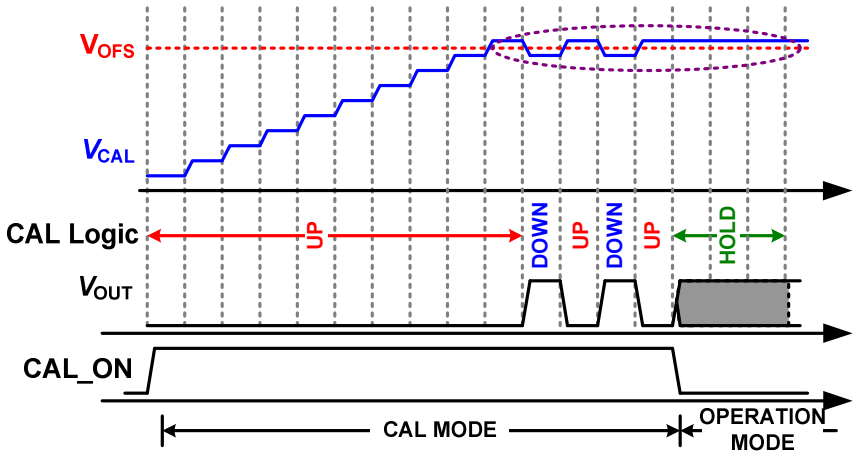


Figure 3.22 Process of offset voltage calibration.

comparators in the fine ADC. 4-bit binary weighted PMOS varactors are used as voltage controlled capacitors. The gate size of a unit varactor is 200 nm x 100 nm.

Figure 3.22 shows the calibration process. In Figure 3.22, $V_{CAL}$ is the calibration voltage in the calibration logic and $V_{OFS}$ is the offset voltage of the comparator. During calibration mode, all input nodes of the comparator are connected to the common-mode voltage. Since all input nodes are the same, the output is determined by the offset voltage. Therefore, calibration logic changes the calibration code to cancel the offset voltage; as a result, $V_{CAL}$ gets closer to $V_{OFS}$. When $V_{CAL}$ approaches to $V_{OFS}$ within voltage difference of one bit resolution of calibration, the calibration process is ended. After that, calibration code oscillates around the best calibration result. The comparator incorporates 4-bit calibration that operates at the same frequency as the main clock resulting in a merely 16 clock cycles calibration process. The resolution of the calibration logic is about 2 mV, which is small enough for the 1/2 LSB (about 9 mV) of the proposed ADC. The number of bit for calibration is determined by Monte Carlo simulation.

The Monte Carlo simulation results show that large mismatch of about 10 mV (σ) can be suppressed to 0.9 mV (σ) with calibration. The propagation delay with calibration at the input drive voltage of 1 mV is 140 ps and consumed energy for one conversion is 63 fJ/conv.. The input referred noise voltage is about 0.7 mV per sigma of which value is reduced to 64% for the comparator without offset calibration. The increase of node capacitance reduces input referred noise voltage.

#### 3.3.3.1 Offset Calibration at each Interpolating Point

The introduced offset calibration technique adjusts the slew rate at the $V_{OP\_1st}$, $V_{ON\_1st}$ nodes in Figure 3.20. This slew rate is affected by not only capacitance at the nodes of the $V_{OP\_1st}$ and $V_{ON\_1st}$ but also by the input common-mode voltage. During the calibration mode, all of the comparators are using the same input common-mode voltage. However, in the operation mode, each comparator has a different interpolation ratio, this also means that the input common-mode voltage of each comparator is different. This common-mode voltage difference results in the difference of slew rate between the calibration mode and the operation mode. Therefore, it is necessary to verify that the offset calibration method is effective to reduce the offset voltage for each interpolating point with different input common-mode voltage.

To examine the effect of input common-mode voltage, we introduced variation of $V_{eff}$ against variation of the capacitance at the output nodes such as $V_{OP\_1st}$ and $V_{ON\_1st}$. The result is shown in (3.15).

$$\frac{\partial V_{off}}{\partial C_{o\_1st}} = -\frac{V_{eff}}{2C_{o\_1st}} \tag{3.15}$$

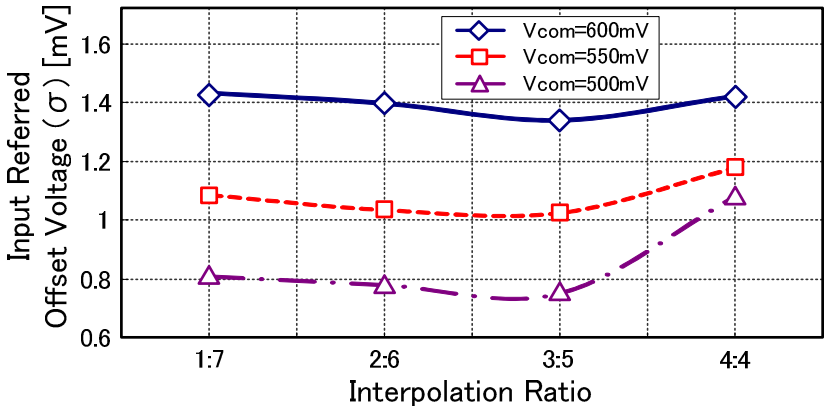


Figure 3.23 Input referred offset voltage after calibration at each interpolation point.

where $V_{off}$ is the offset of the comparator, $V_{eff}$ is ($V_{GS}$-$V_{TH}$) of the input MOS transistor and $C_{o\_1st}$ is the capacitance at the output nodes of $V_{OP\_1st}$ and $V_{ON\_1st}$. Equation (3.15) shows the variation of the offset voltage is proportional to $V_{eff}$; therefore, it is effective to reduce $V_{eff}$ to achieve more accurate offset calibration.

The 1000 times Monte Carlo simulation results of input referred offset voltage after calibration at each interpolating point for 3 common-mode voltages are shown in Figure 3.23. The simulation results show that the offset calibration is effective for all interpolation ratios even if the common-mode voltage is changed from 500 mV to 600 mV. This means that the variation of the slew rate is small enough.

## 3.4 Experimental Results

The proposed ADC has been fabricated in a 90 nm CMOS technology. Figure 3.24 shows chip micro-photograph and layout of the ADC, which occupies an active area of 0.13 mm$^2$.

Figure 3.25 shows the measured DNL and INL at the conversion rate of 700 MS/s after the offset calibration. The DNL is less than +0.6 / -0.6 LSB and the INL is less than +0.8

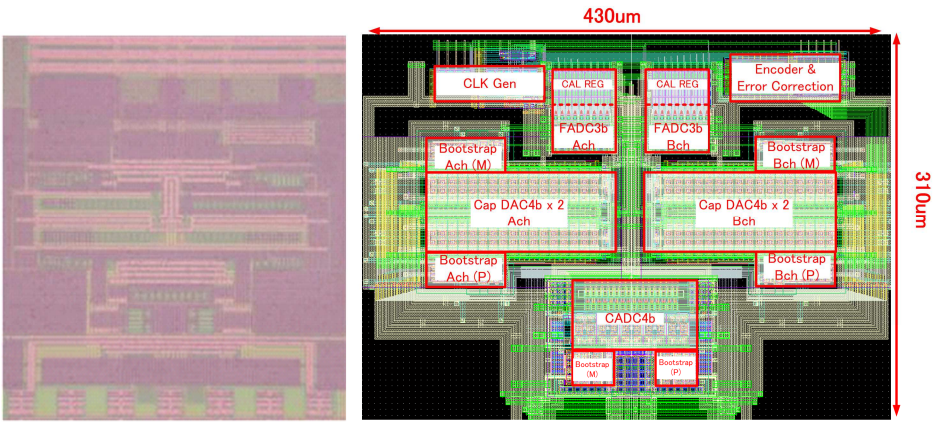


Figure 3.24 Chip micrograph and layout.

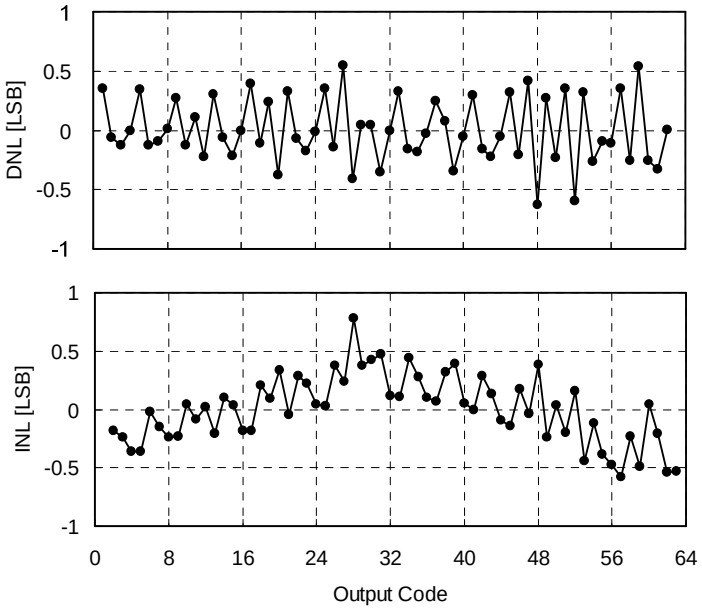


Figure 3.25 INL and DNL at 700 MS/s after calibration.

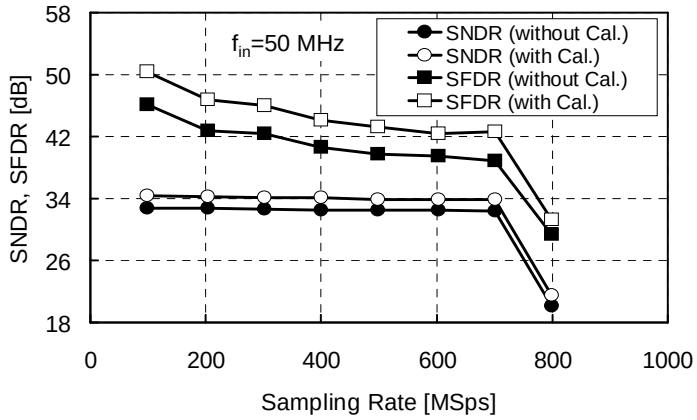


Figure 3.26 SFDR and SNDR vs. sampling rate.

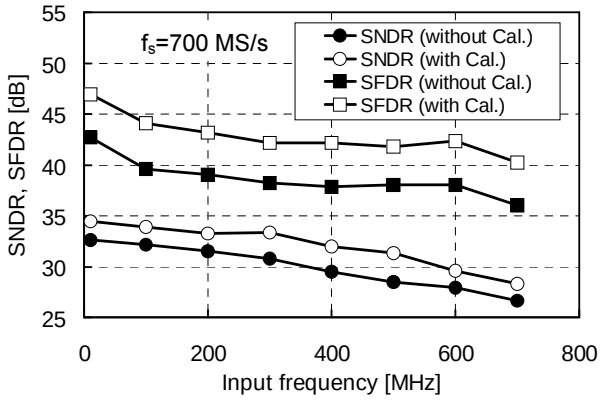


Figure 3.27 SFDR and SNDR vs. input frequency.

Table 3.3 ADC performance summary.

| Refer-ence | Technology [nm] | Resolution [bits] | $F_S$ [GS/s] | Power [mW] | SNDR (DC/Nyq.) [dB] | FoM [pJ/conv.] | Active area [mm$^2$] | Supply Voltage [V] | Architecture |
|---|---|---|---|---|---|---|---|---|---|
| [3.2] | 90 | 6 | 3 | 90 | 37/34 (500 MHz) | 4.6 | 0.28 | 1.2 | Flash |
| [3.3] | 45 | 6 | 1.2 | 28.5 | 36/34 | 0.45 | 0.1 | 1.2 | Flash |
| [3.7] | 65 | 6 | 1 | 6.27 | 31.5/28.5 | 0.21 | 0.11 | 1.2 | SAR, Interleaving |
| [3.8] | 40 | 6 | 2.2 | 2.6 | 31.6/29.6 | 0.04 | 0.03 | 1.1 | Pipeline, Interleaving |
| [3.17] | 90 | 6 | 2.7 | 50 | 36.5/33.6 | 0.47 | 0.36 | 1 | Folding, Interleaving |
| This Work | 90 | 6 | 0.7 | 7 | 35/34 | 0.25 | 0.13 | 1.2 | Subranging |

/ -0.6 LSB. The DNL/INL results are not as good as our expectation. The most likely reason for the degraded performance is the offset of the comparators in the coarse ADC, which don't incorporate offset calibration logic. If the offset voltage is large enough to affect the accuracy of the coarse ADC, the DNL/INL are degraded. About 16 periodic error patterns in the measurement results support our expectation.

Figure 3.26 shows the SFDR and the SNDR vs. the sampling rate when the input signal frequency is about 50 MHz. The SNDR maintains higher than 34 dB (5.3 bit) until 700 MS/s and drops down to 20 dB (3 bit) at 800 MS/s. Figure 3.27 shows the dependency of SNDR on the input frequency at 700 MS/s. The curve shows the SNDR of 34 dB (5.3 bit) is maintained up to the Nyquist input frequency of 350 MHz. The power consumption is only 7 mW at the conversion rate of 700 MS/s. The Figure of merit, as calculated with

$$\mathrm{FoM} = \frac{P_D}{F_S \cdot 2^{ENOB}} \tag{3.16}$$

of 250 fJ/conversion steps.

Table 3.3 summarizes the ADC performance of this work and the recently published ADCs in the same resolution and similar target specification. As shown in Table 3.3, the proposed ADC consumes less power than other ADCs except [3.7] and [3.8]. [3.2] and [3.3] achieved high-speed operation; however, they have large power consumptions due to use of the flash architecture. [3.17] also achieves high-speed operation; however, the power consumption is also large. The ADC in [3.8] shows very impressive performance but 4-times interleaving makes the design difficult. [3.7] shows similar performance of the proposed subranging ADC, however, it is necessary to examine the timing margin carefully because of the interleaving scheme.

## 3.5 Conclusion

The subranging architecture using CDAC, gate-weighted interpolation scheme and double-tail latched comparator with capacitive offset calibration has been demonstrated. By introducing the CDAC, better performance of power consumption, settling time and noise is achieved compared to the RDAC. A small area is also achieved by eliminating S/H circuit. A gate-weighted interpolation is implemented in the saturation region with sufficient performance for a 6-bit resolution ADC. This technique enables the realization of an interpolation in a simple way. Capacitive offset calibration reduces the comparator's offset dramatically from 10 mV to 1.5 mV per sigma. The fabricated ADC occupies 0.13 $mm^2$ die size and achieves 34 dB SNDR with Nyquist input frequency at 700 MS/s. The power consumption is only 7 mW and the attained FoM is 250 fJ/conv..

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# 4. Subranging ADC using Single CDAC Interpolation

## 4.1 Introduction

The subranging ADC in chapter 3 [4.1] - [4.2] achieved high-speed, small core area and small power consumption. However, the ADC still has some parts need to be improved. The large sampling capacitance is one of them. The subranging ADC in chapter 3 has 1 pF as a sampling capacitance for 6-bit resolution ADC. This large capacitance is caused by the two CDACs for the interpolation because the interpolation utilizes two differential signals. As a result of the two CDACs, the core area and the power consumption are increased. Also, the requirement of the bandwidth of the ADC input driver becomes severe. Therefore, if the subranging ADC can realize the interpolation with only one differential signal, the ADC can reduce the number of CDAC and benefits the power consumption, the core area, and the performance requirement of the ADC input driver.

In this chapter, a 6-bit subranging ADC with interpolation technique using only one differential signal and two DC reference voltages is presented. Chapter 4.2 shows the principle of the proposed new interpolation technique. Chapter 4.3 presents the proposed ADC architecture and the composition of the fine stage. The simulation results are shown in chapter 4.4 and the chapter is concluded in chapter 4.5. In this chapter, “previous interpolation” indicates the interpolation using two differential signals and “proposed interpolation” indicates the interpolation using one differential signal and two DC voltages which is introduced in this chapter.

## 4.2 Interpolation using Two Single Slope Signals and Common Level Voltage

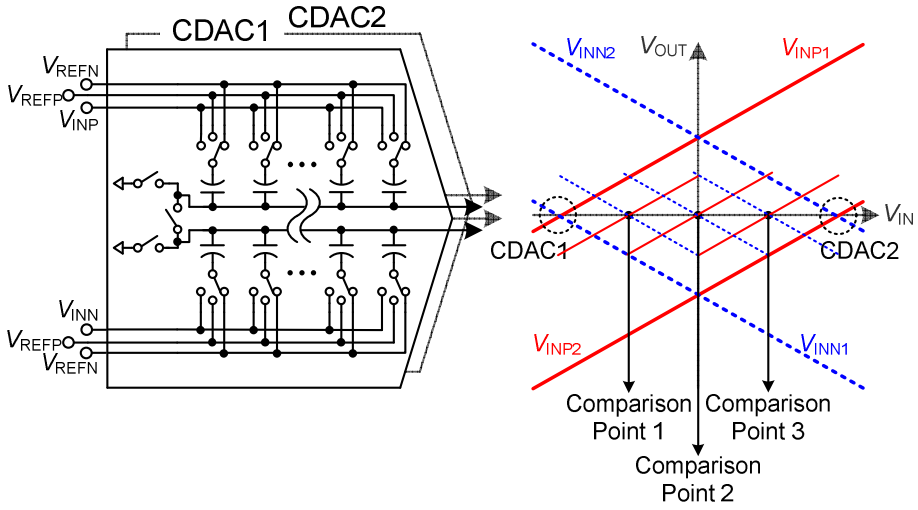


Figure 4.1 CDACs and interpolated signals of previous interpolation.

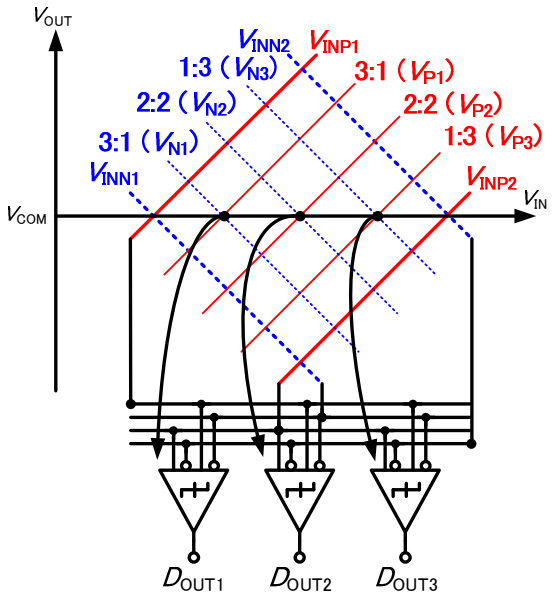


Figure 4.2 Comparison using two differential signals.

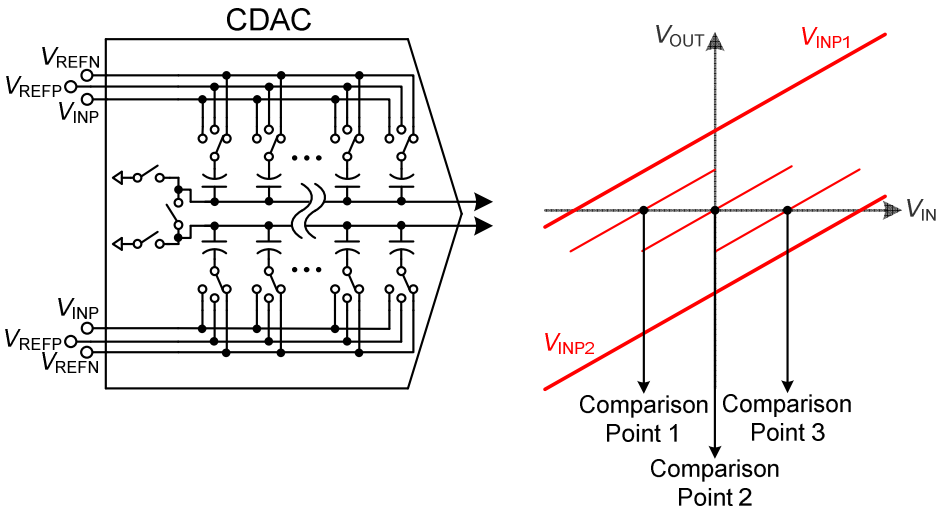


Figure 4.3 CDAC and interpolated signals using single slope signals.

In the previous interpolation, the gate-weighted interpolation (Chapter 2.4.3) using weight controlled CDAC (chapter 3.3.1) are used for the comparison. The CDAC also uses interpolation technique to output the signal in proper range. Figure 4.1 depicts the CDACs and interpolated signals of the previous interpolation. Figure 4.2 explains the A/D conversion of the 2-bit sub-ADC. In Figure 4.2, the comparator utilizes differential interpolated signal for the comparison. However, the same comparison can be performed by two single slope signals and common-mode voltage, such as $V_{INP1}$, $V_{INP2}$ and $V_{ICOM}$ in Figure 4.2.

Figure 4.3 depicts the conceptual diagram of the interpolation using two single slope signals. By using this interpolation, the circuit size of the CDAC becomes half and the negative signals are not necessary. The basic operation is completely same as the

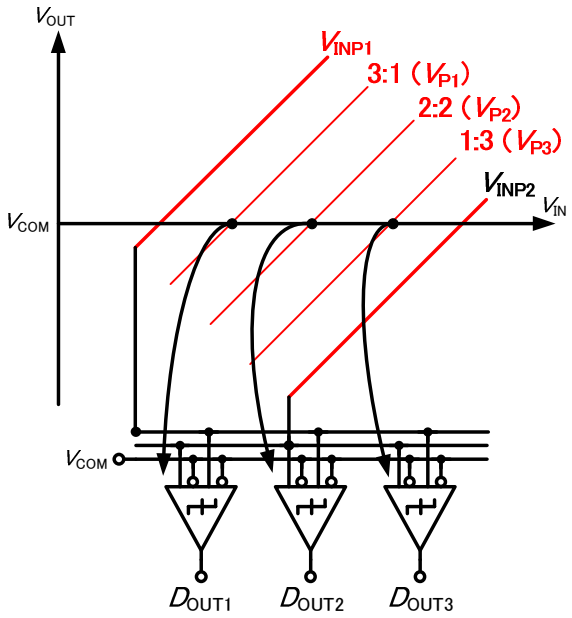


Figure 4.4 Comparison using two single slope signals.

interpolation in Figure 4.1. Figure 4.4 shows the comparison of the interpolation using two single slope signals. Different from the Figure 4.2, there are no differential signals. To make comparison using only single slope signals, the common-mode voltage ($V_{COM}$) is utilized.

The comparison points between two interpolation methods are the same even though CDAC circuit is reduced in half. However, the use of only single slope signals degrades the SNR characteristics because the single signals are weak against the noise. Especially in the recently developed SoC, the digital circuit and the analog circuit are implemented in the same substrate and distance between two signal domain areas becomes closer. It means the noise caused by the digital circuit (signal variation through the parasitic capacitance by digital signal) becomes larger. Therefore, using the only single slope signals has to be rejected so far as possible.

## 4.3 Proposed Interpolation using One Differential Signal and Two DC Voltages

The performance degradation by the interpolation using single slope signals can be suppressed using differential signals instead of the single slope signals. The proposed interpolation technique in this chapter allows realizing the interpolation and the comparison using only one differential signal and two DC voltages. Figure 4.5 shows the CDAC and the conceptual diagram of the proposed interpolation technique. As shown in Figure 4.5, the proposed interpolation technique utilizes only one differential signal. To realize the interpolation, the proposed interpolation introduces two DC voltages, such as $V_{REFPF}$ and $V_{REFNF}$ in Figure 4.5.

Figure 4.6 compares and explains the operation of the previous interpolation technique and the proposed interpolation technique. As explained in chapter 3.2.4, the

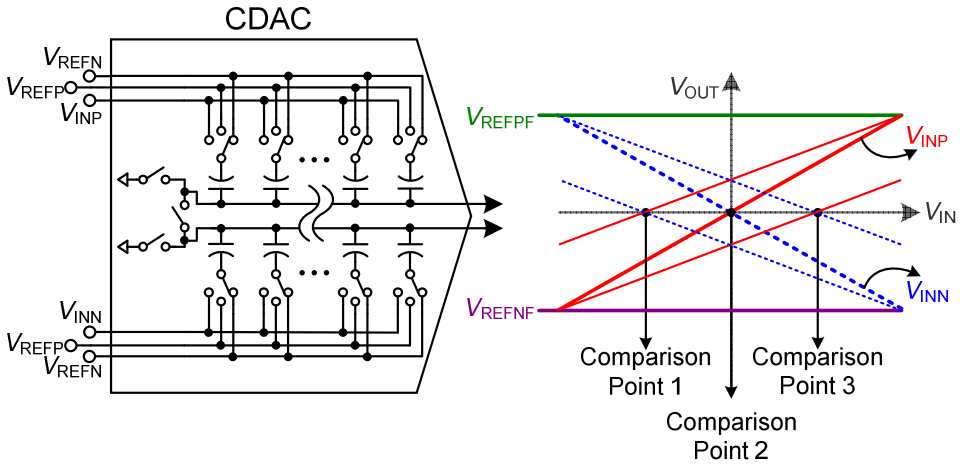


Figure 4.5 CDAC and interpolated signals using one differential signal and DC voltages.

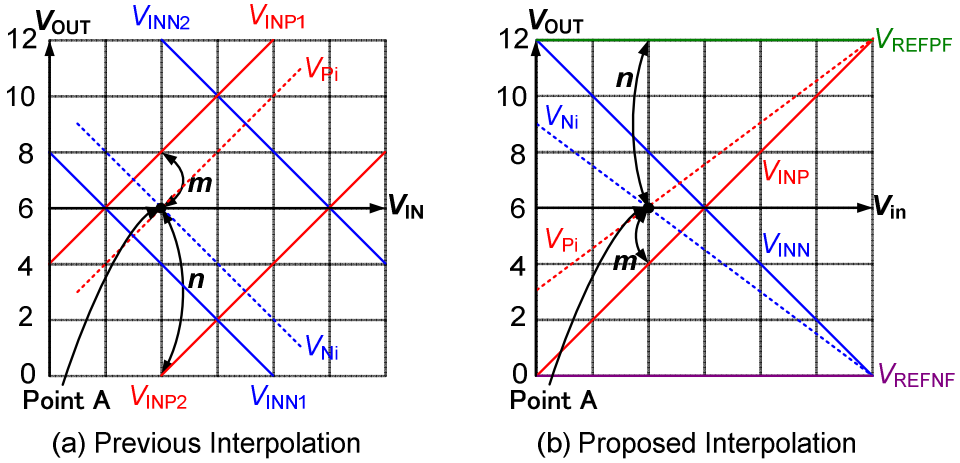


Figure 4.6 Comparison of previous interpolation and proposed interpolation.

previous interpolation divides between two signals with certain ratio, $m$ : $n$ using positive slope signals in Figure 4.6. The negative slope signals can be interpolated in the same way. The previous interpolation can be written as (3.2) and (3.3). In contrast, the proposed interpolation divides between an input signal (having slope) and a DC voltage. This is possible because the interpolation does not have to utilize the same slope signals. The other words, the interpolation still work with a slope signal and a DC voltage. The proposed interpolation can be written as (4.1).

$$V_{\mathrm{N,Pi}} = \frac{m \cdot V_{\mathrm{INN,P}} + n \cdot V_{\mathrm{REFN,PF}}}{m + n} \tag{4.1}$$

Figure 4.6 indicates that the proposed interpolation can realize the same operation with the previous interpolation. For example, to make a comparison at the point A, the previous interpolation and the proposed interpolation can be expressed as below, (4.2) and (4.3) respectively.

$$\frac{3\cdot V_{INP1}+1\cdot V_{INP2}}{3+1}=\frac{3\cdot 8+1\cdot 0}{4}=6 \tag{4.2}$$

$$\frac{3\cdot V_{INP}+1\cdot V_{REFPF}}{3+1}=\frac{3\cdot 4+1\cdot 12}{4}=6. \tag{4.3}$$

In (4.2) and (4.3), only positive interpolation is considered.

The A/D conversion using the proposed interpolation is depicted in Figure 4.7. The three comparison points are same as the previous interpolation. Different from the other interpolation techniques, the proposed interpolation has to be careful of the signal connection because the connected signals are changed at the middle interpolating point. For example, interpolations in the left side from the middle interpolating point use $V_{INP}$ and $V_{REFRF}$; however, interpolations in the right side from the middle interpolating point use $V_{INP}$ and $V_{REFN}$.

## 4.4 ADC Architecture and Simulation Results

Figure 4.8 depicts 6-bit subranging ADC architecture using the proposed interpolation technique. The basic composition of the proposed subranging ADC is same as the ADC in chapter 3. The coarse ADC, CDAC, and error correction logic has the same structure. The difference is come from the different interpolation technique, for example, reduced CDAC circuit and different fine ADC structure (gate-weighted interpolation). The proposed subranging ADC does not incorporate interleaving of the fine stages because it focuses small

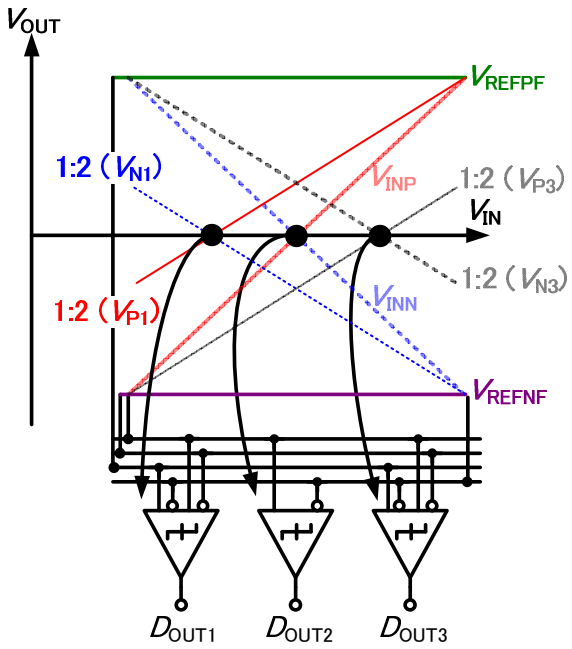


Figure 4.7 A/D conversion using one differential signal and two DC voltages.

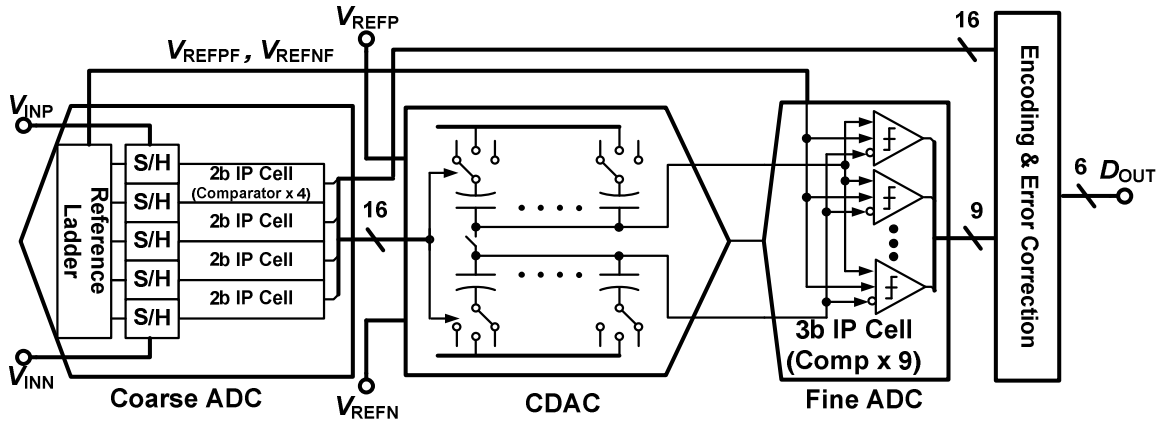


Figure 4.8 ADC structure using one differential signal and two references interpolation.

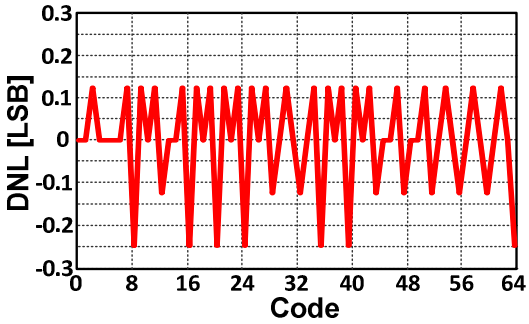


Figure 4.9 DNL simulation result at 500 MS/s.

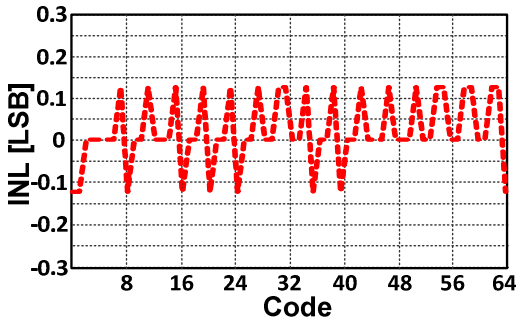


Figure 4.10 INL simulation result at 500 MS/s.

power consumption and small area.

Figure 4.9 and Figure 4.10 shows DNL / INL simulation results, respectively. The simulations are performed at the 500 MHz sampling frequency. The simulation results show that DNL is less than +0.15 / -0.25 and INL is less than +0.15 / -0.15, which are enough high performance for the ADC. Figure 4.11 shows the simulation results of sampling frequency vs. ENOB. The input frequency in each simulation is assigned as Nyquist frequency. ENOB keeps higher than 5.9 bit until 500 MHz of the sampling frequency. After 500 MS/s, the ENOB starts to degrade. The main reason of the performance degradation in the high sampling frequency is the settling error of the CDAC during the reference selection. The

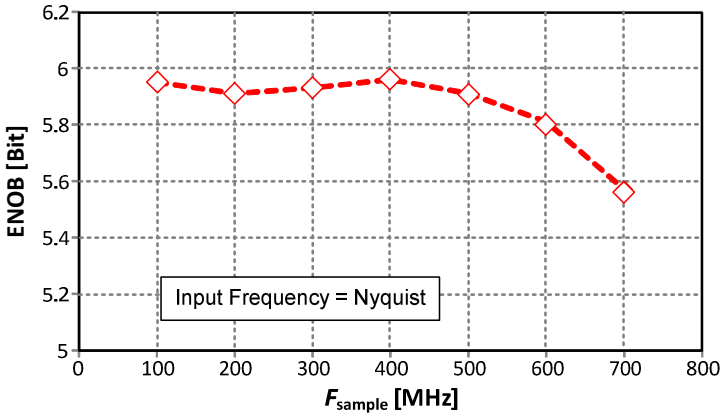


Figure 4.11 Simulation result of sampling frequency vs. ENOB.

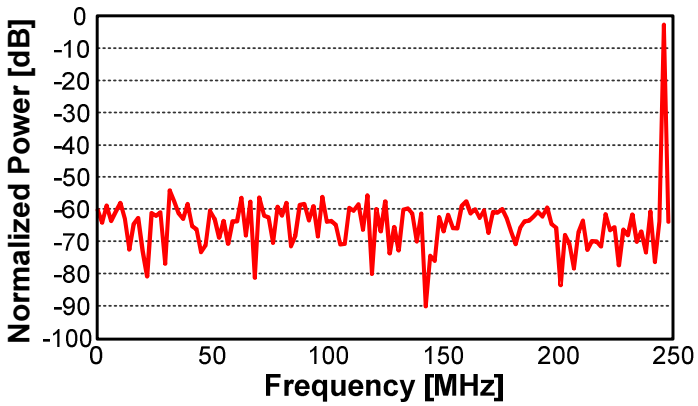


Figure 4.12 FFT simulation result at 500 MS/s and Nyquist input.

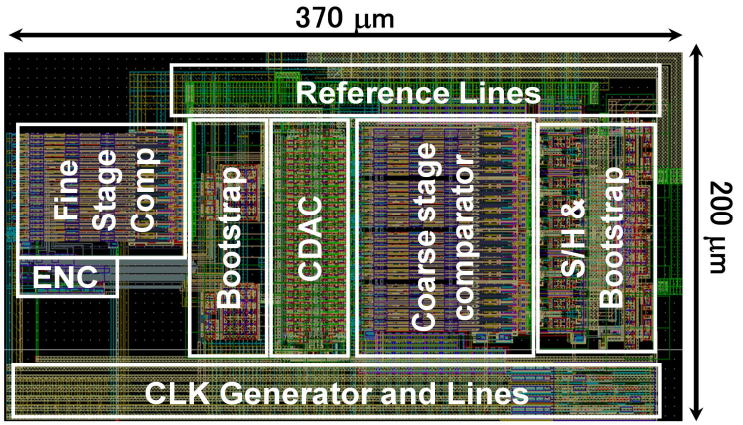


Figure 4.13 Proposed subranging ADC core layout.

settling error can be relaxed by the fine stage interleaving like the previous subranging ADC in chapter 3. Figure 4.12 depicts FFT simulation results at 500 MS/s with Nyquist frequency input. The spurious level is lower than -55-dB. Figure 4.13 shows layout of the proposed 6-bit subranging ADC. The core area is 0.074 $mm^2$. The core size can be reduced by the layout optimization.

Table 4.1 Recently published 6-bit ADCs.

| Reference | Technology [nm] | $F_S$ [GS/s] | $P_D$ [mW] | SNDR [dB] | FoM [pJ/conv.] | Active area [mm²] |
|---|---|---|---|---|---|---|
| [4.2] | 90 | 0.7 | 7 | 35 | 0.25 | 0.13 |
| [4.3] | 45 | 1.2 | 28.5 | 36 | 0.45 | 0.1 |
| [4.4] | 65 | 1 | 6.27 | 31.5 | 0.21 | 0.11 |
| [4.5] | 40 | 2.2 | 2.6 | 31.6 | 0.04 | 0.03 |
| This Work (Sim.) | 90 | 0.5 | 3.3 | 36 | 0.12 | 0.074 |

Table 4.2 Comparison with subranging ADC using two CDACs.

| Reference | $C_{sample}$ [pF] | $F_S$ [GS/s] | $P_D$ [mW] | FoM [pJ/conv.] | Area [mm²] |
|---|---|---|---|---|---|
| [4.2] | 2.7 | 0.7 | 7 | 0.25 | 0.13 |
| This Work (Sim.) | 1.7 (↓38%) | 0.5 (↓29%) | 3.3 (↓53%) | 0.12 (↓52%) | 0.074 (↓43%) |

Table 4.1 shows a performance comparison with recently published 6-bit ADCs. This subranging ADC shows a good performance in comparison with other ADCs. This comparison is not fare because the other ADC's results are measurement results. However, if the proposed subranging ADC is fabricated with small amount of performance degradation, the ADC supposed to show attractive performance, especially in power consumption, FoM and active area. The ADC in [4.5] shows outstanding performance among ADCs in the table. However, the ADC in [4.5] utilizes dynamic amplifier which is very sensitive to noise and jitter. Therefore, it is not easy to use in the industry. The proposed ADC's sampling speed is slower than others; however, it can be improved by the fine stage interleaving and circuit optimization. Table 4.2 shows the comparison results between the previous subranging ADC (chapter 3) and the proposed subranging ADC. The sampling capacitance is reduced by 38 %. The reduction amount cannot be over 50 % because sampling capacitance of the coarse stage does not changed, even though the CDAC is reduced in half. The power consumption and the core area are also reduced by the proposed interpolation technique. Consequently, FoM is reduced almost half, which means the proposed ADC achieved low-power consumption even though the sampling speed slower than the previous ADC.

### 4.4.1 Performance Degradation by Reference Variation

The previous subranging ADC in chapter 3 uses differential signals for the interpolation. Although the CDAC's gain is degraded by the parasitic capacitance in the input of the fine stage, the interpolation is performed without error because the differential signal has the same amount of degradation, as described in chapter 3.2.4. Therefore, if the CDAC satisfies noise and mismatch requirement, it is not necessary to care for the interpolation.

On the other hand, the proposed interpolation technique utilizes one differential signal and two DC reference voltages. It means that the interpolating point is varied with variation of the CDAC's output (differential signal) or reference voltages. Therefore, the proposed interpolation is very sensitive to the CDAC's gain degradation by the parasitic capacitance in the input node of the fine stage or reference voltage variation by the mismatch of the resistor ladder and noise. Figure 4.14 depicts the issues of the proposed subranging ADC. The signal degradation by the parasitic capacitance can be solved by adjusting the reference voltages in consideration of the parasitic capacitance using layout post extraction. Also, the reference voltage variation can be suppressed by the resistor ladder design with the

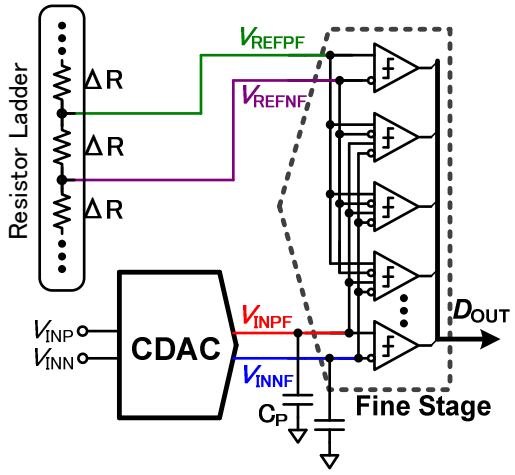


Figure 4.14 Reasons of reference variation and signal gain reduction.

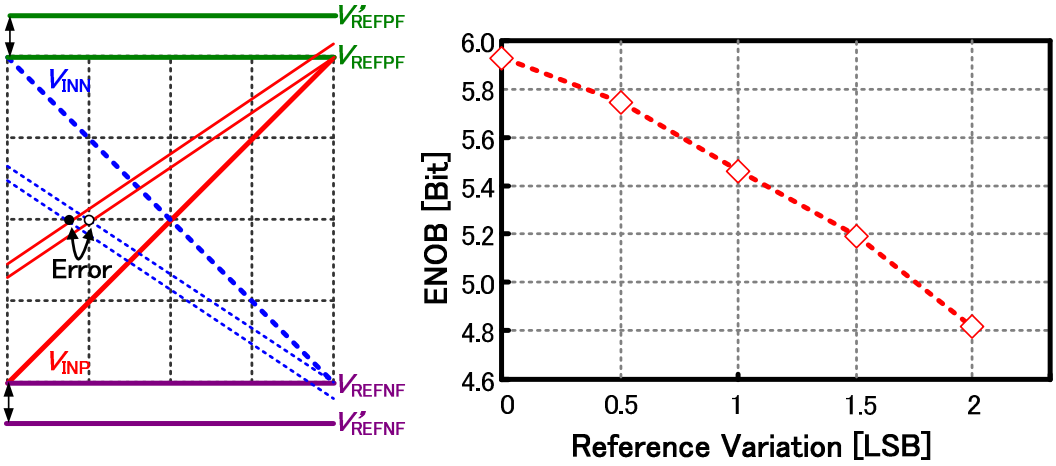


Figure 4.15 ADC performance degradation by reference variation.

mismatch consideration and noise.

It is necessary to figure out the effect of the issues to the ADC's performance. In the simulation, the CDAC's gain degradation is solved by the adjustment of the reference voltage range and the resistor ladder has small mismatch for the 6-bit ADC resolution. It is assumed that the reference voltage is varied by the noise or coupling through parasitic capacitor. Figure 4.15 shows the simulation results of the reference voltage variation vs. the ADC's ENOB. The amount of the variation is normalized to the LSB of the proposed subranging ADC. The simulation environment is 500 MS/s with Nyquist input frequency. According to Figure 4.15, when the reference voltage is varied 0.5 LSB, the ENOB is degraded 0.2 bit. The proposed ADC has 15.6 mV for 1 LSB. Therefore, if the reference voltage variation is suppressed less than 7 mV, the performance degradation is not severe. Even though the allowed reference voltage variation is small enough, adding a calibration circuit for control of reference voltage range is effective method to guarantee the ADC's good performance.

## 4.5 Conclusion

In this chapter, the interpolation technique using one differential signal and two DC reference voltages is introduced. The proposed interpolation technique can reduce the CDAC in half in comparison of the previous interpolation. Therefore, it has advantages in the core area, the power consumption, and the performance requirement for the ADC input driver. The 6-bit subranging ADC using the proposed interpolation method is also presented. The presented ADC achieves that DNL / INL are less than +0.15 / -0.25 LSB and +0.15 / -0.15 LSB, respectively. The ADC keeps the ENOB above 5.9 bit until 500 MS/s and Nyquist input in simulation. At that time, FoM is 0.12 pJ/conv. which is quite small value. The proposed ADC is attractive for the low-power and the small-area applications. It also has a potential to the high-speed operation by the fine stage interleaving. However, a designer has to be careful about the reference voltage variation for high-performance ADC implementation.

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# 5. Design of Interpolated Pipeline ADC using Low-gain Open-loop Amplifiers

## 5.1 Introduction

8 to 10-bit resolution with a conversion speed of hundreds of mega samples per second ADCs are widely used in wireless communication systems. The 8 to 10-bit resolution is high to realize by the subranging architecture. The pipeline ADC topology is suitable for those target specifications as shown in Figure 1.3. The conventional pipeline ADC requires a high gain op-amp for high-resolution. For example, more than 70-dB gain from the op-amp is required for a 10-bit resolution pipeline ADC. By technology scaling, digital circuits benefit from high-speed, low supply voltage, and small chip area. However, analog circuits suffer from low intrinsic gain and small signal swing due to the short channel effect and the low supply voltage. In the conventional pipeline ADC, insufficient op-amp gain might cause a residue amplification error in a pipeline stage. To realize a high gain op-amp with recent scaled technology, several techniques are required such as cascode, gain boosting, and multi-stage amplification. Although these techniques are applied, it is difficult to guarantee sufficient gain for high-resolution pipeline ADC. Furthermore, wide bandwidth of op-amp becomes hard to realize with these techniques due to insufficient phase margin.

Recently published pipeline ADCs solve this issue using calibration technique. [5.1] and [5.2] utilize LMS engine to calibrate capacitor mismatch of the MDAC stage, op-amp's insufficient gain and nonlinearity in the pipeline stage. However, the long-time requirement, the large area and the high power consumption of the calibration circuit are problematic. For example, [5.1] needs tens of thousands of clock cycles for calibration. The off-chip calibration circuit consists of approximately 20,000 gates and consumes 8 mW. The work in [5.2] achieves much less power consumption than [5.1], such as 1.13 mW. There is no information of the calibration time in [5.2]; however, it is possible to estimate that similar calibration time in [5.1] is required because the calibration methods are similar. In [5.3], the gain coefficients of stages are estimated in foreground calibration before the ADC operation. After the ADC starts its operation, background calibration compensates stage gain errors using coefficients estimated from the foreground calibration. This method reduces calibration time; however, additional MDAC stages are required for calibration and it causes extra power and area.

Several works have reported on calibrating stage gain error in the analog domain. In [5.4], reference voltage in each pipeline stage is controlled to adjust stage gain. However, this technique is only applicable when the linear settling of the op-amp is guaranteed. Moreover, reference voltage scaling reduces the voltage swing range of a pipeline stage and degrades SNR. Improving op-amp gain by forming positive feedback loop also has been reported in [5.5]. However, an auxiliary ADC for calibration and complicated calibration circuits degrade its attractiveness. A gain calibration technique of MDAC stage in [5.6] tunes the feedback

capacitance in op-amp. This calibration requires only 168 clock cycles, which is very small in comparison with the technique in [5.1]. However, additional capacitance in the output node of the op-amp reduces its bandwidth. As explained above, an incorporating calibration technique accompanies some disadvantages, such as increasing power consumption, core area, circuit complexity, and extra time for calibration. The issues of the calibration technique are described in chapter 2.6 in detail.

Recently, two pipeline ADCs, [5.7] and [5.8] have reported without MDAC stage's gain calibration. Both of the ADCs incorporate interpolation technique, which makes it possible to realize more than 10-bit ADCs with relatively low-gain amplifiers. In [5.7], a 12-bit, 800 MS/s with 4-times interleaved ADC is demonstrated, which is based on [5.9] - [5.10]. A 40-dB gain pseudo-differential amplifier is utilized in the MDAC stage. The offset of the amplifier is calibrated by a 9-bit DAC. In comparison with [5.7], the pipeline ADC in [5.8] achieves 10-bit, 320 MS/s using low-gain open-loop amplifiers. A 9.5-dB low-gain amplifier is used in [5.8] without any MDAC calibration. Open-loop topology brings other advantages, such as wide bandwidth and fast response.

In this chapter, the design of interpolated pipeline ADC is discussed based on [5.8]. Chapter 5.2 introduces the interpolation technique in the interpolated pipeline ADC and the pipeline stage structure. Chapter 5.3 analyzes the requirements of the linearity and noise characteristic to determine the amplifier's parameters. Chapter 5.4 details the effects of the parameter variation of the amplifier to the performance of the interpolated pipeline ADC, such as load capacitance and gain. Chapter 5.5 describes the resolution optimization in the 1st pipeline stage. After that, the design flow is suggested in chapter 5.6. And, this chapter is concluded in chapter 5.7.

## 5.2 Characteristic of Interpolated Pipeline ADC

### 5.2.1 Interpolation in Pipeline ADC

Many advantages of the ADC in [5.8] are based on the interpolation technique. Therefore, it is necessary to figure out the concept of the interpolation for further analysis and discussions. The principle of the interpolation technique is already explained in chapter 2. In this sub-chapter, the interpolation in the pipeline ADC is reviewed again briefly.

In circuit design, the interpolation can be defined as to construct a new signal with a certain ratio between two given signals by weight control of two signals. There are many methods to realize interpolation in circuit design. Figure 5.1 shows a circuit example for the 2-bit interpolation in a pipeline stage. Since two sets of signals are necessary for interpolation, there are two amplifiers and two interpolators in the stage. In Figure 5.1, the interpolator can be implemented with various components. For example, ADCs in [5.7], [5.11] - [5.15]

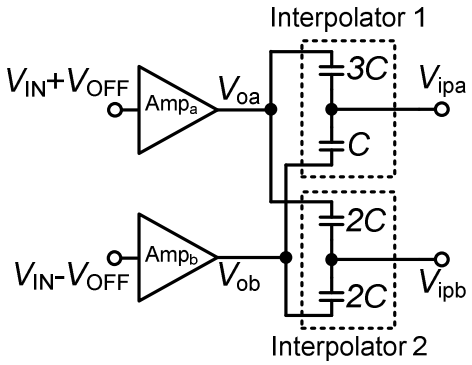


Figure 5.1 Block diagram of amplifier and interpolator.

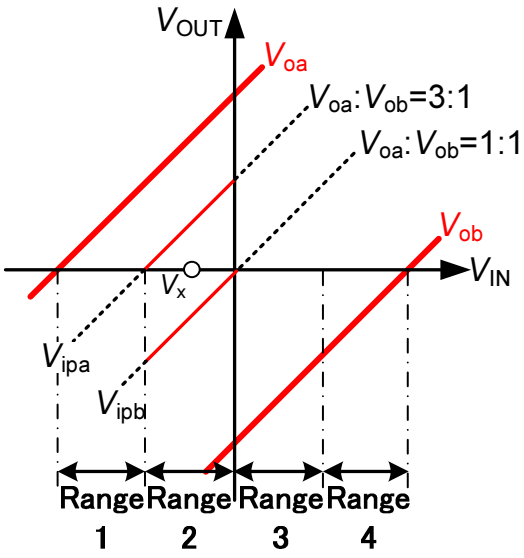


Figure 5.2 Interpolated signals with signal ranges.

realize interpolation using resistor ladder. Also, gate-weighted input MOS transistors of comparator are utilized to ADCs in [5.16] - [5.17] to realize interpolation. Other interpolation methods have been published in [5.18] - [5.20], which incorporate both of resistor ladder and capacitor. In this paper, it is assumed that the interpolator is implemented using capacitor array (CDAC). The CDAC has advantages of power consumption, settling time, and noise in comparison with the RDAC as analyzed in chapter 3.2.5. Also, the CDAC can work as a S/H circuit and circuit components can be reduced. Furthermore, offset voltage of the amplifier is cancelled in a simple way by the CDAC. Therefore, using the CDAC instead of the RDAC is reasonable.

Figure 5.2 shows an example of interpolated signals and signal ranges from Figure 5.1. Assume that signal $V_{IN}$ is inputted to the amplifiers with positive / negative offset voltage, +/- $V_{OFF}$. After that, amplified input signals, $V_{oa}$ and $V_{ob}$ are applied to the interpolators. The interpolators have to output its signal in the proper range based on the voltage level of the input signal. In the pipeline stage, sub-ADC detects the voltage level of the input signal and

notifies to the interpolator. Then, the interpolator sets the interpolation ratio and the interpolated signal is outputted. The interpolated signal can be define as

$$V_{\text{ipa, b}} = \frac{m(V_{\text{IN}} + V_{\text{OFF}}) + n(V_{\text{IN}} - V_{\text{OFF}})}{m+n} = \frac{mV_{\text{oa}} + nV_{\text{ob}}}{m+n} \tag{5.1}$$

where $m$ and $n$ are interpolation ratio. $m$ and $n$ can be described as $2^p = m + n$, where $p$ indicates the resolution of the interpolation, such as 2 in Figure 5.2. $V_{\text{ipx}}$ means $V_{\text{ipa}}$ or $V_{\text{ipb}}$. For example, the input signal $V_x$ is located in the 2nd reference range within the whole $V_{\text{IN}}$ range as shown in Figure 5.2, interpolator 1 and 2 divide between $V_{\text{oa}}$ and $V_{\text{ob}}$ with a ratio of 3:1 and 1:1, respectively. In the conventional pipeline ADC, reference voltages are required to choose reference range. However, in the interpolated pipeline ADC, the reference range is chosen by interpolation; therefore, reference voltage is not necessary as shown in Figure 5.2. Following stages repeat the same operations using interpolated signals from the previous stages.

Figure 5.3 shows another example of the interpolation with gain degradation of the amplifier (similar explanation is described in chapter 2.5.2). In Figure 5.3, the gray colored lines are the original signals and the black colored lines are the gain degraded signals. Even though the gain is changed, the interpolation is completed without any error when two amplifiers' characteristics are matched. This characteristic makes it possible to use low-gain amplifier for the interpolated pipeline ADC with a high-resolution target specification.

The interpolation technique is used for a long time in the analog circuit design as introduced in chapter 2. However, the combination of the interpolation technique and the pipeline topology in [5.8] has not been introduced. The ADC in [5.7] has similar topology; however, the ADC's structure and the interpolation methods in [5.8] are different from [5.7].

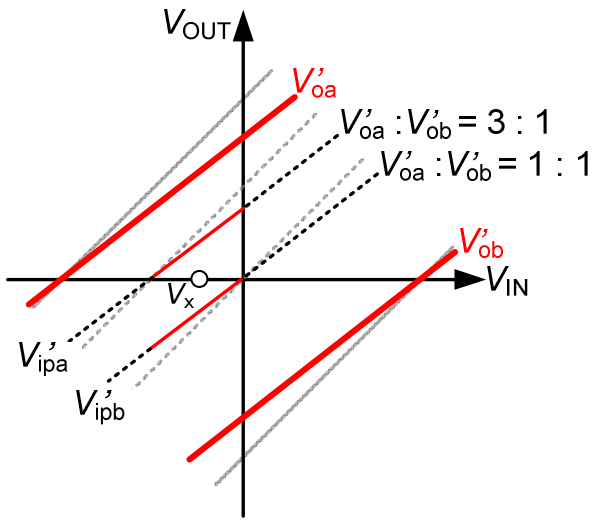


Figure 5.3 Interpolated signals with gain degradation.

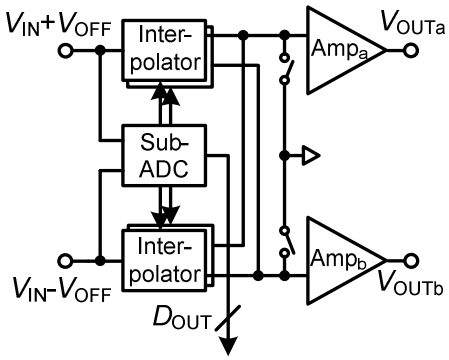


Figure 5.4 Pipeline stage structure.

Also, the analysis of the interpolation in [5.7] is not enough to design the ADC because those analysis mainly concern the offset of the amplifier (source signals of interpolation). Therefore, it is necessary to analyze the interpolated pipeline ADC topology for further design.

### 5.2.2 Interpolated Pipeline Stage

Figure 5.4 shows the structure of a pipeline stage in the interpolated pipeline ADC, which utilizes open-loop amplifiers. The pipeline stage consists of amplifiers, sub-ADC, and interpolators. As explained in Figure 5.1, two amplifiers and interpolators are incorporated for interpolation. Only single-ended nodes are described in Figure 5.4.

Since the interpolation technique does not require reference voltage, the sub-ADC cannot use the conventional comparison method which is comparing input with reference voltage. In [5.7], dual-residue amplifier outputs are connected to a resistor ladder, and comparator uses the divided voltages in the resistor ladder for its comparison. In contrast, the ADC in [5.8] utilize capacitor array for interpolation. Therefore, it is difficult to make such kind of reference voltages. A comparator with gate-weighted interpolation technique in the proposed subranging ADC in chapter 3 and 4 is incorporated in [5.8].

#### 5.2.2.1 CDAC in Interpolated Pipeline Stage

Figure 5.5 shows the structure of the CDAC, which is incorporated to the pipeline stage in [5.8]. The $C$ in Figure 5.5 means unit capacitance. A weight controlled topology is used to reduce the total capacitance. The total number of unit capacitors is $2^{N1st}$, where $N_{1st}$ means the resolution of the stage. For 3-bit interpolation, 8 unit capacitors are necessary in each CDAC. In Figure 5.5, the total capacitance in each CDAC has +/- 0.5 $C$ differences. This is due to the redundancy structure which is explained below. The switches connected to the unit capacitors are reference selection switches. The CDAC has two operation phases, sampling phase and interpolating phase. During the sampling phase, the output signal of the amplifier is charged into all of the unit capacitors. After that, during the interpolating phase, the

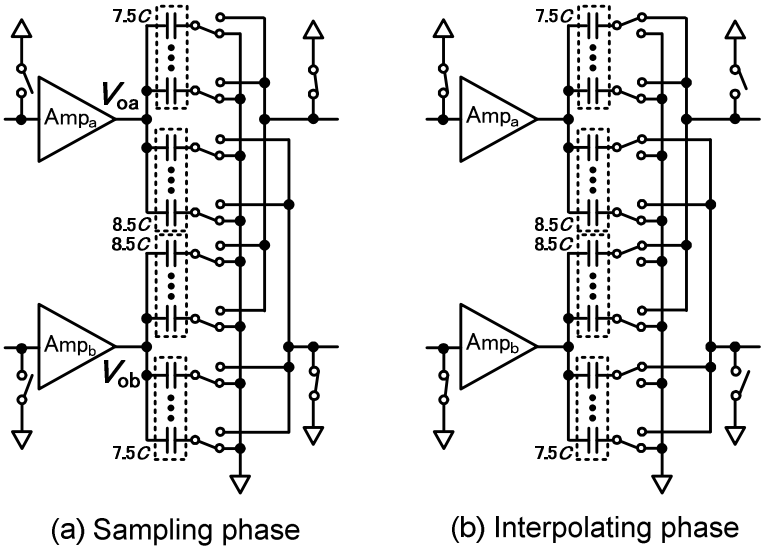


Figure 5.5 Structure and operation of CDAC.

CDAC generates interpolated signal. The interpolation ratio is controlled by the results of the sub-ADC in the stage. The output signal of the CDAC is represented in (5.1).

One of the characteristics of the CDAC is shifting the output voltage to the middle of the output signal swing range. This characteristic is shown in Figure 5.6. The shifted signals are much more linear due to the linearity characteristic of the amplifier is inversely proportional to the output swing range. Another characteristic of the CDAC in the interpolated pipeline topology is one LSB redundancy structure. In Figure 5.6, if there is an offset in the comparator, the CDAC's output signal goes out of its proper range. To solve this issue, one LSB redundancy structure is introduced to the CDAC.

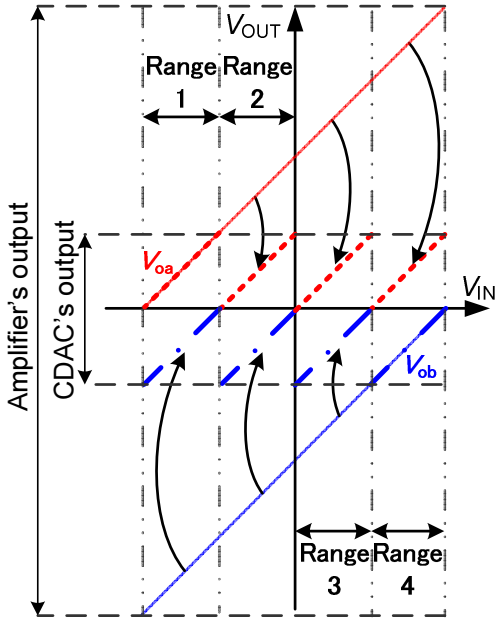


Figure 5.6 Voltage shift of CDAC.

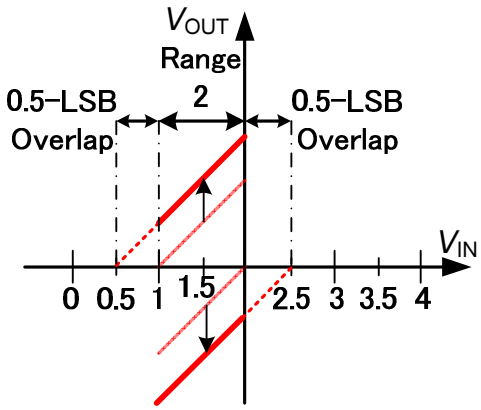


Figure 5.7 One bit redundancy of CDAC.

The offset voltage for redundancy is generated by additional weight control. To realize redundancy, each CDAC has a difference of 0.5 *C*. During the interpolating phase, these capacitance differences generate 0.5-LSB shift of the output signal. This operation can be expressed by (5.1) by adding an amount of 0.5-LSB voltage in the numerator. Figure 5.7 shows the operation of the redundancy structure using the signals in the range 2. The interpolated signals are shifted by (positive / negative) 0.5-LSB resolution of the stage. This relaxes the offset requirement for the comparator in the sub-ADC. To realize the redundancy, the number of capacitors for one extra bit is required. For example, the number of capacitors for a 3-bit CDAC is necessary to realize a 2-bit CDAC with 1-LSB redundancy.

### 5.2.3 Issues of Interpolated Pipeline ADC using Open-loop Amplifier

The proposed interpolated pipeline ADC utilizes the CDAC and low-gain open-loop amplifier for MDAC stage. Two amplifiers are utilized in the MDAC stage to realize the interpolation (structures of the amplifier and the MDAC stage are described in the following chapter in detail). This MDAC stage structure accompanies some issues which do not exist in the conventional pipeline ADC. In this sub-chapter, three major issues of the interpolated pipeline ADC design are examined, such as gain degradation of the CDAC, the amplifier's offset cancellation, and linearity degradation by the parasitic capacitance of the CDAC.

#### 5.2.3.1 Gain Degradation of CDAC

The gain degradation of the CDAC by the parasitic capacitance in chapter 3.2.2 is also occurred in the interpolated pipeline ADC because the ADC utilizes the open-loop amplifier topology. Figure 5.8 depicts this issue. During the interpolating (holding) phase, the CDAC is connected to the amplifier and the charges in the CDAC are distributed to the parasitic capacitor in the input of the amplifier. This charge distribution causes gain degradation of the CDAC. In the conventional pipeline ADC, this problem does not occur because the

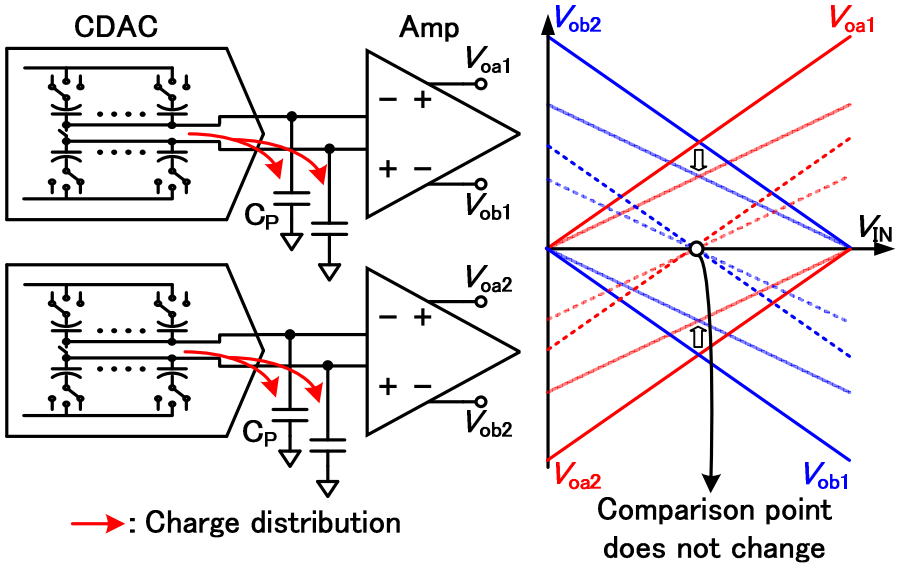


Figure 5.8 Gain degradation of CDAC.

amplifier utilizes the feedback loop. However, in the interpolated pipeline ADC, the amplifier utilizes open-loop topology; therefore, the output of the CDAC becomes the amplifier's input directly. Furthermore, the amplifier requires large amount of current for high-speed operation. It means the transistor's size becomes large and it worsens the issue by the increase of the parasitic capacitance. For example, the ADC in [5.8], the 1st MDAC stage's gain is reduced from 3-times to 2-times due to the CDACs gain degradation.

To be more exact, this gain degradation does not a problem in the interpolated pipeline topology. As explained in chapter 2.5.2, the comparison result does not changed even though the signal's gain is varied. However, reduced signal gain reduces the SNR and it might cause the ADC performance degradation.

#### 5.2.3.2 Amplifier's Offset Cancellation

The gain degradation issue in chapter 5.2.3.1 does not affect to the ADC's performance directly. However, if there is offset in the amplifier, the ADC's performance is degraded because the offset shifts the amplifier's output signal and it causes the change of comparison point. Figure 5.9 depicts this issue. In Figure 5.9, the translucent line is the signal with offset. As shown in Figure 5.9, the offset changes the comparison point and it causes a A/D conversion error.

Practically, offset surely appears in any component in the circuit, of course including amplifier. For the conventional pipeline ADC, offset of the amplifier does not a crucial because there is only one amplifier is utilized. However, the interpolated pipeline ADC utilizes two amplifiers for the interpolation; therefore, offset voltages in each amplifier have to be removed. Fortunately, the offset is cancelled smoothly by the CDAC during the ADC

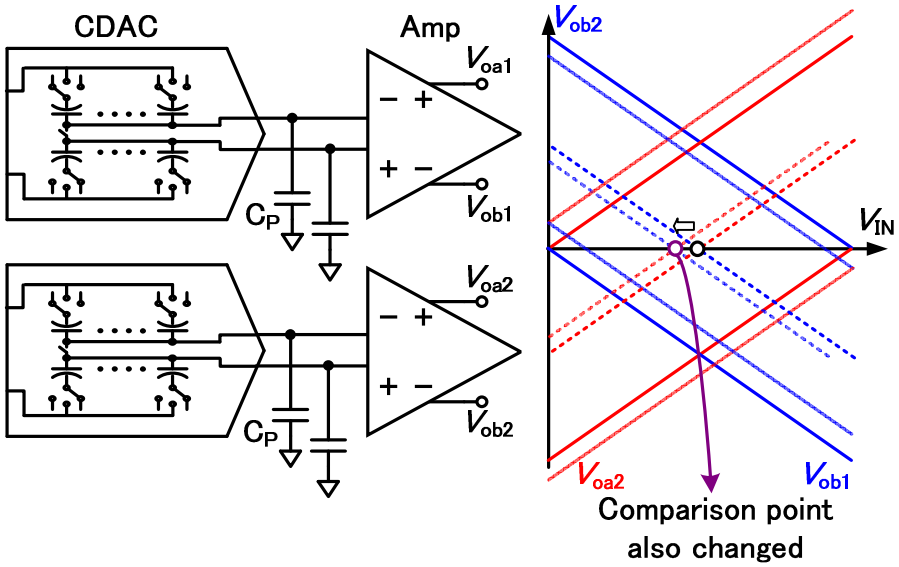


Figure 5.9 Effect of offset voltage in amplifier.

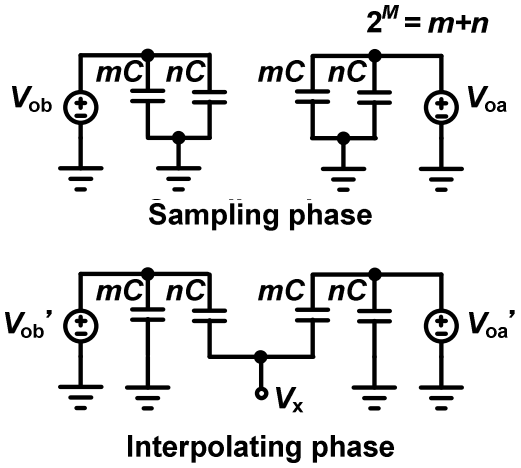


Figure 5.10 Offset cancelling procedure of interpolated pipeline ADC.

operation without additional timing budget and offset cancellation circuit.

Figure 5.10 shows the offset canceling procedure of the interpolated pipeline ADC. The amplifier's offset is cancelled through the sampling phase and the interpolating (holding) phase. In Figure 5.10, $m$ and $n$ mean weight of the capacitance in the CDAC which are determined by the sub-ADC's comparison results. The resolution of the CDAC, $M$ has a relationship with $m$ and $n$ as below,

$$2^M = m + n. \tag{5.2}$$

During sampling phase, the two amplifiers' output, $V_{oa}$ and $V_{ob}$ can be represented as,

$$V_{oa} = G_a\left(V_{in} - V_{ra} - V_{off\_a}\right) \tag{5.3}$$

$$V_{ob} = G_b\left(V_{in} - V_{rb} - V_{off\_b}\right) \tag{5.4}$$

where $G_a$, $G_a$ are gain of the amplifiers, $V_{in}$ is the ADC's input signal, $V_{ra}$, $V_{rb}$ are voltages for reference selection, and $V_{off\_a}$, $V_{off\_b}$ are offset voltages in the amplifiers. After that, during the interpolating phase, the amplifiers' output voltages become as below,

$$V'_{oa} = G_a\left(-V_{off\_a}\right) \tag{5.5}$$

$$V'_{ob} = G_b\left(-V_{off\_b}\right). \tag{5.6}$$

The CDAC's output voltage, $V_x$ is organized in (5.7),

$$V_x = -\left[\frac{m}{m+n}G_a\left(V_{in} - V_{ra}\right) + \frac{n}{m+n}G_b\left(V_{in} - V_{rb}\right)\right]. \tag{5.7}$$

As shown in (5.7), offset voltages of the amplifiers are disappeared in the CDAC's output. This offset canceling procedure is basically same as the output offset cancellation of the amplifier. The output offset canceling technique is only applicable to the low-gain open-loop amplifier topology which is exactly same as the amplifier in the interpolated pipeline ADC. Therefore, the amplifier's offset in the interpolated pipeline ADC is not a problem.

#### 5.2.3.3 CDAC's Linearity

As shown in Figure 5.5, the CDAC in the interpolated pipeline ADC consists of unit capacitors and switches. Since the CDAC has many unit cells (capacitors and switches), the circuit structure is very complicate. For example, the interpolated pipeline ADC in [5.8] utilizes 3 and 4-bit stage resolution. It means each signal passes through 16 unit capacitors and switches. Furthermore, the 1st stage CDAC has two parts in unit cell, sampling circuit and reference selection circuit. Therefore, careful layout is required to design the CDAC.

Figure 5.11 shows an example of the most likely to cause nonlinearity error in the CDAC. As shown in Figure 5.11, there is a parasitic capacitance ($C_P$) between two nodes of $SW_2$. Such kind of parasitic capacitor is caused by careless layout. In Figure 5.11, during the sampling phase, the amplifier's output is charged into the unit capacitor, $C$. At that time, even though there is a parasitic capacitance between two nodes of $SW_2$, it does not affect to the CDAC's operation. However, during interpolating phase and the $SW_2$ is turned off, $C_P$ transfers charge to the next stage which is not desired and it causes the CDAC's linearity error. Figure 5.12 shows a layout example of the CDAC and the cause of the parasitic capacitor. In left side of Figure 5.12, the metal-line for the next stage runs under the bottom

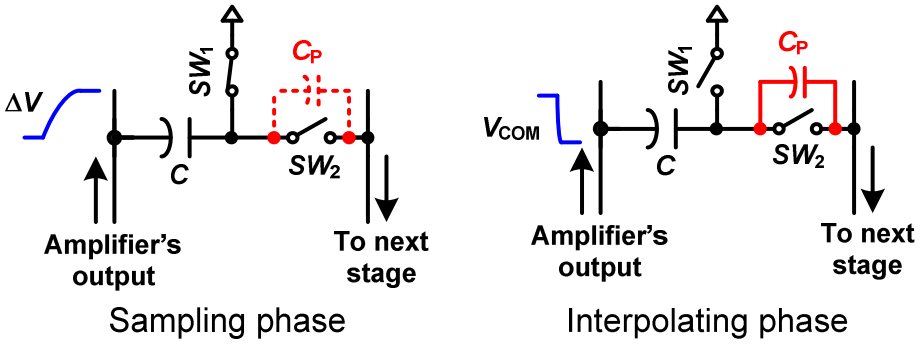


Figure 5.11 Charge leak through parasitic capacitance in CDAC.

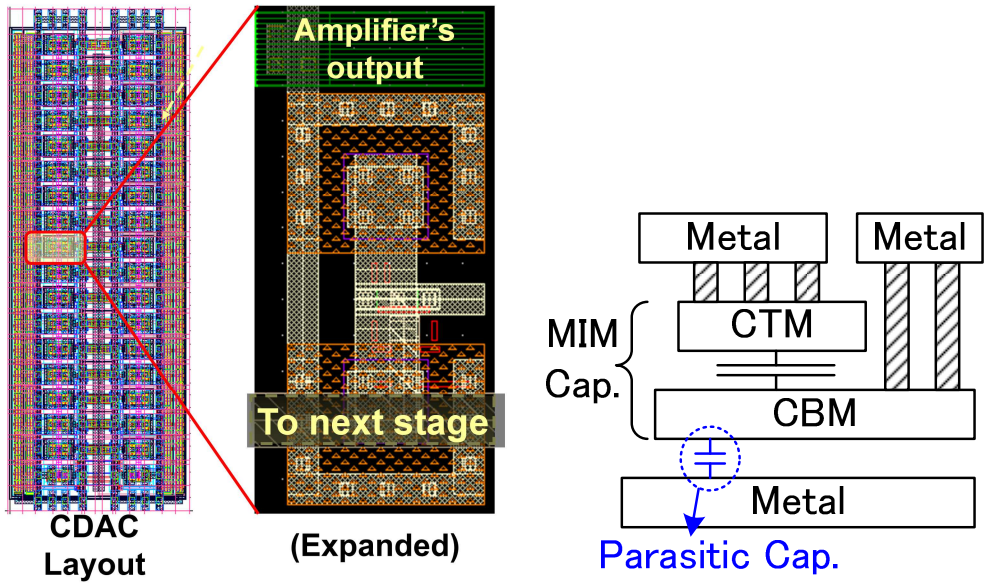


Figure 5.12 Layout example of CDAC's linearity issue.

metal-plate for MIM capacitor. If the metal-line and the bottom metal-plate are close, a parasitic capacitor becomes large enough to affect the CDAC's linearity as illustrated in right side of Figure 5.12.

Figure 5.13 and Figure 5.14 show the DC simulation results when the CDAC has the nonlinearity problem. A 10-bit interpolated pipeline ADC is utilized to the simulation. The simulation is performed by the transistor model and the parasitic capacitors are included in the CDAC in each stage of the ADC. The $C_P$ is assigned to 0.5 fF which is estimated by LPE simulation. In Figure 5.13, step-errors appear regularly over the whole ADC output codes. The reason of the step-error is clear that it is the added parasitic capacitor, especially the 1st stage CDAC. Figure 5.14 shows enlarged graph of the simulation result. By the Figure 5.14, it is recognized that smaller step-errors are exist between larger step-errors. These smaller step-errors are caused by 2nd stage CDAC's nonlinearity. There is no error that it is caused by the 3rd and 4th CDACs because the amplified signals cover the nonlinearity error of the

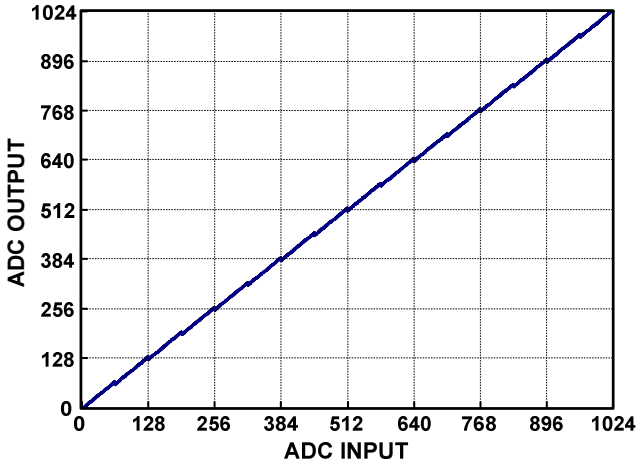


Figure 5.13 DC simulation result with charge leak.

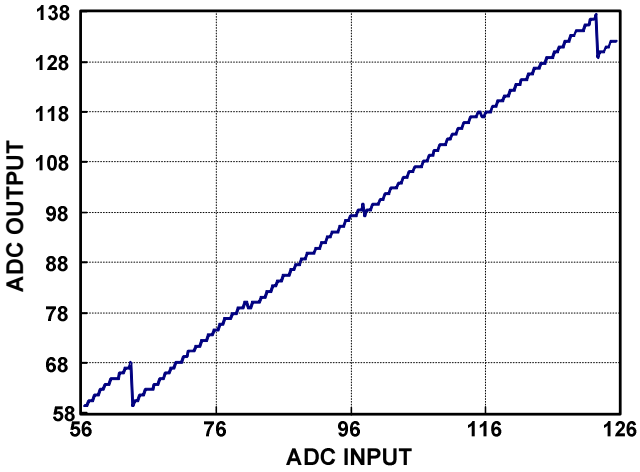


Figure 5.14 DC simulation result with charge leak (expanded).

CDAC.

To solve the charge leak issue (CDAC's nonlinearity), two solutions are applied to the CDAC. Figure 5.15 depicts those solutions. One effective solution is inserting additional switch ($SW_3$) to prevent charge leak as shown in Figure 5.15 (a). The $SW_3$ operates the

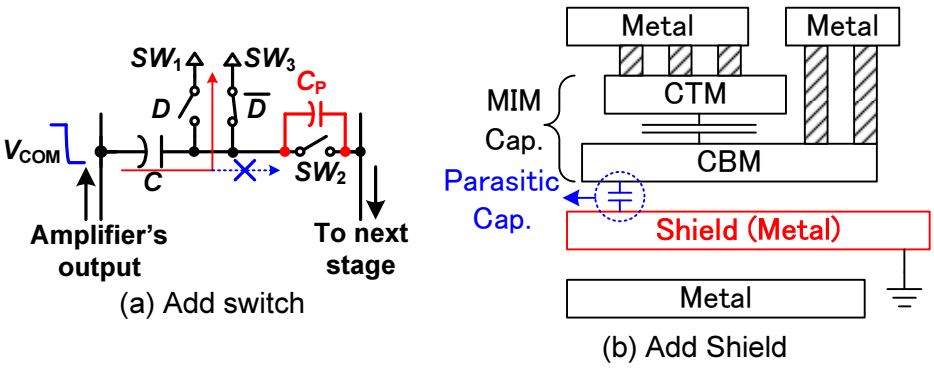


Figure 5.15 Solutions for charge leak issue.

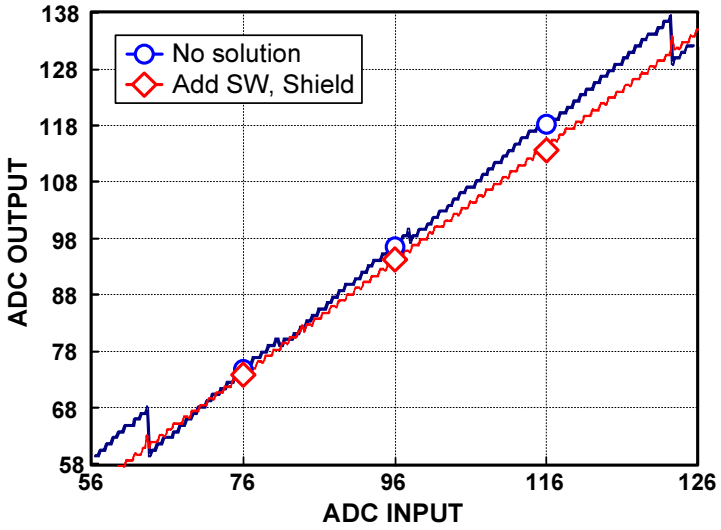


Figure 5.16 DC simulation results after applying solutions (expanded).

opposite control signal of $SW_1$. By the $SW_2$, charge from $C$ cannot pass through the $C_P$ because $SW_3$ holds the node to common-mode voltage. Also, a shield metal layer is added between MIM capacitor metal layer (CBM) and signal metal line (Figure 5.15 (b)). By the shield metal layer, the parasitic capacitor cannot couple with signal metal line directly. DC simulation is performed again after applying those solutions to the ADC. Figure 5.16 shows the effect of the solutions. As shown in Figure 5.16, the errors by the parasitic capacitor are removed successfully even though the parasitic capacitors still exist. The interpolated pipeline ADCs in this thesis incorporate these charge leak solutions for high-performance ADC realization.

### 5.2.4 ADC Performance

From chapter 5.2.1 to chapter 5.2.3, characteristics and advantages of the interpolated pipeline ADC are reviewed. Although A/D conversion in the pipeline stage is not affected by the gain of the amplifier, other characteristics of the amplifier are still crucial for the performance of the ADC, such as linearity and noise. In the following analysis, the effects of the amplifier's characteristics to the ADC's performance are examined.

Before starting the analysis, it is useful to define the general definition of the ADC performance. The total noise of the ADC including the quantization noise and the amplifier's error, $v_{n\_total}$ is

$$\boldsymbol{v}_{n\_total}^2 = \frac{\boldsymbol{v}_q^2}{12} + \boldsymbol{v}_{err}^2 \tag{5.8}$$

where $v_q$ is the LSB of the ADC and $v_{err}$ is the sum of the amplifier's errors, such as distortion and noise. In (5.8), by substituting $\alpha v_q$ for $v_{err}$, the formula can be expressed as a function of

$v_q$. α is a coefficient of the amplifier's error. By using the total noise power in (5.8) and power of sine wave, SNR definition of the ADC will be

$$\mathrm{SNR} = 10\log_{10}\left(\frac{2^{2N}}{\frac{2}{3}+8\alpha^2}\right) \tag{5.9}$$

where $N$ is the resolution of the ADC. Equation (5.9) indicates that SNR of the ADC degrades by increasing the amplifier's error. ENOB definition can be derived from (5.9) as below,

$$\mathrm{ENOB} = N - \frac{1}{2}\log_2\left(1+12\alpha^2\right). \tag{5.10}$$

More detailed effect of the amplifier's error will be analyzed in the following sub-chapters with circuit models and formulas. Some characteristics of the ADC are assumed as below for further analysis. In the pipeline stage, the following analysis uses the 1st stage, which is the most crucial in the ADC performance. Analysis is also applicable for the following stages because those stages also have the same structure. It is assumed that the CDAC has a reasonably small mismatch to achieve the target specification. This assumption is reasonable because the mismatch of the CDAC can be suppressed easily by proper components size as shown in chapter 3.3.1.1. And, the mismatch of the CDAC can be calibrated easily by digital circuit, unlike nonlinearity. Also, assume that the offset of the comparator is about 1.5 mV (σ) which is enough for a 10-bit resolution ADC. The offset of the amplifier is assumed to be cancelled by the offset cancelation technique in chapter 5.2.3.2. Simulations are performed using transistor model. However, for the ADC simulation in chapter 5.3.5 and chapter 5.4, only the 1st stage is the transistor model and other parts are ideal model to reduce the simulation time. This is reasonable because the 1st stage mainly determine the ADC's performance. The specific simulation conditions are described in each simulation results. The power consumption of the dynamic type comparator in chapter 5.5 is estimated in [5.8] at 320 MS/s operation frequency. Also, all parameters listed in the table 5.1 are estimated from the circuits in [5.8].

## 5.3 Amplifier

### 5.3.1 Topology

Even though the interpolation technique solves the gain issue, if the input signal of the interpolator (CDAC) includes distortion, the ADC performance degrades. There are several reasons to cause the distortion of the amplifier. In the interpolated pipeline ADC, the most

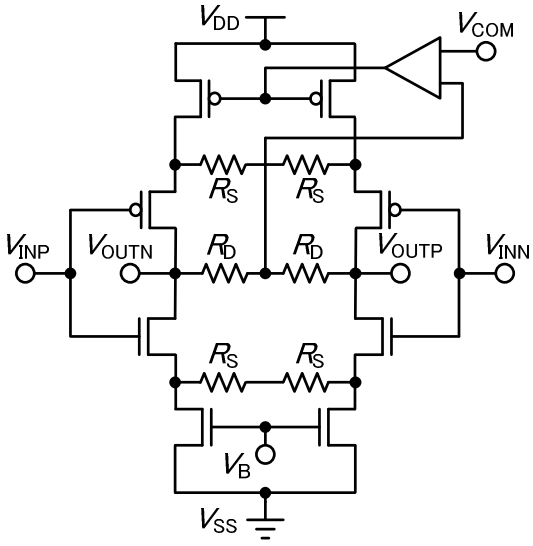


Figure 5.17 Schematic of amplifier for analysis.

severe characteristic is the linearity because low-gain open-loop amplifiers are used.

Several works have been published for the linearity improvement of the amplifier. The MIFG transistors [5.21] are used for a large input swing range; however, this technique requires additional process. A double pseudo differential pair CMOS OTA is also introduced in [5.22]. The pseudo differential pair OTA realizes good linearity using simple structure. However, the balance of the differential pair can collapse easily due to the mismatch of the transistors. Considering the use of the standard CMOS technology and robustness, one good choice is source degeneration technique. In this chapter, an amplifier with source degeneration is analyzed with interpolated pipeline scheme.

Figure 5.17 shows the schematic of the amplifier, which is used in [5.8]. The amplifier incorporates single-stage differential structure without feedback loop. Since it uses single-stage topology, it is unnecessary to care about phase margin. The gain of the amplifier is only 9.5-dB. The simple structure of the amplifier in Figure 5.17 represents one of the advantages of the interpolated pipeline ADC.

In Figure 5.17, $V_B$ is the bias voltage for the current source, $R_S$ is the source degeneration resistance, and $R_D$ is the output resistance. The amplifier has CMOS input to increase $g_m$. The effective $g_m$ ($g_{m\_eff}$), DC-gain ($G_0$), and 3-dB bandwidth ($\omega_{p1}$) are given by

$$g_{m\_eff} = \frac{1}{R_S}\frac{1}{1+\frac{1}{g_m R_S}} \tag{5.11}$$

$$G_0 = \frac{R_D}{R_S}\frac{1}{1+\frac{1}{g_m R_S}} \tag{5.12}$$

$$\omega_{p1} = \frac{1}{R_D C_L} \tag{5.13}$$

where $C_L$ is the load capacitance of the amplifier. It is well known that for the source degeneration amplifier, if the $g_m R_S$ is large enough, the $g_{m\_eff}$ is determined by $R_S$. Also, the gain is determined by the ratio of $R_S$ and $R_D$. The 3-dB bandwidth is determined by $R_D$ and $C_L$.

In the following analysis, the amplifier's gain is set to 3-times which is the same value as [5.8]. In [5.8], the 3-times gain is enough to achieve less than 1/4 LSB input referred comparator's offset, even though the signal degradation by the input parasitic capacitance of the amplifier is considered. The offset voltage of the comparator is caused by the comparator's mismatch and the calibration circuit. If the offset is varied, the gain of the amplifier should be reconsidered. At that time, the values of $R_S$ and $R_D$ have to be assigned by proper calculation. The effect of $R_D$ will be discussed in detail in chapter 5.4.2.

### 5.3.2 Linearity

Before starting the amplifier's linearity analysis, brief explanation of the amplifier's linearity is useful to understand further analysis. Figure 5.18 depicts why the amplifier's linearity is important. If there is no linearity error in the amplifier, the amplifier's output signal changes straightly for all output range, as the blue colored line in Figure 5.18. However, in the real circuit, the amplifier has linearity characteristic and the output signal is distorted as the red colored lined in Figure 5.18. This kind of distortion also affects to the interpolation and it causes an error. The amplifier's linearity also related with the stage's resolution (signal range). It is depicted in Figure 5.19. If the stage's resolution is low, the amplifier's output swing range becomes wide. Usually, the amplifier's distortion is increased with the output signal range as shown in Figure 5.18; therefore, increasing the stage's resolution is effective

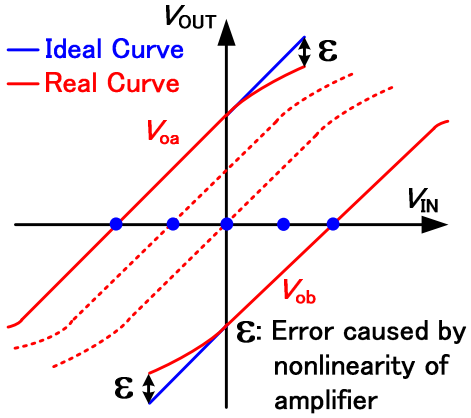


Figure 5.18 Ideal and real output curve of amplifier.

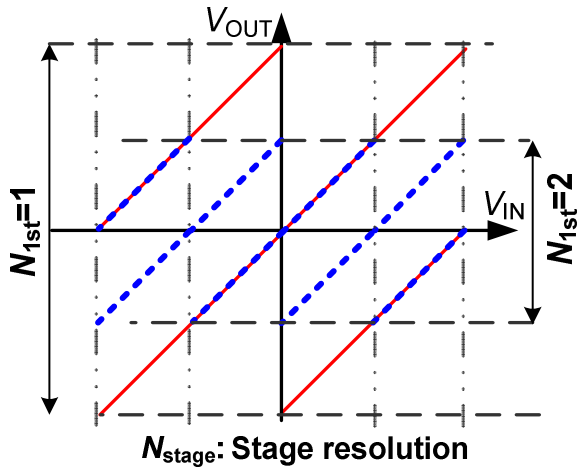


Figure 5.19 Relation of stage's resolution and amplifier's output swing range.

to improve the amplifier's linearity characteristic. This relationship is also represented in (5.28).

To examine the linearity of the amplifier, it is necessary to define the distortion of the amplifier first. The output voltage of the amplifier including nonlinearity can be defined as below,

$$V_{out} = a_1 V_{in} - a_3 V_{in}^3. \tag{5.14}$$

In (5.14), the 1st order and the 3rd order terms are considered because they are dominant. The 2nd order term is omitted by the differential structure of the amplifier. The amount of the distortion caused by the amplifier's 3rd harmonic can be represented by $a_3/a_1$. $a_3/a_1$ can be calculated using the current formula of the MOS transistor. The current in the differential amplifier without source degeneration, $\Delta I_{out}$ is

$$\Delta I_{out} = \frac{K}{2}\Delta V_{in}\sqrt{\frac{4I_s}{K} - \Delta V_{in}^2} \tag{5.15}$$

where

$$K = \mu C_{ox}\frac{W}{L}. \tag{5.16}$$

In (5.15), $I_s$ is the sink current. The output voltage of the amplifier, $\Delta V_{out}$ using Taylor series until 3rd order, can be written as

$$\Delta V_{out} = R_D \Delta I_{out} \approx \sqrt{KI_s}R_D\Delta V_{in} - \frac{1}{8}\sqrt{\frac{K^3}{I_s}}R_D\Delta V_{in}^3. \tag{5.17}$$

In (5.17), $a_1$ and $a_3$ are written as below.

$$a_1 = \sqrt{KI_s}R_D. \tag{5.18}$$

$$a_3 = \frac{1}{8}\sqrt{\frac{K^3}{I_s}}R_D. \tag{5.19}$$

Based on (5.18) and (5.19), $a_3/a_1$ can be represented as

$$\frac{a_3}{a_1} = \frac{1}{8(V_{gs} - V_{th})^2}. \tag{5.20}$$

Equation (5.20) represents the $a_3/a_1$ without the source degeneration resistance. By introducing the source degeneration resistor, a negative feedback path is formed between the gate and the source node in the input MOS transistor. Therefore, the amount of distortion is reduced by the feedback loop gain; it means $a_3/a_1$ is reduced by $(1+g_mR_S)$. $a_3/a_1$ for the source degeneration amplifier can be rewritten as

$$\frac{a_3}{a_1} = \left(\frac{1}{1+g_mR_s}\right)\frac{1}{8(V_{gs} - V_{th})^2}. \tag{5.21}$$

If the amplifier does not incorporates source degeneration resistor, $R_S$ in (5.21) becomes 0, then (5.21) becomes equal to (5.20). At that time, the $a_3/a_1$ is determined by $V_{gs}$ and $V_{th}$. This means the distortion varies with input signal level, and it degrades the linearity characteristic of the amplifier. However, by introducing the source degeneration resistor, the distortion is suppressed by $(1+g_mR_S)$. Therefore, the source degeneration amplifier can achieve better linearity characteristic.

The calculation and the simulation results of (5.21) are shown in Figure 5.20. The simulation is performed in two input signal range conditions, +/- 75 mV and +/- 100 mV. In the simulation, $R_D$ is assigned 400 Ω which is the same value as [5.8]. As analyzed in (5.20) - (5.21), the linearity characteristic becomes better with increasing $R_S$. However, wide signal

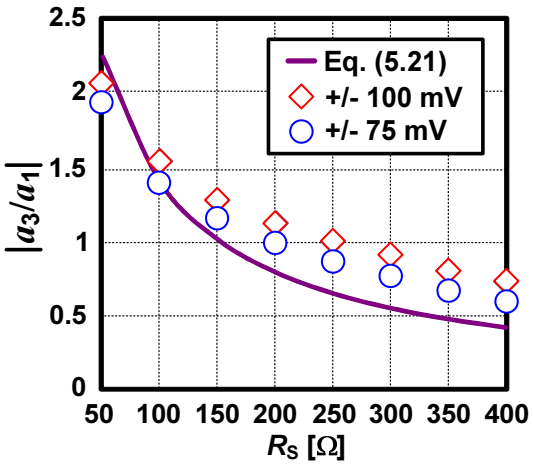


Figure 5.20 $R_S$ vs. linearity of amplifier.

swing range degrades linearity characteristic. Therefore, large $R_S$ and small signal range is preferred for better linearity characteristic. There is a small difference between the calculation and the simulation. The difference is caused by $g_m$, which is fixed in the calculation, but it varies in the simulation. The largest difference is 0.2 in +/- 75 mV input signal range which is the same condition in [5.8]. This means the analysis is usable.

Equation (5.21) can be rewritten in (5.22) using the relation of ($V_{gs}$- $V_{th}$) and current,

$$\frac{\alpha_3}{\alpha_1} = \left(\frac{1}{1+\beta_m R_s}\right)\left(\frac{\beta_m^2}{32 I_D^2}\right). \tag{5.22}$$

Equation (5.22) shows that it is difficult to achieve good linearity characteristic with small current. Therefore, large power consumption is essential for good linearity.

Next, the relationship between the amplifier's linearity and the ADC's performance is analyzed. To investigate the effect of the amplifier's linearity to the performance of the interpolated pipeline ADC, the characteristic of the interpolation has to be considered. Unlike the conventional pipeline ADC, the interpolated pipeline ADC uses two sets of differential signal. The input referred distortion of the amplifier; $\Delta V_{IN}$ can be written with considering 3rd order distortion as shown in (5.14),

$$\Delta V_{IN} = \frac{m}{m+n}\frac{\alpha_3}{\alpha_1}\left(V_{IN}-V_{OFF}\right)^3 + \frac{n}{m+n}\frac{\alpha_3}{\alpha_1}\left(V_{IN}+V_{OFF}\right)^3. \tag{5.23}$$

In (5.23), $m$ and $n$ are the ratio of the interpolation and $V_{OFF}$ is the offset voltage for the interpolation. The $V_{OFF}$ is used as the same concept in Figure 5.1. Equation (5.23) can be rearranged to the following,

$$\Delta V_{IN} = 8m(M-m)(2m-M)\frac{\alpha_3}{\alpha_1}\left(\frac{V_{OFF}}{M}\right)^3 \tag{5.24}$$

where

$$M = m+n,\ V_{IN} \approx \frac{2m-M}{M}V_{OFF},\ V_{OFF} = \frac{V_{FS}}{2^{N_{1st}}}. \tag{5.25}$$

In (5.25), $V_{FS}$ is the full-scale reference range and $N_{1st}$ is the resolution of the 1st stage. The input referred distortion of the amplifier is proportional to the amplifier's linearity coefficient, $a_3/a_1$. Furthermore, the terms of signal swing range, $V_{OFF}$ and $M$ are more crucial, since they are cubed. Therefore, to achieve better linearity characteristic, small $a_3/a_1$ of the amplifier and increasing the resolution of the stage are effective.

The averaged input referred distortion by using (5.24) is equal to

$$\overline{\Delta V_{IN}} = \frac{2}{M}\int_{M/4}^{3M/4} \Delta V_{IN}\, dm = 0. \tag{5.26}$$

In (5.26), the integration range, $M/4$ to $3M/4$ is determined by the result of considering a 1-LSB redundancy. The averaged noise power is

$$\overline{v_n^{\,2}} = \frac{2}{M}\int_{M/4}^{3M/4} \left(\Delta V_{IN} - \overline{\Delta V_{IN}}\right)^2 dm = \frac{407}{1680}\left(\frac{a_3}{a_1}V_{OFF}^3\right)^2. \tag{5.27}$$

To calculate the effect of the noise power from the amplifier's distortion on the ADC's performance, the formula of the ENOB in (5.10) can be used. Before using (5.10), the averaged noise power is necessary to be normalized to $v_q$. After that, the normalized averaged noise power is substitute for α in (5.10). Then, (5.10) can be rearranged as

$$\text{ENOB} \approx N - \frac{1}{2}\log_2\left\{1 + 2.9\left(\frac{a_3}{a_1}V_{FS}^2\, 2^{N-3N_{1st}}\right)^2\right\}. \tag{5.28}$$

The calculation and the simulation results of the ENOB vs. the linearity of the amplifier are shown in Figure 5.21 and Figure 5.22. The calculation and the simulation are performed in two ADC resolutions, 10-bit and 12-bit. Both of graphs in Figure 5.21 and Figure 5.22 draw similar shape, however, the linearity requirement are quite different. In Figure 5.21, about 2.5 of $a_3/a_1$ is enough to achieve 0.2-bit ENOB degradation when $V_{FS}$=0.8 V. The requirement of $a_3/a_1$ becomes more relaxed to 4 when $V_{FS}$ becomes 0.6 V. On the other hand, the requirement of $a_3/a_1$ is 0.5 when the resolution of the ADC is increased to 12-bit. Even though the $V_{FS}$ is reduced to 0.6 V, the $a_3/a_1$ requirement is not relaxed larger than 1.

By (5.28), Figure 5.21 and Figure 5.22, the relationship of amplifier's linearity, reference range, and resolution of the stage is analyzed. To achieve better ENOB, reducing $a_3/a_1$ and reference range are effective, because the bad 3rd harmonic and the wide reference range degrade the amplifier's linearity characteristic. The high-resolution of stage is also effective for better performance. This is because the output signal swing range of the CDAC is reduced by $2^{NIst}$ as shown in Figure 5.6. However, the reference range is usually determined by system specification and increasing stage resolution affects other parameters, such as smaller offset requirement for the comparators and complexity.

As explained above, the resolution of the 1st stage affects a lot to the ADC's performance. Therefore, it is useful to examine the effect of the resolution of the 1st stage. Figure 5.23 shows the calculation of the ENOB vs. $a_3/a_1$ with variation of $N_{1st}$ for the 12-bit resolution interpolated pipeline ADC. The calculation of 10-bit resolution is omitted since it

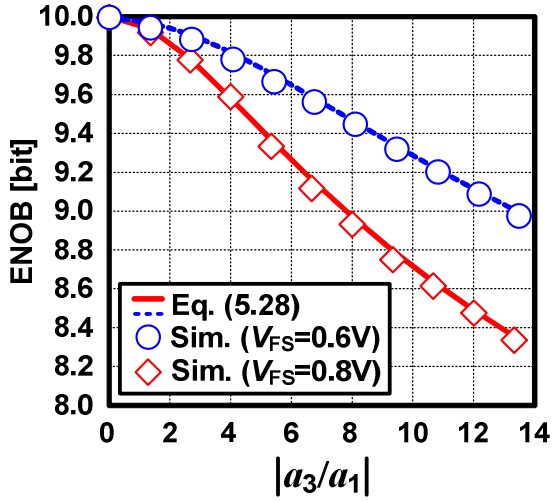


Figure 5.21 ENOB vs. linearity of amplifier (10-bit).

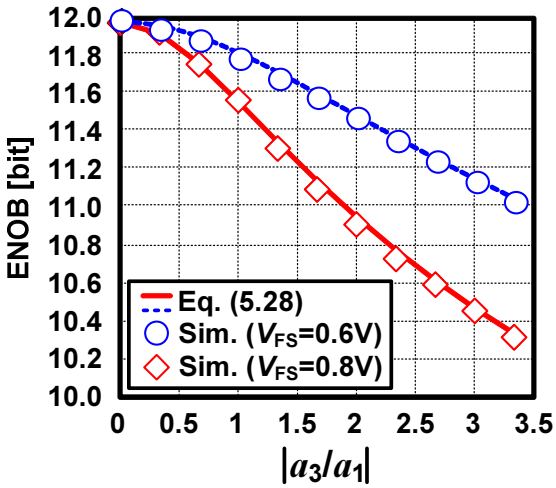


Figure 5.22 ENOB vs. linearity of amplifier (12-bit).

has almost same shape of 12-bit results like Figure 5.21 and Figure 5.22. The 10-bit calculation results can be examined by using (5.28). The $V_{FS}$ is assigned as 0.6 V. Figure 5.23 shows that 4-bit 1st stage is balanced for the ADC design. When 1st stage is 3-bit, the structure of the stage becomes simple; however, the linearity requirement of the amplifier becomes very severe and the ADC's performance is degraded drastically. On the other hand, 5-bit 1st stage relaxes a lot of $a_3/a_1$ requirement; however, the circuit complexity is increased. For Figure 5.23, the simulation results are omitted due to the long simulation time. However, the calculation results in Figure 5.23 are reliable because the calculation and the simulation are well matched in the previous simulation and calculation in Figure 5.21 and Figure 5.22.

### 5.3.3 Noise

The noise of the amplifier is another important characteristic to achieve high ENOB of the

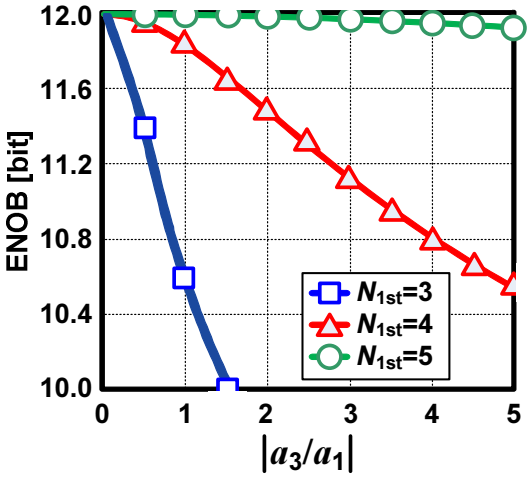


Figure 5.23 ENOB vs. linearity of amplifier with 1st stage resolution variation.

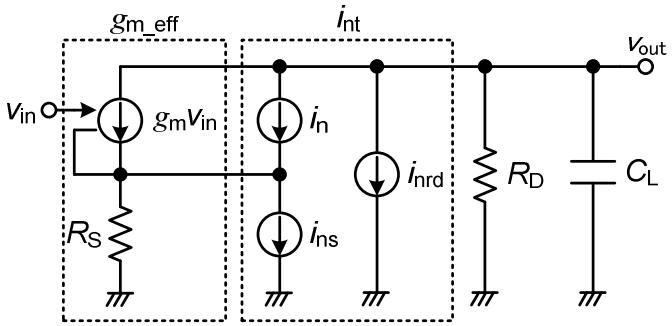


Figure 5.24 Noise analysis model for source-degeneration amplifier.

ADC. Especially, since the amplifier topology in the interpolated pipeline ADC is different to the conventional pipeline ADC, the noise characteristic has to be calculated by the structure used in the ADC, as shown in Figure 5.17.

To analyze the noise characteristic of the amplifier, a noise model is necessary. Figure 5.24 shows the noise analysis model of the amplifier which is introduced in Figure 5.17. In Figure 5.24, $g_m$ is the transconductance of the input MOS transistor, $i_n$ is the noise current in the input MOS transistor, $i_{ns}$ is the noise current of the current source and $R_S$, and $i_{nrd}$ is the noise current of $R_D$. The input referred noise spectrum density with regard to $i_n$, $i_{ns}$, and $i_{nrd}$ are expressed as below.

$$\overline{v_{ni}^2} = \left( \frac{\overline{i_n}}{g_m} \right)^2 . \tag{5.29}$$

$$\overline{v_{nsi}^2} = \left( \frac{v_{nso}}{G_0} \right)^2 = R_S^2 \overline{i_{ns}^2} . \tag{5.30}$$

$$\overline{v_{\text{nrdi}}^{\,2}} = \overline{i_{\text{nrd}}^{\,2}}\left(R_{\text{s}} + \frac{1}{g_{\text{m}}}\right)^2. \tag{5.31}$$

The total input referred noise power with consideration of the bandwidth will become

$$v_{\text{nit}}^{\,2} = \left(\overline{v_{\text{ni}}^{\,2}} + \overline{v_{\text{nsi}}^{\,2}} + \overline{v_{\text{nrdi}}^{\,2}}\right)\Delta f \tag{5.32}$$

where

$$\Delta f = \frac{1}{4R_{\text{D}}C_{\text{L}}}. \tag{5.33}$$

Through (5.29) to (5.31), it is recognized that each noise spectrum density is affected by $g_{\text{m}}$ and $R_{\text{S}}$. Detailed discussion to determine $g_{\text{m}}$ and $R_{\text{S}}$ is described in chapter 5.4.1.

### 5.3.4 Input Parasitic Capacitance

The linearity improvement by the source degeneration is explained in chapter 5.3.2. It also reduces the input parasitic capacitance of the amplifier. A small signal model of the amplifier in Figure 5.17 with consideration of the parasitic capacitance is presented in Figure 5.25.

By adding the source degeneration resistor, the Miller effect occurs to both gate-drain capacitance and gate-source capacitance. For accurate analysis, drain resistance of the MOS transistor is also considered. The gains of gate-drain ($G_{\text{d}}$) and gate-source ($G_{\text{s}}$) can be represented in (5.34) and (5.35), respectively.

$$G_{\text{d}} = -\frac{g_{\text{m}}R_{\text{D}}}{1 + (g_{\text{m}} + g_{\text{ds}})R_{\text{S}} + g_{\text{ds}}R_{\text{D}}}. \tag{5.34}$$

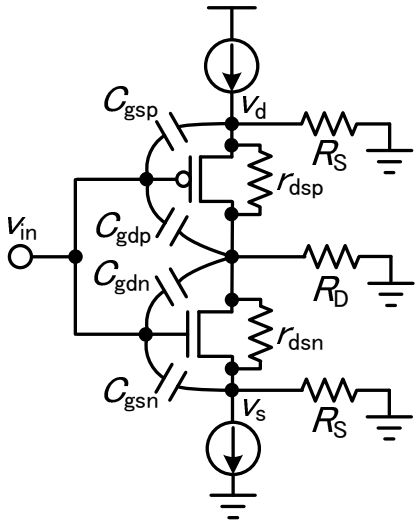


Figure 5.25 Small signal model for input parasitic capacitance analysis.

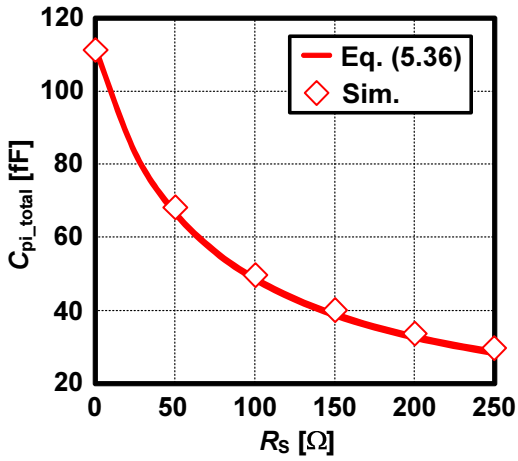


Figure 5.26 $C_{pi\_total}$ vs. $R_S$ of source degeneration amplifier.

$$G_s = \frac{g_m R_S}{1+(g_m+g_{ds})R_S}\left(1+\frac{g_{ds}}{g_m}G_d\right). \tag{5.35}$$

$$C_{pi\_total} = (1-G_d)C_{gd} + (1-G_s)C_{gs}. \tag{5.36}$$

Through (5.34) and (5.35), $1/r_{dsp}$ and $1/r_{dsn}$ are assumed the same value, and it is represented as $g_{ds}$. In (5.36), $C_{pi\_total}$ means the total input parasitic capacitance. $C_{pi\_total}$ can be calculated by adding up $C_{gs}$ and $C_{gd}$ with consideration of the Miller effect. The calculation and the simulation results are shown in Figure 5.26. In Figure 5.26, the total input parasitic capacitance is reduced with increasing $R_S$. For example, when $R_S$ varies from 0 to 200 Ω, the total input capacitance is reduced from 113 fF to 36 fF.

The input parasitic capacitance reduces the gain of the CDAC and the SNR. When the amplifier utilizes source degeneration of 200 Ω, the ENOB is improved by 0.25-bit using the SNR calculation. The actual improvement considering other parameters in the MDAC is 0.15-bit, which is analyzed in the following chapter. If the amplifier does not use the source degeneration, the input signal swing range is reduced and it might become a problem due to the mismatch voltage of the comparator. To compensate reduced signal swing range, the amplifier's gain has to be increased. However, increasing gain degrades the settling characteristic of the amplifier. Therefore, the effort on reducing the input parasitic capacitance is important.

### 5.3.5 Matching Between Two Amplifiers

As shown in Figure 5.1, Figure 5.4, and Figure 5.5, the interpolated pipeline ADC utilizes two amplifiers in MDAC stage to realize interpolation. Therefore, the matching of the amplifier's characteristic is another issue for the ADC design. In this chapter, the effect of the mismatch

between two amplifiers is examined in gain and bandwidth (Linearity characteristic is already examined by chapter 5.3.2). By the proposed formulas, calculation and simulation results, the designers can figure out the required mismatch for the target specification.

### 5.3.5.1 Gain Mismatch

If there is a gain mismatch between two amplifiers, each amplifier's output range becomes different, in which causes the comparison error in sub-ADC. To help the understanding the effect of the gain mismatch, the interpolated signals without and with gain error are shown

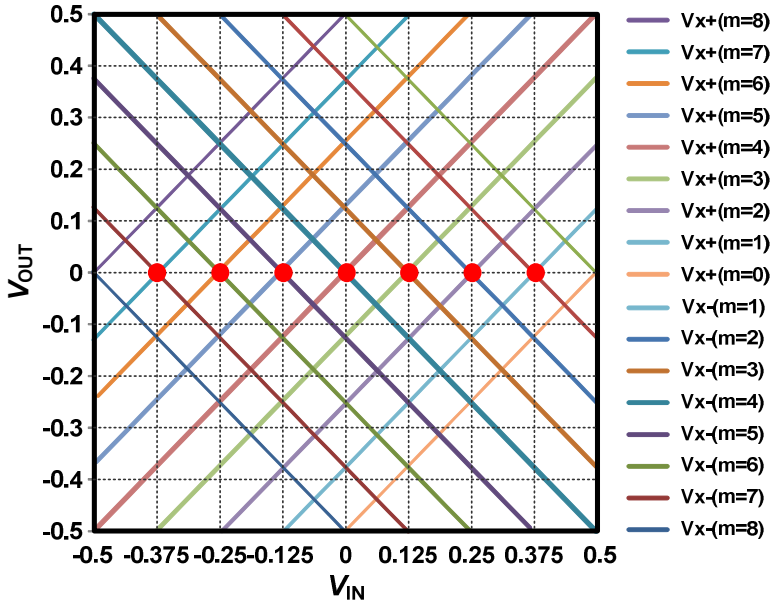


Figure 5.27 Interpolated signals without gain mismatch (ΔG/G = 0).

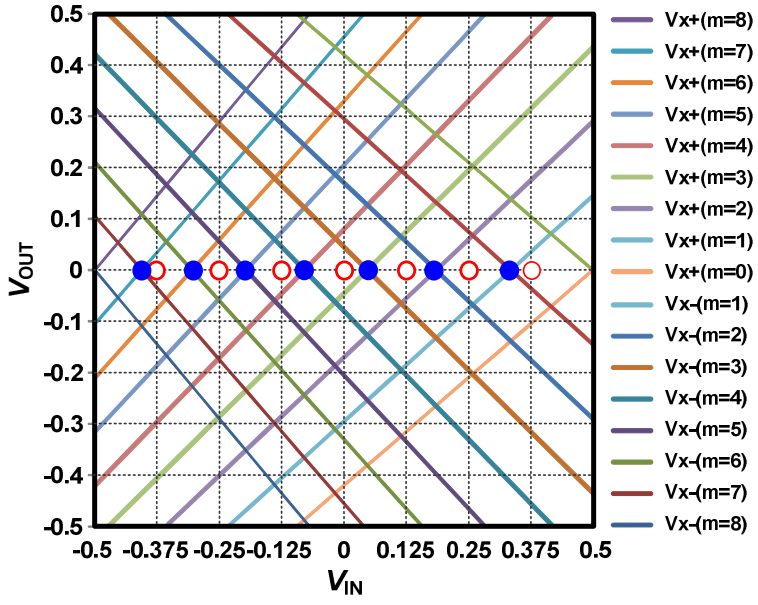


Figure 5.28 Interpolated signals with gain mismatch (ΔG/G = 0.16).

in Figure 5.27 and Figure 5.28, respectively. In Figure 5.27, x-axis means amplifier's input and y-axis means amplifier's output. Figure 5.27 shows 3-bit interpolation and the gain of the amplifier is 1. The $V_x$ means original input signal and $m$ means the weight for the interpolation, such as in (5.1). If there is no gain error ($\Delta G/G = 0$), the interpolated signals are generated with equal offset. This means the A/D conversion in the sub-ADC is performed without error. However, if there is gain mismatch between two amplifiers, the offset between interpolated signals are different and error occurs in A/D conversion in the sub-ADC. In Figure 5.28, it is assumed that there is 0.16 of the gain mismatch between two amplifiers ($\Delta G/G$ = 0.16). The comparison points in Figure 5.28 (the point when two opposite slope signals are crossed on the 0 x-axis) move from the original points in Figure 5.27. This error causes the DNL and the SNR degradation of the ADC.

The amplifier's output signal with considering of gain mismatch can be written as (5.37),

$$V_{OUT} = \frac{m}{m+n}(G+\Delta G)(V_{IN}-V_{OFF}) + \frac{n}{m+n}(G-\Delta G)(V_{IN}+V_{OFF}). \tag{5.37}$$

In (5.37), the parameters are the same as the definition of chapter 5.3.2. $G$ means the gain of the amplifier and $\Delta G$ means amount of the gain mismatch of the amplifier. Equation (5.37) can be arranged to the following,

$$V_{OUT} = GV_{IN} - \frac{m-n}{m+n}V_{OFF} + \left(\frac{m-n}{m+n}\Delta GV_{IN} - \Delta GV_{OFF}\right). \tag{5.38}$$

In (5.38), the left part represents the amplifier's output signal and the right part represents the error amount caused by the amplifier's mismatch. The input referred error by the amplifier's gain mismatch can be calculated using the error amount in (5.38).

$$\Delta V_{IN} = \frac{\Delta V_{out}}{G} = \frac{\Delta G}{G}\left(\left(\frac{m-n}{m+n}\right)^2 + 1\right)V_{OFF} = \frac{\Delta G}{G}\left(\left(\frac{2m-M}{M}\right)^2 + 1\right)V_{OFF}. \tag{5.39}$$

In (5.39), $M$ is the same definition as (5.25). The averaged input referred error by the amplifier's gain mismatch is equal to

$$\overline{\Delta V_{IN}} = \frac{2}{M}\int_{M/4}^{3M/4}\Delta V_{IN}\,dm = \frac{13}{12}\frac{\Delta G}{G}V_{OFF}. \tag{5.40}$$

As explained in chapter 5.3.2, the integration range is from $M/4$ to $3M/4$ by the result of considering a 1-LSB redundancy structure. The averaged noise power by the amplifier's gain mismatch is

$$\overline{v_{n\_g}^{\,2}} = \frac{2}{M}\int_{M/4}^{3M/4}\left(\Delta V_{IN} - \overline{\Delta V_{IN}}\right)^2 dm = \frac{1}{180}\left(\frac{\Delta G}{G}V_{OFF}\right)^2. \tag{5.41}$$

The amount of the ENOB degradation which is caused by the averaged noise power in (5.41) can be defined as the same way in (5.28). The ΔENOB can be derived from (5.10) as below,

$$\Delta ENOB = \frac{1}{2}\log_2\left(1+12\left(\frac{\overline{v_{n\_q}^2}}{V_q^2}\right)\right) \tag{5.42}$$

The α in (5.10) is substitute to averaged noise power ($v_{n\_q}$) and 1-LSB voltage ($V_q$). Finally, the ENOB is represented to

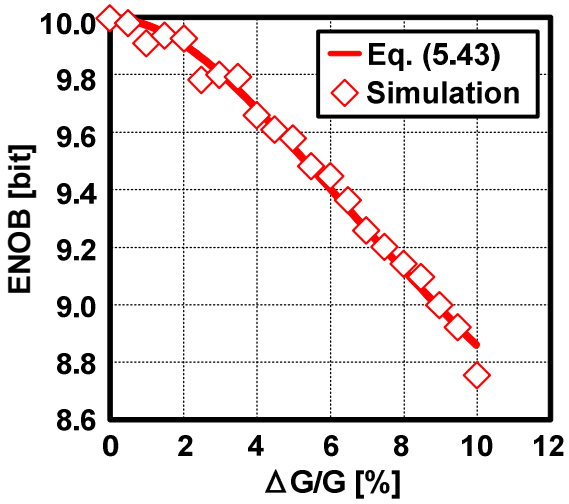


Figure 5.29 ENOB vs. amplifier's gain mismatch for 10-bit.

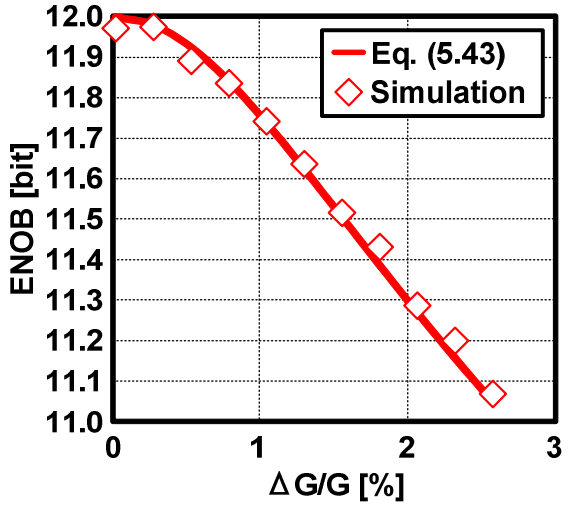


Figure 5.30 ENOB vs. amplifier's gain mismatch for 12-bit.

$$\mathrm{ENOB} = N - \frac{1}{2}\log_2\left(1+\frac{1}{15}\left(\frac{\Delta G}{G}2^{N-N_{1st}}\right)^2\right) \tag{5.43}$$

where $N$ and $N_{1st}$ are the same definition in chapter 5.3.2. The calculation and the simulation results of ENOB vs. the amplifier's gain mismatch ($\Delta G/G$) are shown in Figure 5.29 and Figure 5.30. The calculation and the simulation are performed in 10- and 12-bit resolution. The ENOB degrades with increase of the amplifier's gain mismatch. For example, to suppress the ENOB degradation less than 0.2-bit, the gain mismatch has to be smaller than 3 % in 10-bit resolution ADC. The requirement becomes more severe when the resolution of the ADC is increased, for example, lower than 0.8 % gain mismatch to achieve 0.2-bit ENOB degradation.

By (5.43), Figure 5.29 and 5.30, it is recognized that the ENOB of the ADC is affected by the amplifier's gain mismatch, the 1st stage's resolution, and the ADC's resolution. The effect of the amplifier's gain mismatch and the ADC's resolution is understandable intuitionally. The reason of the effect of the 1st stage's resolution is the high resolution of the stage reduces the amplifier's output swing range and the amount of the error by the amplifier's gain mismatch is getting larger with increase of the signal swing range. However, increasing stage resolution causes the requirement of the smaller offset for comparator, increase of power consumption and the complexity.

Figure 5.29 and Figure 5.30 is performed with 4-bit 1st stage resolution. The effect of 1st stage resolution variation in 12-bit interpolated pipeline ADC is examined in Figure 5.31. As shown in Figure 5.31, the increasing the resolution of the stage relaxes the gain mismatch requirement. For example, to suppress the ENOB degradation less than 0.2 LSB, 0.8 % of $\Delta G/G$ is required for 4-bit 1st stage resolution. The mismatch requirement becomes severe to

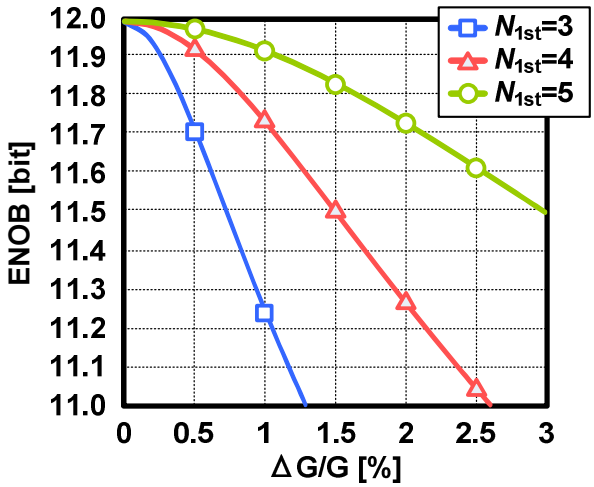


Figure 5.31 ENOB vs. gain mismatch with variation of 1st stage's resolution.

0.4 % when the resolution of the 1st stage becomes 3-bit. However, it is relaxed to 1.5 % for 5-bit 1st stage resolution. The demerits of the increasing stage's resolution are already mentioned in chapter 5.3.2 and above paragraph. Therefore, designer has to determine the resolution of the stage with consideration of the demerits and the amplifier's mismatch.

#### 5.3.5.2 Bandwidth Mismatch

The interpolated pipeline ADC does not utilize reference voltage for the pipeline stage. It means that there is no absolute value for the settling in the interpolated pipeline stage. Figure 5.32 shows output voltages of the two amplifiers in the pipeline stage. Assume that the amplifiers have only one pole; therefore, its' output voltages draws the 1st order transfer curve. If two amplifiers' bandwidth matches completely, those amplifiers have the same settling characteristic and the sampling timing becomes no matter to the ADC's performance. In other words, there is no settling requirement. Even though the output signals are sampled

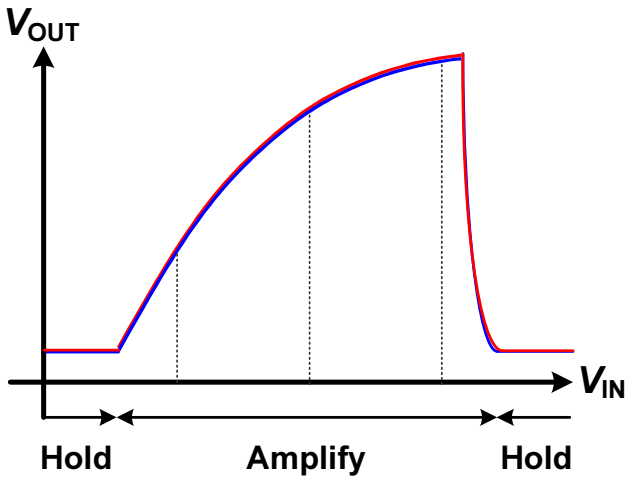


Figure 5.32 Amplifier's output signal without bandwidth mismatch.

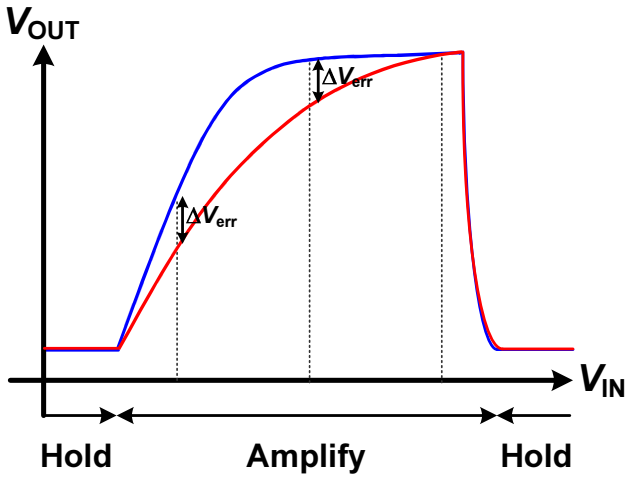


Figure 5.33 Amplifier's output signal with bandwidth mismatch.

early or lately, it is same as the amplifier's gain is changed for the A/D conversion (unless the settling characteristic is completely same), and as already explained in chapter 2.5.2, the interpolated pipeline ADC's performance is not affected by the amplifier's gain. This is a huge merit for the low power ADC design because the settling requirement is one of the main reasons for the high power consumption of the amplifier.

According to the explanation of the above paragraph, the interpolated pipeline ADC does not need to care about the amplifier's settling characteristic. However, as described in above paragraph, the relaxed settling requirement is valid when two amplifiers' bandwidths are matched. As shown in Figure 5.33, if two amplifiers' have different bandwidths, the settling characteristics are also different and the pipeline stage has to wait for sampling until two amplifiers' settling is finished. For the optimized interpolated pipeline ADC design, it is necessary to figure out the allowed bandwidth mismatch between two amplifiers for the target specification.

To examine the effect of the bandwidth mismatch, calculation and simulation are necessary. The 1st order output signal can be written as below,

$$V_{OUT} = G_0 V_{IN}\left(1 - e^{-\omega_p t}\right) \tag{5.44}$$

In (5.44), $G_0$ means amplifier's gain and $\omega_p$ means 1st pole of the amplifier. The bandwidth mismatch can be express as the gain mismatch (assume that the settling time is not enough). The effect of the gain mismatch to the interpolated pipeline ADC is examined in the chapter 5.3.5.1. Therefore, if the bandwidth mismatch can be written in terms of the gain mismatch, an ENOB formula can be derived including the bandwidth mismatch parameter.

The interpolated pipeline ADC utilizes two amplifiers. The each amplifier's gain including the bandwidth mismatch can be written as below,

$$G_1 = G_0\left(1 - e^{-\omega_p\left(1+\Delta\omega/\omega_p\right)t}\right). \tag{5.45}$$

$$G_2 = G_0\left(1 - e^{-\omega_p\left(1-\Delta\omega/\omega_p\right)t}\right). \tag{5.46}$$

The gain mismatch between two amplifiers due to the bandwidth mismatch, $\Delta G/G$ is

$$\frac{\Delta G}{G} = 2\frac{G_1 - G_2}{G_1 + G_2} = \frac{2\left(-e^{-\omega_p\left(1+\Delta\omega/\omega_p\right)t} + e^{-\omega_p\left(1-\Delta\omega/\omega_p\right)t}\right)}{2 - \left(e^{-\omega_p\left(1+\Delta\omega/\omega_p\right)t} + e^{-\omega_p\left(1-\Delta\omega/\omega_p\right)t}\right)}. \tag{5.47}$$

Assume that the settling time is assigned as the half of the sampling frequency, it means $t=1/(2F_S)$. Equation (5.47) can be arranged as,

$$\frac{\Delta G}{G}=\frac{-2\left(\exp\left(\alpha\left(1+\frac{\Delta F}{F_p}\right)\right)-\exp\left(\alpha\left(1-\frac{\Delta F}{F_p}\right)\right)\right)}{2-\left(\exp\left(\alpha\left(1+\frac{\Delta F}{F_p}\right)\right)+\exp\left(\alpha\left(1-\frac{\Delta F}{F_p}\right)\right)\right)} \tag{5.48}$$

In (5.48), $F_p$ means the frequency of 1st pole and $\Delta F/F_p$ means the 1st pole mismatch between two amplifiers, which indicates the bandwidth mismatch. Also, α is defined as below,

$$\alpha=-\frac{F_p}{F_s}\pi \tag{5.49}$$

and then, equation (5.48) is organized as

$$\frac{\Delta G}{G}=\frac{-2\left(1-\exp\left(\frac{\Delta F}{F_s}\pi\right)\right)}{2\exp\left(-\alpha\left(1+\frac{\Delta F}{F_p}\right)\right)-\left(1+\exp\left(\frac{\Delta F}{F_s}\pi\right)\right)}. \tag{5.50}$$

By substituting (5.50) to (5.43), the effect of the bandwidth mismatch to the ENOB can be calculated. Figure 5.34 shows the calculation and the simulation results. The 10-bit ADC is utilized for the examination. In Figure 5.34, the resolution of the 1st stage is 4-bit and the gain of the amplifier is assigned as 3-times. Also, $F_{3dB}$ means 3-dB bandwidth and $\Delta F_P/F_P$ means the 1st pole mismatch between two amplifiers. As explained at the 1st paragraph in this sub-chapter, if there is no bandwidth mismatch, the ENOB is not degraded even though the amplifier's bandwidth is not wide. Basically, the ENOB is degraded with increase of the

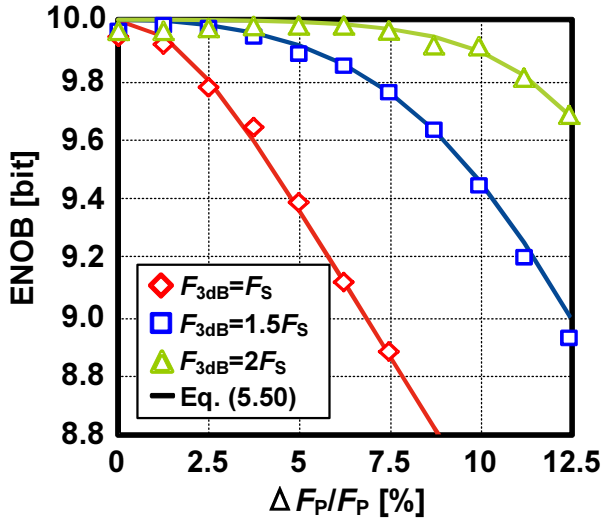


Figure 5.34 ENOB vs. bandwidth mismatch with variation of bandwidth.

bandwidth mismatch. However, the ENOB degradation is reduced with increase of the amplifier's bandwidth. For example, $2F_S$ of $F_{3dB}$ shows better performance than $F_S$ of $F_{3dB}$ when the bandwidth mismatch is the same. Therefore, to suppress the ENOB degradation by the amplifier's bandwidth mismatch, reducing the bandwidth mismatch or wide bandwidth amplifier design are effective. However, increase of the bandwidth accompanies high power consumption. Also, enough long time for settling can suppress the ENOB degradation; however, it also reduces the ADC's operation speed. The most effective way to solve this issue is elimination of bandwidth mismatch by the careful layout.

### 5.3.6 Amplifier Summary

In this sub-chapter, the amplifier's characteristics and performance requirements are analyzed and examined by the calculation and the simulation, such as the amplifier's linearity, noise, gain mismatch and bandwidth mismatch. Through the analysis, the amplifier's parameters and required mismatch characteristics are becomes clear for the target specification. For example, amplifier's $g_m$ and $R_S$ are important parameters for the amplifier's linearity. Because the amplifier's linearity affects the ENOB, it is necessary to determine the components' values carefully. Also, the gain mismatch and the bandwidth mismatch affect the ENOB; therefore, those mismatches have to be suppressed as much as possible. In the interpolated pipeline ADC design, the 1st stage resolution is one of the most important parameter because it is related to the most of the ENOB degradation analysis. Usually, the higher resolution for the 1st stage is the better for the high-performance ADC realization. However, it also accompanies several issues such as increase of power consumption and circuit complexity.

## 5.4 MDAC Stage

### 5.4.1 MDAC Noise Analysis

Some characteristics of the amplifier, such as noise and gain have to be analyzed with the MDAC stage. Several works have been published for the analysis of the MDAC stage in conventional pipeline ADC. [5.23] - [5.24] analyze the MDAC stage for noise, speed, and power consumption. Also, [5.25] proposes a performance model and an analysis of the MDAC stage for noise and speed. However, previous works are only applicable to the conventional pipeline ADC topology. Therefore, an adequate MDAC stage model and analysis are necessary for the interpolated pipeline ADC.

Figure 5.35 shows a small signal model of the 1st MDAC stage in interpolated pipeline ADC. In Figure 5.35, $R_{swi}$ is the on-resistance of the reference selection switch, $C_S$ is the sampling capacitance, $C_{pi}$ is the input parasitic capacitance of the amplifier, $C_{po}$ is the

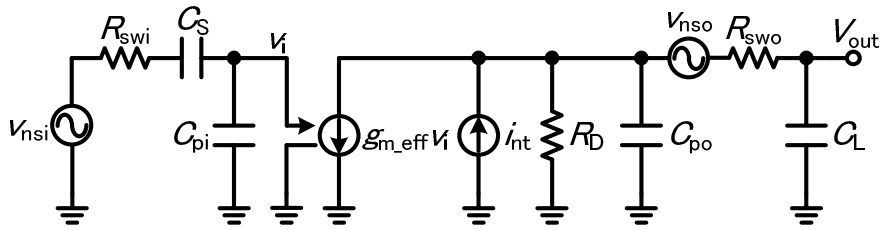


Figure 5.35 Small signal model of 1st MDAC stage in interpolated pipeline ADC.

Table 5.1 Parameters' value for noise calculation

| $V_{REF}$ [mV] | $C_S$ [fF] | $C_{po}$ [fF] | $G_{pi}$ | $G_0$ | $g_{m\_eff}R_{swi}$ | γ |
|---|---|---|---|---|---|---|
| 600 | 320 | 57 | 0.76 | 3 | 1 | 1 |

output parasitic capacitance of the amplifier, $R_{swo}$ is the on-resistance of S/H switch in the following stage, and $C_L$ is the load capacitance (sampling capacitance of the following stage). $g_{m\_eff}$ is the effective $g_m$ of source degeneration amplifier and $i_{nt}$ is the total noise current of the amplifier as shown in Figure 5.24. The input referred noise power is represented in (5.51),

$$\boldsymbol{V}_{ni}^2 = \frac{\boldsymbol{kT}}{\left(\boldsymbol{C}_L + \boldsymbol{C}_{po}\right)} \frac{1}{\boldsymbol{G}_{pi}^2 \boldsymbol{G}_0} \left( \frac{1}{\boldsymbol{G}_0} + \boldsymbol{G}_{pi}^2 \boldsymbol{g}_{m\_eff} \boldsymbol{R}_{swi} + \gamma \right) \tag{5.51}$$

where $k$ is the Boltzmann constant, $T$ is the ambient temperature, $G_0$ is the gain of the amplifier, $G_{pi}$ is the gain of the input signal path, and γ is the transistor noise coefficient. In (5.51), $R_{swo}$ (and $v_{nso}$) in Figure 5.35 is omitted because $R_{swo}$ is much smaller than $R_D$. Also, noise from the following stage is not considered. $G_{pi}$ can be defined as below.

$$\boldsymbol{G}_{pi} = \frac{1}{1 + \dfrac{\boldsymbol{C}_{pi}}{\boldsymbol{C}_S}}. \tag{5.52}$$

Equation (5.52) shows that $C_{pi}$ degrades signal's gain and worsens the ADC's SNR performance. Therefore, the input transistor size of the amplifier has to be determined with $C_{pi}$ consideration. In calculation, $g_{m\_eff}R_{swi}$ is assigned as 1 for simplicity. The other parameters' values are described in Table 5.1. On-resistance and parasitic capacitance are estimated from [5.8]. The ENOB of the ADC can be written as (5.53).

$$\mathrm{ENOB} = \boldsymbol{N} - \frac{1}{2}\log_2 \left\{ \frac{12}{\boldsymbol{V}_q^{\,2}} \frac{\boldsymbol{kT}}{\left(\boldsymbol{C}_L + \boldsymbol{C}_{po}\right)} \frac{1}{\boldsymbol{G}_{pi}^2 \boldsymbol{G}_0} \times \left( \frac{1}{\boldsymbol{G}_0} + \boldsymbol{G}_{pi}^2 \boldsymbol{g}_{m\_eff} \boldsymbol{R}_{swi} + \gamma \right) + 1 \right\}. \tag{5.53}$$

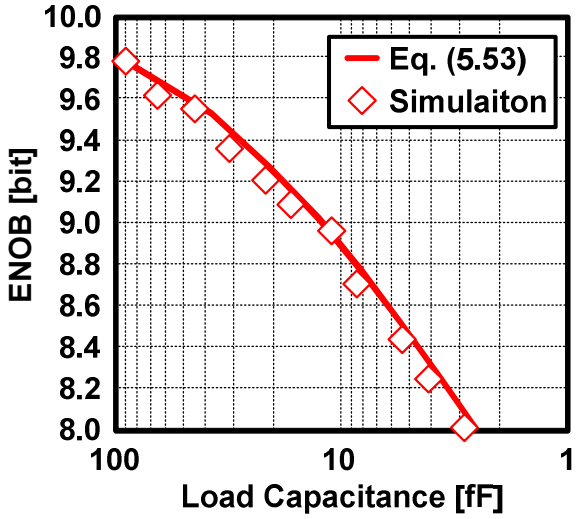


Figure 5.36 ENOB vs. load capacitance of amplifier.

More information for (5.51) and (5.53) are written in Appendix C.

Figure 5.36 shows the calculation and the simulation results of ENOB vs. load capacitance. The same ADC is utilized for the simulation in [5.8]. It is recognized that to achieve 0.2-bit of ENOB degradation, about 100 fF of the load capacitance is required. Equation (5.53) shows that in order to suppress the noise of the circuit, increasing $G_0$, $G_{pi}$, and $C_L$ are effective. In (5.53), $G_0$ is $R_D/R_S$ in the source degeneration amplifier. The gain is determined by the comparator's mismatch voltage. If the gain is increased by $R_D$, the bandwidth is degraded. $G_{pi}$ is increased by large $C_S$; however, large $C_S$ increases ADC input driver's performance requirement. The load capacitance, $C_L$ affects both noise and bandwidth; therefore, it has to be determined considering both of the effects. As described above, relationship between the parameters and the ADC's performance are complicate. Detailed design flow to determine the ADC's parameters are shown in chapter 5.6.

### 5.4.2 ADC Performance with Gain Variation

In this chapter, the interpolated pipeline ADC's $F_S$ and ENOB with changing amplifier's current ($I_D$) will be analyzed. The values of the parameters for the calculation and the simulation are the same values given in the Table 5.1. The load capacitance of the amplifier is set as 100 fF to achieve a 0.2-bit ENOB degradation, which is determined by Figure 5.36. Comparator's latch time is set as 200 ps, which is estimated from the circuit in [5.8]. $F_S$ is calculated by the settling time and comparator's latch time. The settling time is calculated within 1/4 LSB error, which is considered as the worst case. ΔENOB is calculated based on (5.53) when the ADC's resolution is 10 bit. In Figure 5.37 and Figure 5.38, the solid lines are calculation results and the symbols are simulation results.

First, the default condition performance is examined to help the understanding for further analysis. The calculation and the simulation results are shown in Figure 5.37. $F_S$

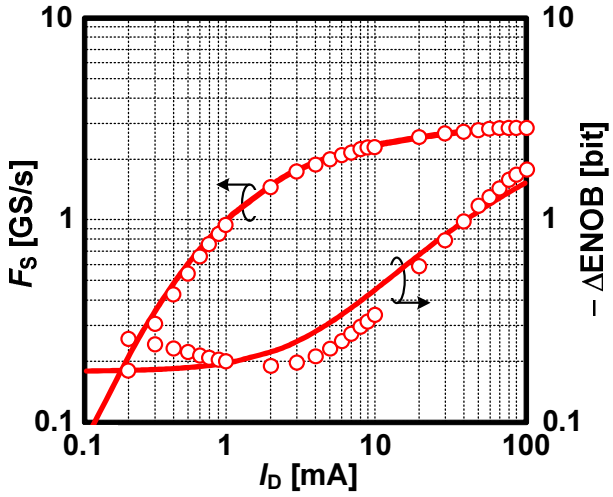


Figure 5.37 $F_S$, ΔENOB vs. $I_D$.

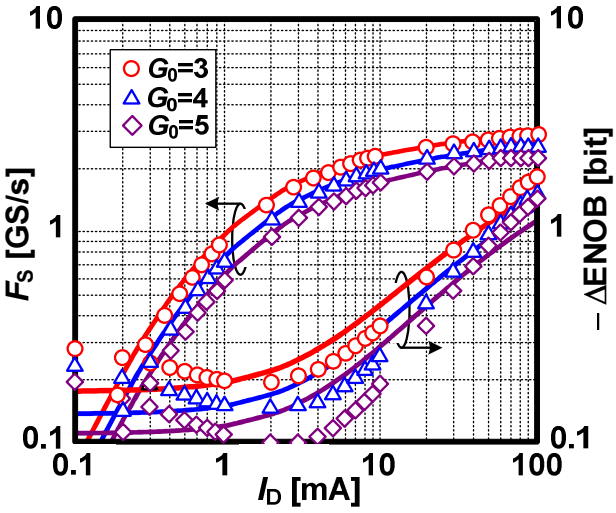


Figure 5.38 $F_S$, ΔENOB vs. $I_D$ with amplifier's gain variation.

becomes higher with increasing $I_D$. However, the growth of $F_S$ slows down significantly after 5-6 mA in Figure 5.37 because of the increase of the parasitic capacitance. Due to the same reason, the input signal gain is also reduced and it causes performance degradation of the ADC as represented in (5.52) and (5.53). In Figure 5.37, the ENOB is degraded by 0.3 bit when $I_D$ is 8 mA (simulation) and the degradation grows to 1 bit when $I_D$ reaches 40 mA. By this analysis, below 6 mA current shows reasonable performance with 1 - 2 GS/s and 0.2 - 0.3 bit ENOB degradation.

In Figure 5.37, the simulation and the calculation shows good matching in speed. However, there is a 0.1 bit difference in ENOB results from 2 mA to 10 mA. This difference might be caused by the influence of noise due to other components. Lower than 1 mA current, the noise of the simulation results increases due to 1/f noise, which is not considered in the calculation.

Figure 5.38 shows the ADC's performances by changing the amplifier's gain. The gain is controlled by the output resistance, $R_D$. In Figure 5.38, increasing the gain of the amplifier improves the ADC's SNR. However, increased $R_D$ causes narrow bandwidth of the amplifier and it degrades $F_S$. The results with different gains can be adjusted to the default results (shown in Figure 5.37) by changing the load capacitance, $C_L$. For example, $F_S$ and ΔENOB are almost same when $G_0$=3, $C_L$=100 fF and $G_0$=4, $C_L$=70 fF. Decreased $C_L$ causes increasing noise and mismatch in CDAC; however, increased gain cancels those degradations. Moreover, decreased $C_L$ brings advantages of bandwidth and core area. Therefore, within the allowance of the linearity of the amplifier, it is better to use higher gain of amplifier with smaller load capacitance.

### 5.4.3 Comparison with Multi-Bit Pipeline ADC

In this chapter, the 1st MDAC stage's resolution is assigned as 4-bit which is the same resolution as the ADC in [5.8]. The conventional pipeline ADC utilizes 1-bit resolution for its pipeline stage. On the other hand, some pipeline ADCs utilize multi-bit resolution for its pipeline stage. The 1-bit pipeline stage's structure is basically different from the interpolated pipeline ADC. However, the multi-bit pipeline stage's structure is similar with interpolated pipeline stage, because both of stages convert more than 1-bit. Therefore, comparison of multi-bit pipeline ADC and interpolated pipeline ADC is useful to choose ADC topology for target specification.

Figure 5.39 depicts the structures and output signals of 1-bit resolution and 2-bit resolution pipeline stage. The 1-bit resolution structure utilizes two capacitors in MDAC stage, a sampling capacitor ($C_S$) and a feedback capacitor ($C_F$). On the other hand, the 2-bit

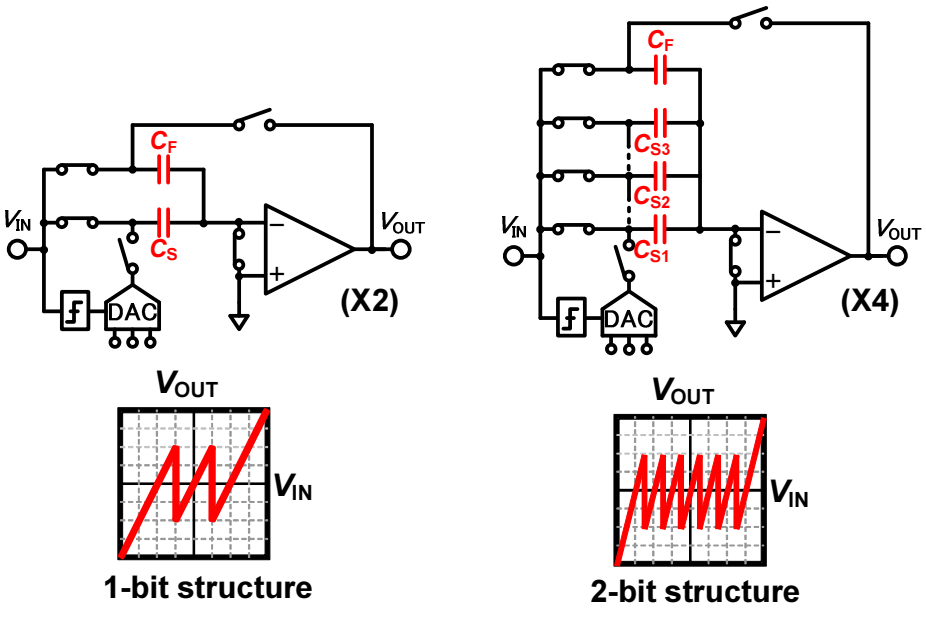


Figure 5.39 Structure of single-bit and multi-bit pipeline stage.

(multi-bit) structure utilizes several capacitors as the sampling capacitors. In Figure 5.39, there are three sampling capacitors in multi-bit MDAC stage to realize 2-bit. Also, the feedback capacitance has to be adjusted to gain of the MDAC stage because the multi-bit structure utilizes different gain. For example, 2-bit resolution stage amplifies the residue signal 4-times. The gain is determined by $2^m$, where $m$ means the resolution of the stage.

To compare the interpolated pipeline ADC with multi-bit pipeline ADC, performance requirements for the amplifier are utilized. Among the amplifier's performances, gain, linearity, and power consumption (with the ADC's operation frequency and the ENOB degradation) are selected. There are a couple of preconditions for the multi-bit pipeline ADC for comparison.

1) Only 1st stage utilizes multi-bit structure. Following stages are assumed as a single-bit structure.
2) The resolution of the multi-bit stage is assigned to same as the 1st stage of the interpolated pipeline ADC. The assigned resolution is 3-bit (considering the redundancy). Also, the ADCs' resolution is assigned as 10-bit.
3) The unit capacitors in the multi-bit stage are assumed that they do not have any mismatches. Also, the total capacitance of the sampling capacitors is assigned as the same value of $C_S$ in Table 5.1. The feedback capacitance of multi-bit stage is assigned to realize 8-times higher stage gain.
4) Other parameters of the multi-bit stage, such as following stage's sampling capacitance (amplifier's load capacitance) is assigned as the same value in the interpolated pipeline ADC's.
5) The settling time is calculated when settling error becomes less than 1/4 LSB. The analysis on the settling time in multi-bit ADC is referred to [5.26].
6) For the calculation of the ENOB degradation, it is assumed that the amplifier in the multi-bit pipeline stage has enough high DC gain to achieve 10-bit resolution of the ADC. In this analysis, the amplifier's gain is assigned as 70-dB.

#### 5.4.3.1 Amplifier's Gain in Multi-Bit Pipeline ADC

The required gain of the amplifier in the multi-bit pipeline ADC is identical to the amplifier in the conventional (single-bit) pipeline ADC. The required amplifier's gain can be written as below,

$$\boldsymbol{G} = 6\boldsymbol{N} + 10[\mathrm{dB}] \tag{5.48}$$

where $G$ means the required gain of the amplifier and $N$ means the ADC's resolution. More explanation for (5.48) is described in chapter 2.5.1.

The 1st stage's gain of the multi-bit pipeline ADC is larger than conventional pipeline ADC. It looks like to achieve better SNR; however, the single-bit pipeline ADC gets the same

gain trough the multiple-stage amplification. Therefore, the requirement for input referred noise is same between multi-bit and single-bit pipeline ADC. Equation (5.48) is derived from the feedback loop gain error in MDAC stage. And the feedback loop gain errors in multi-bit and single-bit pipeline ADC are same at the input of the stage. It means that the required gain of the amplifier in multi-bit pipeline ADC does not changed from the single-bit pipeline ADC. As a result, the multi-bit pipeline ADC has to solve the reduced gain problem in recent scaled technology of which the largest bottleneck of recent pipeline ADC development.

#### 5.4.3.2 Amplifier's Linearity in Multi-Bit Pipeline ADC

The multi-bit pipeline ADC has higher resolution of the pipeline stage (in this analysis, only 1st stage has higher resolution) than the conventional pipeline ADC. It makes relax the following stages' performance requirement because the signal amplification is large. However, the linearity requirement does not changed because the multi-bit pipeline ADC must convert the signal within full-range as well as the conventional pipeline ADC.

Figure 5.40 explains the linearity requirement between the interpolated pipeline ADC and the multi-bit pipeline ADC. As shown in Figure 5.40, the interpolated pipeline ADC's signal range is reduced by increase of the resolution. And it makes relax the amplifier's linearity requirement. However, in the multi-bit pipeline ADC, even though the stage's resolution is increased, the signal range is not change.

If the amplifier in the multi-bit pipeline ADC has enough high gain to realize the ADC, the linearity requirement usually does not become a problem. However, if the amplifier's gain is not enough and the ADC tries to solve the issue by the calibration, the linearity becomes a large portion to be corrected and it is a huge demerit.

#### 5.4.3.3 Settling Time and ENOB Degradation in Multi-Bit Pipeline ADC

The power consumption (settling time) of the amplifier is also important characteristic. To

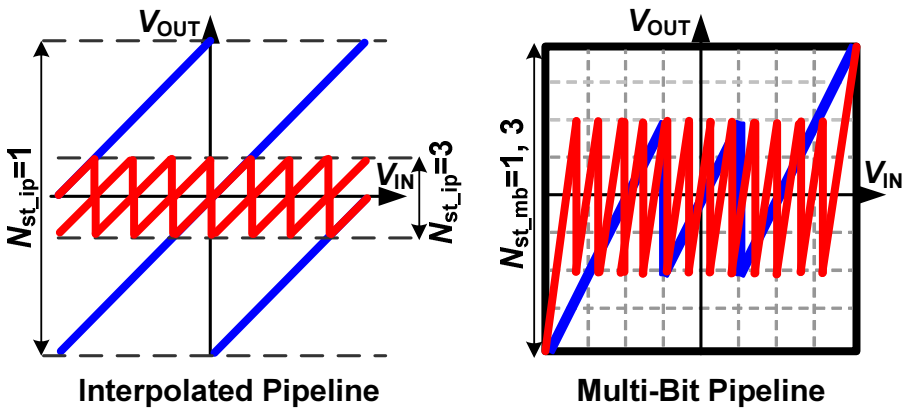


Figure 5.40 Relation of signal range and stage's resolution.

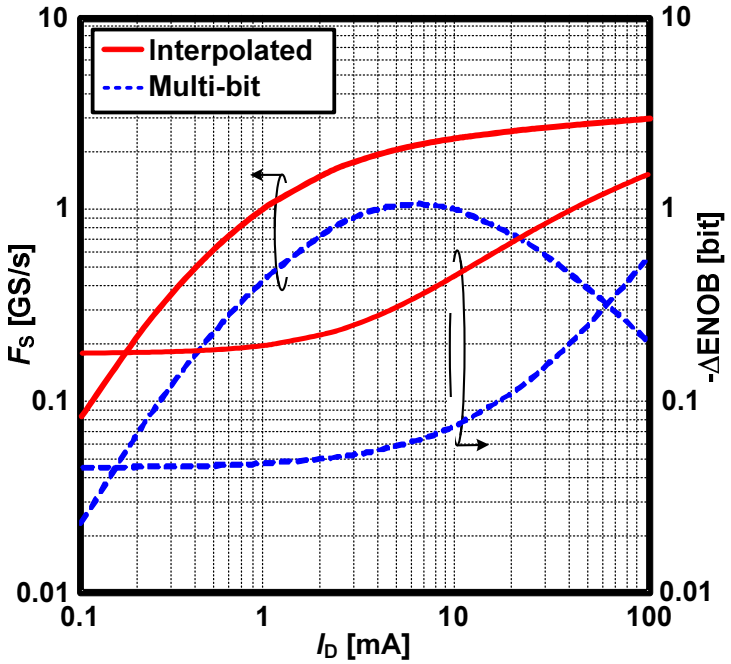


Figure 5.41 $F_S$, ΔENOB vs. $I_D$ in interpolated and multi-bit pipeline ADC.

compare the settling time of the amplifier in the multi-bit pipeline ADC and the interpolated pipeline ADC, the ADC's operation frequency and the ENOB degradation is utilized with the amplifier's power consumption. The analysis of the settling time for multi-bit pipeline ADC is referred to [5.26]. The graph form of $F_S$, ΔENOB vs. $I_D$ graph in Figure 5.37 is used for the comparison. In Figure 5.41, both of the interpolated pipeline ADC and the multi-bit pipeline ADC's operation frequency is proportional to the amplifier's current. However, the multi-bit pipeline ADC shows slow operation frequency due to the feedback capacitance at the output of the amplifier. Furthermore, the ADC's speed start to decrease around 7 ~ 8 mA. This is because the increased parasitic capacitance at the input of the amplifier affects to the settling time.

Although the interpolated pipeline ADC's operation speed is better than multi-bit pipeline ADC, the multi-bit pipeline ADC shows better ENOB characteristic. The ENOB degradation of the multi-bit pipeline ADC usually almost half of the interpolated pipeline ADC's for the calculation range. The reason of the ENOB degradation is reduced feedback factor. Along with increase of the amplifier's current, the ENOB starts to decrease; however, the gap between two ADCs is not diminished.

In this comparison, the amplifier in the multi-bit pipeline is assumed that it has enough DC gain for the ADC's resolution, such as 70-dB for 10-bit. However, difficulty of realization for such kind of high-gain amplifier using recent scaled process is already mentioned in chapter 1.3. Therefore, to be more exact, the ENOB degradation comparison has to consider the design of high gain amplifier which is the bottleneck of recent high-resolution ADC design.

#### 5.4.3.4 Comparison Summary

In this sub-chapter, the performance requirements for the amplifier in the interpolated pipeline ADC and the multi-bit pipeline ADC are compared. The multi-bit pipeline ADC has similar characteristics with interpolated pipeline ADC, such as multi-bit A/D conversion and large amplification in pipeline stage. However, the principle of the A/D conversion is basically same as the conventional (single-bit) pipeline ADC. As the result, the performance requirements of the amplifier for the multi-bit pipeline ADC is almost same as the conventional pipeline ADC.

Table 5.2 shows the comparison results of the interpolated pipeline ADC and multi-bit pipeline ADC in amplifier's gain, linearity, settling speed, and ENOB degradation. According to the Table 5.2, the multi-bit pipeline ADC shows better characteristic in the ADC's ENOB degradation. However, the high-gain requirement for the amplifier is still big issue and it makes difficult to design the high-resolution multi-bit pipeline ADC. Also, even though the stage's resolution is increased, the input-output signal range does not changed, which means the linearity requirement is not relaxed. Moreover, the amplifier's settling speed is reduced by the feedback capacitor, in which also decreases the ADC's operation speed than the interpolated pipeline ADC. Therefore, it is recognized that the interpolated pipeline ADC has advantages in comparison of the multi-bit pipeline ADC for the amplifier's performance requirement. This comparison gives some insight to design of the interpolated pipeline ADC with feedback loop which is described in chapter 6, because it has similar structure with the multi-bit pipeline ADC.

## 5.5 Pipeline Stage Resolution

The interpolated pipeline ADC can be designed with any resolution in its pipeline stage. In this sub-chapter, the optimized stage resolution is examined using the 1st stage. In the

Table 5.2 Comparison of amplifier's performance requirement.

| | **Multi-bit pipeline ADC** | **Interpolated pipeline ADC** |
|---|---|---|
| **Required gain** | Severe | **Lenient** |
| **Linearity satisfaction** | Severe | **Lenient** |
| **Settling speed** | Slower | **Faster** |
| **ENOB degradation** | **Better** | Worse |

interpolated pipeline topology, one of the most important criteria to determine the resolution of the stage is the power consumption. The pipeline stage consists of 3-parts, which are amplifiers, sub-ADC, and interpolators. In these parts, the interpolators do not consume much power because they charge and discharge its input signal dynamically. Therefore, the power consumption is determined by the amplifiers and the sub-ADC. For example, two amplifiers in 4-bit stage occupy 67 % of total analog power consumption in [5.8].

The power consumption and the circuit size in the sub-ADC increases with $2^{N1st}$, where $N_{1st}$ is the resolution of the 1st stage. Although the power consumption of each comparator is small, it increases exponentially with increase of resolution. Therefore, it is desirable to have a low-resolution for the sub-ADC. On the other hand, the power consumption of the amplifier is a function of $g_m$. As explained in chapter 5.3.2, there is a trade-off between the linearity requirement and the stage resolution. Assume that the ADC's resolution is 10-bit and $V_{FS}$ is 0.6 V. For a 4-bit resolution of the 1st stage, to achieve the ENOB degradation less than 0.2-bit, about 3.7 of $a_3/a_1$ is required. However, $a_3/a_1$ requirement becomes more severe to less than 0.45 for a 3-bit stage resolution because the output swing range of the amplifier is inversely proportional to the stage's resolution. And amplifier's linearity becomes worse with the increased signal swing range. Therefore, increasing stage resolution makes it possible to use smaller $g_m$ for the amplifiers to achieve the same ADC performance. Furthermore, it contributes to the small power consumption. The $a_3/a_1$ requirements in this paragraph are based on (5.21) and (5.28).

As described above, the power consumption of the sub-ADC and the amplifiers have an inverse proportional relationship. The calculation results of the power consumption vs. stage's resolution are shown in Figure 5.42. Parameters for the calculation are estimated from the circuit in [5.8] with 320 MHz sampling speed. Three ADC resolution examples are shown in Figure 5.42, such as 8, 10, and 12-bit for 3 to 5-bit stage resolutions. The optimized

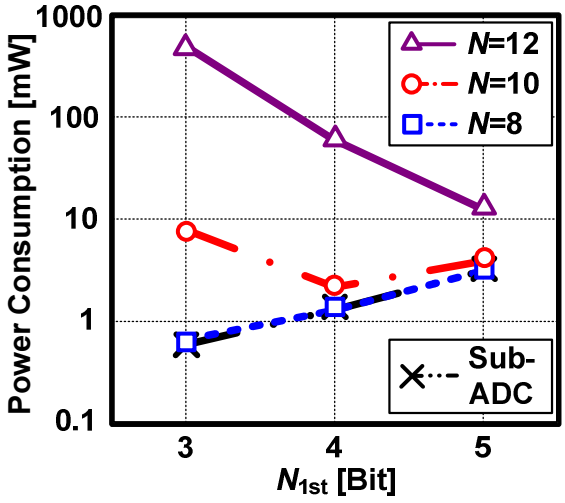


Figure 5.42 Power consumption vs. 1st stage resolution with 3 ADC resolution examples.

stage resolutions are different in each case. For example, for an 8-bit ADC, the linearity requirement is not severe; therefore, the power consumption is almost determined by the sub-ADC. In this case, source degeneration for the amplifier might not necessary. However, for 10-bit ADC, the linearity requirement becomes severe. Up to 4-bit stage resolution in 10-bit ADC, large $g_m$ for the linearity is the main reason of the large power consumption. Therefore, the power consumption is decreased with stage resolution increasing. However, when the stage resolution becomes 5-bit, the linearity requirement becomes much more relaxed and the power consumption of the amplifier is also reduced. Even though required $g_m$ becomes smaller, total power consumption is increased because of the increased number of the comparator (sub-ADC). For a 12-bit ADC, the linearity requirement becomes more severe. This causes large power consumption of the amplifiers. In that case, the linearity requirement can be relaxed by using a 5-bit stage resolution; however, the power consumption is still high. For 12-bit ADC, it may be better to use higher gain op-amp with feedback loop to reduce power consumption. 1 and 2-bit stage resolution are not considered in this analysis because it is impossible to achieve 1-bit redundancy with below 2-bit structure by the interpolation. From the 2nd stage, the resolution is determined by the designer because the linearity requirement is not severe like the 1st stage. Considering of power consumption and core size of the sub-ADC, 3 or 4-bit resolution is suitable.

## 5.6 Design Flow

Similar to the conventional pipeline ADC, the amplifier determines the performance of the interpolated pipeline ADC. However, the important point is not the gain but the linearity due to low-gain characteristic and open-loop usage. To achieve the target performance, linearity enhancement technique is essential such as source degeneration. However, linearity improvement affects other performance, such as increase of the power consumption. Therefore, the trade-off between design parameters needs to be verified.

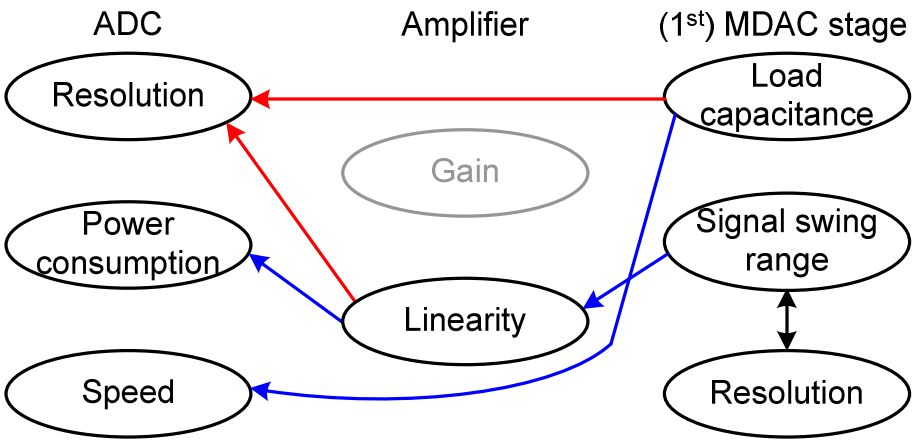


Figure 5.43 Trade-off for interpolated pipeline ADC design.

Figure 5.43 shows the simple trade-off in the interpolated pipeline ADC design. The parameters used in this chapter are listed in Figure 5.43. As explained above, the gain of the amplifier is not considered in this trade-off because it is not crucial. In Figure 5.43, the red colored line means positive effect, which means one parameter becomes better; the related parameter also becomes better. The blue colored line means opposite. It means that one parameter becomes better, the related parameter becomes worse. For example, if the amplifier's linearity is improved; the ADC's resolution is also increased. On the contrary, when the amplifier's linearity is improved, the ADC's power consumption is increased. The trade-off in Figure 5.43 is rough; however, remembering the trade-off is useful for design of the interpolated pipeline ADC, especially for determination of the parameter.

Also, a reasonable design flow to determine the parameters is shown in Figure 5.44. When the ADC specification is given, designers have to examine the validity of the interpolated pipeline topology for the given specification. The validity can be checked by Figure 5.37. If the interpolated pipeline is determined as a suitable topology, the resolution of the 1st stage can be optimized by Figure 5.42.

The ADC's performance can be represented by the operation speed and the resolution. After the stage resolution is determined, other parameters have to be assigned to

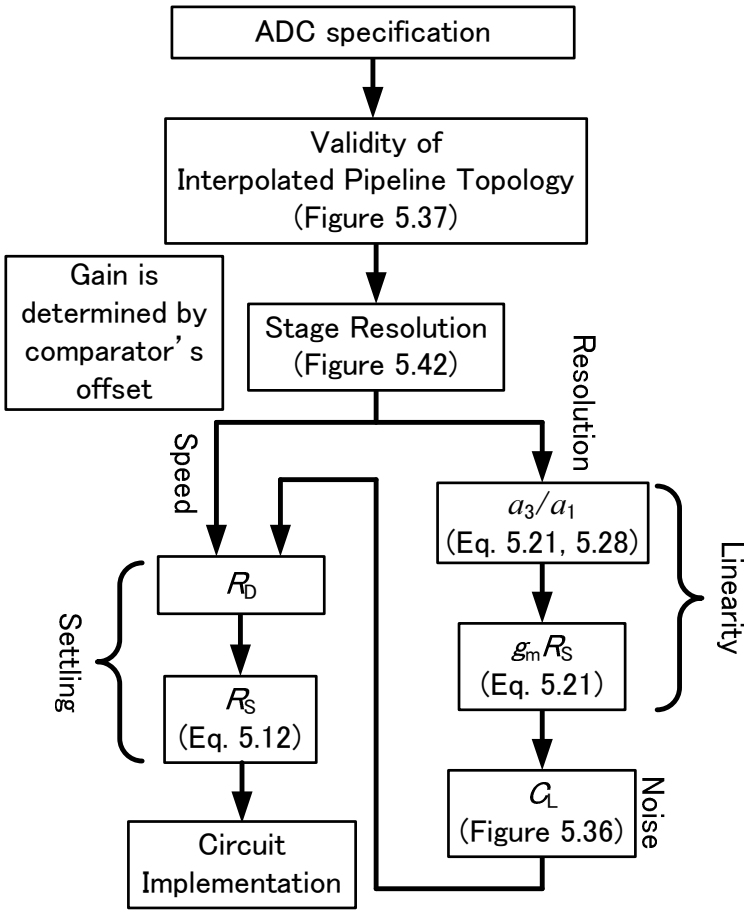


Figure 5.44 Design flow of interpolated pipeline ADC.

satisfy the target speed and resolution. The resolution is affected by the amplifier's linearity and noise characteristics. For the linearity, $g_m R_s$ is calculated by $a_3/a_1$ requirement for the given ADC specification, using (5.21) and (5.28). The noise requirement is achieved by selecting a proper value for $C_L$, which is shown in Figure 5.36. On the other hand, $C_L$ affects to the bandwidth. Also, $R_D$ is a parameter for the bandwidth. Because $C_L$ is already defined, $R_D$ can be calculated for the bandwidth requirement. After that, $R_S$ is determined by the gain, which is determined by the comparator's mismatch voltage. Through above design flow, designers can estimate the required values for the parameters to achieve target specification.

## 5.7 Conclusion

In this chapter, the design of the interpolated pipeline ADC using low-gain open-loop amplifiers has been introduced. The interpolated pipeline topology allows high-resolution ADC to be realized with low-gain open-loop amplifiers by using the interpolation technique. To realize the ADC without any MDAC calibration, parameters of the amplifiers and the MDAC have to be determined based on proper analysis, especially for linearity, noise, and settling time. In this chapter, the linearity requirement and the noise characteristic of the amplifier are analyzed. Through the given analysis, the required parameters of the amplifier become clear, such as $g_m R_S$. Also, the noise analysis of MDAC suggests the value of $C_L$ with considering the ENOB degradation. The performance limitation of the interpolated pipeline ADC is shown by $F_S$ and ΔENOB vs. $I_D$ with the amplifier's gain variation. Finally, the stage resolution optimization is discussed based on the power consumption. Through the above analysis, $g_m$, $R_S$, $R_D$, and $C_L$ are determined for the target specification. Also, the issues of interpolated pipeline ADC design and the comparison of the multi-bit pipeline ADC are analyzed. The analysis for the ADC design is organized in Figure 5.44 as a design flow chart. The analysis shows that the interpolated pipeline ADC is suitable for the recent scaled technology and has a strong potential for future development.

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# 6. A 12-bit Interpolated Pipeline ADC using Body Voltage Controlled Amplifier

## 6.1 Introduction

High data-rate and high performance telecommunication systems are the leading parts in the recent SoC field. The data-rate in the telecommunication system is determined by not only RF circuits but also baseband circuits. Among the baseband circuits, ADC is the most important part because the signal bandwidth and the SNR are almost determined by the performance of the ADC. In the recent telecommunication systems, high-resolution (> 10-bits) and high-speed (> 100 MS/s) ADCs are usually required. To fulfill the requirements for the ADC, the pipeline architecture is a good candidate. However, the recent scaled CMOS technology makes the design of the pipeline ADC difficult due to the low intrinsic gain of the transistor and the narrow signal swing range of the system. Among those problems, the low intrinsic gain is more serious for the pipeline ADC because the ADC's linearity is limited by the finite DC gain of the amplifier. For example, more than 80-dB DC gain of the amplifier is required for a 12-bit pipeline ADC.

There are two methods to solve the amplifier's gain issue. One method is increasing the amplifier's DC gain using gain boosting technique. The amplifier in [6.1] utilizes nested gain boosting and two-level recursive boost technique to achieve 130-dB DC gain. Also, a three-stage amplifier using RNMC technique is shown in [6.2]. The amplifier in [6.2] achieves more than 90-dB DC gain although it uses 65 nm CMOS technology. Those techniques used in the amplifiers can increase the amplifier's gain to the necessary level; however, bandwidth of the amplifier is degraded due to the phase compensation and the design complexity is increased by the several gain-boosting techniques. Another method to solve the amplifier's gain issue is incorporating the calibration technique to the MDAC stage in the pipeline ADC. Several calibration techniques have been introduced for the purpose [6.3] - [6.8]. The works in [6.3] - [6.4] utilize LMS engine to calibrate the amplifier's nonlinearity and the capacitor mismatch of the MDAC stage. However, utilizing LMS engine causes long calibration time and extra power consumption. Moreover, the calibration method in [6.3] - [6.4] is a foreground calibration which cannot track temperature variation during circuit operation. The ADC in [6.5] combines foreground and background calibration. It reduces the calibration time effectively; however, the temperature variation problem during circuit operation is still crucial. Moreover, the power consumption and the core area are increased by the extra MDAC stage for the calibration. The MDAC stage's gain calibration methods also have been reported. The ADC in [6.6] adjusts the reference voltages in each pipeline stage to realize accurate MDAC stage gain. The limitation of this method is that the calibration can only be realized when the amplifier's linearity is guaranteed. Tuning the feedback capacitance of the amplifier's feedback loop is introduced in [6.7]. This method can be realized in a simple way;

however, the increased capacitance of the amplifier's output node reduces the amplifier's bandwidth. Improving the amplifier's gain by forming the positive feedback loop has been introduced in [6.8]. The calibration technique in [6.8] can increase the amplifier's gain up to the required value; however, an auxiliary ADC for the calibration causes an increase of power consumption and core area. The works mentioned above show that incorporating calibration technique accompanies some disadvantages, such as increasing of power consumption, core area, and circuit complexity. More information on calibration is explained in chapter 2.6.

Recently, pipeline ADCs using interpolation technique are introduced [6.9] - [6.10]. These ADCs achieve high-resolution (> 10-bit) and high-speed (> 300 MS/s) with relatively low-gain amplifiers. For example, the work in [6.9] realizes 10-bit, 320 MS/s ADC with only 9.5-dB gain amplifier. Another ADC in [6.10] achieves 12-bit 800 MS/s using 40-dB gain pseudo differential amplifier with 4-times interleaving. These become possible by the property of the interpolation, which allows the ADC's performance to be independent of the amplifier's DC gain. Even though the interpolation technique relaxes the gain requirement of the amplifier, the linearity of the amplifier is still crucial. Especially higher than 12-bit resolution ADC, a low-gain open-loop amplifier in [6.9] consumes too much power to satisfy the linearity requirement. For this case, a relatively high gain amplifier with feedback loop is a good candidate for the amplifier's topology, such as in [6.10].

In this chapter, a 12-bit interpolated pipeline ADC with body voltage controlled amplifiers is presented. Chapter 6.2 introduces the structure of the proposed ADC, which is based on [6.9]. The offset calibration method for the proposed amplifier is also introduced in chapter 6.2. Chapter 6.3 describes the proposed body voltage controlled amplifier. The amplifier's operation, current biasing method and common mode feedback loop are explained in detail. After that, the simulation and the measurement results are presented in chapter 6.4. Finally, this chapter is concluded in chapter 6.5.

## 6.2 12-bit Interpolated Pipeline ADC Structure

In this sub-chapter, the proposed 12-bit ADC's structure is explained. The proposed ADC utilizes the interpolation technique to relax the gain requirement of the amplifier. Several methods have been introduced to realize the interpolation. Traditionally, the resistor ladder is used for the interpolation, for example, ADCs in [6.10] - [6.15]. After the MOS transistor is used widely for circuit design, combination of the resistor ladder and the capacitor array is suggested [6.16] - [6.18]. Meanwhile, gate-weighted input MOS transistors in comparator is utilized to ADCs in [6.19] - [6.20] for the interpolation. The proposed ADC incorporates two interpolation techniques; weight controlled CDAC for the reference selection and gate-weighted MOS transistor interpolation for comparator. Both of techniques contribute to reduce the number of circuit components. Therefore, power consumption and core area are

reduced. Furthermore, the CDAC improves the settling time characteristic in comparison with using RDAC. The schematic and the operation of the CDAC in the pipeline stage are explained in chapter 5.2.2.1 and [6.21]. Also, the explanation of the gate-weighted interpolation and the comparison of the CDAC and the RDAC are described in chapter 3.3.2 and chapter 3.2.5, respectively [6.22].

Figure 6.1 shows a block diagram of the proposed 12-bit interpolated pipeline ADC, in which consists of 5-stages. The 1st stage converts 4-bit and the other four stages convert 3-bit. The ADC employs 1-bit redundancy in 1st to 4th stages to reduce the effect of the comparator's offset voltage. The ADC in [6.9] utilizes only open-loop amplifiers with source degeneration. However, as explained in chapter 1, the power consumption of the amplifier increases so much for 12-bit resolution when the open-loop topology is used. In the proposed ADC, the 1st stage uses the proposed body voltage controlled amplifier with 45-dB gain and feedback loop. The single stage open-loop amplifiers are used for the 2nd to 4th stages, since the linearity requirement is not severe for those stages. The feedback loop gain of the 1st stage is 4-times and the open-loop gain from 2nd to 4th stages is 3-times. There is no calibration circuit for the linearity or the gain mismatch in the stages, which is one of the merits of the proposed 12-bit interpolated pipeline ADC.

### 6.2.1 Amplifier's Offset Calibration

Offset voltages of the open-loop amplifiers in the 2nd to 4th stages can be cancelled by the output offset cancellation technique as explained in chapter 5.2.3.2 and [6.23]. This is possible because those open-loop amplifiers have small DC gain and they do not need to work

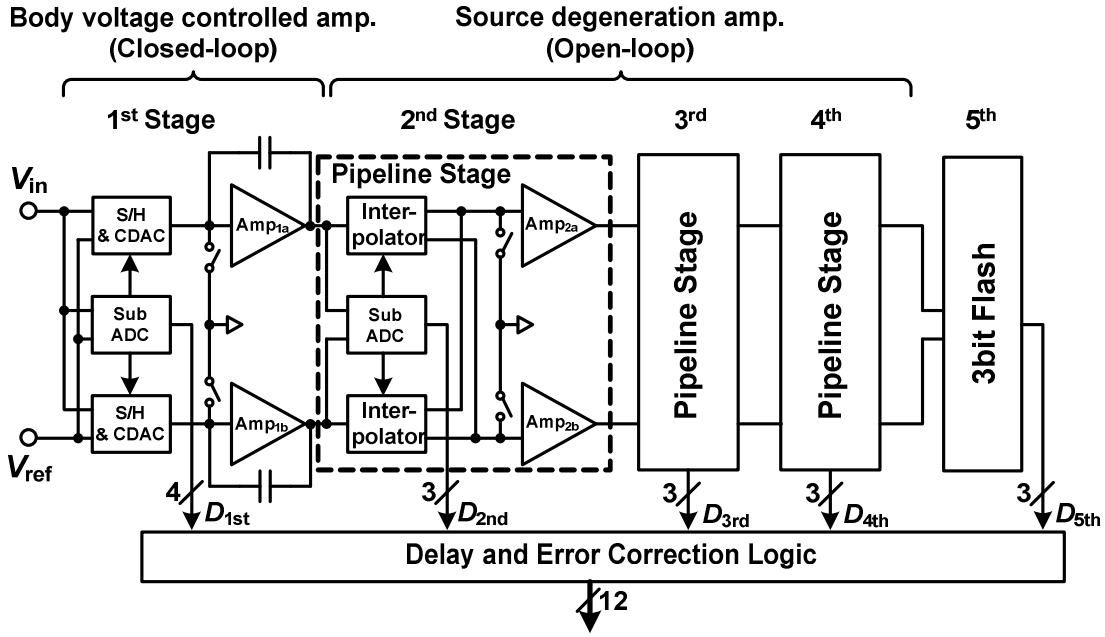


Figure 6.1 Block diagram of proposed 12-bit interpolated pipeline ADC.

during holding phase. Also, the following stages utilize the CDAC as a S/H circuit, therefore, an additional circuit is not necessary. However, the amplifier with capacitive closed-loop topology in the 1st stage cannot use the same approach. Due to the switched-capacitor amplifier topology, the output node of the amplifier has to be connected to the common-mode voltage ($V_{COM}$) to prevent the memory effect. Therefore, the other offset calibration technique has to be applied for the 1st stage amplifier.

Figure 6.2 illustrates the proposed amplifier's offset calibration circuit with CDAC. As mentioned before, the proposed ADC utilizes 1-bit redundancy structure from 1st to 4th stages. Because the ADC utilizes CDAC for the reference selection in the 1st stage, the redundancy can be realized by the extra capacitor ($C_{OFF}$) of the CDAC as shown in Figure 6.2.

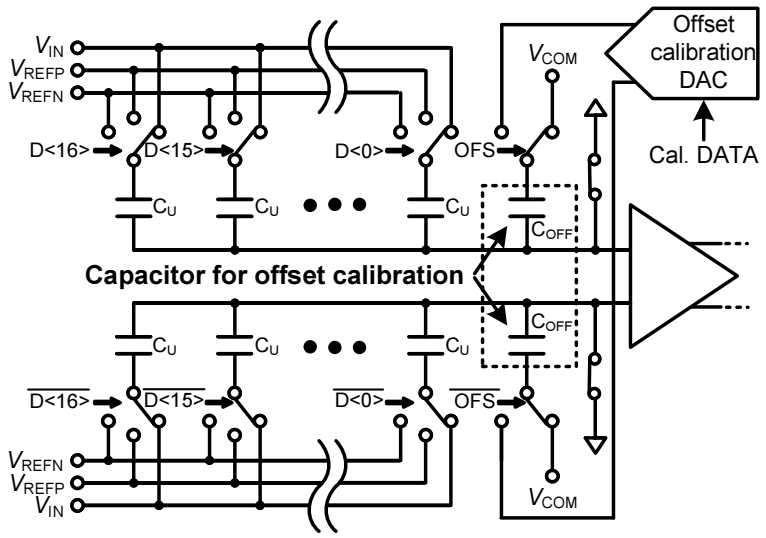


Figure 6.2 Structure of CDAC with amplifier's offset calibration in 1st stage.

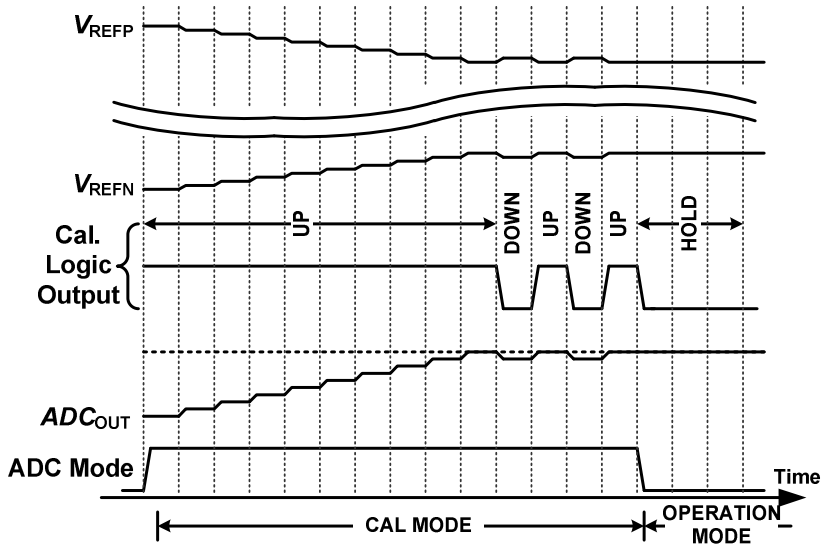


Figure 6.3 Procedure of offset calibration for amplifier.

Basically, the capacitor charges and discharges via $V_{COM}$ and reference voltages, i.e. $V_{REFP}$ or $V_{REFN}$, accordingly. The ADC controls these reference voltages for the amplifier's offset calibration. Figure 6.3 shows the procedure of the offset calibration. During the offset calibration mode, the ADC's input nodes are connected to $V_{COM}$. If there is no offset in the amplifier, the ADC's output becomes the middle value (code=2048). On the other hand, if the amplifier has an offset, the output goes up or down from the middle value. The ADC verifies this value and adjusts the reference voltage to calibrate the amplifier's offset. This function can be realized by the simple comparison of the ADC's output with middle value and an extra DAC for the generation of calibrated reference voltage.

### 6.2.2 Amplifier's Linearity

For the interpolated pipeline ADC, the amplifier's linearity is more crucial than gain. The severity for the linearity requirement is proportional with the ADC's resolution. For example, a low-gain open-loop amplifier with source degeneration resistor has enough linearity characteristic for the 10-bit resolution interpolated pipeline ADC [6.9]. However, it is not enough for the 12-bit resolution. The relationship between the amplifier's linearity and the ADC's performance is shown in Figure 6.4. In Figure 6.4, the x-axis is linearity characteristic of the amplifier and y-axis is the ENOB. The linearity characteristic in Figure 6.4 is defined by the formula,

$$V_{OUT} = a_1 V_{IN} - a_3 V_{IN}^3. \tag{6.1}$$

Equation (6.1) shows the input-output relationship of the amplifier. In (6.1), up to the 3rd order terms are considered for the linearity since it is dominant. For example, $a_5$ is almost half of $a_3$ when $V_{IN}$ is +/- 75 mV. Also, it is assumed that 2nd order term is cancelled by the differential topology. The ENOB with the consideration of the amplifier's linearity can be written as,

$$\text{ENOB} \approx N - \frac{1}{2}\log_2\left\{1 + 2.9\left(\frac{a_3}{a_1} V_{FS}^2 2^{N-3N_{1st}}\right)^2\right\}. \tag{6.2}$$

In (6.2), $N$ means the ADC's resolution, $V_{FS}$ means full-scale reference range and $N_{1st}$ means the 1st stage's resolution in the interpolated pipeline ADC. The amplifier's linearity is represented as $a_3/a_1$ in (6.2). More explanation for (6.2) is described in chapter 5.3.2.

The calculation and simulation results in Figure 6.4 are performed by the same structure and the same condition of the proposed 12-bit interpolated pipeline ADC. For the calculation and the simulation, $V_{FS}$ is assigned as 75 mV and $N_{1st}$ is assigned as 4. Only the 1st stage of the ADC uses transistor model and the other stages use ideal model to verify the effect of the 1st stage accurately. This is reasonable because the 1st stage is the most

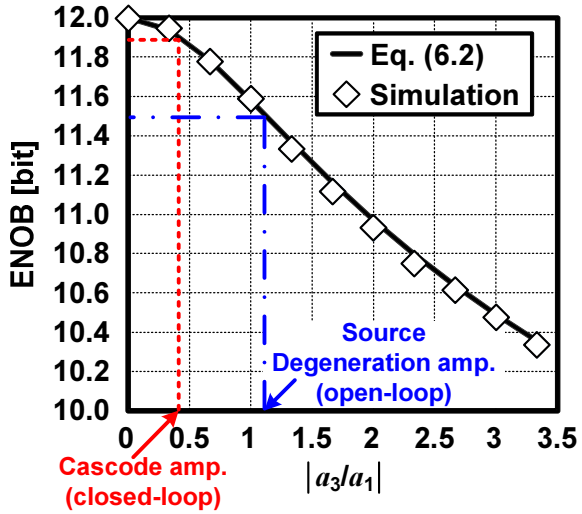


Figure 6.4 ENOB vs. linearity of amplifier for 12-bit ADC resolution.

important in the pipeline ADC. Figure 6.4 shows that if the 12-bit ADC utilizes the low-gain open-loop source degeneration amplifier (chapter 5.3.1); the ENOB is degraded about 0.5-bit by the effect of only the 1st stage's amplifier. Such amount of degradation is too large for ADC design. On the other hand, if the ADC utilizes a closed-loop cascode amplifier with a DC gain of 45-dB, the ENOB degradation is suppressed to 0.2 bit, which is a reasonable amount.

The open-loop amplifier has advantages, such as fast settling time and simple amplifier's offset cancellation. Although the low-gain open-loop amplifier with source degeneration is utilized in the ADC design, the linearity requirement might be satisfied by increase of $g_m$ as described in chapter 5.3.2. However, hundreds of milliwatt of the power consumption is required to achieve the linearity requirement. Therefore, the cascode amplifier with 45-dB gain and feedback loop is preferable.

## 6.3 Body Voltage Controlled Amplifier

As noted in chapter 6.2, the linearity of the amplifier is the most important parameter for the interpolated pipeline ADC. Because the open-loop topology has advantages of fast settling time and simple offset cancellation, it is preferable to use the open-loop amplifiers if the linearity requirement can be satisfied. Several works have been published for the amplifier's linearity improvement technique. A FVF amplifier has been introduced in [6.24] to improve the linearity characteristic. The problem of the FVF technique is that the performance is determined by the amplifier's feedback loop gain. Since the interpolated pipeline stage gain is limited to small value, the FVF technique is not suitable for the ADC design. The MIFG technique also improves the amplifier's linearity [6.25]. However, the MIFG requires extra process and it causes extra cost. An amplifier using double pseudo differential pair in [6.26] shows good linearity. Also, the amplifier has simple structure and no extra process. However, the linearity performance varies easily by the mismatch of the pseudo differential pair. As

describe above, increasing the linearity characteristic of the amplifier is a huge challenge. As a result, using a relatively high gain amplifier with feedback loop is a reasonable solution for the proposed 12-bit interpolated pipeline ADC.

As shown in Figure 6.4, a 45-dB gain cascode amplifier with feedback loop can suppress the ENOB degradation to less than 0.2 bit. The amount of 45-dB is derived from the cascode amplifier's gain without any gain-boosting technique in the given 90 nm CMOS technology. There are two general topologies for the cascode amplifier. One is the folded cascode amplifier and another one is the telescopic amplifier. Figure 6.5 depicts the schematics of the two cascode amplifiers. The most of folded cascode amplifier has a wide swing range because only 4-$V_{DS}$ are necessary for the amplifier's operation. However, it has two differential current paths and it causes large power consumption. On the other hand, the telescopic amplifier has only one differential current path. However, it requires 5-$V_{DS}$ for the amplifier's operation and it degrades the ADC's SNR characteristic. To solve the amplifier's topology issue, a body voltage controlled amplifier, which is based on the inverter-based amplifier, is introduced for the proposed 12bit interpolated pipeline ADC. Therefore, it is reasonable to examine the inverter-based amplifier topology before the proposed amplifier explanation.

Table 6.1 Comparison table of two conventional cascode amplifiers.

| | Folded Cascode | Telescopic |
|---|---|---|
| Power consumption | High (4*I*) | **Low (2*I*)** |
| Output swing range | **Wide ($V_{DD}$-4 $V_{ds}$)** | Narrow ($V_{DD}$-5 $V_{ds}$) |

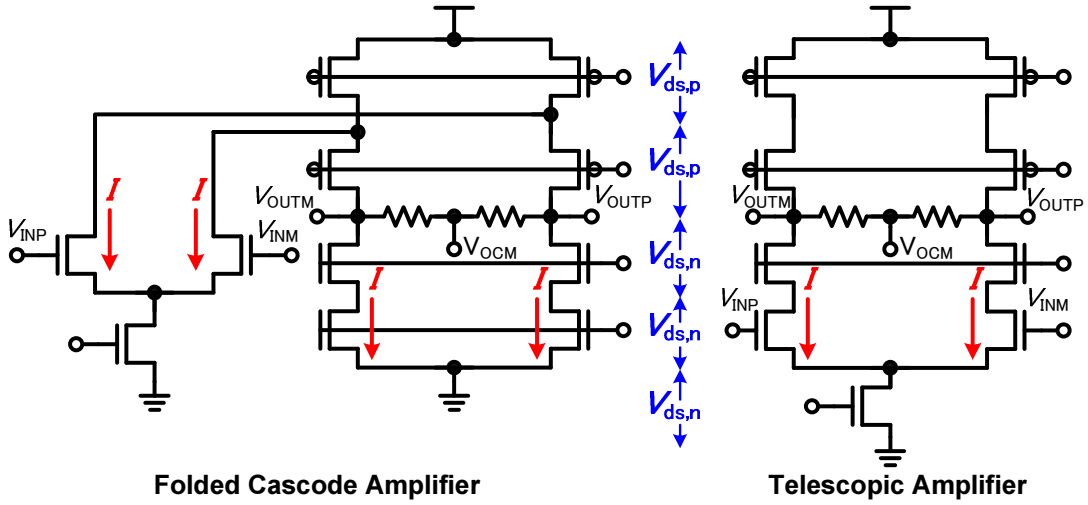


Figure 6.5 Schematics of folded cascode and telescopic amplifier.

### 6.3.1 Inverter-Based Amplifier Topology

An inverter-based amplifier is utilized in many fields, such as LNA and ADC [6.27] - [6.29]. Usually, the inverter-based amplifier is designed using multi stage topology. The multi stage inverter-based amplifier can achieve high gain, for example, the amplifier in [6.28] achieves 90-dB gain. However, multi stage inverter-based amplifier has a limited operation speed due to the phase margin compensation and has a complex structure for the DC biasing. By virtue of the interpolation technique, the proposed ADC does not require such kind of high gain. Therefore, a single stage inverter-based amplifier with cascode transistor is enough. This topology is more suitable for the high-speed operation because it is not necessary to care the amplifier's phase margin.

Figure 6.6 shows the basic topologies of the cascode inverter-based amplifier. $C_{FB}$, $C_{FBP}$ and $C_{FBN}$ in Figure 6.6 indicate the feedback capacitors for switched capacitor circuit operation. Also, $C_B$, $C_{BP}$ and $C_{BN}$ indicate capacitors for DC biasing. There are two kinds of usage for the DC biasing of the inverter-based amplifier. One is using input common-mode level (Figure 6.6.(a)) and another one is using input signal level shift technique (Figure 6.6.(b) and 6.6.(c)). Figure 6.6.(a) has a simple structure, however, the power efficiency is not good because the gate-source voltage of input transistors is fixed to common-mode voltage. On the other hand, amplifiers in Figure 6.6.(b) and 6.6.(c) have better power efficiency because there gate-source voltages are shifted. However, the implementation of Figure 6.6.(b) and 6.6.(c) becomes complex because two-path feedback is required. Moreover, the core area of Figure 6.6.(b) is increased by $C_B$ and the noise characteristic is degraded the reduction of the input signal due to the charge redistribution. Figure 6.6.(c) can be implemented without increasing core area in the proposed 12-bit interpolated pipeline ADC by using unit capacitors in CDAC as $C_{BP}$ and $C_{BN}$. However, the design becomes more complex than Figure 6.6.(b) and it degrades the amplifier's attractiveness. As the results, Figure 6.6.(a) is selected for the amplifier topology in the proposed ADC.

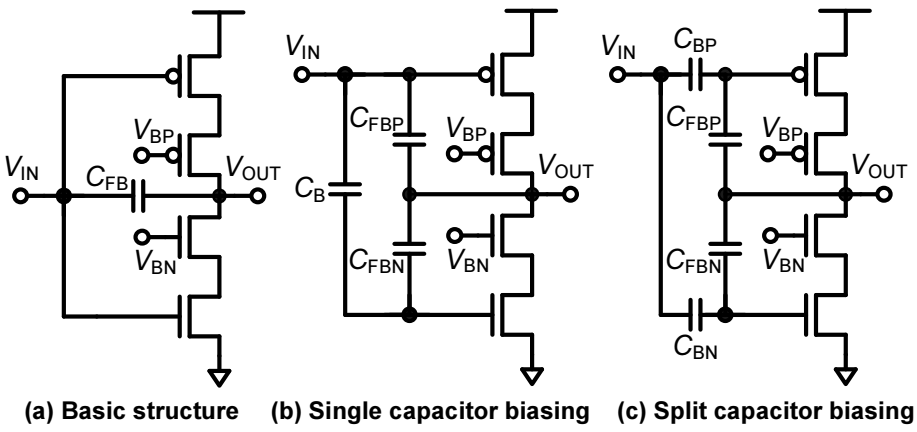


Figure 6.6 Structures of inverter-based amplifier.

### 6.3.2 Proposed Amplifier Structure

In the previous sub-chapter, the inverter-based amplifier is chosen for the amplifier topology in the proposed 12-bit interpolated pipeline ADC. However, the inverter-based amplifier is usually used without tail current source and common-mode feedback loop as shown in Figure 6.6. Therefore, it is necessary to insert the constant current biasing circuit for the amplifier. The simplest method is inserting a tail current transistor to the amplifier. However, it reduces the amplifier's signal swing range. In the proposed 12-bit interpolated pipeline ADC, the body voltage control method is proposed for the constant current biasing.

Figure 6.7 shows the topology of the proposed body voltage controlled amplifier. The amplifier incorporates the cascode inverter-based topology to increase gain with simple structure. Furthermore, the CMOS input achieves faster settling time by increasing the amplifier's transconductance. There are two additional MOS transistors ($M_{NB1}$ and $M_{NB2}$) in the proposed amplifier for current biasing. Furthermore, there are two feedback loops in the amplifier. One is for the current biasing and the other is for the CMFB. This might cause unstable operating point for the amplifier if the feedback loop values are chosen incorrectly. In order to prevent this issue, a large capacitance ($C_{STBL}$) is inserted in the CMFB loop for the stabilization. There is only one differential current path in the proposed amplifier. In addition, the amplifier stacks only four MOS transistors. This means that the proposed amplifier has the advantages of the telescopic amplifier consuming small power ($2I$) and of the folded cascode amplifier realizing a large output signal swing ($4 \cdot V_{DS}$). These characteristics are

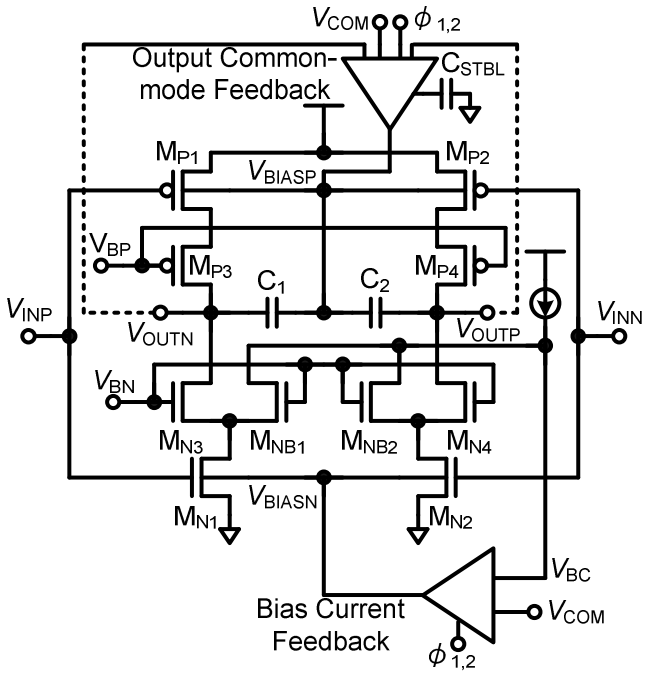


Figure 6.7 Schematic of body voltage controlled amplifier.

accomplished by body voltage control technique which is detailed in the following sub-chapters.

### 6.3.3 Body Voltage Controlled Current Biasing

As mentioned in chapter 6.3.1, the proposed amplifier is implemented without the input signal level shift topology for the simple structure. Even though the input common-mode level is defined by the CDAC, the current biasing circuit is necessary for the amplifier's operation. Instead of the traditional current source, the current mirroring in NMOS cascode transistor by body voltage control technique is applied to the proposed amplifier. Because the current of the MOS transistor is a function of $g_m$ and $g_{mb}$, the current can also be adjusted by body voltage control. The $g_{mb}$ can be defined as below,

$$g_{mb} = \mu_n C_{ox} \frac{W}{L}(V_{GS} - V_{TH})\left(-\frac{\partial V_{TH}}{\partial V_{BS}}\right). \tag{6.3}$$

Figure 6.8 shows the detailed current biasing method in the proposed amplifier. In Figure 6.8, the current of $2I$ flows from the current bias circuit to the amplifier. These current's paths are connected to the bias NMOS transistors ($M_{NB1}$ and $M_{NB2}$). The bias NMOS transistors and NMOS cascode transistors ($M_{N3}$ and $M_{N4}$) of the amplifier have the same gate-source voltages which result in current mirroring from NMOS bias transistors to NMOS cascode transistors. The current of the amplifier can be defined as below,

$$W_{NB1,2} : W_{N3,4} = I : \alpha I \tag{6.4}$$

where $W$ means MOS transistor's size and α means the size ratio of $M_{NB1,2}$ to $M_{N3,4}$. Equation (6.4) shows that the amount of current can be controlled by the transistor size. Nonetheless, if

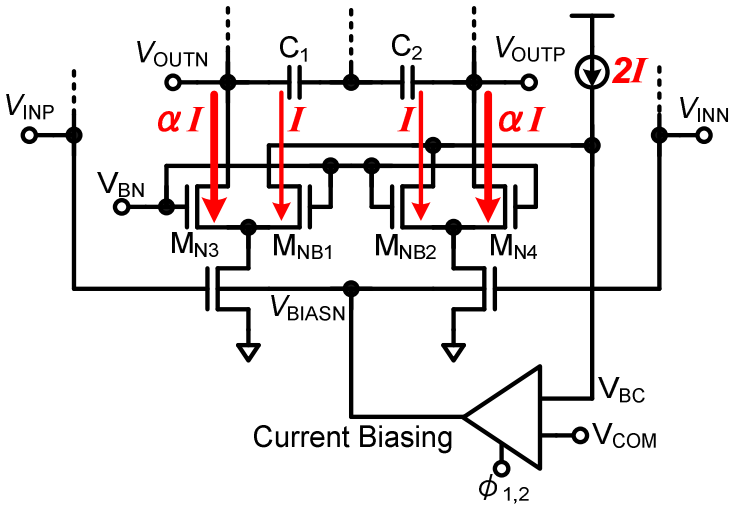


Figure 6.8 Current biasing method of proposed body voltage controlled amplifier.

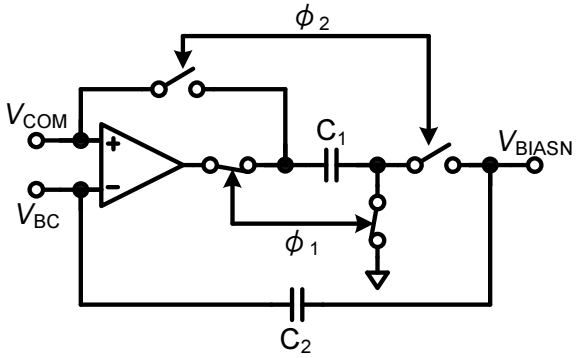


Figure 6.9 Feedback loop for current bias.

the drain voltages of the input NMOS transistors ($M_{N1}$ and $M_{N2}$) vary, the current changes also. To keep the current constant, a feedback loop is introduced from current bias circuit to the body of the input NMOS transistors. When the current of the bias NMOS transistor is changed, the feedback loop senses its variation and adjusts the body voltage of the input NMOS transistors. Figure 6.9 depicts the structure of the current bias feedback loop that works as a switched capacitor circuit. In the feedback loop, $C_2$ is charged by the current from the bias circuit. During $\phi_1$, $C_1$ is charged by the difference between $V_{BC}$ and $V_{COM}$ by the amplifier. During $\phi_2$, the charged difference is applied to the body voltage. The amplifier in the feedback loop is a single-stage amplifier because the feedback loop does not require high gain.

It is necessary to figure out the current control ability of the current bias feedback loop. Figure 6.10 presents the simulation results of $g_{mb}$, $I_{ds}$ vs. $V_{bs}$. The range of $V_{bs}$ is determined by the actual control range of the feedback loop. The current variation range is from 4.5 mA to 10.5 mA with a default current of 7 mA, which is wide enough for the current adjustment. The current control voltage range ($V_{bs}$) in Figure 6.10 includes +/- 0.2 V margin. The amount of margin is estimated by the mismatch simulation. Within the whole range, the

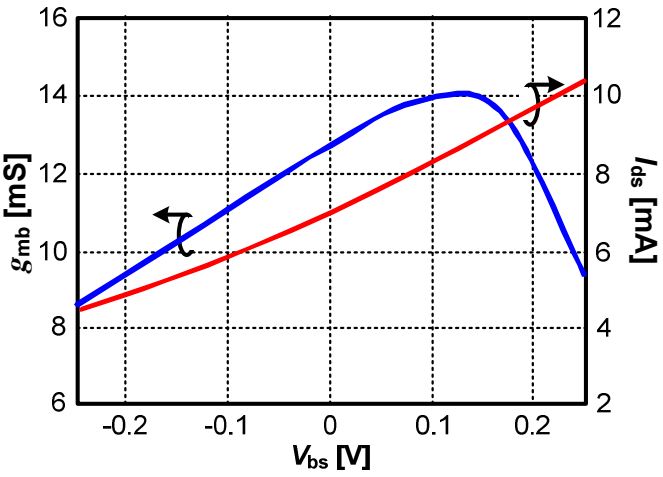


Figure 6.10 Simulation results of $g_{mb}$, $I_{ds}$ vs. $V_{bs}$.

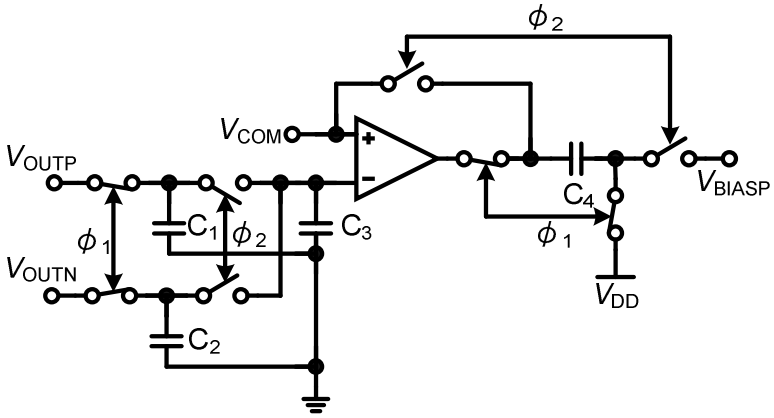


Figure 6.11 Feedback loop for CMFB.

current is changed almost linearly; it means the proposed current control method can be applicable.

### 6.3.4 Body Voltage Controlled CMFB

The proposed amplifier utilizes body voltage control of the PMOS input transistors for CMFB. The structure of the feedback loop for CMFB is depicted in Figure 6.11. $V_{OUTP}$ and $V_{OUTN}$ in the feedback loop are connected to the amplifier's output as shown in Figure 6.7. The $C_1$ and $C_2$ charge the output voltages of the amplifier. After that, the feedback loop averages the output voltages using $C_3$ and senses the difference from $V_{COM}$. Finally, the output of the feedback loop is applied to the body of the PMOS input transistors in the amplifier. By this operation, the proposed amplifier realizes the CMFB function without a current source transistor.

## 6.4 Simulation and Experimental Results

The proposed ADC was designed in 1P9M 90 nm CMOS technology. The ADC operates with only 1.2 V supply voltage. The simulation result of the ENOB vs. sampling frequency at 50 MHz input signal is provided in Figure 6.12. The ENOB keeps above 11.4 bit until 400 MHz sampling frequency. Above 500 MHz, the performance of the ADC degrades. At that point, the ENOB is 11.3 bit. Figure 6.13 provides the simulation result of the ENOB vs. the input signal frequency at the sampling frequency of 400 MHz. The ENOB degrades from 11.5 bit at the input frequency is 50 MHz, with increasing input signal frequency. When the input frequency becomes Nyquist frequency, the ENOB degrades to 10.8 bit.

Figure 6.14 and Figure 6.15 show DNL / INL measurement results at 300 MS/s and 100 kHz input. The DNL / INL results are +1.4 LSB / -1 LSB and +3.1 LSB / -4.5 LSB, respectively. The DNL results excluding of end-sides are improved to +1 LSB / -0.7 LSB. This is reasonable because those end-sides are usually not used in the ADC operation. Measured

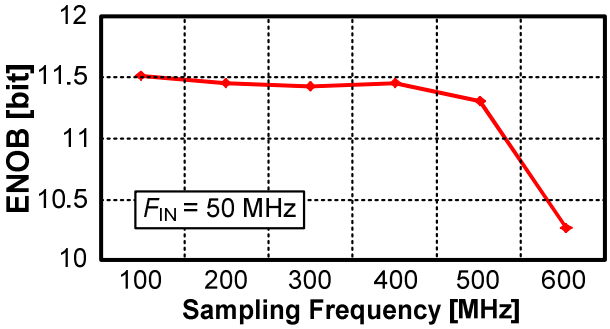


Figure 6.12 Simulation result of ENOB vs. sampling frequency ($F_{IN}$ = 50 MHz).

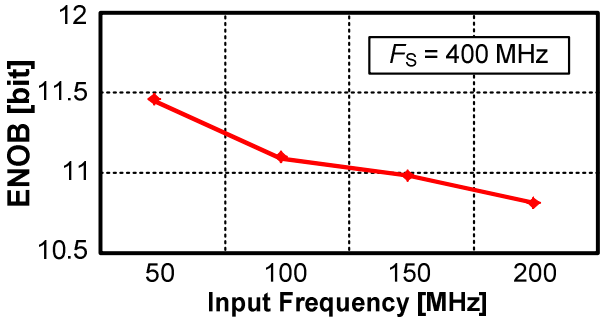


Figure 6.13 Simulation result of ENOB vs. input frequency ($F_S$ = 400 MHz).

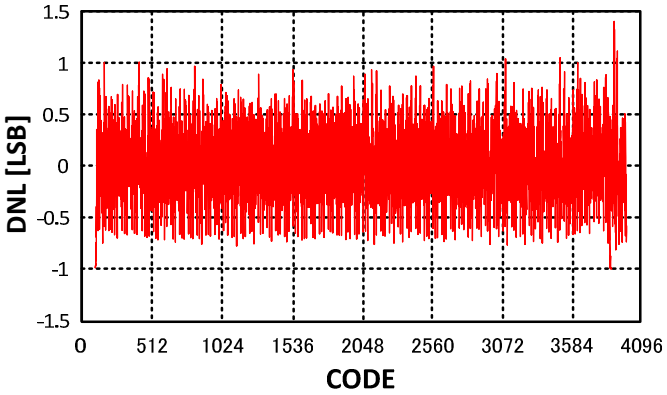


Figure 6.14 DNL measurement results at 300 MS/s and 100 kHz input.

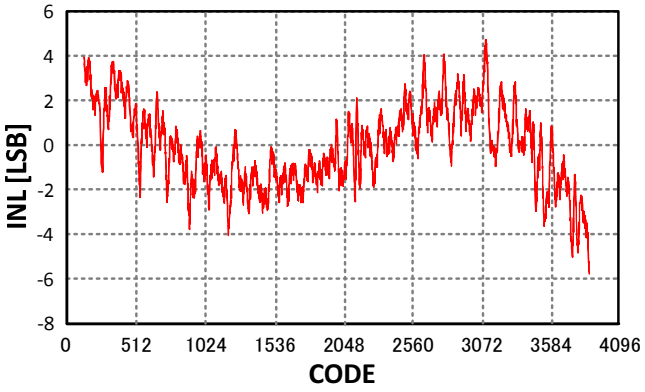


Figure 6.15 INL measurement results at 300 MS/s and 100 kHz input.

output spectrum at 300 MHz sampling frequency and 100 kHz input frequency are given in Figure 6.16. At the mentioned setting, the ENOB becomes 10 bit.

Usually, ADC converts the input signal until half of the sampling frequency (Nyquist frequency) by Shannon's Nyquist theorem. In the simulation, the proposed ADC can convert the Nyquist input frequency although there is a little performance degradation. However, in the measurement, ADC's performance is degraded drastically with increase of the input signal frequency. Also, the INL results show 3rd harmonic error which causes performance degradation as shown in Figure 6.15. The performance degradation of the measurement

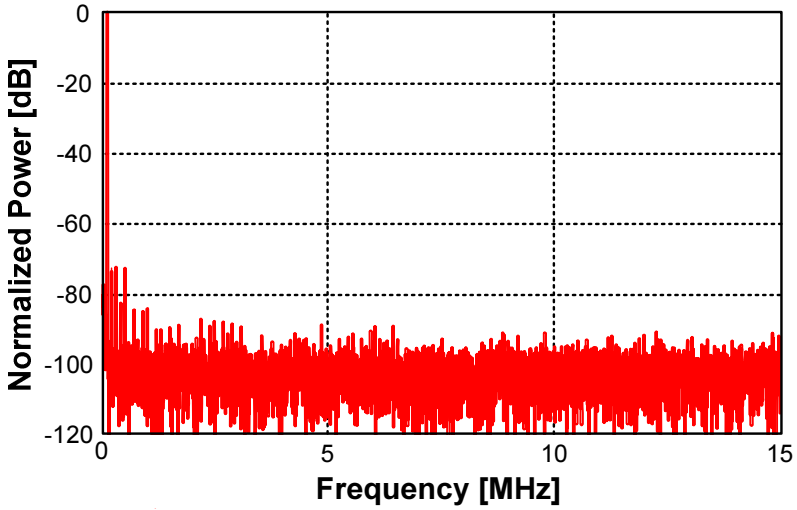


Figure 6.16 Measured output spectrum at 300 MS/s and 100 kHz input.

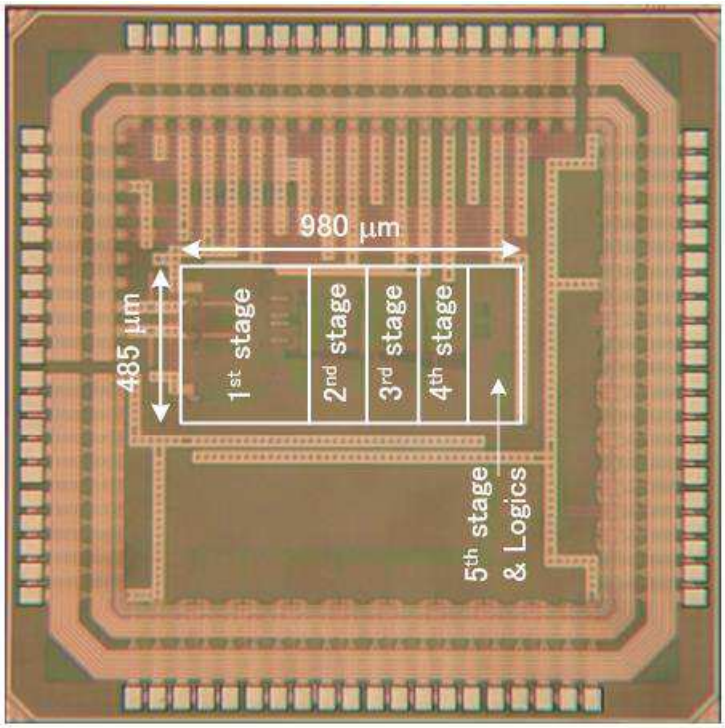


Figure 6.17 Chip photo.

results is due to the parasitic components (capacitance, inductance, and resistance) in the package and the PCB test board. These parasitic components cause input / reference voltage ringing which is reason of settling error and signal distortion. Because the proposed ADC does not incorporate any buffers in the input and the reference nodes, the parasitic components affect the ADC performance directly. It is expected that the measurement results will be improved if the ADC input driver and the reference drivers are inserted in the ADC core. The performance degradation by the parasitic components is confirmed by the simulation; therefore, the expectation is reasonable. The simulation results are shown in the following sub-chapter. Figure 6.17 shows the proposed ADC's chip photo. The occupied core area is 0.48 $mm^2$ including clock timing control circuit and reference lines.

### 6.4.1 Effect of Parasitic Components

As described in the previous paragraph, the proposed ADC does not work properly in high frequency input signal due to the parasitic components. Figure 6.18 depicts those parasitic components. There are two types of the parasitic components, one is come from package and another one is come from PCB test board. Among the two parasitic sources, the package is more crucial to the ADC's performance because the parasitic components from the PCB test board can be reduced by careful PCB test board layout and short signal connection line by the optimized component location. Therefore, the effect of inductors (red colored inductors in Figure 6.18) from the package is examined by the simulation. Also, decoupling capacitors (red colored capacitors in Figure 6.18) are considered simulation because they are inserted in the proposed 12-bit interpolated pipeline ADC.

The simulation is performed by ideal model of 10-bit interpolated pipeline ADC to figure out the effect of the inductor accurately. Although the ideal model is utilized, the structure of the ADC is completely same as the actual transistor model. Also, the

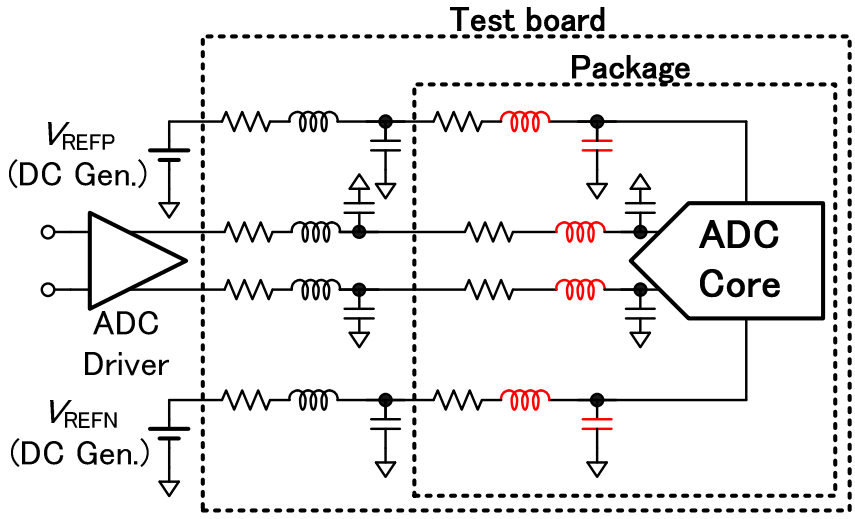


Figure 6.18 Parasitic components in package and PCB test board.

Table 6.2 Effect of parasitic inductance.

| $F_S$ [MS/s] / $F_{IN}$ [MHz] | ENOB [bit] | |
|---|---|---|
| | Without Inductor | With Inductor |
| 320 / 1 | 11.7 | 10.4 |
| 320 / 160 | 10.9 | 8.5 |

on-resistance of the switch in the CDAC is considered for the accurate simulation results. There is no transient noise in the simulation; therefore, the performance degradation is almost caused by the parasitic inductor. The parasitic inductance is assigned as 2 nH which is came from the parasitic components modeling. Also, decoupling capacitance in the reference nodes is assigned as 500 pF to realize the same environment of the actual measurement. Actually, the structure of the parasitic components is more complicate. However, only inductors in the package are considered for simplicity. This is reasonable because the inductors in package are the main reason of the performance degradation.

Table 6.2 shows the simulation results with / without the parasitic inductor. The sampling frequency is 320 MS/s which is almost same as the measurement results in Figure 6.16. Two input frequencies, 1 MHz (DC) and 160 MHz (Nyquist) are examined because the effect of inductor depends on the frequency. When the input signal is 1 MHz, ENOB is degraded from 11.7 bit to 10.4 bit due to the parasitic inductor. Even though the input frequency is very slow, high frequency sampling frequency causes signal ringing in the reference node and it degrades ENOB. When the input signal frequency is increased to 160 MHz (Nyquist frequency), the ENOB is degraded from 10.9 bit to 8.5 bit by the parasitic inductor. This is because the ringing is also occurred at the input node due to the high frequency input signal. In the measurement, the ENOB shows about 7 bit at 320 MS/s and 160 MHz input frequency.

Figure 6.19 shows the ringing at the input and the reference node during the simulation (320 MS/s and 160 MHz input). If there is no inductor, each signal draws clear sine-wave / DC reference voltages. However, as shown in Figure 6.19, the reference signals are varied with clock signal. For the reference signals, direction of voltage variation is opposite between $V_{REFP}$ and $V_{REFN}$ because the current flowing direction is opposite. At that time, this variation is just shown as the reference range variation On the other hand, for the input signals, the ringing is very crucial because it causes the sampling error no matter what the ringing direction. That is the reason of the large performance degradation with high frequency input signal.

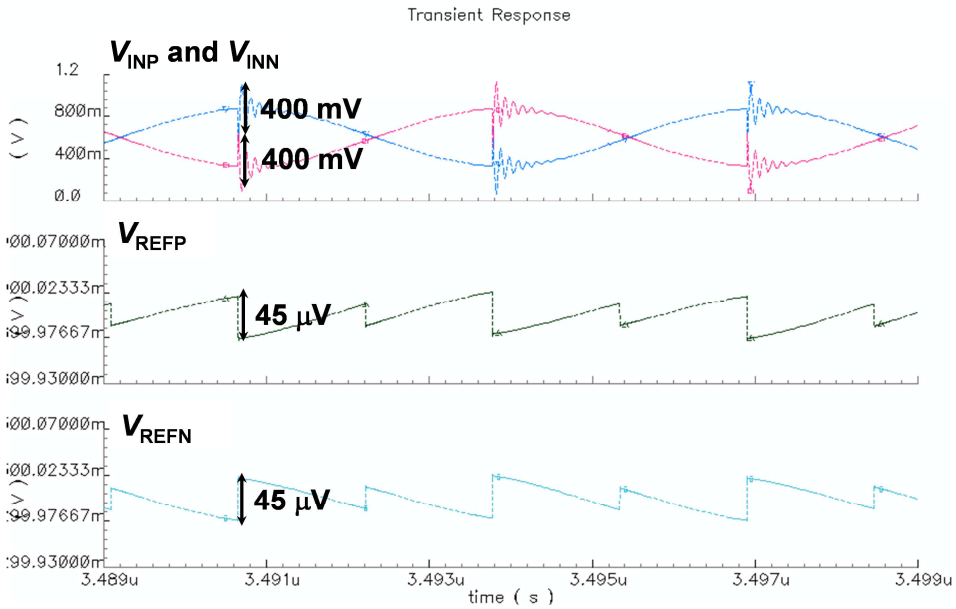


Figure 6.19 Effect of parasitic inductor at 320 MS/s and 160 MHz input.

As shown in Table 6.2 and Figure 6.19, the parasitic inductor causes severe problem. There is a large difference between the simulation results and the measurement results because the parasitic components have more complicate structure and the PCB test board is customized to suppress the parasitic components' effect. The most effective method to eliminate the effect of the parasitic components is using bare chip (no package for the ADC core) for the measurement; however, it increases test cost a lot due to the special wiring between bare chip and PCB test board. Another method to reduce the effect of the parasitic components is inserting buffer in the ADC core to separate the ADC's input from the parasitic components. This is also very effective. However, design of high-performance buffer is another challenge of circuit design.

### 6.4.2 Performance Table

Table 6.3 shows the performance table of the proposed body voltage controlled amplifier. The power consumption and the settling time satisfy the requirement of a 12-bit 400 MS/s interpolated pipeline ADC. The proposed amplifier achieves 40% reduction of the power consumption in comparison with folded cascode amplifier. Furthermore, in comparison with telescopic amplifier, the output signal swing is increased by 12.5%. Considering the output signal swing range for telescopic amplifier, the power consumption would increase to acquire the same SNR with the proposed amplifier. It means that the power consumption can be reduced by 58% with the use of the proposed amplifier. The results indicate that the proposed amplifier is a good candidate to achieve the ADC's target specification even though it utilizes the body voltage control. The performance comparison data between the proposed 12-bit interpolated pipeline ADC and recently published 12-bit high-speed ADCs are given in Table

Table 6.3 Performance table of proposed amplifier.

| Topology | Body voltage control |
|---|---|
| DC gain [dB] | 45 |
| Power consumption [mW] | 15.6<br>(↓ 40 % from folded cascode amp) |
| Settling time [ps] | 500 |
| Output swing range [$mV_{pp}$] | 600<br>(↑ 12.5 % from telescopic amp) |

6.4. The values in this table are all measurement data. There are two FoM in Table 6.4. Those FoM are explained in following paragraph. It can be observed that [6.30] and [6.31] achieve very high-speed conversion frequency. However, the power consumptions are also very high. The work in [6.10] shows a good balance in the sampling frequency and the power consumption. The ADC in [6.10] utilizes 4-times interleaving. It means that one ADC channel works at 200 MHz frequency. Therefore, in comparison of one channel ADC in [6.10], the proposed 12-bit interpolated pipeline ADC has an advantage of the operating speed. Table 6.5 organizes more specific information on calibration and special circuits. As written in Table 6.4 and Table 6.5, other ADCs utilize a high supply voltage and a specialized S/H circuit to acquire input signal without distortion. Unfortunately, there is a little information about the calibration technique. However, it is assumed that large amount of calibration is used in the ADCs by chapter 2.6. As written in the ENOB row in Table 6.4, the results of the proposed 12-bit interpolated pipeline ADC are measured with the low input signal frequency. Therefore, the measured condition has to be considered when checks the Table 6.4.

Even though the ADC cannot convert high frequency input signal properly, the ADC has several advantages in comparison of the other ADCs. For example, the linearity characteristic of the proposed 12-bit interpolated pipeline ADC is highest level in the table. It is very remarkable achievement because other ADCs utilize high supply voltage, special process, and specialized S/H circuit to achieve the linearity level of the 12-bit resolution. In contrast to other ADCs, the proposed 12-bit interpolated pipeline ADC does not utilize any special process or high supply voltage. Furthermore, the proposed 12-bit interpolated pipeline ADC does not utilize any MDAC stage linearity calibration. Therefore, the proposed 12-bit interpolated pipeline ADC has high versatility than others. By the high linearity achievement, the proposed 12-bit interpolated pipeline ADC's FoM also has competition with low frequency input signal. Although the ADC has problem at the high frequency input signal, it is useful for low frequency signal A/D conversion application, such as the power supply adjustment system. If the proposed 12-bit interpolated pipeline ADC is used such kind of application, the validity of usage has to be examined in comparison of other ADC topologies. Also, if the problems related with the parasitic components are solved, the proposed 12-bit

Table 6.4 Recently Published 12-bit ADCs.

| | This work | [6.10] | [6.30] | [6.31] |
|---|---|---|---|---|
| Resolution [bit] | 12 | 12 | 12 | 12 |
| $F_S$ [MS/s] | 300 | 800 | 1000 | 3000 |
| $V_{DD}$ [V] | 1.2 | 1 / 2.5 | 1.8 / 3.3 | 1 / 2.5 |
| Power [mW] | 60 | 105 | 575 | 500 |
| ENOB [bit] | 9.96 (100 kHz) | 9.5 | 9.5 (by SNR) | 7.8 |
| $FoM_W$ [pJ/conv.] | 0.2 | 0.18 | 0.79 | 0.75 |
| $FoM_S$ [dB] | 156 | 155 | 148 | 154 |
| Technology [nm] | 90 | 40 | 180 (SiGe) | 40 (Thin-Oxide) |
| Core area [mm$^2$] | 0.48 | 0.88 | 2.35 | 0.4 |
| Linearity compensation | No | Yes | Yes | Yes |
| Interleave | No | 4-times | No | 2-times |

Table 6.5 Additional information on calibration and special circuits.

| Reference | Calibration and special circuit detail |
|---|---|
| [6.10] | • 2.5-V buffer and sampling block (Special input)<br>• Offset of amplifier, Channel mismatch (On-chip)<br>• No detailed Information<br>(Only amplifier's offset calibration is described) |
| [6.30] | • 1.8-V / 3.3-V large supply voltage<br>• Channel mismatch (Off-chip)<br>• No detailed information |
| [6.31] | • 2.5-V special sampling block<br>• Channel mismatch (Off-chip)<br>• No detailed information |

interpolated pipeline ADC can convert high frequency input signal and it can compete with other ADCs in high speed applications.

In Table 6.4, there are two FoM items, $FoM_W$ and $FoM_S$. Each FoM has different priority to express the ADC's performance. For example, $FoM_W$ has priority for the ADC's power consumption. $FoM_W$ is written as

$$\mathrm{FoM_W} = \frac{\boldsymbol{P}_\mathrm{D}}{2^{\boldsymbol{ENOB}} \times \boldsymbol{F}_\mathrm{S}}. \tag{6.5}$$

As described in (6.5), the smaller FoMW means that the ADC has better power efficiency.

Figure 6.20 shows state-of-the-art ADCs in $F_S$ vs. FoMW [6.32]. The proposed 12-bit interpolated pipeline ADC and the references in Table 6.4 ([6.10], [6.30] - [6.31]) are plotted. In Figure 6.20, the proposed 12-bit interpolated pipeline ADC shows better FoMW than [6.30] - [6.31] and almost same value with [6.10]. However, the proposed 12-bit interpolated pipeline ADC has slower sampling frequency than other ADCs. Therefore, solving the parasitic components problem and increasing operating speed are necessary to the proposed 12-bit interpolated pipeline ADC.

As shown in (6.4), FoMW is focusing on the power consumption. It is a good guideline for the low-power low-resolution ADCs' performance comparison; however, some ADCs which have high-speed operation, high-resolution and high power consumption have disadvantage in comparison of using FoMW. Another ADC performance comparison parameter, FoMS is usually used for such kind of the ADCs. The FoMS is defined as below,

$$\mathrm{FoM_S} = \boldsymbol{SNDR} + 10\log\left(\frac{\boldsymbol{BW}}{\boldsymbol{P_D}}\right). \tag{6.6}$$

It is recognized that the FoMS concentrates the SNDR and the ration of BW and power consumption. Therefore, the FoMS is usually used for hig-resolution high-speed ADC comparison. Figure 6.21 shows state-of-the-art ADCs in $F_S$ vs. FoMS [6.32]. In Figure 6.21, almost same conclusion in the previous paragraph can be derived, which means the proposed 12-bit interpolated pipeline ADC has a good FoMS; however, sampling frequency needs to be improved.

Through Figure 6.20 and Figure 6.21, the performance of the proposed 12-bit

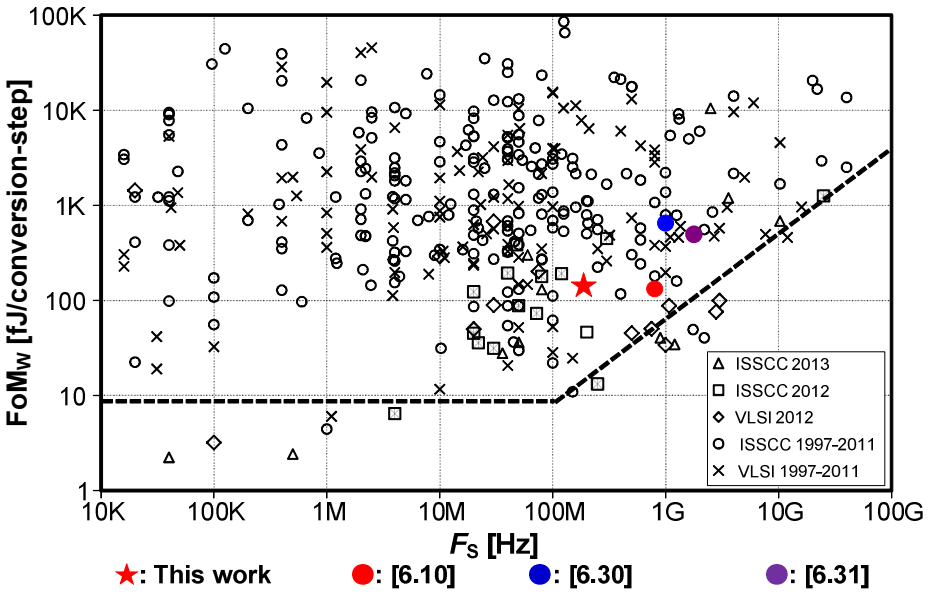


Figure 6.20 State-of-the-art ADCs in $F_S$ vs. FoMW [6.32].

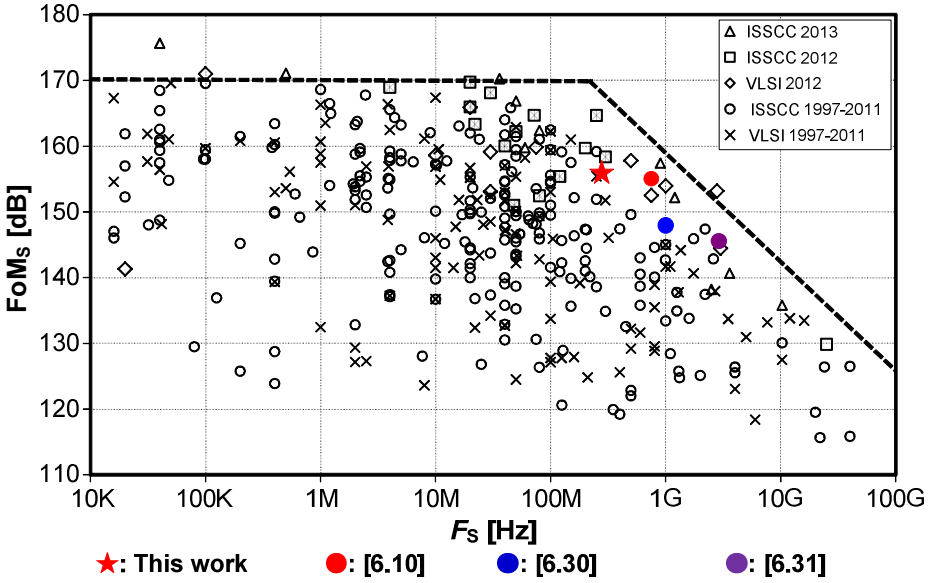


Figure 6.21 State-of-the-art ADCs in $F_S$ vs. $FoM_S$ [6.32].

interpolated pipeline ADC is compared with state-of-the-art ADCs. Because the proposed ADC has achieved good performance in the value of $FoM_W$ and $FoM_S$, it can say that the ADC has enough high potential to compete with other ADCs. To become one of the top-level ADCs, increase of the sampling frequency and the input frequency are necessary. The sampling frequency can be increased by the interleaving as well as other ADCs. Also, the input frequency is improved by suppressing the effect of the parasitic components as described in chapter 6.4.1.

## 6.5 Conclusion

In this chapter, a 12-bit interpolated pipeline ADC with body voltage controlled amplifier is demonstrated. Even though the interpolation technique relaxes the DC gain requirement of the amplifier, a relatively high gain amplifier with feedback loop is required to obtain the required linearity characteristic. The proposed body voltage controlled amplifier achieves the required DC gain (45 dB) with small power consumption and large signal swing range. The amplifier's current biasing and CMFB are realized with body voltage control feedback loops. The control range of the current is enough for the amplifier's operation. The 12-bit interpolated pipeline ADC using proposed amplifier shows a good performance in the simulation, such as the ENOB of 10.8 bit at 400 MS/s for Nyquist input frequency. The DNL / INL measurement results are +1 / -0.7 and +3.1 / -4.5 LSB, respectively. Also, the measured FFT spectrum at 300 MS/s and 100 kHz input shows 10 bit of ENOB without MDAC linearity calibration and high supply voltage. The 12-bit interpolated pipeline ADC's performance at high frequency input signal is degraded due to the parasitic components in the package and the PCB test board. Therefore, by solving the parasitic components problem, the proposed

12-bit interpolated pipeline ADC can become an attractive candidate for the high performance communication systems.

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# 7. Suitable Amplifier Topology in Interpolated Pipeline ADC

## 7.1 Introduction

In this thesis, two types of amplifier usages are introduced, the open-loop and the closed-loop. In the conventional pipeline ADC design, the realization of the accurate MDAC stage gain is one of the most important issues for the ADC design. Therefore, the MDAC stage is composed of high gain operational amplifier with capacitance feedback loop. On the other hand, accurate MDAC stage gain does not matter to the interpolated pipeline ADC. As a result, a low-gain open-loop amplifier can be incorporated to high resolution interpolated pipeline ADC, such as 10-bit resolution in [7.1]. Instead of the amplifier's gain, linearity of the amplifier becomes more crucial for the ADC design. However, for the realization of the 12-bit resolution, the interpolated pipeline ADC utilizes closed-loop amplifier because low-gain open-loop amplifier (for example, source degeneration amplifier) is not suitable to satisfy the linearity requirement, as shown in chapter 6. The 12-bit interpolated pipeline ADC with closed-loop amplifier achieves good performance; however, it makes a little confusing to choose the amplifier's feedback type for the interpolated pipeline ADC design.

In this chapter, the suitable amplifier's topology and feedback type are discussed in terms of the interpolated pipeline ADC's performance. Also, the 12-bit interpolated pipeline ADC using open-loop amplifier is also presented.

## 7.2 Open-loop and Closed-loop Amplifiers in Interpolated Pipeline ADC

The biggest merit of the interpolated pipeline ADC design is the realization of high-speed and high-resolution ADC using low-gain open-loop amplifier without calibration. This merit is already verified by the ADC demonstration in [7.1]. The problem is appeared when the ADC's target specification becomes higher than 10-bit.

The amplifier's topology in [7.1] is source degeneration amplifier. This is reasonable because the important characteristic of the amplifier in the interpolated pipeline ADC is the linearity not the gain. And the linearity requirement becomes severe with increase of the ADC's resolution. The linearity improvement of the source degeneration amplifier accompanies the increase of the power consumption. According to the analysis in chapter 5.5, the realization of the 10-bit ADC using the source degeneration amplifier is reasonable, such kind of 4 mW power consumption of the 4-bit 1$^{st}$ pipeline stage. However, the power consumption is increased drastically when the ADC's resolution becomes 12-bit, for example, 80 mW for 4-bit 1$^{st}$ pipeline stage and 20 mW for 5-bit 1$^{st}$ pipeline stage.

To satisfy the linearity requirement with reasonable power consumption for 12-bit interpolated pipeline ADC, a cascode amplifier with feedback loop is proposed in chapter 6. This looks like the merit of interpolated pipeline ADC design is disappeared. However, in

comparison of the conventional pipeline ADC, the interpolated pipeline ADC does not requires extremely high-gain op-amp, such as 80 dB gain. As described in chapter 1 and chapter 2, high-gain op-amp design in recent scaled technology is very difficult. And, calibration circuit to compensate the insufficient op-amp's gain accompanies other issues. In contrast, the interpolated pipeline ADC topology can realize 12-bit resolution ADC using about 45 dB gain cascode amplifier. The gain of 45-dB is not much difficult to realize in recent scaled technology. Therefore, the merit of the interpolated pipeline ADC is still effective.

There is another issue of closed-loop amplifier topology. To realize the high-resolution ADC, the offsets of the amplifiers in the interpolated pipeline ADC have to be calibrated. The open-loop amplifier's offset is cancelled smoothly during the ADC's operation without additional circuit, as shown in chapter 5.2.3.2. However, closed-loop amplifier cannot use the same offset cancellation technique. The 12-bit interpolated pipeline ADC in chapter 6, DAC is incorporated for the amplifier's offset calibration. Even though the DAC circuit is added, the amplifier's offset calibration does not affect the ADC's operation. Also, only 120 cycles of calibration time is enough to reduce the amplifier's input referred offset less than 1 LSB. Therefore, the interpolated pipeline ADC using cascode amplifier with feedback loop and offset calibration circuit is an attractive candidate for the target specification.

There are other issues of the open-loop and closed-loop amplifier for the interpolated pipeline ADC design. Table 7.1 organizes those issues, CDAC's gain degradation, amplifier's settling speed, and offset calibration method. In Table 7.1, $C_{load}$ means load capacitance of the amplifier and $C_{feedback}$ means capacitance in feedback loop. As explained in above paragraph, an open-loop has an advantage for simple offset calibration of the amplifier. For the CDAC's gain degradation issue, a closed-loop has a merit because the open-loop reduces the CDAC's gain due to the input parasitic capacitance of the amplifier. This issue is also explained in chapter 5.2.3.1. For the settling time, it is not difficult to imagine the open-loop amplifier has faster settling characteristic. As written in Table 7.1, the close-loop amplifier has not only the load capacitance but also feedback capacitance at the output node. In contrast, the open-loop

Table 7.1 Performance comparison of open-loop and closed-loop amplifier.

| | CDAC's gain | Settling | Offset calibration |
|---|---|---|---|
| Open-loop | Worse<br>(Reduced by parasitic capacitor of amplifier) | **Faster**<br>**(Only $C_{load}$)** | **Simple**<br>**(No additional circuit)** |
| Closed-loop | **Better**<br>**(No reduction)** | Slower<br>($C_{load}$ + $C_{feedback}$) | Complicate<br>(Additional Circuit needed) |

amplifier only has load capacitance; therefore, it has faster settling characteristic.

In conclusion, the open-loop has more merits than closed-loop for the amplifier's topology. It means that if the amplifier's linearity requirement is satisfied, it is better to utilize the open-loop amplifier for any ADC resolution.

## 7.3 A 12-bit interpolated pipeline ADC using $g_m$-Cell

As shown in Table 7.1, the open-loop amplifier gives more merits than the closed-loop for the interpolated pipeline ADC design. The determination of two amplifier topologies is based on the linearity of the amplifier. It means that if the amplifier has enough linearity, the interpolated pipeline ADC can be designed with open-loop amplifier even though ADC's resolution is higher than 10 bit.

In this sub-chapter, a 12-bit, 200 MS/s, and 600 MHz input signal frequency ADC is proposed. The actual input signal frequency is around 1 MHz; however, the input signal is transferred with 600 MHz carrier signal by the system specification. Therefore, the ADC has to be designed that it can cope with 600 MHz input signal frequency even though its sampling frequency is 200 MHz. The ADC in this sub-chapter has almost same structure in chapter 6. However, the ADC in this sub-chapter utilizes open-loop amplifier topology for the 1st MDAC stage. It becomes possible by use of the $g_m$-cell [7.2], which has good linearity characteristic even though open-loop usage. By using the open-loop amplifier topology, the offset cancellation of the amplifier becomes very simple as described in chapter 5.2.3.2. Also, settling characteristic of the amplifier is improved by removal of feedback capacitance. The CDAC's gain is reduced by the open-loop amplifier; however, the gain is not a severe problem in the interpolated pipeline ADC.

In chapter 7.3.1, the proposed ADC's architecture is described. After that, the $g_m$-cell is introduced in chapter 7.3.2 which allows the open-loop topology by its high linearity characteristic. And, in chapter 7.3.3, DC / AC simulation results of the proposed ADC are shown.

### 7.3.1 ADC Architecture

The proposed ADC in this sub-chapter is based on the 12-bit interpolated pipeline ADC in Chapter 6. However, the body voltage controlled amplifier in the 1st stage is substituted to the $g_m$-cell which can achieve enough high linearity for the 12-bit interpolated pipeline ADC without feedback loop. Figure 7.1 depicts the block diagram of the proposed ADC. By introducing the $g_m$-cell, the merits of open-loop amplifier can be applicable to the ADC in this sub-chapter. It means that there is no calibration circuit for amplifier's offset. Also, the proposed 12-bit interpolated pipeline ADC using $g_m$-cell improves sampling timing in the 1st stage because the ADC has to convert 600 MHz input signal. Those improvements are

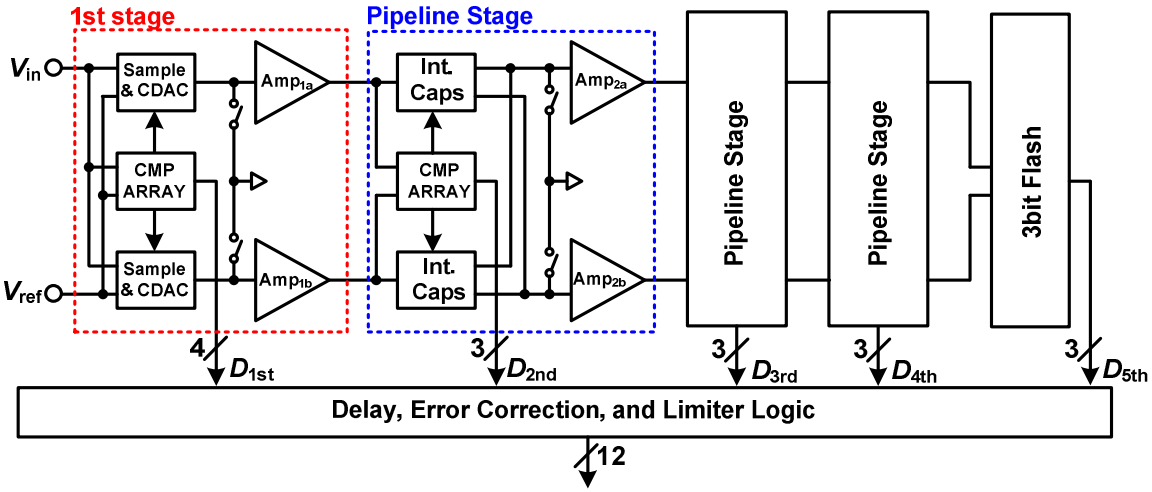


Figure 7.1 Block diagram of 12-bit interpolated pipeline ADC using $g_m$-cell.

omitted in Figure 7.1. Most of circuits in the proposed 12-bit interpolated pipeline ADC using $g_m$-cell are introduced in chapter 5 and chapter 6. Therefore, only the $g_m$-cell is explained in the following chapter.

### 7.3.2 $g_m$-Cell

Figure 7.2 shows the schematic of the $g_m$-cell. The topology of the $g_m$-cell is much resembled to the cascode current mirror circuit with basic $g_m$-cell. The mirrored current from $M_3$ to $M_7$ generates output. Figure 7.3 shows the small signal model of the $g_m$-cell. The number of $g_m$ is matched to the number of transistor in Figure 7.2. In Figure 7.3, $R_o$ means drain resistance of the $M_1$ and $M_5$. The gain of the $g_m$-cell can be calculated as below,

$$G = M\frac{R_L}{R_s}\frac{1}{1+\dfrac{1}{g_{m3}R_o}+\dfrac{1}{g_{m1}R_s g_{m3}R_o}}. \tag{7.1}$$

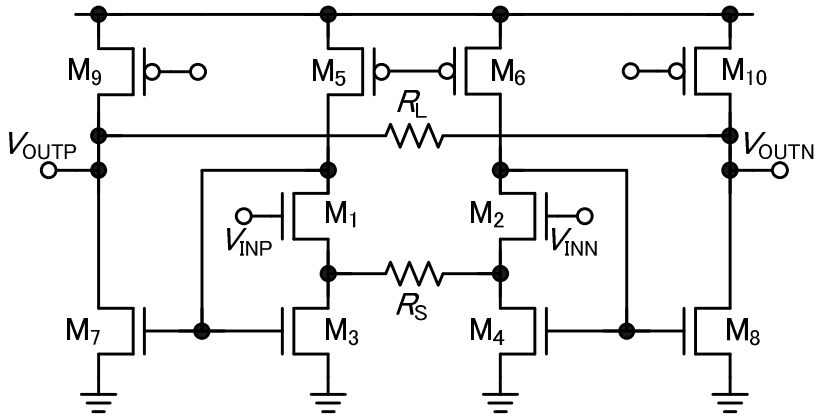


Figure 7.2 Schematic of $g_m$-cell.

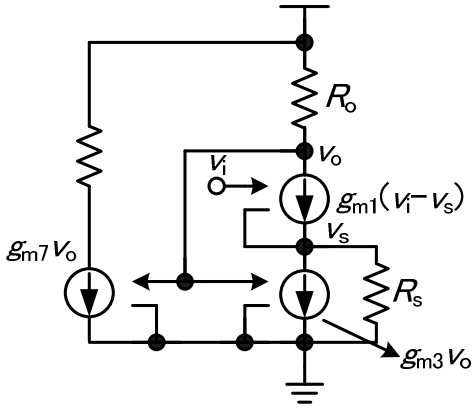


Figure 7.3 Small signal model of $g_m$-cell.

In (7.1), the $M$ means ratio of current mirroring between $M_3$ and $M_7$. Also, $g_{m3}R_o$ is usually much larger than 1; therefore, the second term in the denominator can be ignored. And, the effect of $g_{m1}R_s$ in the third term of the denominator is usually smaller than 1; however, the effect of small $g_{m1}R_s$ is eased off by $g_{m3}R_o$. Therefore, the gain of $g_m$-cell is almost determined by $R_L$ and $R_s$ and it can achieve high linearity even though the $g_{m1}$ is small.

The $g_m$-cell in the proposed 12-bit interpolated pipeline ADC in this sub-chapter is designed with 4-times gain. Figure 7.4 shows the ENOB vs. the $a_3/a_1$ for the interpolated pipeline ADC as shown in chapter 6.2.2. There are three amplifier types are shown in Figure 7.4, such as source degeneration, body voltage control, and $g_m$-cell. According to Figure 7.4, the proposed $g_m$-cell shows about 0.35 of $a_3/a_1$ in +/- 75 mV input range, which is the actual circuit operation range. It means that the $g_m$-cell achieves almost 0.1 bit ENOB degradation. This is better performance than the cascode amplifier with closed feedback loop, in which the $a_3/a_1$ is about 0.4. The results show that the $g_m$-cell is very attractive for the interpolated

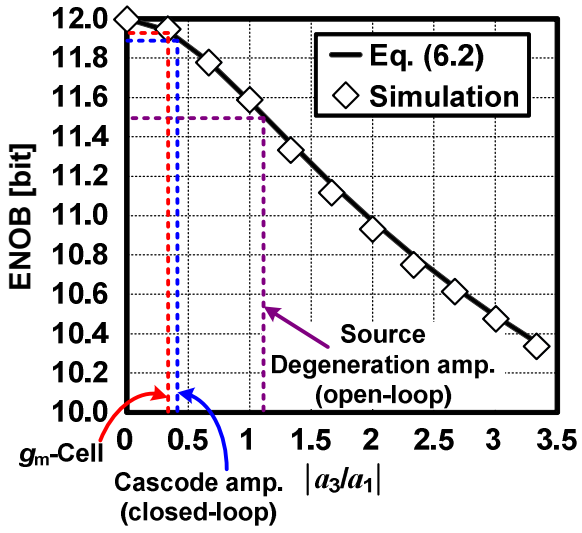


Figure 7.4 ENOB vs. amplifier's linearity with 3 amplifier topologies.

pipeline ADC.

### 7.3.3 Simulation Results

Figure 7.5 and Figure 7.6 depict the DNL and the INL simulation results. The DNL and the INL is +0.5 / -0.5 and +0.85 / -0.9, respectively. Figure 7.7 shows simulation results of FFT spectrum at 200 MS/s and 601 MHz input signal. In Figure 7.7, input signal frequency indicates around 1 MHz, not 601 MHz. This is because the calculation of the FFT (and

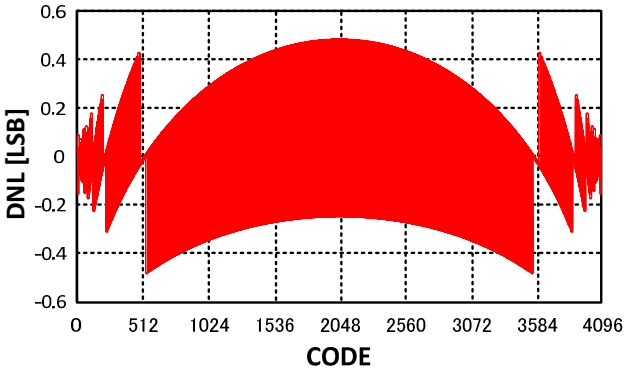


Figure 7.5 DNL simulation results.

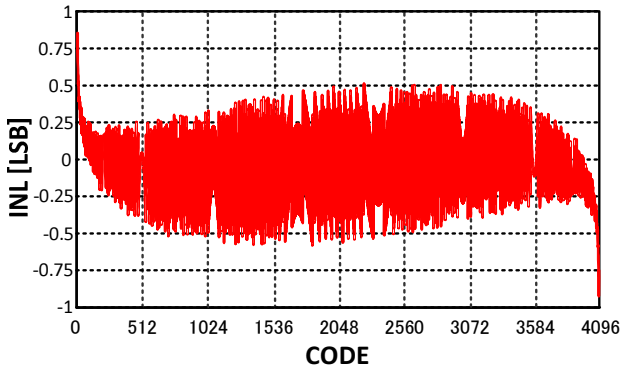


Figure 7.6 INL simulation results.

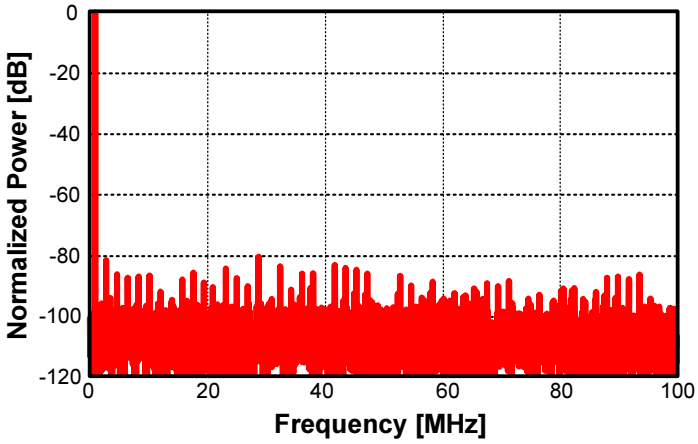


Figure 7.7 Simulation results of FFT spectrum at 200 MS/s and 601 MHz input.

Table 7.2 Simulation results at 200 MS/s and 601 MHz input.

| SNR [dB] | SFDR [dB] | THD [dB] | SNDR [dB] | ENOB [Bit] |
|---|---|---|---|---|
| 70.46 | 82.67 | -81.81 | 70.16 | 11.36 |

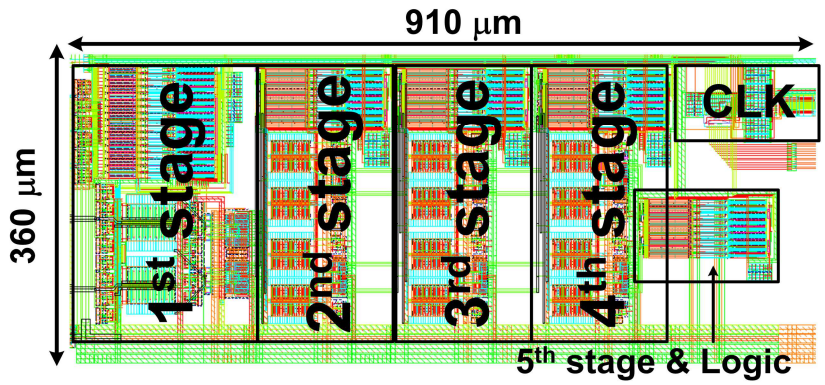


Figure 7.8 ADC core layout.

coherent frequency) is performed using 1 MHz frequency. In the simulation, the input signal is combined with 600 MHz and the actual input signal of the ADC is 601 MHz. Table 7.2 shows more information of the simulation results. The proposed 12-bit interpolated pipeline ADC using $g_m$-cell achieves 11.36 bit of the ENOB even though the input frequency is 601 MHz. Figure 7.8 shows ADC core layout including clock timing control circuit. The proposed 12-bit interpolated pipeline ADC using $g_m$-cell is designed by 1P8M 65 nm CMOS technology. The occupied core size is 0.33 $mm^2$. In the SoC, the ADC input driver will be included to suppress the performance degradation as shown in the 12-bit interpolated pipeline ADC in chapter 6.

## 7.4 Comparison of Amplifier Topology

In this thesis, there are three amplifier topologies has been proposed for the interpolated pipeline ADC design. Those topologies are source degeneration, cascode (body voltage control), and $g_m$-cell. In chapter 7.2, comparison of open-loop and closed-loop is examined. In this sub-chapter, performance of three amplifier topologies is verified to help choosing the amplifier topology for the interpolated pipeline ADC design.

Table 7.3 shows performance comparison of the three amplifier topologies. The linearity and the power consumption in Table 7.3 are the simulation results. Also, the results of $g_m$-cell are all simulation results because the 12-bit interpolated pipeline ADC using $g_m$-cell has not been delivered yet. Even though the body voltage controlled amplifier and $g_m$-cell is designed for 12-bit ADC, the technology of two circuits are different. It may cause the performance difference between two circuits.

For the below 10-bit resolution ADC, it is not to concern the amplifier topology. Since the source degeneration amplifier with open-loop can achieve the linearity requirement. On the other hand, for the higher than 10-bit resolution ADC, $g_m$-cell is better choice than body voltage controlled amplifier because open-loop amplifier has more advantages than closed-loop as explained in chapter 7.2. The source degeneration amplifier is difficult to apply higher than 10-bit resolution due to its limited linearity characteristic. In power per speed product, source degeneration amplifier shows best result due to lower resolution of the ADC. For 12-bit resolution, $g_m$-cell shows better performance because the body voltage controlled amplifier's measured operation speed is lower than expectation. Among the amplifiers, the $g_m$-cell has widest output swing range because it has only NMOS input. It means if the $g_m$-cell is designed by CMOS input, the power per speed product can be improved. In conclusion, among the three amplifier topologies, the source degeneration amplifier is suitable for below 10-bit ADC resolution and the $g_m$-cell is suitable for higher than 10-bit

Table 7.3 Comparison of amplifier topologies.

| | Source Degeneration | Cascode (Body voltage control) | $g_m$-cell |
|---|---|---|---|
| Topology | Open-loop | Closed-loop | Open-loop |
| Technology and $V_{DD}$ | 1P9M 90 nm, 1.2 V | 1P9M 90 nm, 1.2 V | 1P8M 65 nm, 1.2 V |
| Practical ADC resolution [bit] | 8 ~ 10 | 11 ~ 14 | 11 ~ 14 |
| ADC operation frequency [MS/s] | 320 | 300 | 200 |
| Linearity ($a_3/a_1$) | 1 @ X3 gain | 0.6 @ X4 gain | 0.4 @ X4 gain |
| Offset calibration | Cancelled in operation | Additional DAC needed | Cancelled in operation |
| Power per speed [mA/MHz] | 0.011 (320 MHz) | 0.037 (300 MHz) | 0.023 (200 MHz) |
| Required voltage headroom | 4- $V_{DS}$ (CMOS input) | 4- $V_{DS}$ (CMOS input) | 3- $V_{DS}$ (NMOS input) |

ADC resolution.

## 7.5 Suitable Amplifier Topology for Interpolated Pipeline ADC design

There are two topologies for amplifier is introduced, open-loop and closed-loop. Also, three types of the amplifiers are incorporated for interpolated pipeline ADC design. At this point, organization of the suitable topology for interpolated pipeline ADC design is necessary.

The merit of interpolated pipeline ADC is a high-resolution and high-speed ADC with low-gain open-loop amplifier can be designed without MDAC calibration. The issues to choose the amplifier topology are the linearity requirement and the offset calibration method. In other words, better method to solve those issues is to select the suitable amplifier topology for the interpolated pipeline ADC design. The comparison in chapter 7.2 concludes that the open-loop amplifier is better than the closed-loop amplifier. And, in chapter 7.4, it is recognized that the source degeneration amplifier and the $g_m$-cell can cover below 10-bit and higher than 10-bit with open-loop topology, respectively.

## 7.6 Conclusion

In this chapter, a 12-bit interpolated pipeline ADC using $g_m$-cell is proposed. The $g_m$-cell has a good linearity characteristic, which can be used for higher than 10-bit resolution ADC. By introducing $g_m$-cell, the proposed 12-bit ADC is designed with open-loop amplifier. The proposed ADC is fabricated in 1P8M 65 nm CMOS technology. The ADC shows good simulation results. For example, DNL and INL simulation results are +0.5 / -0.5 and +0.85 / -0.9, respectively. Also, AC simulation result with 200 MS/s and 601 MHz input signal frequency achieves ENOB of 11.36 bit.

Also, performance comparison of the amplifiers and feedback topologies are organized. In comparison of open-loop and closed-loop, open-loop is selected as a better topology due to the amplifier's offset calibration and the settling speed although it has the CDAC's gain degradation problem. And, the source degeneration amplifier and $g_m$-cell are selected as a suitable topology for the below 10-bit resolution and higher than 10-bit resolution interpolated pipeline ADCs, respectively. This chapter suggests a useful guideline for interpolated pipeline ADC design.

## Reference

[7.1] M. Miyahara, H. Lee, D. Paik, and A. Matsuzawa, "A 10b 320 MS/s 40 mW Open-loop Interpolated Pipeline ADC," in *Dig. Symp. VLSI Circuits*, pp.126-127, Jun. 2011.

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# 8. Conclusion

## 8.1 Conclusion of Thesis

In this thesis, ADCs using interpolation technique are introduced. By the CMOS technology scaling, many impacts appear in the circuit design. Among those impacts, reduced supply voltage and transistor size benefit to the digital circuits such as low-power consumption, small core area, and high operation speed. However, the supply voltage scaling degrades the SNR characteristic of the ADC. Furthermore, reduced intrinsic gain of the transistor suffers the ADCs using high gain amplifiers. Chapter 1 introduced the ADC development under the recent scaled technology. Also, the applications of the high-speed and high-resolution ADCs have been introduced with system level block diagram. After that, the problems of the recent scaled technology were described with graphs. And chapter 1 was concluded with research purpose and the thesis composition.

Chapter 2 introduced interpolation techniques which is the key-technique of the ADCs in this research. The interpolation means generating a new signal by weight control of two signals (voltage or current). By introducing the interpolation technique, circuit components can be reduced, such as S/H circuits and pre-amplifiers. Also, the reference selection between stages in the multi-stage ADC and the A/D comparison in the sub-ADC are realized without reference voltage. These characteristics bring many advantages to the multi-stage ADCs. In chapter 2, the principle and the basic operation of the interpolation have been introduced. Also, the characteristics, such as merit and demerit of interpolation technique were described with examples. The interpolation can be realized with several methods, such as resistive interpolation, capacitive interpolation, and gate-weighted interpolation. Those circuit implementation examples were also shown. The chapter 2 included the realization of the interpolation in the multi-stage ADCs. Finally, the calibration techniques have been introduced. Those calibration techniques are used widely in recent developed high performance ADCs. To understand recent ADC development trend, principle, examples, and pros and cons of the calibration techniques were analyzed.

In chapter 3, design of 6-bit subranging ADC using CDAC and gate-weighted interpolation has been introduced. By virtue of the interpolation, the signal consistence of the coarse to fine stage is adjusted automatically. It means the subranging ADC does not need to care of the reference range adjustment; therefore, the merit of CDAC is fully exhibited. The interpolation can be realized with CDAC and RDAC. The comparison of the CDAC and RDAC were analyzed in speed, power consumption, and noise characteristic. By those analysis, it was cleared that the CDAC has better performance than the RDAC. After that, the whole ADC architecture and operations were explained. Also, the gate-weighted interpolation technique and offset calibration technique were described. Especially, the mismatch of the

CDAC and the effect of the common-mode input level to the offset calibration in gate-weighted interpolation were analyzed and examined. The ADC in this chapter has been fabricated in a 90 nm CMOS technology. It achieved the DNL +0.6 / -0.6 LSB and the INL of +0.8 / -0.6 LSB. It also achieved FoM of 250 fJ/conv. which is the lowest one when the ADC was demonstrated.

Chapter 4 introduced another subranging ADC using one differential signal and two reference voltages. The subranging ADC in chapter 3 demonstrated good performance, however, it has a drawback of using two CDACs for the interpolation. Those CDACs occupy large area and increase the ADC input driver's performance requirements. To improve the performance of the subranging ADC using two CDACs, a new interpolation method has been proposed. The proposed interpolation method uses only one differential signal, which means that it needs only one CDAC. Instead of another differential signal, the proposed new interpolation uses two reference voltages. The subranging ADC using the proposed new interpolation technique was designed by 1P9M 90 nm CMOS technology. The ADC achieved +0.5 / -0.5 LSB of the DNL and the INL in the simulation. It also achieved more than 5.9 bit ENOB until 500 MS/s with Nyquist input frequency in simulation. In comparison with the subranging ADC in chapter 2, the ADC using proposed new interpolation technique achieved -38 % of sampling capacitance, -53 % of power consumption, and -43 % of core area. Even though the ADC's results were the simulation, it showed attractive performance. Therefore, it could become a good candidate for 6 to 7-bit, several hundred mega sampling speed applications.

In chapter 5, the design of interpolated pipeline ADC using low-gain open-loop amplifier has been introduced. By introducing the interpolation technique to the pipeline ADC, the ADC does not require high gain amplifier. Instead of gain, linearity of the amplifier became crucial. Also, the interpolated pipeline ADC has other design issues which are not exist in the conventional pipeline ADC. Those issues and solutions were discussed. Chapter 5 described the performance requirement for the amplifier, such as linearity and the input parasitic capacitance using the source degeneration amplifier. Also, the effects of the mismatch between two amplifiers were analyzed, for example, gain mismatch and bandwidth mismatch. And, the noise characteristic of the MDAC stage was analyzed. The ADC's sampling frequency and the ENOB degradation with amplifier's current was shown to determine the optimized operating speed. By those analyses, the effect of the design parameters of the amplifier and the MDAC stage became clear, such as the reference voltage, the resolution of the 1$^{st}$ pipeline stage, the amplifier's gain, the parasitic capacitance, and the load capacitance. All of the analysis was examined by the simulation. The optimized pipeline stage resolution in terms of power consumption and the ADC's resolution were suggested. Also, the design flow for the interpolated pipeline ADC has been proposed. This chapter is very helpful for not only the ADC designer using interpolated pipeline topology but also the

circuit designer using interpolation with the signal amplification.

Chapter 6 presented the 12-bit interpolated pipeline ADC using body voltage controlled amplifier. For the resolution being higher than 12-bit, the linearity of the single stage open-loop amplifier, such as source degeneration amplifier is not high enough. By the analysis, cascode amplifier with feedback loop can give enough linearity for the target specification. In chapter 6, a body voltage controlled amplifier was proposed, which has the advantages of the telescopic amplifier topology in the low-power consumption and the folded-cascode amplifier topology in the large output swing signal. The architecture and the operation of the proposed amplifier were presented in chapter 6. Especially, the proposed amplifier has a unique current biasing and a CMFB, the operations and the circuit structures were described specifically. And, the 12-bit interpolated pipeline ADC using the proposed amplifier was presented. The proposed ADC achieved good performance in sufficiently low-input frequency, such as ENOB of 10 bit with 300 MS/s and 100 kHz input signal. However, when the input signal frequency is increased, the performance is decreased. The reason of the performance degradation was estimated to the parasitic components in the package and the PCB test board. Even though the proposed 12-bit ADC in this chapter has a problem for the high-frequency input signal, it still has remarkable linearity without MDAC calibration, low-power operation, and realization using only general purpose technology. If the ADC solves the parasitic problem, it will be a very attractive candidate for target application.

The body voltage controlled amplifier has some advantages. However, it requires special offset calibration circuit because of its closed-loop usage. In chapter 7, the 12-bit interpolated pipeline ADC using $g_m$-cell has been presented. The $g_m$-cell has enough linearity characteristic with open-loop amplifier for the 12-bit interpolated pipeline ADC; therefore, it can exhibit the merit of open-loop amplifier such as simple offset calibration and fast settling time. The ADC showed enough high performance in simulation, for example, 11.36 bit of ENOB at 200 MS/s and 601 MHz input signal. In the thesis, two types of the amplifiers (open-loop and closed-loop) and three types of the amplifier topologies (source degeneration, body voltage controlled, and $g_m$-cell) have been presented. In chapter 7, those architectures' performances were compared. As a result, the open-loop architecture is better than the closed-loop architecture for ADC design. Also, it was concluded that source degeneration amplifier for below 10-bit resolution and $g_m$-cell for higher than 10-bit are suitable amplifier topologies.

## 8.2 Prospect of high-speed and high-resolution ADC and Interpolation Technique

As described in chapter. 1, it is expected that the technology scaling will be continued for a while. Although the long channel processes are still used in industry such as 0.35 μm, it is

expected that those long channel technology will be substituted to short channel technology along with the improvement of the design skill and production yield. It is reasonable because the short channel technology has several advantages; for example, low-power consumption, high operation speed, and small core area. The digital circuit benefits by the advantages of the scaled technology. However, the analog circuit suffers from the reduced supply voltage and the reduced transistor's intrinsic gain. This is unavoidable for the SoC development because the analog and the digital circuits are developed by the same technology. Therefore, analog circuit design using scaled technology has to be prepared.

The most suffered analog circuit by reduced transistor's intrinsic gain is an operational amplifier and its application such as high-resolution pipeline ADC. Recently, the calibration techniques (in chapter 2.6) are usually utilized in high-resolution ADC. However, the calibration techniques cause several issues. Therefore, elimination or reduction of the calibration circuit in ADC is one of the important issues. The interpolation technique is one of solutions for the calibration issue. By introducing the interpolation technique, high-speed and high-resolution can be realized without high-gain operational amplifier and complicate calibration technique. Therefore, the drawbacks which are caused by the calibration technique are disappeared.

The merit and the effectiveness of the interpolation technique are proved through the works in this thesis. The subranging ADCs in chapter 3 ~ 4 show how the interpolation technique realizes subranging ADC in low-power consumption without calibration technique. Also, the interpolated pipeline ADCs in chapter 5 ~ 7 prove the effectiveness of the interpolation technique for high-speed and high-resolution ADCs without MDAC calibration, high supply voltage, and specialized S/H circuits. Especially, the analysis in chapter 5 provides a good guideline not only for the interpolated pipeline ADC but also for the circuit

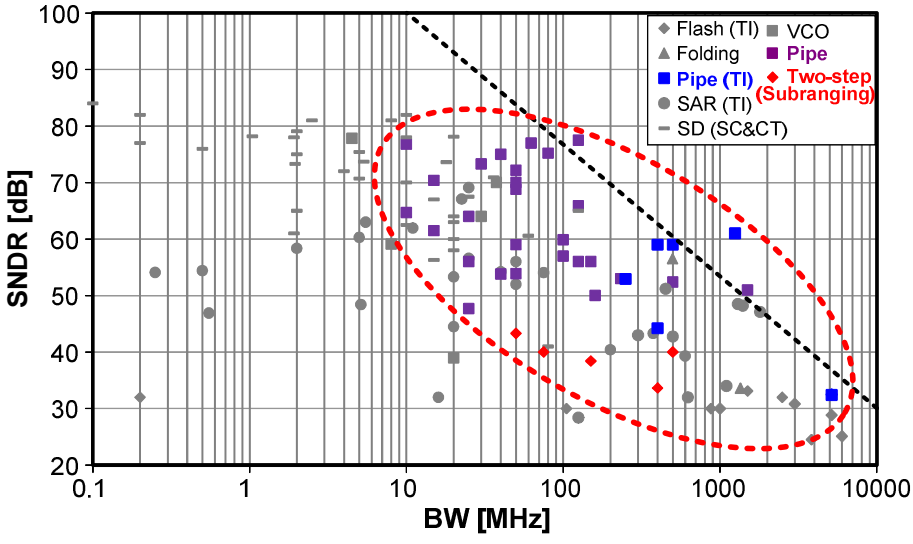


Figure 8.1 A survey on BW vs. SNDR of stage-of-the-art ADC [8.1].

using interpolation technique.

It is difficult to expect that the transistor's intrinsic gain will be increased in the future. On the other hand, it is expected that the requirement of the high-gain operational amplifier will be continued for a while. Figure 8.1 supports the expectation [8.1]. Figure 8.1 shows a survey on the state-of-the-art ADC in BW vs. SNDR. The colored symbols in Figure 8.1 mean the multi-stage ADCs, for example, subranging ADCs and pipeline ADCs. As shown in Figure 8.1, a lot of multi-stage ADCs are located around the performance saturation area (near of the black-dot line). It means that the multi-stage ADCs are leading architecture in recent ADC development. And, as explained in early part in this thesis, the high-resolution pipeline ADC requires high-gain operational amplifier. Because the interpolation technique is one of the good solutions to solve the high-gain operational amplifier requirement issue, the interpolation technique is deserved to develop with high-speed and high-resolution multi-stage ADCs.

## 8.3 Interpolation Technique and Calibration Technique

As introduced in chapter 2, 5, 6, and 7, recent developed high-speed and high-resolution ADCs basically incorporate calibration technique. It means that the calibration technique is very effective method to realize such kind of high-performance ADCs. However, it is obvious that the calibration techniques have several disadvantages as described in chapter 2.6.

On the other hand, the interpolation technique allows high-speed and high-resolution ADC without calibration technique. However, the interpolation technique also has drawback, such kind of the amplifier's linearity requirement or offset calibration. For example, the proposed 12-bit interpolated pipeline ADC in chapter 6 incorporates offset calibration DAC for the amplifier's offset calibration. It decreases the interpolation technique's attractiveness. Another 12-bit interpolated pipeline ADC in chapter 7 solves the offset calibration problem using $g_m$-cell with open-loop. The ADC realizes 12-bit resolution without calibration; however, the verification using actual chip is necessary. At that time, the ADC design meets again to the linearity requirement or offset calibration.

One reasonable design method in the future ADC design for high-speed and high-resolution specification is a combination of the interpolation technique and the calibration technique. Figure 8.2 shows the reduced calibration process in the pipeline ADC design by combination of the interpolation technique. The pipeline ADC's error sources in Figure 2.16 is utilized for the explanation. If the ADC incorporates the interpolation technique, the gain of the amplifier is not a problem as explained in the previous chapters. Therefore, the calibration time for the gain error can be skipped. Also, the linearity requirement can be relaxed because the amplifier's output swing range can be reduced in the interpolated pipeline ADC design (refer to chapter 5.4.3.2). In Figure 8.2, it is assumed that

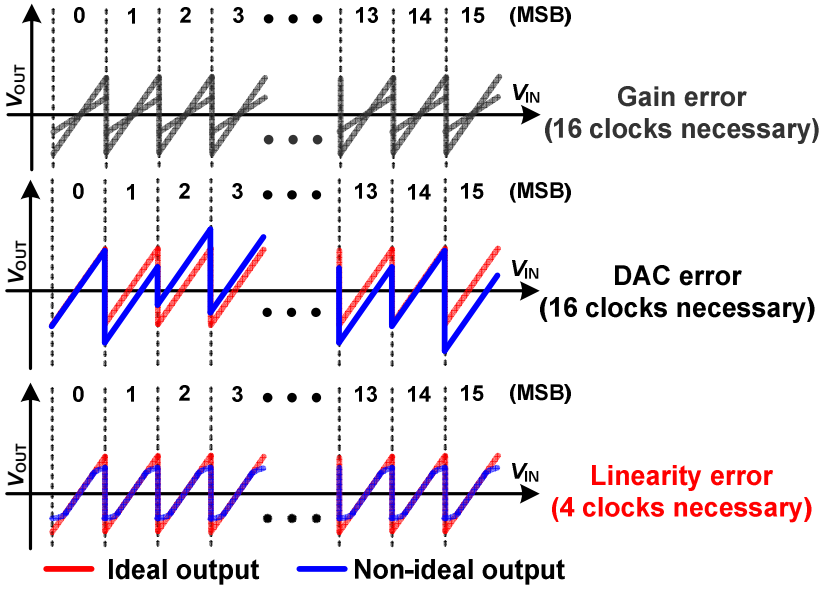


Figure 8.2 Reduced calibration time by introducing interpolation technique.

the linearity requirement is reduced by 4 by use of 4-bit stage resolution. For the DAC error, the interpolated pipeline ADC utilizes the same structure of CDAC as the conventional pipeline ADC, there is no reduction of the calibration time. As a result, the total calibration time is reduced from 48 clock cycles to 20 clock cycles by introducing the interpolation technique. The calculation in Figure 8.2 is very rough. Actually, there are many issues to determine the amount of calibration, such as the amplifier's performance. However, Figure 8.2 shows a good example to explain how the interpolation techniques can help the calibration technique.

As described in chapter 8.2, the requirement for the high-speed and high-resolution ADC will continue in the future. For the realization of such kind of the high-performance ADC, the composition of the light calibration and the interpolation becomes one of the good solutions. Therefore, it is necessary to develop both of the interpolation technique and the calibration technique for the future ADC design.

## Reference

[8.1] B. Murmann, "ADC Performance Survey 1997-2013," [Online]. Available: http://www.stanford.edu/~murmann/adcsurvey.html.

Appendix. A Analysis of Capacitor Mismatch in CDAC

Figure A.1 shows a CDAC which has the same structure with Figure 3.18. $V_{IN}$ and parasitic capacitor are ignored and one of the two reference voltages is changed to GND to simplify the analysis. The number of capacitors in the CDAC, $h$, is decided by resolution of the CDAC. All of the capacitors in the CDAC have the same capacitance, it means $C_1 = C_2 = \cdots = C_h$. When $m$-th capacitor changes its connection node, the variation of output voltage, $V_{STEP}$ is represented as (A.1).

$$\boldsymbol{V}_{\mathrm{STEP}} = \frac{\mathrm{C}_{\boldsymbol{m}}}{\sum_{\boldsymbol{i}=1}^{\boldsymbol{h}} \mathrm{C}_{\boldsymbol{i}}} \mathrm{V}_{\mathrm{REF}} \tag{A.1}$$

A sensitivity of $V_{STEP}$ by the variation of each capacitance is represented as below.

$$\Delta\boldsymbol{V}_{\mathrm{STEP}} = \frac{\partial \boldsymbol{V}_{\mathrm{STEP}}}{\partial \boldsymbol{C}_1}\Delta\boldsymbol{C}_1 + \frac{\partial \boldsymbol{V}_{\mathrm{STEP}}}{\partial \boldsymbol{C}_2}\Delta\boldsymbol{C}_2 + \cdots + \frac{\partial \boldsymbol{V}_{\mathrm{STEP}}}{\partial \boldsymbol{C}_{\boldsymbol{h}}}\Delta\boldsymbol{C}_{\boldsymbol{h}} \tag{A.2}$$

$$\Delta\boldsymbol{V}_{\mathrm{STEP}} = \left\{ -\frac{\mathrm{C}_{\boldsymbol{m}}}{\left(\sum_{\boldsymbol{i}=1}^{\boldsymbol{h}} \mathrm{C}_{\boldsymbol{i}}\right)^2} \left( \sum_{\boldsymbol{i}=1}^{\boldsymbol{m}-1} \Delta\mathrm{C}_{\boldsymbol{i}} + \sum_{\boldsymbol{i}=\boldsymbol{m}+1}^{\boldsymbol{h}} \Delta\mathrm{C}_{\boldsymbol{i}} \right) + \frac{\left( \sum_{\boldsymbol{i}=1}^{\boldsymbol{m}-1} \mathrm{C}_{\boldsymbol{i}} + \sum_{\boldsymbol{i}=\boldsymbol{m}+1}^{\boldsymbol{h}} \mathrm{C}_{\boldsymbol{i}} \right)}{\left(\sum_{\boldsymbol{i}=1}^{\boldsymbol{h}} \mathrm{C}_{\boldsymbol{i}}\right)^2} \Delta\mathrm{C}_{\boldsymbol{m}} \right\} \mathrm{V}_{\mathrm{REF}} \tag{A.3}$$

Because all of the capacitors have the same capacitance, it is possible to substitute for all capacitors to $C$, (A.3) can be simplified as (A.4).

$$\Delta\boldsymbol{V}_{\mathrm{STEP}} = \frac{1}{(\boldsymbol{h}\mathrm{C})^2} \left\{ -\mathrm{C}\left( \sum_{\boldsymbol{i}=1}^{\boldsymbol{h}-1} \Delta\mathrm{C}_{\boldsymbol{i}} \right) + (\boldsymbol{h}-1)\mathrm{C}\Delta\mathrm{C}_{\boldsymbol{m}} \right\} \mathrm{V}_{\mathrm{REF}} \tag{A.4}$$

Equation (A.4) can be organized including standard deviation form, such as $\Delta C/C(\sigma)$.

$$\Delta\boldsymbol{V}_{\mathrm{STEP}}(\sigma) = \frac{1}{\boldsymbol{h}^2} \left\{ \sqrt{ \left\{ -\left( \sum_{\boldsymbol{i}=1}^{\boldsymbol{h}-1} \frac{\Delta\mathrm{C}_{\boldsymbol{i}}}{\mathrm{C}}(\sigma) \right) \right\}^2 + \left\{ (\boldsymbol{h}-1)\frac{\Delta\mathrm{C}}{\mathrm{C}}(\sigma) \right\}^2 } \right\} \mathrm{V}_{\mathrm{REF}} \tag{A.5}$$

In (A.5), each $\Delta C/C(\sigma)$ has the same value because all capacitors have the same capacitance. Equation (A.5) is calculated as below.

$$\Delta V_{STEP}(\sigma) = \frac{1}{h^2}\sqrt{h(h-1)}\,\frac{\Delta C}{C}(\sigma)V_{REF} \tag{A.6}$$

To express (A.6) using total capacitance, $C_{total}$, $\Delta C_{total}/C_{total}$ (σ) is substituted for $\Delta C/C(\sigma)$.

$$\frac{\Delta C}{C}(\sigma) = \sqrt{h}\,\frac{\Delta C_{total}}{C_{total}}(\sigma) \tag{A.7}$$

Substitute (A.7) to (A.6) and normalize to the LSB format of the ADC,

$$DNL(\sigma)\ [\mathrm{LSB}] = 2^N\,\frac{\Delta C_{total}}{C_{total}}(\sigma)\frac{1}{\sqrt{h}}\sqrt{1-\frac{1}{h}} \tag{A.8}$$

where $N$ is the resolution of the ADC.

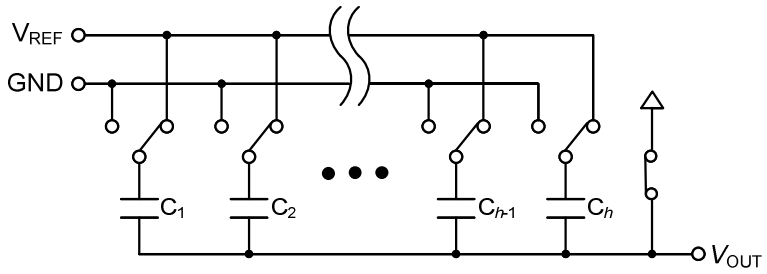


Figure A.1 Simplified CDAC schematic.

Appendix. B Sensitivity of Offset Calibration in Comparator

The comparators in the proposed ADC calibrate its offset voltage by adjusting the slew rate of the input MOS transistor. The slew rate is defined as (B.1),

$$SR = \frac{dV_{OP\_1st}}{dt} = \frac{I_P}{C_{OP\_1st}} \tag{B.1}$$

where $V_{OP\_1st}$ and $I_P$ are illustrated in Figure 3.20. $C_{OP\_1st}$ means node capacitance including offset calibration capacitance in the $V_{OP\_1st}$. In this case, only the positive side is utilized; however, it is also applicable to the negative side. The current $I_P$ flows through the input MOS transistor in the comparator. Therefore, it can be expressed as (B.2)

$$I_P = \alpha \cdot V_{eff}^2 \tag{B.2}$$

where α means a coefficient and $V_{eff}$ means ($V_{GS}$- $V_T$) of the input MOS transistor. Substitute the $I_P$ in (B.2) to (B.1), the slew rate is derived as (B.3).

$$SR = \frac{\alpha \cdot V_{eff}^2}{C_{OP\_1st}}. \tag{B.3}$$

The main reason of the offset voltage of the comparator is the mismatch of the threshold voltage, especially the input MOS transistors. If there is an offset in the comparator, current $I_P$ is changed; therefore, $SR$ is also changed from its initial value. According to (B.1), it is realized that the offset voltage can be described using $V_{eff}$, because $V_{eff}$ includes $V_T$. The sensitivity of the offset by the variation of the calibration capacitance is expressed as (3.15).

$$\frac{\partial V_{off}}{\partial C_{OP\_1st}} = \frac{\partial V_{eff}}{\partial C_{OP\_1st}} = \frac{\partial SR / \partial C_{OP\_1st}}{\partial SR / \partial V_{eff}} = -\frac{V_{eff}}{2C_{OP\_1st}} \tag{3.15}$$

Appendix. C Input Referred Noise in Interpolated Pipeline MDAC Stage

From Figure 5.35, a formula can be derived for the output noise power ($V_{no}^2$) with consideration of the frequency as below.

$$V_{no}^2 \approx 4kT\left\{\left(\gamma g_{m\_eff} + \frac{1}{R_D}\right)R_D^2 + R_{swi}\left(G_{pi} g_{m\_eff} R_D\right)^2\right\}\int_0^\infty \frac{1}{1+\left(\frac{f}{f_L}\right)^2} df. \quad \text{(C.1)}$$

Parameters in (C.1) are the same as explained in chapter 5.4.1. Also, the effect of $R_{swo}$ in Figure 5.35 is omitted. In (C.1), $f$ means frequency and $f_L$ means the cut-off frequency. Equation (C.1) can be arranged as

$$V_{no}^2 = 4kT\left\{\gamma g_{m\_eff} R_D^2 + R_D + R_{swi}\left(G_{pi} g_{m\_eff} R_D\right)^2\right\}\frac{\pi}{2} f_L. \quad \text{(C.2)}$$

Equation (C.2) can be reorganized by substituting $f_L$ to the output resistance and capacitance.

$$V_{no}^2 = kT\left\{\gamma g_{m\_eff} R_D^2 + R_D + R_{swi}\left(G_{pi} g_{m\_eff} R_D\right)^2\right\}\frac{1}{R_D\left(C_L + C_{po}\right)}. \quad \text{(C.3)}$$

The output parasitic capacitance is considered for the accurate calculation. Equation (C.3) is rewritten as

$$V_{no}^2 = \frac{kT}{\left(C_L + C_{po}\right)}\left\{1 + R_{swi}\left(G_{pi} g_{m\_eff}\right)^2 R_D + \gamma g_{m\_eff} R_D\right\} \quad \text{(C.4)}$$

To obtain the input referred noise power, the output noise power has to be divided by gain.

$$V_{ni}^2 = \frac{kT}{\left(G_{pi} G_0\right)^2\left(C_L + C_{po}\right)}\left\{1 + R_{swi}\left(G_{pi} g_{m\_eff}\right)^2 R_D + \gamma g_{m\_eff} R_D\right\} \quad \text{(C.5)}$$

As explained in chapter 5.4.1, the signal path gain $G_{pi}$ is also considered to figure out the effect by the input parasitic capacitance of the amplifier. Lastly, equation (C.5) can be reorganized to (5.45) by substituting $G_0$ to $g_{m\_eff}R_D$.

The input referred noise power with consideration of the ENOB degradation is expressed as below [C.1].

$$V_{ni}^2 \approx \left(2^{2\times\Delta ENOB} - 1\right)\frac{V_q^2}{12}. \quad \text{(C.6)}$$

By substitute $V_{ni}^2$ in (C.6) to $V_{ni}^2$ in (5.45), the ENOB degradation can be expressed as (5.53).

**Reference**

[C.1] Akira Matsuzawa, Invited, “Essence and Technology Direction of ADC Design,” *International Meeting for Future of Electron Devices (IMFEDK)*, Japan, May. 2012.

# Appendix. D. Measurement Results of Temperature Variation

In chapter 2.6, the calibration techniques are introduced. Among the calibration techniques, the temperature variation of the circuit after foreground calibration is pointed as a serious problem. To become a counterpart of the calibration techniques for high-speed and high-resolution ADC, the interpolated pipeline ADC has to be examined about the temperature variation.

In this Appendix, the measurement results for the temperature variation are explained. To perform the temperature variation measurement, special equipment is necessary to maintain the temperature of the measurement environment in constant. This is because temperature of the chip (inside package) is increased to several tens of degree after starting the operation.

Figure D.1 shows the measurement equipment for temperature variation. As shown in Figure D.1, the equipment can control the equipment temperature. Usually, PCB test board including test package are utilized for the measurement as shown in Figure D.1. On the side wall of the equipment, there is a hole to connect power and signal cables for the measurement set up.

For the temperature variation measurement, a 10-bit 80 MS/s interpolated pipeline ADC is utilized. The ADC is demonstrated in 1P9M 90 nm CMOS technology. Basically, the ADC for the measurement has completely same structure with the interpolated pipeline ADC in [D.1]. It is designed for the communication system which is developed a company; therefore, target performance is different from [D.1]. Even though the performance is different from [D.1], both of ADCs has the same structure. Therefore, this measurement results can be applied to other interpolated pipeline ADCs.

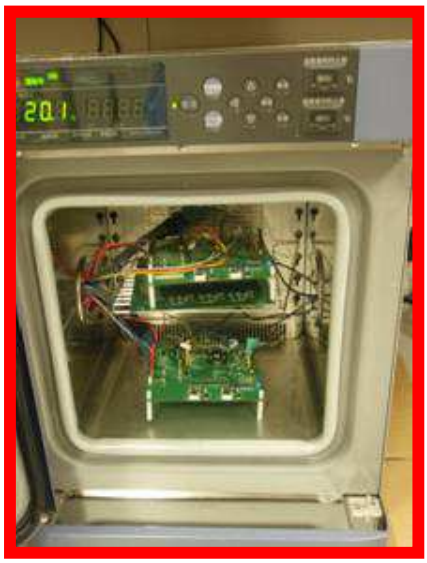

Figure D.1 Equipment for temperature variation measurement.

Figure D.2 shows the measurement results of the 10-bit interpolated pipeline ADC. The input frequency is set to 1 MHz and the sampling frequency is swept from 10 MHz to 110 MHz. The measurement is performed under three temperature conditions, -40, 20, 80 degree. Only comparator's offset calibration is performed before the ADC operation. As shown in Figure D.2, the ADC keeps ENOB of 8.4-bit in any temperature until 90 MS/s. In the measurement results, -40 degree condition shows the best performance. The ENOB difference between -40 degree and 80 degree is only 0.3-bit which can be negligible. By the temperature measurement results, it is proved that the interpolated pipeline ADC has high robustness for the temperature variation.

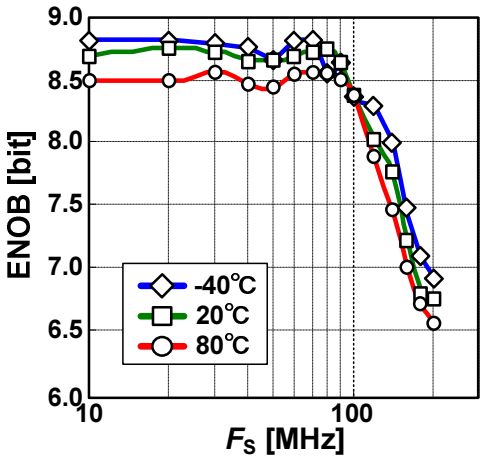


Figure D.2 Measurement results with temperature variation (1 MHz input).

**Reference**

[D.1] M. Miyahara, H. Lee, D. Paik, and A. Matsuzawa, "A 10b 320 MS/s 40 mW Open-loop Interpolated Pipeline ADC," in *Dig. Symp. VLSI Circuits*, pp.126-127, Jun. 2011.

# Appendix. E. Research Achievements

## E.1 Journal Paper

[E.1] **Hyunui Lee**, Yusuke Asada, Masaya Miyahara, and Akira Matsuzawa," A 6 bit, 7 mW, 700 MS/s Subranging ADC using CDAC and Gate-Weighted Interpolation," in *IEICE Transactions on Fundamentals*, Vol. E96-A, No. 2, pp. 422-433, Feb. 2013.

[E.2] **Hyunui Lee**, Masaya Miyahara, and Akira Matsuzawa, "Design of Interpolated Pipeline ADC using Low-gain Open-loop Amplifiers," in *IEICE Transactions on Electronics*, Vol. E96-C, No. 6, pp. 838-849, Jun. 2013.

[E.3] **Hyunui Lee**, Masaya Miyahara, and Akira Matsuzawa, "A 12-bit Interpolated Pipeline ADC using Body Voltage Controlled Amplifier," in *IEICE Transactions on Fundamentals*, Vol. E96-A, No. 12, pp. - , Dec. 2013.

## E.2 International Conference

[E.4] **Hyunui Lee**, Masaya Miyahara, and Akira Matsuzawa, "A 6-bit Subranging ADC with Single CDAC Interpolation," *IEEE International Conference on Electron Devices and Solid-State Circuits (EDSSC)*, Hong Kong, Paper ID. 41, Jun. 2013

[E.5] **Hyunui Lee**, Masaya Miyahara, and Akira Matsuzawa, "A 12-Bit Interpolated Pipeline ADC Using Body Voltage Controlled Amplifier," *IEEE International NEWCAS Conference*, Paris, France, Paper ID. 4061, Jun. 2013

## E.3 International Workshop

[E.6] **Hyunui Lee**, Yusuke Asada, Kei Yoshihara, Tatsuya Urano, Masaya Miyahara, and Akira Matsuzawa, "A 6 bit, 7 mW, 250 fJ, 700 MS/s Subranging ADC," *The International Workshop on Millimeter Wave Wireless Technology and Applications*, Tokyo, Japan, Dec. 2010

[E.7] **Hyunui Lee**, Masaya Miyahara, and Akira Matsuzawa, "A 6-bit Subranging ADC using one differential signal and two reference voltages," *Workshop and IEEE EDS Mini-colloquium on Nanometer CMOS Technology 37*, Tokyo, Japan, p.62, Feb. 2013

## E.4 Domestic Conference

[E.8] **Hyunui Lee**, Daehwa Paik, Masaya Miyahara, and Akira Matsuzawa, "Offset Calibration Technique for Comparator in Nanoscale CMOS Process," *LSI and System Workshop*, Kitakyushu International Conference Center, 1001-34, May. 2010

[E.9] **Hyunui Lee**, Masaya Miyahara, and Akira Matsuzawa, "Study of Influence on SAR ADC by Range of Input Signal," *in Proc. IEICE Society Conference*, Osaka

Prefecture University, C-12-6, Sep. 2010

[E.10] **Hyunui Lee**, Masaya Miyahara, and Akira Matsuzawa, “An Influence of Parasitic Capacitors on a Performance of Interpolated Pipeline ADC,” *in Proc. IEICE Society Conference*, Hokkaido University, C-12-8, Sep. 2011

E.5 Co-author Publication

E.5.1 International Conference

[E.11] Masaya Miyahara, **Hyunui Lee**, Daehwa Paik, and Akira Matsuzawa, "A 10b 320 MS/s 40 mW Open-loop Interpolated Pipeline ADC," *IEEE Symposium on VLSI Circuits*, Kyoto, Japan, pp.126-127, Jun. 2011.

E.5.2 Domestic Conference

[E.12] Yoshihiro Tsunokawa, **Hyunui Lee**, Masaya Miyahara, and Akira Matsuzawa, “Setting accuracy and mismatch measurement of MOM capacitors,” *in Proc. IEICE Society Conference*, C-12-9, Sep. 2011

[E.13] Yoshiyuki Hirooka, **Hyunui Lee**, Masaya Miyahara, and Akira Matsuzawa, “High Linearity Open-loop Amplifier for Interpolated Pipeline ADC,” *in Proc. Integrated Circuits and Devices*, Dec, 2011