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Doctoral Thesis

A Study on Process and Device Structure for Schottky and Heterojunction Tunnel FETs using Silicide-Silicon interface

ショットキー及びヘテロシリサイド・シリコン接合トンネル FET の
プロセス及び構造因子に関する研究

A dissertation submitted to the department of electronics and applied physics,

Interdisciplinary graduate school of science and engineering,

Tokyo institute of technology

for the degree of Doctor of engineering

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Abstract

Power consumption reduction of MOSFETs is pursued by the lowering supply voltage. However, keeping the trend is difficult due to increase in off-leakage current, which increases the total power consumption. Therefore, FETs with steep subthreshold slope (SS) have been intensively investigated. Among a few candidates for the steep SS FETs, tunneling FET (TFET) is a most promising one owing to its simple structure and its capability of the drain voltage reduction. However, TFETs suffer from relatively low drivability due to its high tunneling resistance. In order to boost the drivability, TFET using III-V semiconductor hetero-junction structure has been investigated, however III-V semiconductor FET itself has issues such as formation of gate stack with good interface integrity as well as realization of low contact resistance with conducting metal wires in circuits. Considering all of these backgrounds, a study on process and device structure of Si-based TFET with high drivability has been conducted.

In this thesis, Si-based tunneling FETs (TFETs) with silicide/silicon junction are studied using 2-dimentional device simulation. One of such device is TFET using Schottky-type conducting silicide/Si interface. The study on the Schottky barrier TFET revealed that Schottky barrier height influence on the SS characteristics in a different manner between long (50nm) and short (10nm) gate length devices. Eventually, it has been revealed that this type of short channel TFET can achieve almost the same drivability to the conventional MOSFETs with smaller SS by the optimization of structural parameters.

For the realization of the silicide/Si structure suitable for Schottky barrier TFETs, defect free silicidation at the interface with quite wide range of the barrier Φ_{bn} controllability is desired. In order to meet the demand, a

novel silicide formation process using annealing of metal/silicon thin film stack is proposed and its applicability to FETs was demonstrated.

Since it is understood that the elimination of electrons which belong to a high energy tail in Fermi-Dirac distribution in the source electrode is effective to reduce SS further, the band-to-band tunneling from semiconducting source and the influence of valence band and conduction band discontinuities at source-channel interface are investigated using device simulations. A steeper SS with higher ON current can be both achieved with larger discontinuity, owing to reduced tunneling distance and lower energy barrier for the quantum mechanical tunneling of electrons.

In order to realize such hetero-junction in Si-based TFETs, TFETs using semiconducting silicide/Si hetero-junction are proposed. The simulation study on TFETs using semiconducting silicide (Mg_2Si)/Si hetero junction revealed that narrow band gap of the silicide and large conduction/valence band edge discontinuities at the junction lead to a drastic SS reduction. It could be concluded that this novel TFET is a promising candidate for a steep SS FET with comparable drivability to the conventional MOSFETs.

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Chapter 1
Introduction

1.1 The scaling of MOSFETs and the reduction of the power consumption

1.1.1 History of integrated circuits

The first commercial release of a computer based on integrated circuit (IC) technology dates back to late-1960s. Due to the low-cost manufacturing potentialities offered by emerging ICs, researchers and industrial partners have directly joined their effort to convert a promising technology at its birth to the biggest technological revolution of the twentieth century. Initially mainly designed for military applications, the computers integrate nowadays our every day's life: from basic communication and entertainment to fussy scientific supports for the forthcoming new technologies. In the heart of this tremendous adventure, lies the silicon Complementary Metal-Oxide-Semiconductor (CMOS) transistor - currently the most widespread semiconductor switch. The big success of the CMOS devices is explained by the possibility to increase the drive current and the cut-off frequency at the same time only by reducing the size of the devices [1.1]. The downscaling of the transistors has allowed very large scale integrated chips operating at increasingly high frequency. The functionalities of the computers have become more and more various and complex for a lower cost per functions of the chips.

The CMOS scaling has been governed by the so-called Moore's law since 1965. The co-founder of Intel company, G. Moore, predicted that the number of transistors on

a chip would double every 24 months. In order to meet the Moore's law specifications and the market requirements, the International Technology Roadmap for Semiconductors (ITRS) , has suggested for more than 10 years the strategies to adopt for the semiconductor industry, forecasting the market evolution 15 years ahead.

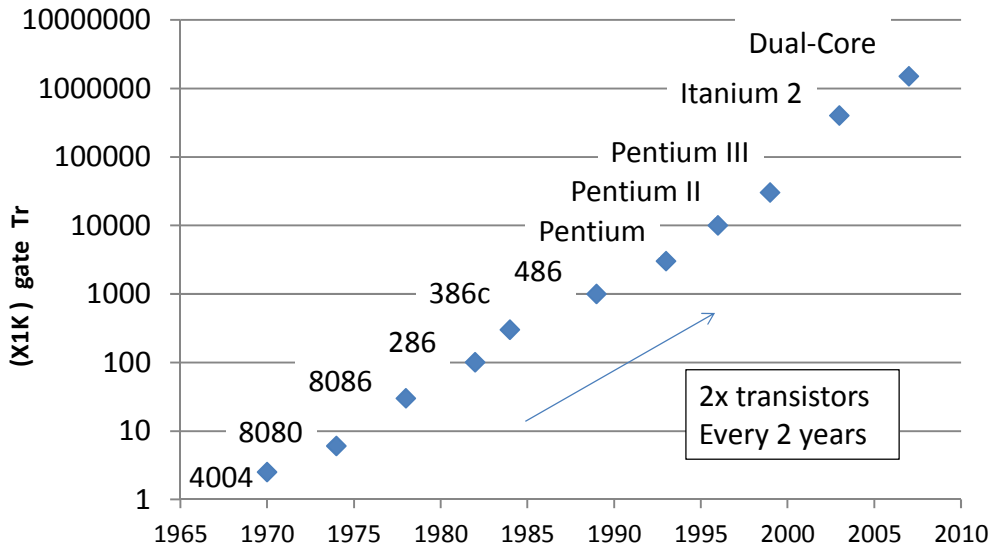
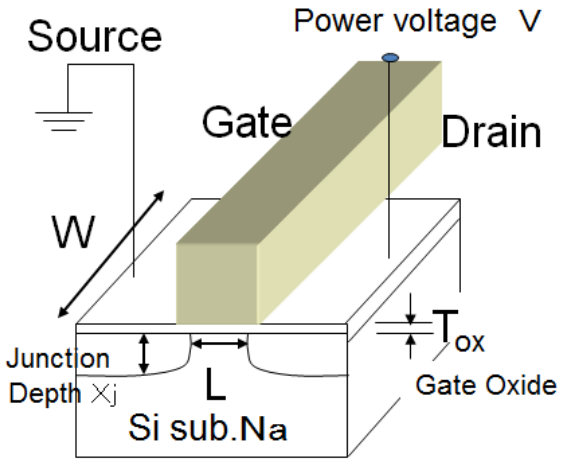


Figure 1.1 History of Intel processer. Moore's law predicted the the number of transistors on a chip would double every 24 months.

1.1.2 CMOS scaling Law

As briefly introduced in the previous section, MOSFETs and the integrated circuits using the devices has been developing along the scaling law [1.1] In this rule, the power voltage is scaled with the minimization of the device scale in order to keep the electric field inside the devices constant. Figure 1.2 shows the scaling of each component of MOS transistors and the power voltage with the scaling factor K.



Parameter	Symbol	Scaling
Channel Length	L	1/K
Channel Width	W	1/K
Gate Oxide Thickness	Tox	1/K
S/D Junction Depth	Xj	1/K
Channel Doping Conc.	Na	K
Power Voltage	V	1/K

Figure 1.2 Scaling of each component of MOS transistors and the power voltage with the scaling factor K.

The drain current Id is simply written as follows:

$$I_d = \frac{W\mu C_{ox}}{2L}(V_G - V_{th})^2 \qquad (1.1)$$

, where C_{ox}, V_G, V_{th} are mobility of the carrier, gate capacitance of unit area, gate voltage, and the threshold voltage, respectively. When the scaling is applied to the equation, Id

can be scaled by 1/K. On the other hand, gate delay can be modeled as follows:

$$\tau = \frac{C_G V}{I_d} \qquad (1.2)$$

, where C_G is the gate capacitance. Therefore, the gate delay is scaled by 1/K. It means that the device speed can be increased by a factor of K. The power consumption of the each device is modeled as follows:

$$P = \frac{1}{2} f C_G V^2 \qquad (1.3)$$

, where *f* is the device speed. Therefore, one can estimate the scaling reduces the power consumption of device drastically by the factor of $1/K^2$.

1.1.3 Ultimate CMOS downsizing

Nowadays, the best processors available in the market are clocked at a frequency of around 3.5 GHz with a gate length of 22nm (Intel Core i7 4770K). Meanwhile, microelectronic research is currently working towards the 14 nm technology node and even far beyond. According to the ITRS forecasts, research follows two different directions: either pushing the conventional Metal-Oxide-Semiconductor Field- Effect Transistor (MOSFET) toward its physical limits, with a possible modification of the planar architecture, or exploring a new way of making transistors, e.g. devices based on Si nanowires, carbon nanotubes, single electrons FETs, and much more advanced

devices such as quantum cellular automata and spin-based electronics. For the 10 years to come, it is believed that the aggressive downscaling of MOSFETs will be adopted for the mass-production devices. The downscaling of CMOS transistors is now facing several difficulties stemming from the reduced size of the devices. Technological solutions must be brought by the research centers in order to make the small transistors meeting the ITRS requirements. Currently, four trends emerge from the publications related to this subject:

New transistor architectures

The downscaling toward short-channel transistors implies a threshold voltage (V_{th}) reduction and a drain-induced barrier lowering (DIBL), i.e the reduction of V_{th} induced by the drain voltage. Both effects belong to phenomena of so-called Short-Channel Effects (SCE). Fully depleted silicon-on-insulator substrates and multiple gate devices such as FinFET have been proposed to overcome SCE by the suppression of the charge share issue [1.2] and the enhancement of the controllability of the gate electrode.

Replacements of the gate stack

In order to boost the gate controllability, a lot of studies are related to a better gate engineering, however, one of the biggest problems is the current leakage trough the thin gate stacks. The gate oxide should be scaled in the same way as the channel length and have reached down to 1nm region, where SiO_2 shows a vast amount of leakage current. Therefore, high-k dielectric materials such as Hafnium oxide (HfO_2) and metal gate have been proposed to replace the usual SiO_2 oxide

and the poly-silicon gate for sub-45 nm transistors.

Change of the channel material

Another trend is the increase of the channel mobility. Alternative substrates such as Ge, III-V or strained-Si could be used for improving the hole and electron channel mobility. Since the introduction of different materials such as III-V, Ge on Si is a difficult challenge, it need lots of work to be done. Therefore, it seems that the strained-Si is the best alternative channel to be implemented in CMOS technology, so far.

Reduction of parasitic resistance

The miniaturization of the device geometry also brings the shrink of the source drain to metal contact windows. This leads to the drastic increase in the contact resistance of those regions [1.3]. In order to use the window as much as possible, self-aligned silicide technology has been developed. TiSi2 [1.4], CoSi2[1.4], and NiSi[1.5] are used as the materials in this process because of their low resistivity as well as relatively high thermal stability. Nowadays, however, the contact resistivity near ~~to~~ or less than $1x10^{-8}$ Ωcm^2 is required.

1.1.4 Reduction of the operation voltage

As mentioned in previous sections, the scaling of the MOS transistors requires the shrink of each part of the devices and the power supply voltage at the same time. This is because the electric field inside the devise has to be kept constant [1.1].It is necessary to reduce the threshold voltage in accordance of the power voltage reduction. In order to

keep the drain current high and abide by the scaling law, gate over drive, i.e. the portion (V_G -*Vth*) in the eq.(1) should be scaled by 1/K. Therefore, in case that power voltage V_G is scaled to be 1/K, the threshold voltage should also be scaled down by 1/K.

1.1.4.1 Power voltage reduction trend shown in ITRS

Power voltage reduction trend of MOS transistors until 2020 is shown in Figure 1.3. It clearly shows although the scaling law requires the reduction of the power voltage by the factor of 1/K in accordance with the technology node, the reduction is not expected to be kept. Figure 1.3 shows power voltage as a function of the half pitch of MOS transistors predicted in ITRS until 2024. For example, for the reduction of technology node from 55nm to 22nm, the power voltage is reduced only by 20% and 5% for high-performance (HP) and low stand-by power (LSTP) transistors although one expects the reduction should be 60% in this case, if he tries to meet the scaling law.

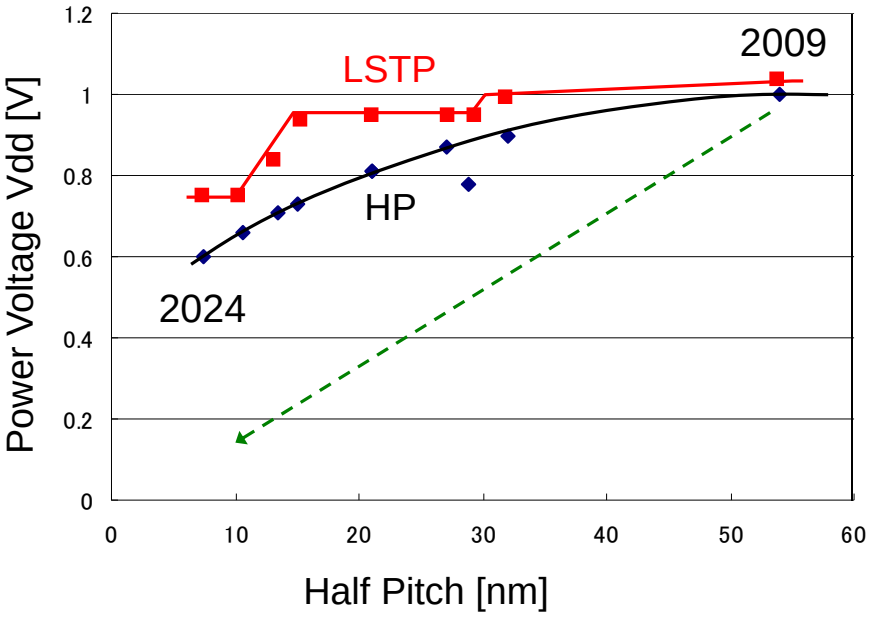


Figure 1.3 Power voltage as a function of the half pitch of MOS transistors from ITRS. The prediction until year 2024 is shown.

In the following sections, the reason why the power voltage cannot be scaled will be explained closely.

1.1.4.2 Reduction of drain current

Drain current Id is represented by the eq.(1). This equation indicates that the supply voltage reduction drastically decreases Id by the power of two. This relationship can be explained by the fact that the reduction of the gate overdrive leads to the decrease in the number of sheet charge in the unit area under the gate, and in addition to that the reduction of the electric field along the channel leads to the decrease in the carrier velocity in the channel. These two factors influence on the drive current by the reduction of supply voltage. Scaling law predicts that the gate capacitance and voltage decrease compensate the above-mentioned drain current decrease, resulting in the gate delay decrease, however in reality, the threshold voltage cannot be scaled due to the off leakage current increase, which will be discussed in the next section. High threshold voltage reduces V_G -*Vth* much more than expected and this fact leads to the reduction of drain current in a great manner.

1.1.4.3 Power consumption increase by Off leakage current

As the size of the MOSFET becomes small, the leakage current in the subthreshold region increases. This is the short channel effect (SCE) mentioned in the previous

section. In order to overcome the issues, ultra-thin silicon on insulator (UTSOI) or High-k gate oxide have been applied in order to improve the controllability of the channel potential against the shot channel effects. Recently, nanowires with gate all-around structure have been studied intensively. But even without the SCE, the *Vth* reduction of the MOSFET leads to the increase in the off-leakage current. This phenomenon has its origin in the intrinsic characteristics of MOSFETs: The subthreshold swing S, which represents the cut-off property of the device, is expressed as in the following equation.

$$S = \frac{kT}{q}\left(1 + \frac{C_d}{C_{ox}}\right) \qquad (1.4)$$

, where k, T, q, C_d, C_{ox} are the Boltzmann constant, temperature of the device, elementary charge, capacitance of the space charge region under the channel in the substrate, and the gate oxide capacitance, respectively. This equation means that the diffusion current flowing through the channel at the weak inversion state is governed by the numbers of the carriers inside the source electrode which are thermally exited up to the channel potential. At the room temperature, the minimum S is 60mV/dec, provided that the $C_d/C_{ox}<<1$, i.e. the gate oxide is very thin compared to the space charge region thickness. Because of this fact, MOSFETs need a certain amount of threshold voltage in order to reduce the off current to very low levels. The lowering of the threshold voltage in accordance with the scaling law brings about the increase in the off current as shown in Figure 1.4, This phenomenon throughout the USLI chips results in the drastic increase in the power consumption in the static states. Figure 1.5 shows the increase in the power consumption predicted for the coming years. (P_{leak} represents the power

consumption by the leakage current.)

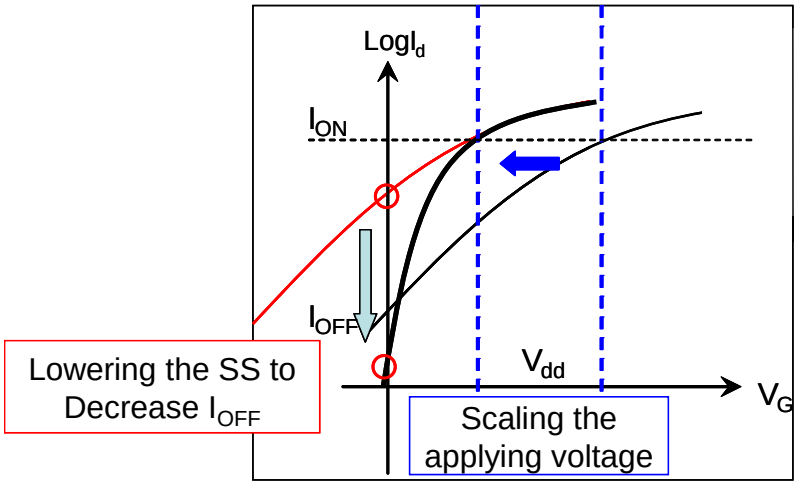


Figure 1.4 Reduction of the threshold voltage leads to the increase in the off leakage current. A device with much steeper subthreshold characteristic is required for the reduction of the supply voltage.

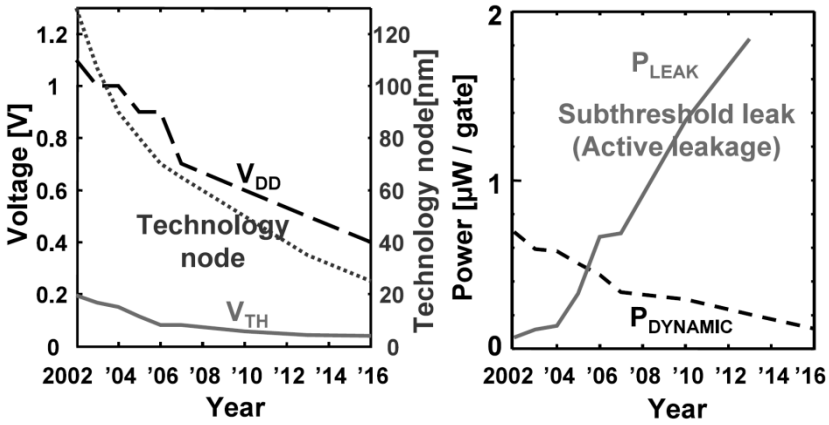


Figure 1.5 ITRS predicts the reduction of the supply voltage and the threshold voltage in accordance with the V_{dd}. Consequently, static power consumption due to the off leakage current becomes much larger than the dynamic power

consumption.

1.2 Steep subthreshold swing devices

Many MOSFETs whose function is not governed by the drift-diffusion mechanism in the channel region as in the conventional MOSFETS are proposed in order to realize steeper subthreshold characteristics. In the following sections some examples which has been intensively studied are introduced.

1.2.1. I-MOS

It is well known that when electrons obtain large kinetic energy around the MOS channel/drain interface enough to transfer the energy to the electron inside the valence band and enhance them to the conduction band, proliferation of electron-hole pairs happens in that region. In most cases, it brings about adverse effect such as degradation of MOSFET and floating body effect of SOI MOSFETs. Recently, however Stanford university proposed a novel concept of MOSFET in which this phenomenon is used for obtaining the steep subthreshold characteristics. This is called ‘Impact Ionization MOS transistor (I-MOS). [1.6,1.7] In this device, gate voltage is used to form channel in the i-region under the gate in order to modulate the width of the intrinsic semiconductor region between p-type and n-type source and drain as shown in Figure 1.6. By this modulation, amount of the impact ionization and eventually the drain current is changed.[1.6]

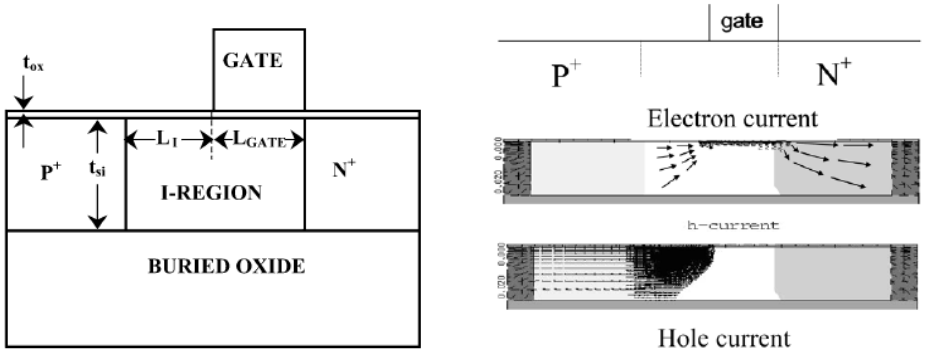


Figure 1.6 Device structure of Impact Ionization MOSFET (IMOS), ***(b)*** current through the IMOS under the ON state. [1.6]

S slope below 10mV/dec has been obtained [1.6]. Issue for this device is that high drain voltage V_d >>1 is required to obtain a reasonable level of drain current. Therefore, many measures for the enhancement of the drain current such as vertical multi nano-wire structure [1.8] strain introduction [1.9], as well as introduction of smaller bandgap material [1.10] have been proposed. Another issue is the controllability of the length of intrinsic semiconductor region between the gate and P-type region (L_I in Figure 1.6(a)).

1.2.2 Feedback FET

Feedback FET is depicted in Figure 1.7. This devise uses the trapping of electrons and holes at channel/drain and channel/source interface region, where spacers separate the i-region under the gate from source/drain.

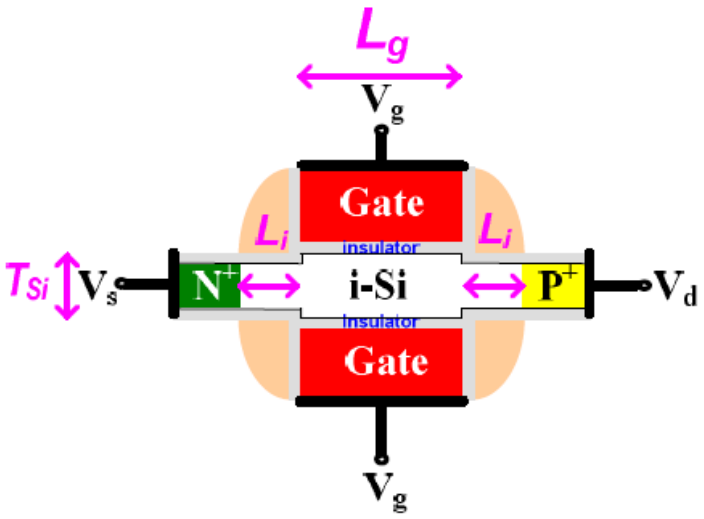


Figure 1.7 Structure of Feedback MOSFET. Holes and electrons gradually accumulate at the boundary portion (L_i) between N^+-source and i-channel, i-channel and P^+-drain under the on state, which reduces the potential barrier for the current flow between source and drain. [1.11]

This device operates as follows: Positive voltage is applied to P+-type drain so that the P-i-N diode is under forward condition. Once channel is formed by the gate voltage increase, electrons and holes flow under the gate. Due to the energy barrier existence at the boundary portion (L_i) beside the gate region, holes and electrons gradually accumulate at the portion (L_i) between N+-source and i-channel, i-channel and P+-drain under the on-state. Those holes and electrons reduce the potential barrier for the current flow between source and drain, resulting in the enhancement of the forward P-i-N diode current. [1.11] Such a 'positive beedback' makes the subthreshold characteristics very steep and S factor less than 10mV/dec was obtained.

According to the functional principle of this device, L_I portion is indispensable to this device, however, the existence of this portion increases the channel resistance,

resulting in the small drivability of this device. Similar to I-MOS, the controllability of the length of L_I between the gate and source, gate and drain may become the issue for the mass production of these devices in ULSIs.

1.2.3 Tunneling MOSFET

Similar to IMOS and feedback FET, Tunneling MOSFET uses p-i-n structure, the device concept which makes this device different from others is that this device uses quantum-mechanical tunneling phenomenon through the bandgap of semiconductors. In this device the function of the gate electrode is to modulate the potential of i-region so that it can control the tunneling phenomenon from the source to the channel region. [1.12] Figure 1.8 shows the principle for the case of N-type tunneling MOSET.

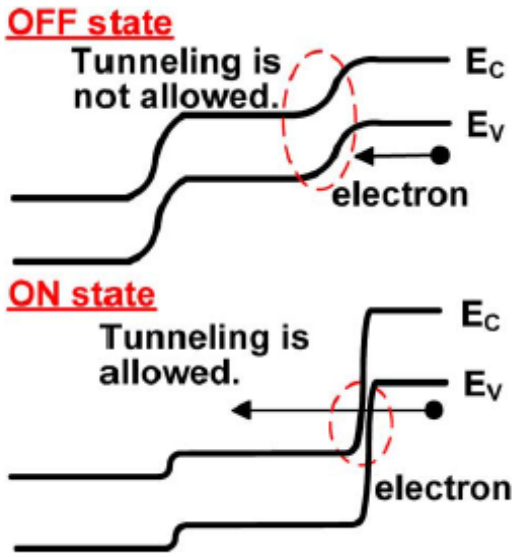


Figure 1.8 Band diagram of a tunneling MOSFET. P-i-N structure is formed with gate electrode above i-region. The gate voltage modulates the potential of i-region so that it can control the tunneling phenomenon from the source to the channel

region [1.12].

By using the novel function, this device also shows the subthreshold swing less than 60mV/dec.[1.12] Advantage of this device to IMOS and Feedback MOSFETs is that this device does not require the existence of Li region, however, using the quantum-mechanical tunneling through a certain bandgap of semiconductor materials, this device also suffers from the low drivability compared to the conventional MOSFETs. In order to boost the drain current many measures such as high-mobility (i.e. small effective mass) channel[1.13], hetero-junction source/channel structure [1.14], nano-wire, nano-tube structure [1.15] have been proposed.

Table1.1 shows the FETs with new carrier injection mechanisms. Tunneling FET uses the electron/hole tunneling probability so that a subthreshold slope less than 60 can be achieved. On the other hand, impact ionization FETs use the phenomenon around the channel/drain interface to dramatically increase the number of carriers so that the subthreshold slope can be kept small. Feedback FET uses dramatic charge injection modification at the sidewall of the gate by the potential profile change under the sidewall between on and off states. These new FETs have features that the off-current can be suppressed even at a temperature of operation. One of the issues of I-MOS as well as the feedback FETs is the degradation of the on-current, and therefore, the operation voltage cannot be scaled. And also there exists a reliability problem with charge trappings during the operation. Therefore, among these devices, tunneling FET can be one of the candidates for future FETs with low power consumption.

Table 1-1 Comparison of Various NEW type MOS devices

Device type	n^+-p-n^+ (Conv)	Tunnel (P-i-N) FET	Impact ionization FET	Feedback FET
Subthreshold Slope (mV/dec.)	60>	60<	60<<	60<<
Temperature Dependence of I_{off}	Large	Small	Small	Small
ON current	○	△	Small	Small
Scaling of V_{Apply}	○	○	△	△
Reliability Issues	—	—	Hot carriers	Charge injection into sidewall

1.3 MOSFETs with Silicided Junction

1.3.1 Silicides as LSI material and their properties

Silicides are chemical compounds between metal and silicon. Variety of metals ranging from Magnesium (atomic No.12) to Tungsten (74), and even Uranium (92) reacts with silicon to form silicides. Some silicides such as Ti silicide [1.4] , Co silicide [1.4] and Er silicide [1.16] are conductors, while others such as Mg silicide [1.17] as well as Fe silicide [1.18] have semiconducting properties. Until recently, a few conducting metal silicides have been applied to ULSIs in order to reduce the parasitic resistances. Figure 1.9 shows the parasitic resistance of a MOSFET.

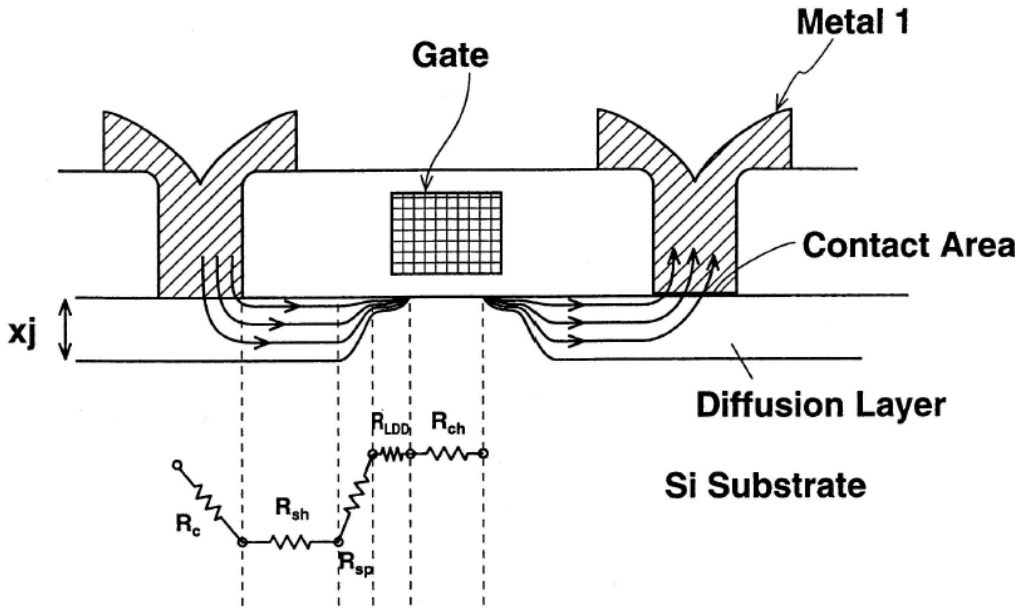


Figure 1.9 parasitic resistance of a MOSFET

The parasitic resistance can be categorized as follows:

1) source/drain sheet resistance
2) contact resistance between the source/drain and conducting metal
3) sheet resistance of extension
4) spreading resistance
5) gate electrode resistance

Highly-doped diffusion layer have been used as source drain electrodes, however its resistivity is as high as 1m Ω cm. In order to reduce the parasitic resistance, metal silicide is formed on the source drain diffusion layer. The formation of the low resistivity silicide can reduce the source/drain sheet resistances, spreading resistance and moreover contact resistance between the source/drain and conducting metal due to the widening the contact area between the source/drain diffusion layer and metal part

(metal silicide in this case). Selective formation of metal silicide only on the source/drain is indispensable, because otherwise, the source-gate-drain electrode would be short-circuited. Self-aligned silicide (SALICIDE) process [1.4,1.5] is used for the selective formation, in which metal thin film is deposited all over the surface followed by the silicide annealing. In this annealing, silicide is formed only on source/drain surface region where metal thin film and Si surface contact directly. Unreacted metal removal by chemical solution leaves the silicide layer, keeping the electrical isolation between source, drain and gate electrodes. Among various silicide, those with low resistivity such as TiSi2[1.4], CoSi2[1.4] and NiSi[1.5] are used for this process. Figure 1.10 shows the cross-sectional image of a MOSFET with the self-aligned silicide.

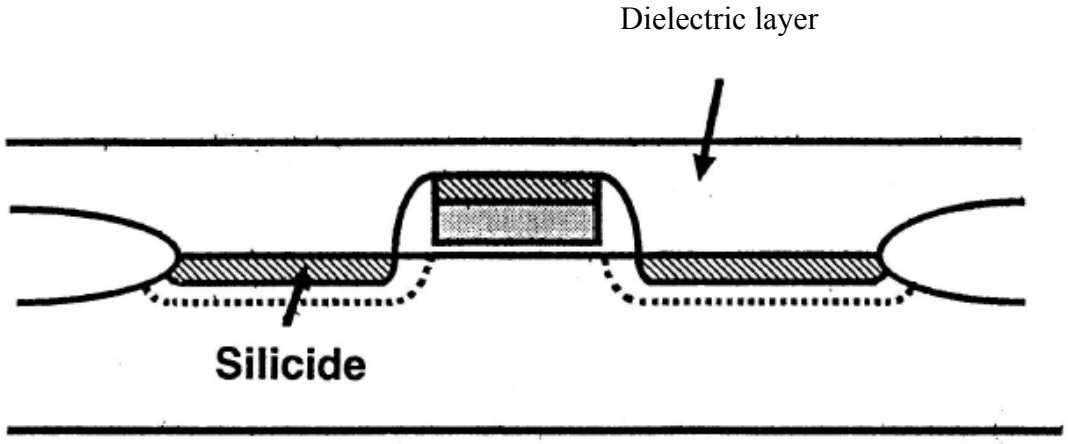


Figure 1.10 cross-sectional image of a MOSFET with the self-aligned silicide (SALICICE).

As far as the parasitic resistance of MOSFETs along the gate electrode is concerned, reduction of the gate electrode resistance is important, because it influences the speed of charge/discharge of the gate electrode. In order to reduce the resistance, self-aligned silicide is also very effective.

1.3.2 Schottky MOS transistor

Other than the application of the metal silicide to MOSFETs mentioned above, Schottky transistors [1.19, 1.20] have been proposed. In these devices, metal silicides are formed not on heavily-doped source/drain diffusion layers but directly on Si substrate. Therefore, in these devices, metal silicides form a Schottky junction in source/drain with rectifying electrical characteristic, which is explained in the next section. For example, N-type MOSFETs use silicide/p-type Si source/drain. Metal silicide with large Schottky barrier height to p-type is used in order to cut off the leakage current under null or negative gate voltages. Once positive gate voltage is applied and the n-channel under the gate is formed, large drain current starts to flow because the metal silicide has small barrier height to n-type silicon. The operation mechanism for P-type device is totally opposite. N-type channel and metal silicide with large Schottky barrier height to n-type are used in this device. Schottky MOSFETs have several advantages to the conventional MOSFETs, such as smaller parasitic resistance, low-temperature process capability, and elimination of parasitic bipolar action. [1.21]

1.3.3 Principle of the Schottky junction

The junctions between a metal and a semiconductor find numerous applications in microelectronic devices. The semiconductor industry has been using for several decades metallic junctions with heavily doped semiconductor, for the electric contacts between the semiconductor regions and the copper wires in integrated circuits as mentioned in a previous section.

In the case of metal and silicon contact, the potential that is called Schottky barrier

height is formed at metal/silicon interface and this shows rectifying characteristics similar to the pn junction. Supposing the work function of metal is ϕ_m and the electron affinity is χ, . the schottky barrier height is calculated as in the following equation:

$$\phi_B = \phi_m - \chi \tag{1.5}$$

Theoretically, electrons should flow through or over this potential barrier. But, in fact the schottky barrier heights are measured and it is revealed that they do not follow the metal work function dependence shown in the equation (1.5). In general, the dependence on work function is much smaller than that in equation (1.5). That reason for this is believed to be the existence of interfacial trap and interfacial layer.

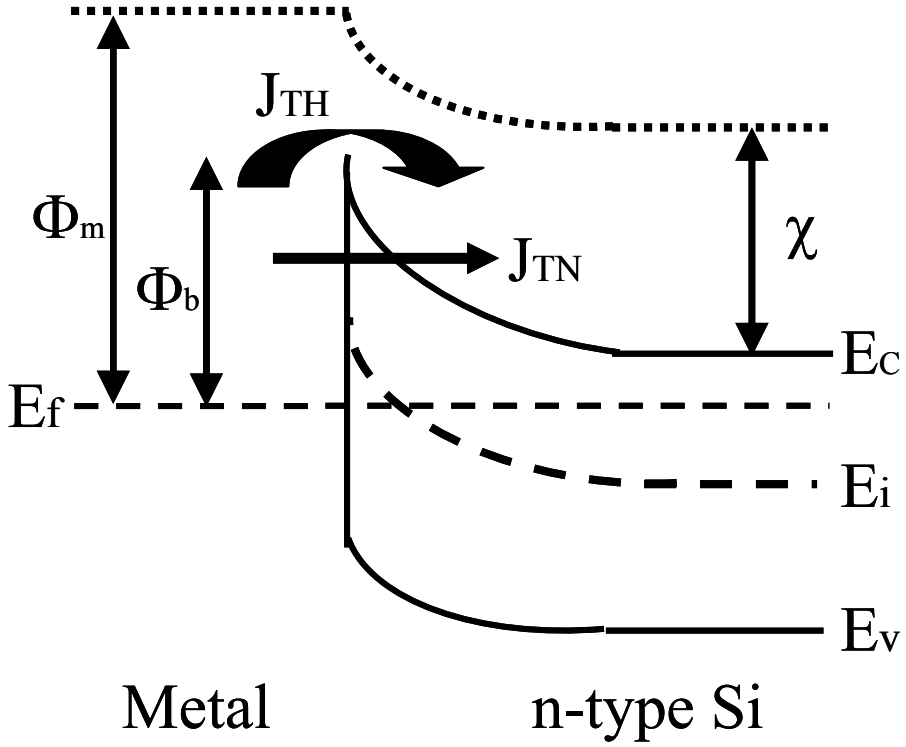


Figure 1.11 schematic illustration of Schottky diode band diagram

A lot of models are suggested in relationship among Fermi level pinning. In any cases, when reverse bias is applied to the Schottky junction, the electron transportation includes that of thermal electron emission over the potential barrier J_{TH}, and tunneling component through Schottky potential barrier J_{TN} as shown in Figure 1.11.

1.3.4 S parameters of Schottky junction and the effect of the surface states

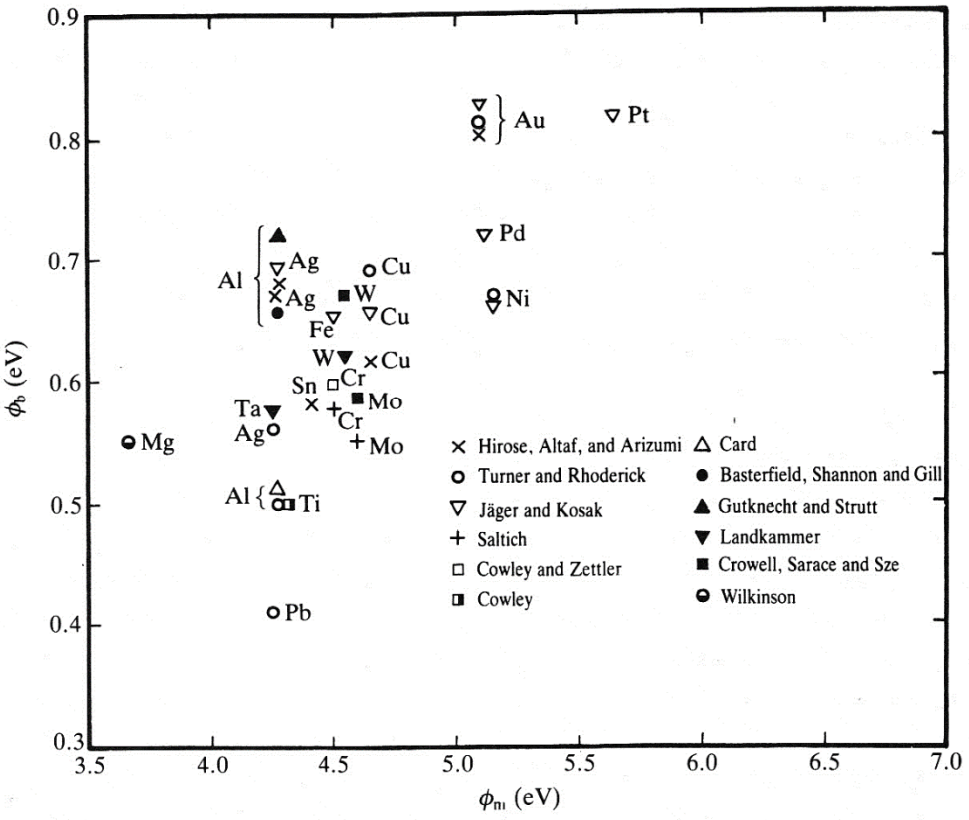


Figure 1.12 Dependence of Schottky barrier height to n-Si on the metal work function. [1.22]

Figure 1.12 shows the dependence of Schottky barrier height to n-Si on the metal work function. [1.22] This figure indicates that Schottky barrier heights do not follow the values predicted by eq.(1.5). Kurtin et al. analyzed a large set of relationship

between Schottky barrier height and metal work function and extracted the following linear equation [1.23] :

$$\phi_B = S(\phi_m - \chi) + C \tag{1.6}$$

, where S is slope factor and C is a constant. S is sometimes called S parameter.

According to Figure 1.12, S parameter wou1.5ld be around 0.2-0.3 in case of chemically etched Si surface. The crystal configuration in surface semiconductors differs from its bulk structure due to the presence of dangling bonds at the boundaries of the lattice. Within the solid, the electrons are influenced by the periodic electrostatic potential resulting in the energy band configuration with the forbidden energy gap. At the surface, the potential is abruptly terminated and is no longer periodic. The band configuration no longer prevails, which means that electrons can occupy surface states whose wave function decays exponentially from the surface to the bulk (imaginary wave vector k). Some of these states have an energy located within the energy gap.

A simple model associates the surface states to the dangling bonds of the atoms at the surface. The unpaired atomic orbitals can either accept (acceptor states) or give up (donor states) an electron. The occupancy of donor and acceptor states is fully determined by the charge neutrality condition. A neutral level ϕ_0 is usually defined as the position of the Fermi level corresponding to electrical neutrality at the surface (Figure 1.13). The main effect of these surface states to the SBH is to reduce its dependency on the metal workfunction as in eq. (1.6). Bardeen claimed that these surface states located at the Metal/semiconductor junction screen the effect of the metal to the semiconductor.

In the absence of surface states, the negative charge Qm on the surface of the metal

must be equal and opposite to the positive charge Qd due to the uncompensated donors in the depletion region. Due to their nature, surface states can also store charges, modifying the equilibrium situation Qm = Qd. In the Schottky model assuming no effect of the surface states, the Fermi level is located below the neutral level of the surface. On the other hand, in Bardeen model, a positive charge is stored in the surface states and the charge in the depletion region will be reduced accordingly to the neutrality condition. The reduction of the charge in the depletion region pushes the Fermi level towards ϕ_0 and the barrier height is lowered [see Figure. 1.13-(b)]. Similarly, if the Fermi level is located above the neutral level, a negative charge is stored and the increase of the positive charge in the depletion region pushes again the Fermi level towards ϕ_0. Therefore, ϕ_0 acts as an attractor for the Fermi level. In the limit of high surface states density, the SBH remains constant at ϕ_0-χ , no matter how large is the metal work function. In most semiconductors, we see experimental data set show intermediate situation between the two cases.

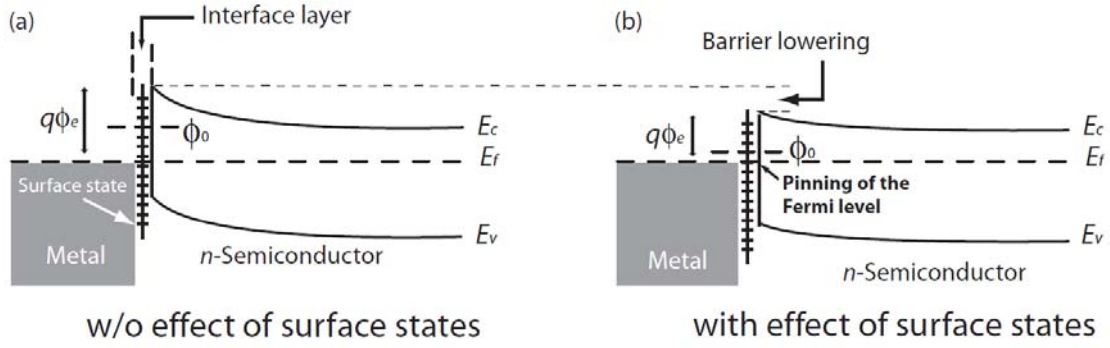


Figure 1.13 Energy band diagram of a Schottky contact without (a) and with (b) the effect of the surface states. The Fermi-level E_f is pushed towards the neutral level ϕ_0.

1.3.5. Schottky barrier modification

As mentioned in the previous section, in order to modify the Schottky barrier height ϕ_B from one end to the other of Si bandgap, we should change the metal work function by the factor of 2 to 3. ErSix [1.16] is used for the realization of ϕ_B of 0.28eV, while PtSi is used for ϕ_B of 0.82eV. [1.24] But for the continuous modification of the Schottky barrier height, changing the silicide material is not very appropriate. Moreover, changing the silicide material by devices in ULSI (for example, N-MOS and P-MOS) is not a convenient way as far as the ULSI manufacturing process is concerned. Therefore, impurity segregation method, in which specific impurities such as As, P and B are segregated, is proposed. [1.25] Impurities in Si are segregated at the silicide-Si interface during the silicidation reaction and these unique peak regions could modify the Schottky barriers. This technique provides continuous modification of Schottky barriers using one kind of silicide in ULSIs.

1.3.6. Semiconducting Silicides

Metal silicides and their application to ULSIs have been introduced, so far. However it is well-known that there are several semiconducting silicides. These silicides are listed in Figure 1.14.[1.26]

Inside the list, numbers in each section represent bandgap of materials. These range from 0.1-1.8eV, indicating these materials have semiconducting properties. These silicides have been intensively investigated as materials applied to photovoltaic devices and thermoelectric devices. [1.26]

	I	II	III	IV	V	VI	VII	VIII		
1	H							He		
2	Li	Be	B	C	N	O	F	Ne		
3	Na	Mg Mg_2Si 0.78 eV	Al	Si	P	S	Cl	Ar		
4	K Cu	Ca Zn	Sc Ga	Ti Ge	V As	Cr $CrSi_2$ 0.35 eV Se	Mn $MnSi_{2-x}$ 0.7 eV Br	Fe $FeSi_2$ 0.78 eV Kr	Co	Ni
5	Rb Ag	Sr Cd	Y In	Zr Sn	Nb Sb	Mo $MoSi_2$ 0.07 eV Te	Tc I	Ru Ru_2Si_3 0.8 eV Xe	Rh	Pd
6	Cs Au	Ba $BaSi_2$ 1.3 eV Hg	La → Lu Tl	Hf Pb	Ta Bi	W WSi_2 0.07 eV Po	Re $ReSi_{1.75}$ 0.12 eV At	Os OsSi 0.34 eV Os_2Si_3 2.3 eV $OsSi_2$ 1.8 eV Rn	Ir Ir_3Si_5 1.2 eV	Pt
7	Fr	Ra	Ac → Lr	Ku	Ns					

$MnSi_{2-x}$: $Mn_{11}Si_{19}$ ($MnSi_{1.727}$), $Mn_{26}Si_{45}$ ($MnSi_{1.730}$), $Mn_{15}Si_{26}$ ($MnSi_{1.733}$), $Mn_{27}Si_{45}$ ($MnSi_{1.741}$), Mn_4Si_7 ($MnSi_{1.750}$)

Figure 1.14 Semiconducting silicide are listed as in the periodic table. Numbers inside each section represent bandgap of silicide.[1.26]

1.3.7 Tunnel FET with semiconducting silicides

As mentioned in section 1.2.3 (Tunneling FET), hetero-junction source/channel structure [1.14] is investigated in order to boost the drain current of the device, which suffers from the lack of the drivability. In most of the case, the hetero-junction consists of the III-V semiconductors with only exception of GeSi(Ge)/Si [1.13]. Recently, III-V semiconductor MOSFET technology has been developed intensively with a hope of the future application to high-speed, low power consumption MOSLSIs, however there are still several issues to be solved in fields such as metal gate/high-k/III-V semiconductor gate stack formation with small EOT (ex. Less than 1nm), low gate leakage and good interface integrity. In addition to that, metal contact formation with low parasitic resistance should be accomplished. On the other hand, GeSi(Ge)/Si hetero-junciton does

not provide large drain current enough to compete with the conventional MOSFETs. Therefore, Si based tunneling FETs with appropriate hetero-junction structure which could provide a large drain current is desired. Since some semiconducting silicides have smaller bandgap than that of Si and moreover they can form hetero structure desirable for the large tunneling probability [1.27], a study on the semiconducting silicide application to Si-based tunneling FETs is important.

1.4 Objective and outline of this thesis

As mentioned in this chapter, MOSFETs have been developed in accordance with the scaling law in order to enhance the device speed and reduce their power consumption during the operation. Scaling law requires the reduction of the supply voltage of MOSFETs, however recently the subthreshold leakage started hindering this trend. Therefore steep subthreshold FETs have been intensively investigated. Among a few candidates for the steep subthreshold FETs, tunneling FET is a most promising one due to its simple structure and its capability of the drain voltage reduction. Therefore, it is very important to conduct a research on tunneling FETs especially in terms of their on-state and subthreshold characteristics. On the other hand, Si base technology is still prevailing in ULSI field even with an intensive work all over the world for the development of III-V semiconductors. Therefore, Si-based tunneling FET could be one promising solution for the drastic power consumption reduction of the ULSI chips. Concerning all of these backgrounds, I conducted the research on a study on process and device structure impact on Silicide-Silicon Schottky or Heterojunction Tunnel FET characteristics. This thesis consists of 7 chapters as listed in Figure 1.15.

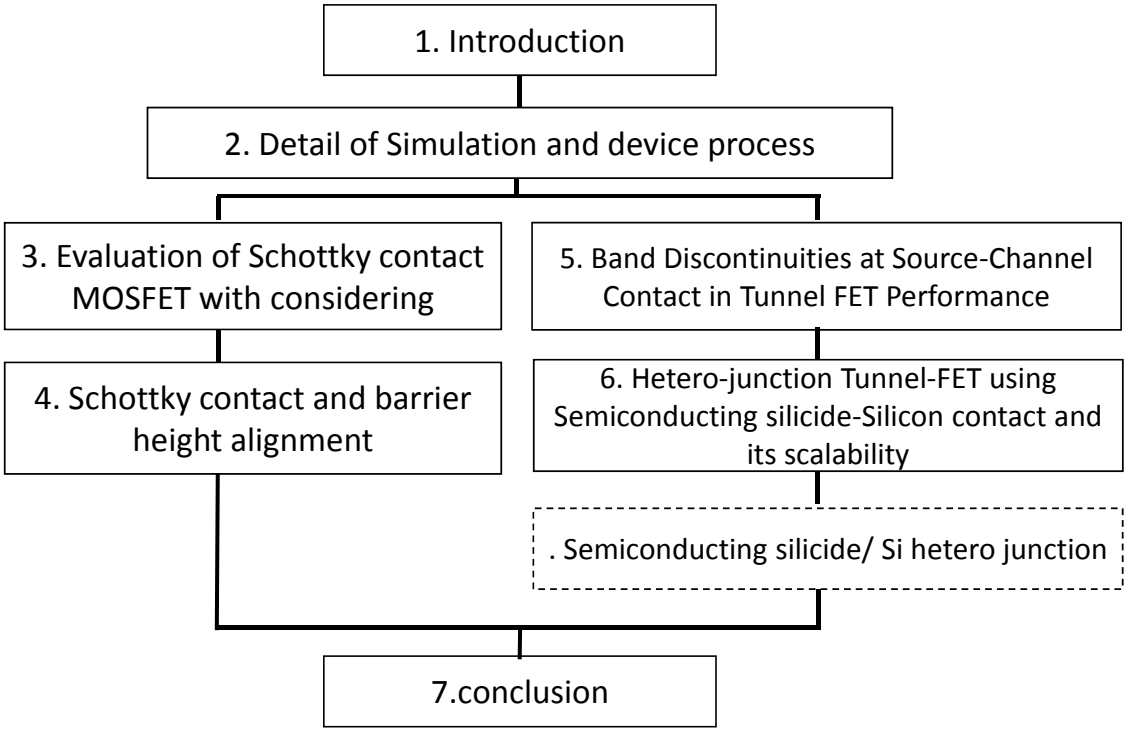


Figure 1.15 Chapter structure of this thesis.

In chapter 2, basic carrier transportation models inside the simulation tool SILVACO, which is used in this study for the extraction of the electrical characteristics and its dependence on the device fine structures, are explained. Moreover experimental setups and analyzing tools used for the study on a novel silicide formation process using annealing of metal/silicon thin film stack structure are introduced.

In chapter 3, the influence of structural parameters, including the Schottky barrier height, channel doping, on the electrical characteristics of a scaled Schottky barrier tunneling FET have been clarified by the device simulation.

In chapter 4, a novel silicide formation process using annealing of metal/silicon thin film stack structure is proposed as the suitable process for these devices. It is realized that an atomically flat interface and surface are formed. This stacked silicide formation

process could achieved ideal diode characteristics and robust Schottky barrier and *n*-factor against the subsequent annealing because of formation of an atomically flat interface. It is also obtained that the significant amount of the impurity incorporation at the silicide-Si interface could modify and control the Schottky barrier height.

In chapter 5, the influence of valence band discontinuity at source and channel interface on device performance of tunneling FET are revealed by the device simulations. A steep slope with high I_{ON} can be both achieved with larger discontinuity, owing to reduced tunneling distance and lower energy barrier for tunneling.

In chapter 6, silicon-based tunneling FET using semiconducting silicide Mg_2Si/Si source-channel hetero-junction is proposed and the device simulation has been presented. With narrow bandgap of silicides and the conduction and valence band discontinuous at the hetero-junction, larger drain current and smaller subthreshold swing than those of Si homo-junction TFET can be obtained. Finally in chapter 7, this thesis is summarized.

1.5 References of this chapter

[1.1] R.H. Dennard, F.H. Gaenesslen, H.N. Yu, V.L. Rideout, E. Bassous, A.R. Le Blanc, “Design of Ion-Implanted MOSFETs with very small physical dimensions”, IEEE J Solid State Circuits” 1974;SC-9;256.

[1.2] Taylor GW, “The effect of two dimensional charge sharing on the above-threshold characteristics of short-channel IGFET”, 1979;22;701-719.

[1.3] K.K. Ng and W.T. Lynch, “The impact of intrinsic series resistance on MOSFET scaling” IEEE Trans. Electron Devices 34(1987), 503.

[1.4] K.Maex, ” Silicides for integrated circuits: $TiSi_2$ $CoSi_2$” Mater. Sci. Eng.

R11(1993), 53.

[1.5] T. Morimoto, T. Ohguro, H. S. Momose, T. Iinuma, I. Kunishima, K. Suguro, I. Katakabe, H. Nakajima, M. Tsuchiaki, M. Ono, Y. Katsumata, and H. Iwai, "Self-Aligned Nickel-Mono-Silicide Technology for High-Speed Deep Submicrometer Logic CMOS ULSI," IEEE Trans. Electron Devices, vol. 42, pp.915-922 , May 1995

[1.6] K.Gopalakrishnan, P.B. Griffin, and J.D. Plummer, "Impact Ionization MOS (I-MOS) – Part I: Device and. Simulation,"IEEE Trans. Electron Dev., 52(2005), 69.

[1.7] K.Gopalakrishnan, R.Woo, C.Jungemann, P.B. Griffin, and J. D.Plummer, IEEE Trans. Electron Dev., "Impact Ionization MOS (I-MOS)—Part II: Experimental Results" 52(2005), 77.

[1.8] M.T. Bjoerk, O.Hayden, H.Schmid, H.Riel, and W. Riess, "Vertical surround-gated silicon nanowire impact ionization field-effect transistors" Appl.Phys.Lett., 90(2007), 142110.

[1.9] E.-H. Toh, G. H. Wang, G.-Q. Lo, L. Chan, G. Smaudra, and Y.-C. Yeo, "Performance enhancement of n-channel impact-ionization MOS (I-MOS) transistor by strain engineering," Appl. Phys. Lett., 90(2007), 023505

[1.10] E.-H. Toh, G. H. Wang, L. Chan, G.-Q. Lo, G. Smaudra, and Y.-C. Yeo, I-MOS transistor with an elevated silicon-germanium impact-ionization region for bandgap engineering," IEEE Electron Dev.Lett, 27(2006), 975.

[1.11] A. Padilla, C. W. Yeung, C. Shin, C. Hu, and T. Liu "Feedback FET: A Novel Transistor Exhibiting Steep Switching Behavior at Low Bias Voltages" IEDM Tech. Dig., pp. 1 (2008).

[1.12] W.Y. Choi, B.-G. Park, J. Duk, and T.-J. King, "Tunneling Field Effect Transistor (TFETs) With Subthreshold Swing (SS) Less Than 60 mV/dec",IEEE Electron Dev.Lett,

28(2007), 743

[1.13] T. Krishnamohan, D. Kim, S. Raghunathan, K. Saraswat, “Douple-gate strained-Ge heterostructure tunneling FET (TFET) with record high drive current and <60mV/dec subthreshold slope”, IEDM Tech. Dig.:2008: 947-950.

[1.14] D. Mohata, S. Mookerjea, A. Agrawal, Y. Li, T. Mayer, V. Narayanan, A. Liu, D. Loubychev, J. Fastenau, and Su. Datta, “Experimental staggered-source and N+ pocket-doped channel III-V tunneling field-effect transistors and their scalabilities”, App.Phys.Exp.;2011;4;024105.

[1.15] H.M. Fahad, and M.M. Hussain, ” High-Performance Silicon Nanotube Tunneling FET for Ultralow-Power Logic Applications” IEEE Trans. Electron Dev., 60(2013), 1034.

[1.16] N. Reckinger, X. Tang, V. Bayot, D.A. Yarekha, E. Dubois, S. Godey, X. Wallart, G. Larrieu, A. Laszcz, J. Ratajczak, P.J. Jacques, and P.Raskin, J.Appl.Phys., “Low Schottky barrier height for ErSi2−x /n-Si contacts formed with a Ti cap” 104(2008), 103523.

[1.17] T. Kato, Y. Sago, H. Fujiwara, “Optoelectronic properties of Mg2Si semiconducting layers with high absorption coefficients” J. Appl. Phys., 110(2011), 063723.

[1.18] S.J. Clark, H.M. Al-Allak, S. Brand, and R.A. Abram, “Structure and electronic properties of $FeSi_2$” Phys Rev. B58(1998), 10389.

[1.19] K. Ikeda, Y. Yamashita, A. Endoh, T. Fukano, K. Hikosaka, and T. Miura, “50-nm gate Schottky source/drain p-MOSFETs with a SiGe channel” IEEE Electron Device Lett., 23(2002), 670.

[1.20] W. Saitoh, A. Itoh, S. Yamagami, and M. Asada, “Analysis of Short-Channel

Schottky Source/Drain Metal-Oxide-Semiconductor Field-Effect Transistor on Silicon-on-Insulator Substrate and Demonstration of Sub-50-nm n-type Devices with Metal Gate" Jpn. J. Appl. Phys., 38(1999), 6226.

[1.21] M. Sugino, L.A. Akers and M.E. Rebeschini, "Latchup-free Schottky-barrier CMOS", IEEE Trans. Electron Devices, 30, (1983) 110.

[1.22] E.H. Rhoderick and R.H. Williams, Metal-Semiconductor Contacts (2nd edition), Oxford Science Publication.

[1.23] S. Kurtin, T.C. McGill, and C.A. Mead, "FUNDAMENTAL TRANSITION IN THE ELECTRONIC NATURE OF SOLIDS" Phys.Rev.Lett., 22(1969), 1433.

[1.24] H. Jaeger, and W. Kosak, Solid State Electron, "'MODULATION EFFECT BY INTENSE HOLE INJECTION' IN EP1TAXIAL SILICON SCHOTTKY-BARRIER-DIODES", 12(1969), 511.

[1.25] G. Larrieu and E. Dubois, IEEE Electron Device Lett, "CMOS Inverter Based on Schottky Source–Drain MOS Technology With Low-Temperature Dopant Segregation" ,32(2011), 728.

[1.26] V.E. Borisenko (Ed.) 'Semiconducting Silicides' , Springer series in Material Science 39.

[1.27] Y. Wu, H. Hasegawa, K. Kakushima, K. Ohmori, H. Wakabayashi, K. Tsutsui, A.Nishiyama, N. Sugii, Y. Kataoka, K. Natori, K. Yamada' and H. Iwai' "Influence of Band Discontinuities at Source-Channel contact in Tunnel FET Performance" Proceedings of 2013 International Workshop on Dielectric Thin Films, Tokyo, 2000

Chapter 2

Detail of Simulation and Device Process

2.1 Fabrication procedure

Figure 2.1 shows fabrication procedure of Schottky diodes. The diodes were fabricated on *n*-type (100)-oriented Si substrate. The substrate impurity concentration is 3 x 10^{15} cm^{-3}. To determine the diode area, 400nm thermal oxide was formed, patterned by photolithography and etched SiO_2 by buffered HF (BHF). After SPM cleaning and HF treatment, thermal oxidation was performed because of protecting Si surface from resists and developers. Lift-off patterning and HF treatment due to removing SiO_2 formed by thermal oxidation were performed. Metal layer was deposited by RF sputtering. Metal which exists at excess area was removed by lift off process. An Al film was formed as a back contact by thermal evaporation. Rapid thermal annealing (RTA) in N_2 ambient was performed due to silicidation.

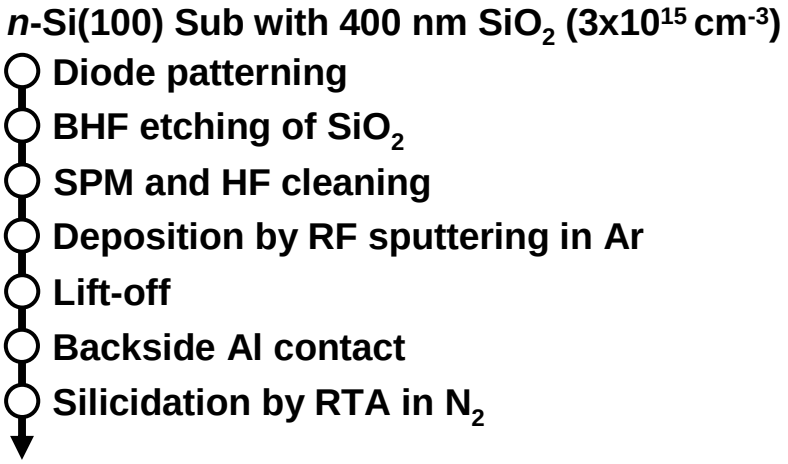


Figure 2.1 Fabrication flow of Schottky diode.

2.2 Experimental details

2.2.1 SPM cleaning and HF treatment

Particles and organic substance at the surface of Si substrate become a cause of false operation. Therefore, it is important to clean the surface of Si substrate. SPM cleaning is one of the effective cleaning methods. The cleaning liquid is made from H_2O_2 and H_2SO_4 (H_2O_2:H_2SO_4 = 1:4). Because of its oxidizability, particles and organic substance are oxidized and separated from the surface of Si substrate. However, the surface of Si substrate is oxidized and SiO_2 is formed during SPM cleaning. 1% HF is used to eliminate the SiO_2.

2.2.2 RF magnetron sputtering

Metal is deposited by radio frequency (RF) magnetron sputtering with Ar gas. An RF with 13.56 MHz is applied between substrate side and target side. Because of the difference of mass, Ar ions and electrons are separated. A magnet is set underneath the target, so that the plasma damage is minimized. Electrons run through the circuit from substrate side to target side, because substrate side is subjected to be conductive and target side is subjected to be insulated. Then, target side is negatively biased and Ar ions hit the target.

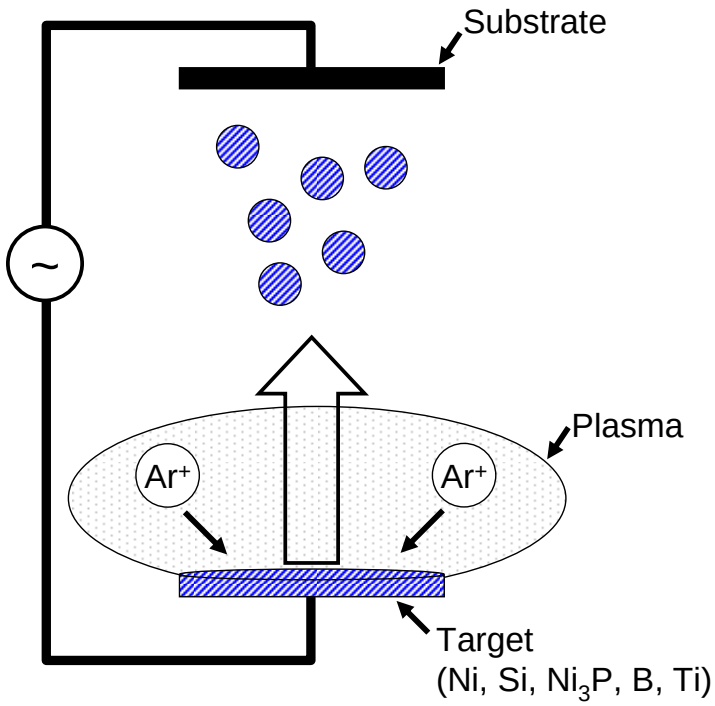


Figure 2.2 Schematic illustration of RF magnetron sputtering.

2.2.3 Lift-off process

Lift-off is the process which selectively removes deposited films. Following photolithography and deposition, resists and deposited films which exist on excess area are left by ultrasonic cleaning with acetone.

2.2.4 Vacuum evaporation for Al deposition

Al for wiring and backside contact is deposited by vacuum evaporation. Al source is set on W boat and heated up to boiling point of Al by joule heating. However, melting point of W is higher than boiling point of Al, W boat doesn't melt. The base pressure in the chamber is maintained to be 10^{-3} Pa (Figure 2.3).

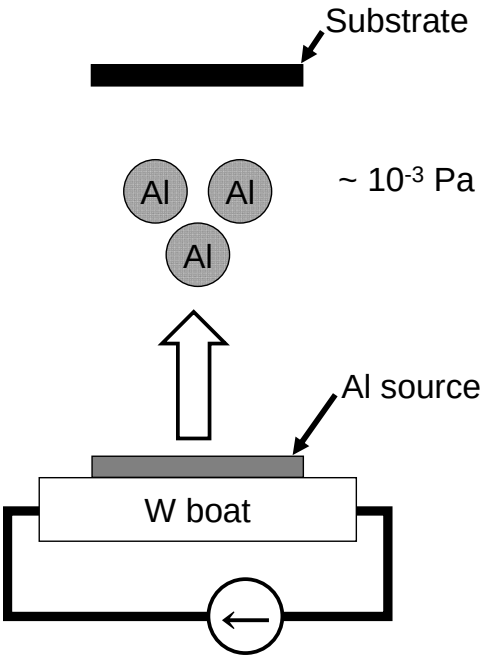


Figure 2.3 Schematic illustration of vacuum evaporation.

2.2.5 Rapid thermal annealing (RTA)

Rapid thermal annealing (RTA) is performed for silicidation. Heating chamber is filled with N_2 to interfere with oxidation. In this study, the time of elevated temperature is 30 seconds and the time of annealing is 1 minute.

A schematic illustration of Schottky diode fabrication process is shown in Figure 2.4.

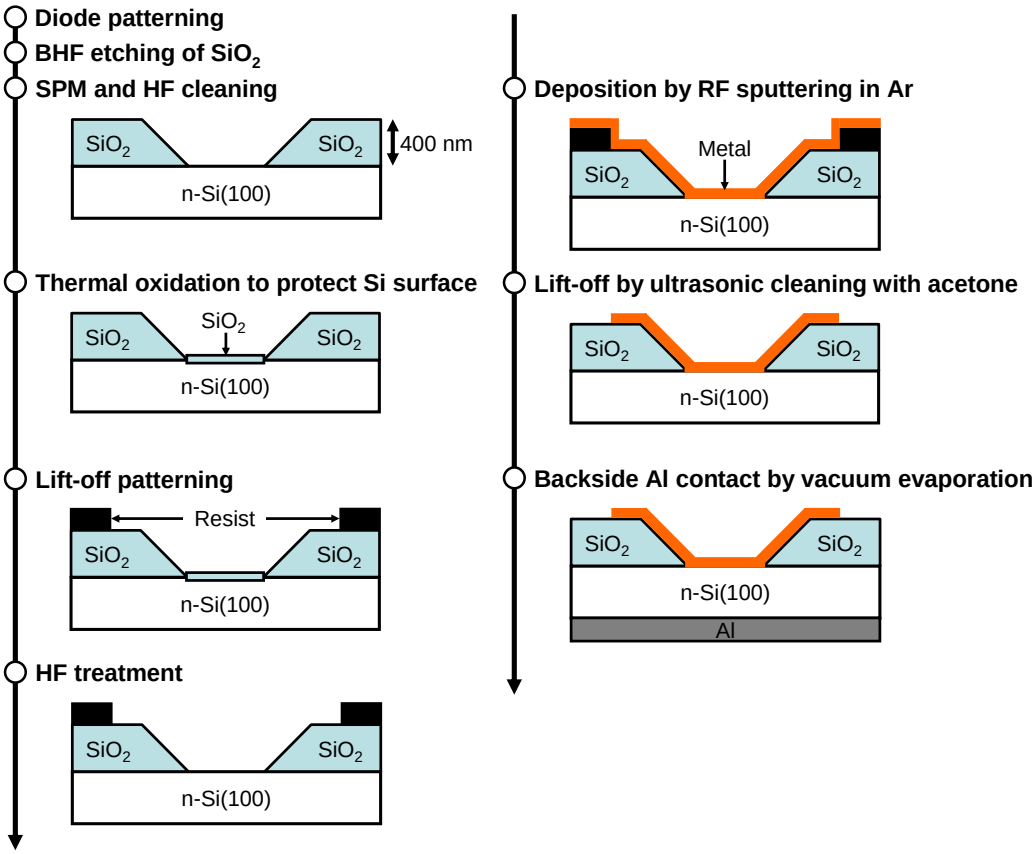


Figure 2.4 Schematic illustration of Schottky diode process.

2.3 Electrical characterization of Schottky diode

Schottky diode characteristics are evaluated by *J*-*V* characteristics, ϕ_B and *n*-factor. ϕ_B and *n*-factor can be extracted by fitting with ideal *J*-*V* curve. In this study, for analyzing Schottky diode characteristics, image force lowering and thermionic emission are considered [2.1]. In this chapter, Schottky diodes of metal (silicide) and *n*-Si contacts are discussed.

2.3.1 Metal-silicon contact

When metal and silicon contact, these must share the same free electron level at the interface [2.2]. Also, at thermal equilibrium or when there is no net electron or hole current through a system, the Fermi level of the system is spatially constant. These two factors lead to the band diagram as shown in Figure 2.5 for a metal-*n*-Si contact at thermal equilibrium. Considering free electron energy level, Schottky barrier height for electron (ϕ_{Bn0}) is given by

$$q\phi_{Bn0} = q(\phi_m - \chi) \tag{2.1}$$

where ϕ_m is the metal work function and χ is the electron affinity of silicon.

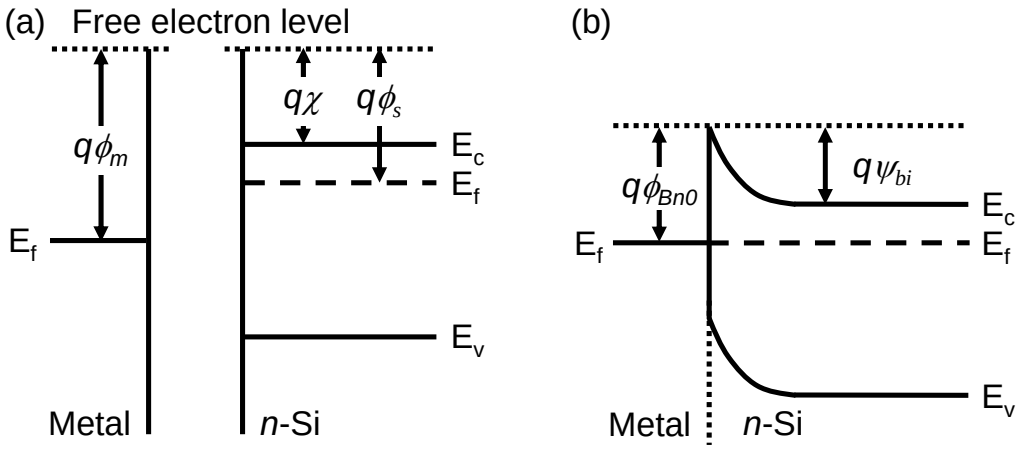


Figure 2.5 Band diagram of metal-n-Si contact. (a) When the metal and the Si are far apart. (b) When the metal is in contact with the Si. ψ_{bi} is built-in potential.

2.3.2 Image-force lowering

Image-force lowering is the image-force-induced lowering of the barrier energy for charge carrier emission [2.2]. Image-force lowering ($\Delta\phi$) for the metal-Si contact is

$$\Delta\phi_{Bn0} = \sqrt{\frac{qE_m}{4\pi\varepsilon_{Si}}} \tag{2.2}$$

where E_m is maximum value of electric field and ε_{Si} is the Si permittivity. Therefore, Schottky barrier height (ϕ_{Bn}), considering image-force lowering, is given by

$$q\phi_{Bn} = q(\phi_{Bn0} - \Delta\phi) \tag{2.3}$$

as shown in Figure 2.6.

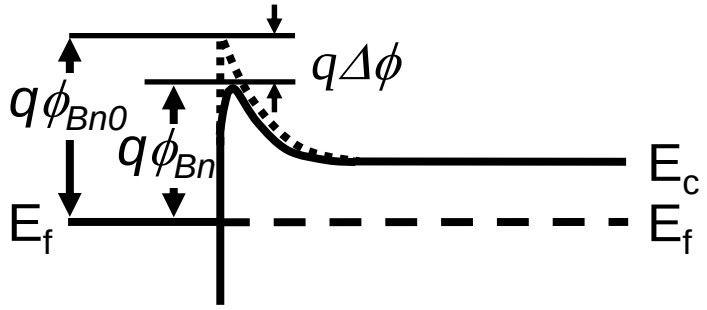


Figure 2.6 Band diagram of metal-n-Si contact incorporating image-force lowering.

2.3.3 Thermionic emission

In thermionic emission, the simplest theory is to deal with the electron as an ideal gas that follows Boltzman statistics in energy distribution [2.1]. The electron emission current from Si into metal ($J_{s\rightarrow m}$) is given by

$$I_{s\rightarrow m} = A^{*}T^{2}\left[-\exp\left(\frac{\phi_{Bn0}}{kT}\right)\right]\left[\exp\left(\frac{qV}{nkT}\right)\right] \tag{2.4}$$

where A^{*} is effective Richardson's constant, n is ideality factor (n-factor) and V is applied voltage. On the other hand, the electron emission current from metal into Si ($J_{m\rightarrow s}$) is

$$I_{m-s} = A^{*}T^{2}\left[-\exp\left(\frac{\phi_{Bn0}}{kT}\right)\right] \tag{2.5}$$

Therefore, the total current J_{n0} is given by

$$I_{n0} = A^{*}T^{2}\left[-\exp\left(\frac{\phi_{Bn0}}{kT}\right)\right]\left[\exp\left(\frac{qV}{nkT}\right)-1\right] \tag{2.6}$$

With an addition of image-force lowering, total current J_n is

$$I_{n} = A^{*}T^{2}\left[-\exp\left(\frac{\phi_{Bn0}-\Delta\phi}{kT}\right)\right]\left[\exp\left(\frac{qV}{nkT}\right)-1\right] - A^{*}T^{2}\left[-\exp\left(\frac{\phi_{Bn}}{kT}\right)\right]\left[\exp\left(\frac{qV}{nkT}\right)-1\right] \tag{2.7}$$

as shown in Figure 2.7. ϕ_{Bn} and *n*-factor are extracted by fitting measurement data and (2.7).

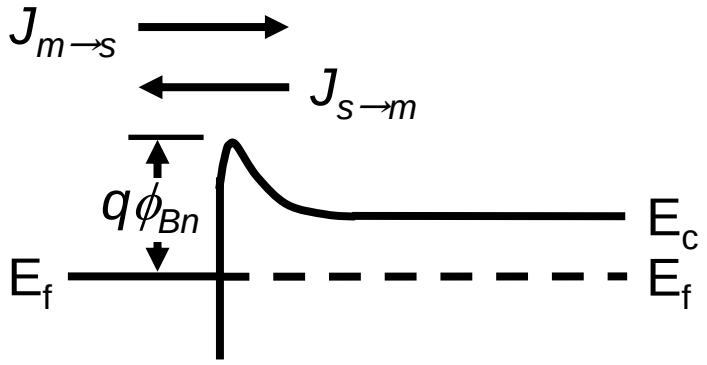


Figure 2.7 Band diagram of metal-n-Si contact incorporating image-force lowering to show the thermionic emission current.

2.4 Detail of models in 2-D device simulation used in this thesis

MOSFET with Schottky and band to band tunneling mechanism is modeled in the 2-dementional device simulator ATLAS by SILVACO Inc. It is considered by Matsuzawa and Ieong's Schottky tunneling model [2.4, 2.5] and Kane's band to band tunneling model [2.3]. Tunneling rates using this model is calculated for silicon , silicide and germanium then put into ATLAS for each material contact tunneling simulations.

2.4.1 Mobility model

To obtain accurate results for MOSFET simulations, need to account for the mobility degradation that occurs inside inversion layers. The degradation normally occurs as a result of the substantially higher surface scattering near the semiconductor to insulator interface.

The inversion layer model from Lombardi (CVT) is selected in this simulation. In the CVT model, the transverse field, doping dependent and temperature dependent parts of the mobility are given by three components that are combined using Matthiessen's rule. These components consists of the impurity scattering μ_{AC}, the phonon scattering μ_b , and the surface roughness scattering μ_{sr} as in the following equation:

$$\mu_T^{-1} = \mu_{AC}^{-1} + \mu_b^{-1} + \mu_{sr}^{-1} \qquad (2.8)$$

2.4.2 Current model through Schottky barrier

Current through the Schottky barrier consist of two injection current models: Thermionic (I_{TH}), tunneling (I_{TN}) injection. Figure 2.8 [2.6] shows the electron tunneling current is represented by localized tunneling rates at grid locations near the Schottky contact. The key feature of the model is that tunneling current through the barrier is converted into a local generation or recombination process where the local rate, G_T (T), depends on the local Fermi-level, ϕ_n and the potential profile along the tunneling path. This is possible because the tunneling integral over distance and energy can be transformed into a double integral over distance alone.

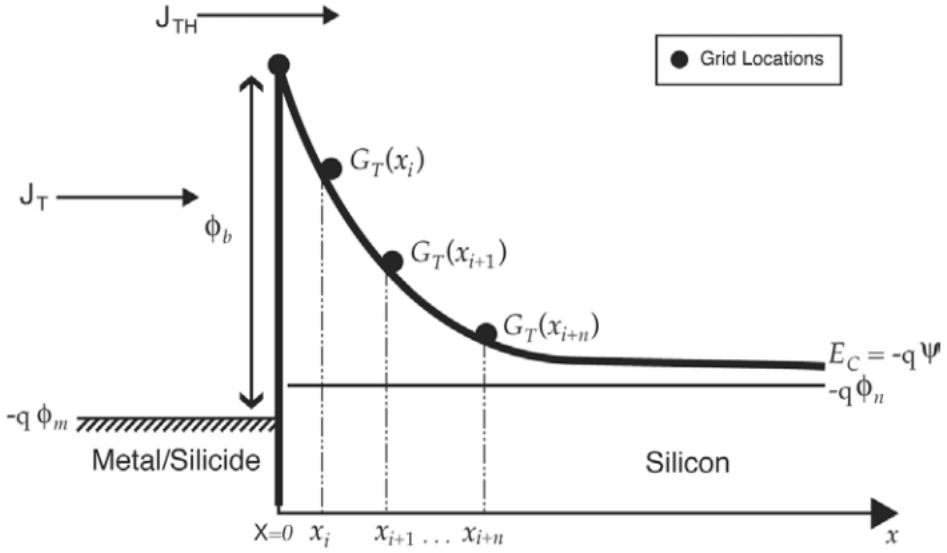


Figure 2.8 Local tunneling generation rate representation of the universal Schottky tunneling model

The local generation rate associated with the tunneling can be related to the local tunneling current (J_T)

$$J_T = \frac{A^* T}{k} \int_E^{\infty} T(E') \ln\left[\frac{1+f_s(E')}{1+f_m(E')}\right] dE' \qquad (2.8)$$

Here, J_T is the tunneling current density, A* is the effective Richardson's coefficient, TL is the temperature, T(E) is the tunneling probability, $f_s(E)$ and $f_m(E)$ are the Maxwell-Boltzmann distribution functions in the semiconductor and metal and E is the carrier energy.

The G_T is the localized tunneling rate which applying by the transformation

$$G_T = \frac{1}{q} \nabla J_T \qquad (2.9)$$

Appling the transformation given in equation 2.8 and 2.9, these can obtain the expression given in next

$$G_T = \frac{A^* T \vec{E}}{k} T(x) \ln\left[\frac{1+n/\gamma_n N_c}{1+\exp[-(E_c - E_{FM})/kT_L]}\right] \qquad (2.10)$$

Here, $\vec{E}$ is the local electric field, n is the local electron concentration, N_c is the local conduction band density of states, γ_n is the local Fermi-Dirac factor, E_c is the local conduction band edge energy and E_{FM} is the Fermi level in the metal.

The tunneling probability $T(x)$ can be described by next

$$T(E) = exp\left[-\frac{2\sqrt{2m^*}}{\hbar}\int_0^{x'}\left(E_c(x') - E_c(x)\right)dx'\right] \qquad (2.11)$$

In equation 2.11, m is the electron effective mass for tunneling, and $E_c(x)$ is the conduction band edge energy as a function of position. Assuming linear variation of each grid location of E_c around.

$$T(E) = exp\left[-\frac{4\sqrt{2m^*}x}{3\hbar}\left(E_F + q\phi_b - E_c(x)\right)^{\frac{3}{2}}\right] \qquad (2.12)$$

ϕ_b is the Schottky barrier height. Similar expression to (2.8) through (2.12) exist for hole.

2.4.3 Band to band tunneling model

Tunneling injection in heavily doped p-n semiconductor junction at high back bias was shown by Zener break down [2.3]. In 1960s, the tunnel diode with the reverse resistivity was published by Dr. Esaki and receive the honor price novel in 1973.

The band-to-band tunneling models described so far in this section calculate a tunneling generation rate at each point based solely on the field value local to that point. For this reason, we refer to them as local models. To model the tunneling process more accurately, you need to take into account the spatial variation of the energy bands. You also need to take into account that the generation/recombination of opposite carrier types is not spatially coincident. Figure 2.9 illustrates this for a reverse biased p-n

junction where it is assumed that the tunneling process is elastic. For degenerately doped p-n junctions, you can obtain tunneling current at forward bias and consequently can obtain negative differential resistance in the forward I-V curve.

In this Tunneling current calculate model considered energy band profile along each tunneling slice with reverse bias applied across the junction. [2.4]The range of valence band electron energies for which tunneling is permitted is shown in the schematic of the energy band profile in Figure 2.9. The highest energy at which an electron can tunnel is E upper and the lowest is E lower. The tunneling can be thought of being either the transfer of electrons or the transfer of holes across the junction. The rates for electrons and holes are equal and opposite because the tunneling results in the generation or recombination of electron-hole pairs.

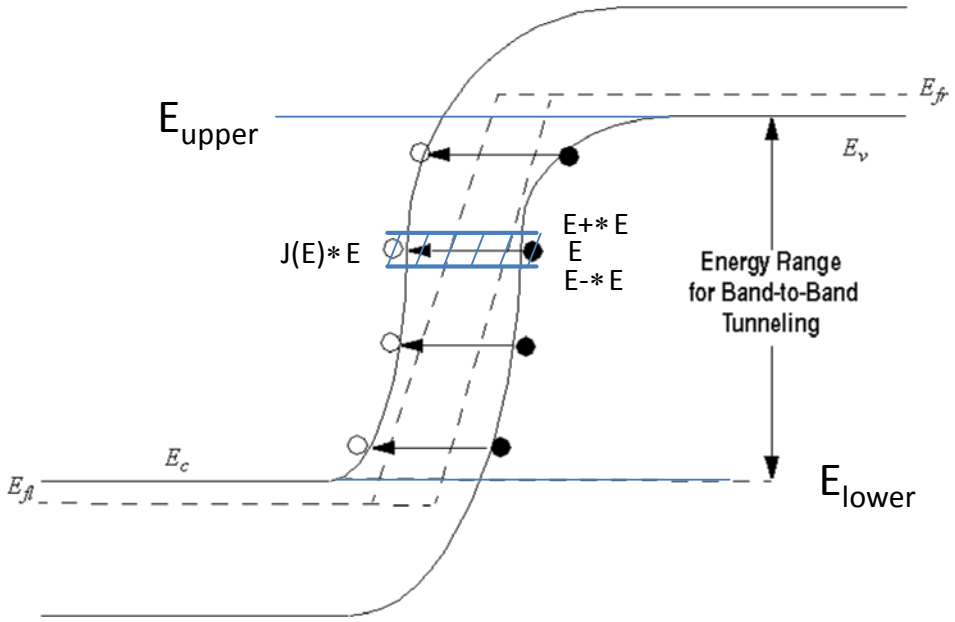


Figure 2.9 Schematic of band to band tunneling in p-n junction reverse bias

The resolution of the tunneling slices in the tunneling direction should also be fine enough to capture these rapid changes. Each tunneling slice must include exactly one

p-n junction for the model to work. The start and end points of the tunnel slices should ideally be in the flat band regions on either side of the junction.

Considering the tunneling process as a transfer of an electron across the junction the net current per unit area for an electron with longitudinal energy E and transverse energy E_T is

$$J(E) = \frac{q}{\pi\hbar}\int\int T(E)[f_l(E+E_T) - f_r(E+E_T)]\rho(E_T)dEdE_T \qquad (2.13)$$

where T(E) is the tunneling probability for an electron with longitudinal energy E.$\rho(E_T)$ is the 2-dimensional density of states corresponding to the 2 transverse wavevector components and

$$f_l = \left(1 + exp\left[\frac{E+E_T-E_{Fl}}{kT}\right]\right)^{-1} \qquad (2.14)$$

is the Fermi-Dirac function using the quasi Fermi-level on the left hand side of the junction. Similarly

$$f_r = \left(1 + exp\left[\frac{E+E_T-E_{Fr}}{kT}\right]\right)^{-1} \qquad (2.15)$$

uses the quasi-Fermi level on the right hand side of the junction. This assumes that the transverse energy is conserved in the tunneling transition. Because we are using a 2-band model to give the evanescent wavevector, the transverse electron effective mass and the transverse hole effective mass are combined in the 2D density of states

$$\rho(E_T) = \frac{\sqrt{(m_e m_h)}}{2\pi\hbar^2} \qquad (2.16)$$

By integrating over transverse carrier energies, we obtain the contribution to the current from the longitudinal energy range E - ΔE/2 to E + ΔE/2 as follows:

$$J(E)\Delta E = \frac{q\sqrt{(m_e m_h)}}{2\pi^2\hbar^3} T(E) \left| ln\left(1 + exp\left[\frac{E_{Fl} - E - E_T}{KT}\right]\right) - ln\left(1 + exp\left[\frac{E_{Fr} - E - E_T}{KT}\right]\right)\right|_0^{E_{max}} \Delta E$$

(2. 17)

where the upper limit of integration, E_{max} is smaller of E - E_{lower} and E_{upper} - E. This is consistent with the 2-band model of the tunneling and the restriction on total carrier energy for tunneling $E_{lower} \leqq E + E_T \leqq E_{upper}$. Putting the above integration limits into Equation (2.17) we obtain

$$J(E) = \frac{q\sqrt{(m_e m_h)}}{2\pi^2\hbar^3} T(E) log\left(\frac{(1+exp[(E_{fr}-E)/KT])(1+exp[(E_{fl}-E-E_{max})/KT])}{(1+exp[(E_{fl}-E)/KT])(1+exp[(E_{fr}-E-E_{max})/KT])}\right)\Delta E \qquad (2.\ 18)$$

The Fermi levels used in Equation (2.18) are the quasi-Fermi levels belonging to the majority carrier at the relevant side of the junction. In Figure 2.9, the start and end points of the tunneling paths, x_{start} and x_{end}, depend on Energy. This model calculates these start and end points for each value of E and calculates the evanescent wavevector at points in between as

$$k(x) = \frac{k_e k_h}{\sqrt{k_e^2 + k_h^2}} \qquad (2.\ 19)$$

where

$$k_e(x) = \frac{1}{\hbar}\sqrt{2m_o m_e(x)(E_C(x) - E)} \qquad (2.\ 20)$$

and

$$k_h(x) = \frac{1}{\hbar}\sqrt{2m_o m_e(x)(E - E_V(x))} \qquad (2.\ 21)$$

This ensures that the energy dispersion relationship is electron-like near the conduction band and hole-like near the valence band, and approximately mixed in between. The tunneling probability, T(E), is then calculated using the WKB approximation

$$T(E) = \exp\left(-2\int_{x_{start}}^{x_{end}} k(x)dx\right) \qquad (2.\ 22)$$

2.5 References of this chapter

[2.1] Y. Taur, T. H. Ning, “Fundamentals of MODERN VLSI DEVICES”, Cambridge University Press (1998).

[2.2] S. M. Sze, Kwok K. NG, “Physics of Semiconductor Devices”, Wiley, New York (2006).

[2.3] E.O.Kane, “Zener tunneling in semiconductors” J.Pyhs. Chem. Solids 12, 181 (1960)

[2.4]Ieong, M., Solomon, P., Laux, S., Wong, H., and Chidambarro, D., "Comparison of Raised and Schottky Source/Drain MOSFETs Using a Novel Tunneling Contact Model", Proceedings of IEDM (1998): 733-736.

[2.5]K. Matsuzawa, K. Uchida and A. Nishiyama “A unified simulation of Schottky and ohmic contacts” IEEE Trans. Electron Devices, **47**, (2000) 103.

[2.6] ATLAS user’s manual by Silvaco Inc

Chapter 3
Influence of Structural Parameters on Electrical Characteristics of Schottky Tunneling FET and its Scalability

3.1 Introduction

As the metal-oxide-semiconductor field-effect transistor (MOSFET) scaling goes down to 10-nm gate length (L_g) region, MOSFETs suffer from severe SCE, losing their gate controllability, which results in threshold voltage (V_{th}) shifts, and an increase in subthreshold swing (SS) to degrade the off-state leakage current (I_{off}), and so on.[3.1] Although the supply voltage (V_{dd}) is expected to be lowered, V_{th} should be redesigned accordingly so as to meet the requirements for on-state drive current (I_{on}). [3.2] [3.3] Therefore, an important task to suppress the I_{off} is to achieve an SS as low as possible by using an extremely scaled gate oxide thickness and/or channel doping optimizations. [3.4] Recently, non-planar MOSFETs, using three dimensional channels, including fins or nanowires, have been focused on as they allow higher gate controllability by wrapping the channel with gate electrodes. [3.5-8] However, even with three dimensional channels, the issue of the lateral spread of on doping profile in the channels near source and drain (S/D) regions is still presented to increase the I_{off} current due to dopant diffusions due to heat treatments. [3.9] Historically, the use of a metal S/D,

especially silicide Schottky barrier S/D MOSFETs (SBFET), has been proposed to solve this issue. [3.10-12] In addition to its atomically abrupt junction formations at silicide and channel interfaces, low parasitic S/D resistance, low-temperature process capability, and elimination of parasitic bipolar action are some of the advantages of SBTFETs. [3.13] Despite these numerous advantages, silicides with proper Schottky barrier height (ϕ_B) for both NMOS and PMOS should be selected since the potential barrier limits the on-state drive current. Commonly, rare-earth silicides, such as YbSi or ErSi with a barrier height of 0.3 eV for electrons (ϕ_{Bn}), have been used for NMOS [3.14] and PtSi with a barrier height of 0.2 eV for holes (ϕ_{Bp}) has been used for PMOS. [3.15, 16] However, compared to MOSFET with a conventionally doped S/D, SBTFETs with smaller ϕ_B or even with a negative barrier height should be achieved to surpass the FET performances. [3.17] In addition, owing to the strong Fermi level pinning of metals on Si substrates, the achievement of a very small or negative ϕ_B has been one of the most difficult challenges for SBFETs. [3.18] On the other hand, beside thermionic emission current (I_{TH}), another important carrier conduction in SBFETs is the tunneling current (I_{TN}) through the silicide and channel barrier. [3.19] Recently, the reduction of SS of MOSFETs by using the band-to-band tunneling current has been investigated[3.20-24] and by enhancing the tunneling current (I_{TN}) in SBFETs, a similar functional advantage is expected. [3.25] [3.26] As the tunneling probability is dependent on the triangular-shape potential determined by a ϕ_B and the channel doping concentration, one may expect better FET performances if proper tunneling parameters are well designed. Therefore, we try to redesign the SBFETs in terms of this aspect and we call the device a SBTFET.

In this chapter, the device simulations have been performed to investigate the influence

of the structural parameters on the electrical characteristics of SBTFETs. The dependence of the characteristics on gate-length scaling have also been investigated, using ϕ_{Bn}, channel doping concentration (N_a), and effective masses (m^*) as parameters. For simplicity, an SBTFET on an SOI wafer is used as a model with a constant gate oxide thickness.

3.2 Simulation and Device Structure

Silvaco TCAD tool ATLAS[3.27] was adopted for the simulation in this study. In this simulation tool, a universal current model including thermionic emission and tunneling components through the Schottky contact, which was verified by the fit to the experimental data[3.19], is implemented. A schematic illustration of the calculated device is shown in Figure 1(a). Subscript Figure 1(b) shows the schematic band structure of p-SOI at the interface with the gate oxide, under ON ($V_G > V_{th}$) and OFF ($V_G < V_{th}$) states. An N-type silicon MOS structure on an SOI wafer with a thickness of 6 nm was used in the present simulation. The silicide-source region was modeled with a source-to-channel Schottky contact. The ϕ_{Bn} at this interface was varied intentionally from 0.21 to 0.81eV, which is practically attainable with various silicides such as $ErSi_2$ (0.28eV) [3.28], $NiSi_2$ (0.66eV) [3.29], and PtSi (0.88eV) [3.30] on Si. On the other hand, the ϕ_{Bn} of silicide at the channel-to-drain region was set to 0 eV. The purpose of this drain structure resides in the elimination of parasitic resistances in this region under ON state as well as the suppression of drain-to-channel hole current, which would increase I_{off}. Electrical characteristics for MOSFET with the conventional S/D were also simulated, assuming an ideal abrupt S/D doping profile.

The gate oxide thickness and the buried-oxide thickness (BOX) were set to 0.3 and 1000 nm, respectively, and the work function of the metal gate was set to 4.8 eV. The gate electrode was overlapped to the source and drain with the overlap distance of 100nm for all simulations.

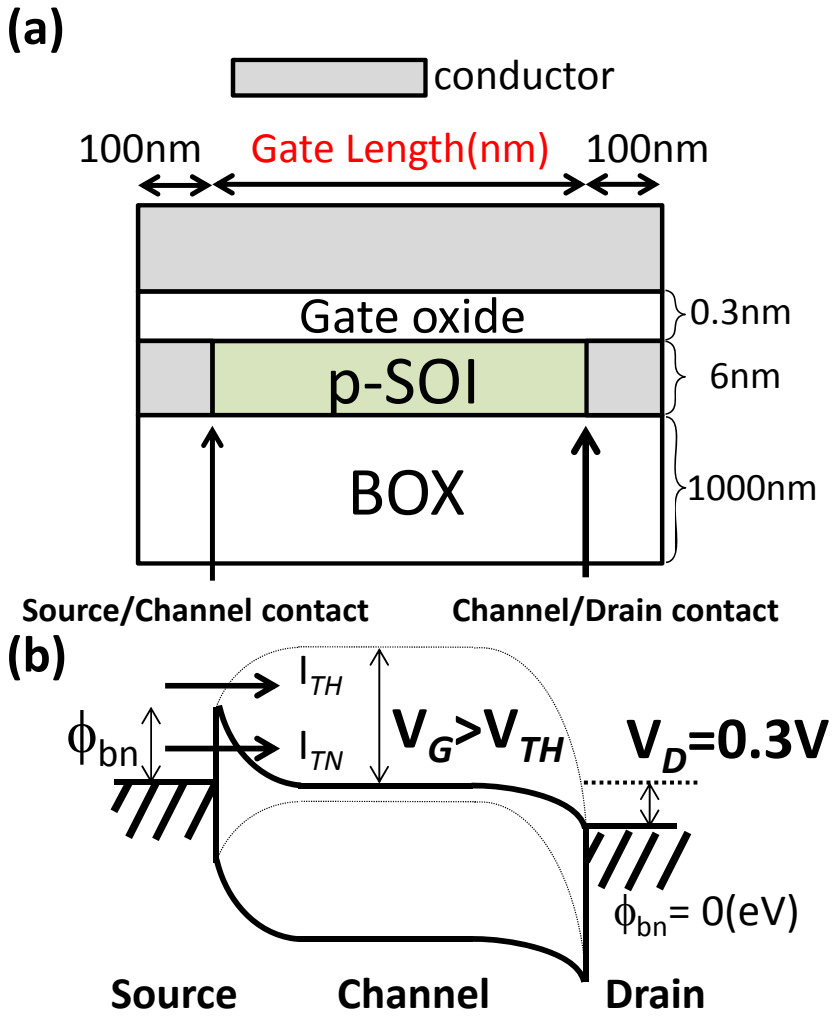


Figure 3.1(a) Schematic device illustration of an SBTFET and (b) schematic band structure of p-SOI at the interface with the gate oxide, under ON ($V_G > V_{th}$: solid line) and OFF ($V_G < V_{th}$: dotted line) states.

N_a was tuned mainly from 5×10^{18} to 2×10^{19} cm^{-3}. m^* was varied from 0.03

to $0.10m_0$, where m_0 is the mass of a free electron. For all N_a value, the SOI layers of the devices are fully depleted when the inversion channel is formed in it. ϕ_{Bn}=0.61eV, N_a=2×10^{19} cm^{-3}, and m^*=$0.08m_0$[31] are used as a default parameter set for both SBTFETs and conventional FETs. Considering the required supply voltage in sub-10 nm FETs, the drain voltage is set to be 0.3 V. Gate length scaling of FET characteristics was carried out in the range of 10 to 50 nm. All simulations were carry out at room temperature.

3.3 Results and Discussion

3.3.1 Structural parameter influence on SBTFET performance

Firstly, the effect of ϕ_{Bn} on the drain current (I_d) and SS for devices with L_g of 50 nm is examined and its gate voltage (V_G) dependency is shown in Figure 2(a) with three different ϕ_{Bn} values (0.41, 0.61, and 0.81 eV). Here, the channel doping was set to 2×10^{19} cm^{-3}. In this figure, dotted lines for the drain current correspond to the I_{TH} component, while the solid lines correspond to the total I_d of the devices. It can be easily expected that the lower the ϕ_{Bn} is, the larger the current is, and this is indeed true in the low V_G region as shown by a dashed line in Figure 2(a). However, when I_{TN} is taken into account, the main current component beyond V_{th} becomes I_{TN}. As the triangular-like potential profile becomes steep with larger V_G, the tunneling probability increases exponentially and most of the carriers can tunnel through the barrier. As a result, the SS at each V_G just below the V_{th}, defined as an I_d of 10^{-7}A/μm at a V_d of 0.3 V, is mostly dominated by I_{TN} and reflects the change in tunneling probability. The ϕ_{Bn} dependency also leads to significant change in SS, where

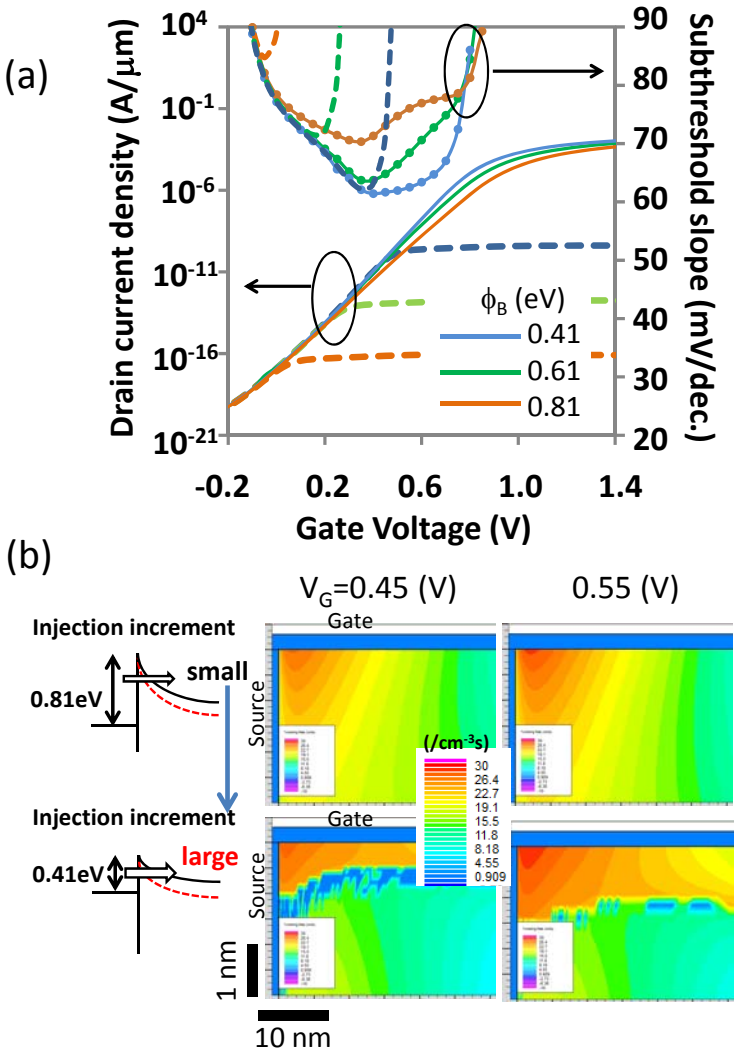


Figure. 3.2 (a) I_d- V_G and SS characteristics of SBTFET with different ϕ_{Bn} values from 0.41 to 0.81eV. (b) Schematic band diagram under ON state and tunneling rate distribution near source/channel interface at subthreshold region for ϕ_{Bn} values of 0.81eV and 0.41eV. Tunneling rate distribution maps at the source corner of the devices for both ϕ_{Bn} cases at V_G =0.45 and 0.55V are also shown. Much increase in the tunneling rate distribution from V_G =0.45 to 0.55V is observed in the larger ϕ_{Bn} case.

a smaller ϕ_{Bn} exhibits a smaller SS value, which is favorable for low standby power applications (LSTPs). Tunneling rate distribution maps at the source corner of the devices for ϕ_{Bn} of 0.81, and 0.41eV at V_G =0.45 and 0.55V are shown in Figure 2(b). For a large ϕ_{Bn}, the distribution hardly changed with the increase in V_G, while obvious tunneling probability enhancement was observed for a small $\phi_{Bn.}$ The energy dependence of the electron concentration in the source region can be understood from the Fermi distribution of electrons, where the number of electrons higher than the Fermi level of the source exponentially decreases with energy. Therefore, this smaller SS for a small ϕ_{Bn} can be explained by the drastic enhancement of the tunneling probability for large numbers of electrons near the Fermi level in the source electrode. As a smaller ϕ_{Bn} also leads to a larger I_{on} of SBTFETs as shown in this figure, we could conclude that a smaller ϕ_{Bn} is preferable for this relatively long L_g.

Secondly, the influence of channel doping on I_d and SS is examined. Figure 3.2 shows the I_d- V_G characteristics with four different doping densities, 5×10^{18}, 8×10^{18}, 1×10^{19} and 2×10^{19} cm^{-3}. Here, ϕ_{Bn} was set to 0.61 eV. With the increase in channel doping, the V_{th} shifts toward the positive direction, reflecting the change in the Fermi level of the channel. Although the smallest SS showed almost comparable values down to 60 mV/dec for all cases, when we focus on the SS values in the V_G range around V_{th} or higher, they are smaller for a larger N_a. Furthermore, the I_d values with the same gate drive (V_G -V_{th}), for example, 0.55V, were 0.43 and 0.52 mA/μm for the doping concentrations of 5×10^{18} and 2×10^{19} cm^{-3}, respectively. Therefore, we could conclude that a larger *Na* is preferable for this relatively long L_g. As shown in Figure 3.2, under ON state, I_d is dominated by I_{TN}. Therefore, this phenomenon can be understood by the steeper and thinner triangular-like potential barrier for a higher channel doping

concentration, as depicted in Figure 3(b).

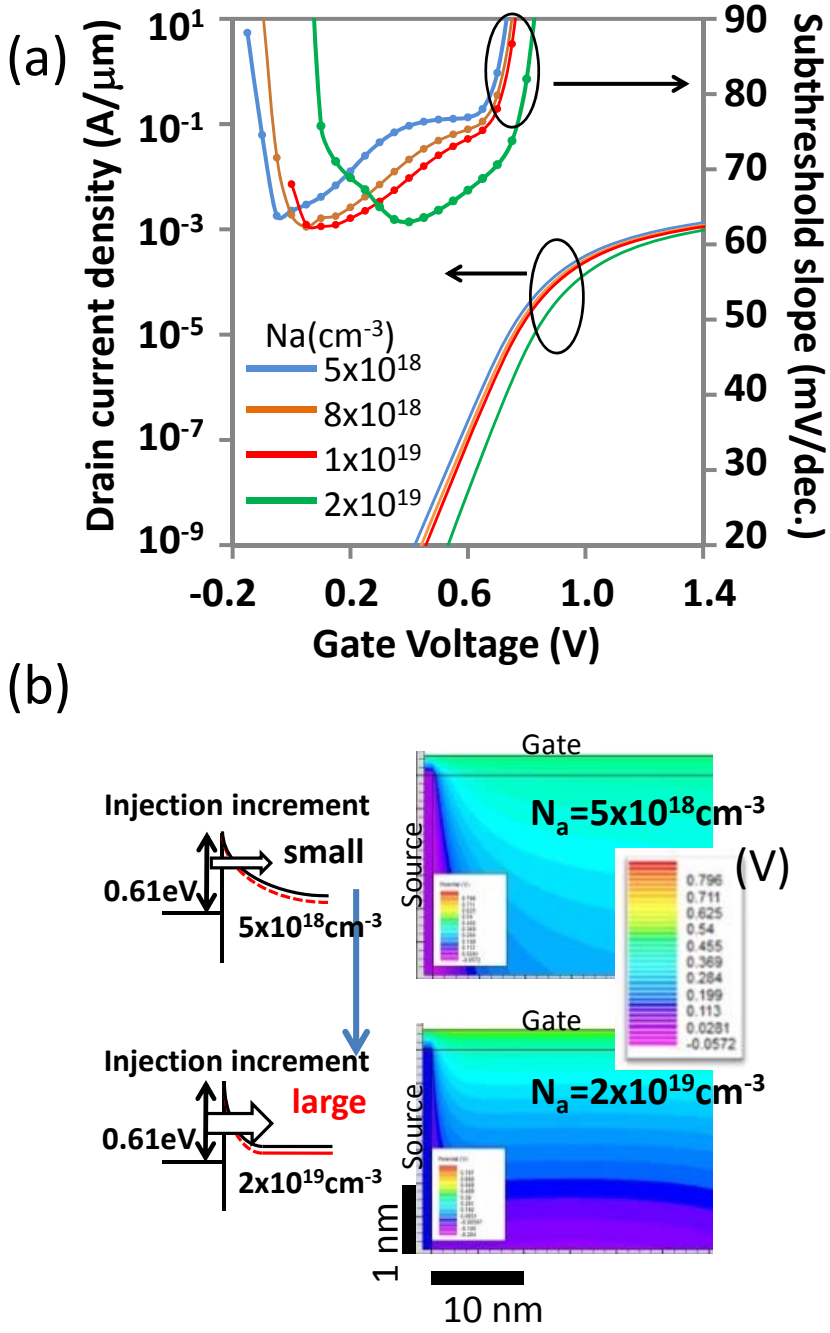


Figure 3.3(a) I_d- V_G and SS characteristics of SBTFET with different channel doping concentrations from 5×10^{18} to 2×10^{19} cm^{-3}. (b) Potential distribution in the channel near the source for N_a of 5×10^{18} and 2×10^{19} cm^{-3} , V_G =0.55V.

As tunneling probability is a function of m^*, the I_d of the SBTFET, which is mainly dominated by I_{TN}, should have strong influence of m^*. Figure 4 shows the I_d- V_G and SS characteristics with three different m^*values; $0.03m_0$, $0.08m_0$, and $0.1m_0$. Here ϕ_{Bn} and N_a were set to 0.61 eV and 2×10^{19} cm^{-3}, respectively. One can see an increase in I_d once V_G surpasses V_{th}, and SS remains below 70 mV/dec, correspondingly. Moreover, owing to the increase in tunneling probability, the I_{ON} also increases with a smaller m^*. An almost negligible difference was observed at regions of V_G far below V_{th}, where I_{TH} dominates. Therefore, it can be concluded that higher SBTFET performance can be achieved with the use of smaller the m^*. A practically small m^* can be obtained using a strained Si channel or III-V materials.[3.32]

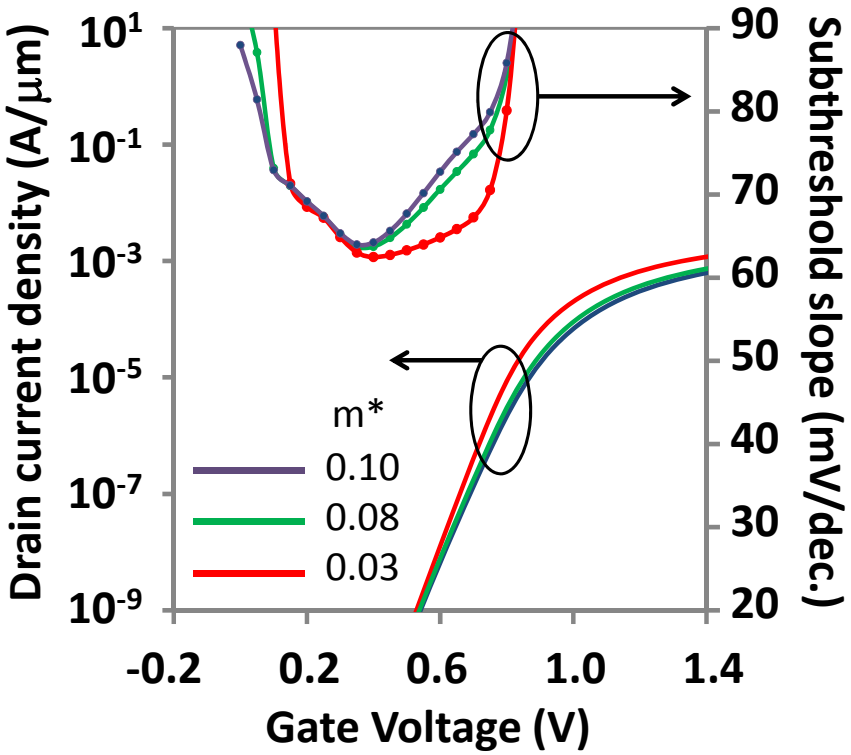


Figure 3.4. I_d- V_G and SS characteristics of SBTFET with different m^* from $0.03m_0$ to $0.1m_0$, where m_0 denotes the electron mass in the free space. ϕ_{Bn} and

N_a were set to 0.61 eV and 2×10^{19} cm^{-3} , respectively.

3.3.2 Gate length scaling of SBTFETs: comparison with conventional MOSFETs

The I_d- V_G and SS characteristics of SBTFETs and conventional MOSFETs with different L_g values are shown in Figure 5(a) and summarized in Figure 5(b). Here, the Schottky barrier height of the SBTFET is 0.61eV. The channel doping was set to 2×10^{19} cm^{-3} for both cases. One can observe a severe roll-off shift in V_{th} with conventional FETs. This implies that further L_g scaling for conventional MOSFETs requires higher channel doping to suppress the SCE. On the other hand, the V_{th} roll-off is well suppressed even for a L_g of approximately around 10nm. Although slight degradations were observed in the smallest SS in the subthreshold region for both FETs, the values were almost comparable at L_g values down to 10 nm. As a whole, the SBTFET showed improved resistance against L_g scaling to 10 nm.

The improved SCE immunity with the SBTFET can be understood from the channel potential profile in the OFF-state, where the depletion layer width in the channel near the source end is small due to the smaller built-in potential between the source electrode and the channel p-Si, as shown in Figure 6 For example, the built-in potential at the source end is about 0.3eV a with ϕ_{Bn} of 0.81eV. (the Fermi level in p-Si with the doping concentration of 2×10^{19} cm^{-3} lies almost at the Ev level in Si.) On the other hand, FETs with a conventional n+-S/D have a large built-in potential of 1.1eV. These built-in potentials of 0.31 and 1.1eV lead to the depletion layer thicknesses of about 4.5 and 8.7nm, respectively, without the influence of the gate. Therefore, it may be expected that the conventional FETs tend to suffer from the increasing channel potential for

short-channel devices more than SBTFETs.

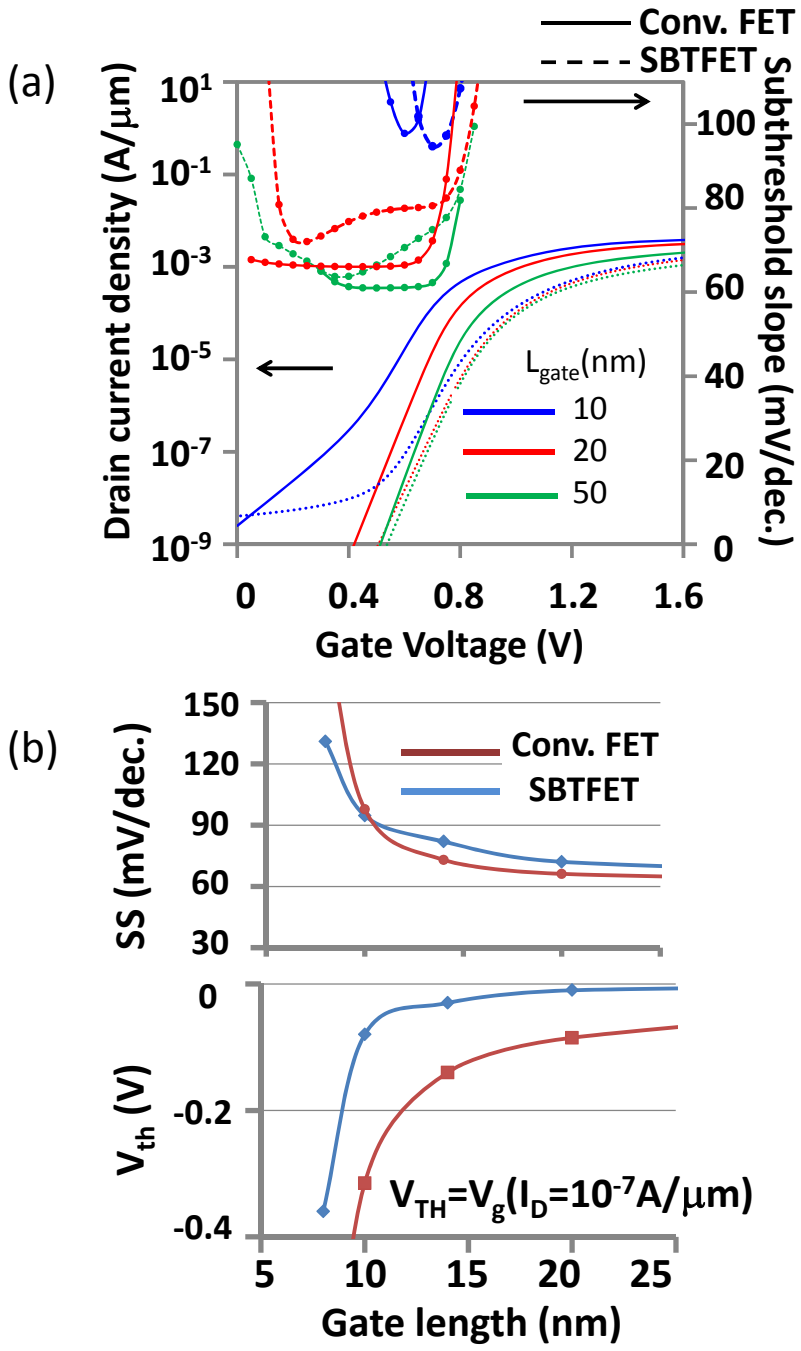


Figure 3.5(a) I_d - V_G and SS characteristics of SBTFETs and conventional MOSFETs. The Schottky barrier height of the SBTFET is 0.61eV. The channel doping concentration was set to 2×10^{19} cm^{-3} for both cases. ***(b)*** Smallest SS in

the subthreshold regions and V_{th} as a function of gate length.

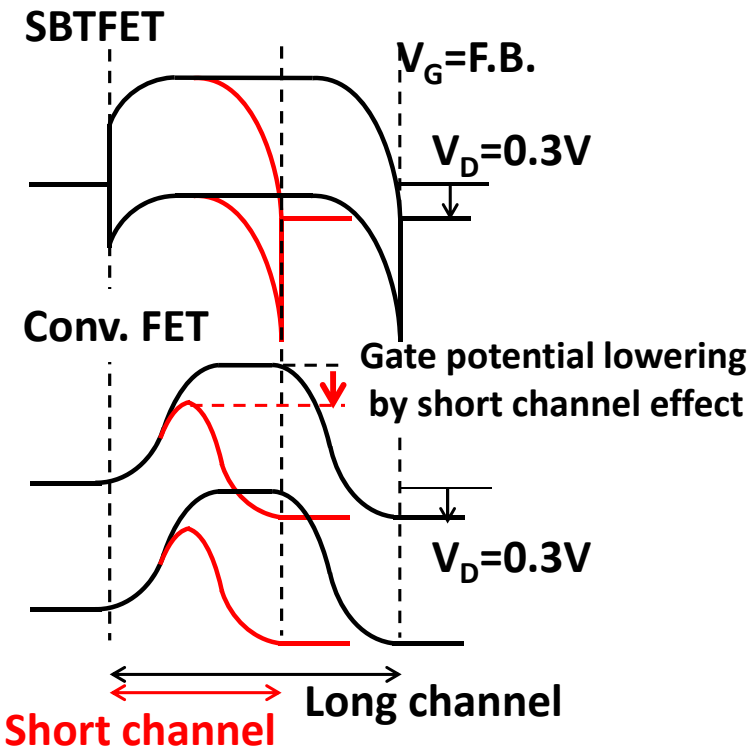


Figure 3.6 Channel potential profile difference of SBTFET and conventional FETs with L_g scaling under V_G smaller than V_{th} (OFF state).

The influences of N_a and ϕ_{Bn} on the I_d- V_G and SS characteristics of the SBTFET with an L_g of 10 nm are shown in Figure 7. With the increase in N_a, the V_{th} shifts to the positive direction, reflecting the change in the Fermi level of the channels. Along with the shift in V_{th}, one can see an improvement in SS with higher N_a. On the other hand, the improved I_d- V_G with a smaller SS was obtained with a large ϕ_{Bn}, which is in contract to the results obtained with an L_g of 50 nm. This can be understood from the depletion layer thickness reduction at the source side for a larger ϕ_{Bn} owing to the smaller built-in potential between the source electrode and the channel p-Si. A larger ϕ_{Bn} leads to the suppression of the SCE. Therefore, these results strongly imply the existence of an

optimum ϕ_{Bn} for each L_g.

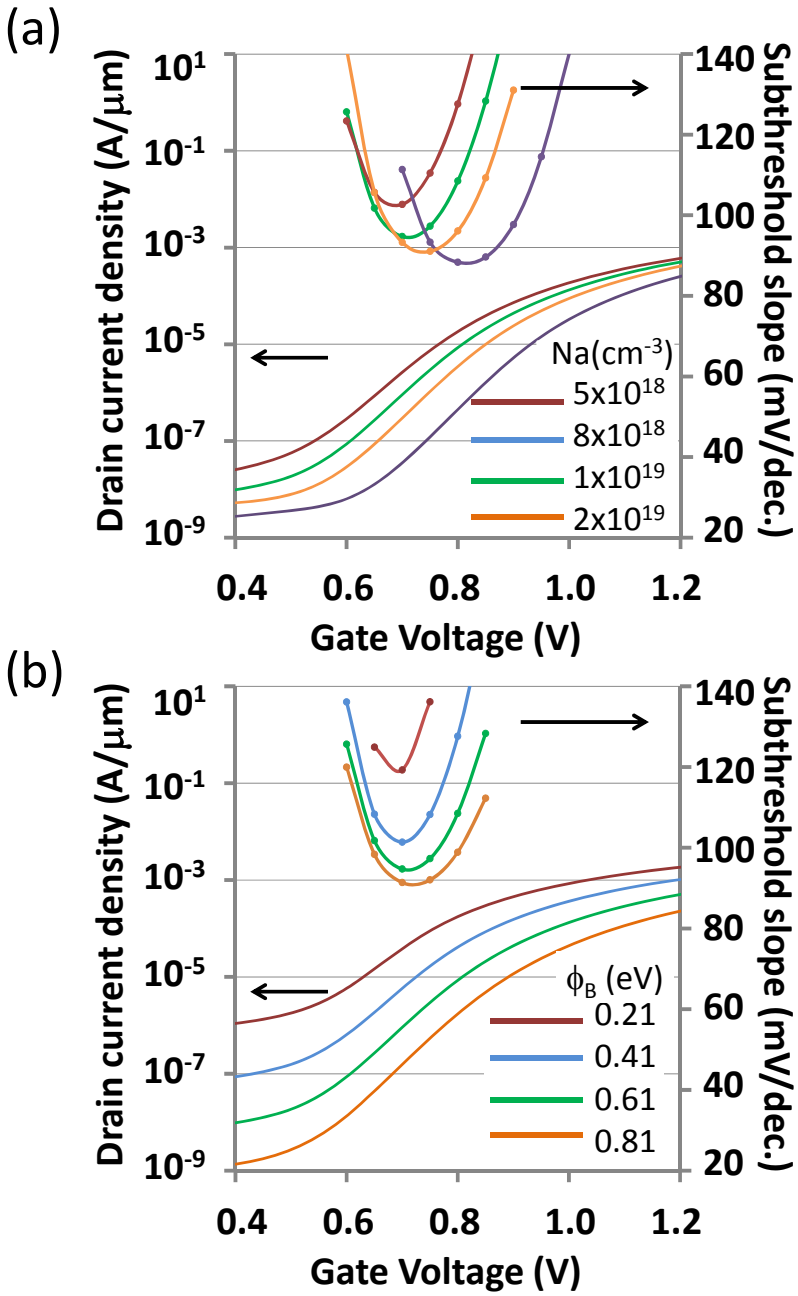


Figure 3.7 I_d- V_G and SS characteristics of SBTFET with L_g of 10 nm. (a) N_a was varied from 5×10^{18} to 2×10^{19} cm^{-3}. ϕ_{Bn} was set to 0.61eV. (b) ϕ_{Bn} was varied from 0.21 to 0.81eV. N_a was set to 2×10^{19} cm^{-3}

Figure 3.8 shows the I_{ON}/I_{OFF} ratio of the SBTFET and the smallest SS as a function of gate length. For the *I*on/*I*off ratio calculation, the gate overdrive is set to 0.5V. The Schottky barrier for electrons ϕ_{Bn} is taken as a parameter. The channel doping was set to 2×10^{19} cm^{-3}. It can be observed that SS and I_{ON}/I_{OFF} behave in completely different ways between the short L_g region and the long L_g region with the critical channel length at approximately 15 nm in the case of these structural parameters. Compared with the conventional FET at an L_g of 10 nm, SBTFET shows higher I_{ON}/I_{OFF} for ϕ_{Bn} larger than 0.41eV. Taking a small SS and a large I_{ON}/I_{OFF} ratio and their stabilities against L_g fluctuation at around 10nm into consideration, we can conclude that an optimum ϕ_{Bn} value for the SBTFET exists at around 0.61 eV, which is practically attainable with silicides such as NiSi [29]. It should be noted that this optimum barrier height is for the above-mentioned device structure (SOI thickness of 6nm) and operation condition (V_d=0.3V) and that the value could be varied for different SOI thicknesses as well as drain voltage conditions.

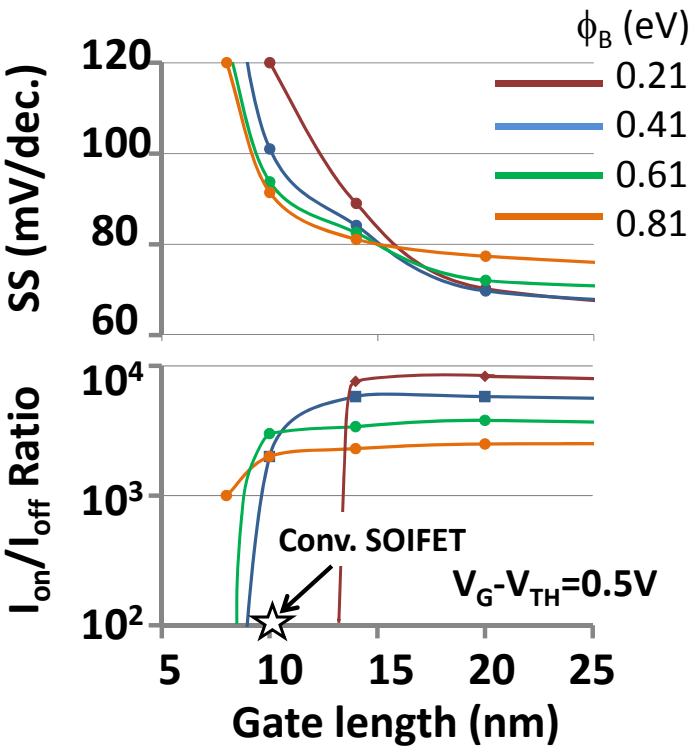


Figure3. 8 (a) SS and (b) I_{ON}/I_{OFF} characteristics as a function of L_g. Gate overdrive is set to 0.5V. ϕ_{Bn} was varied from 0.21 to 0.81eV. The channel doping was set to 2×10^{19} cm^{-3}.

3.4. Conclusions

The device simulation has been performed to investigate the structural parameter influence on the electrical characteristics of SBTFETs. Schottky barrier height and channel doping concentration as well as gate length are mainly taken as the structural parameters. For relatively long-channel MOSFETs (50 nm), a low Schottky barrier height as well as a high substrate impurity concentration lead to the increase in the tunneling probability through the barrier, resulting in the smaller SS. On the other hand, for short channel length MOSFETS (10 nm), the SCE has much influence on the characteristics of SBTFETs. Since a larger SBH is effective to suppress the SCE, an

optimum ϕ_{Bn} exists for the short-channel SBTFETs. The SBTFET showed good subthreshold performance and a higher *I*on/*I*off than the conventional SOIMOS-FET in the 10nm region with the Schottky barrier height optimization.

3.5 References of this chapter

[3.1] R. Troutman "VLSI limitations from drain-induced barrier lowering" IEEE Trans. Electron Device. **26** (1979) 461.

[3.2] Y. Taur, Y.-J. Mii, H.-S. Wong, D.A. Buchanan, S. J. Wind, S. A. Rishton, G. A. Sai-Halasz and E. J. Nowak "CMOS Scaling into the 21st Century0.1 □m and Beyond" IBM J. Res. Dev. **39** (1995) 245

[3.3] Y. Mii, S. Wind, Y. Taur, Y. Lii, D. Klaus and J. Bucchignano "An ultra-low power0.1/spl mu/m CMOS" VLSI Symp. Tech. Dig., 1994, p.9.

[3.4] T.N. Nguyen and J.D. Plummer "Physical mechanisms responsible for short channel effects in MOS devices" IEDM Tech. Dig., 1981, p. 596.

[3.5] B. Yu, L. Chang, S. Ahmed, H. Wang, S. Bell, C.-Y. Yang, C. Tabery, C. Ho, X. Qi, T.-J. King. J. Bokor, C.M. Hu, M.-R. Lin and D. Kyser "FinFET scaling to 10 nm gate length" IEDM Tech. Dig., 2002 p. 251.

[3.6] F.-L. Yang, D.-H. Lee, H.-Y. Chen, C.-Y. Chang, S.-D. Liu, C.-C. Huang, T.-X. Chung, H.-W. Chen, C.-C. Huang, Y.-H. Liu, C.-C. Wu, C.-C. Chen, S.-C. Chen, Y.-T. Chen, Y.-H. Chen, C.-J. Chen, B.-W. Chan, P.-F. Hsu, J.-H. Shieh, H.-J. Tao, Y.-C. Yez, Y. Li. J.-W. Lee, P. Chen, M.-S. Liang, and C. Hu: VLSI Symp. "5nm-gate nanowire FinFET" Tech. Dig., 2004, p. 196.

[3.7] S.C. Rustagi, N. Singh, W.W. Fang, K.D. Buddharaju, S.R. Omampuliyur, S.H.G. Tao, C.H. Tung, G.Q. Lo, and D.L. Kwong "CMOS Inverter Based on Gate-All-Around

Sillicon-Nanowire MOSFETs Fabricated Using Top-Down Approach" IEEE Electron Device Lett., **28** (2007) 1021.

[3.8] K. Mao, T. Mizutani, A. Kumar, T. Saraya, and T. Hiramoto "Suppression of Within-Device Variability in Intrinsic Channel Tri-Gate Silicon Nanowire Metal—Oxide—Semiconductor Field-Effect Transistors" Jpn.J.Appl.Phys., **51** (2012) 02BC06.

[3.9] K. Tanaka, K. Takeuchi and M. Hane "Practical finFET design considering GIDL for LSTP(low standby power) devices" IEDM Tech. Dig., 2005, p. 980.

[3.10] J. M. Larson and J.P. Snyder "Overview and status of metal S/D Schottky-barrier MOSFET technology" IEEE Trans. Electron Devices, **53**, (2006) 1048.

[3.11] M. Jang, Y. Kim, J. Shin, S. Lee, and K. Park "A 50-nm-gate-length erbium-silicided n-type Schottky barrier metal-oxide-semiconductor field-effect transistor." Appl. Phys. Lett., **84** (2004) 741.

[3.12] M. Jang, Y. Kim, M. Jeon, C. Choi, I. Baek, S. Lee, and B. Park "N_2-Annealing Effects on Characteristics of Schottky-Barrier MOSFETS" IEEE Trans. Electron Devices, **53** (2006) 1821.

[3.13] M. Sugino, L.A. Akers and M.E. Rebeschini "Latchup-free Schottky-barrier CMOS" IEEE Trans. Electron Devices, **30**, (1983) 110.

[3.14] E.J. Tan, K.-L. Pey, N. Singh, G.-Q. Lo, D.Z. Chi, Y.K. Chin, K.M. Hoe, G. Cui, and P.S. Lee "Demonstration of Schottky Barrier NMOS Transistors With Erbium Silicided Source/Drain and Silicon Nanowire Channel" IEEE Electron Device Lett., **29** (2008) 1167.

[3.15] C. Wang, J.P. Snyder, and J.R. Tucker "Sub-40 nm PtSi Schottky source/drain metal–oxide–semiconductor field-effect transistors" Appl.Phys.Lett. **74** (1999)

1174.

[3.16] J. Kedzierski, P. Xuan, E.H. Anderson, J. Bokor, T.-J. King, C. Hu "Complementary silicide source/drain thin-body MOSFETs for the 20 nm gate length regime" IEDM Tech. Dig., 2000, 57.

[3.17] J. Guo and M.S. Lundstrom "A computational study of thin-body, double-gate, Schottky barrier MOSFETs" IEEE Trans. Electron Devices, **49** (2002) 1897.

[3.18] S. Hara and I. Ohdomari "Chemical trend in silicide electronic structure and Schottky-barrier heights of silicide-silicon interfaces" Phys. Rev. B., **38**, (1988) 7554.

[3.19] K. Matsuzawa, K. Uchida and A. Nishiyama "A unified simulation of Schottky and ohmic contacts" IEEE Trans. Electron Devices, **47**, (2000) 103.

[3.20] W.Y.Choi, B.G. Park, J. D. Lee, T.K. Liu "Tunneling Field-Effect Transistors (TFETs) With Subthreshold Swing (SS) Less Than 60 mV/dec" IEEE Electron Device Lett. Vol.28, pp.743-745 (2007).

[3.21] S. H. Kim, H. Kam, C. Hu and T.-J. K. Liu "Germanium-source tunnel field effect transistors with record high ION/IOFF" VLSI Symp. Tech. Dig., 2009, P.179.

[3.22] T. Krishnamohan, D. Kim, S. Raghunathan, and K. Saraswat "Double-Gate Strained-Ge Heterostructure Tunneling FET (TFET) With record high drive currents and ≪60mV/dec subthreshold slope" IEDM Tech. Dig., 2008, p. 947.

[3.23] V. Nagavarapu, R. Jhaveri, and J. C. S. Woo "The Tunnel Source (PNPN) n-MOSFET: A Novel High Performance Transistor" IEEE Trans. Electron Devices, **55** (2008) 1013.

[3.24] A. Mallik, and A. Chattopadhyay "The Impact of Fringing Field on the Device Performance of a p-Channel Tunnel Field-Effect Transistor With a High-κGate Dielectric" IEEE Trans. Electron Devices, **59** (2012) 277.

[3.25] K. Jeon, W. Y. Loh, P. Patel, C. Y. Kang, J. Oh, A. Bowonder, C. Park, C. S. Park, C. Smith, P. Majhi, H. Tseng, R. Jammy, T. K. Liu, and C. Hu "Si tunnel transistors with a novel silicided source and 46mV/dec swing" VLSI Symp. Tech. Dig., 2010, p. 121

[3.26] R. Jhaveri, V. Nagavarapu, and Jason C. S. Woo "Asymmetric Schottky Tunneling Source SOI MOSFET Design for Mixed-Mode Applications" IEEE Trans. Electron Devices, **56**,(2009) 93

[3.27] ATLAS user's manual by Silvaco Inc.

[3.28]N. Reckinger, X.Tang, V. Bayot, D.A. Yarekha, E. Dubois, S. Godey, X. Wallart, G. Larrieu, A. Laszcz, J. Ratajczak, P.J. Jacques, and J.-P. Raskin "Correlation of Schottky-Barrier Height and Microstructure in the Epitaxial Ni Silicide on Si(111)" J. Appl. Phys. **104**(2008) 103523.

[3.29] M. Liehr, P.E. Schmid, F.K. Le Gones, and P.S. Ho "Correlation of Schottky-Barrier Height and Microstructure in the Epitaxial Ni Silicide on Si(111)" Phys. Rev. Lett., **54** (1985) 2139.

[3.30] G. Ottaviani, K.N. Tu, J.W. Mayer "Barrier heights and silicide formation for Ni, Pd, and Pt on silicon" Phys Rev. B **34** (1981) 3354.

[3.31] K.-H. Kao, A.S. Verhulst, W.G. Vandenberghe, B. Sorée, G. Groeseneken, and K. De Meyer "Direct and Indirect Band-to-Band Tunneling in Germanium-Based TFETs" IEEE Trans. Electron Devices, **49** (2012) 292.

[3.32] S. Takagi, T. Tezuka, T. Irisawa, S. Nakaharai , T. Numata, K. Usuda ,N. Sugiyama, M. Shichijo, R. Nakane and S. Sugahara " Device structures and carrier transport properties of advanced CMOS using high mobility channels" Solid-State Electron, **51**, (2007) 526.

Chapter 4

A novel Silicide formation and Schottky Barrier Height Modulation

4.1 Introduction

As described in chapter 1, Ni silicide is widely used for the reduction of the parasitic resistance of MOSFETs. In addition to that, this material can be a good candidate for the application to Shottky barrier type tunneling FETs mentioned in chapter 3. However as far as the stable formation of the silicide with thermal stability is concerned, there is a room for the improvement of the silicidation process. Moreover simulation study in chapter 3 revealed that the precise control of the Schottky barrier is required to obtain the optimum electrical characteristics. Since the simulation study indicated the optimum Schottoky barrier height depends on the gate length of the devices, it is desired that this control is accomplished on the same silicide material basis.

This chapter consists mainly of 3 parts: in section 4.2, a novel Ni silicide formation process using annealing of the Ni/Si thin film stack is introduced as a means of the stable formation of the silicide with thermal stability. In section 4.3, Schottky barrier modification in the new process is explained followed by the result of these process application to SOI MOSFETs in section 4.4.

4.2 Novel Ni silicide formation process using annealing of the Ni/Si thin film stack

Introduction

This novel Ni/Si stack process is based on the fact that thin Ni reaction with Si could form very thin flat NiSi2 on Si with high thermal stability. Therefore this concept is firstly introduced in section 4.2.1 and then the multiple Ni/Si process using this thin Ni film reaction with Si is introduced in following section 4.2.2. The electrical characteristics of the resultant Ni silicide/Si interface are described in section 4.2.3.

4.2.1 Thermally resistant Ni silicide formation by Ni thin film reaction with Si

4.2.1.1 Introduction

Ni silicides have been widely investigated for contact materials in microelectronic devices because of relatively low resistivity, relatively low formation temperature and relatively small Si consumption during the formation in comparison with other silicide materials [4.2.1]. One of the issues of Ni silicides is that the formed NiSi, a low-resistive phase in Ni silicides, starts to agglomerate at an annealing temperature of 600 ^{o}C [4.2.2]. As the agglomeration is the results of minimizing the gain boundary between NiSi grains and the interface energy of NiSi and Si substrate, the temperature for agglomeration decreases when the thickness of NiSi is reduced [4.2.3]. Recently, Ni films with thicknesses less than 4 nm were found to be resistant to agglomeration up to an annealing temperature of 850 ^{o}C [4.2.4]. The difference in the silicide films is the formation of $NiSi_2$ phase even at an annealing temperature of 300 ^{o}C, which is commonly formed at an annealing temperature of 800 ^{o}C [4.2.5]. Therefore, the

suppression of the agglomeration can be understood by the difference in the energy of $NiSi_2$ and NiSi phases. The suppression of agglomeration is also advantageous to obtain a flat interface between silicides and Si substrates. The interface of silicide and Si substrates tends to form pyramid shapes with Si(111) plane [4.2.6]. Therefore, another advantage of agglomeration-resistant Ni silicides is the suppression of forming interfaces with different crystallographic orientations. This chapter confirms the phase and the surface morphology changes of Ni silicide films on annealing temperature.

4.2.1.2 Thermal stability of Ni silicide formation

Figures 4.2.1 and 4.2.2 show sheet resistance (ρ_{sh}) and surface roughness of the films on annealing temperature, respectively. For the sample with 5.5-nm-thick Ni layer, ρ_{sh} showed a large decrease over 300 ^{o}C, which is attributed to the formation of NiSi phase in the silicide. When the annealing temperature is over 500 ^{o}C, the ρ_{sh} showed a large increase due to agglomeration of the silicides which is shown in figure 4.2.2. On the other hand, for the sample with Ni thickness of 3.0 nm, a gradual reduction in the ρ_{sh} was observed over 300 ^{o}C, and the value became stable at annealing temperatures from 400 to 800 ^{o}C, which is in good agreement with previous reports [4.2.4, 4.2.6]. Considering the resistivity of typical bulk $NiSi_2$ (34~50 μΩcm) [4.2.7], the phase of the silicide film can be considered as $NiSi_2$. Consequently, both of the thickness of these samples is estimated about 10 nm [4.2.7].

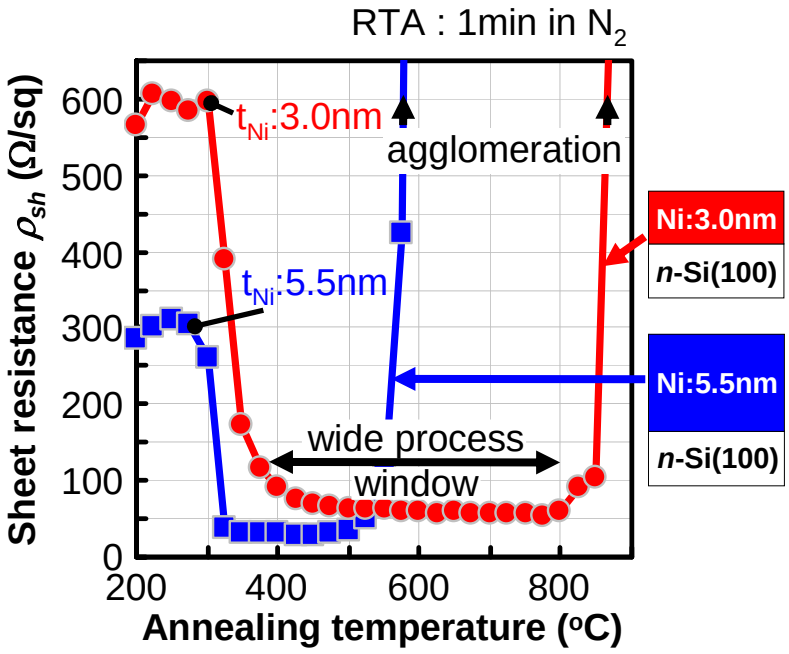


Figure 4.2.1 Sheet resistance (ρ_{sh}) of silicides with 3.0 and 5.5 nm thick Ni layers on annealing temperature (t_{Ni} is Ni thickness).

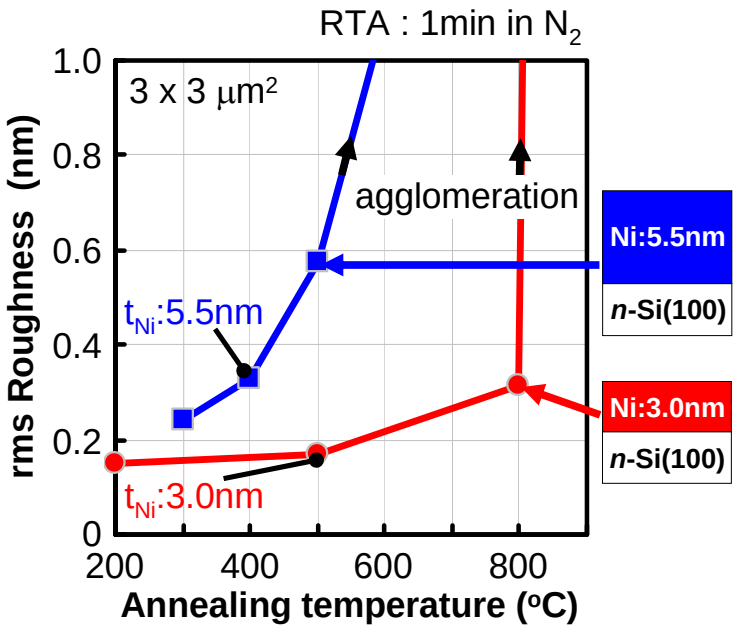


Figure 4.2.2 Surface roughness of silicide films with 3.0 and 5.5 nm thick Ni layers on annealing temperature.

4.2.1.3 Bonding states of Ni silicide film

Ni $2p_{3/2}$ spectra of the samples annealed at various temperatures are shown in figure 4.2.3. The binding energy at the peak intensity was found to shift to higher energy from pure Ni, which was obtained by as-deposited sample. At an annealing temperature of 250 ^{o}C, the spectrum indicates the main composition is Ni-rich phase, which is in good agreement with the ρ_{sh} as high resistivity is reported for Ni-rich phase. The sample with 5.5-nm-thick-Ni showed a single peak at 500 ^{o}C annealing, which corresponds to the NiSi phase at 853.72 eV [4.2.8]. For 3-nm-thick-Ni samples, while increasing the annealing temperature, two peak intensities, one at 854.19 eV with large intensity and the other Ni-rich phase with small intensity, were observed at 500 ^{o}C. The intensity at 854.19 eV further increased when the sample was annealed at 800 ^{o}C, indicating that the residual Ni-rich phase was converted to $NiSi_2$ phase by annealing [4.2.9].

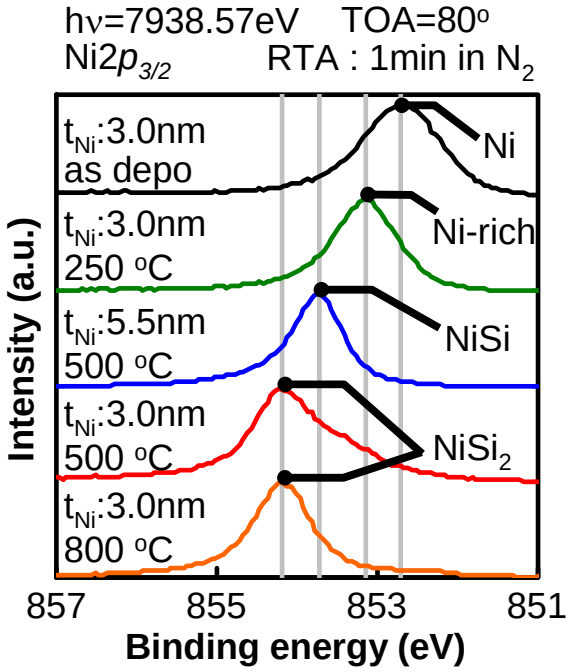


Figure 4.2.3 Ni $2p_{3/2}$ spectra of the silicide films annealed at various temperature.

4.2.1.4 Conclusion

Ni silicides, reactively formed by 3.0-nm-thick Ni, have shown a stable sheet resistance, flat morphology against annealing temperature up to 800 ^{o}C compared to those formed with thicker Ni film. These properties are owing to the formation of stable $NiSi_2$ phase at a temperature as low as 500 ^{o}C. The summary of Ni silicide phase and morphology change is shown in figure 4.2.4.

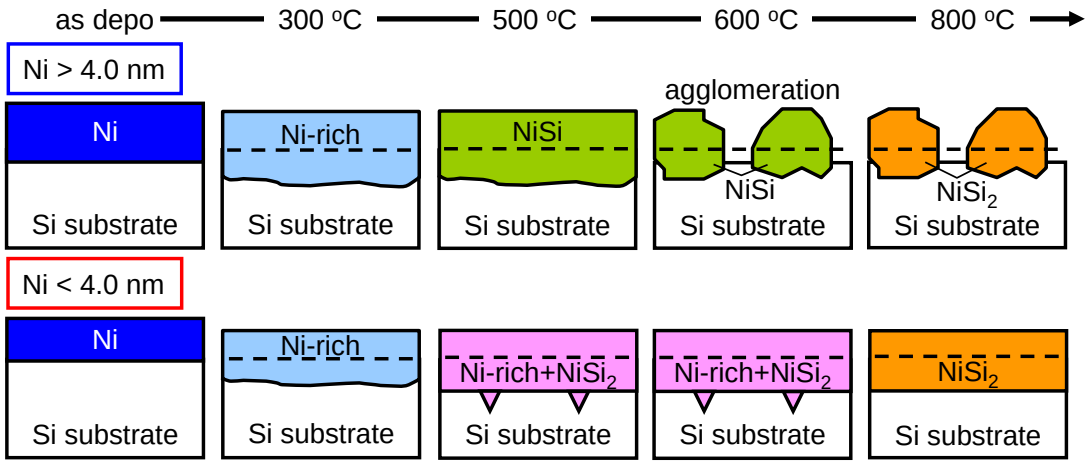


Figure 4.2.4 Ni silicide phase and morphology change dependent on Ni thickness.

4.2.2. Multiple Ni/Si process using this thin Ni film reaction with Si

4.2.2.1 Introduction

As shown in the section 4.2.1., the case of 3.0-nm-thick Ni layer deposition, the stable composition and morphology can be obtained at wide process temperature range because $NiSi_2$, which is the most stable phase in Ni silicides, is formed at low temperature. However, there remain some issues which are pattern dependent reaction

and limitation of silicide thickness because of limitation of initial Ni thickness within 4.0 nm to form $NiSi_2$ at low temperature [4.2.10-12]. Thereby, to solve these issues, stacked silicidation process is proposed as shown in figure 4.2.5. In this process, interface reaction can be suppressed because Si substrate reacts with only first 0.5-nm-thick Ni layer and silicide thickness can be changed easily by changing the number of a set of Ni/Si. In this chapter, therefore, characteristics of Ni silicide using stacked silicidation process are investigated. Furthermore, stacked silicidation process of other semiconductor substrates and extension of stacked silicidation process to Ti are examined.

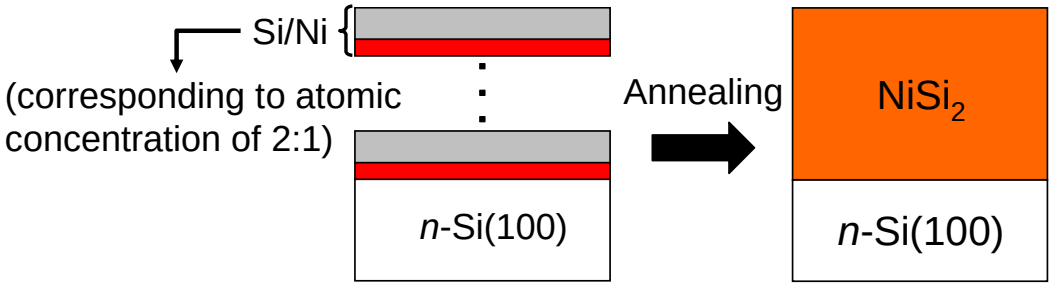


Figure 4.2.5 Schematic illustration of stacked silicidation process. A set of Si/Ni, with an atomic ratio of 2:1, is cyclically stacked on n-Si (100) substrates, followed by annealing in N_2 ambient to form $NiSi_2$ film.

4.2.2.2 Interface reaction

As shown in figure 4.2.6, TEM images of silicide/Si interface formed from Ni/Si stacked silicidation process before (Figure 4.2.6(a)) and after annealing at 500 ^{o}C for 1 min in N_2 ambient to form $NiSi_2$ (Figure 4.2.6(b)). TEM images revealed the formation of 10-nm-thick stacked silicide, no change in the thickness and atomically flat interface

and surface before and after annealing at 500 ^{o}C because consumption of Si from substrate is limited to the first Ni layer.

Owing to little reaction of $NiSi_2$ formed from stacked silicidation process with Si channel, diffusions of Ni atoms into channels can be well suppressed. Figure 4.2.7 shows SEM images of Si Fins after annealing with (a) Ni or (b) stacked silicide stripe on the right-hand-side. Due to excess supply of Ni atoms into Si Fins, in the case of Ni deposition, lateral silicidations were observed with scattered encroachment length.

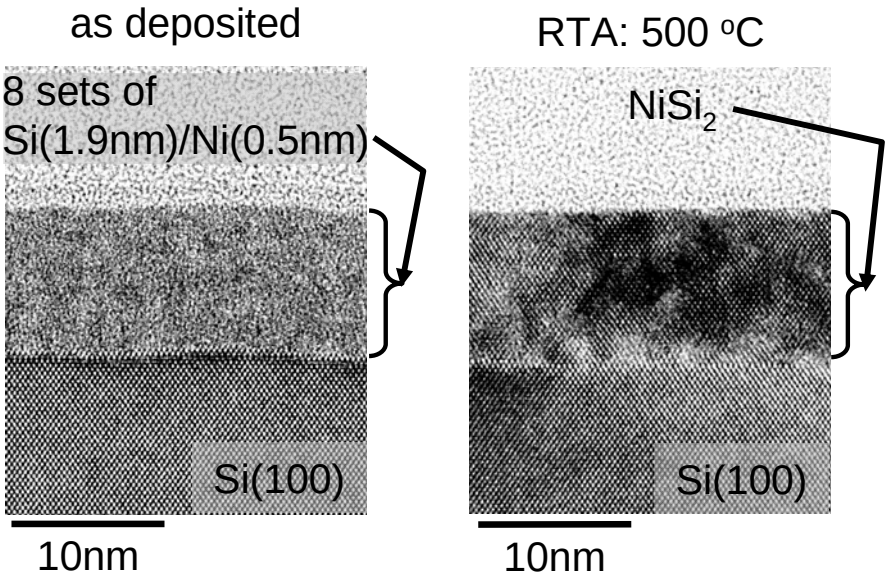


Figure 4.2.6 TEM images of stacked silicidation process at ***(a)*** as deposited and ***(b)*** after annealing at 500 ^{o}C. Atomically flat interface and surface are achieved.

On the other hand, with the use of stacked silicidation process, one can observe a complete inhibition of encroachments into Si Fins, owing to suppression of interface reaction between silicide and Si Fins. In other words, interface position can be well-defined by using stacked silicidation process. Although suppression of lateral

encroachments has been reported with 2-step annealing or nitrogen atom incorporation [4.2.13, 4.2.14], stacked silicidation process has an advantage for S/D in 3D Si channels as it completely suppresses the encroachments.

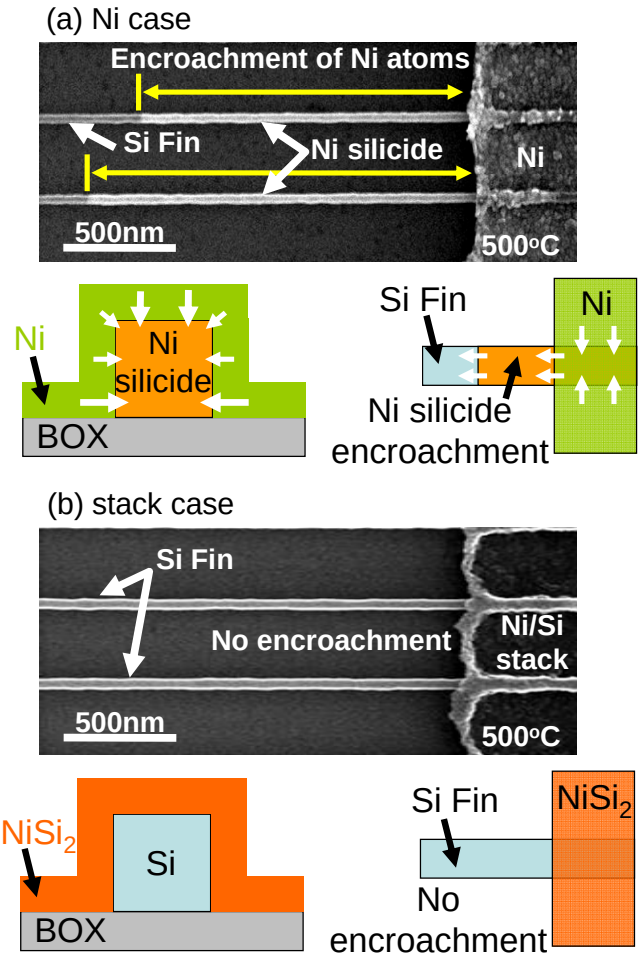


Figure 4.2.7 SEM images of Si Fins after annealing with (a) Ni or (b) stacked silicide. (a) Ni atoms encroach into Si Fin. (b) Complete suppression of encroachment can be achieved using Ni/Si stacked silicidation process.

4.2.2.3 Morphology and composition

4.2.2.3.1 Thermal stability of stacked silicidation process

Figure 4.2.8 and Figure 4.2.9 show sheet resistance (ρ_{sh}) and surface roughness of the films on annealing temperature, respectively. The silicide thickness of all samples is 10 nm. For the sample with Ni/Si stacked silicidation process showed a decrease over 325 ^{o}C and kept the stable value up to 875 ^{o}C. Although ρ_{sh} of stacked silicide is slightly larger than 3.0-nm-thick Ni layer, ρ_{sh} of stacked silicide is stable at wide process temperature window. On the other hand, the surface roughness of stacked silicide is slightly larger than those of 3.0-nm-thick Ni sample, however, the value is small enough. The surface morphology of stacked silicide was flat over wide range temperature.

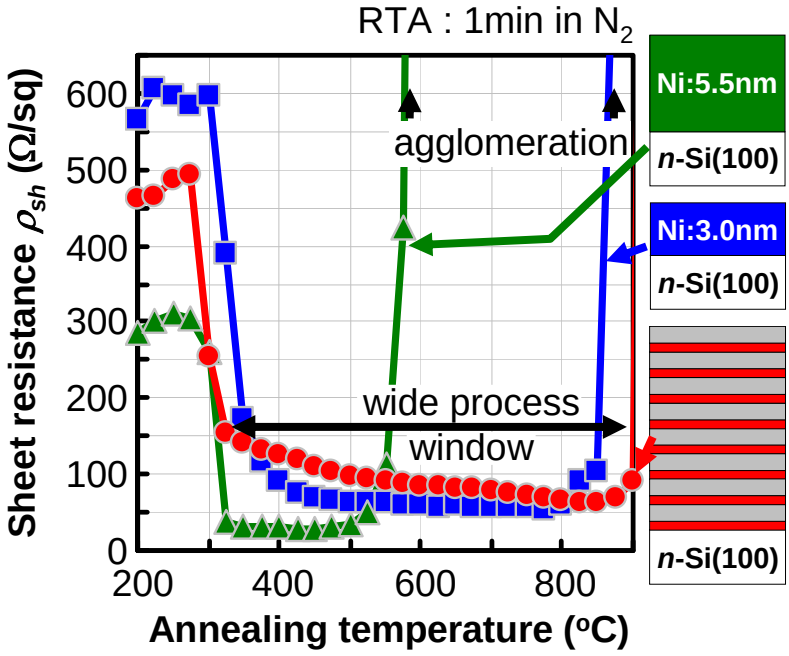


Figure 4.2.8 ρ_{sh} of stacked silicide, 3.0-nm- and 5.5-nm- thick Ni layers on

annealing temperature. ρ_{sh} of stacked silicide is stable at wide process window.

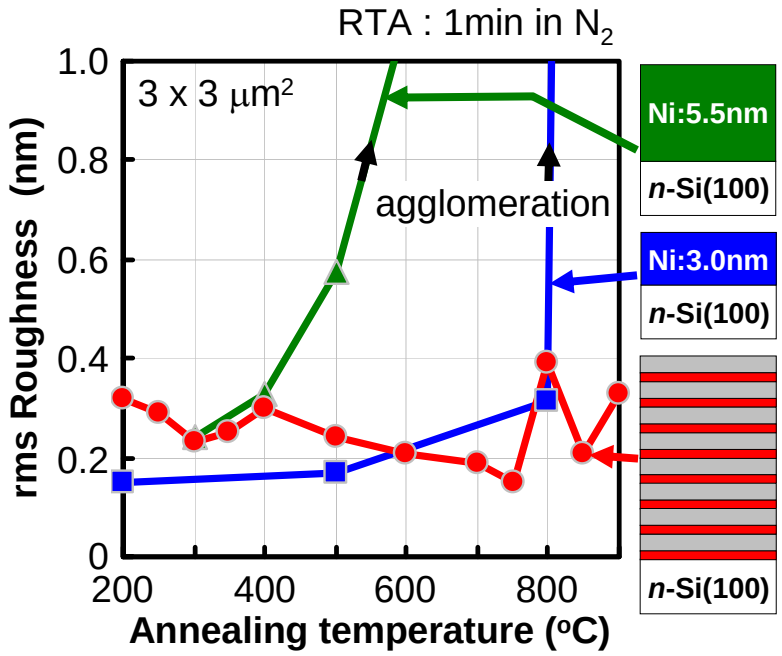


Figure 4.2.9 Surface roughness of stacked silicide, 3.0-nm- and 5.5-nm-thick Ni layers on annealing temperature. Surface roughness of stacked silicide is stable at wide process window.

4.2.2.4 XRD analysis of stacked silicide film

Figure 4.2.10 shows Out-of-plane XRD (2θ/ω scan) profile of stacked silicide. $NiSi_2$(004) peak can be detected at 2θ = 70.56°. Whereat, Rocking curve measurement (ω scan) at 2θ = 70.56° is shown in Figure 4.2.11. Because rocking curve width is about 0.1° which is narrow value, it is considered that $NiSi_2$ formed by stacked silicidation process is epitaxially grown.

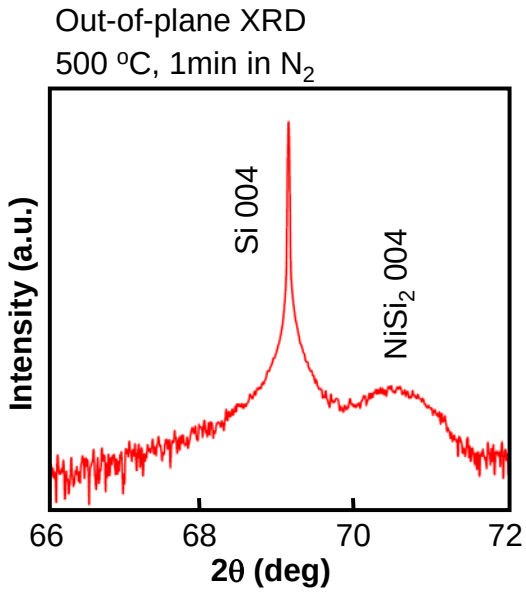


Figure 4.2.10 Out-of-plane XRD (2θ/ω scan) profile of stacked silicide annealed at 500 °C. $NiSi_2$(004) peak can be detected at 2θ = 70.56°.

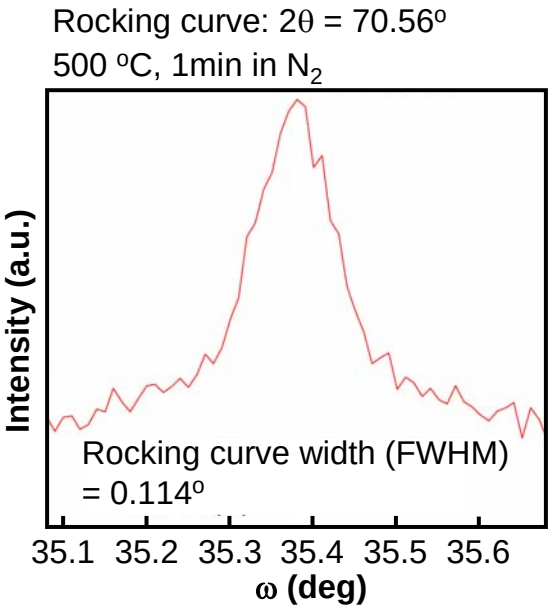


Figure 4.2.11 Rocking curve measurement (ω scan) at 2θ = 70.56°. Because rocking curve width is about 0.1° which is narrow value, it is considered that $NiSi_2$ formed by stacked silicidation process is epitaxially grown.

Figure 4.2.12 shows that In-plane XRD ($2\theta\chi/\phi$ scan) profile of stacked silicide annealed at 500 ^{o}C in $\omega = 0.3^{o}$. In-plane XRD has some characteristics which are large irradiated area and small penetration depth due to low incident angle. Red line shows X-ray incident direction can be observed Si(400) peak ($\phi = 0^{o}$) and blue line shows $\phi = 15^{o}$. In the case of $\phi = 0^{o}$, $NiSi_2$(200) and $NiSi_2$(220) peaks are detected. When ϕ is displaced to 15^{o}, $NiSi_2$(200) can not be observed, on the other hand, $NiSi_2$(220) can be observed. Rocking curve measurement (ϕ scan) at $NiSi_2$(200) is shown in figure 4.2.13. Because rocking curve width is about 0.6^{o} which is narrow value, it is considered that $NiSi_2$ is epitaxially grown. On the other hand, when ϕ is displaced, $NiSi_2$(220) can be observed. Thus, it is expected that in-plane orientation is random. Therefore, it is predict that the element which is cube-on-cube epitaxially grown for Si substrate and the oriented element that (110) axis is distributed at random in in-plane exist. However, $NiSi_2$(200) peak can not be observed in $\phi = 15^{o}$ (figure 4.8 blue line). From this result, it is expected that the oriented element has a texture that (111) axis is oriented to surface normal direction. In the crystal structure of $NiSi_2$ (Fluorite type structure), (111) plane is dense plane, it is suggested that this orientation texture can be formed in addition to the epitaxial element as shown in Figure 4.2.14.

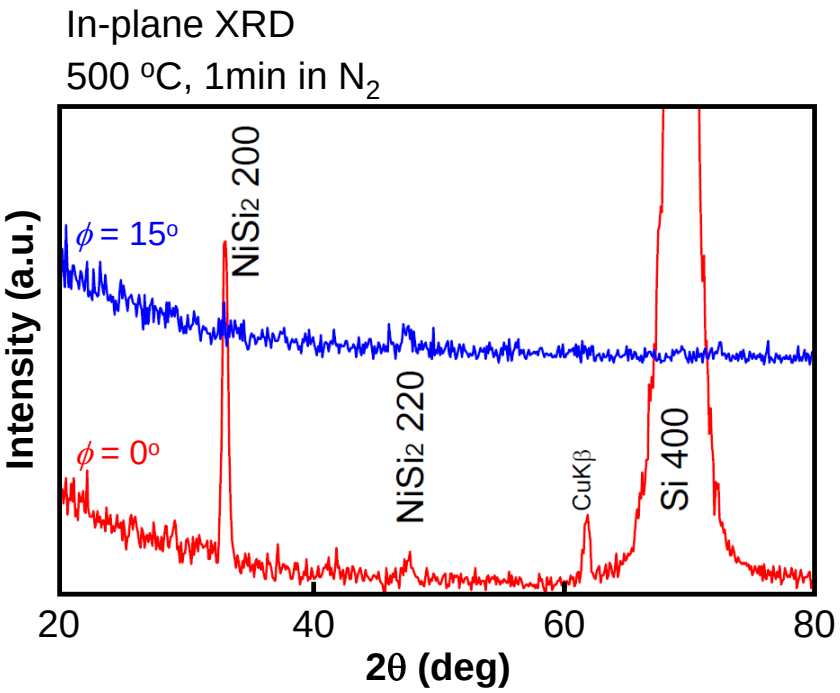


Figure 4.2.12 In-plane XRD (2θχ/ϕ scan) profile of stacked silicide annealed at 500 °C in ω = 0.3°. Red line is ϕ = 0° and blue line is ϕ = 15°. When ϕ is displaced to 15°, $NiSi_2$(200) peak can not be observed, on the other hand, $NiSi_2$(220) peak can be observed.

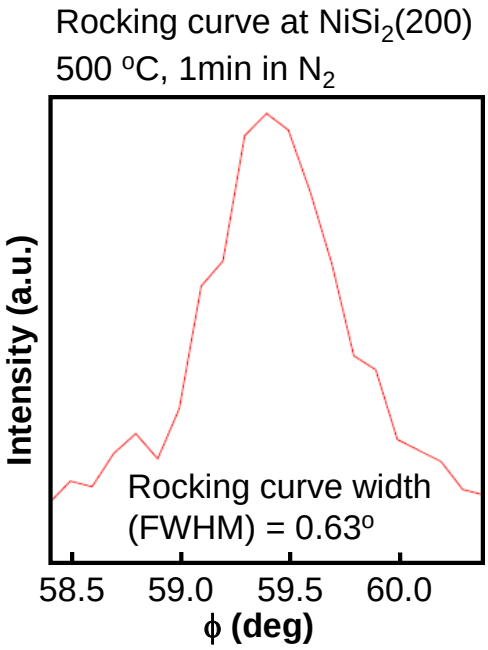


Figure 4.2.13 Rocking curve measurement (ϕ scan) at $NiSi_2$(200). Because rocking curve width is about 0.6° which is narrow value, $NiSi_2$ is epitaxially grown.

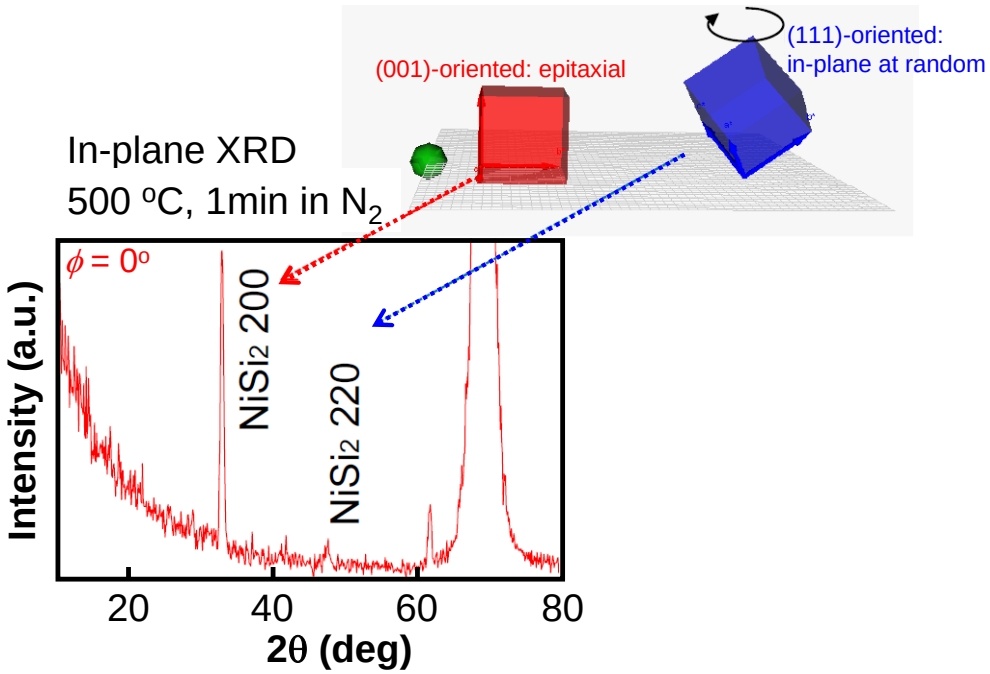


Figure 4.2.14 The images of orientation of $NiSi_2$ film. It is suggested that (111)-oriented texture can be formed in addition to the epitaxial element.

4.2.2.5 XPS analysis of stacked silicide film

Ni $2p_{3/2}$ spectra of the samples annealed at various temperatures are shown in Figure 4.2.15. Stacked silicide showed similar peaks with 3.0-nm-thick-Ni, thus, the phase of stacked silicide is $NiSi_2$.

Ni $2p_{3/2}$ spectra of the stacked silicide annealing at 500 ^oC measured changing photoelectron take-off angles (TOAs) from 30^o to 80^o are shown in Figure 4.2.16. Inelastic mean free path (λ) is calculated by TPP-2M. In this case, λ is equal to 9.6 nm. All spectra were close to the same each other independent of TOAs. From the results of TEM images, XRD profiles and Ni $2p_{3/2}$ spectra, it is considered that stacked silicide film is uniform and epitaxially grown $NiSi_2$.

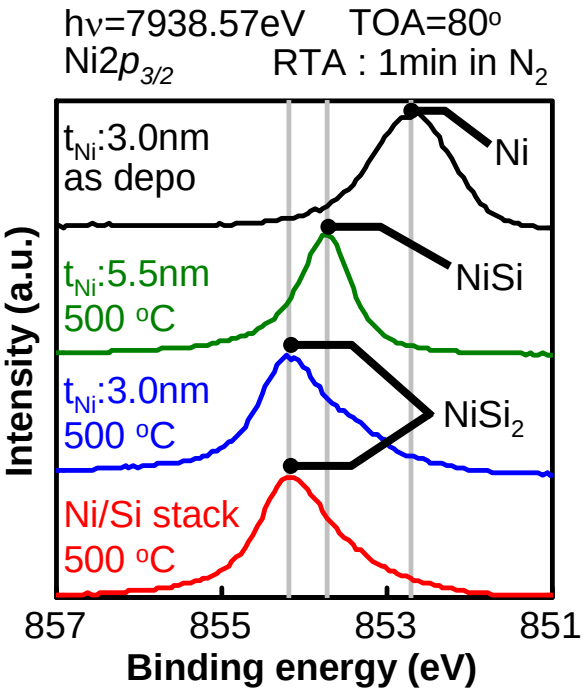


Figure 4.2.15 Ni $2p_{3/2}$ spectra of the silicide films annealed at 500 ^oC. The phase of stacked silicide is $NiSi_2$.

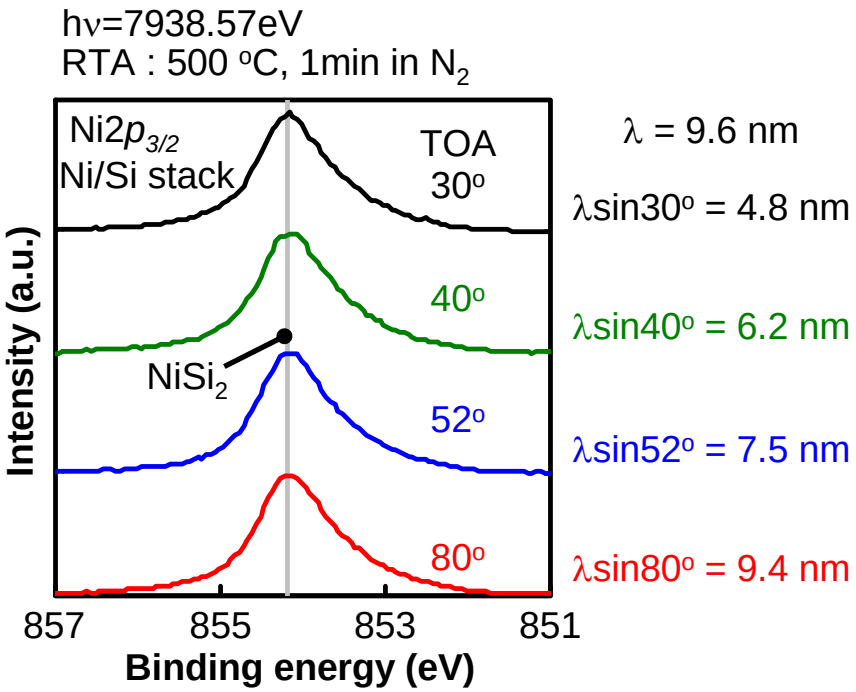


Figure 4.2.16 Ni $2p_{3/2}$ spectra of stacked silicide annealed at 500 ^{o}C measured by Angle Resolved-XPS (AR-XPS) changing TOAs from 30^{o} to 80^{o}. Stacked silicide film is uniform $NiSi_2$.

4.2.2.6 Annealing temperature dependent the phase of stacked silicide

Ni $2p_{3/2}$ spectra of stacked silicide annealed at various temperatures are shown in figure 4.2.17. The phase of stacked silicide is Ni-rich silicide from as deposited to 300 ^{o}C. At 325 ^{o}C, the phase of stacked silicide is Ni-rich silicide and $NiSi_2$. The Ni-rich silicide intensity decreased and $NiSi_2$ intensity increased with increase in annealing temperature, indicating that the residual Ni-rich silicide is converted to $NiSi_2$ by annealing. Therefore, the silicide phase change on annealing temperature corresponds with ρ_{sh} of stacked silicide on annealing temperature. Then, Ar 1s spectra of stacked silicide annealed at various temperatures are shown in figure 4.2.18. Ar intensity is large

from as deposited to 300 °C. Over 325 °C, Ar intensity decrease. This trend corresponds with the trend of ρ_{sh}. Therefore, it is speculated that the decrease of Ar in stacked silicide film causes the decrease of ρ_{sh}, which means formation of $NiSi_2$. In the following chapter, the relation between the amount of Ar in the stacked silicide film and the annealing temperature is investigated.

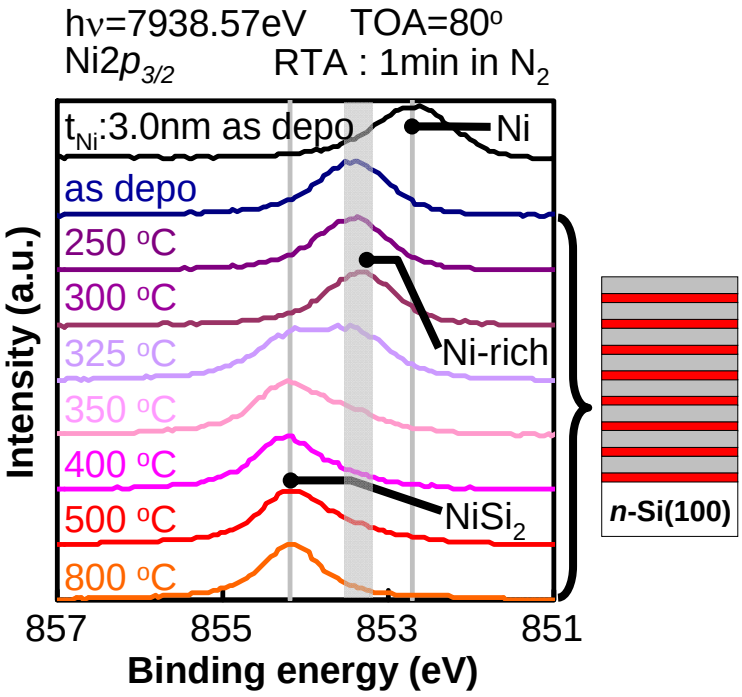


Figure 4.2.17 Ni $2p_{3/2}$ spectra of stacked silicide on annealing temperature. The phase of stacked silicide changes from Ni-rich silicide to $NiSi_2$ with increase in annealing temperature.

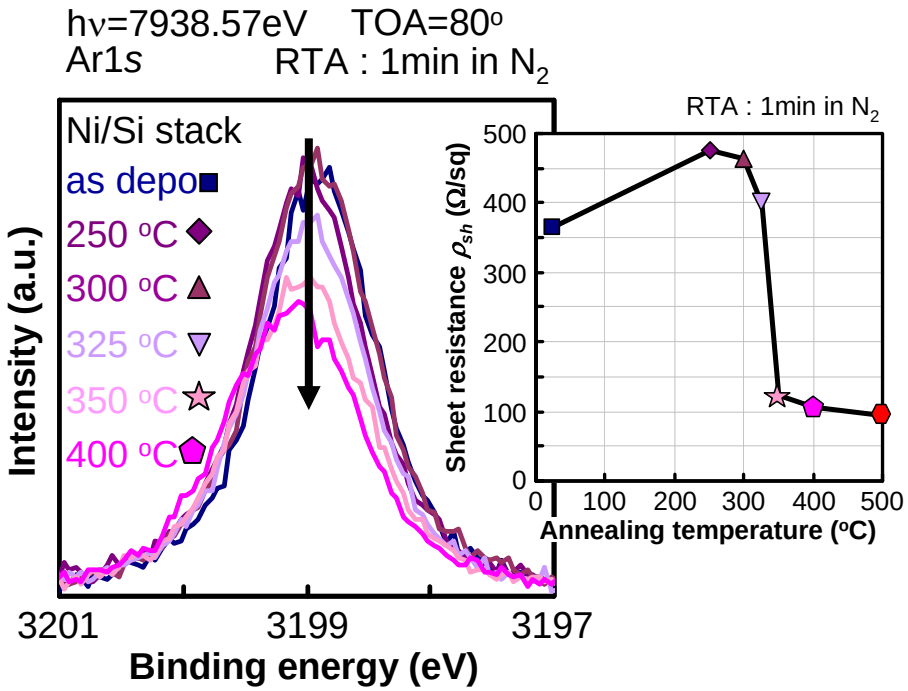


Figure 4.2.18 Ar 1s spectra of stacked silicide on annealing temperature. The decreasing of Ar intensity is related to the decreasing of ρ_{sh}.

4.2.2.7 The effect of sputtering pressure on sheet resistance of stacked silicide

As previously indicated, it is shown that there are Ar atoms into the silicide film and $NiSi_2$ is formed by desorption of Ar atoms from the silicide film with annealing. Thus, in this section, stacked silicide is deposited in various sputtering pressures to change the amount of Ar atoms in the silicide film. Thereby, the effect of Ar atoms which are in the silicide film on the formation of $NiSi_2$ is investigated.

The amount of Ar atoms in sputtering chamber by increasing sputtering pressure, consequently, it is considered that the amount of Ar atoms in silicide film increases. Also, there is a relationship between sputtering pressure and film properties, such as surface morphology, crystallographic orientation and grain size [4.2.15, 4.2.16].

Therefore, it is possible to relate to quality of $NiSi_2$.

Figure 4.2.19 shows the ρ_{sh} of stacked silicide on annealing temperature deposited in various sputtering pressures. The temperature of decreasing ρ_{sh} decreased with decrease in sputtering pressure. The sample of 0.55 Pa achieves the lowest ρ_{sh} and the lowest annealing temperature of formation of $NiSi_2$. Because for the sample of 0.55 Pa, the amount of initial Ar atoms in silicide film is few in comparison to the sample of 2 Pa, it can be formed $NiSi_2$ at lower annealing temperature. Thus, it is considered that $NiSi_2$ can be formed at low temperature by decreasing sputtering pressure to decrease the amount of Ar in the stacked silicide film.

The crystallinity of $NiSi_2$ film dependent on sputtering pressure is discussed below. Figure 4.2.20 shows XPS profile of stacked silicide which is deposited in 0.55 Pa annealed at 500^{o}C. $NiSi_2$(004) peak can be detected at $2\theta = 70.50^o$. Whereat, Rocking curve measurement (ω scan) at $2\theta = 70.50^o$ is shown in figure 4.17. Because rocking curve width is about 0.2^o which is narrow value, it is considered that $NiSi_2$ formed by stacked silicidation process is epitaxially grown. However, the crystallinity of the sample of 2 Pa is well in comparison to the sample of 0.55 Pa from the result of rocking curve width (figure 4.2.11). From the results of ρ_{sh}, it is considered that $NiSi_2$ is formed by desorption of Ar atom from stacked silicide film. However, from the XRD profiles, the crystallinity of $NiSi_2$ is good when the the amount of Ar in the film is few. The relationship of these results has not cleared yet. SIMS profile of Ar should be measured.

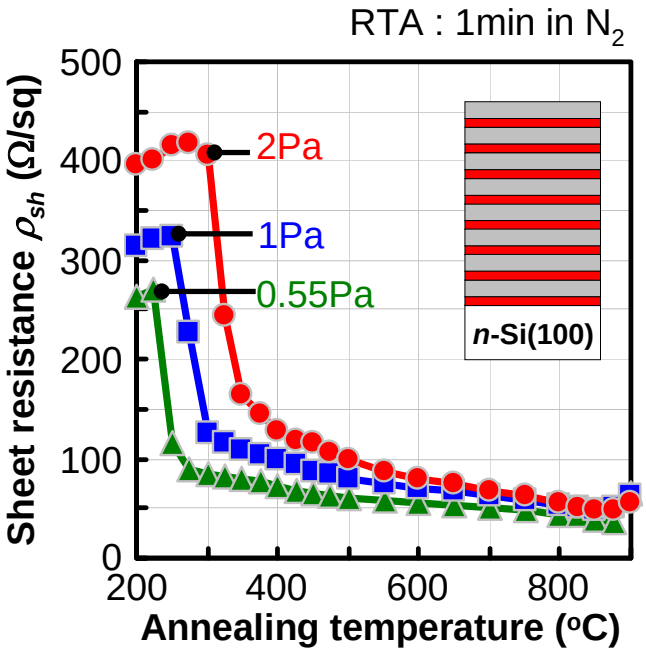


Figure 4.2.19 ρ_{sh} of stacked silicide on annealing temperature. ρ_{sh} of stacked silicide is stable at wide process window. When the sputtering pressure is 0.55 Pa, ρ_{sh} decrease occurs at the lowest annealing temperature.

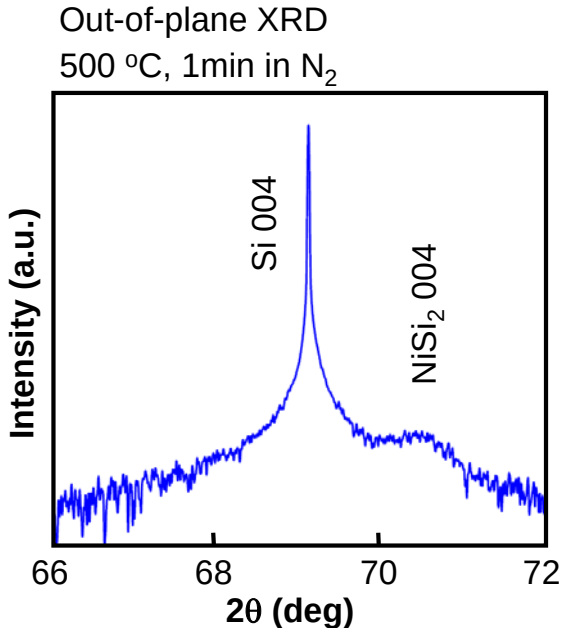


Figure 4.2.20 Out-of-plane XRD (2θ/ω scan) profile of stacked silicide annealed at 500 °C. $NiSi_2$(004) peak can be detected at 2θ = 70.50°.

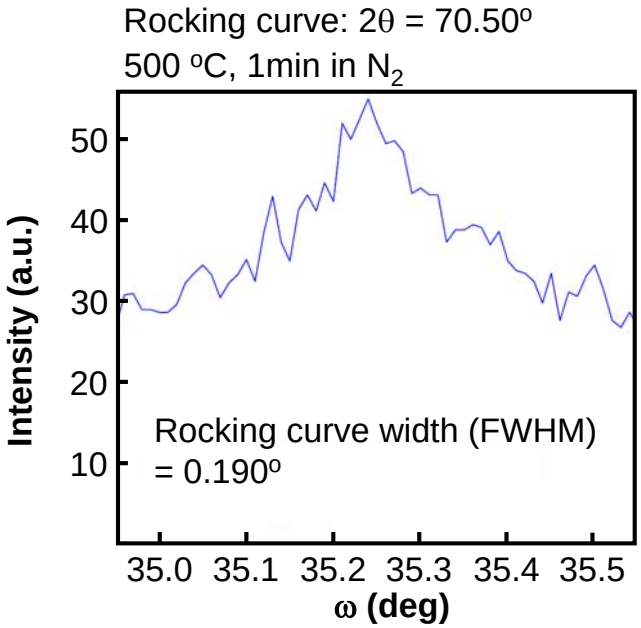


Figure 4.2.21 Rocking curve measurement (ω scan) at 2θ = 70.50°. Because rocking curve width is about 0.2° which is narrow value, it is considered that $NiSi_2$ formed by stacked silicidation process is epitaxially grown.

4.2.2.8 Stacked silicidation process of other semiconductor substrates

4.2.2.8.1 Characteristics of stacked silicide on different Si orientation

Figure 4.2.22 shows the ρ_{sh} of stacked silicide which is several thicknesses deposited on various oriented Si substrates. Figure 4.2.22(a), (b) and (c) show Si(100), Si(110) and Si(111), respectively. In these results, morphology of stacked silicide is stable at wide temperature range independent of stacked silicide thickness and Si substrate orientations. Therefore, it is considered that the stacked silicidation process is promising for Si Fin or Si nanowire FETs.

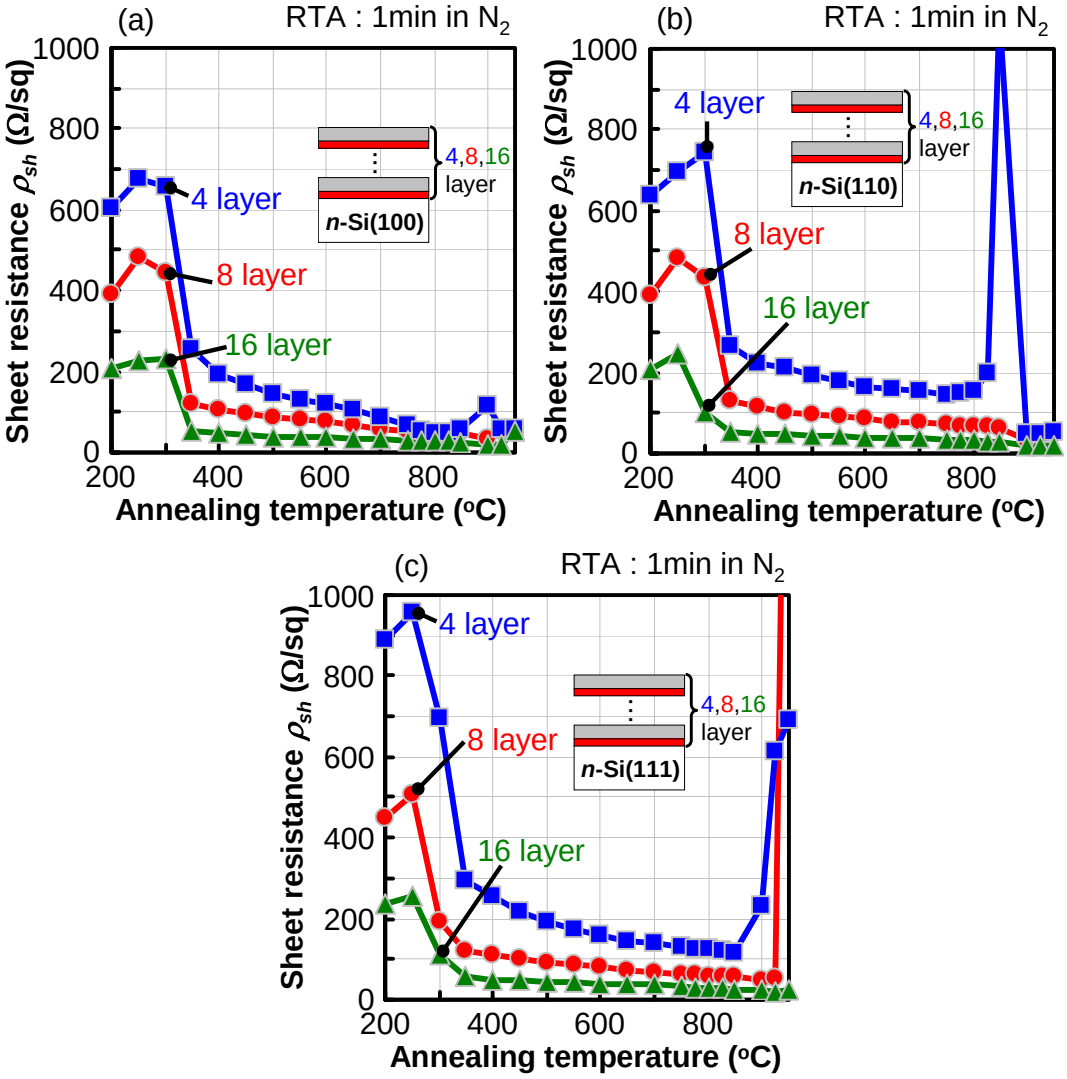


Figure 4.2.22 ρ_{sh} of different stacked silicide thickness on annealing temperature. Each stacked silicide is deposited on (a) n-Si(100), (b) n-Si(110) and (c) n-Si(111) substrate. ρ_{sh} of stacked silicide is stable at wide process window independent of Si substrate orientation.

4.2.2.8.2 Characteristics of stacked silicide on other semiconductor substrates

Germanium has been receiving attention as an alternative channel material [4.2.17, 4.2.18] because of its high intrinsic mobility (two times higher for electrons and four times higher for holes as compared to those in silicon). Reduction of parasitic resistance

of metallic contact on Ge substrate is one of the issues for Ge FETs, and low contact resistance of NiGe with Ge substrate has been studied as metallic contact on Ge substrate [4.2.19]. However, agglomeration of NiGe roughens metal/Ge interface thereby increasing the sheet resistance at the interface [4.2.20]. Therefore, in order to obtain resistant agglomeration compared to NiGe, Ni/Si stacked silicidation process is applied for Ge substrate.

Figure 4.2.23 shows ρ_{sh} of stacked silicide on Ge substrate on annealing temperature. Although small sheet resistance could be obtained by forming NiGe on Ni films, process temperature were limited (Ni-5.5-nm film was from 250 ^{o}C to 375 ^{o}C) due to agglomeration of the NiGe surface. On the other hand, once $NiSi_2$ is formed over 350 ^{o}C, stable sheet resistances can be obtained up to 700 ^{o}C, which gives process compatibility for dopant activation in Ge devices.

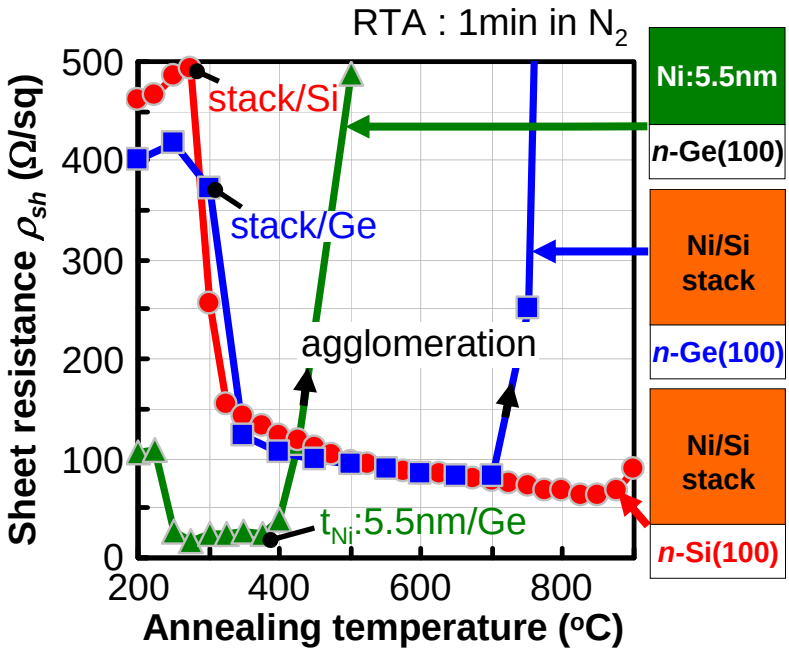


Figure 4.2.23 ρ_{sh} of stacked silicide on Ge substrate on annealing temperature. ρ_{sh} of stacked silicide on Ge is more stable than that of 5.5-nm-thick Ni layer on Ge.

GaN based devices have been focused as a semiconductor for power electronics applications [4.2.21]. One of the issues is that metal contact with GaN based devices is degraded by surface agglomeration. Thus, it is proposed that stacked silicidation process is applied for GaN based devices.

Figure 4.2.24 shows ρ_{sh} of stacked silicide on GaN and AlGaN substrates on annealing temperature. It is considered that stable rsh can be obtained due to suppression of interface reaction and formation $NiSi_2$ at low temperature.

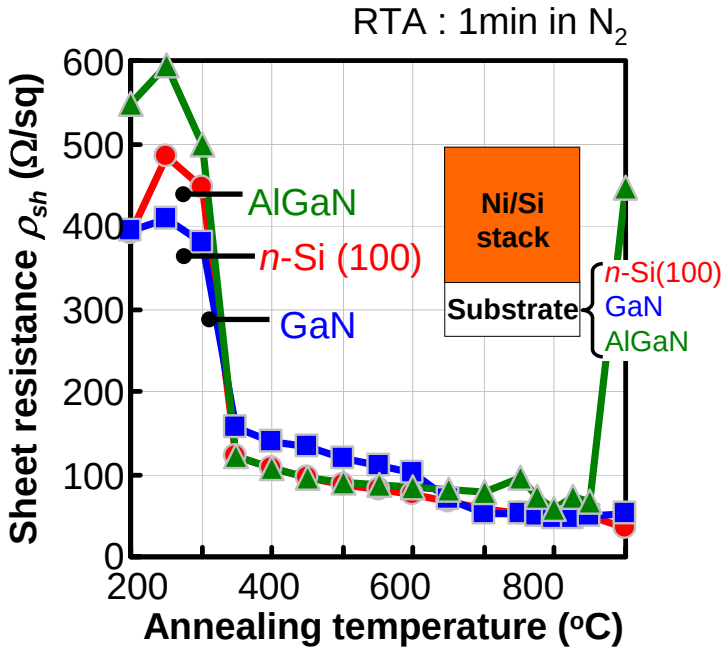


Figure 4.2.24 ρ_{sh} of stacked silicide on GaN and AlGaN substrates on annealing temperature. ρ_{sh} of stacked silicide on each substrate is stable.

4.2.2.9 Extension of stacked silicidation process for Ti

$TiSi_2$ is the most stable phases in Ti silicides, however, there are two crystal structure in $TiSi_2$. One is C49-$TiSi_2$ and the other is C54-$TiSi_2$ [4.2.22]. C54-$TiSi_2$ is the most stable phase in Ti silicides [4.2.23]. C54-$TiSi_2$ has been used due to low resistivity but there are some issues. One of the issues is that formation temperature is high and the other is degradation of surface morphology by agglomeration [4.2.24]. As previous indicated, stacked silicidation process using Ni has some advantages compared to conventional Ni silicidation process. Thus, it is investigated about extension of stacked silicidation process for Ti as shown in figure 4.2.25.

Figure 4.2.26 shows ρ_{sh} of Ti silicide formed by stacked silicidation process and by deposition 20-nm-thick Ti layer on annealing temperature. In 20-nm-thick Ti layer, it is confirmed that ρ_{sh} decreases over 600 ^{o}C and further decreases at 800 ^{o}C that correspond with formation of C49-$TiSi_2$ and C54-$TiSi_2$, respectively. On the other hand, Ti/Si stacked silicidation process shows different trend to 20-nm-thick Ti layer. Moreover, Ti/Si stacked silicide can not achieve stable ρ_{sh} at wide range temperature range.

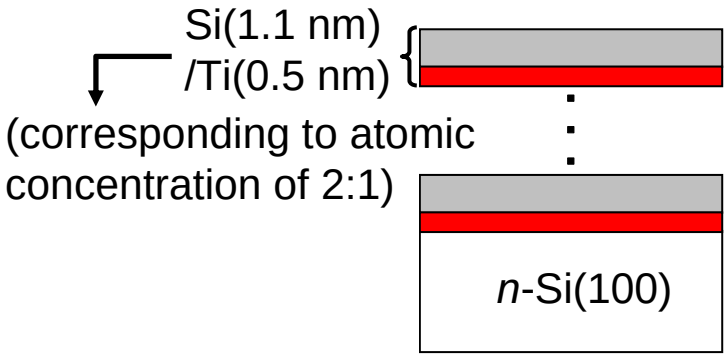


Figure 4.2.25 Schematic illustration of Ti/Si stacked silicidation process. A set of Si/Ti, with an atomic ratio of 2:1, is cyclically stacked on n-Si (100)

substrates.

The reaction of Ti/Si stacked silicide is between thin-Ti-layer and thin-Si-layer, on the other hand, the reaction of 20-nm-thick Ti layer is between thick-Ti-layer and single crystal Si substrate. Therefore, it is considered that the phase or crystallinity of these samples is different. However, the phase and crystallinity of Ti/Si stacked silicide is not still measured. It is considered that to form the most stable silicide phase by stacked silicidation process at wide process temperature range is unique characteristics of Ni silicide.

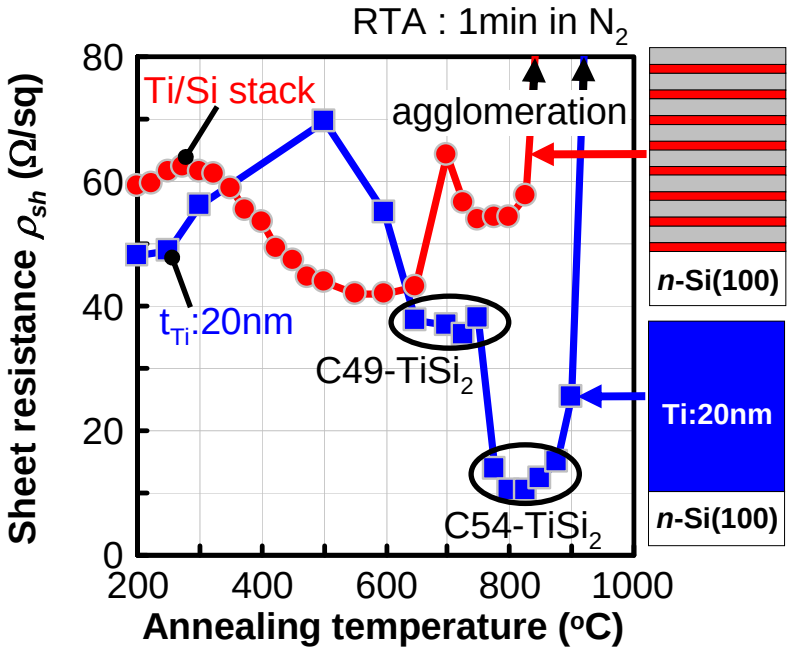


Figure 4.2.26 ρ_{sh} of Ti silicide which is formed by Ti/Si stacked silicidation process and 20-nm-thick-Ti layer on annealing temperature.

4.2.2.10 Conclusion

In order to achieve the control of interface reaction and stable composition and

morphology at wide temperature range, stacked silicidation process has been investigated. It is realized that an atomically flat interface and surface are formed before and after annealing and Ni atoms encroachment into Si Fin is suppressed completely. In fact, it is an advantage for scaled 3D devices that the shape of Si substrate after silicidation does not change due to suppression of interface reaction.

Second, it is achieved that $NiSi_2$ which is formed by staked silicidation process is stable composition and morphology at wide temperature range. Moreover, it is suggested that $NiSi_2$ formation is advanced by desorption of Ar atoms which are in silicide films.

Third, it is accomplished that the ρ_{sh} of stacked silicide on various substrates is stable at wide temperature range. Stacked silicidation process can be applied for 3D Si channel and other semiconductor substrates.

And finally, extension of stacked silicidation process for Ti has been examined. It is considered that to form the most stable silicide phase by stacked silicidation process at wide process temperature range is unique characteristics of Ni silicide.

As discussed above, it is considered that Ni/Si stacked silicidation process is the key for future scaled 3D SB-FET.

4.2.3Electrical characteristics of Ni silicide Schottky diodes

4.2.3.1 Introduction

In previous sections, the physical properties of silicide films, which are formed by different methods, such as interface reaction, composition and morphology are examined. In this chapter, the electrical characteristics of Schottky diodes which are

formed by those silicides are investigated.

There are some problems in Ni silicide Schottky diodes [4.2.25]. One is increasing the reverse leakage current because of the leakage current at the electrode periphery where excess silicidation occurs, and the other is the variation of ϕ_{Bn} and n-factor due to existing on roughness and facets at the interface and the electrode periphery. Thus, to obtain the ideal Schottky diode characteristics, it is necessary to achieve an atomically flat interface including the electrode periphery. In this chapter, therefore, Schottky diode characteristics using stacked silicidation process which can be obtained an atomically flat interface are investigated.

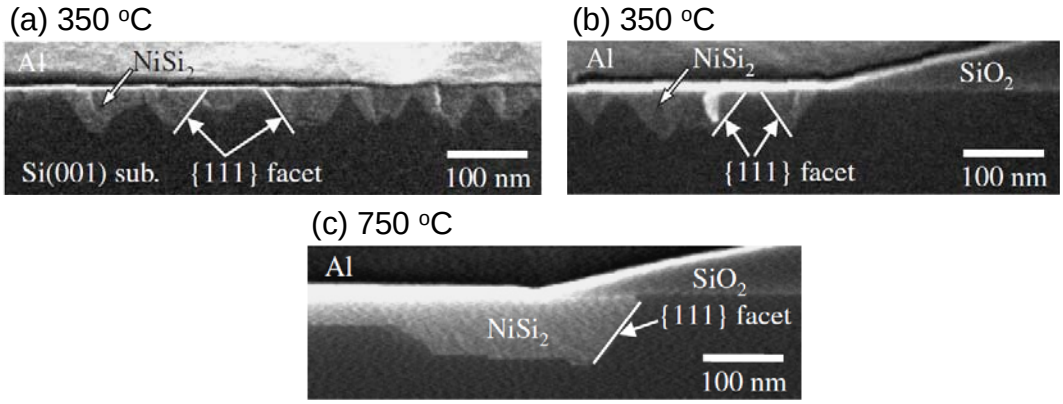


Figure 4.2.27 the presence of facets and roughness which occur leakage currents at interface and periphery [5.1].

4.2.3.2 Schottky diode characteristics

Figure 4.2.28 shows diode current density-voltage (*J*-*V*) characteristics of the fabricated Ni silicide Schottky diodes. For 3-nm-thick and 5.5-nm-thick Ni samples, the increase of reverse current from theoretical value was observed. On the other hand, for

stacked silicide, the increase of reverse current from theoretical was not observed. Figure 4.2.29 shows ϕ_{Bn} and ideality factor (n-factor) extracted by J-V characteristics on annealing temperature. For stacked silicide, it is observed that ϕ_{Bn} is stable value 0.61 ~ 0.63 eV and n-factor is less than 1.05 up to 700 °C. On the other hand, for 3.0-nm-thick and 5.5-nm-thick Ni samples, ϕ_{Bn} was not stable and n-factor was worse than that of stacked silicide. From these results, it is considered that these differentials between stacked silicide and conventional silicides depend on a method of silicide formation. For conventional silicide which formed by reacting between Ni film and Si substrate, issues of interface reaction such as excessive growth of silicide at the periphery of the electrodes and formation of plane orientation which is not Si(100) existed [4.2.25, 4.2.26]. Thereby, it is considered that increasing reverse current from theoretical value and variation of ϕ_{Bn} and n-factor occurred. On the other hand, for stacked silicide, issues of interface such as conventional silicide did not occur because stacked silicide was able to form suppressing the reaction with Si substrate as shown in figure 4.2.1. Using stacked silicide, the issues of conventional silicide are overcome.

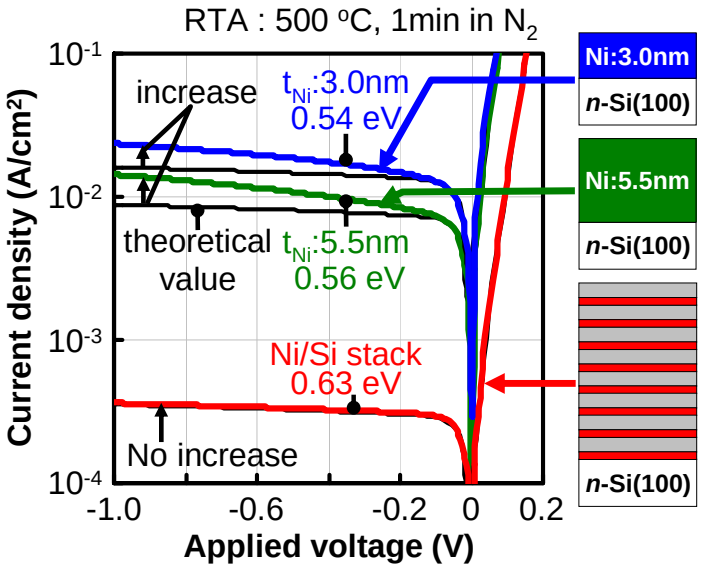


Figure 4.2.28 The Schottky diode J-V characteristics of stacked silicide, 3.0-nm- and 5.5-nm-thick Ni layers. J-V characteristic of stacked silicide is ideal.

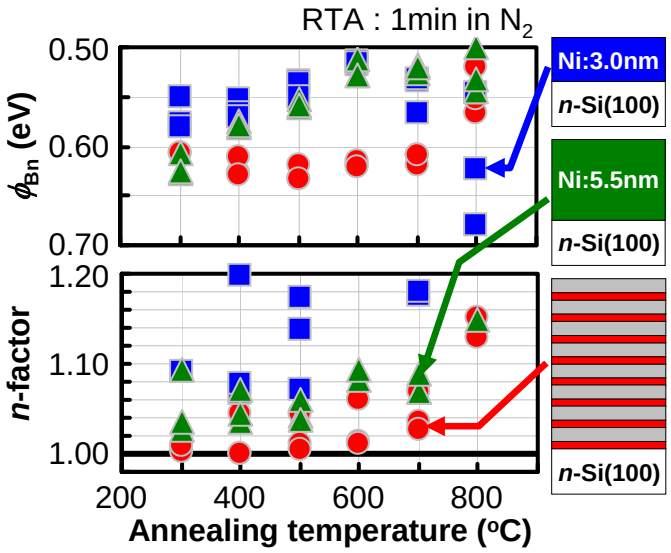


Figure 4.2.29 ϕ_{Bn} and n-factor of stacked silicide, 3.0-nm- and 5.5-nm-thick Ni layers on annealing temperature. ϕ_{Bn} and n-factor of stacked silicide are stable value up to 700 °C.

4.2.3.3 TiN capping on stacked silicide

Ni silicides should be protected by etchant, which is used in etching process, in fabrication process of transistors because Ni silicides can be etched by HF [4.2.27]. Then, the protection of Ni silicides by TiN capping is proposed. In this section, the effect of TiN capping on electrical characteristics is stated.

Figure 4.2.30 shows the fabrication procedures of Schottky diodes with or without TiN capping. 50-nm-TiN layer is deposited by sputtering.

Figure 4.2.31 shows *J-V* characteristics of diodes with or without TiN capping. It is clear that *J-V* characteristics remain ideal even with TiN capping. However, ϕ_{Bn} of with

TiN capping is a little bit larger than that of without TiN capping. Figure 4.2.32 shows ϕ_{Bn} and ideality factor (n-factor) extracted by J-V characteristics on annealing temperature. It is investigated that stable ϕ_{Bn} and n-factor remain even with TiN capping, furthermore, scatter of ϕ_{Bn} and n-factor with TiN capping is suppressed compared with without TiN capping. Therefore, it is considered that TiN capping on stacked silicide does not degrade electrical characteristics of Schottky diode.

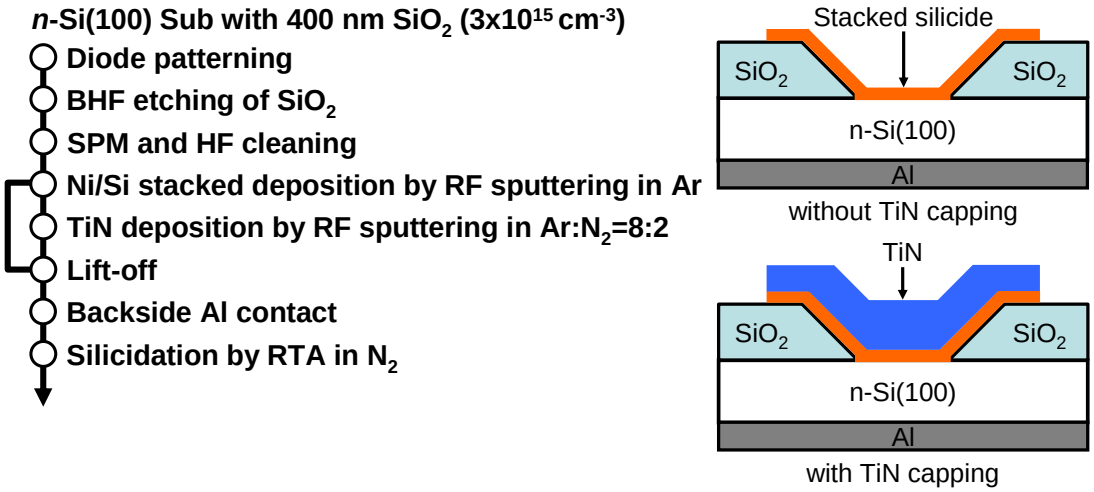


Figure 4.2.30 Fabrication processes of Schottky diodes with or without TiN capping.

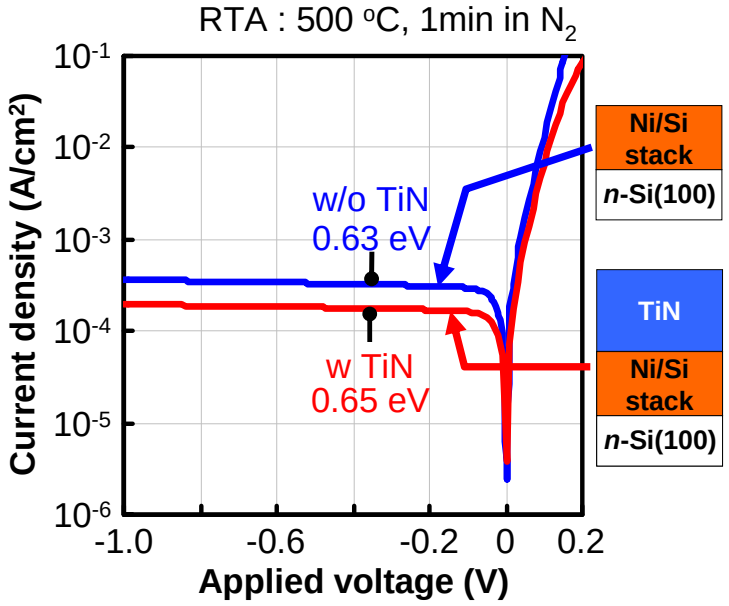


Figure 4.2.31 The Schottky diode J-V characteristics of stacked silicide with or without TiN capping. J-V characteristics remain ideal characteristics even with TiN capping.

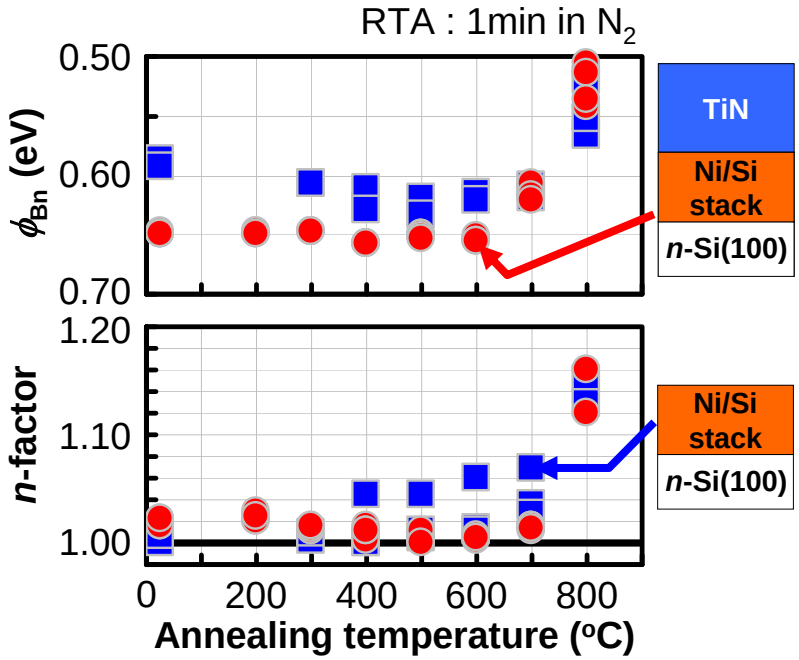


Figure 4.2.32 ϕ_{Bn} and n-factor of stacked silicide with or without TiN capping on annealing temperature. Scatter of ϕ_{Bn} and n-factor with TiN capping is suppressed compared with without TiN capping.

4.2.3.4 Conclusion

Electrical characteristics of Schottky diodes using Ni silicides are investigated. Schottky diode characteristics of conventional Ni silicides show the reverse leakage current and the variation of ϕ_{Bn} and *n*-factor due to excess silicidation at the electrode periphery. On the other hand, those of stacked silicide are achieved ideal diode characteristics and robust ϕ_{Bn} and *n*-factor because of formation of an atomically flat interface including the electrode periphery. Moreover, more robust ϕ_{Bn} and *n*-factor even

with ideal *J-V* characteristics are obtained by TiN capping on stacked silicide.

4.2.4 References of this section

[4.2.1] H. Iwai, T. Ohguro, S Ohmi, ”NiSi salicide technology for scaled CMOS”, Microelectron. Eng. 60, pp.157-169 (2002).

[4.2.2] K. Tsutsui, R. Xiang, K. Nagahiro, T. Shiozawa, P. Ahmet, Y. Okuno, M. Matsumoto, M. Kubota, K. Kakushima, and H. Iwai, “Analysis of irregular in sheet resistance of Ni silicides on transition from NiSi to $NiSi_2$”, Microelectron. Eng., 85, pp.315-319 (2008).

[4.2.3] T. P. Nolan and R. Sinclair, R. Beyers, “Modeling of agglomeration in polycrystalline thin films: Application to $TiSi_2$ on a silicon substrate”, J. Appl. Phys., 71, pp.720-724 (1992).

[4.2.4] K. De Keyser, C. Van Bockstael, R. L. Van Meirhaeghe, C. Detavernier, E. Verleysen, H. Bender, W. Vandervorst, J. Jordan-Sweet, and C. Lavoie, “Phase formation and thermal stability of ultrathin nickel-silicides on Si(100)”, Appl. Phys. Lett., 96, pp.173503 (2010).

[4.2.5] C. Lavoie, C, Detavernier, C. Cabral Jr., F. M. d’Heurle, A. J. Kellock, J. Jordan-Sweet, J. M. E. Harper, ”Effects of additive elements on the phase formation and morphological stability of nickel monosilicide films”, Microelectron. Eng., 83, pp.2042-2054 (2006).

[4.2.6] L. Knoll, Q. T. Zhao, S. Habicht, C. Urban, B. Ghyselen, and S. Mantl, “Ultrathin Ni Silicides With Low Contact Resistance on Strained and Unstrained Silicon”, IEEE Electron Devices Lett., 31, pp.350-352 (2010).

[4.2.7] L. J. Chen, “*Silicide Technology for Integrated Circuits*”, London: The Institute

of Electrical Engineers (2004).

[4.2.8] P. J. Grunthaner and F. J. Grunthaner, A. Madhukar, Chemical bonding and charge redistribution: Valence band and core level correlations for the Ni/Si, Pd/Si, and Pt/Si systems J. Vac. Sci. Technol., 20, pp.680-683 (1982).

[4.2.9] S. Ray, J. Hommet, G. Schmerber, F. Le Normand, “Diamond growth on polycrystalline nickel silicides”, J. Crys. Grow., 216, pp.225-234 (2000).

[4.2.10] M. Koyama, N. Shigemori, K. Ozawa, K. Tachi, K. Kakushima, O. Nakatsuka, K. Ohmori, K. Tsutsui, A. Nishiyama, N. Sugii, K. Yamada and H. Iwai, “Si/Ni-Silicide Schottky Junctions with Atomically Flat Interfaces using $NiSi_2$ Source”, Proc. 41st ESSDERC, pp.231-234 (2011).

[4.2.11] K. De Keyser, C. Van Bockstael, R. L. Van Meirhaeghe, C. Detavernier, E. Verleysen, H. Bender, W. Vandervorst, J. Jordan-Sweet, and C. Lavoie, “Phase formation and thermal stability of ultrathin nickel-silicides on Si(100)”, Appl. Phys. Lett., 96, pp.173503 (2010).

[4.2.12] O. Nakatsuka, A. Suzuki, S. Akimoto, A. Sakai, M. Ogawa and S. Zaima, “Dependence of Electrical Characteristics on Interfacial Structure of Epitaxial $NiSi_2$/Si Schottky Contacts Formed from Ni/Ti/Si System”, J. J. Appl. Phys., 47, pp.2402-2406 (2008).

[4.2.13] H. Arai, H. Kamimura, S. Sato, K. Kakushima, P. Ahmet, K. Tsutsui, N. Sugii, K. Natori, T. Hattori, H. Iwai, ” Annealing Reaction for Ni Silicidation of Si Nanowire”, ECS Trans., 25, pp.447-454 (2009).

[4.2.14] N. Shigemori, S. Satou, K. Kakushima, P. Ahmet, K. Tsutsui, A. Nishiyama, N. Sugii, K. Natori, T. Hattori, H. Iwai, “Suppression of Lateral Encroachment of Ni Silicide into Si Nanowires using Nitrogen Incorporation”, ECS Trans., 33, pp.19-26

(2011).

[4.2.15] John A. Thornton, “Influence of apparatus geometry and deposition conditions on the structure and topography of thick sputtered coatings”, J. Vac. Sci. Technol., 11, pp.666-670 (1974).

[4.2.16] John A. Thornton, “The microstructure of sputter-deposited coatings”, J. Vac. Sci. Technol. A, 4, pp.3059-3065 (1986).

[4.2.17] A. Ritenour, S. Yu, M. L. Lee, N. Lu, W. Bai, A. Pitera, E. A. Fitzgerald, D. L. Kwong, and D. A. Antoniadis, “Epitaxial strained germanium p-MOSFETs with HfO_2 gate dielectric and TaN gate electrode”, IEDM Tech. Dig., pp.433 (2003).

[4.2.18] C. O. Chui, S. Ramanathan, B. B. Triplet, P. C. McIntyre, and K. C. Saraswat, “Germanium MOS Capacitors Incorporating Ultrathin High-k Gate Dielectric”, IEEE Electron Device Lett., 23, pp.473 (2002).

[4.2.19] X. V. Li, M. K. Husain, M. Kiziroglou, and C.H. de Groot, “Inhomogeneous Ni/Ge Schottky barriers due to variation in Fermi-level pinning”, Microelectronic Engineering, 86, pp.1599-1602 (2009).

[4.2.20] Q. Zhang, N. Wu, T. Osipowicz, L. K. Bera, and C. Zhu, “Formation and Thermal Stability of Nickel Germanide on Germanium Substrate”, J. J. Appl. Phys., pp.44, L1389-L1391 (2005).

[4.2.21] O. Ambacher, “Growth and applications of Group III-nitrides”, J. Phys. D, 31, pp.2653-2710 (1998).

[4.2.22] L. J. Chen, “Silicide Technology for Integrated Circuits”, The Institution of Electrical Engineers, London (2004).

[4.2.23] K. L. Saenger, C. Cabral, Jr., L. A. Clevenger, R. A. Roy and S. Wind, “A kinetic study of the C49 to C54 TiSi2 conversion using electrical resistivity

measurements on single narrow lines", J. Appl. Phys., 78, pp.7040-7044 (1995).

[4.2.24] T. P. Nolan and R. Sinclair, R. Beyers, "Modeling of agglomeration in polycrystalline thin films: Application to $TiSi_2$ on a silicon substrate", J. Appl. Phys., 71, pp.720-724 (1992)

[4.2.25] O. Nakatsuka, A. Suzuki, S. Akimoto, A. Sakai, M. Ogawa and S. Zaima, "Dependence of Electrical Characteristics on Interfacial Structure of Epitaxial $NiSi_2$/Si Schottky Contacts Formed from Ni/Ti/Si System", J. J. Appl. Phys., 47, pp.2402-2406 (2008).

[4.2.26] L. Knoll, Q. T. Zhao, S. Habicht, C. Urban, B. Ghyselen, and S. Mantl, "Ultrathin Ni Silicides With Low Contact Resistance on Strained and Unstrained Silicon", IEEE Electron Devices Lett., 31, pp.350-352 (2010).

[4.2.27] S. P. Murarka, "SILICIDES FOR VLSI APPLICATIONS", Academic Press, New York (1983).

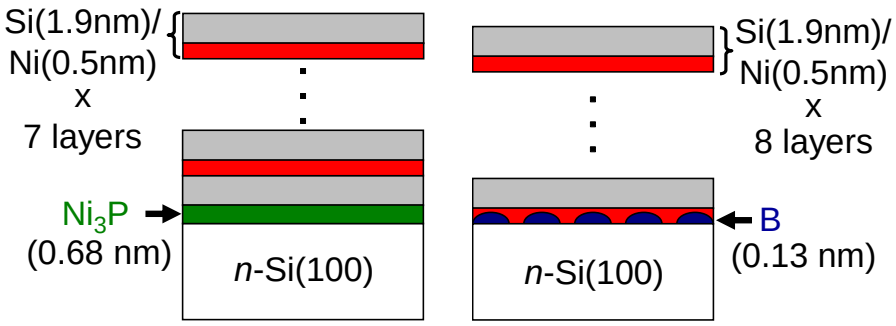
4.3 Schottky barrier height modulation

4.3.1 Introduction

As described in chapter 3, it is necessary to modulate ϕ_B to achieve SB-FET with high performance [4.3.1]. ϕ_B modulation has been achieved by dopant segregation using ion implantation, however, there are some issues [4.3.2, 4.3.3]. Thereby, it is proposed that the method of impurity incorporation without ion implantation, and ϕ_B modulation by the impurity incorporation is examined.

In this study, P and B are used as impurity. It is reported that ϕ_{Bn} becomes small value by P and ϕ_{Bn} becomes large value by B [4.3.4, 4.3.5]. The method of impurity incorporation with stacked silicidation process is to deposit Ni_3P or B by sputtering. For B incorporation, pure B target is used for sputtering, whereas for P case, a 0.68-nm-thick Ni_3P layer is deposited instead of the first 0.5-nm-thick Ni layer as shown in figure 4.3.1. The number of Ni atoms in 0.68-nm-thick-Ni_3P layer equals that of 0.5-nm-thick Ni layer. This method can incorporate impurity without ion implantation, moreover, the control of impurity position is expected because stacked silicidation process can suppress interface reaction.

In this chapter, interface reaction with impurity incorporation at the interface, impurity profiles and electrical characteristics with impurity incorporation are investigated. Furthermore, ϕ_{Bn} modulation depending on impurity position and amount are examined.



impurity	process
P	(Ni/Si)x7+(Ni_3P/Si)
B	(Ni/Si)x8+B

Figure 4.3.1 Schematic illustration of stacked silicidation process with impurity incorporation. P is incorporated at the interface by 0.68-nm-thick Ni_3P deposition instead of the first Ni layer. B is incorporated at the interface.

4.3.2 ϕ_{Bn} modulation with stacked silicidation process

4.3.2.1 Interface reaction of impurity incorporation

As shown in figure 4.3.2, TEM images of silicide/Si interface formed from Ni/Si stacked silicidation process incorporated P (Figure 4.3.2(a)) and B (Figure 4.3.2(b)) at the interface at annealed 500 ^{o}C for 1 min in N_2 ambient. TEM images revealed no change in the thickness and atomically flat interface and surface. Even with impurity incorporation, the interface reaction with stacked silicidation process is also maintained.

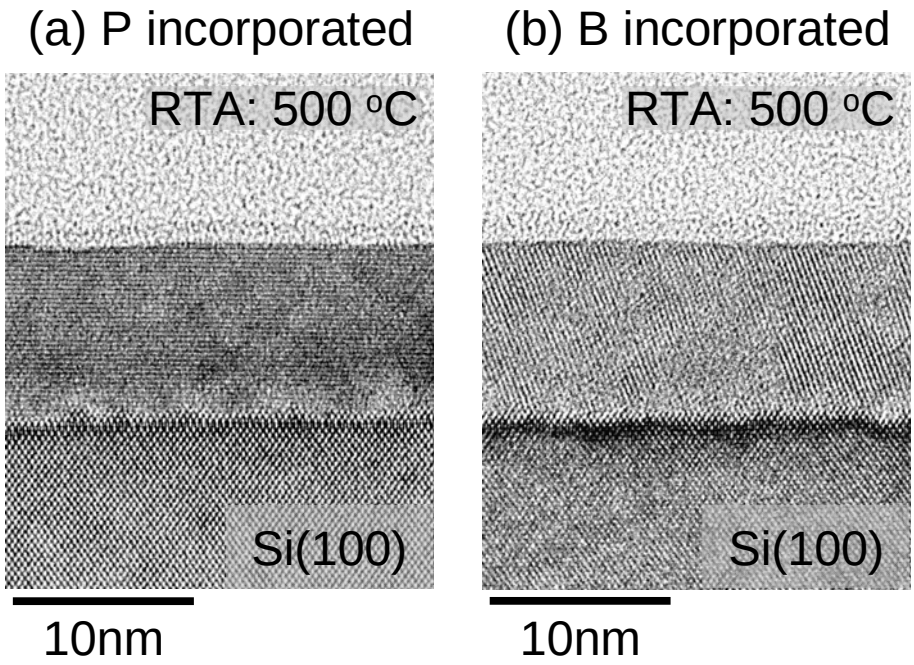


Figure 4.3.2 TEM images of stacked silicidation process incorporated (a) P and (b) B at the interface after annealing at 500 °C. Even with impurity incorporation, atomically flat interface and surface are maintained.

4.3.2.2 SIMS impurity profiles

Figure 4.3.3 shows SIMS profiles of (a) P and (b) B before and after annealing when impurities incorporated at interface. Although some of the impurities diffused into silicide layer, significant amount of them remained at the silicide/Si interface which is initial incorporated position. Therefore, impurity position can be controlled by stacked silicidation process because stacked silicidation process can be suppressed interface reaction.

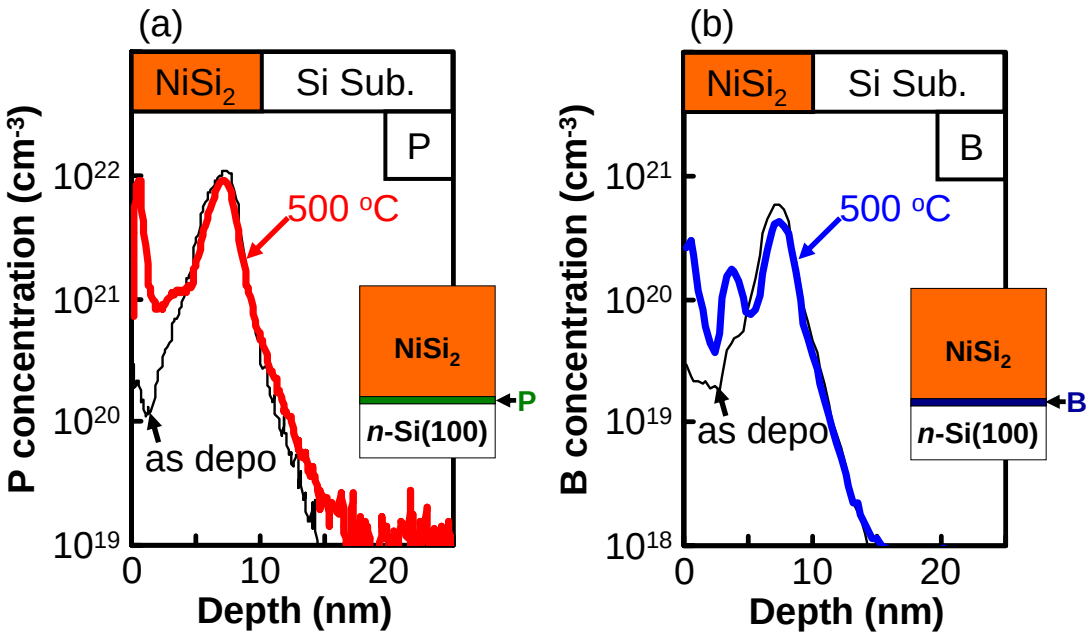


Figure 4.3.3 SIMS profiles of (a) P and (b) B before and after annealing. Although some of the impurities diffused into silicide layer, significant amount of them remained at silicide/Si interface.

4.3.2.3 ϕ_{Bn} modulation by impurity incorporation

Figure 4.3.4 shows the *J-V* characteristics of the stacked silicide Schottky diodes with P and B incorporation annealed at 500 °C. ϕ_{Bn} can be effectively modulated by placing P or B atoms at the interface, where the initial ϕ_{Bn} of 0.63 eV was modulated to ohmic and 0.68 eV, respectively. Furthermore, robust ϕ_{Bn} and *n*-factor were obtained at wide process window as shown in figure 4.3.5.

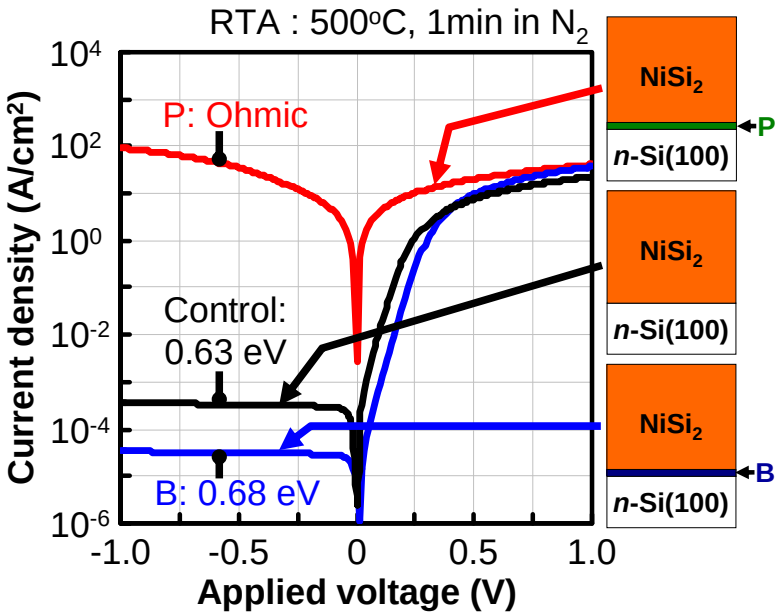


Figure 4.3.4 J-V characteristics of stacked silicide with P and B incorporation annealed at 500 °C. Successful effectively ϕ_{Bn} shift by P or B incorporation with stacked silicidation process.

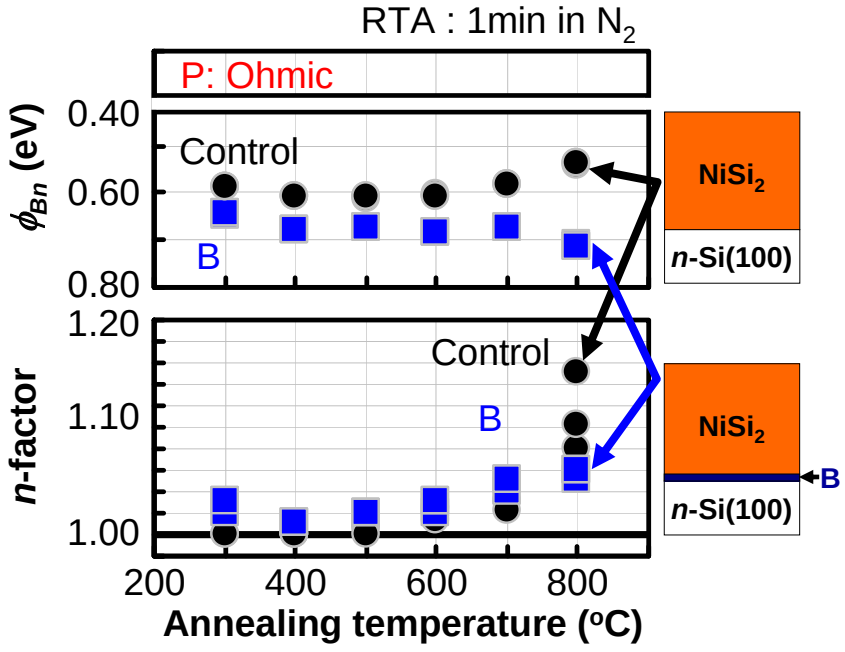


Figure 4.3.5 ϕ_{Bn} and n-factor of the diodes extracted from J-V characteristics depending on annealing temperature. Ohmic characteristic and larger ϕ_{Bn} is realized by incorporating P and B, respectively. ϕ_{Bn} and n-factor were stable up to 700 °C.

4.3.3 ϕ_{Bn} controllability by impurity incorporation

4.3.3.1 Annealing conditions dependent *J-V* characteristics with impurity at the interface

Figure 4.3.6 shows *J-V* characteristics of stacked silicide incorporated P at the interface annealed at (a) 400 ^{o}C, (b) 500 ^{o}C and (c) 600 ^{o}C for 1 min and 30 min. As shown in figure 6.6(a), annealed at 400 ^{o}C, large current density can be obtained by annealing for 30 min compared to the sample annealed for 1 min. On the other hand, current density is almost unchanged annealed 500 ^{o}C and 600 ^{o}C independent of annealing time. Therefore, large current density can be achieved by long time or high temperature annealing.

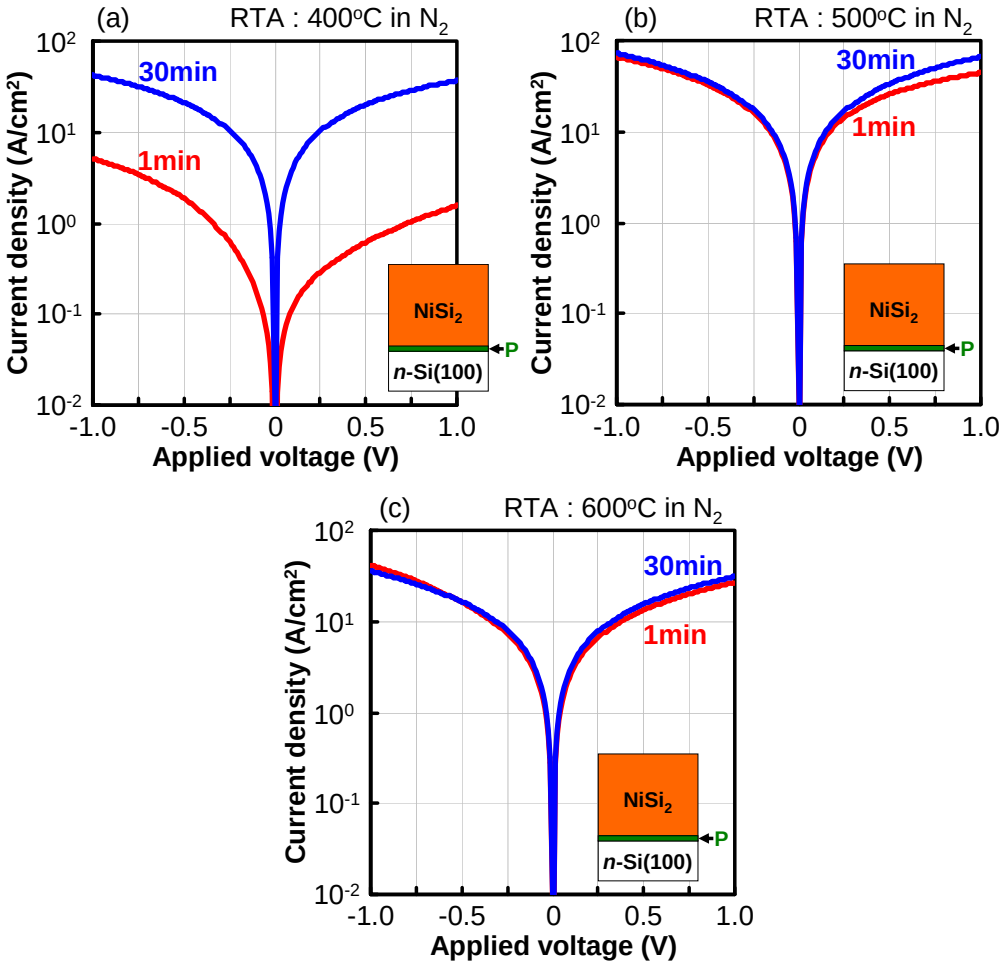


Figure 4.3.6 J-V characteristics of stacked silicide incorporated P at the interface annealed at (a) 400 °C, (b) 500 °C and (c) 600 °C for 1 and 30 min. Ohmic characteristics can be achieved by long time or high temperature annealing.

4.3.3.2 Impurity position dependent *J-V* characteristics

As shown in figure 4.3.6, when P is incorporated at the interface, ohmic characteristics can be obtained by annealing at 500 °C for 1min. In this chapter, the impurity position dependent *J-V* characteristics investigated. Figure 4.3.7 shows *J-V* characteristics of stacked silicide depending on the position of P incorporation annealed at 500 °C for 1 min. When the position of P incorporation gradually comes

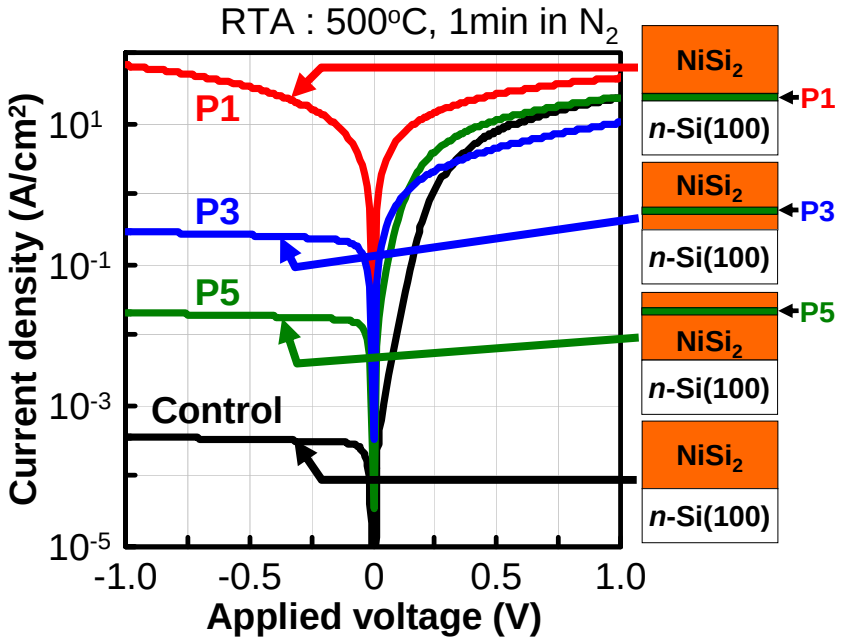


Figure 4.3.7 J-V characteristics of stacked silicide dependent the position of P incorporation annealed at 500 °C. When the position of P incorporation gradually comes close to the interface, small ϕ_{Bn} and ohmic characteristic are obtained.

close to the interface, small ϕ_{Bn} and ohmic characteristic are obtained. Therefore, it is considered that P which exists at interface is the key to modulate ϕ_{Bn}.

4.3.3.3 Annealing conditions dependent *J-V* characteristics with impurity far from the interface

Figure 4.3.8 shows *J-V* characteristics of stacked silicide incorporated P far from the interface annealed at (a) 400 °C, (b) 500 °C and (c) 600 °C for 1 min and 30 min. As shown in figure 4.3.8(a), which is annealed at 400 °C, *J-V* characteristics are Schottky characteristics both of annealing for 1min and 30 min, however, ϕ_{Bn} of 30 min is smaller than that of 1 min. On the other hand, Ohmic characteristics are obtained by annealing for 30 min at 500 °C and 600 °C as shown in figure 4.3.8(b) and (c),

respectively. Therefore, it is realized that ϕ_{Bn} modulation and ohmic characteristics can be achieved even with the position of P incorporation far from the interface because P atoms are diffused by high temperature or long time annealing and arrive at interface as shown figure 4.3.8(d).

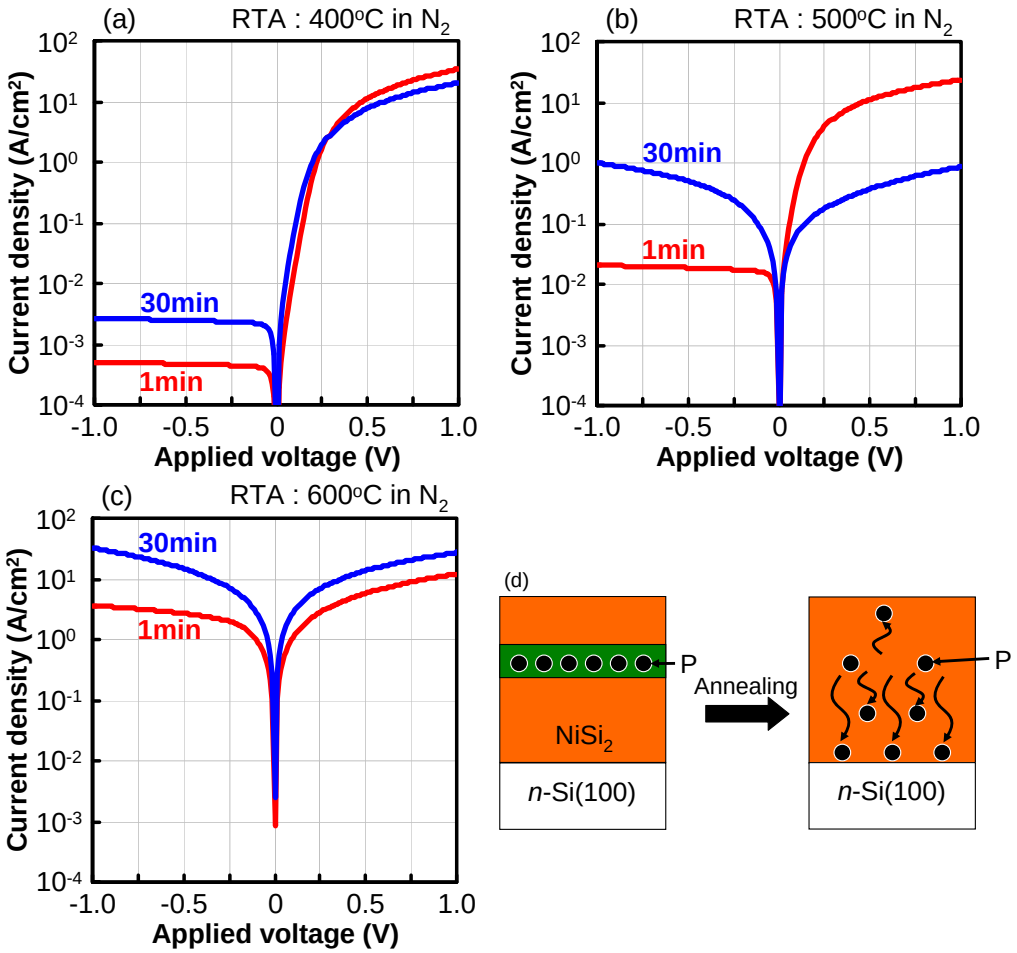


Figure 4.3.8 J-V characteristics of stacked silicide incorporated P far from the interface annealed at (a) 400 °C, (b) 500 °C and (c) 600 °C for 1 min and 30 min. (d) the image of P diffusion by annealing. Ohmic characteristics can be achieved by long time or high temperature annealing.

Finally, electrical characteristics of P incorporation depending on incorporated position and annealing temperature and time are summarized, and here the origin of ϕ_{Bn} modulation is discussed. One of the origins is the formation of a dipole which is generated from dopant at the silicide/Si interface as shown in figure 4.3.9 [4.3.4]. The other of the origins is the change of silicide work function by impurity doping into silicide [4.3.5]. As the result of table 4.3.1, it is considered that the origin of ϕ_{Bn} modulation is not so much the change of silicide work function as the presence of impurities at the interface in using stacked silicidation process.

Table 4.3.1 *Electrical characteristics of P incorporation depending on incorporated position and annealing temperature and time*

Sample	Annealing temperature (°C)	Annealing time (min)					
		0	1	・・・	10	20	30
P1	300						
	400						
	500						
	600						
P3	300						
	400						
	500						
	600						
P5	300						
	400						
	500						
	600						
P7	300						
	400						
	500						
	600						

Ohmic

Schottky

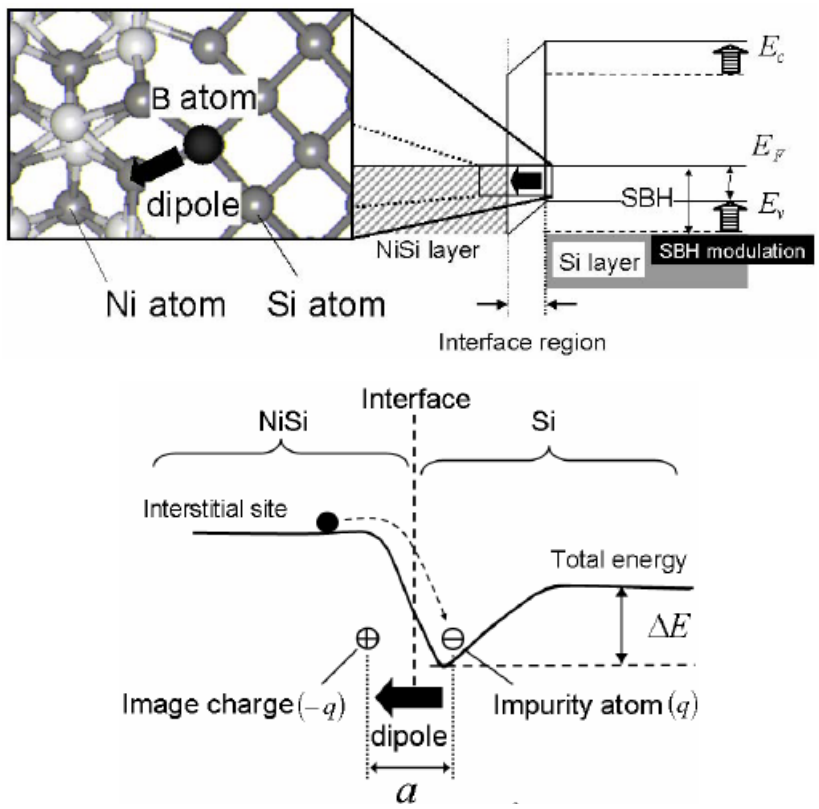


Figure 4.3.9 Schematic images of interface dipole model [6.4].

4.3.3.4 Impurity amount dependent diode characteristics

In the previous chapters, it is investigated that impurities which exist at the interface cause ϕ_{Bn} modulation. In this chapter, it is stated that impurity amount dependent diode characteristics. Figure 4.3.10 shows *J-V* characteristics of stacked silicide dependent the amount of B incorporation at the interface annealed at 500 ^{o}C for 1 min. Reverse currents decrease with increasing the amount of B incorporation at the interface compared to control sample. In addition, figure 4.3.11 shows ϕ_{Bn} of the diodes extracted from *J-V* characteristics depending on the amount of B incorporation at the interface. Large ϕ_{Bn} modulation can be achieved by increasing the amount of B incorporation at the interface. Therefore, effective ϕ_{Bn} modulation is controlled by controlling the amount of B atoms which exist at interface.

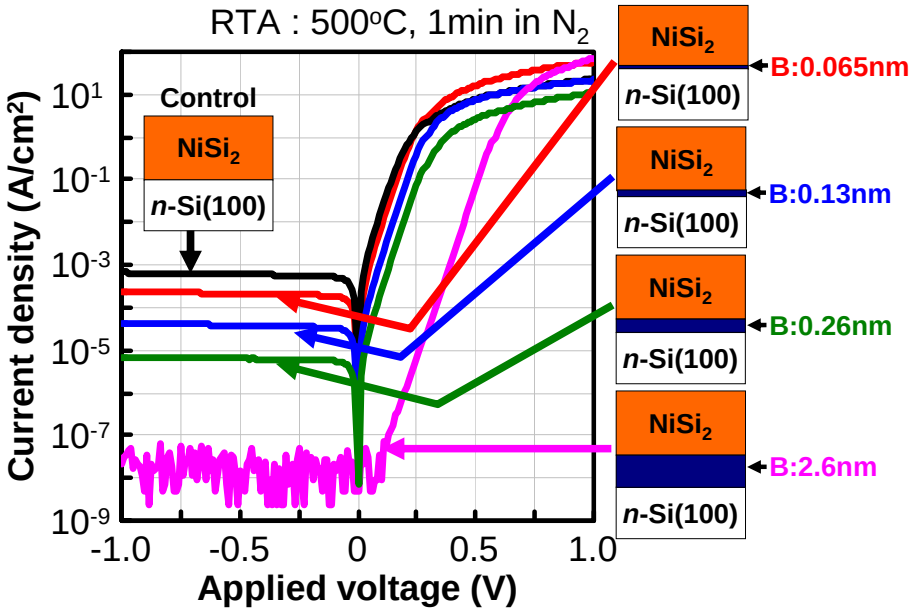


Figure 4.3.10 J-V characteristics of stacked silicide dependent the amount of B incorporation at the interface annealed at 500 °C. ϕ_{Bn} can be controlled by the amount of B incorporation.

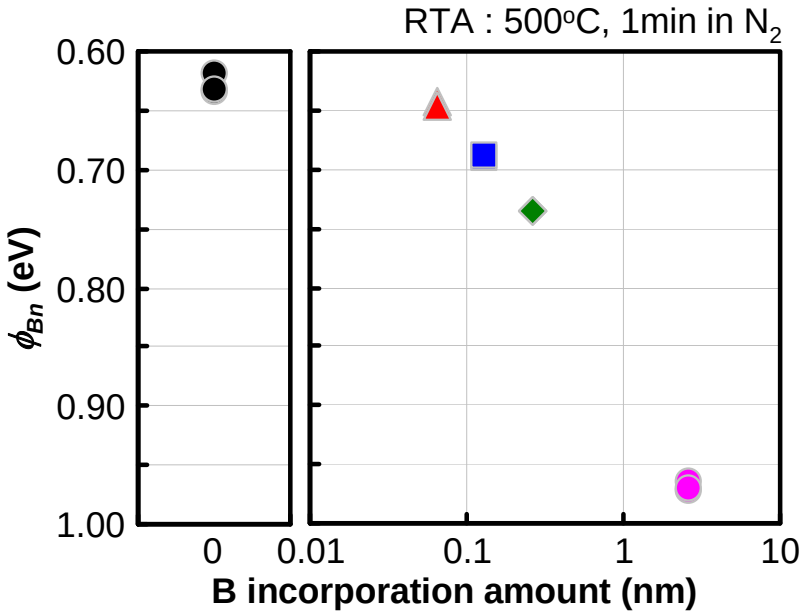


Figure 4.3.11 ϕ_{Bn} of the diodes extracted from J-V characteristics depending on the amount of B incorporation at the interface. Large ϕ_{Bn} modulation can be achieved by increasing the amount of B incorporation at the interface.

4.3.4 Conclusion

The effect of impurity incorporation on ϕ_{Bn} is investigated. At first, even with impurity incorporation, the interface reaction with stacked silicidation process is also maintained. Second, it is obtained that the significant amount of the impurities remained at the initial incorporated position due to suppression of interface reaction. Further, effective ϕ_{Bn} modulation is achieved by impurity incorporation at interface with stacked silicidation process. Moreover, impurity incorporation position and amount dependent ϕ_{Bn} modulation is examined. As a result, the main fact of ϕ_{Bn} modulation is that impurity exists at the interface. Additionally, it is found that ϕ_{Bn} modulation is controlled by controlling the amount of impurity which exists at interface.

4.3.5 References of this section

[4.3.1] W. Mizubayashi, S. Migita, Y. Morita, and H. Ota, “Exact Control of Junction Position and Schottky Barrier Height in Dopant-Segregated Epitaxial $NiSi_2$ for High Performance Metal Source/Drain MOSFETs”, Symp. on VLSI Tech. Dig., pp.88-89 (2011).

[4.3.2] A. Kinoshita, Y. Tsuchiya, A. Yagishita, K. Uchida and J. Koga, “Solution for High-Performance Schottky-Source/Drain MOSFETs: Schottky Barrier Height Engineering with Dopant Segregation Technique”, Symp. on VLSI Tech. Dig., pp.168-169 (2004).

[4.3.3] N. Mise, S. Migita, Y. Watanabe, H. Satake, T. Nabatame and A. Toriumi, “(111)-Faceted Metal Source and Drain for Aggressively Scaled Metal/High-k MISFETs”, IEEE Trans. Electron Devices, 55, pp.1244-12498 (2008).

[4.3.4] T. Yamauchi, Y. Nishi, Y. Tsuchiya, A. Kinoshita, J. Koga and K. Kato, “Novel

doping technology for a 1nm NiSi/Si junction with dipoles coforting Schottky (DSC) barrier", IEDM Tech. Dig., pp.963-966 (2007).

[4.3.5] T. Nakayama, K. Kakushima, O. Nakatsuka, Y. Machida, S. Sotome, T. Matsuki, K. Ohmori, H. Iwai, S. Zaima, T. Chikyow, K. Shiraishi and K. Yamada, "Theory of Workfunction Control of silicides by Doping for Future Si-Nano-Devices based on Fundamental Physics of Why Silicides Exist in Nature", IEDM Tech. Dig., pp.375-378 (2010).

4.4 Demonstration of Schottky barrier S/D FET with barrier height modulation

4.4.1 Introduction

As described above, it is considered that stacked silicidation process with impurity incorporation is the key to achieve the future scaled 3D SB-FETs. In this chapter, SB-FET using stacked silicidation process with ϕ_{Bn} modulation is demonstrated. Then, the effect of ϕ_{Bn} modulation on the device characteristics is investigated.

4.4.2 Fabrication process

SB-FET using the stacked silicide with B or P incorporation at S/D was fabricated on a SOI wafer as shown in figure 4.4.1. After SOI patterning, gate oxide was formed by thermal oxidation in 1000 ^{o}C. To form S/D, stacked silicidation process with impurity incorporation was performed. SiO_2 was deposited by plasma CVD (TEOS) owing to passivation. After gate metal deposition and etching, Al was deposited as contact by vacuum evaporation. Finally, annealing was performed at 500 ^{o}C in forming gas (F.G.) (N_2:H_2=97:3), so that the effect of terminating the dangling bonds with H^+ at the interface of oxide/Si substrate is obtained. Therefore, this process can achieve a process temperature below 500 ^{o}C, except for the gate oxidation.

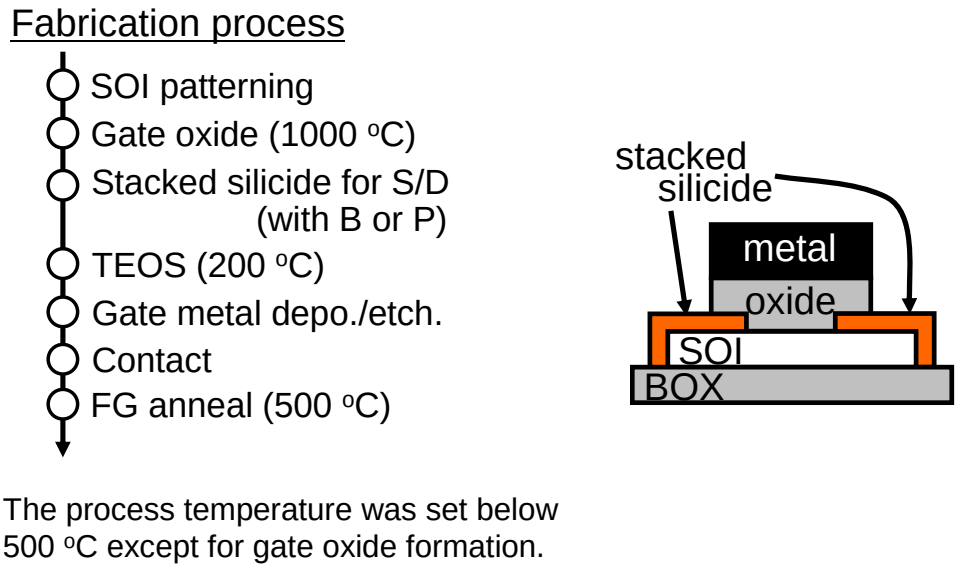


Figure 4.4.1 Fabrication process of Schottky S/D FET.

4.4.3 Electrical characteristics for SB-FET

I_d- V_G characteristics are shown in figure 4.4.2. B incorporated device showed ambipolar characteristics. On the other hand, P incorporated device can suppress ambipolar characteristics with lower ϕ_{Bn}, moreover, improvement in the on-current (V_G =V_d=3V) also supports the ϕ_{Bn} modulating. The schematic illustration of band diagram for operation is shown in figure 4.4.3 [4.4.1, 4.4.2, 4.4.3].

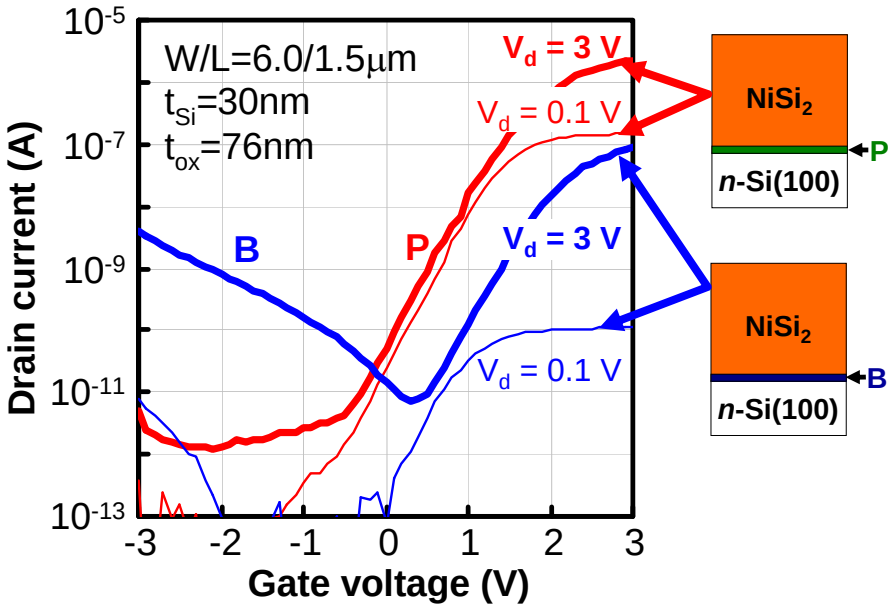


Figure 4.4.2 I_d - V_G characteristics of SB-FET with ϕ_{Bn} modulated stacked silicide. P incorporated device shows larger on-current with suppressed ambipolar characteristics.

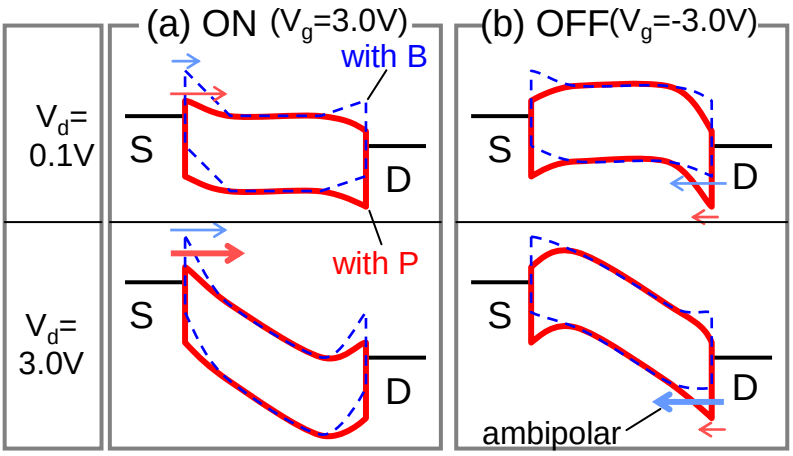


Figure 4.4.3 Band diagram of the SB-FET at (a) on and (b) off-states with different ϕ_{Bn}. Ambipolar characteristics are suppressed and larger on-current is obtained by modulating ϕ_{Bn} to smaller value.

4.4.4 Conclusion

SB-FETs using stacked silicidation process with B or P incorporation at S/D were fabricated below 500 ^{o}C except for the gate oxidation. The effect of ϕ_{Bn} modulation on the device characteristics is confirmed. It is considered that ambipolar characteristics are suppressed and on-current is improved because ϕ_{Bn} is modulated to small value. It is necessary for high performance to modulate ϕ_{Bn} to smaller value.

4.4.5 References of this section

[4.4.1] M. Zhang, J. Knoch, Q. T. Zhao, U. Breuer and S. Mantl, “Impact of dopant segregation on fully depleted Schottky-barrier SOI-MOSFETs”, Solid-State Electron., 50, pp.594-600 (2006).

[4.4.2] C. Urban, C. Sandow, Q. T. Zhao, J. Knoch, S. Lenk, S. Mantl, “Systematic study of Schottky barrier MOSFETs with dopant segregation on thin-body SOI”, Solid-State Electron., 54, pp.185-190 (2010).

[4.4.3] L. E. Calvet, H. Luebben and M. A. Reed, C. Wang, J. P. Snyder, J. R. Tucker, “Suppression of leakage current in Schottky barrier matal-oxide-semiconductor field-effect transistors”, J. Appl. Phys., 91, pp.757-759 (2002).

Chapter 5
Band Discontinuities at Source-Channel Interface and their influence on Tunneling FET Performance

5.1 Introduction

Upon further device size scaling, transistors with steep subthreshold slope have been focused as low standby power devices for next generation [5.1]. Among variety of steep subthreshold devices including feedback FET [5.2], impact-ionization FET [5.3] and nano-electro-mechanical FET [5.4], tunnel FETs (TFET) have been considered to have high potentials to achieve a large I_{ON}-I_{OFF} ratio over a small gate voltage swing. As shown in chapter 3, Schottky barrier tunneling FETs have advantages to the conventional MOSFETs such as steeper subthreshold swing and larger Ion/Ioff for short Lg regions, keeping their drivability high. This devices also receive several benefits of the Schottky MOSFETs such as low parasitic S/D resistance, low-temperature process capability, and elimination of parasitic bipolar action. [5.5] However the Schottky barrier tunneling FETs suffer from relatively large subthreshold swing compared to the band-to-band tunneling MOSFETs, presumably due to the presence of the high-energy electron distribution tail of the Fermi-Dirac distribution in source metal region, whose influence is discussed as the subthreshold swing of highly degenerated p+ source region in ref [5.6]. Therefore the elimination of the high-energy tail is effective in order to obtain small subthreshold swings, by using band-to-band tunneling with an appropriate impurity concentration source

semiconductor region. In addition to that, recently, hetero-junction TFETs (H-TFETs) with the presence of a band discontinuity at source/channel interface have been proposed in order to boost the drivability of the devices. [5.7] Since H-TFET operation is based on band-to-band tunneling from valence band of the source region ($E_{V,source}$) to conduction band of the channel ($E_{C,channel}$), the tunneling probability can be determined by a potential barrier with triangular shape as shown in Figure 5.1(b)[5.7], in which a tunneling barrier and tunneling distance are determined by ($E_{C,channel} - E_{V,source}$), gate bias and channel concentration(N_d). In this study, we investigate the influence of valence band discontinuity (ΔE_V) at source and channel interface on device performance of TFET by numerical simulations.

5.2 Simulated model

SILVACO TCAT tool ATLAS with non-local tunneling model was used for the simulation. The device structure used for this simulation was depicted in Figure 5.2. An *n*-type SOI layer (E_g=1.12eV, N_d=1×10^{17} cm^{-3}) with a thickness of 10 nm and a channel length of 100 nm were used. Gate oxide with an equivalent oxide thickness of 0.3 nm was adopted. ΔE_V between the p^+-source and channel was varied from 0 (homojunction) to 0.6 eV. The bandgap of semiconductor in source region was kept to be 1.12eV, meaning that ΔEc at source/drain interface is equal to ΔE_V. The carrier distribution of source material property sited Si carrier.

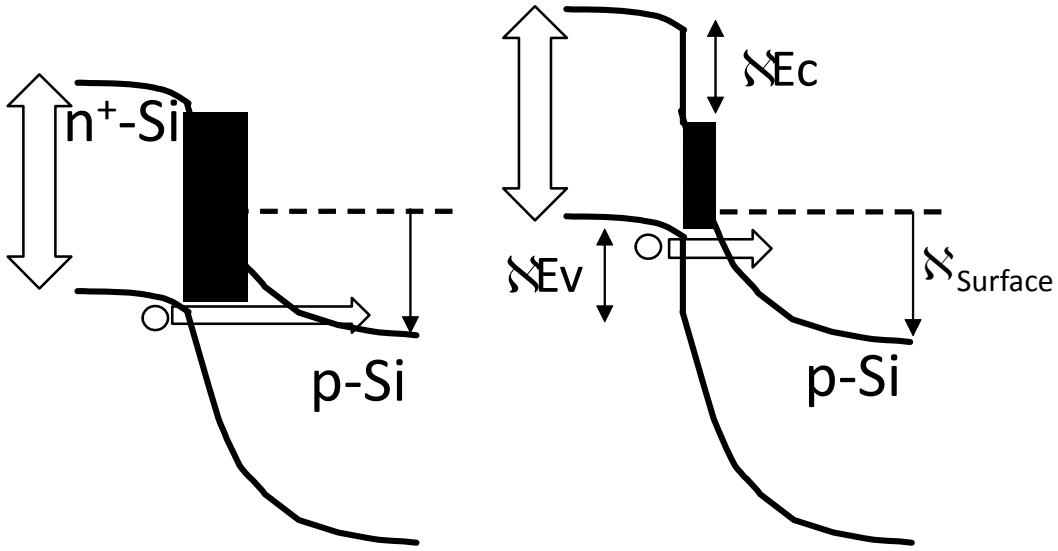


Figure 5.1 Band diagrams of source-channel junction (a) with band discontinuities and (b) without band discontinuity.

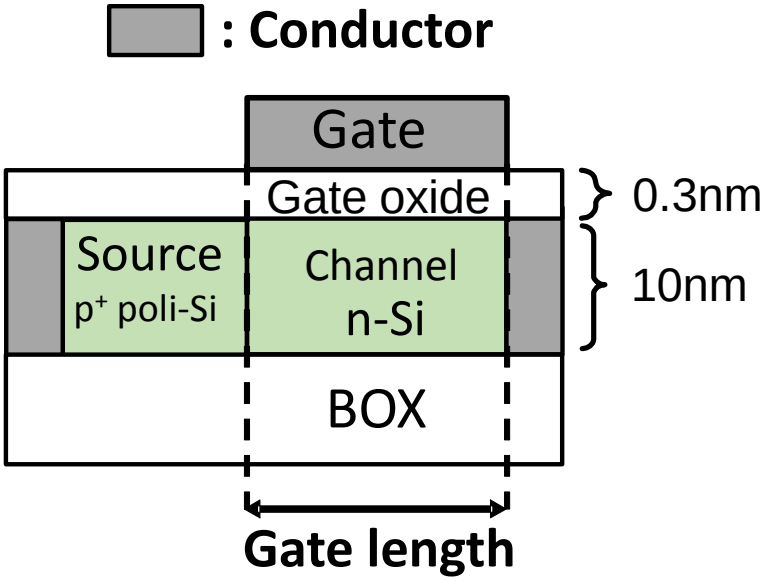


Figure 5.2 Device structure in simulation in this chapter

5.3 Influence of valence band discontinuity

Figures 5.3, 5.4 show I_d- V_G and subthreshold swing (SS) characteristics of TFET with different values of ΔE_V. One can observe higher I_{ON} as well as smaller SS with larger ΔE_V. The drivability increased by 2 order of magnitude and the SS values are well under the conventional MOSFET minimum value of 60mV/dec for large V_G range. The smallest SS of 14 mV/dec. was obtained with ΔE_V of 0.6 eV. Transconductance (g_m) also increased with larger ΔE_V as shown in Figure 5.5.

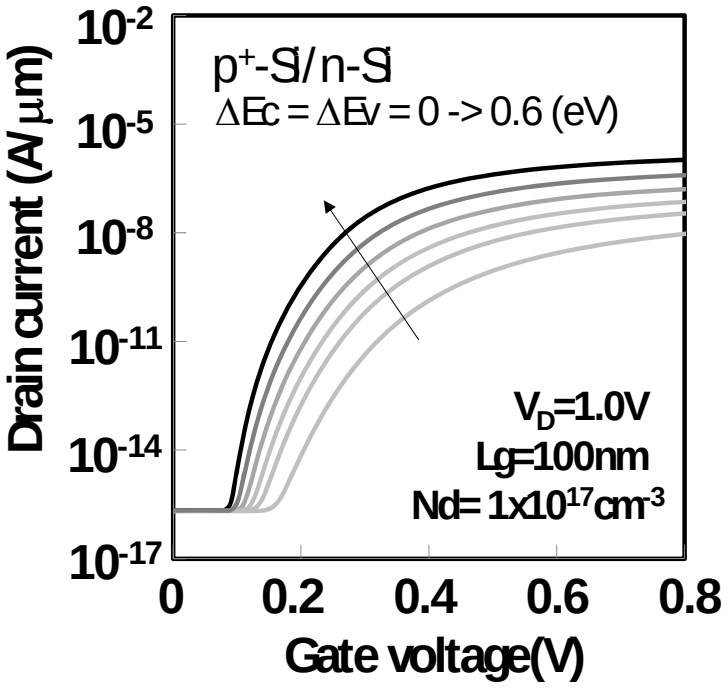


Figure 5.3 I_d - V_G characteristics of for each band offset in TFET

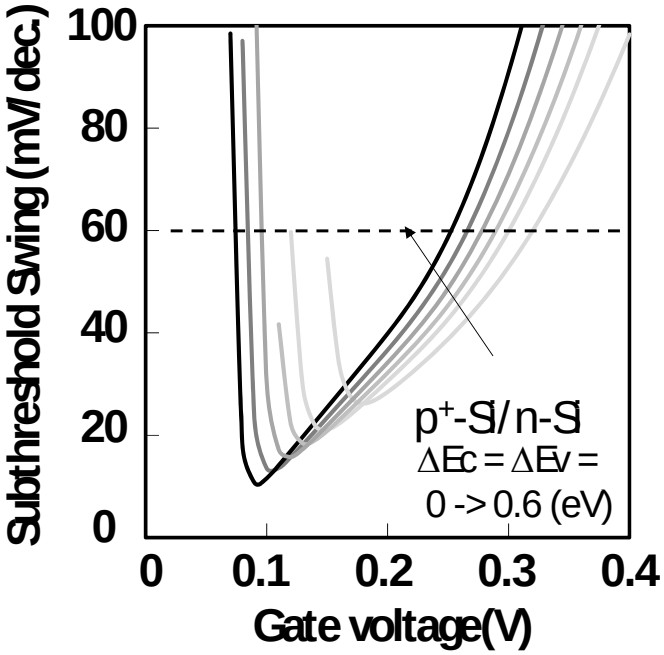


Figure 5.4 Subthreshold swing characteristics of for each band discontinuity at source/channel interface of TFET

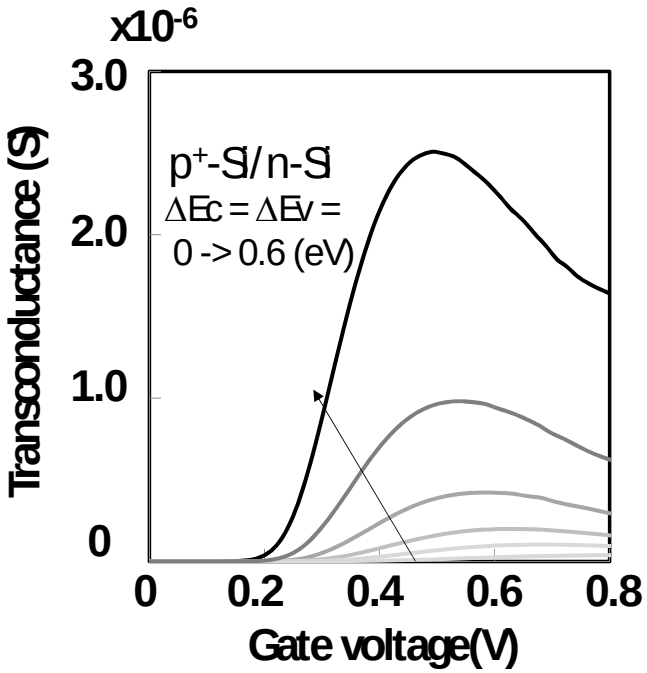


Figure 5.5 Transconductance characteristics of for each band each band discontinuity at source/channel interface of TFET

Threshold voltage, V_{th}, which is defined as V_G at I_d=10^{-8}A/μm, decreased gradually with larger ΔE_V as shown in Figure 5.6(a), due to reduced tunneling distance.. Large increase in I_{ON}, defined as V_G =V_{th}+0.7V as shown in Figure 5.6(b), is due to lower energy barrier. On the other hand, I_{OFF}, defined as V_G =V_{th}-0.3V, showed no dependency on ΔE_V as shown in Figure 5.6(c), which lead to the large I_{ON}/I_{OFF} ratio.

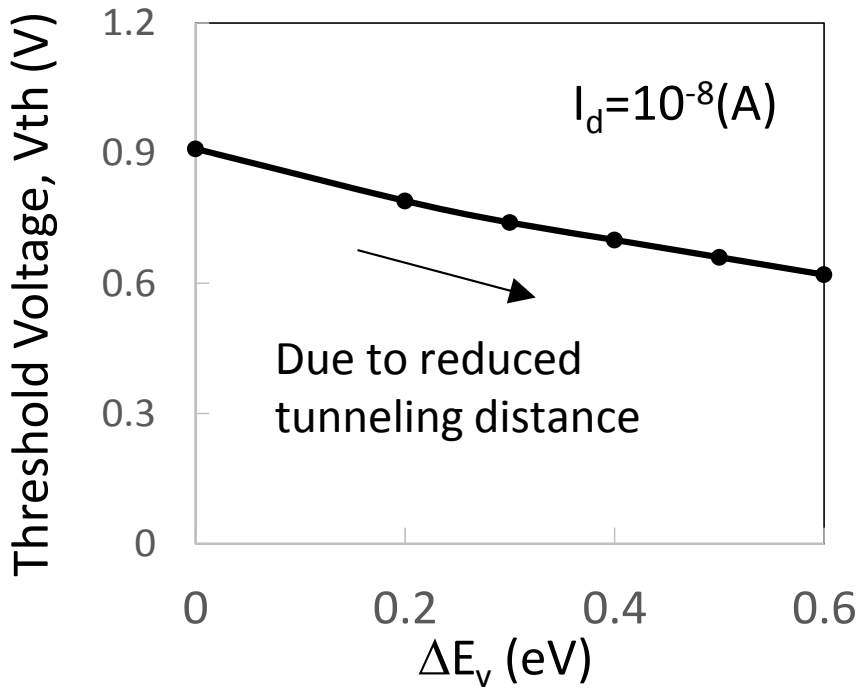


***Figure 5.6** (a)*: Threshold voltage dependence on ΔE_V. V_{th}, is defined as V_G at I_d=10^{-8}A/μm.

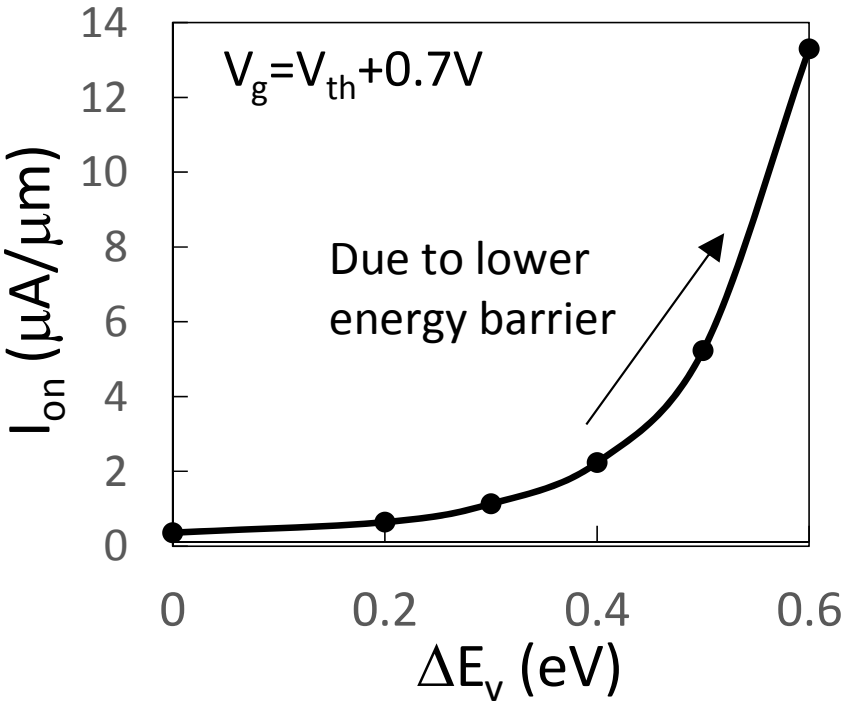


***Figure 5.6** (b)*: Drain Current dependence on ΔE_V. *Ion* at V_G =*Vth*+0.7V is plotted in this figure.

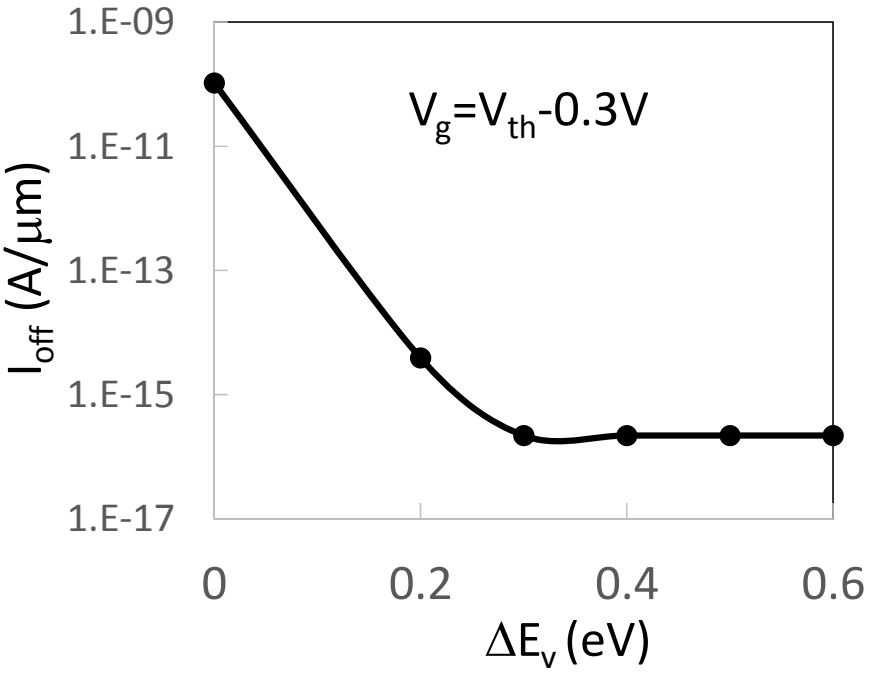


***Figure 5.6**(c)*: Leakage current *Ioff* dependence on ΔE_V.

Potential semiconductors for source region in terms of the formation of band discontinuity with channel region are summarized in Fig. 5.7 [5.8], Mg_2Si (E_g=0.75 eV) [5.9] source can be a good candidate for *n*- TFETs with Si channel. In the same way, β-$FeSi_2$ (E_g=0.85eV) [5.10] can be a prospective candidate for *p*-TFETs.

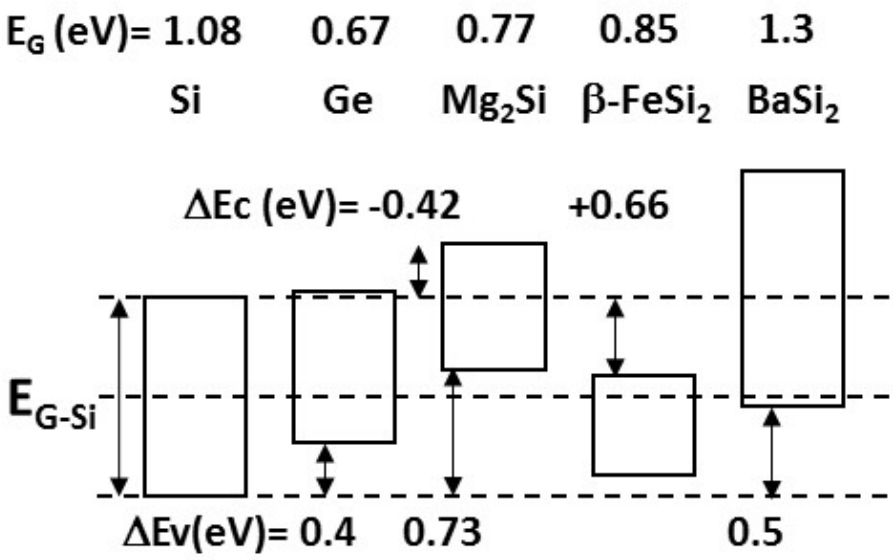


Figure.5.7 Band alignment of various semiconductor materials. Well-known semiconducting silicide is also shown in this figure.

5.4 Conclusions

We have investigated the influence of valence band discontinuity at source and channel interface on device performance of TFET by numerical simulations. A steep slope with high I_{ON} can be both achieved with larger discontinuity, owing to reduced tunneling distance and lower energy barrier for tunneling. As prospective candidates for the source semiconducting materials, Mg_2Si and β-$FeSi_2$ are selected for N-channel and

P-channel tunneling FETs, respectively.

5.5 References of this chapter

[5.1] A. Tura and Jason C. S. Woo, “Performance Comparison of Silicon Steep Subthreshold FETs”, IEEE Trans. Electron Dev., Vol. 57, pp. 1362 (2010).

[5.2] A. Padilla, C. W. Yeung, C. Shin, C. Hu, and T. Liu “Feedback FET: A Novel Transistor Exhibiting Steep Switching Behavior at Low Bias Voltages” IEDM Tech. Dig., pp. 1 (2008).

[5.3] K. Gopalakrishnan, R. Woo, C. Jungemann, P. B. Griffin, and J. D. Plummer “Impact Ionization MOS (I-MOS)—Part II: Experimental Results” IEEE Trans. Electron Devices, Vol. 52, pp. 69 (2005).

[5.4] Hei Kam, D. T. Lee, R. T. Howe, and T. J. King “A New Nano-Electro-Mechanical Field Effect Transistor (NEMFET) Design for Low-Power Electronics” IEDM Tech. Dig., pp. 463 (2005).

[5.5] M. Sugino, L.A. Akers and M.E. Rebeschini “Latchup-free Schottky-barrier CMOS” IEEE Trans. Electron Devices, 30, (1983) 110.

[5.6] L. Michielis, L. Lattanzio, K.E. Moselund, H. Riel, A.M. Ionescu, “Tunneling and Occupancy Probabilities: How Do They Affect Tunnel-FET Behavior?” IEEE Electron Device Letters, VOL. 34, NO. 6, JUNE 2013

[5.7] D. K. Mohata, R. Bijesh, S. Mujumdar, C. Eaton, R. Engel-Herbert, T. Mayer, V. Narayanan, J. M. Fastenau, D. Loubychev, A. K. Liu and S. Datta, “Demonstration of MOSFET-Like On-Current Performance in Arsenide/Antimonide Tunnel FETs with Staggered Hetero-junctions for 300mV Logic Applications” IEDM Tech. Dig., p. 781 (2011).

[5.8] Semiconductor - Basic Data 2nd Edition , O.Madelung, Springer

[5.9] M. I. Baleva, E. A. Goranova, M. M. Marinova, A. A. Atanassov "Heterojunctions between Silicon and the Semiconducting Metal Silicides b-FeSi2 and MgSi2" ECS Transactions - ULSI vs. TFT Conference, Volume 8, July 2007.

[5.10] T. Suemasu, K. Morita, M. Kobayashi, M. Saida and M. Sasaki “Band Diagrams of BaSi2/Si Structure by Kelvin Probe and Current–Voltage Characteristics” JJAP 45 (2006) L519

Chapter 6

A novel Hetero-junction Tunnel-FET using Semiconducting Silicide-Silicon contact and its scalability

6.1. Introduction

The scaling of metal-oxide-semiconductor field-effect transistors (MOSFETs) has been pursued for more than 3 decades and the device size reached down to less than 30-nm gate length (L_g) region. The scaling law of MOSFETs requires the proportional downsizing of each component of the device such as gate length, gate oxide and source/drain junction depth [1]. The reduction of the supply voltage (V_{dd}) is also required in order to keep the electric field inside the devices constant [6.1]. The threshold voltage (V_{th}) is expected to be lowered accordingly so as to keep on-state drain current (I_{on}) high. However, the lowering of the V_{th} leads to the drastic increase in off-state leakage current between source and drain (I_{off}), because of the intrinsic lower limit of the subthreshold swing (SS) of MOSFET at room temperature (60mV/dec) [6.2]. The increase in SS due to the short channel effect for extremely scaled MOSFET even makes the situation worse [6.3]. Recently, in order to keep SS low and obtain the value less than 60mV/dec at RT, the tunneling field effect transistor (TFET) has been proposed [6.4,6.5]. For this device, gate voltage controls the channel potential in order to modulate the tunneling current through the source/channel junction, instead of modulating the drift-diffusion

current in the channel as in the conventional MOSFETs. However, as the TFETs use the tunneling phenomenon through the semiconductor junctions with a certain bandgap, they suffer from the small I_{on}, in general [6.4-6]. Improvement of the drivability of TFETs has been pursued by using hetero-junctions [6.7,6.8], in which the tunneling probability is enhanced by the reduction of tunneling width with the conduction or valence band discontinuities. In most cases, the hetero-junction has been realized by III-V semiconductors, with much experiences of hetero-junction engineering such as high-electron-mobility transistor (HEMT) and power MOS transistors. Although much work has been done so far in terms of the implementation of III-V transistors in Si ULSI technologies, further developments are necessary in issues such as the formation of the high-k gate stack with low interface state density and low gate leakage current [6.9] and the metal contact formation to the semiconductors with low contact resistance [6.10]. On the other hand, hetero-junctions among semiconductors of group IV has also been proposed for their application to the TFETs using Ge-Si and SiGe-Si structures [6.11,6.12].

Metal silicides have been used as self-aligned silicide (SALICIDE) on source and drain in order to reduce the parasitic resistance of the electrodes in Si ULSI technology [13]. Metal silicides such as $TiSi_2$, $CoSi_2$ and NiSi are used as conductors with low resistivity for that purpose [6.13,6.14]. On the other hand, semiconducting silicide such as $FeSi_2$, $BaSi_2$ and Mg_2Si have been developed for the photovoltaic cells and thermoelectric materials [6.15,16]. By using these semiconducting silicides as hetero-junction materials with Si, TFETs with low SS and high drivability could be realized. Furthermore, application of SALICIDE technology to these semiconducting silicide formations could makes self-aligned formation of the hetero-junction much

easier than the molecular beam epitaxy (MBE) of other semiconductors.

In this study, novel silicide hetero-junction tunneling FET using the semiconducting silicide is proposed and the device simulations have been performed to investigate the influence of the structural parameters such as channel doping concentration and the gate-source overlaps on the electrical characteristics of TFETs. The dependence of the characteristics on gate-length has also been investigated in order to elucidate the scalability of this device.

6.2. Device Concept and simulation

Figure 6.1(a) shows the band alignment of Si, Ge and semiconducting metal Silicides. Among various silicides, the figure shows that Mg_2Si has a relatively small bandgap of around 0.7-0.8eV and that there are large conduction band and valence band discontinuities with Si as the result of its large band energy shift towards the vacuum level [6.15, 6.17, 6.18]. Previous work revealed that this material can be doped as n-type as well as p-type [18, 19] and this fact also indicates the good potential of this material as a candidate for the Si hetero-junction tunneling FETs. Figure 6.1(b) shows the band diagram of the p-type Mg_2Si/n-type Si hetero-junction along with that of Si homo-junction. The tunneling probability through the pn junction P_T can be calculated as follows [6.2]:

$$P_T = exp\left(-\frac{4\sqrt{2m^*}E_g^{3/2}}{3q\hbar\varepsilon}\right) \quad (6.1),$$

where m^*, E_g, q, h, ε are tunneling mass of electron, bandgap of semiconductor, elementary charge, Plank constant and electric field in the junction,

respectively. In the case of hetero-junction, E_g of semiconducting silicide is much smaller than that of Si and moreover, the effective tunneling barrier is reduced by the presence of large conduction and valence band discontinuities once the electrons enter the silicon region as shown Figure 1(b). This leads to the enhancement of the probability and the resulting drivability of the tunneling FET.

All simulation was done in Silvaco TCAD tool ATLAS. This simulation tool includes drift-diffusion, thermionic emission and tunneling components. The tunneling part uses a non-local band-to-band tunneling model with a two-band approximation for the evanescent wave vector, and it applies a careful Wentzel–Kramer–Brillouin method [6.20]. Gate leak current was neglected in these simulations. Bandgap narrowing, CVT (Lombardi) mobility [6.21] model was enabled.

A schematic illustration of the device is shown in Figure 2(a). An n-type silicon MOS structure in an SOI with a thickness of 10 nm was used in the present simulation. The gate oxide thickness and the buried-oxide thickness (BOX) were set to 0.3 and 40 nm, respectively, and the work function of the metal gate was set to 4.3 eV. The gate electrode overlapped was varied in the simulation. Doping concentration of channel (Si) N_d was tuned mainly from 1×10^{15} to 1×10^{18} cm^{-3}. Doping concentration of source N_a (Mg_2Si, Ge, Si) was set to be $1x10^{20}cm^{-3}$. The tunnel mass (m^*) was set to be $0.25m_0$ [22], where m_0 is the mass of a free electron.

The semiconducting Mg_2Si source region was modeled according to Figure 6.1 (a), where bandgap, conduction band offset, and valence band offset are 0.77eV, 0.42eV, and 0.73eV, respectively. The dielectric constant is of this material is set to be 20 [6.17,6.23]. For the drain electrode, a conductor with an Ohmic-contact to Si channel is assumed in order to eliminate the parasitic resistance in this region.

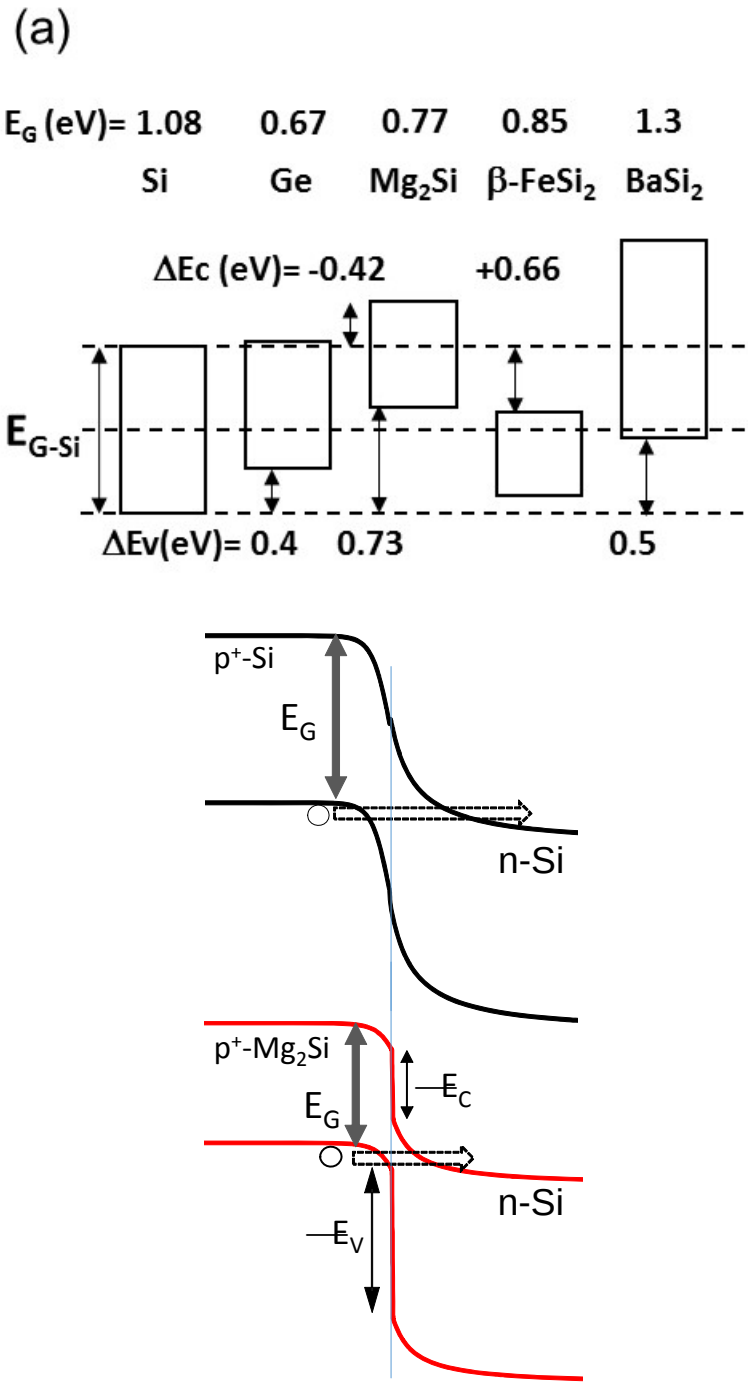


Figure 6.1 (a) Band alignment of Si, Ge and semiconducting silicides. (b) Band diagram of P^+-Si/n-Si homo-junction and P^+-Mg_2Si/n-Si hetero-junction

Considering the required supply voltage in less100 nm FETs, the drain voltage is varied. Gate length scaling of FET characteristics was carried out in the range of 20 to 100 nm. All simulations were carried out at room temperature. The electrical characteristics for TFET with Si homo-junction and p^+- Ge/n- Si hetero-junction were also calculated for comparison.

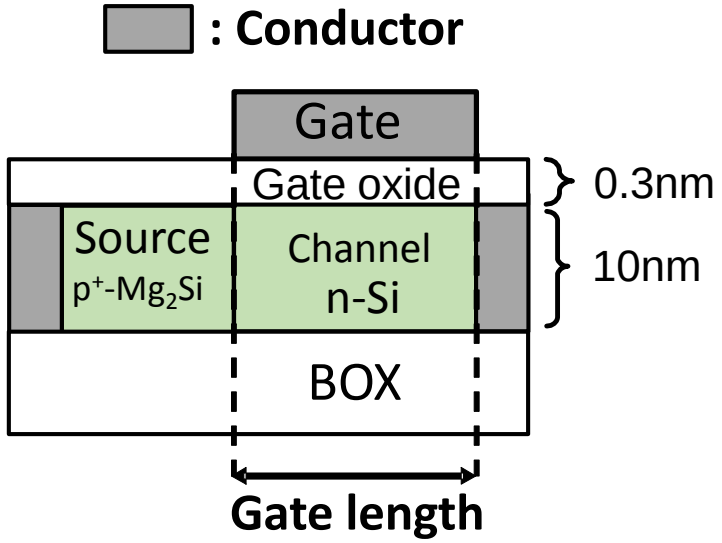


Figure 6.2. Schematic device illustration of a tunnel FET with Mg_2Si source structure. Structural parameters in the device simulation is also shown.

6.3. Results and discussion

Figure 6.3(a) shows $I_d - V_G$ characteristics of the TFET with p-Mg_2Si source hetero-junction. The gate length L_g and the channel doping concentration N_d are 100nm and $1x10^{17}cm^{-3}$, respectively. The drain voltage was set to be 1.0V in this case. Also shown are the characteristics of Si homo-junction tunneling FET and that of p-Ge/Si source hetero-junction tunneling FET. The drain current of Mg_2Si hetero-junction TEFT was larger than that of Si case by more than two orders of magnitude. Even when it is

compared to the Ge-Si case, I_d increase by about one order of magnitude was obtained. This figure also shows steeper subthreshold characteristic for the Mg_2Si hetero-junction TFET. Figure 6.3(b) shows the subthreshold swing SS dependence on the gate voltage. The smallest SS less than 10mV/dec is observed for Mg_2Si source hetero-junction TFET at the region where the drain current starts to rise from the off state. As the drive current increases, the SS gradually increases, however it keeps small value below 60mV/dec for the gate voltage range of about 0.2V. Although the SS dependence of Si homo-junction and the Ge-Si hetero-junction shows similar dependence on the gate voltage, those minima are larger than that of Mg_2Si hetero-junction TFET.

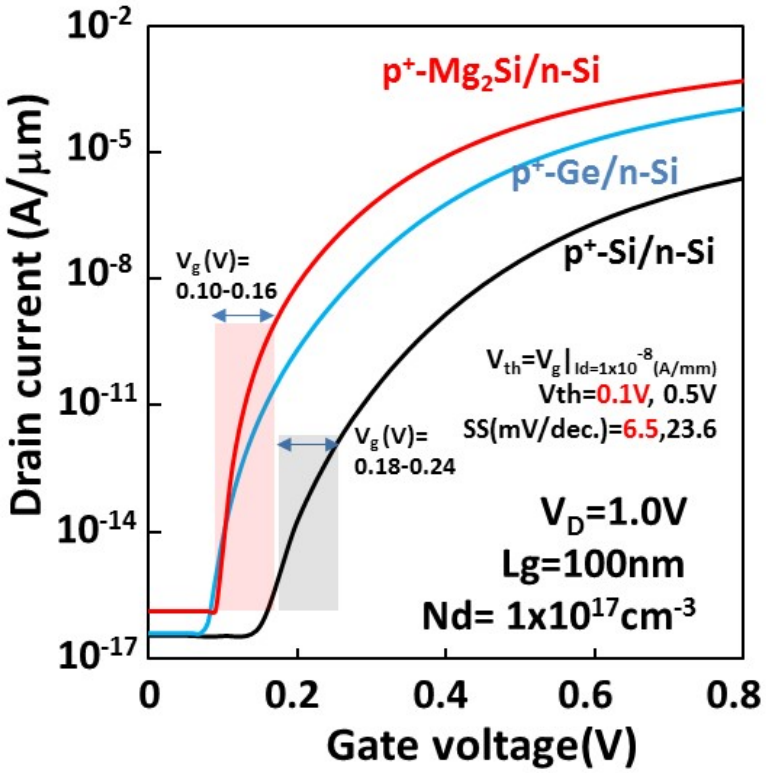


***Figure* 6.3** (a). $I_d - V_G$ characteristics of the TFET with p-Mg_2Si source hetero-junction. The gate length L_g and the channel doping concentration N_d are 100nm and $1x10^{17}cm^{-3}$, respectively. The drain voltage was set to be 1.0V. Also shown are the characteristics of Si homo-junction tunneling FET and that of p-Ge/Si source hetero-junction tunneling

FET.

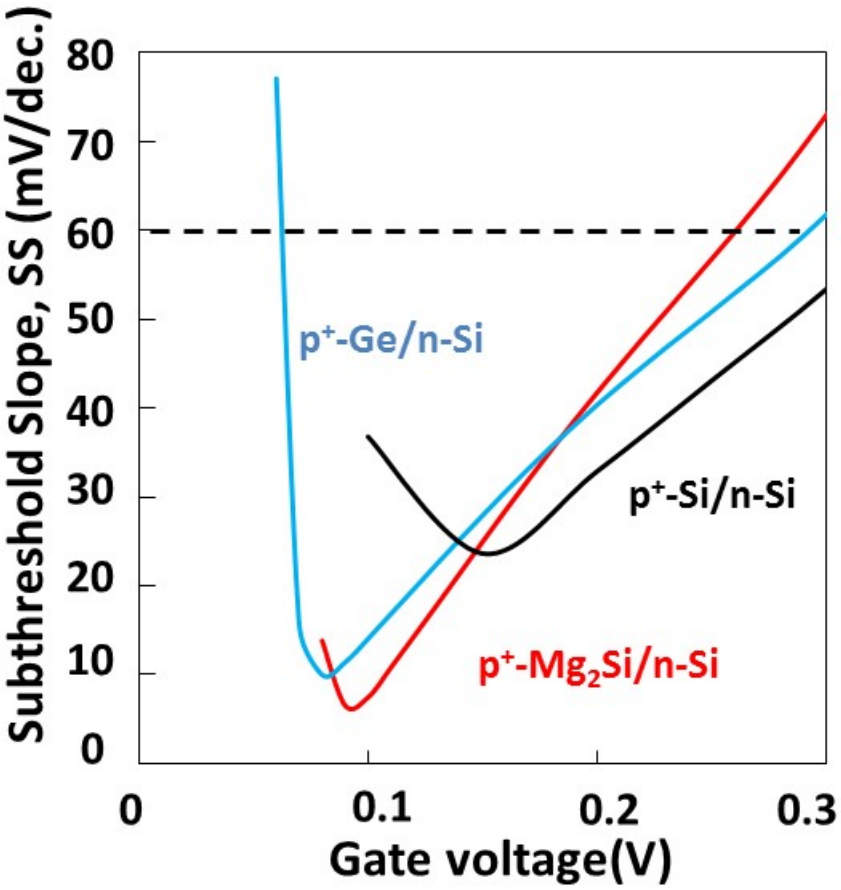


Figure 6.3(b) The subthreshold swing SS dependence on the gate voltage for the three cases.

In order to elucidate the reason for the smaller SS for the Mg_2Si junction, the current density in the channel was closely checked as shown in Figure 6.4(a). This figure shows the current density at the channel depth of 1nm from the gate dielectric and substrate interface. In Figure 6.4(a) the horizontal axis shows the position along the hetero-junction with metallurgical junction position as the origin. The current in the left shows the hole current in the p-type source, while that in the right shows the electron current in the Si channel in this figure. Solid lines and dotted lines indicate the result for

the Mg_2Si hetero-junction TFET and Si homo-junction TFET, respectively. The gate voltage range is in Figure 6.4(a) is 0.1V-0.16V-for the Mg_2Si hetero-junction case, while that is 0.18-0.24V for the Si homo-junction case. These gate voltage range was shown in Figure 6.3(a).

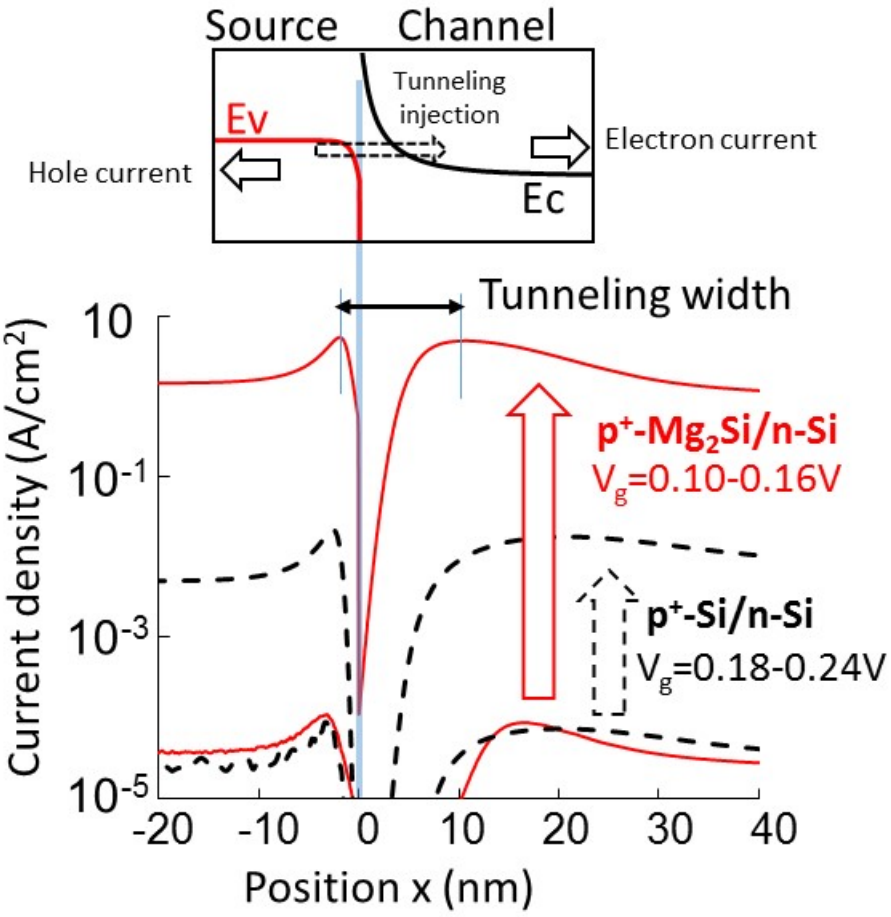


Figure 6.4(a) Current density at the channel depth of 1nm from the gate dielectric and substrate interface. The horizontal axis shows the position along the hetero-junction with metallurgical junction position as the origin. The current in the left shows the hole current in the p-type source, while that in the right shows the electron current in the Si channel. Solid lines and dotted lines indicate the result for the Mg_2Si hetero-junction TFET and the conventional Si TFET, respectively. The tunneling width was defined as the length along the channel between points where the hole and electron current show maxima. Gate voltage range shown in (a) is indicated.

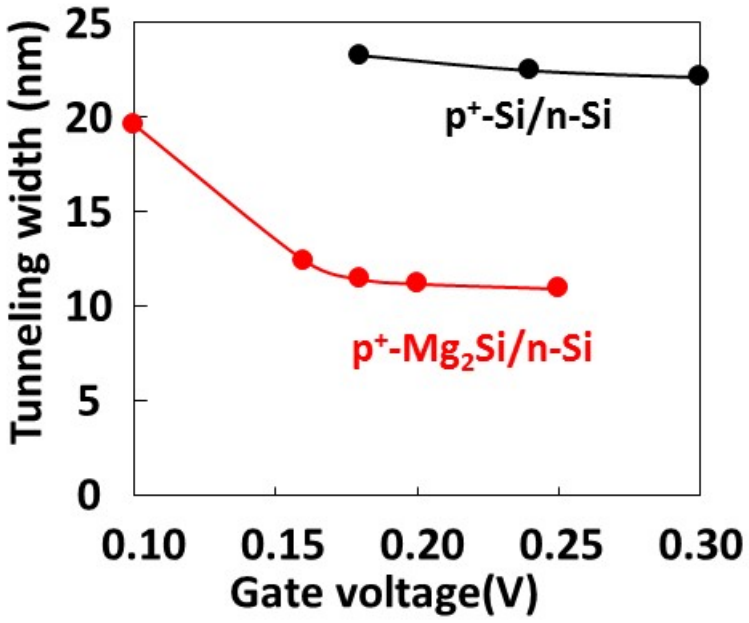


Figure 6.4(b) Tunneling width as a function of gate voltage.

The tunneling width was defined as the length along the channel between points where the hole and electron current show maxima as in Figure 6.4(a). Figure 6.4(b) shows the tunneling width as a function of the gate voltage. It indicates that the widths are shorter for Mg_2Si hetero-junction TFET than those of the conventional Si TFET throughout the gate voltage simulated and this is considered to be the reason for the larger drain current of Mg_2Si hetero-junction TFET. In addition to that, the figure shows the tunneling width drastically changes especially for the gate voltage range 0.1V-0.16V and this can be regarded as the reason for the smaller SS for Mg_2Si hetero-junction TFET than that of Si homo-junction TEFT.

It should be noted that the off leakage current is larger for the larger channel doping concentration. It is opposite trend to the conventional MOSFET, where smaller channel concentration leads to a larger off leakage. This is because of the difference in the channel doping type: For n-channel FET in which positive gate voltage is applied to let

electrons flow in the channel, p-type dopant is introduced in the conventional MOSFET, while n-type dopant is introduced in TFET case. Therefore, there is no short channel effect originated in charge share issue [24]. The larger off leakage current for higher N_d, especially for 20nm case, is regarded as the increase in the influence of the drain potential (drain-induced tunneling width reduction), which will be discussed in detail at Figure 8 below. Figure 5(b) shows the tunneling width as a function of gate voltage, taking the N_d as a parameter. This figure shows Lighter doping provides larger change in tunneling width with the same V_G modulation, leading to smaller SS. On the other hand, Figure 6.5(a) shows almost the same level of on-state drain current at larger V_G region with N_d variation. Therefore, lighter doping is preferable in terms of the TFET characteristics.

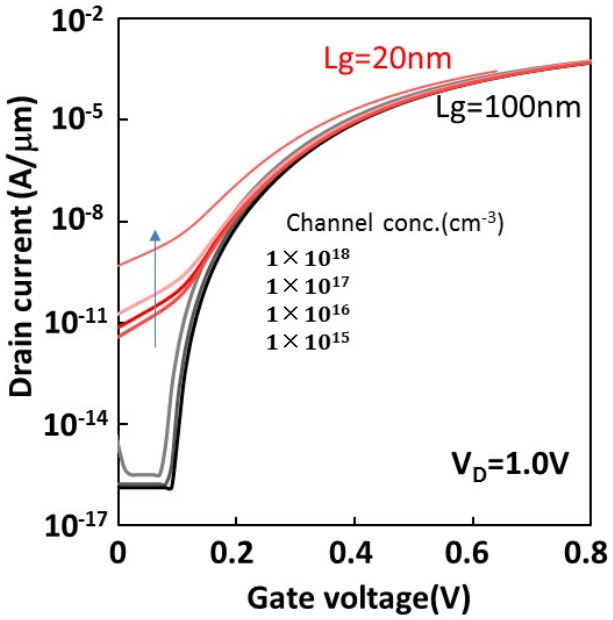


Figure 6.5(a) $I_d - V_G$ characteristics of the TFET with Mg_2Si hetero-junction with the gate length L_g of 100nm (black lines) and 20nm (red lines). The drain voltage was set to be 1.0V. The channel doping concentration N_d was varied as a structural parameter from

$1x10^{15}$ to 1 $x10^{18}cm^{-3}$.

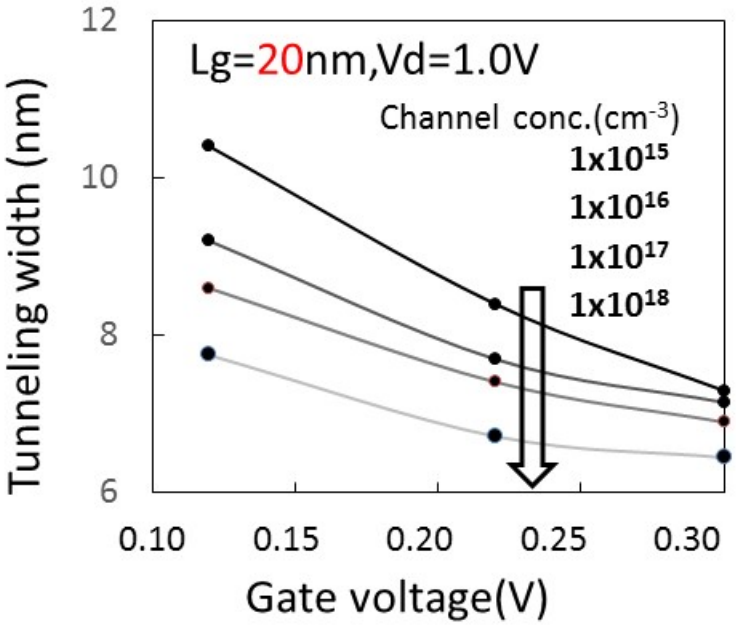


Figure 6.5(b) Tunneling width as a function of gate voltage for TFET Mg_2Si hetero-junction TFET with the gate length L_g of 20nm.

Figure 6.6(a) shows the $I_d - V_G$ characteristics of the TFET with Mg_2Si hetero-junction with the gate length L_g and N_d of 100nm and 1 $x10^{17}cm^{-3}$, respectively. The drain voltage was set to be 1.0V. The gate electrode edge position relative to the Mg_2Si/Si interface, which is called gate-source overlap, was varied as a parameter. The gate-source overlap is positive when gate electrode edge is located above Mg_2Si, while it is negative when it is located above Si substrate as shown in Figure 6.6(b). The overlap was changed from -20 to +20nm in this study. The drive current and minimum SS do not change much when gate overlap is positive, while the drain current decreases and SS increases much in case of negative gate overlap.

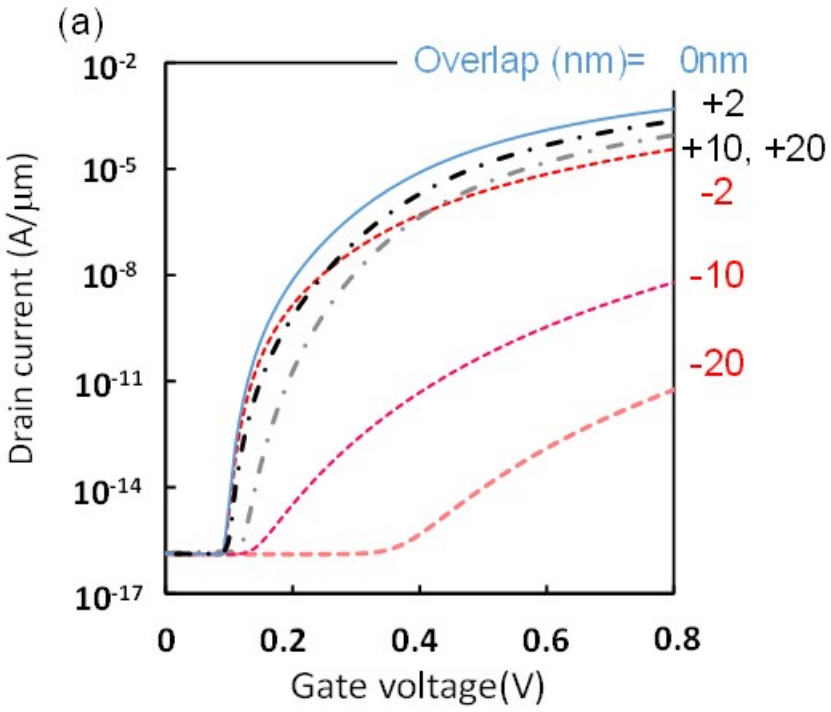


Figure 6.6(a) $I_d - V_G$ characteristics of the TFET with Mg_2Si hetero-junction with the gate length L_g and N_d of 100nm and 1 x$10^{17}$$cm^{-3}$, respectively. The drain voltage was set to be 1.0V.

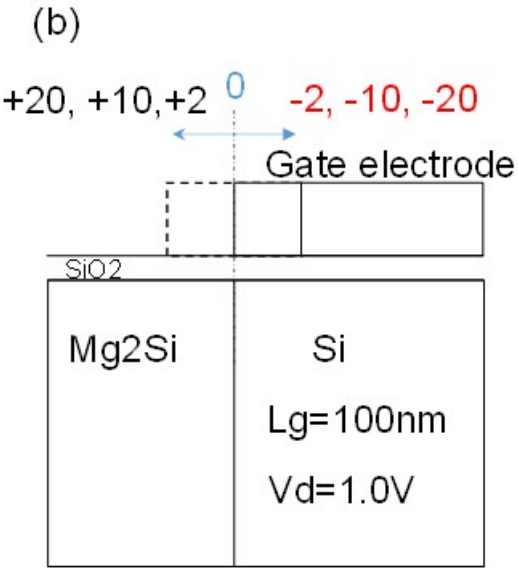


Figure 6.6(b) Definition of the gate overlap: it is positive when gate electrode edge is located above Mg_2Si, while it is negative when it is located above Si substrate.

The band diagram of Mg_2Si hetero-junction just under the gate dielectric/substrate interface is depicted in Figure 6.7(a) at V_G =1.0V. In case of positive overlap, gate voltage slightly modifies the Mg2Si potential resulting in the slight decrease in the electric field in the hetero-junction. On the other hand, in case of negative overlap, gate voltage does not influence the Si potential at the hetero-junction interface much. Therefore, the electric field is drastically reduced, leading to the smaller drain current and large increase in the subthreshold slope. The result is summarized in Figure 6.7(b), where the amount of overlap is taken as the horizontal axis. It should be noted that the optimum overlap giving the most current drive as well as smallest SS is not 0nm. Therefore exact alignment of the gate edge to Mg_2Si hetero-junction is desirable for obtaining the largest electric field at the hetero-junction.

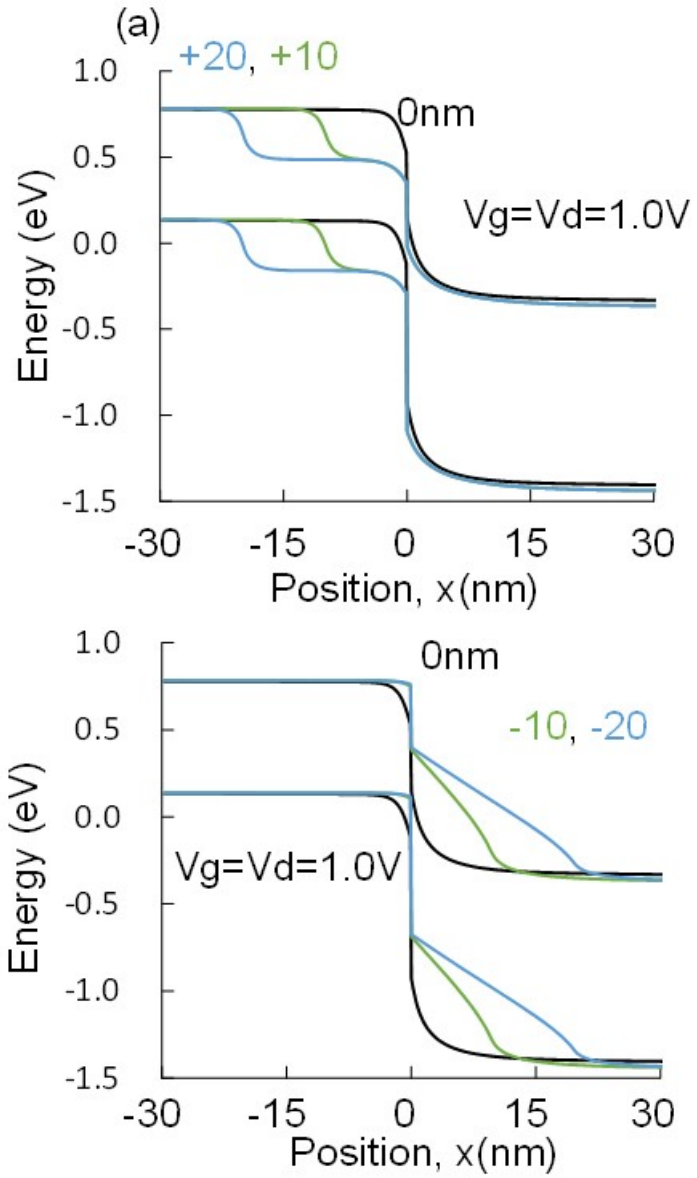


Figure 6.7(a) Band diagram of Mg_2Si hetero-junction just under the gate dielectric/substrate interface with positive gate overlap and negative overlap. The amount of the overlap is varied from -20 to 20nm. The gate voltage was 1V for both cases.

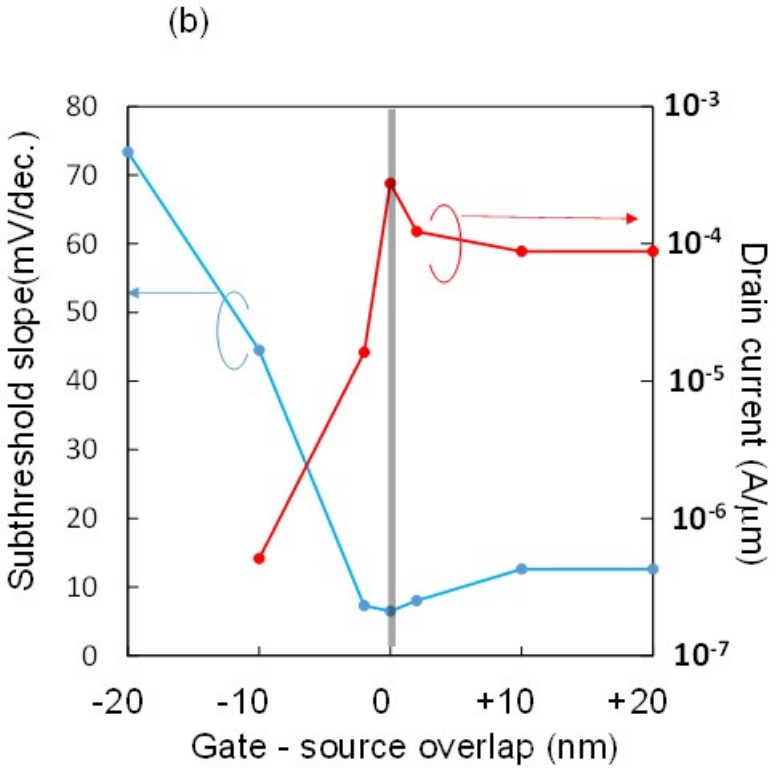


Figure 6.7(b) Minimum subthreshold slope and drain current ($V_G = V_{th}$+0.5V) as a function of the gate overlap.

Figure 6.8(a) shows the $I_d - V_G$ characteristics of the TFET with Mg_2Si hetero-junction with Lg of 100nm and N_d of 1 x10^{17}cm^{-3}. The drain voltage is taken as a parameter ranging from 0.1V to 1.0V. Also shown in Figure 6.8(b) is the $I_d - V_G$ characteristics of the TFET with Mg_2Si hetero-junction with Lg of 20nm and N_d of 1 x10^{17}cm^{-3}. The drain voltage is also varied from 0.1V to 1.0V. Although there is not much change in the characteristics in 100nm case, the reduction in the off leakage current by the lowering of the drain voltage is clearly observed in 20nm case. This is considered to be due to the reduction of the drain-induced tunneling width modulation observed especially in short Lg devices. The tunneling width was increased (15.0nm to 18.8nm) by the lowering of drain voltage from 1.0 to 0.3V.

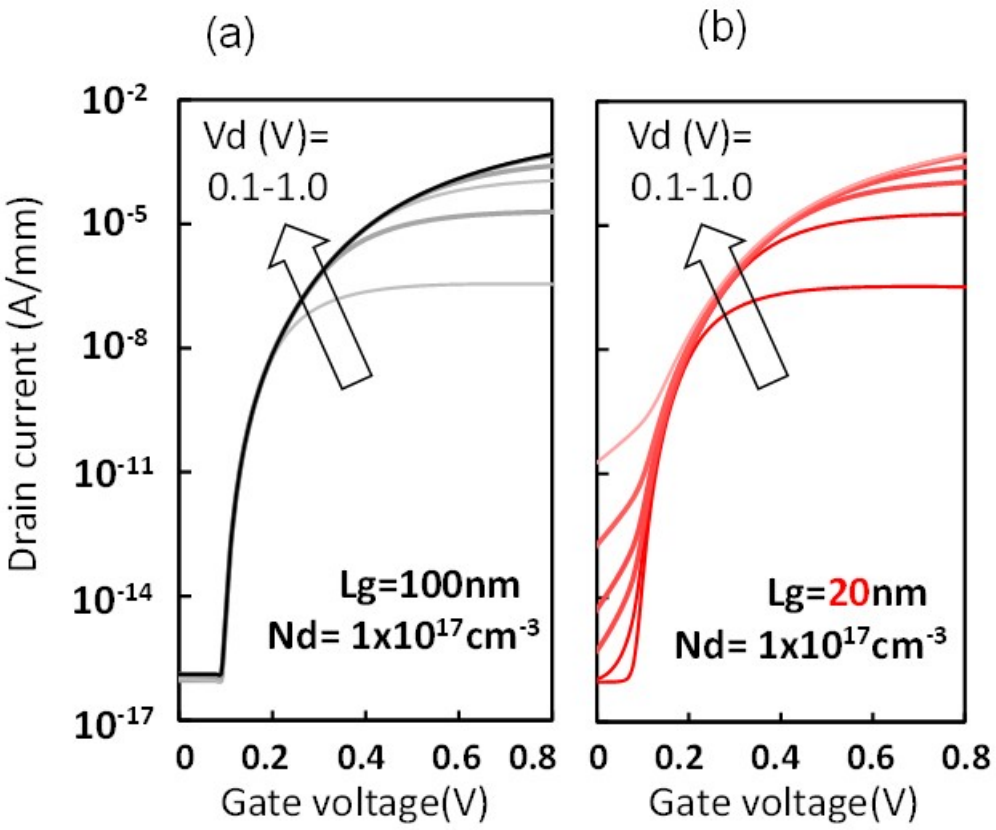


Figure 6.8 (a), (b) $I_d - V_G$ characteristics of the TFET with Mg_2Si hetero-junction with the N_d and 1 x10^{17}cm^{-3}, the gate length L_g of (a) 100nm and (b) is 20nm. The drain voltage is varied from 0.1 to 1.0V for both cases.

Figure 6.9(a) shows the minimum SS as a function of the drain voltage. It should be noted that the on-state drain current is not changed much even when the drain voltage is reduced to as low as 0.3V. The result is summarized in Figure 6.9(b). Therefore, it could be concluded that this device is scalable by the drain voltage reduction in accordance with its gate length minimization.

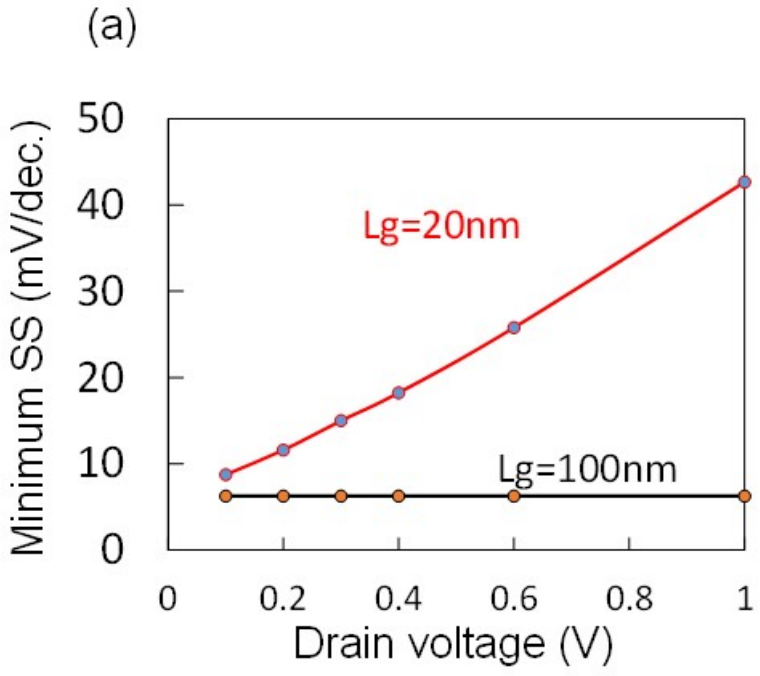


Figure 6.9 (a) Minimum subthreshold slop SS as a function of drain voltage. Gate length is taken as a parameter

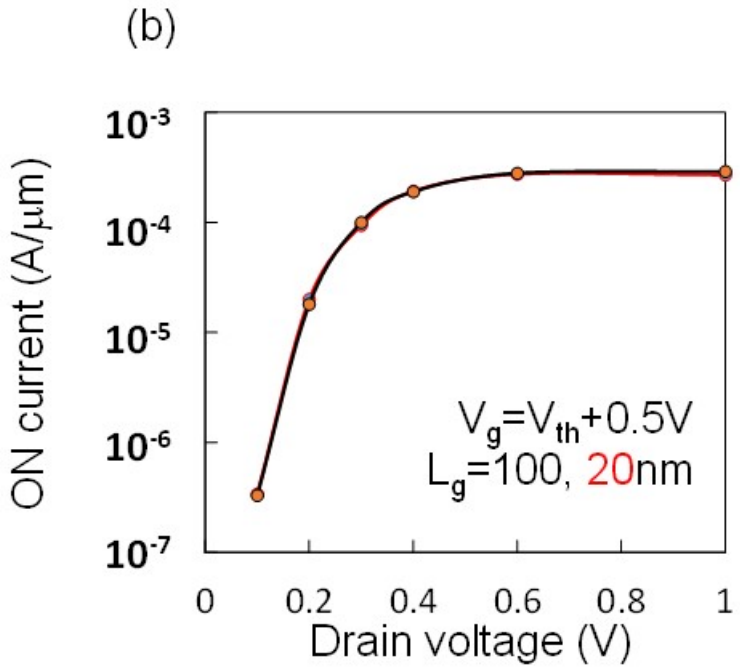


Figure 6.9(b) On-state drain current as a function of drain voltage at V_G =*Vth*+0.5V. The results for devices with gate length 20 to 100nm are almost the same.

Finally, the performance of Mg_2Si hetero-junction TFET (L_g=20nm) was compared with the conventional SOI-MOSFET as well as those in recent literatures on other highly-scaled TFETs [6.8, 6.25-27] as shown in Fig.6.10.

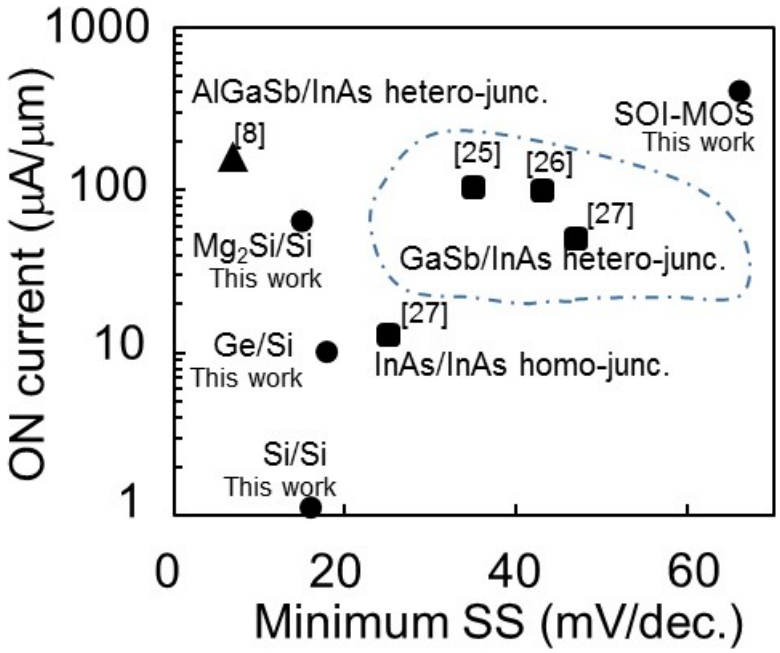


Fig.6.10. Comparison of the performance of Mg_2Si hetero-junction TFET (L_g=20nm) with the conventional SOI-MOSFET as well as those in recent literatures on other highly-scaled TFETs [8, 25-27]. The performance of the conventional SOI-MOSFET with similar device structure to Fig.2 was simulated. In this simulation, source/drain electrodes were n^+-Si and the channel doping concentration was $1x10^{17}cm^{-3}$. Performance of TFETs (L_g=20nm) with Si homo-junction and Ge/Si hetero-junction were also simulated with the channel doping concentration of $1x10^{17}cm^{-3}$. Performance of all devices at $V_G = V_{th}+0.3V$ and V_d=0.3V are plotted for the comparison.

The performance of the conventional SOI-MOSFET with similar device structure to

Fig.6.2 was simulated. In this simulation, source/drain electrodes were n^+-Si and the channel doping concentration was $1x10^{17}cm^{-3}$. Performance of TFETs (L_g=20nm) with Si homo-junction and Ge/Si hetero-junction were also simulated with the channel doping concentration of $1x10^{17}cm^{-3}$. Performance of all devices at $V_G = V_{th}+0.3V$ and V_d=0.3V are plotted for the comparison. This figure indicates that Mg_2Si hetero-junction TFET can provide the largest drivability with the smallest minimum SS as Si-based TFETs. Although the drain current was reduced from that of SOI-MOSFET, the reduction was limited to less than 1 orders of magnitude and the reduction of the SS was quite large. This performance is considered to be comparable to those of highly-scaled III-V hetero-junction TFETs.

6.4. Conclusions

In this work, new type of tunneling field-effect transistor using semiconducting silicide Mg_2Si source /Si channel hetero-junction was proposed and the device simulation has been performed. With a large band discontinuity in conduction and valence band edges at the source/channel hetero-junction, the drain current was enhanced by about 2orders of magnitude from the Si homo-junction reference device. The subthreshold swing (SS), which is another key parameter of TFET, can also be reduced from that of Si homo-junction case. The structural parameter influence on the electrical characteristics revealed that a low substrate impurity concentration lead to lower SS as a result of larger tunneling distance modification by the gate voltage. It was also shown that the alignment of the gate edge to the hetero-junction lead to the smallest SS and the largest drain current by the realization of the largest electric field at the junction. Scaling of the gate length leads to the increase in SS because the drain

potential induce larger leakage current by the drain induced tunneling width reduction. But with the drain voltage decrease in accordance with the gate length scaling, the high drivability and low SS of Si based TFET device could be maintained.

6.5 References of this chapter

[6.1] Dennard RH, Gaenesslen FH, Yu HN, Rideout VL, Bassous E, Le Blanc AR, "Design of Ion-Implanted MOSFETs with very small physical dimensions", IEEE J Solid State Circuits 1974;SC-9;256.

[6.2] S.M. Sze, Physics of Semiconductor Devices, 2nd Edition, John Wiley & Sons, New York,1981.

[6.3] Taur Y, Ning T, "Fundamentals of modern VLSI devices", 2nd edition, Cambridge University Press, Cambridge, 2009.

[6.4] L.Megala, B.Devanathan, R.Venkatraman, A.Vishnukumar "Tunneling field-effect transistors (TFETs) with subthreshold swing less than 60mV/dec", IEEE Electron Dev.Lett.;2007;28;743-745.

[6.5] M. T. Björk1, J. Knoch, H. Schmid, H. Riel and W. Riess "Silicon nanowire tunneling field-effect transistors", Appl.Phys.Lett.;2008;92;193504.

[6.6] K. Jeon, W.-Y. Loh, P. Patel, C.Y. Kang. J. Oh, A. Bowonder, C. Park, C.S. Park, C. Smith, P. Majhi, H.-H. Tseng, R. Jammy, T.-J.K. Liu, and Chenming Hu, "Si tunnel transistors with a novel silicided source and 46mV/dec swing", Proc. VLSI Symp. Technol.;2010;121-122.

[6.7] D. Mohata, S. Mookerjea, A. Agrawal, Y. Li, T. Mayer, V. Narayanan, A. Liu, D. Loubychev, J. Fastenau, and Su. Datta, "Experimental staggered-source and N+

pocket-doped channel III-V tunneling field-effect transistors and their scalabilities", App.Phys.Exp.;2011;4;024105.

[6.8] Y. Lu, G. Zhou, R. Li, Q. Liu, Q. Zhang, T. Vasen, S. D. Chae, T. Kosel, M. Wistey, H. Xing, A. Seabaugh, and P. Fay "Performance of AlGaSb/InAs TFETs with gate electric field and tunneling direction aligned", IEEE Electron Dev. Lett.;2012;33;655-657.

[6.9] Lee KY, Lee, Y.J. ; Chang, P. ; Huang, M.L. ; Chang, Y.C. ; Hong, M. ; Kwo, J. "Achieving 1nm capacitve effective thickness in atomic layer deposited HfO2 on $In_{0.53}Ga_{0.47}As$", Appl.Phys.Lett.;2008;92;252908.

[6.10] Kim SH, M. Yokoyama, N. Taoka, R. Nakane, T. Yasuda, O.Ichikawa, N. Fukuhara, M. Hata, M. Takenaka and S. Takagi, "Sub 60 nm deeply-scaled channel length extremely-thin body $In_xGa_{1-x}As$-On-Insulator MOSFETs on Si with Ni-InGaAs metal S/D and MOS interface buffer engineering", Proc. VLSI Symp. Technol.;2012;177-178.

[6.11] T. Krishnamohan, D. Kim, S. Raghunathan, K. Saraswat, "Douple-gate strained-Ge heterostructure tunneling FET (TFET) with record high drive current and <60mV/dec subthreshold slope", IEDM Tech. Dig.:2008: 947-950.

[6.12] Villalon A, Le Royer, C. ; Casse, M. ; Cooper, D. ; Previtali, B. ; Tabone, C. ; Hartmann, J. ; Perreau, P. ; Rivallin, P. ; Damlencourt, J. ; Allain, F. ; Andrieu, F. ; Weber, O. ; Faynot, O. ; Poiroux, T. "Strained tunnel FETs with record Ion: first demonstration of ET-SOI TFETs with SiGe channel and RSD", Proc. VLSI Symp. Technol.;2012;49-50.

[6.13] Maex K, "Silicides for integrated circuits: TiSi2 and CoSi2", Mater. Sci. Eng.; 1993;R11;53

[6.14] Morimoto T.; Ohguro, T.; Momose, S.; Iinuma, T.; Kunishima, I.; Suguro, K.; Katakabe, I.; Nakajima, H.; Tsuchiaki, M.; Ono, M.; Katsumata, Y. and Iwai, H. "Self-aligned nickel mono-silicide technology for high-speed deep submicrometer logic CMOS" ULSI, IEEE Trans. Electron Dev.;1995;42;915-922.

[6.15] M. I. Balevaa, E. A. Goranovab, M. M. Marinovaa, and A. A. Atanasova "Heterojunctions between silicon and the semiconducting metal silicides β-$FeSi_2$ and $MgSi_2$", ECS Transactions;2007;8;151-156.

[6.16] S. Muthiah, J. Pulikkotil, A. K. Srivastava, A. Kumar, B. D. Pathak, A. Dhar, and R. C. Budhani, "Conducting grain boundaries enhancing thermoelectric performance in doped Mg_2Si", Appl.Phys.Lett.;2013;103;053901.

[6.17] T. Kato, Y. Sago and H. Fujiwara, "Optoelectronic properties of Mg2Si semiconducting layers with high absorption coefficients", J.Appl.Phys.;2011;110;063723

[6.18] RG. Morris, RD. Redin, GC. Danielson "Semiconducting properties of Mg2Si single crystals", Phys.Rev.;1958;109;1909-1915.

[6.19] Niwa Y, "Thermoelectric property of Na-doped Mg_2Si", J.Japan Inst. Metals; 2008;72;693-697 (*in Japanese*)

[6.20] ATLAS user's manual by Silvaco Inc.

[6.21] C. Lombardi, S. Manzini, A. Saporito and M. Vanzi, "A Physically Based Mobility Model for Numerical Simulation of Nonplanar Devices", IEEE Trans. Comp. Aided Design: 1992: 7: 1154-1171.

[6.22] G. A. M. Hurkx, et al.," A New Recombination Model for Device Simulation Including Tunneling" IEEE Trans. Electron Devices, 1992: 39: 331.

[6.23]J.L. Corkill, M.L. Cohen, "Structural, bonding, and electronic properties of

IIA-IV antifluorite compounds" Phys. Rev. B: 1993: 48: 17138.

[6.24] Taylor GW, "The effect of two dimensional charge sharing on the above-threshold characteristics of short-channel IGFET", 1979;22;701-719.

[6.25]:U. Avci et al., "Energy efficiency comparison of nanowire heterojunction TFET and Si MOSFET at Lg=13nm, including P-TFET and variation considerations", IEDM Tech. Dig.:2013: 33.4.

[6.26]: S. Brocard, et al., "Design options for hetero-junction tunnel FETs with high on current and steep sub-VT slope", IEDM Tech. Dig.:2013: 5.4.

[6.27]:U. Avci et al, "Heterojunction TFET scaling and resonant-TFET for steep subthreshold slope at sub-9nm gate-length", IEDM Tech. Dig.:2013: 4.3.

Chapter 7
Conclusions

7.1 Summary of this thesis

MOSFETs have been developed in accordance with the scaling law in order to enhance the device speed and reduce their power consumption during the operation. Scaling law requires the reduction of the supply voltage of MOSFETs, however recently the subthreshold leakage prevents us from pursuing the trend. Therefore steep subthreshold FETs have been intensively investigated. Among a few candidates for the steep subthreshold FETs, tunneling FET is a most promising one due to its simple structure and its capability of the drain voltage reduction. Therefore, it is very important to conduct a research on tunneling FETs especially in terms of their on-state and subthreshold characteristics. On the other hand, with the fact that Si base technology is still prevailing in ULSI field even with an intensive work all over the world for the development of III-V semiconductors. Therefore, Si-based tunneling FET could be one promising solution for the drastic reduction of the ULSI chips.

Silicides have been used in SALICIDE process in ULSI manufacturing so far in order to reduce the parasitic resistance of MOSFETs. But Metal silicide can also be applied to form the Schottky tunneling interface, while semiconducting silicide can be applied to form the hetero-tunneling junction with Si channel.

Considering all of these backgrounds, I conducted the research on a study on process and device structure Tunnel FETs using Silicide-Silicon Schottky or Heterojunction.

In chapter 3, the device simulation has been performed to investigate the structural parameter influence on the electrical characteristics of Schottky barrier tunneling FETs (SBTFETs). Schottky barrier height and channel doping concentration as well as gate length are mainly taken as the structural parameters. For relatively long-channel MOSFETs (50 nm), a low Schottky barrier height as well as a high substrate impurity concentration lead to the increase in the tunneling probability through the barrier, resulting in the smaller SS. On the other hand, for short channel length MOSFETS (10 nm), the short channel effect (SCE) has much influence on the characteristics of SBTFETs. Since a larger SBH is effective to suppress the SCE, an optimum Schottky barrier exists for the short-channel SBTFETs, depending on the gate length as well as other device parameters.

For the realization of the silicide/Si structure suitable for SBTFETs, defect free silicidation at the interface with quite wide range of ϕ_{Bn} controllability is desired. In chapter 4, novel Ni silicide formation process using annealing of Ni/Si thin film stack is proposed. This process realizes stable NiSi2 composition and morphology at wide temperature range with an atomically flat interface without Ni atoms encroachment into Si channel. Introduction of Phosphorous and Boron at the silicide/Si interface made possible to modify the Schottky barrier height with quite wide range in Si bandgap. Finally, Schottky transistors are fabricated with this process in order to confirm the effectiveness of this process.

The elimination of electrons which belong to a high energy tail in Fermi-Dirac distribution in the source electrode seems to be effective to reduce subthreshold swing further, the band-to-band tunneling from semiconducting source and the influence of valence band and conduction band discontinuities at source-channel interface are

investigated using numerical simulations in chapter 5. A steeper subthreshold swing with higher ON current can be both achieved with larger discontinuity, owing to reduced tunneling distance and lower energy barrier for the quantum mechanical tunneling of electrons.

In chapter 6, new type of tunneling field-effect transistor using semiconducting silicide Mg2Si source /Si channel hetero-junction was proposed and the device simulation has been performed. With a large band discontinuity in conduction and valence band edges at the source/channel hetero-junction, the drain current was enhanced by about 2orders of magnitude from the Si homo-junction reference device. The subthreshold swing (SS), can also be reduced from that of Si homo-junction case. The structural parameter influence on the electrical characteristics revealed that a low substrate impurity concentration lead to lower SS as a result of larger tunneling distance modification by the gate voltage. It was also shown that the alignment of the gate edge to the hetero-junction lead to the smallest SS and the largest drain current by the realization of the largest electric field at the junction. Scaling of the gate length leads to the increase in SS because the drain potential induces larger leakage current by the drain induced tunneling width reduction. But with the drain voltage decrease in accordance with the gate length scaling, the high drivability and low SS of Si based TFET device could be maintained.

Finally, advantages of Schottky barrier and heterojunction tunnel FET with silicide/silicon junction are summarized in the form of their performance comparison with the conventional MOSFETs as below. This table clearly indicates that with the minimal reduction of the on current, large *Ion/Ioff* ratio as well as small SS are realized in SBTFETs and heterojunction tunnel FETs especially for short channel devices.

***Table 7.1**: Comparison of TFETs using Silicide/Si junctions in this study to the conventional MOSFETs in short channel (V_d=0.3V)*

	L_{gate}	Ion (μV/μm)	Ion/Ioff	SS
pn conventinal	10 nm	680	$1.8x10^2$	150
Thermionic FE (Cha. 3,4) Schottky tunnel	short (10nm)	567	$5.5x10^3$	120
Zenner (Cha. 5,6) B to B tunneling	short (20nm)	300	$3.0x10^9$	15
	Short (20nm V_D=1.0) (hypothetical 10nm)	300	$5.0x10^6$	43

7.2 Further Study

As summarized above, I have studied Si-based tunneling FETs using Silicide/Si source-channel interface with 2-D device simulation, but the discussion was limited for N-type tunneling FETs. (I used the word 'N-type' as the device, in which electron is the main carrier in the channel under the gate.) Considering the utilization of CMOS circuits with N-type and P-type tunneling FETs, further study should be done for P-type tunneling FETs. As introduced in Chapter 5, the appropriate semiconducting silicide for P-type device would be β-$FeSi_2$. Therefore, similar discussion as in Chapter 6, assuming N-type β-$FeSi_2$/Si hetero-junction source/channel contact would be useful, although there still remains the issue such as how to implement different silicides for N-FETs and

P-FETs on the same surface. Further discussion on circuits such as SRAM and so on using those materials would be also very useful.

On the other hand, although it is revealed that Mg_2Si hetero-junction tunneling FET using band-to band tunneling can be one of the promising candidates for Si-based steep SS device with high drivability, this result is still a prediction from the device simulation. Therefore, this prediction should be verified with fabrication and evaluation of devices. Although Mg_2Si has been investigated for its usage in optoelectronic, thermoelectricity, and photovoltaic devices, it is not studied as a material for nano-electronics. Therefore, its electrical characteristics as well as compatibility to Si ULSI processes have to be investigated.

Formation of silicide/Si interface with a good integrity itself would be an important topic of research. In that sense, a novel silicidation process using annealing of metal/Si thin film stacks proposed in chapter 4 would be a good method also for the formation of semiconducting silicide/Si interfaces.

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List of Publications and Presentations

Journals

[1] Y. Wu, C. Dou, F. Wei, K. Kakushima, K. Ohmori, P. Ahmet, T. Watanabe, K. Tsutsui, A. Nishiyama, N. Sugii, K. Natori, K. Yamada, Y. Kataoka, T. Hattori, and H. Iwai, "Influence of Structural Parameters on Electrical Characteristics of Schottky Tunneling Field-Effect Transistor and Its Scalability", Japanese Journal of Applied Physics, Volume 52, Number 4, 04CC28.

[2] Y. Wu, H. Hasegawa, K. Kakushima, K. Ohmori, T. Watanabe, A. Nishiyama, N. Sugii, H. Wakabayashi, K. Tsutsui, Y. Kataoka, K. Natori, K. Yamada, and H. Iwai, "A novel hetero-junction Tunnel-FET using Semiconducting silicide-Silicon contact and its scalability", Accepted for publication, Microelectronics reliability

International Conference (peer review)

[1] Y. Wu, C. Dou, K. Kakushima, K. Ohmori, P. Ahmet, T. Watanabe, K. Tsutsui, A. Nishiyama, N. Sugii, K. Natori, K. Yamada, Y. Kataoka, T. Hattori, and H. Iwai,, "Influence of Structural Parameters on Electrical Characteristics of Schottky Tunneling Field-Effect Transistor and Its Scalability",International Conference on Solid State Devices and Materials (SSDM 2012)

[2] Y. Wu, H. Hasegawa, K. Kakushima, K. Ohmori, H. Wakabayashi, K. Tsutsui, A. Nishiyama, N. Sugii, Y. Kataoka, K. Natori, K. Yamada and H. Iwai, "Influence of Band

Discontinuities at Source-Channel Contact on Tunnel FET Performance", 2013 International Workshop on DIELECTRIC THIN FILMS FOR FUTURE ELECTRON DEVICES (IWDTF2013)

Other conferences

[1] Y. Wu, N. Shigemori, S. Sato, K. Kakushima, P. Ahmet, K. Tsutsui, A. Nishiyama, N. Sugii, K. Natori, T. Hattori and H. Iwai, "Observation of tunneling FET operation in MOSFET with NiSi/Si Schottky source/channel interface",218th Electrochemical Society (ECS) Meeting

[2] Y. Wu, N. Shigemori, S. Sato, K. Kakushima, P. Ahmet, K. Tsutsui, A. Nishiyama, N. Sugii, K. Natori, T. Hattori and H. Iwai, "Observation of NiSi/Si Schottky source/channel interface electrical characteristic",Taiwan-Japan Workshop "Nano Devices"

[3] Yan Wu, K. Kakushima, P. Ahmet, A. Nishiyama, N. Sugii, K. Tsutsui, K. Natori, T. Hattori and H. Iwai "An analytical model of a tunnel FET with Schottky junction", G-COE PICE International Symposium and IEEE EDS Minicolloquium on Advanced Hybrid Nano Devices (IS-AHND)

[4] Yan Wu, K. Ohmori, K. Kakushima, A. Nishiyama, K. Yamada, H. Iwai "The tunnel FET with schottky contact simulation",Tsukuba Nanotechnology Symposium 2011

[5] K. Matsumoto, M. Koyama, Yan Wu, K. Kakushima, P. Ahmet, K. Tsutsui, A.

Nishiyama, N. Sugii, K. Natori, T. Hattori, H. Iwai “Size dependent resistivity change of Ni-silicides in nano-region”, Workshop and IEEE EDS Mini-colloquium on Nanometer CMOS Technology

[6] Yan Wu, K. Kakushima, P. Ahmet, A. Nishiyama, N. Sugii, K. Tsutsui, K. Natori, T. Hattori and H. Iwai “A Study on Fabrication and Analytic Modeling of novel Schottky contact tunneling Transistors”,IEEE EDS MQ WIMNACT 32

[7] Yan Wu, K. Ohmori, K. Kakushima, A. Nishiyama, K. Yamada, H. Iwai “Influence of Structural Parameters on Schottky Tunneling Field-Effect Transistor”,Tsukuba Nanotechnology Symposium 2012

[8] Yan Wu, K. Kakushima, P. Ahmet, A. Nishiyama, N. Sugii, K. Tsutsui, K. Natori, T. Hattori and H. Iwai “Electrical Analyses of Nickel Silicide Formed on Si Nanowires with 10-nm-width”,International Symposium on Next-Generation Electronics (ISNE 2013)

[9] Yan Wu, K. Ohmori, K. Kakushima, A. Nishiyama, K. Yamada, H. Iwai “A study of Band offset in Source-Channel Contact improve Tunnel FET Performance”,Tsukuba Nanotechnology Symposium 2013