論文 / 著書情報
Article / Book Information

題目(和文)	ECRスパッタ法により形成した極薄HfNゲート絶縁膜に関する研究
Title(English)	A study on ultrathin hafnium nitride gate insulator formed by ECR plasma sputtering
著者(和文)	韓熙成
Author(English)	Hui-seong Han
出典(和文)	学位:博士(工学), 学位授与機関:東京工業大学, 報告番号:甲第9247号, 授与年月日:2013年6月30日, 学位の種別:課程博士, 審査員:大見　俊一郎,半那　純一,筒井　一生,渡辺　正裕,宮本　智之,嶋田　勝
Citation(English)	Degree:Doctor (Engineering), Conferring organization: Tokyo Institute of Technology, Report number:甲第9247号, Conferred date:2013/6/30, Degree Type:Course doctor, Examiner:,,,,,
学位種別(和文)	博士論文
Type(English)	Doctoral Thesis

Doctoral Thesis

A study on ultrathin hafnium nitride gate insulator formed by ECR plasma sputtering

January, 2013

Supervisor : Associate Professor Shun-ichiro Ohmi

Presenter : Huiseong Han

Dept. of Electronics and Applied Physics

Interdisciplinary Graduate School of Science Engineering

Tokyo Institute of Technology

A study on ultrathin hafnium nitride gate insulator formed by ECR plasma sputtering

Contents

Chapter 1

Introduction

In this chapter, the problem of the conventional SiO_2/poly-Si and why the high-k/metal gate structure is required will be explained. The issues of high-k gate insulator such as interfacial layer and flat-band voltage roll-off are also previewed. Furthermore, the requirements of high-k nitride gate insulator and hafnium nitride gate insulator will be explained for replacing the conventional oxide high-k. Finally, the purposes of this study and the outline of this thesis are summarized.

1.1 Trends of MOSFET scaling

The integrated circuit (IC) industry has been able to maintain an impressive set of trends governing device and performance. Silicon-based metal-oxide-semiconductor field effect transistor (MOSFET) technology has provided an enabling platform for continuous improvement in density, switching speed, and cost per transistor. This improvement is achieved by reducing the dimensions of the key component of these circuits. The scaling of MOSFETs follows the Moore's law, which predicts the exponential increase in the number of transistors integrated on a chip [1]. Since the 1970s, transistor density has doubled every 18 months. This trend reflects the tremendous impact of continuously reducing transistor dimensions and adjusting circuit parameters in a coordinated manner. In addition to gains in transistor density, the intrinsic switching delay for high-performance logic has historically decreased 17% per year. Furthermore, the smallest line width or the minimum feature length has been reduced at a rate of about 13% per year [2]. At that rate, the minimum feature length will shrink to about 28 nm in the 2012. In the future, digital ICs will be able to perform date processing and numerical computation at terabit-per-second rates. As the device becomes smaller, it consumes less power. Therefore, device miniaturization also reduces the energy used for each switching operation. The energy dissipated per logic gate has decreased by over one million times since 1959.

1.2 High-k/metal gate structure for MOSFET

In order to obtain the high on-current, the scaling of MOSFETs is necessary. One of the key elements that allowed the successful scaling of silicon-based MOSFETs is certainly the excellent material and electrical properties of the gate dielectric so far used in these devices, that is SiO_2. This material indeed presents several important features that have allowed its use as a gate insulator. First of all, amorphous SiO_2 is able to be thermally grown on silicon with excellent control in thickness, uniformity, and naturally forms a very stable interface and realize a low density of intrinsic interface defects. Secondly, SiO_2 presents an excellent thermal and chemical stability, which is required for the fabrication of transistors that includes annealing steps at high temperature.

All these superior properties allowed the fabrication of properly working MOSFETs with SiO_2 gate insulator as thin as 1.5 nm [3-4]. However, further scaling of the SiO_2 gate insulator thickness is problematic. The first problem arising from the scaling of the SiO_2 layer thickness concerns the leakage current flowing through the MOS structure. When, the thickness of the SiO_2 layers becomes below 3 nm, carriers are able to flow through the gate dielectric by a direct tunneling mechanism [5-6]. This mechanism involves the tunneling of charge carriers through an energy barrier, the called direct tunneling process [7]. Therefore, in the most aggressive high performance technologies, high-k gate insulator should be introduced to replace the SiO_2.

In this section, the problem of the conventional SiO_2/Poly-Si structure and trends of high-k material will be described.

1.2.1 The problems of the conventional SiO_2/poly-Si structure

As mentioned above, SiO_2 as a gate insulator and poly-Si as a gate electrode were used in the MOSFETs. The SiO_2 has some advantages such as good interface property, thermally stability, and wide bandgap (8.9 eV). And the poly-Si electrode also has many advantages such as a self-align process with implantation of source and drain regions. In recently, however, the limitation of the SiO_2/poly-Si structure becomes remarkable, because of the leakage current and power dissipation due to the tunneling. Figure 1-1 shows current density as a function of the EOT for each application [2]. It is found that the leakage current of SiO_2 is much larger than required value at high performance (HP) and low operation power (LOP). Furthermore, SiO_2/poly-Si structure has other problems such as the reducing of the capacitance due to the depletion of poly-Si electrode and the increasing of RC delay due to the high resistivity of poly-Si electrode. Especially, the p^+ poly-Si has been widely used. The BF_2 implantation is typically used to form the p^+ poly-Si. However, the p^+ poly-Si is not able to suppress the boron penetration through the thin SiO_2 into the Si substrate and causes the increase of interface states [8]. This results in a large threshold voltage (V_{th}) shift, a large charge trapping rate and a poor reliability of device. It has also indicated that the more fluorine atoms pile up at the poly-Si/SiO_2 and Si/SiO_2 interfaces.

For the reason, it is found that the limitation of the SiO_2 thickness is 1 - 1.2 nm and the SiO_2 thickness approaches its limits. An alternative way of increasing the capacitance is to use an insulator with a higher dielectric constant than that of SiO_2. Moreover, there are many researches of metal gate electrode which has low resistivity.

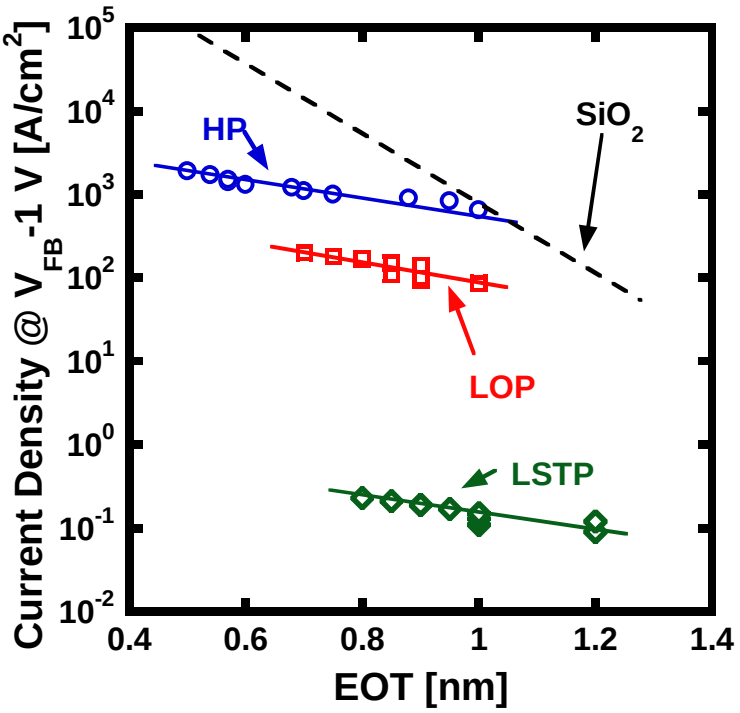


Fig. 1-1 Requirement of current density and EOT for each application.

1.2.2 Trends of high-k material

An insulator with a high dielectric constant is represented by high-k. One could use a thicker gate layer and reduce the leakage current flowing through the structure and also improve the reliability of the gate insulator. A lot of research efforts have been focused recently on the investigation of high-k gate insulator [8], for the potential replacement of SiO_2 in advanced complementary metal-oxide-semiconductor (CMOS) technologies. A list of materials studied is given in Table 1-1, with their relative dielectric constants and band gaps.

The advantage of using high-k materials as a gate insulator in the next generations of MOSFETs is that using high-k ($\varepsilon_r = 39$) would allow us to use a 10 nm thick layer in order to achieve a capacitance equivalent to a 1 nm-thick SiO_2. The thickness becomes 10 times for the thickness of SiO_2. It is able to be reduced leakage current with same capacitance.

However, the material that could potentially replace SiO_2 as a gate insulator in advanced CMOS technologies should also satisfy other requirements as following [8].

- Good thermal stability in contact with Si, preventing the formation of a thick SiO_x interfacial layer and the formation of silicide layers.
- Low density of intrinsic defects at the Si/insulator interface and in the bulk of the material, providing high mobility of charge carriers in the channel and sufficient gate insulator lifetime.
- A sufficiently large energy band gap, providing high energy barriers at the Si/insulator and metal gate/insulator interfaces, in order to reduce the leakage current flowing through the structure.

Table 1-1 Examples of high-k materials with relative dielectric constants and band gaps.

	SiO_2	Al_2O_3	ZrO_2	HfO_2	Ta_2O_5
ε_r	3.9	9	25	20	26
Band gap [eV]	8.9	8.7	5.7	6	4.5

- Compatibility of material with CMOS processing, like high thermal budgets.

The potential high-k gate insulator should thus meet most of these requirements.

Next, the high-k gate insulators which were used in many researches are introduced.

- Al_2O_3 [9-10] : Aluminium oxide is an amphoteric oxide with the chemical formula Al_2O_3. It is an electrical insulator and has a relatively high thermal conductivity. The ε_r and band gap are reported as 9 and 8.7 eV, respectively. In case of Al_2O_3 which is deposited by atomic layer deposition (ALD) method using $Al(CH_3)_3$-H_2O process, a thin interfacial layer (0.15 nm) was found after room temperature air exposure of thin Al_2O_3 film (< 4nm). Using an upper limit of 1 A/cm^2 for the gate leakage current density, Al_2O_3 was concluded to be scalable down to EOT as 1.3 nm.

- ZrO_2 [11-12] : The ε_r and band gap of zirconium oxide are reported as 25 and 5.7 eV, respectively. The ALD process is used based on the $ZrCl_4$-H_2O. However, there is a problem which is particle transportation from the sources to the films. It is known that the chlorine residues are preferentially located at the ZrO_2-Si interface when the film is deposited. Post deposition annealing (PDA) at 1000^{o}C has been found to decrease the

chlorine residue contents in the ZrO_2 film.

- HfO_2 [13-15] : The ε_r and band gap of hafnium oxide are reported as 20 and 6 eV, respectively. The ALD process with the $HfCl_4$-H_2O is used. However, it also has same problem similar to ZrO_2. The crystallization was quite strongly dependent on the annealing condition and deposition method. For example, ALD-HfO_2 was crystallized at 700^oC and DC sputtering-HfO_2 was not crystallized at 900^oC.

1.3 Issue of high-k gate insulator

There are some issues of the high-k gate insulator such as EOT scaling, high-k reliability, mobility, and V_{th} roll-off. The EOT scaling has been studied to replace SiO_2. It is one of the key to obtain the high on-current for the next generation CMOS. Furthermore, V_{th} reliability is also important to reduce the power consumption.

In this chapter, the interfacial layer between the high-k gate insulator and Si substrate and flat-band voltage (V_{FB}) roll-off will be discussed.

1.3.1 Interfacial layer between high-k gate insulator and Si substrate

EOT scaling is very important in terms of high on-current and scaling of MOSFET. To obtain lower EOT, high dielectric constant material is required. However, it is found that the deposition of high-k oxide films on silicon forms an interfacial layer with low dielectric constant. Since this interfacial layer is in series with the deposited material, its EOT should be added to that of the high-k layer. Figure 1-2 shows the formation of interfacial layer between high-k film and Si substrate. When HfO_2 is deposited on Si substrate, an ultrathin low-k interfacial layer, SiO_x, forms at the HfO_2/Si interface [16]. An interfacial layer grows either during the deposition of the high-k gate insulator or during post deposition annealing process (PDA). It should be noticed that another low-k layer is formed at the high-k insulator/metal gate interface. The presence of the low-k interfacial layer increases the EOT of the gate stack, and should thus be as thin as possible to achieve the sufficient EOT required by the International Technology Roadmap for Semiconductors (ITRS). Furthermore, Harada et al. reported that the out-diffusion of silicon into HfO_2 leads to an unintentional silicate interfacial layer, and this interfacial layer leads the lack of the reliability [17]. A number of

groups have shown that nitridation of the surface of the Si before high-k deposition will reduce the thickness of the interfacial layer, but most nitridation also increases the fixed charge density of the stack. However, Park et al. found that the precursor appeared to form a silicate interfacial layer when deposited at 200°C, but this layer caused to phase separation into SiO_2 and HfO_2 when PDA was carried out at temperatures above 500°C [18]. It may be that the nitrogen content of these films is sufficient to suppress the up-diffusion of Si, while the typical metal organic sources do not form an oxynitride at the interface.

Therefore, it is important to suppress the interfacial layer. Recently, the direct stacking of high-k gate insulator technique has been studied. The direct contact architecture would eliminate the increase of EOT from the interfacial layer [19-20]. This method is expected to suppress the interfacial layer formation.

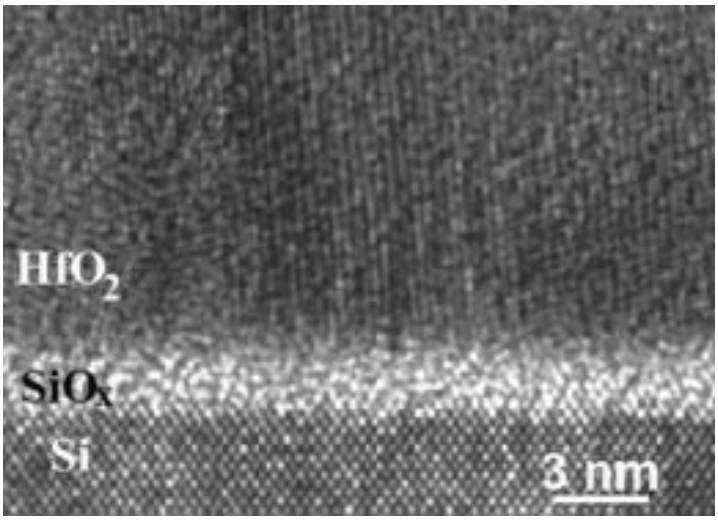


Fig. 1-2 Interfacial layer formation between high-k film and Si substrate [16].

1.3.2 Flat-band voltage roll-off

While employing metal electrodes with high-k dielectrics has many advantages such as elimination of poly depletion and better compatibility with high-k materials, such drastic modification of the CMOS process introduces several challenges. The most difficult issue is obtaining metal gate electrodes with work function matching with the Si valence- and conduction-band edges, respectively. This is important for gate stack electrical characteristics since V_{th} in scaled devices is controlled by the V_{FB}, determined by the gate stack effective work function, which includes modifications to the work function values by charges and dipoles in the dielectric and its interfaces [21]. However, when these gate stacks consisting of the metal electrode, high-k dielectric, and interfacial layer were used in devices of practical interest with scaled down of EOT, their effective work function values were found to be significantly less than those obtained in test structures with thicker gate stacks [22]. This phenomenon, which significantly limits the available options for high-k/metal transistor fabrication, is called V_{FB} roll-off.

V_{FB} roll-off is dependent on some factors such as thickness of the interfacial layer, temperature, electrode work function, high-k thickness and composition. Several models for V_{FB} roll-off have been proposed [23-25], with each one being primarily focused on a limited subset of the V_{FB} roll-off dependences on the gate stack components and processes. In case of interfacial layer, if the thickness of the interfacial layer is thinner, it is easier to obtain small EOT as mentioned in chapter 1.3.1. Unfortunately, when the interfacial layer becomes less than 2 nm, a V_{FB} shift emerges and it is a big challenge to simultaneously achieve low V_{th} [22]. Recent reports have attempted to explain this phenomenon by bulk charge generation, oxygen or bottom

interface dipole at high-k/SiO_2 interfacial layer [23, 26]. However, the observed V_{FB} roll-off is independent of EOT and it is contradictory to bulk charge generation. Furthermore, the model describing the dipole at the high-k/SiO_2 interface fails to explain the V_{FB} roll-off when the thickness of SiO_2 becomes thinner [26]. Especially, the V_{FB} roll-off was caused by oxygen vacancy. Since the charge state of oxygen vacancies in the interfacial SiO_2 layer depends on the position of the substrate Fermi level, the probability for a vacancy to be in a positive charge state (rather than in neutral one) increases in a gate stack fabricated with p-Si as shown in Fig. 1-3 [27].

Therefore, understanding of the V_{FB} roll-off mechanism would guide process improvement toward mitigating the generation of oxygen vacancies in the interstitial SiO_2 layer and suppressing the migration of oxygen vacancies from the high-k dielectric into the interfacial SiO_2.

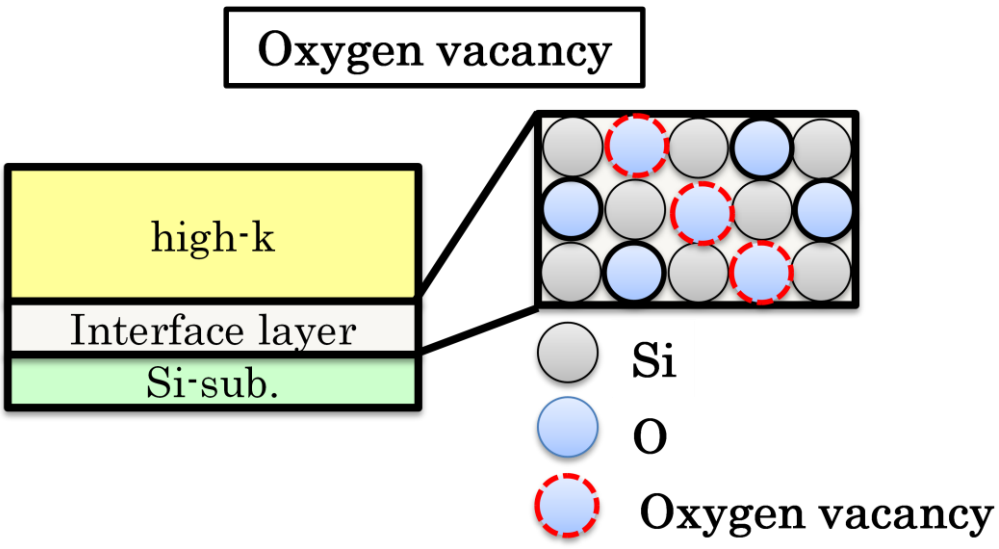


Fig. 1-3 A schematic of oxygen vacancy in the MIS structure.

1.4 Nitride gate insulator

The high-k material which is introduced to many applications includes oxygen. It means that the interfacial layer is easy to be formed and affects to the limitation of EOT scaling and V_{FB} roll-off. To overcome these problems, we propose the use of nitride gate insulator.

In this chapter, nitride gate insulator will be introduced, and especially, the hafnium nitride high-k gate insulator will be introduced as a purpose of this study.

1.4.1 Properties of nitride gate insulator

Nitride insulators are the candidate materials as a gate dielectric instead of oxide dielectrics to suppress interfacial layer formation. The most of the nitride dielectrics reported so far, such as SiN or AlN [28-29]. Among the nitride insulators, SiN is also being investigated as possible replacement of SiO_2. SiN is much easier to integrate into existing CMOS processes, and therefore it is a more likely candidate for the first post-SiO_2 gate dielectrics. Therefore, many researchers have been studied SiN as a gate insulator [30-33]. Among these reports, the SiN formed by a novel Jet Vapor Deposition (JVD) technique with the water vapor annealing treatment showed good electrical properties with lower gate leakage current in the ultrathin regime (< 5 nm) as shown in Fig. 1-4 [31]. The JVD process relies on supersonic jets of a light carrier gas such as helium to transport depositing vapor from the source to the substrate, and has been used to synthesize a wide variety of thin films of metals, semiconductors, and insulators [34-35]. Because of the separation of the depositing species, and their short transit times, there is very little chance for gas-phase nucleation. Metal-insulator-semiconductor (MIS) capacitors formed by the JVD silicon nitride

deposited on Si substrates, exhibit a number of properties that are attractive for ULSI applications, including low leakage current, high breakdown strength, high resistance to hot-carrier damage, high resistance to boron penetration, and high resistance to oxidation. Compared to their MOSFET counterparts, metal-nitride-semiconductor (MNS) FET made of JVD silicon nitride exhibit reduced low-field transconductance and enhanced high-field transconductance [31].

Even though SiN has good electrical properties, it has a limitation to apply ULSI applications. The critical point is that the dielectric constant of SiN is not high enough. The relative dielectric constant of SiN is about 7. That is just 2 times higher than that of SiO_2. Therefore, new material with high relative dielectric constant beyond that of SiN is necessary.

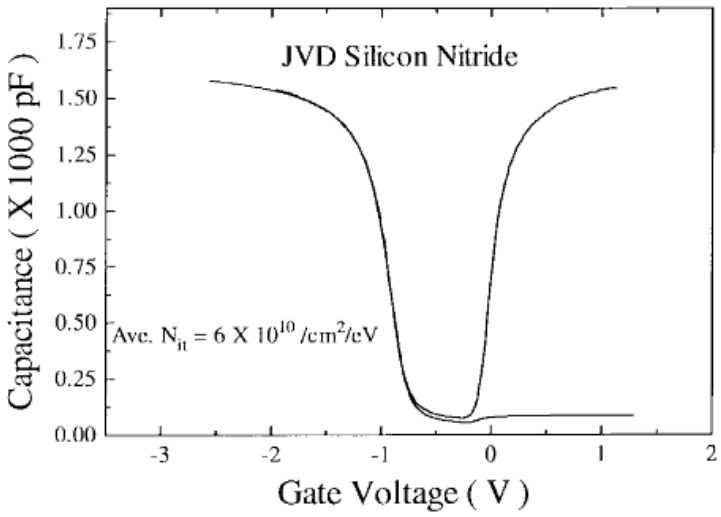


Fig. 1-4 C-V curve for the MIS diode with a JVD silicon nitride [31].

1.4.2 Hafnium nitride (HfN) gate insulator

The mononitride of hafnium of stoichiometry HfN is all metallic conductors [36]. On the other hand, the higher nitride of hafnium is reported to be transparent insulators or semiconductors [37]. In general, the properties of group IV nitrides are well-understood for nitrogen poor materials [36], but the nitrogen-rich compositions remain an active area of research. In addition, the nitrogen-rich HfN has high dielectric constant such as 30 [37].

Figure 1-5 shows the structures of metallic and insulating HfN [38]. The metallic HfN has a NaCl cubic structure. When the ratio of hafnium is either same or larger than that of nitrogen in the film, it shows metallic property. However, when the ratio of nitrogen is larger than that of hafnium, the phase is changed from metal to insulator [36]. At that time, the structure is also changed as shown in Fig. 1-5(b). The bulk resistivity of insulating HfN is larger than 1 Ωcm [39]. Lai et al. reported that the effects of N_2 flow ratio and post metal annealing on the work function of HfN_x gate electrode by dc reactive sputtering as shown in Fig. 1-6 [40]. It showed that the resistivity is modulated by N_2 flow ratio. It means that the phase would be changed by N_2 flow ratio. The mechanism of phase change from metal to insulator is explained as follows. However, it was not sufficient to form the high-quality HfN_x film by rf sputter. In case of Zr_3N_4, zirconium is a transition metal which has a 4 d orbital as a valence band. During the transformation of ZrN into Zr_3N_4 by N_2^+ bombardment, the d-band at the Fermi level is completely depleted. The N 2p band grows as a consequence of a transfer of electrons from the d-band to new available N 2p states until the d-band is completely depopulated and the nitride becomes an insulator [40]. In this manner, HfN also has same mechanism.

Kim et al. reported the atomic layer deposition of ultrathin insulating nitride layer such as Hf_3N_4 on p-Ge(100) substrate as an interfacial layer for HfO_2 and it showed good electrical property with an EOT of 0.82 nm as shown in Fig. 1-7 [42].

These properties of HfN are suitable for ultrathin gate insulator application

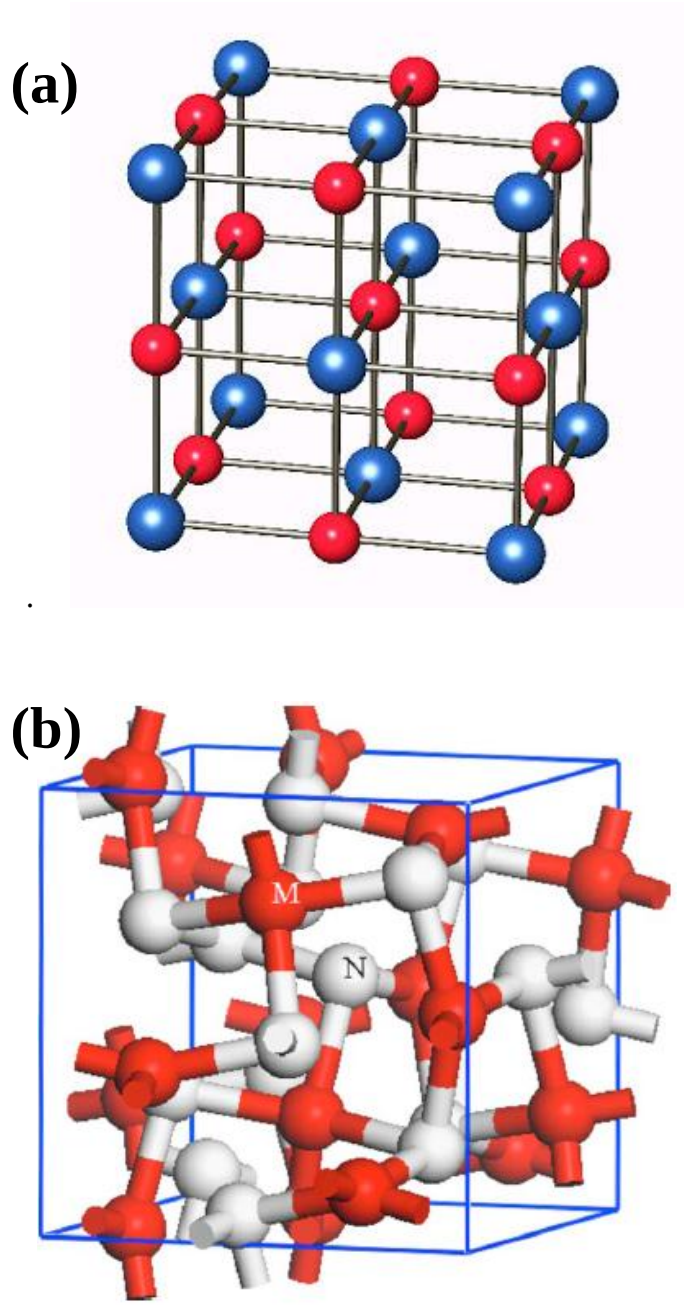


Fig. 1-5 Structures of (a) metallic and (b) insulating HfN [38].

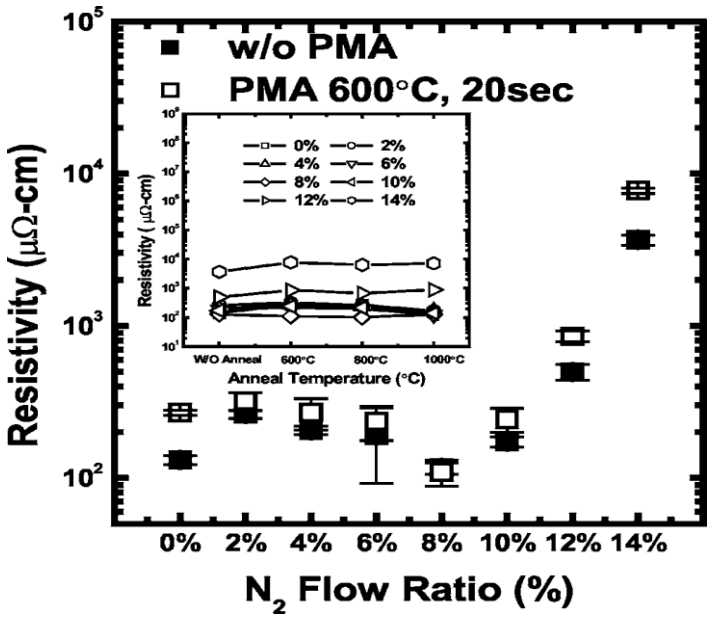


Fig. 1-6 Influence of the N_2 flow ratio on the resistivity of the HfN_x film [40].

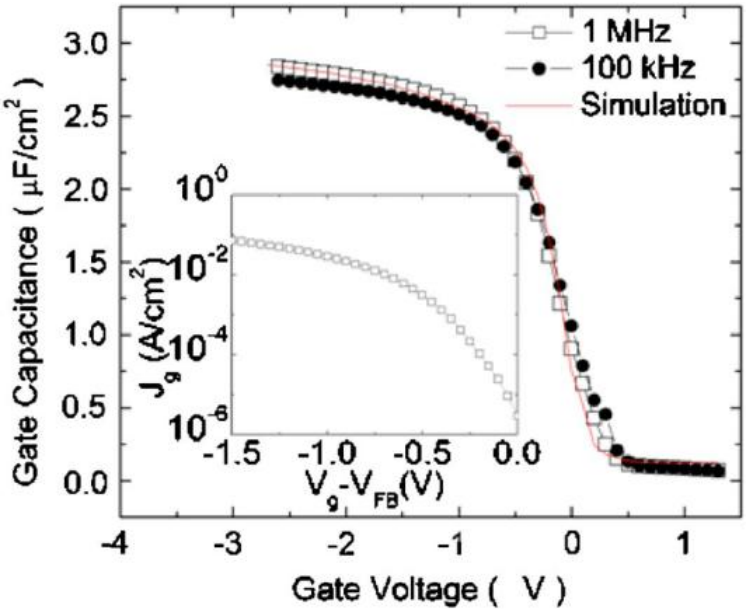


Fig. 1-7 C-V curves of a $WN/HfO_2/Hf_3N_4$/p-Ge MOS capacitor [42].

1.5 Purpose and outline of this dissertation

The main purpose of this study is to obtain under 0.5 nm-thick EOT using HfN gate insulator formed by electron-cyclotron-resonance (ECR) plasma sputtering. Among the plasma source, because, the ECR source operates on microwave energy coupled to the natural resonant frequency of the plasma electrons in the presence of a static dc magnetic field and it is able to deposit metal and insulator with low damage. Amorphous film of nitrogen-rich HfN gate insulator was investigated for the first time. The details of strategies to accomplish this main purpose are itemized as follows.

- The deposition conditions of HfN gate insulator are carefully optimized.

- To improve the electrical properties, post deposition annealing is investigated in forming gas (N_2/4.9%H_2) and nitrogen ambient. Furthermore, physical and chemical properties are also examined.

- Dependence of deposition gas pressure condition and dependence of pre-sputtering condition are investigated for improvement of electrical properties. Furthermore, to obtain beyond 0.5 nm-thick EOT, the characteristics of HfN gate insulator with various thicknesses are evaluated.

- Reliability of HfN gate insulator is investigated. Activation energy, time dependence dielectric breakdown, and stress induced leakage current are evaluated.

- MISFET using HfN gate insulator is fabricated and evaluated.

Under these detailed strategies, the ultrathin HfN gate insulator formed by ECR plasma sputtering will be studied as a promising candidate for next generation high-k gate insulator.

This thesis is composed of 6 chapters. Figure 1-6 shows the outline of this thesis.

In chapter 1, an overview of trends of MOSFET scaling is described. And then, high-k/metal gate structure for MOSFET is introduced from the problem of conventional SiO_2/poly-Si structure. Next, issues of high-k gate insulator are explained such as interfacial layer and V_{FB} roll-off. Finally, the reason of using HfN gate insulator is explained.

In chapter 2, the fabrication methods for HfN gate insulator based devices and their basic principles are discussed. Especially, in order to deposit the hafnium nitride gate dielectric with a good performance, the damage to the dielectric by sputtering should be minimized. Several issues and technologies on them are presented. Finally, the characterization methods for HfN gate insulator based device are summarized.

In chapter 3, the fabrication of HfN gate insulator based devices and their basic principles are discussed. Especially, in order to obtain the insulating properties of hafnium nitride film, the conditions should be optimized. Furthermore, in order to improve the characteristics of HfN gate insulator, hydrogen annealing is investigated.

In chapter 4, the reliability for HfN gate insulator is discussed. In order to calculate the activation energy, the measurement temperature dependence of leakage current

density is evaluated. Furthermore, the time dependent dielectric breakdown (TDDB) is investigated compared to SiN. Finally, the stress induced leakage current is also evaluated.

In chapter 5, the fabrication of metal-insulator-semiconductor field effect transistor (MISFET) using HfN gate insulator and its electrical properties are discussed. First, the etching rate for the HfN should be investigated. Finally, the characterization of electrical properties for the fabricated MISFET will be introduced.

In chapter 6, the obtained results in this study are summarized and concluded. Furthermore, the prospect of this research is discussed.

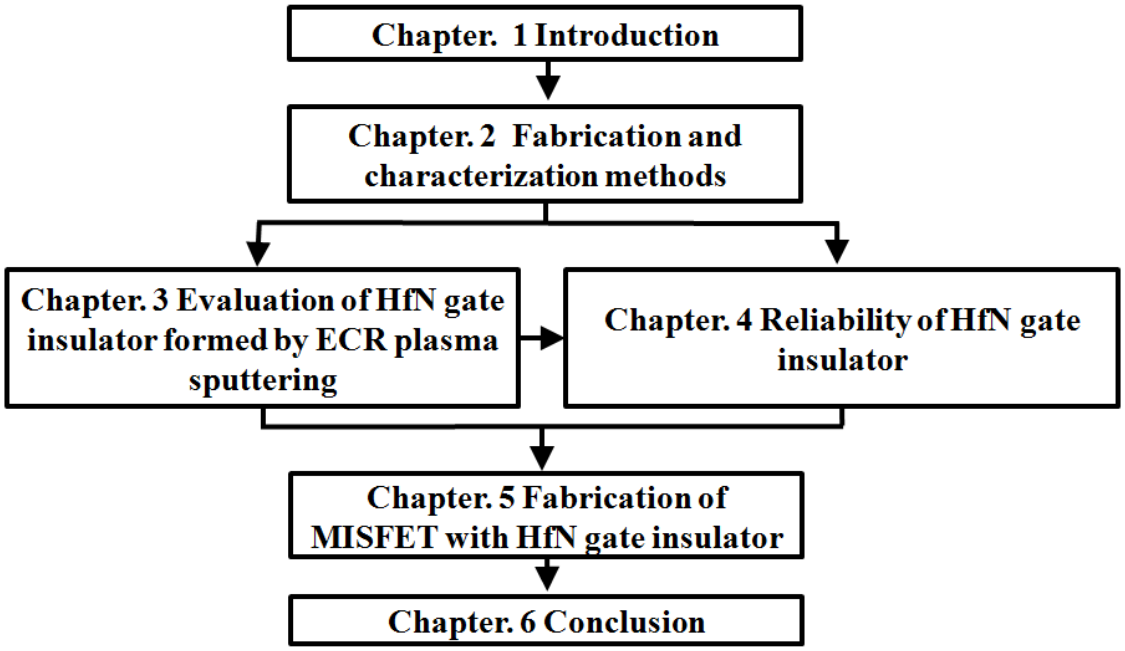


Fig. 1-6 Outline of this thesis.

References

[1] G. E. Moore, “Cramming More Components onto Integrated Circuits”, *Electronics*, vol. 38, pp. 114-117, 1965.

[2] *The International Technology Roadmap for Semiconductors*, 2011 Ed., Semiconductor Ind. Assoc., 2011 (http://www.itrs.net).

[3] G. Timp, J. Bude, K.K. Bourdelle, J.Garno, and M. Green, “The Ballistic Nanotransistor”, *IEDM. Tech. Dig.*, pp. 55-58, 1999.

[4] R. Chau, F. Kavalieros, B. Roberds, R. Schenker, D. Lionberger, D. Barlage, B. Doyle, R. Arghavani, A. Murthy, and G. Dewey, “30 nm physical gate length CMOS transistors with 1.0 ps n-MOS and 1.7 ps p-MOS gate delays”, *IEDM. Tech. Dig.*, pp. 45-48, 2000.

[5] D. A. Muller, T. Sorsch, S. Moccio, F. H. Baumann, K. Evans-Lutterodt, and G. Timp, “The electronic structure at the atomic scale of ultrathin gate oxides”, *Nature*, vol. 399, pp. 758, 1999.

[6] S. H. Lo, D. A. Buchanan, Y. Taur, and W. Wang, “Quantum-Mechanical Modeling of Electron Tunneling Current from the Inversion Layer of Ultra-Thin-Oxide nMOSFET’s”, *IEEE Electron Dev. Lett.*, vol. 18, pp. 209-211, 1997.

[7] A. T. Fromhold, Quantum Mechanics for Applied Physics and Engineering (New York: Dover), 1981.

[8] G. D. Wilk, R. M. Wallace, and J. M. Anthony, “High-k gate dielectrics: Current status and materials properties considerations”, *J. Appl. Phys.*, vol. 89, pp. 5243-5275, 2005.

[9] J. H. Lee, K. Koh, N. I. Lee, M. H. Cho, Y. K. Kim, J. S . Jeon, K. H. Cho, H. S .

Shin, M. H. Kim, K. Fujihara, H. K. Kang, and J. T. Moon, “Effect of polysilicon gate on the flatband voltage shift and mobility degradation for ALD-Al_2O_3 gate dielectric”, *IEDM. Tech. Dig.*, pp. 645-648, 2000.

[10] D. A. Buchananl, E. P. Gusev, E. Cartier, H. Okorn-Schmidt, K. Rim, M. A. Gribelyuk, A. Mocuta, A. Ajmera, M. Copel, S. Guha, N. Bojarczuk, A. Callegari, C. D. Emicl, P. Kozlowskil, K. Chan, R. J. Fleming, P. C. Jamison, J. Brown, and R. Arndt, “80 nm polysilicon gated n-FETs with ultra-thin Al_2O_3 gate dielectric for ULSI applications”, *IEDM. Tech. Dig.*, pp. 223-226, 2000.

[11] W. J Qi, R. Nieh, B. H. Lee, L. Kang, Y. Jeon, K. Onishi, T. Ngai, S. Banerjee, and J. C. Lee, “MOSCAP and MOSFET characteristics using ZrO_2 gate dielectric deposited directly on Si”, *IEDM. Tech. Dig.*, pp. 145-148, 1999.

[12] S. Ferrari, G. Scarel, C. Wiernier, and M. Fanciulli, “Chlorine mobility during annealing in N_2 in ZrO_2 and HfO_2 films grown by atomic layer deposition”, *J. Appl. Phys.*, vol. 92, pp. 7675-7677, 2002.

[13] M. Ritala, M. Leskela, L. Niinisto, T. Prohaska, G. Friedbacher, and M. Grasserbauer, “Development of crystallinity and morphology in hafnium dioxide thin films grown by atomic layer epitaxy”, *Thin Solid Films*, vol. 250, pp. 72-80, 1994.

[14] B. H. Lee, R. Choi, L. Kang, S. Gopalan, R. Nieh, K. Onishi, Y. Jeon, W. J. Qi, C. Kang, and J. C. Lee, “Characteristics of TaN gate MOSFET with ultrathin hafnium oxide (8 Å-12 Å)”, *IEDM. Tech. Dig.*, pp. 39-42, 2000.

[15] B. H. Lee, L. Kang, R. Nieh, W. J. Qi, and J. C. Lee, “Thermal stability and electrical characteristics of ultrathin hafnium oxide gate dielectric reoxidized with rapid thermal annealing”, *Appl. Phys. Lett.*, vol. 76, pp. 1926-1928, 2000.

[16] J. Lu, J. Aarik, J. Sundqvist, K. Kukli, A. Harsta, and J. O. Carlsson, “Analytical TEM characterization of the interfacial layer between ALD HfO_2 film and silicon substrate”, J. *Cryst. Growth*, vol. 273, pp. 510-514, 2005.

[17] Y. Harada, M. Niwa, S. Lee, and D. L. Kwong, “Specific Structural Factors Influencing on Reliability of CVD-HfO_2”, *Symp. VLSI Technol. Dig. Tech.*, pp. 26-27, 2002.

[18] J. H. Park, B. K. Park, M. J. Cho, C. S. Hwang, K. Y. Oh, and D. Y. Yang, “Chemical Vapor Deposition of HfO_2 Thin Films Using a Novel Carbon-Free Precursor”, *J. Electrochem. Soc.*, vol. 149, no. 1, pp. G89-G94, 2002.

[19] C. Choi, C. Y. Kang, S. J. Rhee, M. S. Abkar, S. A. Krishna, M. H. Zhang, H. Kim, T. Lee, F. Zhu, I. Ok, S. Koveshnikov, and J. C. Lee, “Fabrication of TaN-gated Ultra-Thin MOSFETs (EOT< 1.0nm) with HfO_2 using a Novel Oxygen Scavenging Process for Sub 65nm Application”, *Symp. VLSI Technol. Dig. Tech.*, pp. 226-227, 2005.

[20] N. Miyata, “Two-step behavior of initial oxidation at HfO_2/Si interface”, *Appl. Phys. Lett.*, vol. 89, pp. 102903-1-5, 2006.

[21] G. Bersuker, C. S. Park, H. C. Wen, K. Choi, J. Price, P. Lysaght, H. H. Tseng, O. Sharia, A. Demkov, J. T. Ryan, and P. Lenahan, “Origin of the Flatband-Voltage Roll-Off Phenomenon in Metal/High-k Gate Stacks”, *IEEE. Trans. Electron Devices*, vol. 57, no. 9, pp. 2047-2056, 2010.

[22] B. H. Lee, J. Oh, H. H. Tseng, R. Jammy, and H. Huff, “Gate stack technology for nanoscale devices”, *Mater. Today*, vol. 9, no. 85, pp. 32-40, 2006.

[23] S. C. Song, C. S. Park, J. Price, C. Burham, R. Choi, H. C. Wen, K. Choi, H. H. Tseng, B. H. Lee, and R. Jammy, “Mechanism of V_{FB} roll-off with high work

function metal gate and low temperature oxygen incorporation to achieve PMOS band edge work function", *IEDM. Tech. Dig.*, pp. 337-340, 2007.

[24] K. Akiyama, W. Wang, W. Mizubayashi, M. Ikeda, H. Ota, T. Nabatame, and A. Toriumi, "V_{FB} roll-off in HfO_2 gate stack after high temperature annealing process - A crucial role of out-diffused oxygen from HfO_2 to Si", *Symp. VLSI Technol. Dig. Tech.*, pp. 72-73, 2007.

[25] K. Akiyama, W. Wang, W. Mizubayashi, M. Ikeda, H. Ota, T. Nabatame, and A. Toriumi, "Roles of oxygen vacancy in HfO_2/ultra-thin SiO_2 gate stacks", *Symp. VLSI Technol. Dig. Tech.*, pp. 80-81, 2008.

[26] K. Choi, H. C. Wen, G. Bersuker, R. Harris, and B. H. Lee, "Mechanism of flatband voltage roll-off studied with Al_2O_3 film deposited on terraced oxide", *Appl. Phys. Lett.*, vol. 93, no. 13, pp. 133506-1-3, 2008.

[27] G. Bersuker, C. S. Park, H. C. Wen, K. Choi, J. Price, P. Lysaght, H. H. Tseng, O. Sharia, A. Demkov, J. T. Ryan, and P. Lenahan, "Origin of the Flatband-Voltage Roll-Off Phenomenon in Metal/High-k Gate Stacks", IEEE Trans. Electron Devices, vol. 57, pp. 2047-2056, 2010.

[28] Y. C. Yeo, Q. Lu, W. C. Lee, T. J. King, C. Hu, X. Wang, X. Guo, and T.P. Ma, "Direct Tunneling Gate Leakage Current in Transistors with Ultrathin Silicon Nitride Gate Dielectric", *IEEE Electron Device Lett.*, vol. 21, no. 11, pp. 540-542, 2000.

[29] K.S.A. Butcher and T.L. Tansley, "Ultrahigh resistivity aluminum nitride grown on mercury cadmium telluride", *J. Appl. Phys.*, vol. 90, no. 12, pp. 6217-6221, 2001.

[30] X. Guo, T. P. Ma, T. Tamagawa, and B. L. Halpern, "High quality ultra-thin

TiO_2/Si_3N_4 gate dielectric for giga scale MOS technology", *IEDM Tech. Dig.*, pp. 377-380, 1998.

[31] T. P. Ma, "Making Silicon Nitride Film a Viable Gate Dielectric", *IEEE. Trans. Electron Devices*, vol. 45, no. 3, pp. 680-690, 1998.

[32] X. Wang, M. Khare, and T. P. Ma, "Effects of Water Vapor Anneal on MIS Devices Made of Nitrided Gate Dielectrics", *Symp. VLSI Technol. Dig. Tech.,* pp. 226-227, 1996.

[33] S. Mahapatra, V. R. Rao, K. N. ManjulaRani, C. D. Parikh, J. Vasi, B. Cheng, M. Khare, and J. C. S.Woo, "100 nm channel length MNSFETs using a jet vapor deposited ultra-thin silicon nitride gate dielectric", *Symp. VLSI Technol. Dig. Tech.*, pp. 79-80, 1999.

[34] B. L. Halpern, "Fast flow deposition of metal atoms on liquid surfaces", *J. Colloid Interface Sci.*, vol. 86, pp. 337-341, 1982.

[35] X. W. Wang, T. P. Ma, G. J. Cui, T. Tamagawa, J. W. Golz, S. Kareci, B. L. Halpern, and J. J. Schmitt, "Highly reliable silicon nitride films made by jet vapor deposition", *Jpn. J. Appl. Phys.* vol. 34, no. 2B, pp. 955-958, 1995.

[36] L. E. Toth, "Transition metal carbides and nitrides", Academic Press, New York, 1971.

[37] J. S. Becker, E. Kim, and R. G. Gordon, "Atomic Layer Deposition of Insulating Hafnium and Zirconium Nitrides", *Chem. Mater.*, vol. 16, pp. 3497-3501, 2004.

[38] M. Xu, S. Wang, G. Yin, J. Li, Y. Zheng, and L Chen, "Optical properties of cubic Ti_3N_4, Zr_3N_4, and Hf_3N_4", *Appl. Phys. Lett.*, vol. 89, pp. 151908-1-3, 2006.

[39] R. Fix, R. G. Gordon, and D. M. Hoffmann, "Chemical Vapor Deposition of Titanium, Zirconium, and Hafnium Nitride Thin Films", *IEEE. Trans. Electron*

Devices, vol. 45, no. 3, pp. 680-690, 1998.

[40] C. S. Lai, S. K. Peng, T. M. Pan, J. C. Wang, and K. M. Fan, "Work Function Adjustment by Nitrogen Incorporation in HfN_x Gate Electrode with Post Metal Annealing", *Electrochem. Solid-State Lett.*, vol. 9, no. 7, pp. G239-G241, 2006.

[41] P. Prieto, F. Yubero, E. Elizalde, and J. M. Sanz, "Dielectric properties of Zr, ZrN, Zr_3N_4, and ZrO_2 determined by quantitative analysis of electron energy loss spectra", *J. Vac. Sci. Technol. A*, vol. 14, pp. 3181-3188, 1996.

[42] K. H. Kim, R. G. Gordon, A. Ritenour, and D. A. Antoniadis, "Atomic layer deposition of insulating nitride interfacial layers for germanium metal oxide semiconductor field effect transistors with high-k oxide/tungsten nitride gate stacks", *Appl. Phys. Lett.*, vol. 90, pp. 212104-1-3, 2007.

Chapter 2

Fabrication and characterization methods

In this chapter, the fabrication methods for hafnium nitride gate dielectric based devices and their basic principles are discussed. Especially, in order to deposit the hafnium nitride gate dielectric with a good performance, the damage to the dielectric by sputtering should be minimized. Several issues and technologies on them are presented. Finally, the characterization methods for hafnium nitride gate dielectric based device are summarized.

2.1 Fabrication methods

Purpose of this study is to fabricate and evaluate a metal-insulator-semiconductor field effect transistor (MISFET) with ultrathin hafnium nitride (HfN) gate dielectric. To achieve the purpose, it is important to form a HfN gate dielectric on silicon substrate using Electron-cyclotron-resonance (ECR) plasma sputtering method. Moreover, we also used many instruments to fabricate MISFET such as rapid thermal annealing (RTA), thermal evaporation, mask aligner, ion implantation, and so on.

In this section, the fabrication methods for HfN-based devices are described.

2.1.1 Electron-cyclotron-resonance (ECR) plasma sputtering method

When a solid surface is bombarded by atoms, ions, or molecules, many phenomena occur. The kinetic energy of the impinging particles dictates which are the most probable events. For low energies which exceed the binding energy of the target material, surface migration and surface damage effects are taking place. At much higher energies (> 10 keV), the impinging particles travel well into the bulk of the sample before slowing down and depositing their energy. Thus, such particles are most likely to be embedded in the target, and this mechanism is the basis of ion implantation. Some fraction of the energy caused atoms from the surface to be dislodged and ejected into the gas phase. This is called as sputtering.

Among the plasma source, the ECR source operates on microwave energy coupled to the natural resonant frequency of the plasma electrons in the presence of a static dc magnetic field. It is able to deposit metal and insulator. Furthermore, it is an advantage to deposit thin film without substrate annealing [1, 2].

In Fig. 2-1, there is a schematic of an ECR (AFTEX-3400UD-12) with a mirror

magnetic field around the wafer to confine the electron trajectory. The microwave frequency allotted for industrial use is 2.45 GHz. The resonance frequency of the electron will match this microwave frequency value when the magnetic field has a value of 875 gauss (G). Thus, ECR plasma sources are constructed to establish these conditions, as shown in Fig. 2-1. The plasma gas is fed into a chamber maintained at low pressure (e.g., 0.5 to 1.0 mTorr). This chamber is surrounded with magnet coils that set up an axial dc magnetic field with B = 875 G. Microwave power is absorbed by the electrons as described above. If they have a component of motion parallel to the x-axis they will move in a path like spiral shape. Enough electrons must gain energy from the microwave power to sustain the plasma through impact ionization. The ions produced in the plasma chamber diffuse out from it and are accelerated toward the wafer by the rf bias applied to the platform on which the wafers are mounted. Plasma densities of $N_e = 10^{12}/cm^3$ would be achieved toward the low end of the processing pressure range. This density is comparable to the gas concentration itself. Thus, the fractional ionization of the gas in ECR plasmas would approach unity.

In this study, the HfN gate dielectric is deposited using Ar/N_2 plasma by ECR plasma sputtering as shown in Fig. 2-1. At that time, the Hf target is used. In case of rf sputtering, it is difficult to nitrify the film. However, ECR plasma sputtering is easy to nitrify the film and make high quality thin film deposition at room temperature. Furthermore, as mentioned above, the metal and insulator layers also are able to be deposited at the same chamber. It means that the high-k/metal gate stack is able to be formed by in-situ process.

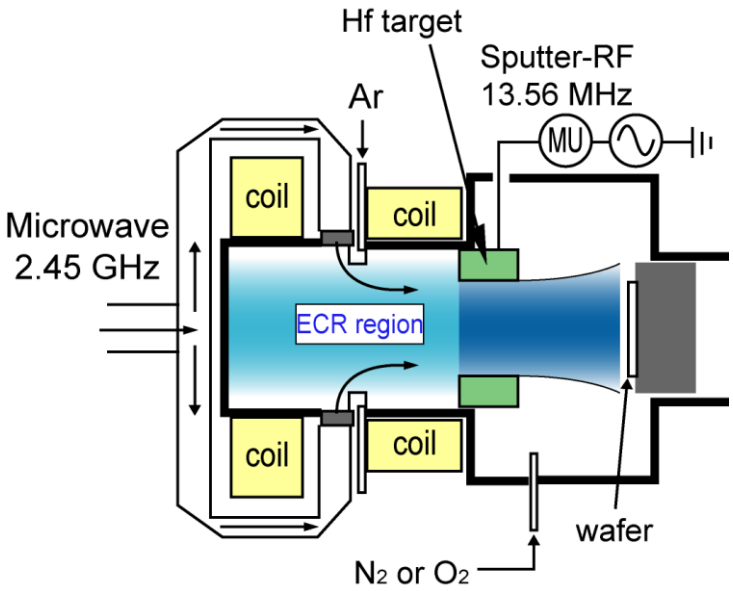


Fig. 2-1 Schematics of electron cyclotron resonance plasma sputter.

2.1.2 Cleaning of substrate

Prior to use a bare Si substrate for integration process of electronic circuit, it should be chemically cleaned to remove the particles as well as any organic, ionic and metallic impurities from the surface. This substrate cleaning process is important for desirable device operations and its reproducibility. Generally, the ultra-clean wafer surface is required to satisfy the conditions as follows [3].

- No particle contamination
- No metal contamination
- No organic contamination
- No water absorption
- No native oxide
- No atomic scale roughness of surface
- Hydrogen-terminated surface
- Electrical neutrality, no ionic contamination

One of the most important chemicals used in full fabrication processes as well as substrate cleaning is ultra-pure water (UPW). UPW is highly purified and filtered to remove all trace of ionic, particulate, and bacterial contamination. The theoretical resistivity of pure water at 25^{o}C is 18.2 MΩ-cm and has fewer than 1.2 colonies of bacteria per milliliter and no particle larger than 0.25 μm. A typical cleaning process using hydrofluoric acid, which is usually called RCA (developed by Radio Corporation of America) cleaning method. In this study, the substrate cleaning process was so designed as to control the ultra-clean Si surface and modified as given in Table 2-1.

Table 2-1 Substrate cleaning procedure.

Cleaning procedure	Removal object
1. Immerse in (4:1) solution of H_2SO_4-H_2O_2 (SPM) for 10 min 2. Wash in DI water for 10 min	Organic, metal contamination
3. Immerse in a (1:100) solution of HF-H_2O for 20 s 4. Wash in DI water for 10 min	Oxide layer
5. Immerse in (4:1) solution of H_2SO_4-H_2O_2 (SPM) for 10 min 6. Wash in DI water for 10 min	Organic, metal contamination
7. Immerse in a (1:100) solution of HF-H_2O for 20 s 8. Wash in DI water for 10 min	Oxide layer

In this study, a cleaning step in a solution of sulfuric acid (H_2SO_4) and hydrogen peroxide (H_2O_2) (H_2SO_4:H_2O_2=1:4, SPM) was performed to remove any organic material and metallic impurities. In order to improve the impurity removability, SPM process was repeated twice. The step in a solution of diluted hydrofluoric acid (HF:H_2O=1:100) was performed to remove any oxide which might have been formed on the Si surface.

2.1.3 Rapid thermal annealing (RTA)

The sputtering damage would be removed by annealing process. After setting the sample in RTA, the chamber was pumped out to 10 Pa, and then the vacuum was purged by pure N_2 gas. This process was repeated three times to reduce oxygen concentration. Following the process, the annealing at 400 - 500^{o}C for 10-30 min in nitrogen and forming gas (N_2/4.9%H_2) was performed for reducing the sputtering damage and improving the interface between the insulator and Si substrate. A schematic of the RTA equipment used in this research is shown in Fig. 2-2.

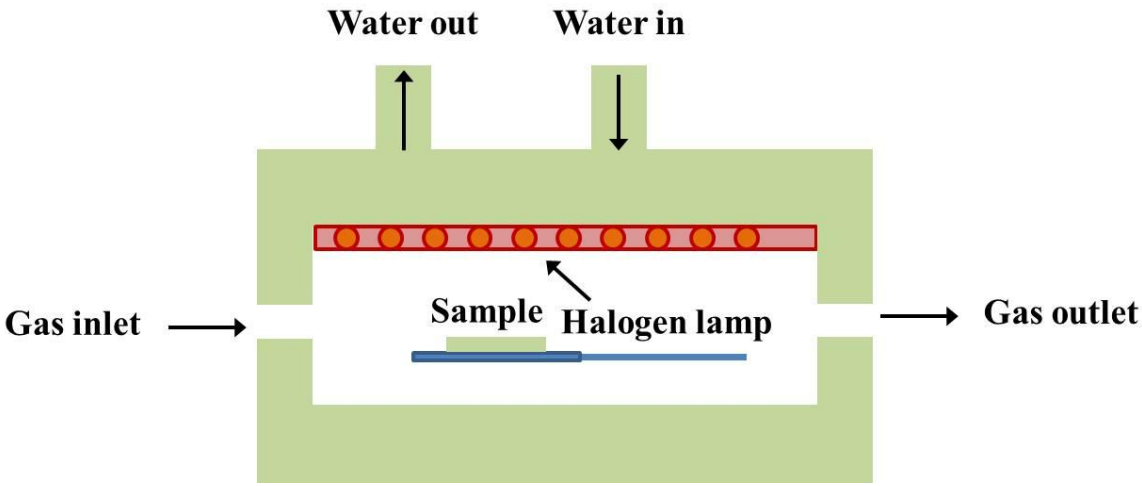


Fig. 2-2 A schematic of RTA system.

2.1.4 Thermal evaporation

The vacuum thermal evaporation deposition technique consists in heating until evaporation of the material to be deposited as shown in Fig. 2-3. The source vapor finally deposits on the cold substrate surface. In this study, Al was used as a top and bottom contact electrodes for a diode and a MISFET, using depostion equipment (VPC-260, ULVAC Co. Ltd.) under the pressure of $1x10^{-5}$ Torr during the depostion.

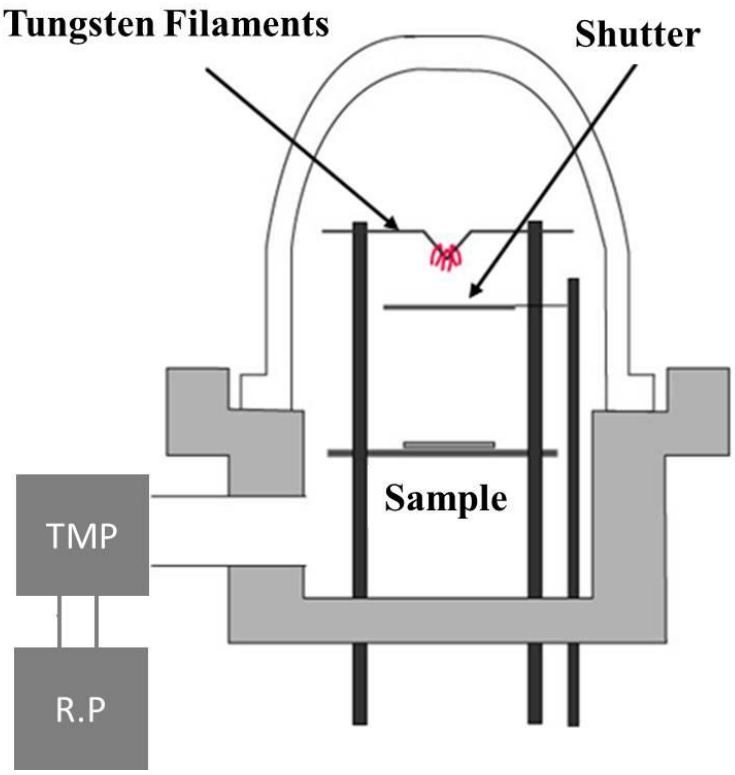


Fig. 2-3 A schmatic of vacuum depostion equipment.

2.1.5 Thermal oxidation

The thermal oxidation process is one of the key steps in the fabrication of silicon devices and integrated circuits. The thermal oxidation of silicon is easily achieved by heating the substrate to a high temperature in an atmosphere containing either pure oxygen or water vapor. Also, wet thermal oxidation generally proceeds with a faster rate than that of dry oxidation. In this study, wet thermal oxide was formed by ultra-clean oxidation system, which includes high pure gases, a specialized water vapor generation tool. And the thermally-grown oxides were used as an isolation field oxide between each MISFET.

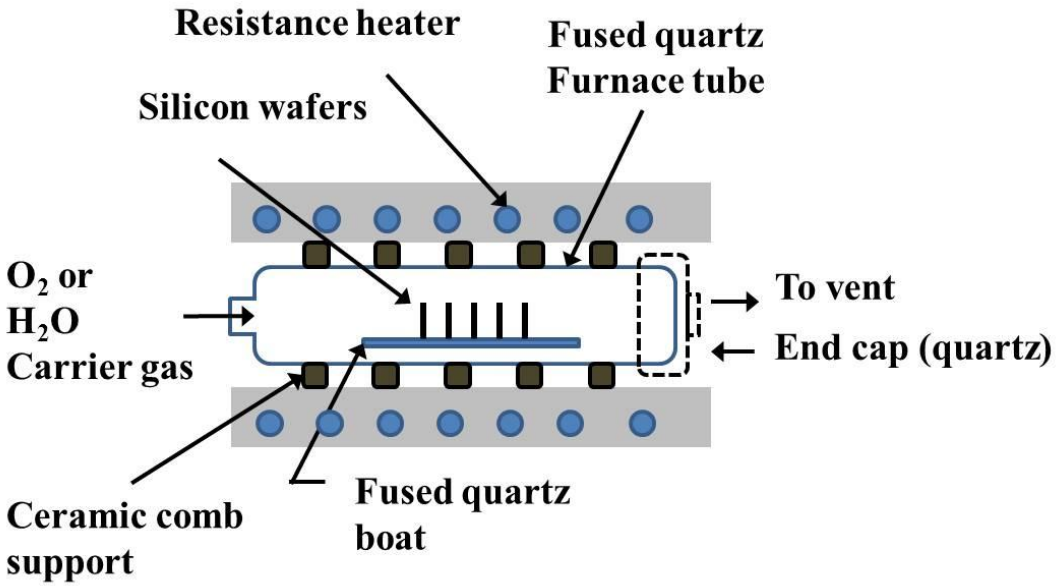


Fig. 2-4 A schmatic of ultra-clean furnace.

2.1.6 Photo lithography

Photolithography is a process used in micro fabrication to selectively remove parts of a thin film or the bulk of a substrate. It uses light to transfer a geometric pattern from a photo mask to a light-sensitive chemical photo resist (PR) on the substrate. A series of chemical treatments then either engraves the exposure pattern into, or enables deposition of a new material in the desired pattern upon, the material underneath the photo resist.

First, PR is formed on substrate by the spin coating method. Then, the PR coated wafer is prebaked at 90 ^{o}C for 20 min. After prebaking, the PR coated wafer is exposed to a pattern of ultra violet light using mask as shown in Fig. 2-5. Some of the PR is removed by a solution called a developer and annealed for 130 ^{o}C for 20 min. Finally, unnecessary part is etched by its only etchant.

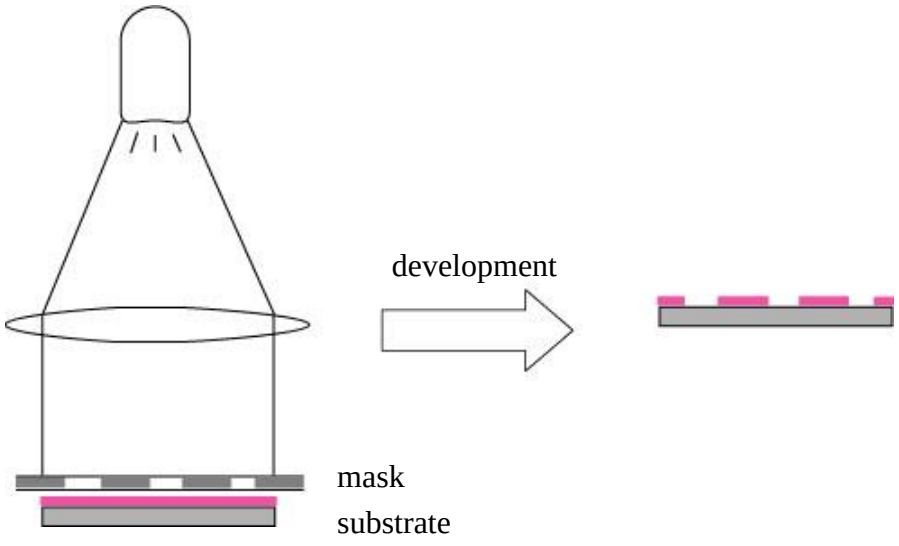


Fig. 2-5 A schmatic of mask aligner.

In order to produce an integrated circuit, thin films of various materials are used as barriers to implantation of impurity atoms, and as insulators between conductive materials and the silicon substrate. Holes or windows are cut through this barrier material wherever impurity penetration or contact is desired. Masks contain the patterns of windows which are transferred to the surface of the silicon substrate using a process called lithography. There are many variations of the lithography process such as photo lithography, e-beam lithography, X-ray lithography and ion-beam lithography. In this study, in order to engrave the desired patterns on silicon substrate in the fabrication processes, only photo lithography was used.

- Substrate preparation : The surface of substrate must be clean and dry to ensure a good adhesion of PR. Prior to application of resist, the substrate cleaning was conducted, since the PR is hydrophobic. Then, a liquid adhesion promoter (OAP, Tokyo Ohka Co. Ltd.) was coated at 500 rpm for 5 s followed by 4000 rpm for 20 s just prior to resist coating.

- PR coating : PR used in this study was OFPR-800 (Tokyo Ohka Co. Ltd.) of positive-type. The substrate was held on a vacuum stage and then spun at high speed for 20 s to produce a thin and uniform layer. PR was coated at 500 rpm for 5 s followed by 5500 rpm for 20 s.

- Pre-baking : A drying step called pre-baking or soft-baking was used to improve adhesion and to remove solvent from the PR. In this study, pre-baking was conducted at a temperature of 90^{o}C for 20 min at an oven.

- Exposure and development : Following mask alignment, the PR is exposed through the mask with ultraviolet light. In this study, the exposure process was performed by contact-type mask aligner. The exposure time was 12 s. The PR was developed using the specified developer (MND-3, Tokyo Ohka Co. Ltd.), stirring for 90 sec.

- Post-baking : Following exposure and development, and additional baking step was performed to harden the PR and improve adhesion to the substrate. The post-baking was conducted at high temperature of 130^{o}C for 20 min at an oven.

- Removal of PR : After patterned windows are etched and ions are implanted, the PR layer must be removed from the surface. Acetone can be used to remove PR which was post-baked at a temperature of 130^{o}C. However, the PR is changed in quality by plasma etching and ion implantation process, and thus PR cannot be removed by the acetone. In this case, O_2 ashing was used to remove the PR.

2.1.7 Induced coupled plasma-Reactive ion etching (ICP-RIE)

In this study, induced coupled plasma-reactive ion etching (ICP-RIE) as a dry etching method is used to fabricate MISFET. Therefore, the origin and principle of ICP and RIE will be explained.

ICP is a type of plasma source in which the energy is supplied by electric currents which are produced by electromagnetic induction, that is, by time-varying magnetic fields [4]. Furthermore, the plasma that is energized by inductively heating the gas with an electrical coil, and contains a sufficient concentration of ions and electrons to make the gas electrically conductive. This etching system would produce high density plasmas which can be used to etch all kinds of silicon-based materials such as silicon, silicon dioxide, and silicon nitride.

The plasma is contained inside a chamber which is surrounded by an inductive coil. An alternating magnetic field is induced by the RF coils located in front of the RF transducer, and this helps to produce high-density plasma due to confinement of electrons. On the sample stage, RF source or DC bias can be added to achieve deep etching.

In this study, to etch SiN, the ICP-RIE was used. Furthermore, after implantation, to remove the residue, the O_2 ashing was also performed. The conditions are shown in table 2-2 and 2-3.

Table 2-2 SiN removing condition.

CF_4/O_2 flow rate [sccm]	Antenna/Bias RF[W]	Pressure [Pa]	He pressure [Pa]	Cooler temperature [°C]
90/10	200/40	0.6	400	-15

Table 2-3 O_2 ashing condition.

CF_4/O_2 flow rate [sccm]	Antenna/Bias RF[W]	Pressure [Pa]	He pressure [Pa]	Cooler temperature [°C]
40	400/0	11.5	200	23

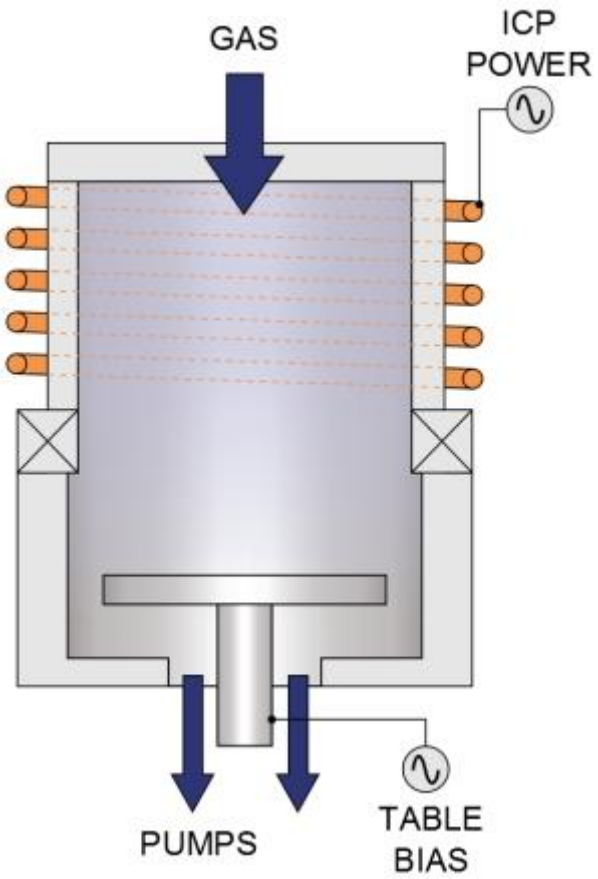


Fig. 2-6 A schmatic of ICP-RIE.

2.1.8 Ion implantation

Since ion implantation offers many advantages over diffusion for the introduction of impurity atoms into Si, it has been a very important technology in modern integrated-circuit fabrications. An ion implantation apparatus is a high-voltage particle accelerator producing a high-velocity beam of impurity ions which can penetrate the surface of silicon wafers. The basic parts of the system are schematically illustrated in Fig. 2-7.

- Ion source : The ion source operates at a high-voltage and produces a plasma containing the desired impurity as well as undesired species. This technique offers a wide range of flexibility in the choice of impurity. In this study, BF_3 and PH_3 were used to implant Boron as a channel stopper and Phosphorous as a channel, respectively.

- Mass spectrometer : An analyzer magnet bends the ion beam through a right angle to select the desired impurity ion. The selected ion passes into the main accelerator column.

- High-voltage accelerator : The accelerator column adds energy to the beam and accelerates the ions to their final velocity. For protection from high-voltage and possible X-ray emission, the ion source and accelerator are mounted within a protective shield.

- Scanning system : X- and y-axis deflection plates are used to scan the beam across the substrate to give uniform implantation and to build up the desired dose. The beam is

bent slightly to prevent neutral particles from hitting the target.

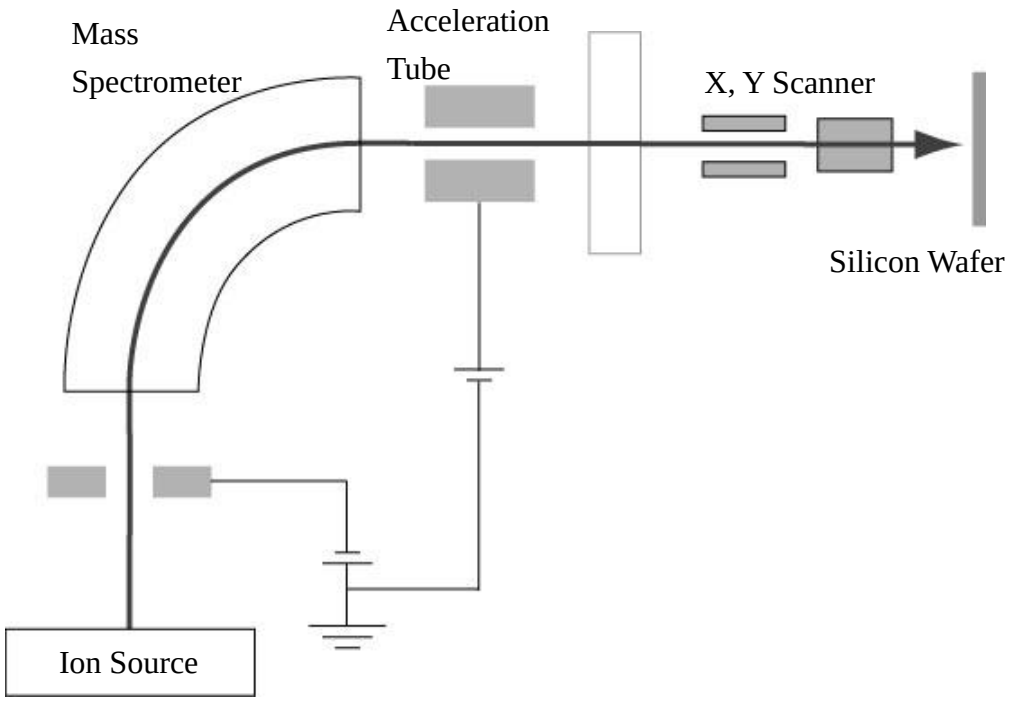


Fig. 2-7 A schmatic of ion implantation system.

2.2 Characterization methods

The fabricated devices are characterized by various methods. In this section, details of characterization methods are summarized.

2.2.1 Capacitance-Voltage (C-V) method

To measure the C-V characteristics of fabricated MIS diode, Agilent Technology 4280A precision system was used with the varied measurement frequency from 10 kHz to 1 MHz. C-V measurement is a technique for characterizing semiconductor materials and devices. The applied voltage is varied, and the capacitance is measured and plotted as a function of voltage. The technique uses a metal-semiconductor junction or a p-n junction or a MOSFET to create a depletion region, which is empty of conducting electrons and holes, but may contain ionized donors and electrically active defects or traps. The depletion region with its ionized charges inside behaves like a capacitor. By varying the voltage applied to the junction, it is possible to vary the depletion width. The dependence of the depletion width upon the applied voltage provides information on the semiconductor's internal characteristics, such as its doping profile and electrically active defect densities. Measurements were carried out at DC, or using both DC and a small-signal AC signal or using a large-signal transient voltage. C-V measurements can reveal oxide thickness, oxide charges, contamination from mobile ions, and density of interface state in wafer processes. These measurements are important for the device after other process steps including lithography, etching, cleaning, dielectric and poly-silicon depositions, and metallization. Once devices have been fully fabricated, C-V profiling is often used to characterize threshold voltages, flat-band voltage, hysteresis and other parameters during reliability and basic device

testing and to model device performance.

- Equivalent oxide thickness (EOT) : An Equivalent oxide thickness is a distance, usually given in nanometers (nm), which indicates how thick a silicon oxide film would need to be to produce the same effect as the high-k material being used. As the thickness approached 3 nm, leakage becomes a problem and alternate materials were necessary to increase the thickness while retaining the switching speed. Materials having larger dielectric constants enable thicker films to be used for this purpose while retaining fast reaction of the transistor. For example, a high-k material with dielectric constant of 39 (compared to 3.9 for silicon oxide) can be made ten times thicker than silicon oxide which helps to reduce the leakage of electrons across the dielectric pad.

$$EOT = t_{high-k}\left(\frac{k_{SiO_2}}{k_{high-k}}\right) \tag{2.1}$$

As shown in Eq. 2.1, when we know the thickness and dielectric constant of high-k layer, the EOT is obtained.

- Flat-band voltage (V_{FB}) : In solid-state physics, the work function is the minimum energy needed to remove an electron from a solid to a point outside the solid surface. For a metal, the Fermi level is inside the conduction band, indicating that the band is partly filled. For a semiconductor or an insulator, the Fermi level lies within the band gap, indicating an empty conduction band; in this case, the minimum energy to remove an electron is about the sum of half the band gap and the electron affinity. In MIS diode, the band is flat when we apply voltage. At this point, the gap between the work

functions of metal and semiconductor is called flat-band voltage as shown in Eq. 2.2.

$$V_{FB} = \phi_m - \phi_s \quad (2.2)$$

2.2.2 Current density-Voltage (J-V) method

Current density-Voltage (J-V) of MIS diode is measured using an Agilent 4156C precision semiconductor parameter analyzer. In an ideal MIS diode, the conductance of the insulating film is assumed to be zero. However, real insulators show some degree of carrier conduction when the electric field or temperature is sufficiently high. Table 2-4 summarized the basic conduction processes in insulators. It also emphasized the voltage and temperature dependence of each process that is used often to identify the exact conduction mechanism experimentally.

- Tunneling : Tunneling is the most-common conduction mechanism through insulators under high fields. The tunnel emission is a result of quantum mechanics by which the electron wave function can penetrate through a potential barrier.

- Poole-Frenkel (PF) emission : The PF emission is due to emission of trapped electrons into the conduction band. The supply of electrons from the traps is through thermal excitation. At low voltage and high temperature, current is carried by thermally excited electrons hopping from one isolated state to the next.

- Fowler-Nordheim (FN) tunneling : FN tunneling is similar to the tunneling. However, in case of FN tunneling, the carriers tunnel through only a partial width of the

barrier.

- Schottky emission : The schottky emission process is similar to the process which thermionic emission over the metal-insulator barrier or the insulator-semiconductor barrier is responsible for carrier transport.

Table 2-4 Basic conduction processes in insulators.

Process	Expression	Voltage & temperature dependence
Schottky emission	$J = A^{*}T^{2}\exp\left[\frac{-q\left(\phi_B - \sqrt{qE/4\pi\varepsilon_i}\right)}{kT}\right]$	$\sim T^{2}\exp\left(a\frac{\sqrt{V}}{T}\right)$
PF emission	$J_{PF} \sim E\exp\left[\frac{-q\left(\phi_B - \sqrt{qE/\pi\varepsilon_i}\right)}{kT}\right]$	$\sim V\exp\left(2a\frac{\sqrt{V}}{T}\right)$
FN tunneling	$J_{FN} \sim E^{2}\exp\left[\frac{4\sqrt{2m^{*}}(q\phi_B)^{3/2}}{3q\hbar E}\right]$	$\sim V^{2}\exp\left(-\frac{b}{V}\right)$
Tunneling	$J_{DT} = \frac{A}{t_{OX}^{2}}\exp\left(-2t_{OX}\sqrt{\frac{2m^{*}q}{\hbar^{2}}\Phi_B - \frac{V_{ox}}{2}}\right)$	

2.2.3 Scanning electron microscopy (SEM)

Scanning electron microscopy (SEM) form the most widely used surface characterization methods [5]. SEM uses electrons instead of light to image a sample. The electrons are generated by thermionic emission from a metal filament, and accelerated to ~25 keV. A system of electrical and magnetic field optics is used to focus the beam to a spot ~10 nm in diameter on the sample surface. A schematic of a typical scanning electron microscope is shown in Fig. 2-8.

The sample surface must be electrically conducting, otherwise the electron beam would charge up the surface. As diamond is an insulating material, the sample is given a thin (~10 nm) Au coating by glow discharge sputtering before SEM examination. SEM must be carried out under a high vacuum. The electron beam is scanned across the sample via magnetic scan coils. The current of electrons reflected from the surface is collected, amplified, and plotted as a two-dimensional 'micrograph' image of the signal intensity. Features down to the spot size (~10 nm) may be resolved. As such, SEM can only give information on the appearance, or morphology, of the sample surface, and not definitive proof that the surface is (for example) diamond. By mounting the sample so it is viewed edge on its thickness can be measured. In the present work, this allows us to determine the growth rate of the diamond film, as we know the amount of time for which growth was carried out for.

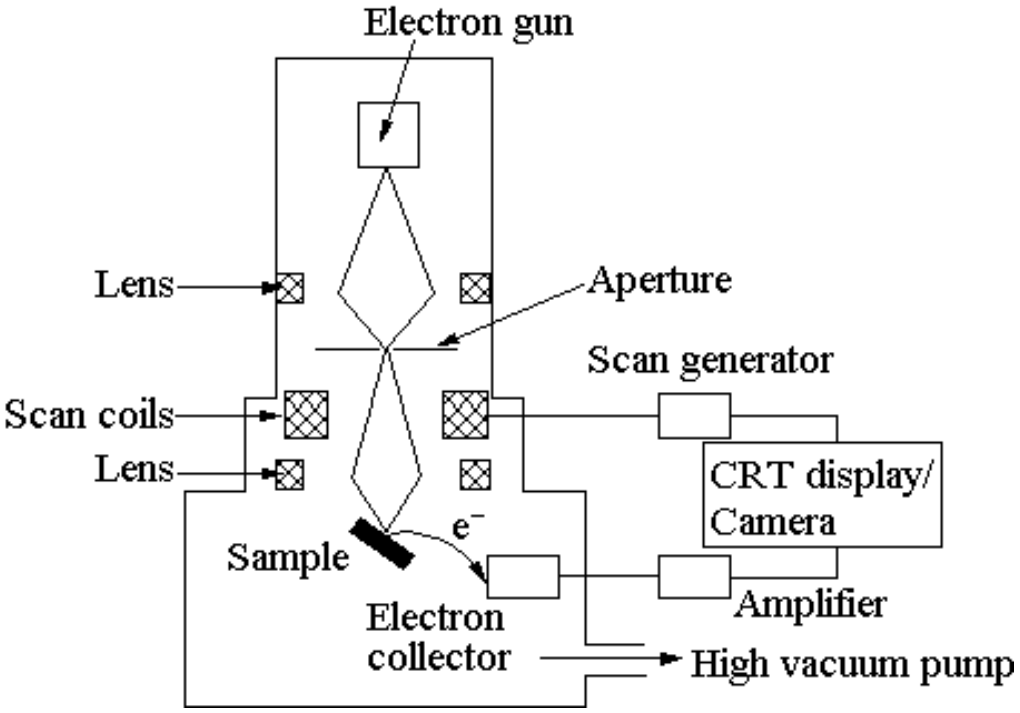


Fig. 2-8 A schematic of SEM.

2.2.4 Transmission electron microscopy (TEM)

Transmission electron microscopy (TEM) is a microscopy technique whereby a beam of electrons is transmitted through an ultra thin specimen, interacting with the specimen as it passes through. An image is formed from the interaction of the electrons transmitted through the specimen; the image is magnified and focused onto an imaging device. TEM is capable of imaging at a significantly higher resolution than light microscopes, owing to the small de Broglie wavelength of electrons. This enables the instrument's user to examine fine detail, even as small as a single column of atoms, which is tens of thousands times smaller than the smallest resolvable object in a light microscope.

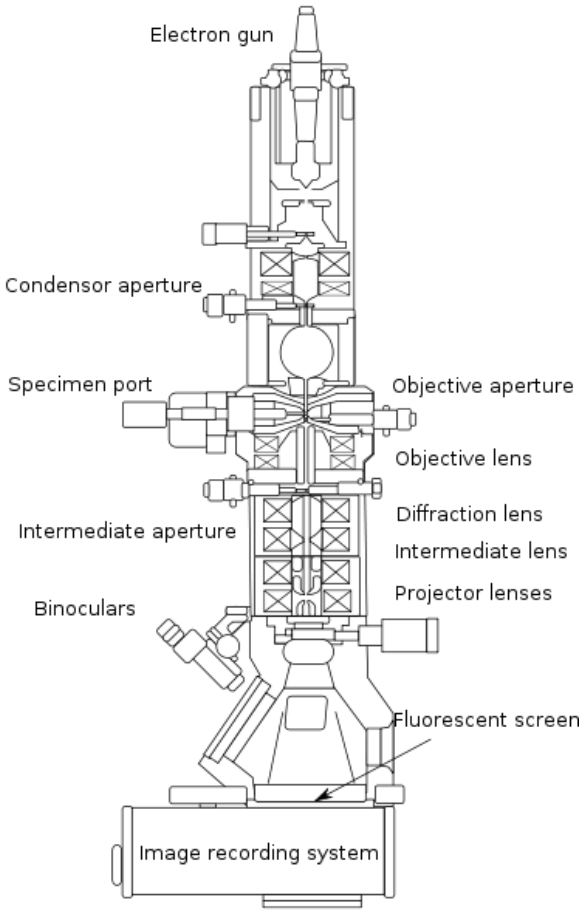


Fig. 2-9 A schematic of TEM.

2.2.5 X-ray photoelectron spectroscopy (XPS)

X-ray photoelectron spectroscopy (XPS) is a technique used to investigate the composition of deposited films by ionizing surface atoms and measuring the energy of ejected photoelectrons. The method requires the sample of interest to be bombarded with low energy X-rays, produced from an aluminum or magnesium source, with energy of hv. These X-rays cause electrons to be ejected from either a valence or inner core electron shell. The energy of the electron, E, is given by $E = hv - E_1 - \Phi$, where E_1 is the binding energy of the atom and Φ is the work function of the sample. Thus, it is possible to calculate the binding energy of the ejected electron, and therefore identify the atom (and its chemical state) from which the electron originates. In order to prevent surface contamination, analysis is carried out under ultra high vacuum ($< 10^{-10}$ Torr). As shown in Fig. 2-10, X-rays are directed onto the sample and the resulting photoelectrons are then focused onto the entrance slit of a concentric hemispherical analyzer. Here a negative and positive potential are applied to the outer and inner cylinders, respectively, such that the central line between the cylinders is a line of zero potential. Scanning the potentials allows control of the energy of electrons that are allowed to pass through the analyzer and onto the detector, usually a channel electron multiplier.

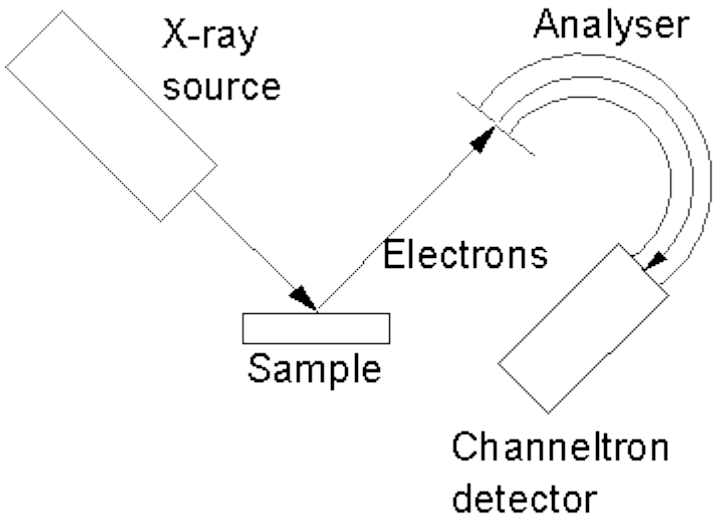


Fig. 2-10 A schematic of XPS.

2.2.6 Atomic force microscopy (AFM)

The surface morphology of HfN film was observed by Atomic force microscopy (AFM, Digital Instrument NanoScope IIIa) as shown in Fig. 2-11. The basic principle and explanation of AFM is as follows.

The AFM consists of a cantilever with a sharp tip (probe) at its end that is used to scan the specimen surface. The cantilever is typically silicon or silicon nitride with a tip radius of curvature on the order of nanometers. When the tip is brought into proximity of a sample surface, forces between the tip and the sample in AFM measurements include mechanical contact force, van der waals forces, capillary forces, chemical bonding, electrostatic forces, magnetic forces, Casimir forces, solvation forces, etc. Typically, the deflection is measured using a laser spot reflected from the top surface of the cantilever into an array of photodiodes. Other methods that are used include optical interferometer, capacitive sensing or piezoresistive AFM cantilevers. These cantilevers are fabricated with piezoresistive elements that act as a strain gauge. If the tip was scanned at a constant height, a risk would exist that the tip collides with the surface, causing damage. Hence, in most cases a feedback mechanism is employed to adjust the tip-to-sample distance to maintain a constant force between the tip and the sample. Traditionally, the sample is mounted on a piezoelectric tube that can move the sample in the z direction to maintain a constant force, and the x and y direction for scanning the sample. Alternatively a ‘tripod’ configuration of three piezo crystals maybe employed, with each responsible for scanning in the x, y, and z directions. This eliminates some of the distortion effects seen with a tube scanner.

The AFM would be operated in a number of modes, depending on the application. In general, possible imaging modes are divided into static (also called contact) modes

and a variety of dynamic (or non-contact) modes where the cantilever is vibrated. In this study, a non-contact mode was used to investigate the morphology characteristics.

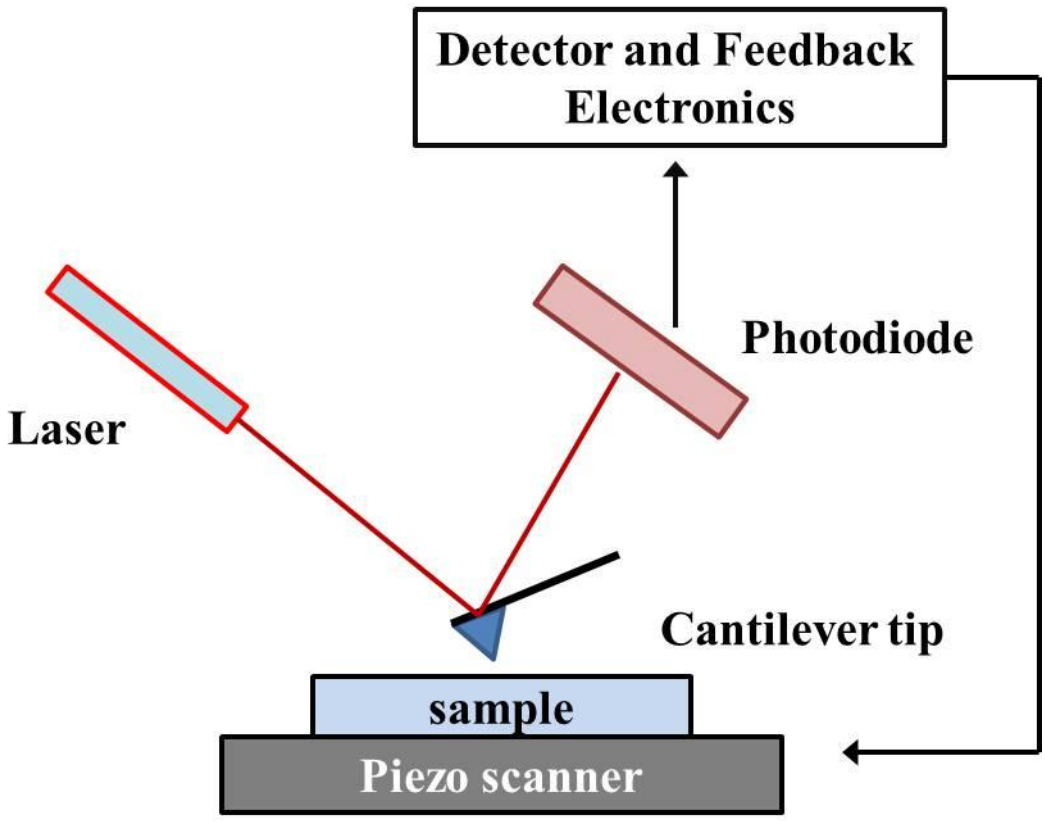


Fig. 2-11 A schematic of AFM.

2.2.7 Ellipsometer

Figure 2-12 shows a schematic of ellipsometer. Upon the analysis of the change of polarization of light, which is reflected off a sample, ellipsometry yields information about layers that are thinner than the wavelength of the probing light itself, even down to a single atomic layer. Ellipsometry probes the complex refractive index or dielectric function tensor, which gives access to fundamental physical parameters and is related to a variety of sample properties, including morphology, crystal quality, chemical composition, or electrical conductivity. It is commonly used to characterize film thickness for single layers or complex multilayer stacks ranging from a few angstroms or tenths of a nanometer to several micrometers with an excellent accuracy. In this study, to evaluate the thickness of HfN film, the ellipsometer was used. The details are shown in appendix C.

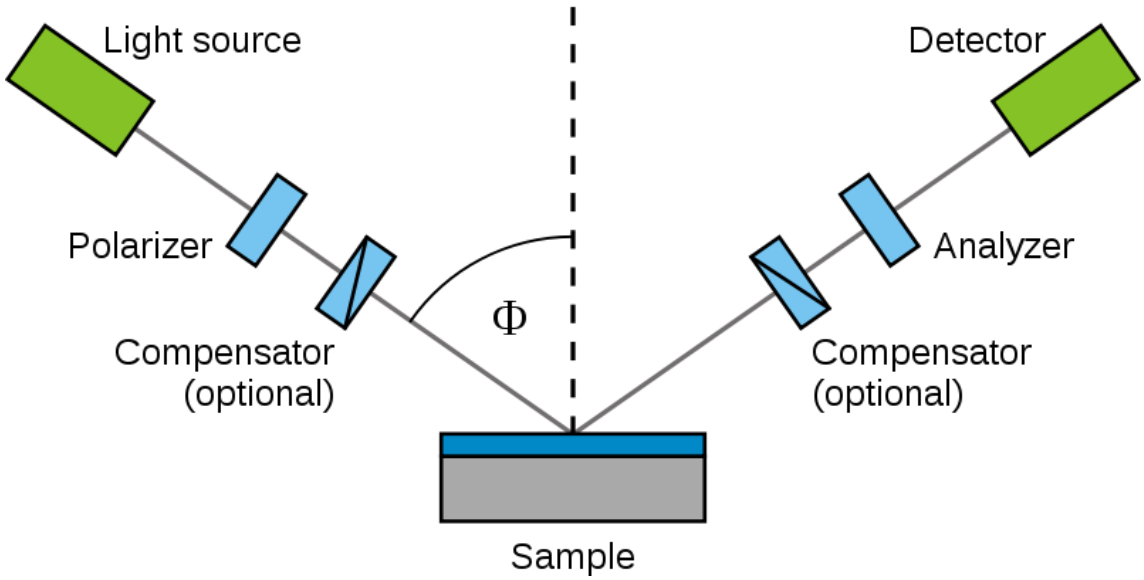


Fig. 2-12 A schematic of ellipsometer.

References

[1] T. Amazawa, T. Ono, M. Shimada, and S. Matsuo, "Ultrathin oxide films deposited using electron cyclotron resonance sputter ", *J. Vac. Sci. Technol. B*, vol. 17, pp. 2222-2225, 1999.

[2] T. Ono, H. Nishimura, M. Shimada, and S. Matsuo, “Electron cyclotron resonance plasma source for conductive film deposition”, *J. Vac. Sci. Technol. A*, vol. 12, pp. 1281-1286, 1994.

[3] T. Ohmi, “Ultra-Clean ULSI Technology”, Advanced Electronic Series, Baifukan, Japan, 1995. (in Japanese)

[4] A. Montaser and D. W. Golightly, Inductively Coupled Plasmas in Analytical Atomic Spectrometry, VCH Publishers, Inc., New York, 1992.

[5] P. E. J. Flewitt and R. K. Wild, Physical Methods for Materials Characterization, Chapter 6, IOP Publishers, Bristol, 1994.

Chapter 3

Formation and evaluation of HfN gate insulator formed by ECR plasma sputtering

In this chapter, the fabrication of hafnium nitride gate dielectric based devices and their basic principles are discussed. Especially, in order to obtain the insulating properties of hafnium nitride film, the conditions should be optimized. Furthermore, in order to improve the characteristics of hafnium nitride gate insulator, hydrogen annealing is investigated.

3.1 Introduction

As mentioned in chapter 1, the hafnium nitride gate insulator is investigated by ECR plasma sputtering method in this chapter. First, to obtain insulating property for HfN film, we deposited HfN film with various Ar/N_2 flow ratio to optimize the deposition condition. And then, the electrical characteristics were evaluated.

In section 3.2, the formation of HfN film on p-Si(100) will be studied with various Ar/N_2 flow ratio. Then, the effect of hydrogen annealing for HfN gate insulator will be studied in section 3.3, including nitrogen annealing. Finally, the dependence of pre-sputtering condition will be studied to improve the electrical characteristics in section 3.4.

3.2 Formation of HfN gate insulator

In this section, the formation of HfN film on p-Si(100) will be studied with various Ar/N_2 flow ratio. The electrical characteristics are investigated by fabrication of the MIS diode with HfN gate insulator. The MIS diodes were fabricated using a conventional top gate structure on p-Si(100) substrate.

3.2.1 Fabrication process

In this experiment, MIS diodes with HfN gate insulator were fabricated on the p-type Si(100) as shown in Fig. 3-1. The p-Si(100) substrate was chemically cleaned using SPM and DHF for two times. Then, HfN films were deposited by ECR plasma sputtering with a hafnium target at sputtering gas pressure of 0.19 Pa at room temperature. At that time, Ar/N_2 flow ratio was changed from 20% to 28% to obtain optimization condition. The resistivity of HfN thin films is changed by the N_2 flow ratio [1]. Therefore, we chose the N_2 ratio over 20% to obtain amorphous thin film with dielectric property. Before the deposition, the Ar/N_2 pre-sputtering was carried out for 10 min. Finally, Al electrodes were deposited by evaporation.

The fabricated Al/HfN/p-Si(100) MIS diodes were characterized by capacitance-voltage (C-V) and current-voltage (J-V) using the Agilent 4284A and Agilent 4156C, respectively.

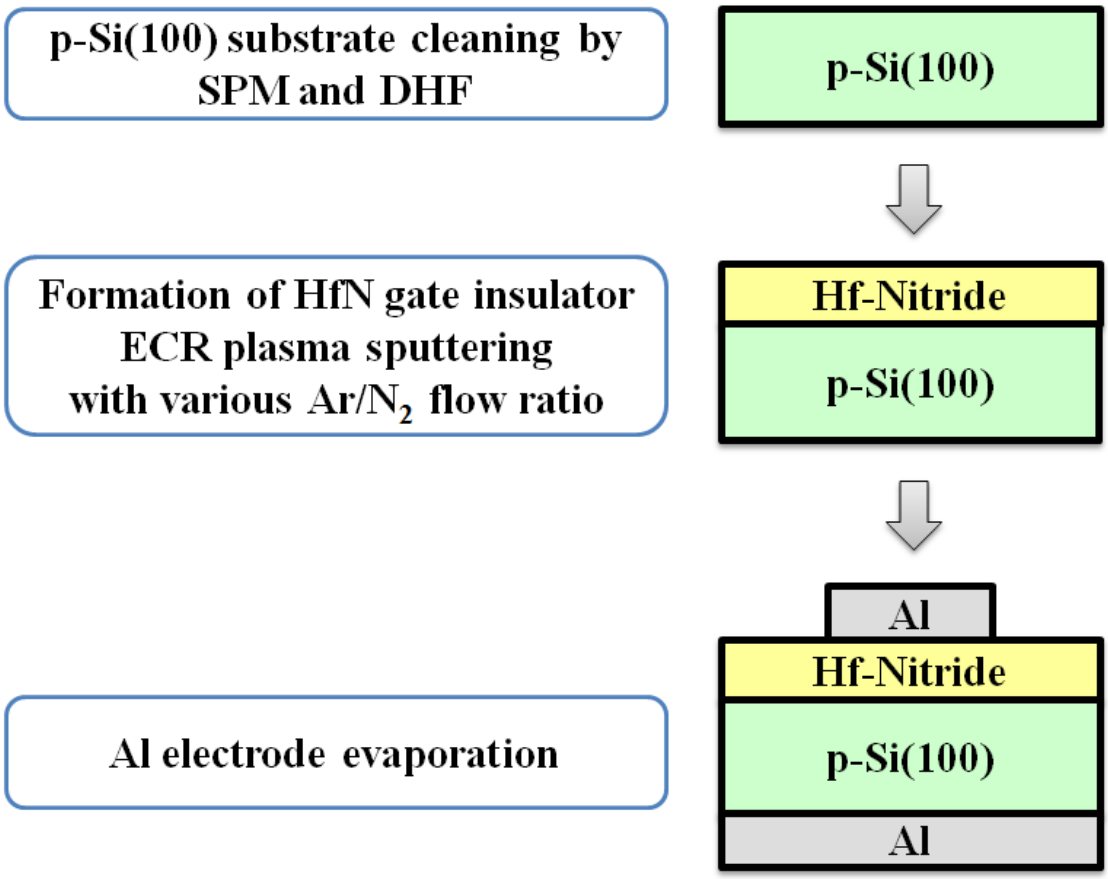


Fig. 3-1 Schematics of fabrication process for MIS diode with HfN gate insulator.

3.2.2 Formation of HfN gate insulator

Figure 3-2 shows the C-V and J-V characteristics for the fabricated MIS diodes with various Ar/N_2 flow ratio. The Ar/N_2 flow ratio was changed from 20% to 28%. At that time, the sputtering gas pressure was same as 0.19 Pa. First, as shown in Fig. 3-2(a), the capacitance was increased as the N_2 flow ratio was increased at 100 kHz. Furthermore, it was found that the V_{FB} shift was also reduced as the N_2 flow ratio was increased. Figure 3-2(b) shows J-V characteristics with various Ar/N_2 flow ratio. As before, the leakage current density was low enough at $N_2/(Ar+N_2)$ = 28%. We can guess that when the N_2 flow ratio was changed, the Hf/N ratio was also changed. Nitrogen ratio for Hf in the HfN film is a factor to change insulating property. Therefore, it was found that when the N_2 flow ratio was increased, the electrical properties were improved. We also investigated over $N_2/(Ar+N_2)$ = 28%. The result shows in Fig. 3-3(a). In this case, when the HfN film was deposited by ECR plasma sputtering, the plasma became unstable due to the limitation of machine. In Fig. 3-3(b), Hf 4f XPS spectra with different gas flow ratio was shown. The take-off angle was 80^o. Under $N_2/(Ar+N_2)$ = 28%, the spectra of Hf 4f show a doublet shape due to spin-orbital splitting into the Hf $4f_{5/2}$ and Hf $4f_{7/2}$. And the doublet shape was shifted as the gas flow ratio was increased. It means that the Hf-N bonds were increased. However, the doublet shape was shifted back at $N_2/(Ar+N_2)$ = 40%. The Hf-N bonds should be decreased due to the instability of plasma.

From these C-V and J-V characteristics, we chose the deposition condition as Ar/N_2 = 20/8 sccm.

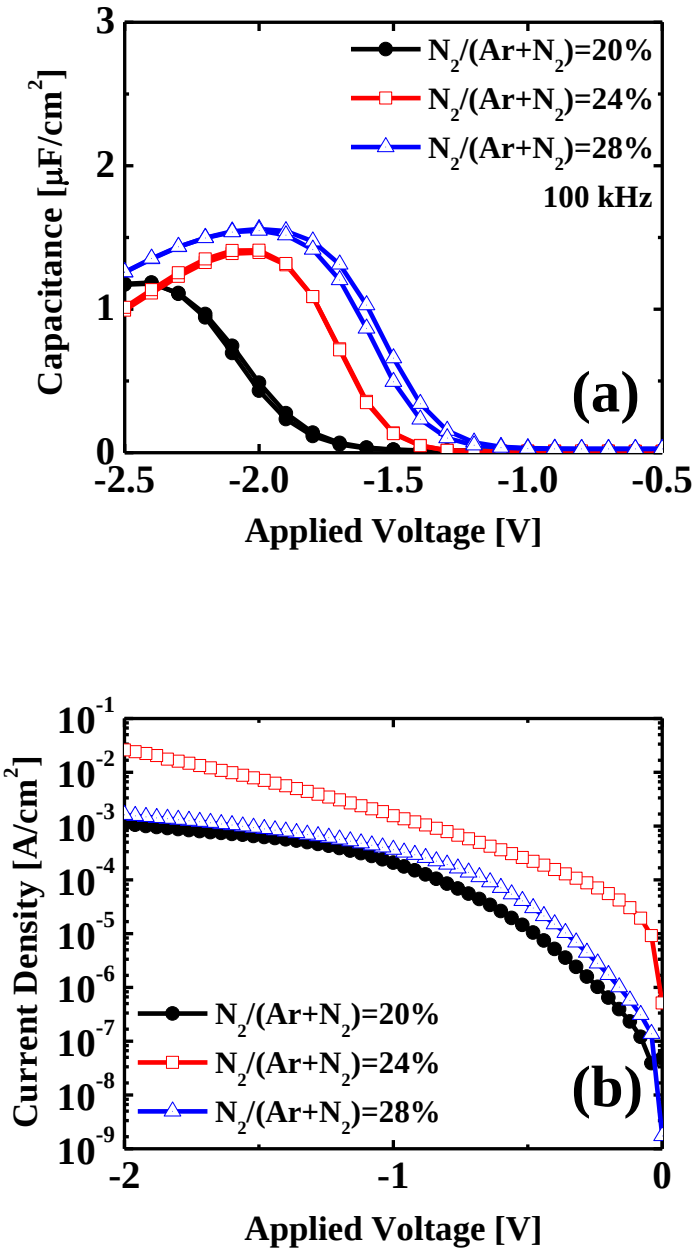


Fig. 3-2 (a) C-V and (b) J-V characteristics of the fabricated MIS diodes with various Ar/N_2 flow ratio.

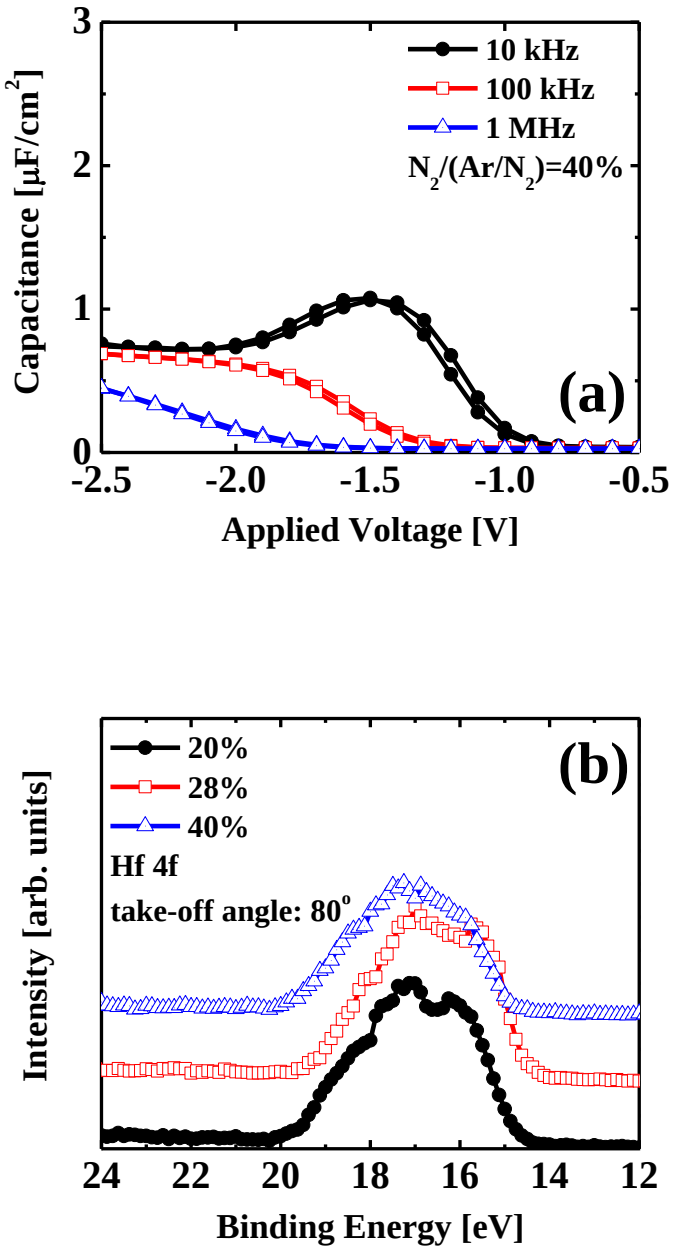


Fig. 3-3 (a) C-V characteristics of the fabricated MIS diodes at $N_2/(Ar+N_2)$ = 40% and (b) Hf 4f XPS spectra with different gas flow ratio (take-off angle: 80^o).

3.3 Effect of hydrogen annealing for HfN gate insulator

The effect of hydrogen annealing for HfN gate insulator will be studied in this section, including nitrogen annealing. First, we explain about hydrogen annealing effect. And then, the electrical characteristics are investigated by fabrication of the MIS diode with hydrogen and nitrogen annealing for the HfN gate insulator.

3.3.1 Effect of hydrogen annealing

In consideration of this study, there are two points for selecting insulator. First it is necessary to suppress interfacial layer formation. Second one is high-k nitride insulator to overcome a problem which is an oxygen vacancy. For such a reason, we focused on high-k nitride insulator such as SiN or AlN [2, 3]. For SiN gate dielectrics, numerous attempts have been reported, however, nitride/Si interface properties as well as high densities of bulk traps still are the issue to introduce in scaled CMOS [4]. To overcome this problem, X. Wang et al. reported that a modest anneal treatment in a steam furnace yields remarkable improvement of transconductance as well as its current drivability for devices containing nitrided while preserving their excellent reliability. They investigated the effect of anneal either in forming gas (FG, $N_2/5\%H_2$) or water vapor at 400^{o}C for 30 min. The water vapor anneal treatment has been demonstrated to improve the properties and reliability of nitride/Si interface, while it does not have any noticeable effect on thermal oxide [5, 6].

According to the mechanism proposed by Balk, the active (nascent or atomic) hydrogen diffuses through pores and reaches the Si-insulator interface and reacts as to

$$\equiv \mathrm{Si}\cdot + \mathrm{H} \rightarrow \equiv \mathrm{Si} - \mathrm{H} \qquad (3.1)$$

form a silane bond. It is further suggested that, even when the oxide is dense but deficient in oxygen, hydrogen will diffuse via single ionized oxygen vacancies as ionic hydrogen, H^+. The observed reduction of the interface in molecular hydrogen would therefore be dependent upon the ratio between H and H_2 and/or between H^+ and H_2 at 500°C. This in turn will depend upon the corresponding equilibrium dissociations constants [7].

3.3.2 Fabrication process

In this experiment, MIS diodes with HfN gate insulator were fabricated on the p-type Si(100) as shown in Fig. 3-4. p-Si(100) substrate was cleaned by sulfuric-peroxide mixture (SPM) and dilute-hydrofluoric (DHF). Then, HfN film was deposited by ECR plasma sputtering with a hafnium target at sputtering gas pressure of 0.19 Pa (Ar/N_2 : 20/8 sccm) at room temperature. The back pressure of the chamber was 1×10^{-4} Pa. Before the deposition, the Ar/N_2 pre-sputtering was carried out for 10 min. The post deposition anneal (PDA) was carried out at 400 - 500^{o}C for 10 min in FG (N_2/4.9%H_2) and nitrogen ambient utilizing rapid thermal anneal (RTA) system (ULVAC MILA-3000). The flow rate of gases was approximately 1 SLM. Finally, Al electrodes were deposited by evaporation. The fabricated Al/HfN/p-Si(100) MIS diodes were characterized by C-V, J-V, and Transmission electron microscopy (TEM). The EOTs were evaluated using exponential potential based quantum mechanical extraction (EPOQUE) method [8].

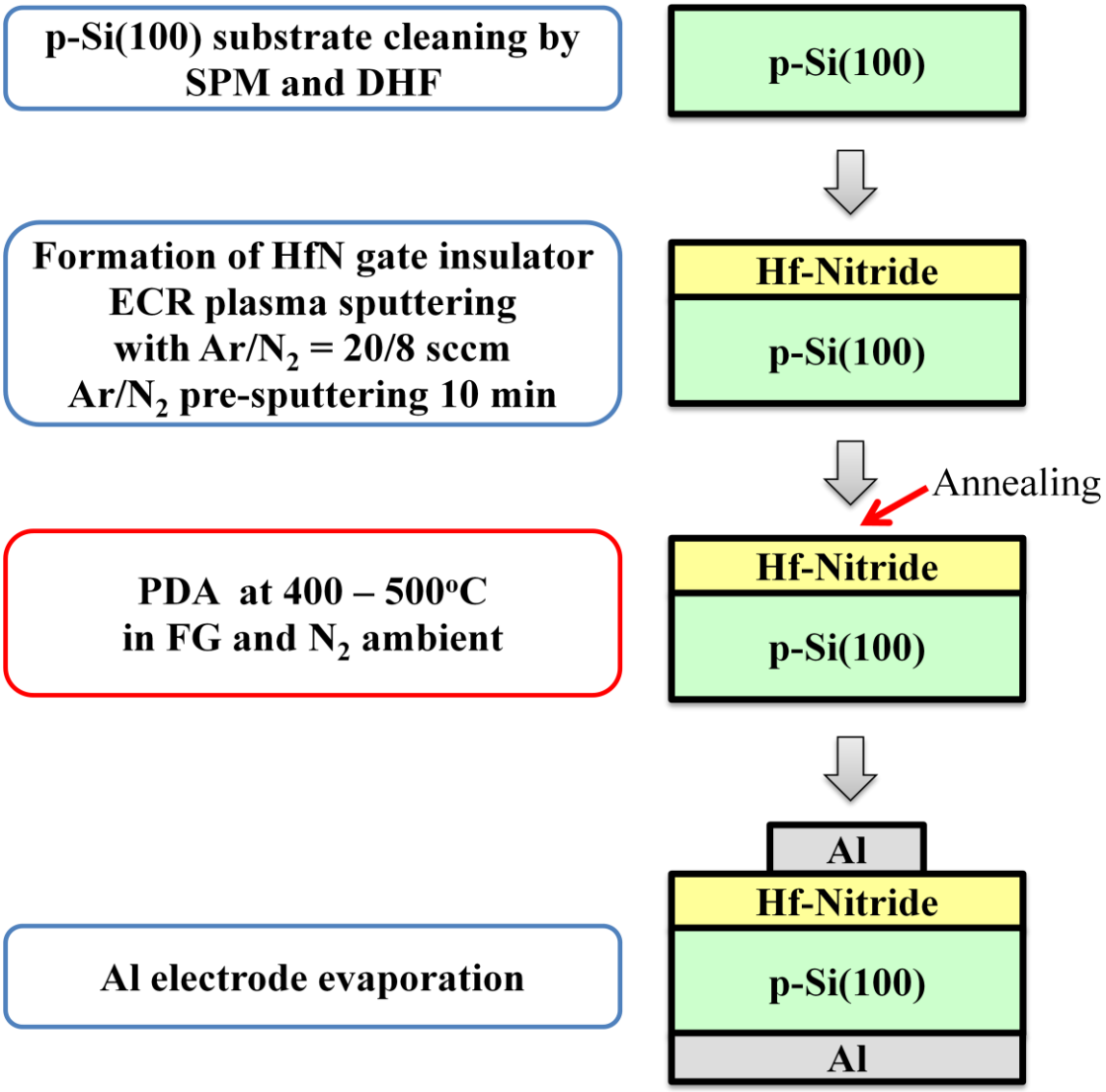


Fig. 3-4 Schematics of fabrication process for MIS diode with annealing.

3.3.3 Comparison of annealing ambient for HfN gate insulator

First, the PDA in nitrogen ambient was carried out to improve the electrical characteristics for the HfN gate insulator. The C-V and J-V characteristics were shown in Fig. 3-5. As shown in Fig. 3-5(a), the capacitance was remarkably reduced compared by the as-deposited sample. The hump was found as well. Furthermore, the frequency dispersion was observed in the C-V curves. In Fig. 3-5(b), it was found that the J-V characteristic was not improved by N_2 annealing. When depositing the HfN film on Si, the sputtering system was used. It means that the sputtering damage should be considered at the interface during the deposition of the film. Therefore, to improve the interface characteristic, the PDA in N_2 ambient was performed. However, there is no improvement by N_2 annealing.

We considered that the interface characteristic is an important factor to improve the electrical characteristics. Therefore, the FGA was introduced to improve the interface characteristic. F.H.P.M. Habraken and P. Balk et al. reported that the active hydrogen diffuses through pores and reaches the Si-SiN interface and reacts as Si-H to form a silane bond [9, 10]. B. Swaroop further suggested that the effect of hydrogen was observed for the SiN-Si interface annealed in atomic hydrogen, which reduced the D_{it} [7]. Because the nitrogen-hydrogen gas mixture was used for anneal, the formation of Si-N-H bonding (or hydrogen passivation) would reduce the chance to generate interface states, which led to improve the electrical characteristics [11]. The FGA was performed at 400 - 500^{o}C for 10 min. At that time, the deposition condition was kept as Ar/N_2 = 20/8 sccm. As shown in Fig. 3-6, the capacitances were remarkably improved by FGA at 400 - 500^{o}C. Furthermore, the hump was also disappeared. As mentioned above, the FGA leads to improvement of interface properties. The

hydrogen reaches the Si-HfN interface and reacts as Si-H. Therefore, it was found that the hydrogen leads to improvement of electrical properties of the HfN gate insulator.

The film thicknesses were determined by the cross-sectional TEM. The cross-sectional TEM images of the as-deposited film and 400^{o}C FGA film for the HfN/p-Si(100) structures were shown in Fig. 3-7. In Fig. 3-7(a), we confirmed no interfacial layer for the as-deposited sample. However, after 400^{o}C FGA, the interfacial layer was slightly formed, as shown in Fig. 3-7(b). Physical thickness of the film after 400^{o}C FGA was slightly increased to 4.1 nm compared to the as-deposited film (3.6 nm). Furthermore, it was found that the interfacial layer was formed after FGA. This is probably because of the oxidation during the FGA process by the residual oxygen in the FGA ambient. From the TEM images, the relative dielectric constant for 400^{o}C FGA sample was obtained as 15.1. However, the reported value of the relative dielectric constant for HfN film is about 30. The obtained value of the relative dielectric constant is insufficiency. Therefore, there is a chance to improve the electrical characteristic more.

We compared the J-V characteristics for the as-deposited and FGA film. Figure 3-8(a) shows the FGA temperature dependence of J-V characteristics. The leakage current was decreased by FGA. Figure 3-8(b) summarized the leakage the current densities versus EOTs. After the FGA, the leakage current density at V_{FB}-1 V was decreased approximately one order of magnitude, and 2.2 x 10^{-4} A/cm^{2} was obtained for the 400^{o}C FGA sample.

Finally, deposition time dependence of electrical properties was investigated. After decreasing the deposition time to 40 s, the EOT was not deceased as shown in Fig. 3-9. When the film thickness was deceased, the influence of interfacial layer was grown.

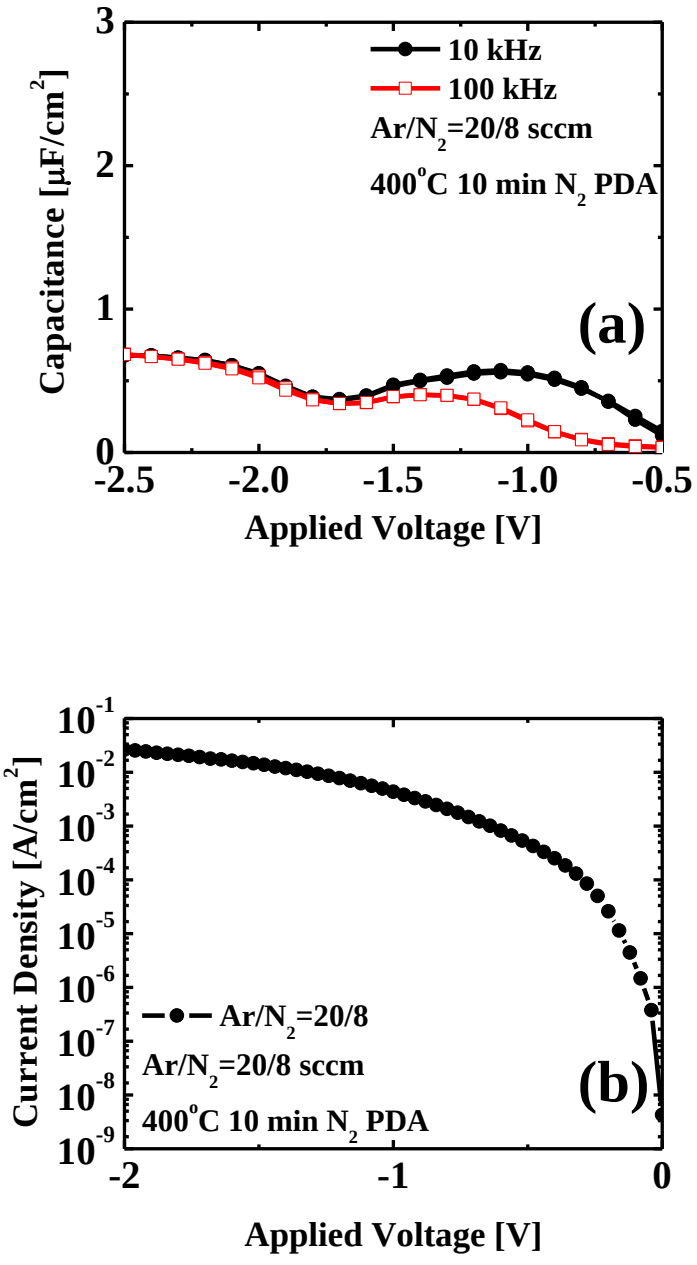
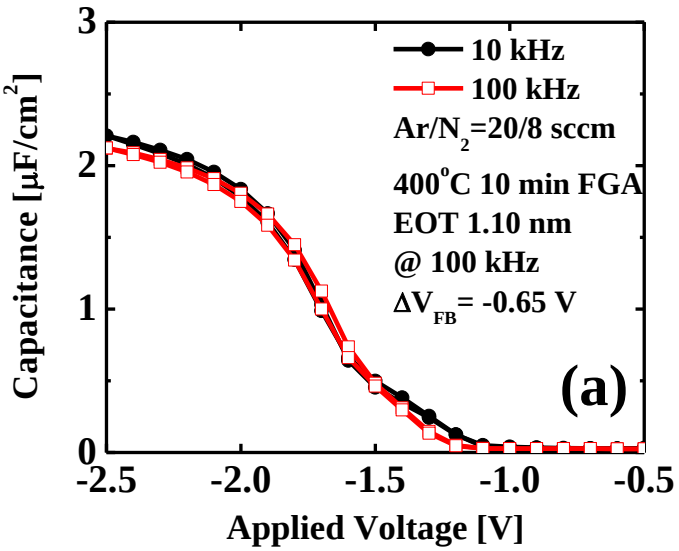


Fig. 3-5 (a) C-V and (b) J-V characteristics of the fabricated MIS diodes with FGA.



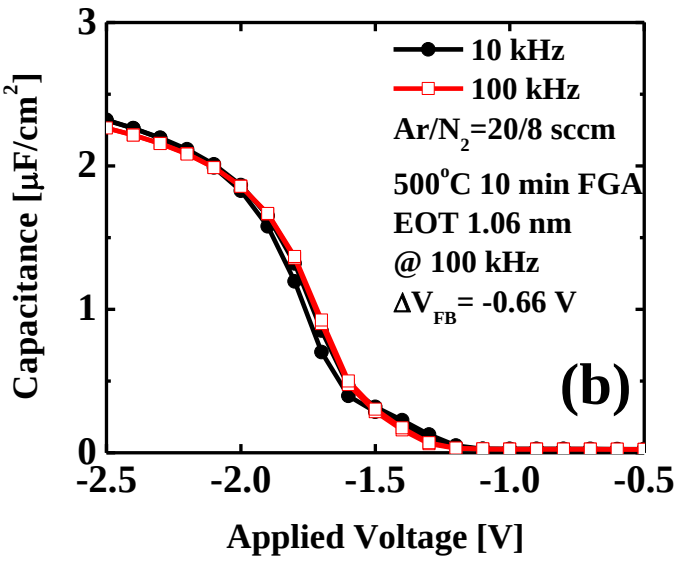


Fig. 3-6 C-V characteristics of (a) 400°C and (b) 500°C FGA for the fabricated MIS diodes.

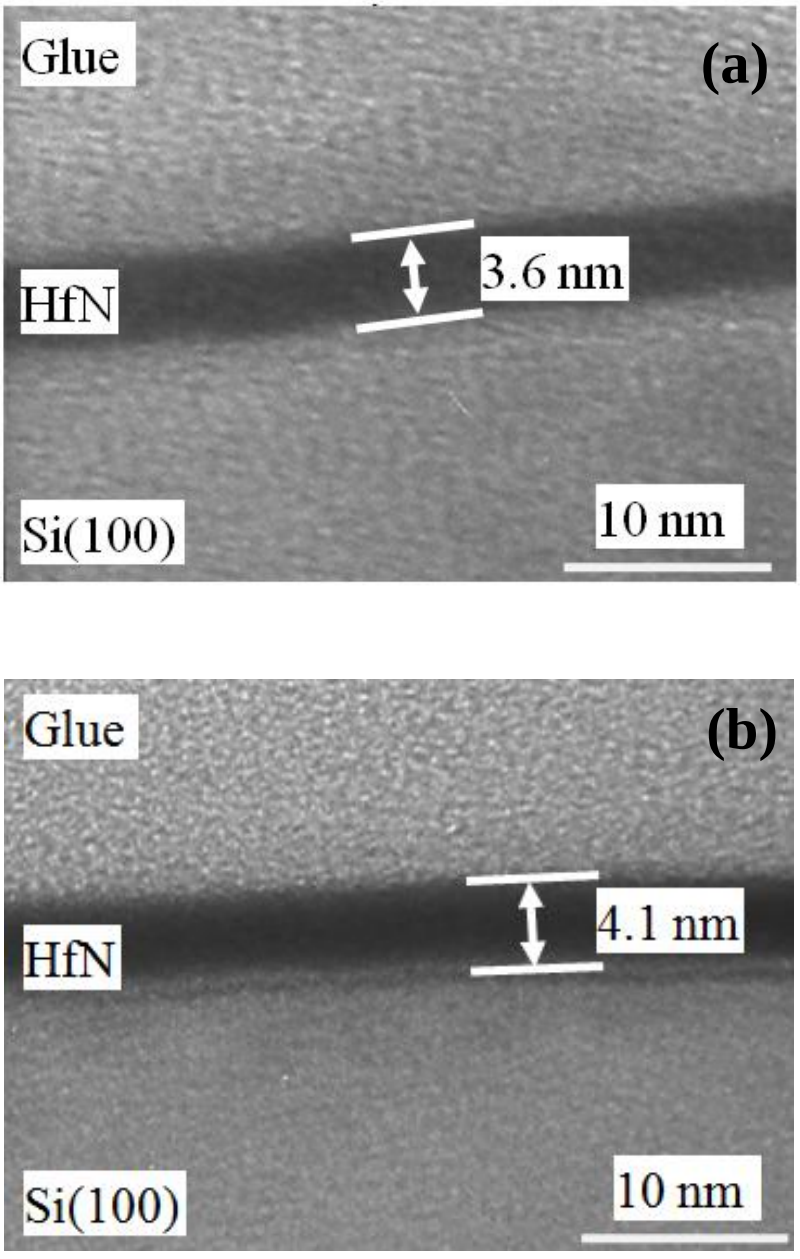


Fig. 3-7 Cross-sectional TEM images for (a) as-deposited and (b) 400^{o}C FGA sample.

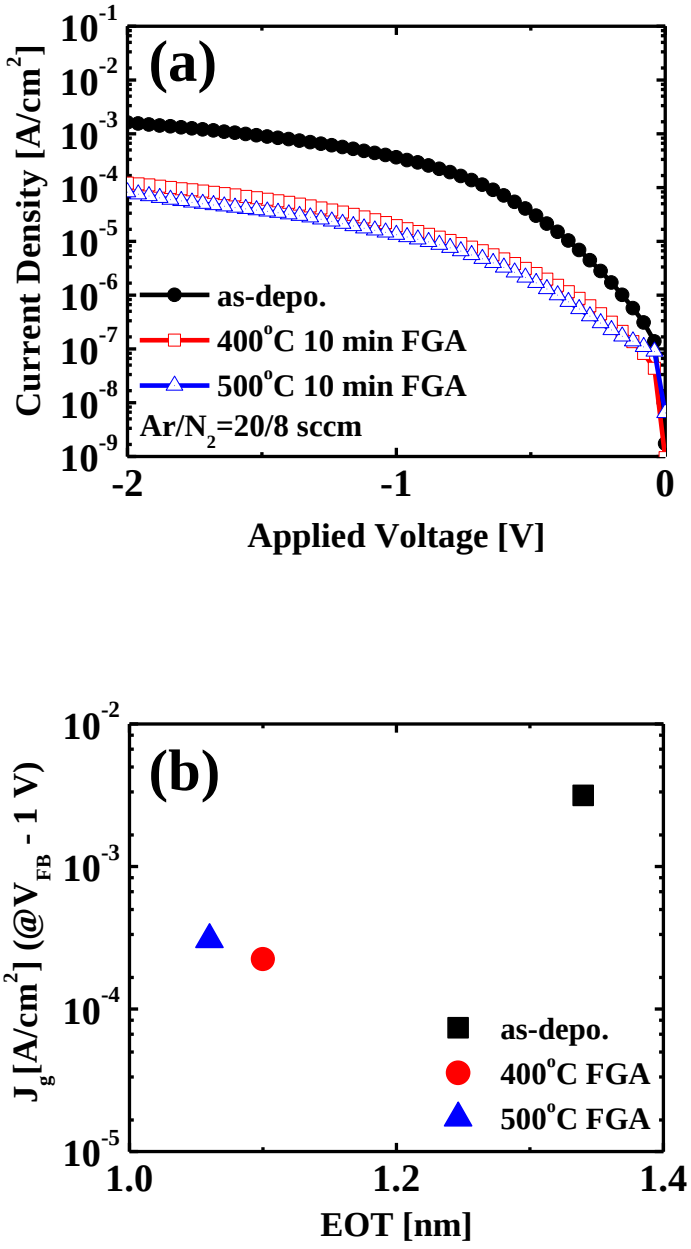


Fig. 3-8 (a) FGA temperature dependence of J-V characteristics and (b) EOT versus current densities.

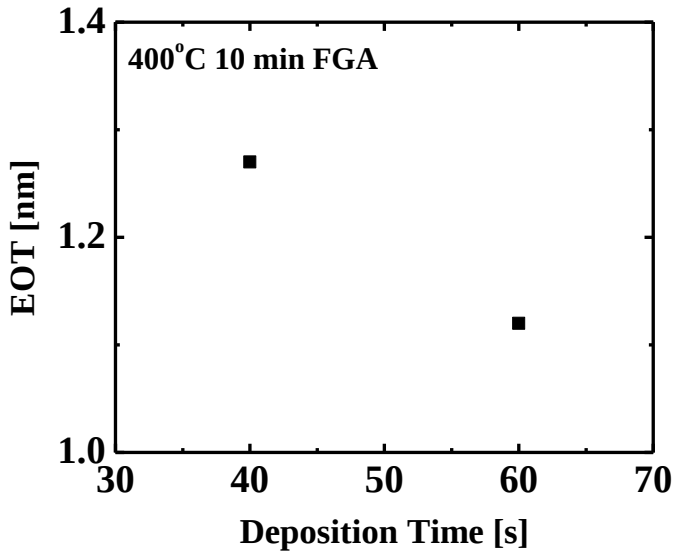


Fig. 3-9 Deposition time dependence of EOT

3.4 Improvement of electrical properties

In section 3.3, we discussed the effect of hydrogen annealing. After the FGA, the electrical characteristics were remarkably improved compared to the N_2 annealing. However, the obtained value of the relative dielectric constant as 15.1 is insufficiency. Therefore, we will discuss the dependence of deposition gas pressure and pre-sputtering condition to improve the electrical characteristics for the HfN gate insulator in this section.

3.4.1 Dependence of deposition gas pressure condition

In generally, when the film is formed by plasma method, the electrical characteristic should be changed by deposition condition such as deposition pressure, substrate temperature and so on. Especially, the deposition condition is an effective factor. To obtain a better properties film, the deposition gas pressure should be lower due to plasma damage. For that reason, we investigated the dependence of deposition gas pressure for the HfN gate insulator. In section 3.3, the Ar/N_2 gas flow ratio was fixed as 20/8 sccm. In this section, $N_2/(Ar+N_2)$ was fixed as 28% and then the deposition gas pressure was changed from 0.04 to 0.19 Pa. After depositing, the FGA was also carried out at 400^{o}C for 10 min. Figure 3-9 shows the C-V and J-V characteristics with various deposition pressures. When the deposition gas pressure was changed, there is no large difference of the maximum capacitance in Fig. 3-10(a). However, it was found that the hump was observed at Ar/N_2 = 10/4 and 2.5/1 sccm. Furthermore, the flat band voltage was shifted at low gas pressure. In Fig. 3-10(b), the leakage current density was low at Ar/N_2 = 20/8 sccm. It means that interface trap and positive trap charge were injected as the deposition gas pressure becomes lower. From the

results, the improvement of the HfN film was not obtained by lowering of the deposition gas pressure.

In Fig. 3-11, the XPS spectra (take-off angle: 80^{o}) of Hf 4f, N 1s, and Si 2p were shown with various deposition gas pressures. The spectra of Hf 4f show a doublet shape due to spin-orbital splitting into the Hf $4f_{5/2}$ and Hf $4f_{7/2}$. However, the spectra was shifted for Ar/N_2 = 20/8 sccm. In the N 1s spectra, Hf-N bonds also observed. However, Si-O bonds were also observed in the Si 2p spectra. Furthermore, it was found that the Hf-O bonds were also observed in the O 1s spectra. The surface and film were oxidized. Therefore, the relative dielectric constant was lower than the reported value.

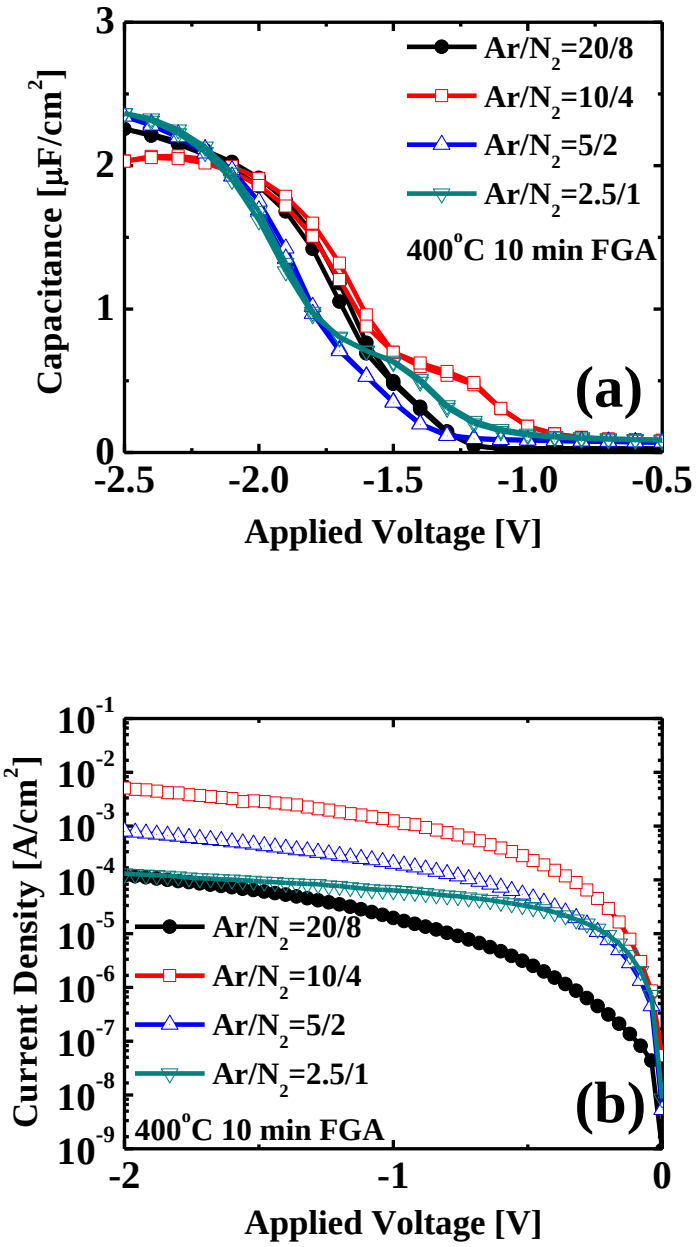


Fig. 3-10 (a) C-V and (b) J-V characteristics with various deposition gas pressures.

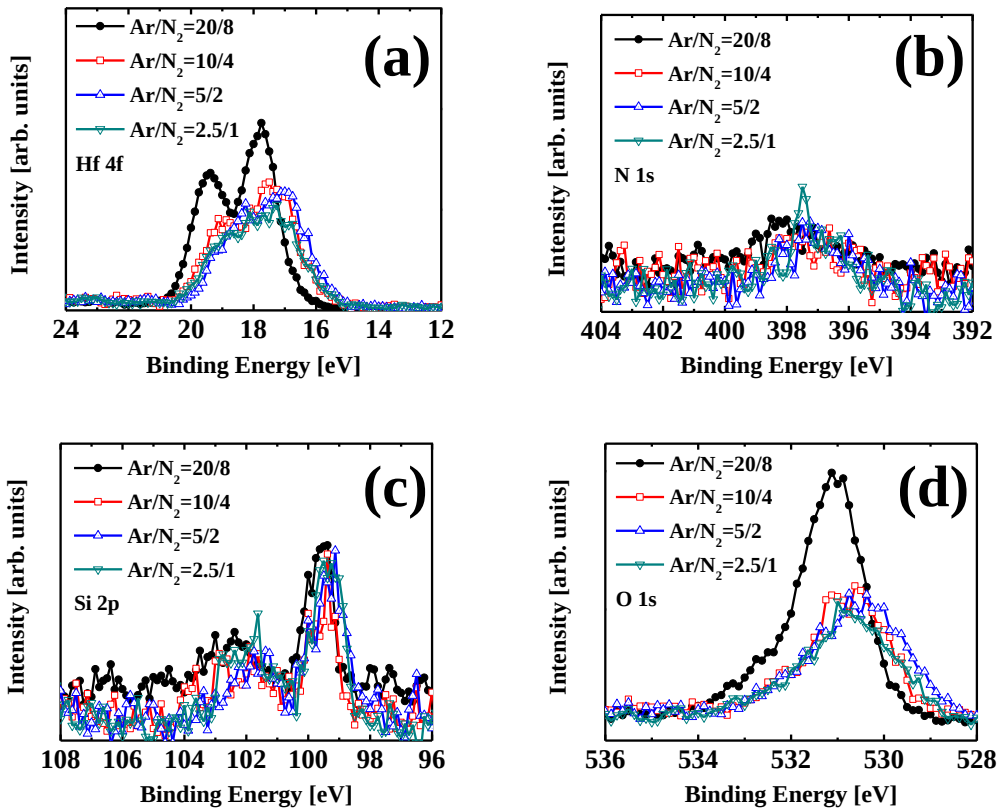


Fig. 3-11 the XPS spectra (take-off angle: 80^{o}) of (a) Hf 4f, (b) N 1s, (c) Si 2p, and (d) O 1s with various deposition gas pressures.

3.4.2 Dependence of pre-sputtering condition

3.4.2.1 Comparison of annealing ambient

Until now, the HfN film was deposited by ECR plasma sputtering in Ar/N_2 ambient. At that time, the pre-sputtering was carried out before the deposition of the HfN film using Ar/N_2 gas for 10 min to clean the Hf target. In case of ECR plasma deposition, there are two deposition modes (metal mode and oxide mode) as shown in Fig. 3-12 [12]. The oxide mode is that the target is oxidized through the Ar/O_2 pre-sputtering before deposition. Through the use of oxide mode, the high-quality oxide film was able to be deposited compared to the metal mode. In this manner, when the HfN film is deposited, the nitride mode was used to form a high-quality HfN film through the Ar/N_2 pre-sputtering. However, it is difficult to form uniform nitride on the surface of the Hf target. As shown in Fig. 3-13, the deposited HfN layer was oxidized over 20%. In order to suppress oxygen incorporation, therefore, before the deposition of HfN film, Ar pre-sputtering for Hf-target cleaning carried out for 10 min instead of Ar/N_2 pre-sputtering. The schematic diagram for the various pre-sputtering condition was shown in Fig. 3-14. The PDA was also carried out at 400^oC for 30 min in FG and nitrogen ambient for comparison utilizing RTA system. The flow rate of gases was approximately 1 SLM.

Figures 3-15(a) and (b) show C-V characteristics for the fabricated samples after PDA in FG and N_2 ambient, respectively. In case of N_2 annealing, the capacitance was much smaller than that of the FGA sample. Furthermore, the frequency dispersion and hysteresis were observed in the C-V curves. On the contrary, the small frequency dispersion and negligible hysteresis were obtained for the FGA sample. The capacitance was also increased remarkably compared to N_2-annealed sample. And

comparing the previous data using Ar/N_2 pre-sputtering, the capacitance was increased about 2 times. Even though the electrical property was improved by FGA, the small frequency dispersion was observed. Y. Lu et al. proposed a dual-frequency method for eliminating the frequency dispersion effect for high leakage devices [13]. By measuring capacitance and dissipation at two different frequencies, we obtained the result by applying technique as shown in Fig. 3-15(c). The two curves were found to be completely overlapped. It serves to demonstrate the efficacy of the technique. After frequency correction, the EOT of 0.6 nm was obtained. Figure 3-16 shows N 1s spectra of the HfN film with different pre-sputtering condition. Before the deposition of the HfN film, the Hf-N bonds were observed. After FGA, the Hf-N bond was disappeared for the Ar/N_2 pre-sputtering. However, the Hf-N bond was remained for the Ar pre-sputtering. It means that the Hf-N bond for the Ar pre-sputtering is stronger than that for the Ar/N_2 pre-sputtering after FGA. As the pre-sputtering condition was changed from Ar/N_2 to Ar, the EOT was greatly reduced.

The film thickness was determined by the cross-sectional SEM and TEM. The cross-sectional SEM and TEM images of the 400^{o}C FGA films for the HfN/p-Si(100) structure which were deposited for 5 and 1 min, respectively, were shown in Fig. 3-17. In Fig. 3-17(b), we confirmed no interfacial layer also. Physical thicknesses of the film after 400^{o}C FGA were 18 and 4 nm, respectively. From the TEM image, the relative dielectric constant for 400^{o}C FGA sample was obtained as 26. The obtained value of the relative dielectric constant is closed to the reported value. It means that the Ar pre-sputtering leads to improve the electrical characteristic of HfN gate insulator. Next, the density of interface states (D_{it}) was evaluated. The Terman method was performed to evaluate D_{it} [14]. Figure 3-18 shows D_{it} for the fabricated MIS diode

after FGA. For 400°C FGA, we can see that the D_{it} was as low as an order of 10^{11} $cm^{-2}eV^{-1}$. It was suggested that the FGA causes diffusion of hydrogen at the interface of nitrogen-rich HfN film and p-Si(100), and then the electrical properties were improved by hydrogen annealing effect and Ar pre-sputtering. Furthermore, the fixed charge density of the film was estimated to be 3.6 x 10^{12} cm^{-2} from the V_{FB} shift (0.11 V). Figure 3-19 shows J-V characteristic of the fabricated MIS diode after FGA and N_2 anneal. The leakage current of 3.7 x 10^{-3} A/cm^2 (@ V_{FB} -1 V) in case of N_2 anneal decreased to 6.2 x 10^{-4} A/cm^2 in case of FGA.

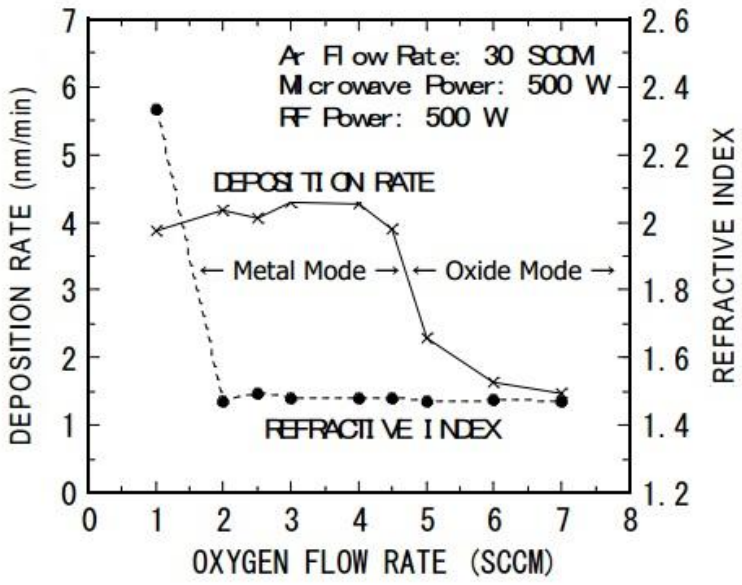


Fig. 3-12 Deposition rate with different deposition mode such as metal mode and oxide mode [12].

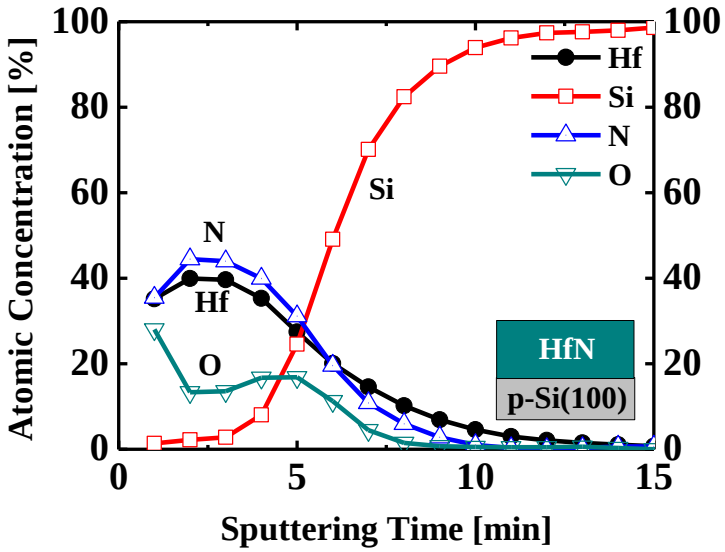


Fig. 3-13 Depth profile of atomic concentrations for Hf, Si, N, and O in the deposited film with Ar/N_2 pre-sputtering.

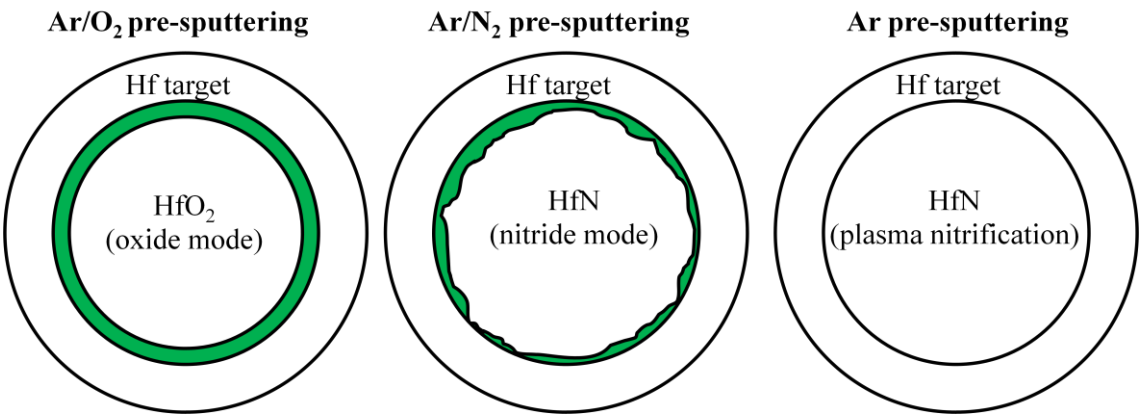


Fig. 3-14 A Schematic diagram for the various pre-sputtering conditions.

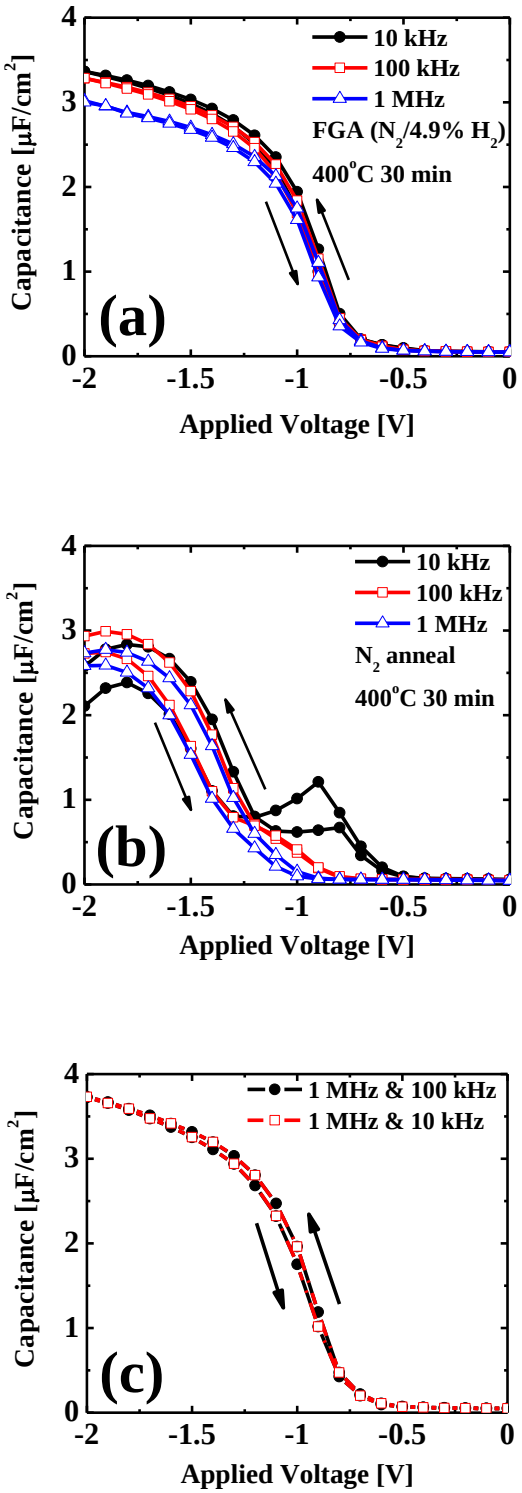


Fig. 3-15 C-V characteristics using Ar pre-sputtering for (a) FGA, (b) N_2 annealing, and (c) dual-frequency method of FGA sample.

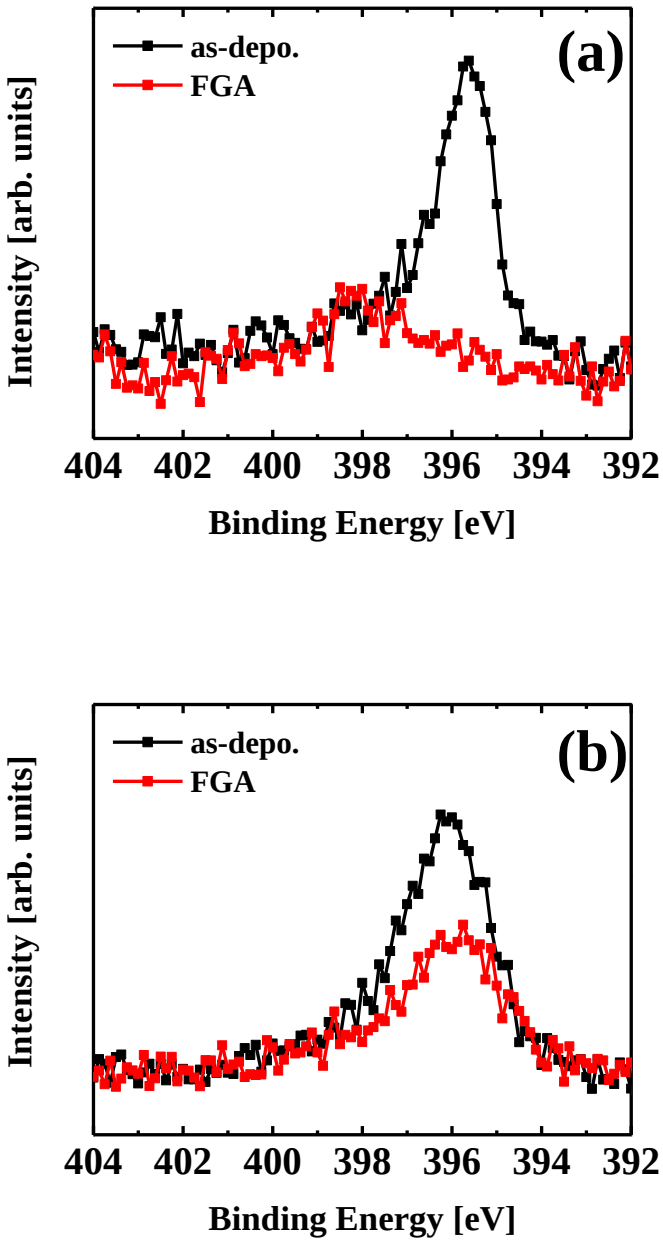


Fig. 3-16 N 1s spectra for the HfN film for (a) Ar/N_2 pre-sputtering and (b) Ar pre-sputtering.

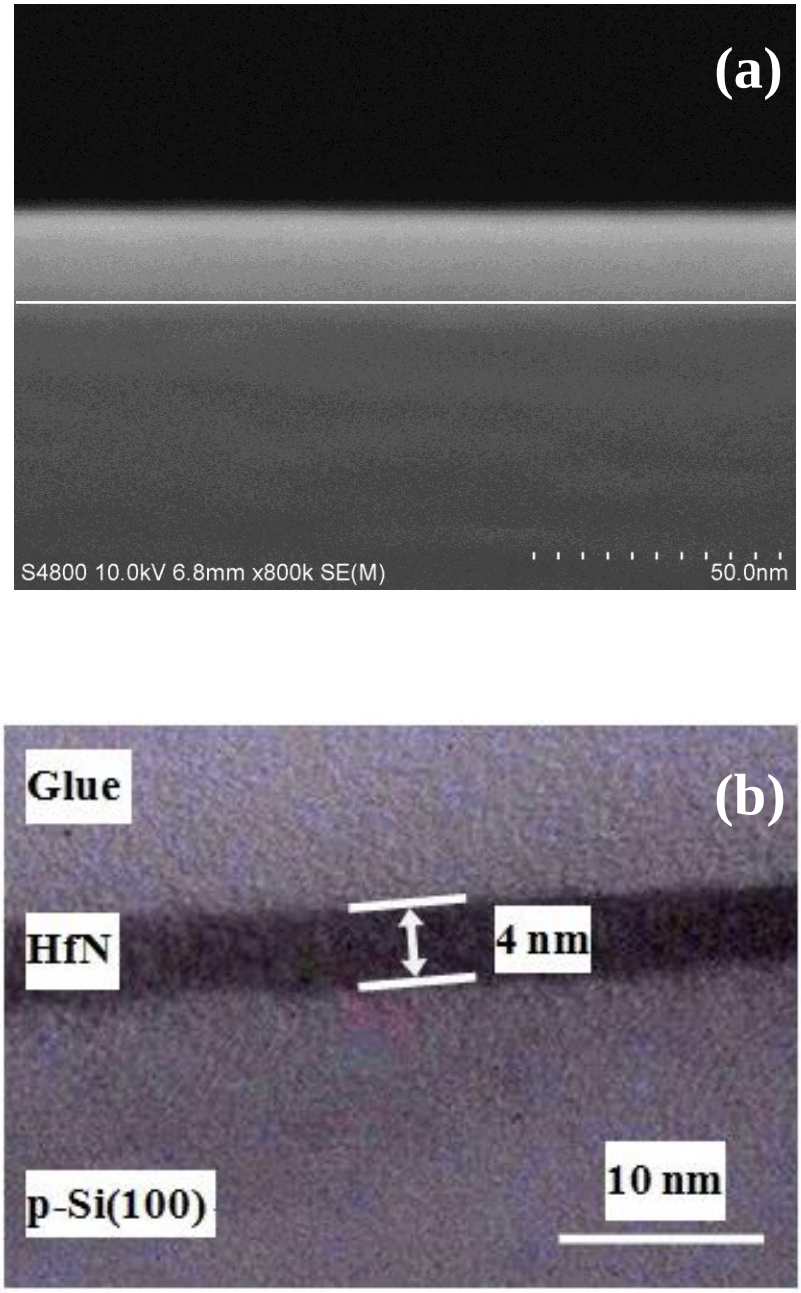


Fig. 3-17 Cross-sectional SEM and TEM images for 400^{o}C FGA sample using Ar pre-sputtering.

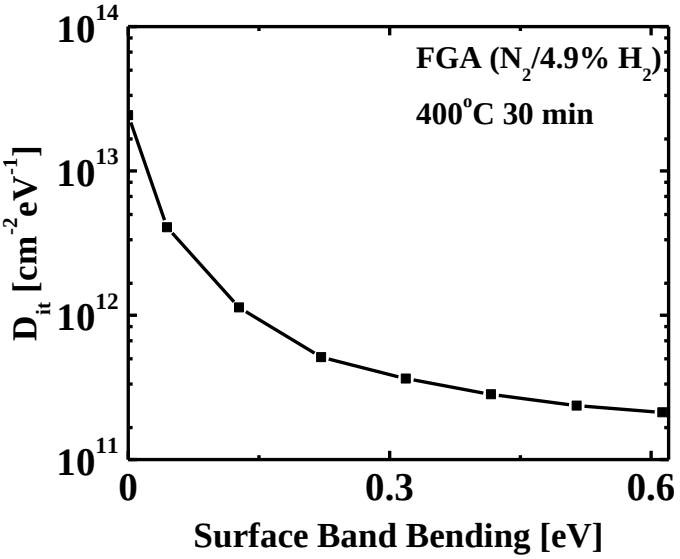


Fig. 3-18 D_{it} as a function of surface band bending for the MIS diode with FGA.

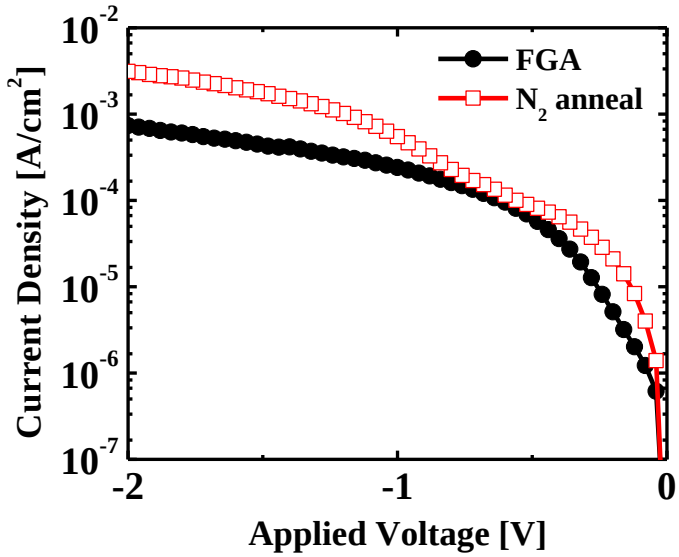


Fig. 3-19 J-V characteristics for the MIS diode with FGA and N_2 annealing.

3.4.2.2 Dependence of hydrogen annealing temperature

We found that the Ar pre-sputtering leads to improve the electrical properties for the HfN gate insulator. In this section, we investigated dependence of hydrogen annealing temperature for the HfN gate insulator. After the deposition of HfN film, the hydrogen annealing was carried out at 600 and 800^{o}C for 30 min. The C-V characteristics are shown in Fig. 3-20. When the hydrogen annealing was carried out over 600^{o}C for 30 min, the capacitances were decreased compared by 400^{o}C annealed sample. In general, the hydrogen was escaped from the interface over 500^{o}C. Therefore, the hydrogen annealing was performed below 500^{o}C. In this reason, the hydrogen annealing cannot affect to the electrical properties. Furthermore, we also measured the film roughness using AFM as shown in Fig. 3-21. The RMS roughnesses were 0.14, 0.18, and 0.18 nm at 400, 600, and 800^{o}C FGA, respectively. The results are summarized in Table 3-1. As increased the annealing temperature, the RMS roughness was increased. It is found that the RMS roughness affects to the electrical properties.

Table 3-1 RMS roughness for the various annealing temperatures.

Annealing temperature	RMS roughness
400^{o}C	0.14 nm
600^{o}C	0.18 nm
800^{o}C	0.18 nm

.

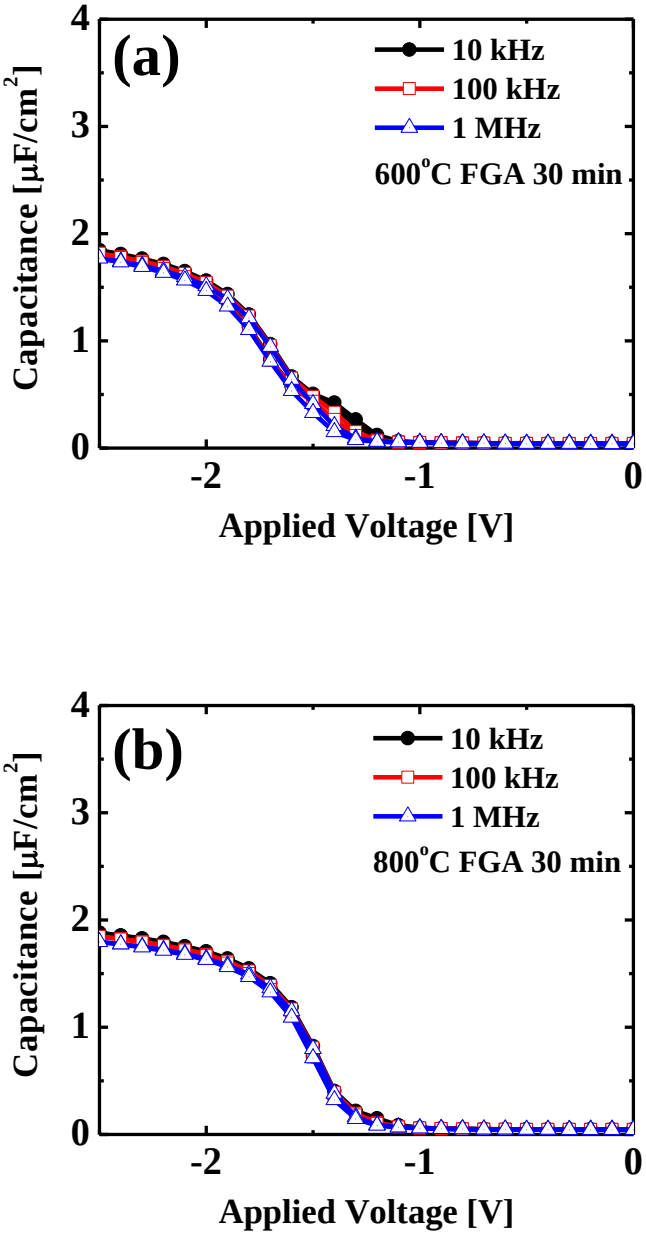


Fig. 3-20 C-V characteristics for (a) 600 and (b) 800°C FGA.

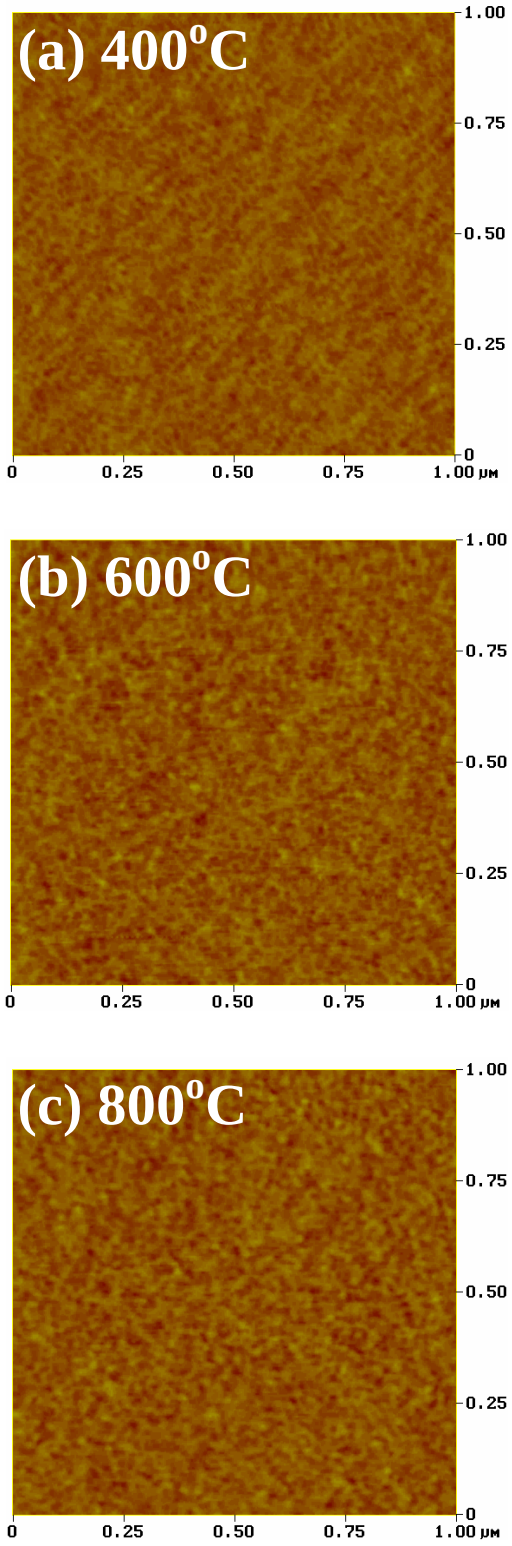


Fig. 3-21 RMS roughness for HfN film at (a) 400, (b) 600, and (c) 800°C FGA.

3.4.3 Atomic concentration of HfN films

In order to evaluate the nitrogen concentration of HfN, we first deposited 30 nm-thick HfN film (Ar/N_2 = 20/8 sccm) with 400^{o}C FGA for 30 min, and then the XPS depth profile measurements were performed. Figure 3-22(a) shows the depth profile of atomic concentrations for Hf, Si, N, and O in the film. The surface of film was oxidized in air and less than 5% oxygen occupied in the film. Furthermore, the film was not oxidized. In the HfN film, the atomic concentration ratio of hafnium and nitrogen was confirmed as 1:1.2 by the XPS depth profile. Figures 3-22(b) and (c) show the XPS spectra of Hf 4f and N 1s obtained from the Ar^+ etching cycles in the film for the sample formed with FGA, respectively. As shown in Fig. 3-22(b), the spectrum of Hf 4f shows a doublet shape due to spin-orbital splitting into the Hf $4f_{5/2}$ and Hf $4f_{7/2}$. The binding energy of Hf $4f_{7/2}$ centered at 15.1 eV was determined to correspond to the Hf-N bond in the nitrogen-rich HfN film, which was consistent with the reported values by Fix et al. for the nitrogen-rich HfN film [15]. The binding energy of 397.4 eV was attributed to the Hf-N bond in the nitrogen-rich HfN film as shown in Fig. 3-22(c). Moreover, the XPS spectrum of Si 2p shows only Si-Si bonding at the interface in Fig. 3-22(d). It means that there is no IL such as SiN or SiON. We confirmed that the deposited film became an insulator without IL from the results mentioned above.

Next, we also evaluated the nitrogen concentration of the HfN films at different Ar/N_2 flow ratio. Figure 3-23 shows the depth profile of atomic concentrations for Hf, Si, N, and O in the films which were deposited at $N_2/(Ar+N_2)$ = 12 and 20%. At that time, the deposition gas pressure was same as 0.19 Pa. Comparing Fig. 3-22(a), the oxygen occupied less than 10%. Furthermore, the atomic concentration ratio of hafnium and nitrogen was different. Nitrogen ratio is larger than hafnium. However, N fraction

for Hf was smaller than that of Fig. 3-22(a). It leads to poor electrical properties. It means that the nitrogen ratio for hafnium is an important factor. The relationship between the N fraction for Hf and EOT is summarized in Fig. 3-24. As increasing the N fraction for Hf, the EOT was also increased. In this study, the nitrogen-rich HfN film showed good electrical properties at 1:1.2.

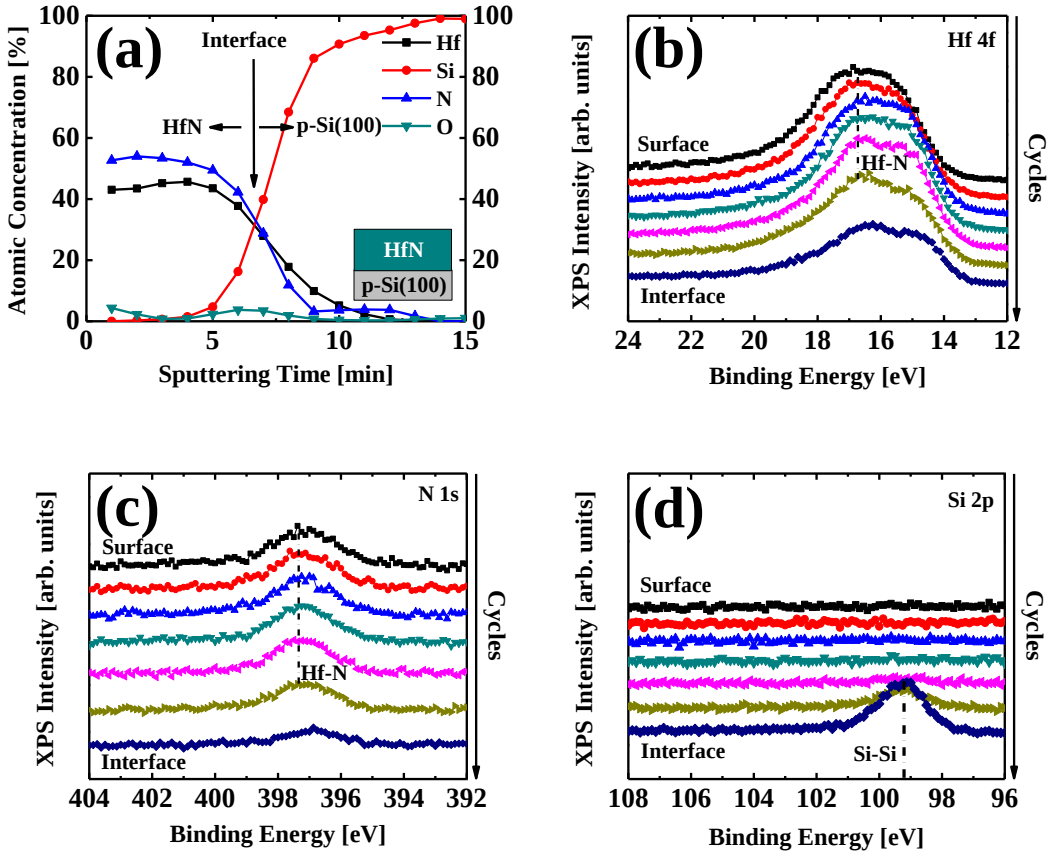


Fig. 3-22 (a) Depth profile of atomic concentrations for Hf, Si, N, and O in the deposited film, (b) Hf 4f, (c) N 1s, and (d) Si 2p XPS spectra.

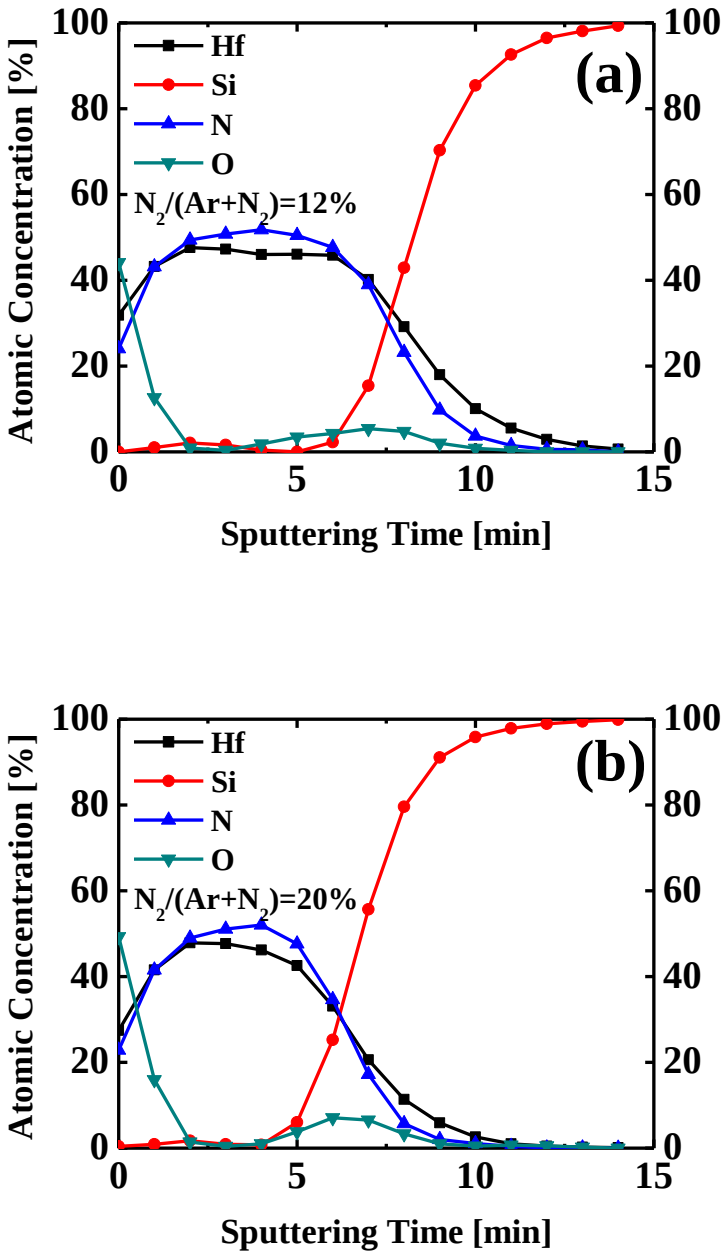


Fig. 3-23 Depth profile of atomic concentrations for Hf, Si, N, and O in the deposited films (a) $N_2/(Ar+N_2)$ = 12% and (b) 20%.

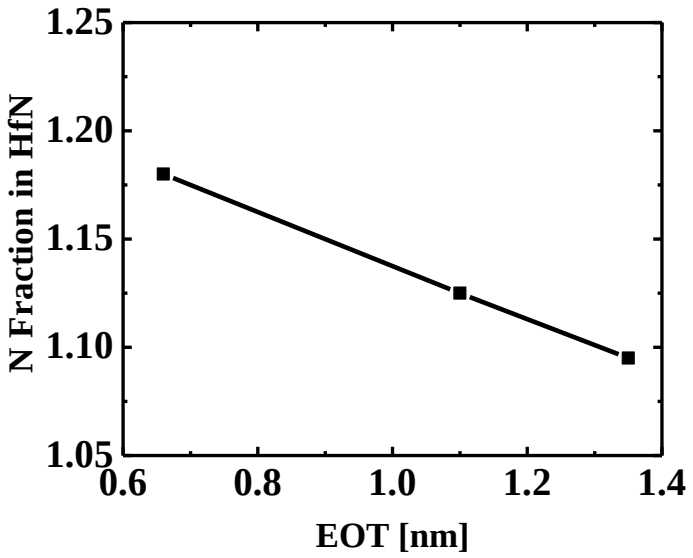


Fig. 3-24 EOT versus Hf/N ratio for the HfN gate insulator.

3.4.4 Thickness dependence of HfN gate insulator

In section 3.4.2, we confirmed the HfN film thickness through TEM image when the HfN film was deposited for 60 s. In order to reduce EOT for HfN gate insulator, we investigated dependence of film thickness through deposition time from 60 to 15 s. The deposition gas pressure and Ar/N_2 flow ratio were same. And the all samples were annealed at 400^{o}C for 30 min using FG. Figure 3-25 shows the thickness dependence of C-V and J-V characteristics. As decreased the deposition time, the capacitance was also decreased dramatically, and the hump was observed. In J-V characteristics, the leakage currents were also increased with reducing the deposition time. We guessed that the obtained energy was changed for HfN film, when the film thickness was decreased. It is necessary to find an optimum annealing condition. Therefore, we changed annealing condition for the HfN film.

Figure 3-26(a) shows C-V characteristics with various annealing conditions for 15 s deposited HfN film. When the annealing temperature was increased to 500^{o}C, the capacitance was also increased. However, the hump was remained. It means that the hydrogen diffusion is not sufficient in the interface. The annealing time was increased from 10 to 20 min, the hump was disappeared and the capacitance was also increased. Furthermore, the hysteresis was not observed. The hydrogen was diffused sufficiently to the interface for 20 min annealing. By measuring capacitance and dissipation at two different frequencies for the 20 min annealed sample, we obtained the result by applying technique as shown in Fig. 3-26(b). After frequency correction, the EOT of 0.5 nm was obtained. This value is the lowest EOT in the high-k nitride dielectric. Figure 3-27 shows a leakage current as a function of EOT for the fabricated Al/HfN/p-Si(100) MIS diodes. The leakage current was measured at the V_{FB} -1 V. The reported data

for direct-contact high-k HfO_2 and HfSiON are also plotted for comparison [16-17]. The leakage current of the gate stack fabricated in this work is much lower than those of direct-contact HfO_2 with k = 13 and HfSiON.

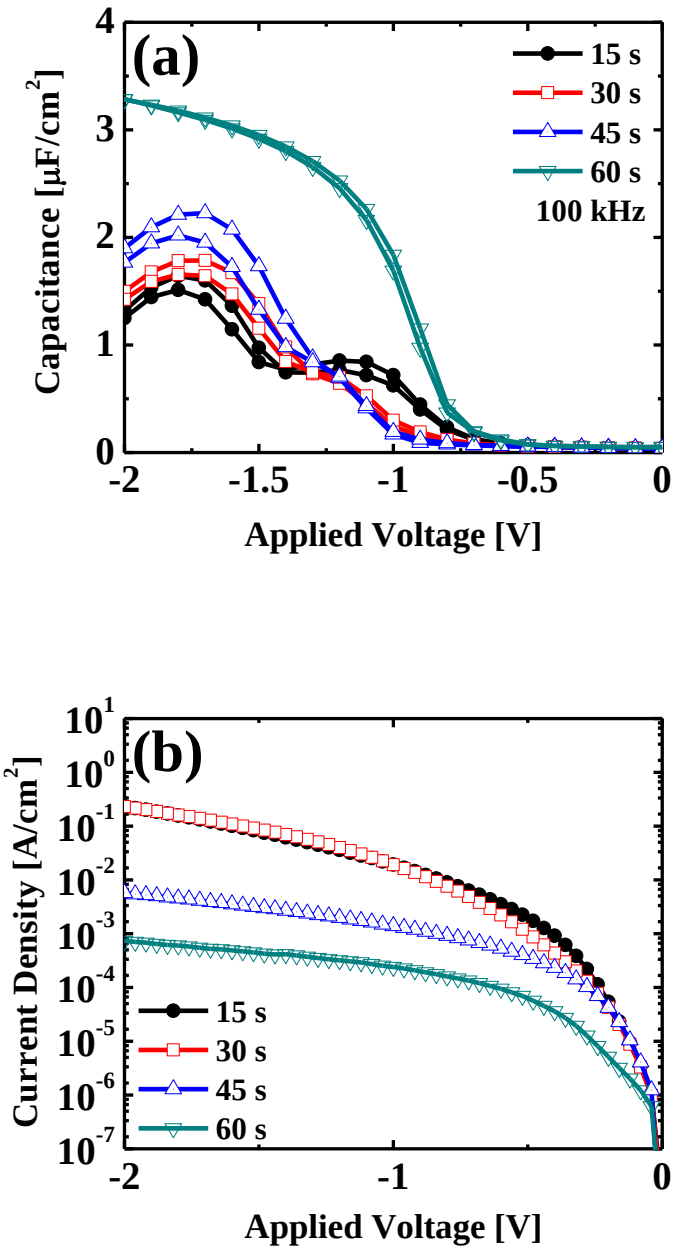


Fig. 3-25 (a) C-V and (b) J-V characteristics with various deposition times.

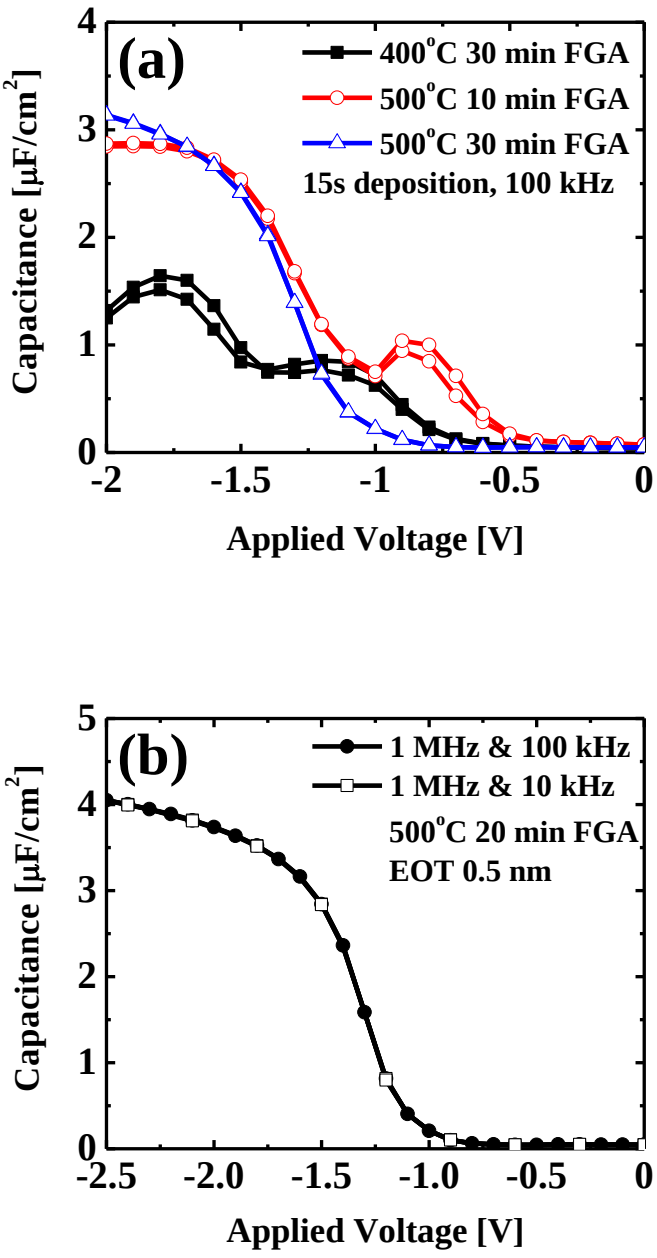


Fig. 3-26 (a) C-V characteristics with various annealing conditions for 15 s deposited HfN film and (b) dual-frequency method of the 500°C 20 min annealed sample.

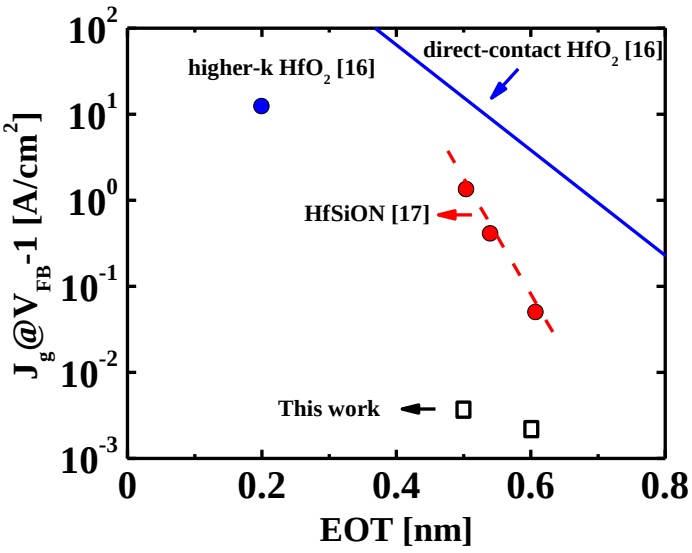


Fig. 3-27 J_g as a function of EOT for Al/HfN/p-Si(100) gate stack with direct-contact HfO_2 and HfSiON gate stacks.

3.5 Summary

The HfN gate insulator was investigated by ECR plasma sputtering method in this chapter. The MIS diodes with HfN gate insulator were fabricated to discuss their characteristics. The obtained results would be summarized as follows.

- The HfN films were deposited by ECR plasma sputtering method with various Ar/N_2 flow ratio. From the C-V and J-V characteristics, we confirmed that the deposited HfN film showed insulating property. At Ar/N_2 = 20/8 sccm, the capacitance was the highest and the leakage current was low enough.

- The effect of hydrogen anneal for HfN gate insulator was investigated. The capacitance was increased and the hump was disappeared by FGA compared to nitrogen annealing. The EOT was 1.12 at 400^{o}C FGA for 30 min. Furthermore, it was found that there is an interfacial layer after FGA from the cross-sectional TEM image.

- After the FGA, the electrical characteristics were remarkably improved. However, the obtained value of the relative dielectric constant as 15.1 is insufficiency. Furthermore, the oxygen was occupied over 20 % in the HfN film. Therefore, we investigated the dependence of deposition gas pressure and pre-sputtering condition to suppress the oxygen. From the dependence of deposition gas pressure, we could not obtain to improve the electrical properties. However, the capacitance was remarkably increased by Ar pre-sputtering, because it is difficult to form uniform nitride on the surface of the Hf target. In order to suppress oxygen incorporation, therefore, before the deposition of HfN film, Ar pre-sputtering for Hf-target cleaning carried out. After

frequency correction, the EOT of 0.6 nm was obtained. Through the cross-sectional TEM image, the thickness of the 400^{o}C FGA HfN film was 4 nm. We confirmed no interfacial layer also. The relative dielectric constant for 400^{o}C FGA sample was obtained as 26. The obtained value of the relative dielectric constant is closed to the reported value. The D_{it} was as low as an order of 10^{11} $cm^{-2}eV^{-1}$. Ar pre-sputtering leads to the formation of the HfN with strong Hf-N bond.

- Atomic concentrations for Hf, Si, N, and O were calculated by XPS the depth profile. It was found that less than 5% oxygen occupied in the film. In the HfN film, the atomic concentration ratio of hafnium and nitrogen was confirmed as 1:1.2. We also evaluated the nitrogen concentration of the HfN films at different Ar/N_2 flow ratio. When the N fraction for Hf was small, it leads to poor electrical properties.

- In order to reduce EOT for HfN gate insulator, we investigated dependence of film thickness through deposition time from 60 to 15 s. As decreased the deposition time, the capacitance was also decreased dramatically, and the hump was observed. However, the EOT of 0.5 nm was obtained at 500^{o}C FGA for 20 min. Comparing other researches, the leakage current was much lower than those of direct-contact HfO_2 with k = 13 and HfSiON.

Reference

[1] C. S. Lai, S. K. Peng, T. M. Pan, J. C. Wang, and K. M. Fan, "Work Function Adjustment by Nitrogen Incorporation in HfN_x Gate Electrode with Post Metal Annealing", *Electrochem. Solid-State Lett.*, vol. 9, no. 7, pp. G239-241, 2006.

[2] Y. C. Yeo, Q. Lu, W. C. Lee, T. J. King, C. Hu, X. Wang, X. Guo, and T.P. Ma, "Direct Tunneling Gate Leakage Current in Transistors with Ultrathin Silicon Nitride Gate Dielectric", *IEEE Electron Device Lett*., vol. 21, no. 11, pp. 540-542, 2000.

[3] K.S.A. Butcher and T.L. Tansley, "Ultrahigh resistivity aluminum nitride grown on mercury cadmium telluride", *J. Appl. Phys*., vol. 90, no. 12, pp. 6217-6221, 2001.

[4] T. L. Chu, J. R. Szedon, and C. H. Lee, "The preparation and C-V charac- teristics of $Si\text{-}Si_3N_4$ and $Si\text{-}SiO_2\text{-}Si_3N_4$ structures", *Solid-State Electron,* vol. 10, pp. 897-905, 1967.

[5] X. Wang, M. Khare, and T. P. Ma, "Effects of Water Vapor Anneal on MIS Devices Made of Nitrided Gate Dielectrics", *Symp. VLSI Technol. Dig. Tech.,* pp. 226-227, 1996.

[6] T. P. Ma, "Making Silicon Nitride Film a Viable Gate Dielectric", *IEEE. Trans. Electron Devices*, vol. 45, no. 3, pp. 680-690, 1998.

[7] B. Swaroop, "Hydrogen annealing effect on silicon-insulator(s) interface states", *J. Phys. D: Appl. Phys.*, vol. 6, pp. 1090-1092, 1973.

[8] S. Saito, K. Torii, M. Hiratani, and T. Onai, "Analytical Quantum Mechanical Model for Accumulation Capacitance of MOS Structures", *IEEE Electron Device Lett.*, vol. 23, no. 6, pp. 348-350, 2002.

[9] F. H. P. M. Habraken and A. E. T. Kuiper, “Silicon nitride and oxynitride films”, *Mater. Sci. Eng.*, vol. R12, pp. 123-175, 1994.

[10] P. Balk, “40 years MOS technology - from empiricism to science”, *Microelectron. Eng*., vol. 48, pp. 3-6, 1999.

[11] H.D. Kim, H. M. An, Y. J. Seo, Y. J. Zhang, and T. G. Kim, “Negative-/Positive-Bias-Instability Analysis of the Memory Characteristics Improved by Hydrogen Postannealing in MANOS Capacitors”, *IEEE. Trans. Device Mater. Rel.*, vol. 10, pp. 295-300, 2010.

[12] http://www.mes-afty.co.jp.

[13] G. Gerlach, K. Maser, and A. M. Saad, “Activation energy of thermally grown silicon dioxide layers on silicon substrates”, *Phys. Status Solidi B*, vol. 246, pp. 2242-2247, 2009.

[14] L. M. Terman, “An investigation of surface states at a silicon/silicon oxide interface employing metal-oxide-silicon diodes”, *Solid-State Electron.*, vol. 5, no. 5, pp. 285-299, 1962.

[15] R. Fix, R. G. Gordon, and D. M. Hoffmann, “Chemical Vapor Deposition of Titanium, Zirconium, and Hafnium Nitride Thin Films”, *IEEE. Trans. Electron Devices*, vol. 45, no. 3, pp. 680-690, 1998.

[16] Y. Morita, S. Migita, W. Mizubayashi, and H. Ota, “Extremely scaled EOT of higher-k ALD-HfO2 gate stacks”, *Ext. Abstr. Solid State Devices and Materials*, 2011, p. 955.

[17] T. Sano and S. Ohmi, “In situ Formation of HfN/HfSiON Gate Stacks with 0.5 nm EOT Utilizing Electron Cyclotron Resonance Plasma Sputtering on Three-Dimensional Si Structures”, *Jpn. J. Appl. Phys.*, vol. 50, pp. 04DA091-5, 2011.

Chapter 4

Reliability of HfN gate insulator

In this chapter, the reliability for hafnium nitride gate insulator is discussed. In order to calculate the activation energy, the measurement temperature dependence of leakage current density is evaluated. Carrier transport mechanism is investigated for the diode with the HfN gate insulator. Furthermore, the TDDB is investigated compared to SiN. Finally, the stress induced leakage current is also evaluated.

4.1 Introduction

High-k gate dielectrics such as Hf-based oxides are being implemented in Si complementary metal-oxide-semiconductor (CMOS) technology to alleviate the rapid gate current increases associated with aggressive dielectric thickness scaling [1-3]. Replacement of SiO_2 as a gate dielectric is most urgent for low power circuits where gate leakage related power consumption and reliability are serious limitations [4-6]. There are some reliability issues for the high-k dielectric such as charge trapping, instability of threshold voltage (V_{th}), negative bias temperature instability (NBTI), and time dependent dielectric breakdown (TDDB).

In this section, we will present our experimental results of the reliability for nitrogen-rich HfN gate insulator. TDDB has been reported for ultrathin gate insulators, showing that thinner insulators have a higher sensitivity to measurement temperature [7]. Although high-k dielectrics have shown excellent reliability at room temperature, the reliability at high temperatures may still be concerns. We evaluated activation energy (E_A), carrier transport mechanism, and the TDDB characteristics for the HfN gate insulator. Furthermore, the stress induced leakage current is also evaluated.

4.2 Measurement temperature dependence of electrical properties

In this section, we will present our experimental results on the temperature effect on the reliability of HfN gate insulator with an equivalent oxide thickness (EOT) of 0.6 nm. Measurements temperature was from 298 to 398 K.

4.2.1 C-V characteristics

First, the measurement temperature dependence of C-V characteristics was shown in Fig. 4-1. The measurement frequency was 1 MHz and all C-V curves were normalized. As the temperature was changed from 298 to 398 K, the C-V curves were shifted toward negative direction and the hysteresis became larger. We consider that the fraction of interface trap density (D_{it}) is increased when the capacitor is subjected to positive charge-temperature change and that it dominates the C-V behavior of the sample under test.

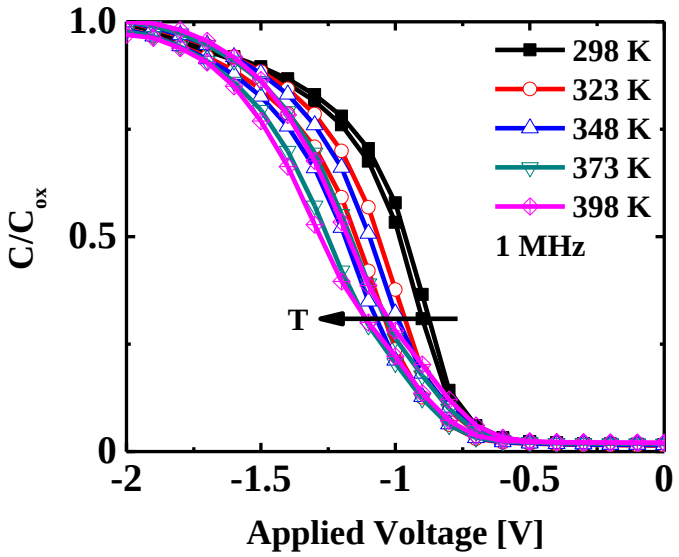


Fig. 4-1 Measurement temperature dependence of C-V characteristics.

4.2.2 J-V characteristics

Next, the measurement temperature dependence of J-V characteristics was shown in Fig. 4-2(a). The leakage current density increases by almost two orders of magnitude with temperature from 298 to 398 K. The variation in leakage current density near the flatband voltage (V_{FB}) as a function of temperature is shown in Fig. 4-2(b). Near the V_{FB}, the leakage current densities were changed linearly.

From the results in section 4.2.1 and 4.2.2, we will evaluate the E_A for the HfN gate insulator.

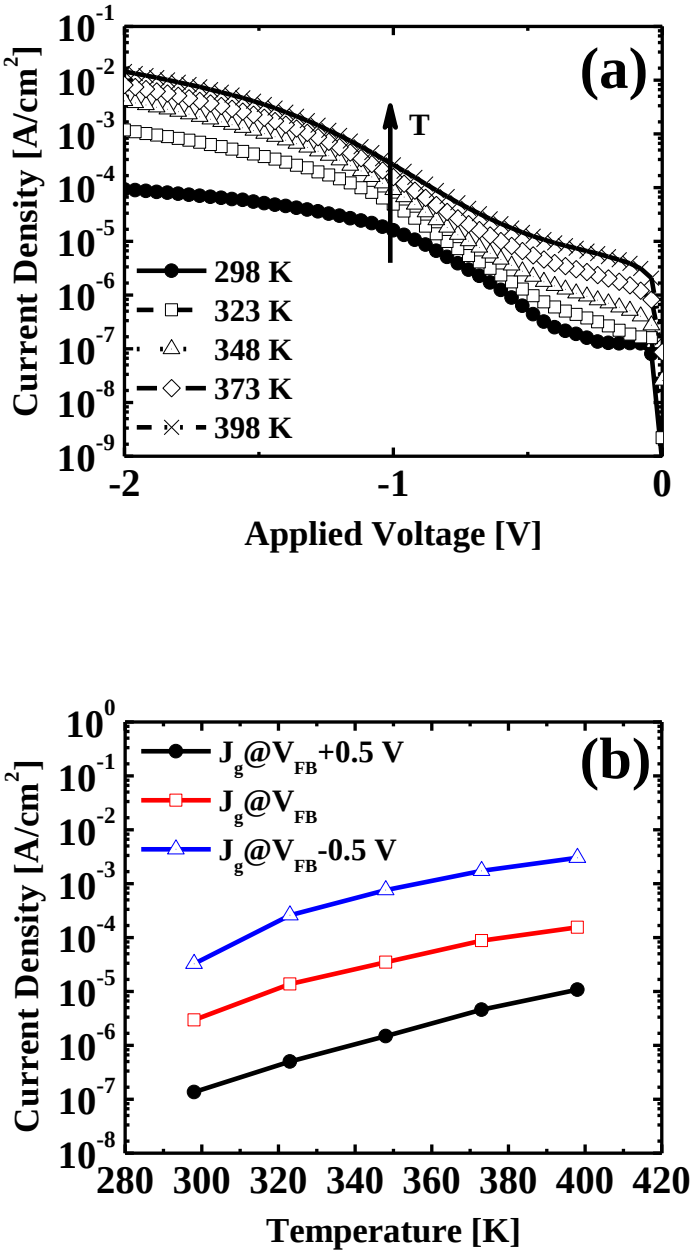


Fig. 4-2 (a) Measurement temperature dependence of J-V characteristics and (b) leakage current density as a function of temperature near the V_{FB}.

4.2.3 Evaluation of activation energy

In chemistry, activation energy is a term introduced in 1889 by the Swedish scientist S. Arrhenius that is defined as the energy that must be overcome in order for a chemical reaction to occur. Activation energy may also be defined as the minimum energy required starting a chemical reaction. The activation energy of a reaction is usually denoted by E_A.

To calculate the E_A, the leakage current density is plotted in Arrhenius scale and shown in Fig. 4-3. The Arrhenius plot for HfN film shows a linear dependence and the measured data were fitted by the following relation [8]:

$$J \propto \exp(-E_A/k_B T) \tag{4.1}$$

where k_B is the Boltzmann constant (8.617×10^{-5} eVK^{-1}), and T is the absolute temperature. The calculated value of E_A was found to be 1.6 eV. If the E_A is smaller than half of the Si band gap energy ($E_A < E_g/2$), the leakage current is explained by the Poole-Frenkel emission mechanism [9]. It means that there are traps in the film and these traps lead to larger leakage current as well. Therefore, it was found that the HfN film is stable and has lower traps.

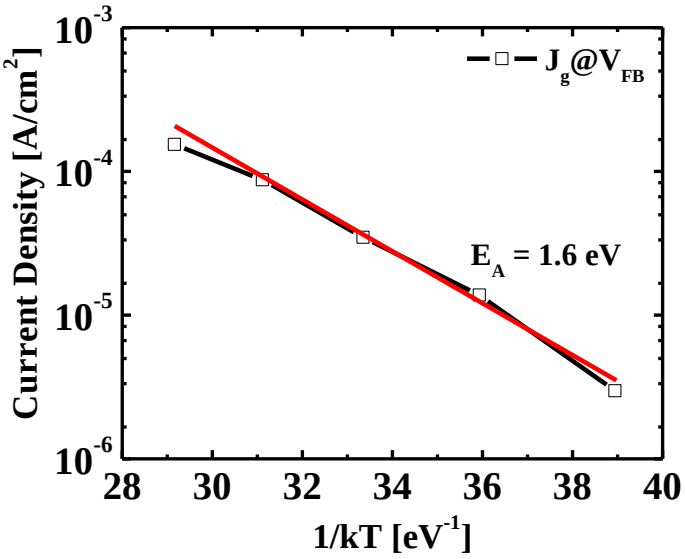


Fig. 4-3 Arrhenius plot of leakage current density for the HfN gate insulator.

4.3 Carrier transport mechanism for the HfN film

In this section, various types of charge conduction mechanisms through a gate oxide will be described in relation to MIS application. There are many carrier transport mechanism of leakage current in the insulator. Among them, some mechanisms should be considered for the HfN film such as Poole-Frenkel (PF) emission, Schottky (SC) emission, and Fowler-Nordheim (FN) tunneling as shown in Fig. 4-4. We already mentioned in section 4.2.3, the HfN film is stable and has lower traps. To confirm that result, J-V equations of each mechanism are transformed into the linear form.

PF is a kind of trap assisted transport mechanism. It relies on electrons or holes hopping into/out-of traps, which means that the trap density in the insulator leads to the PF conduction. The PF emission is given by equation 4.2.

$$J \propto E \exp\left[\frac{-q(\phi_B - \sqrt{qE/\pi\varepsilon_i})}{kT}\right] \quad (4.2)$$

where ϕ_B, ε_i, and k are the PF barrier height and dynamic dielectric constant, Boltzmann's constant, respectively. If the carrier transport mechanism of the HfN film is PF, $\ln(I_g/V_g)$ vs $V_g^{1/2}$ should accord whit linear relationship. The PF emission plot is shown in Fig. 4-5(a). In the $\ln(I_g/V_g)$ vs $V_g^{1/2}$ plot, it was not shown linear relationship, which means that PF emission is not the main mechanism for the HfN film. It fits well with the result of the E_A. Furthermore, the ϕ_B is extracted from eq. 4.2. The extracted PF barrier was 0.89 eV at room temperature.

SC emission is a field-assisted thermionic emission of an electron over a surface barrier. SC emission is given by equation 4.3

$$J = A^{*}T^{2}\exp\left[\frac{-q(\phi_B-\sqrt{qE/4\pi\varepsilon_i})}{kT}\right] \quad (4.3)$$

where $A^{*} = \left(\frac{4\pi q m^{*} k^{2}}{h^{3}}\right)$ which is termed as the effective Richardson constant. m* is the effective electron mass in oxide. ϕ_B and h are the Schottky barrier height and Planck's constant, respectively. For current conducting through an insulator that is following SC emission, a plot of $\ln(I_g)$ vs $V_g^{1/2}$ must be in a linear form. As shown in Fig. 4-5(b), $\ln(I_g)$ vs $V_g^{1/2}$ accord with linear relationship. This indicates that SC emission is the main conduction mechanism.

FN tunneling is a kind of electric filed assisted tunneling. The current-voltage equation under FN tunneling is given by equation 4.4.

$$J = \frac{q^{3}}{16\pi^{2}\hbar\,\phi_B}E^{2}\exp\left[-\frac{3}{4}\frac{\sqrt{2m^{*}}\phi_B}{q\hbar}\frac{1}{E}\right] \quad (4.4)$$

where ϕ_B is the barrier height between the semiconductor and insulator. If the main carrier transport mechanism is FN tunneling, a plot of $\ln(I_g/V_g^{2})$ vs V_g^{-1} should be in a linear form. Figure 4-5(c) shows that $\ln(I_g/V_g^{2})$ vs V_g^{-1} fits linear relationship which means FN tunneling is also the main mechanisms.

The J-V characteristics was investigated to obtain carrier transport mechanism for the HfN film. It was found that the main transport mechanisms for the diode with the HfN gate insulator are SC emission and FN tunneling. PF emission is not responsible for the diode with the HfN gate insulator. Furthermore, as increasing the measurement temperature, the carrier transport mechanism was not changed.

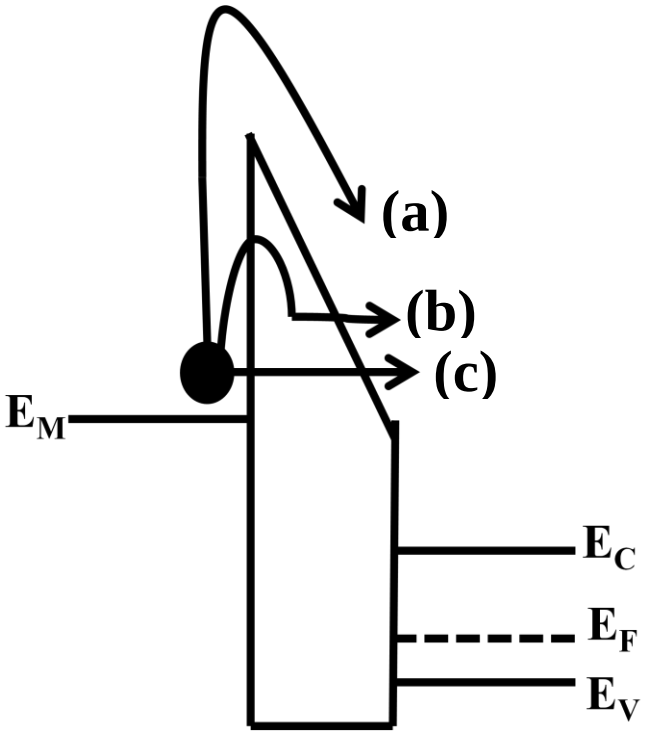


Fig. 4-4 Different carrier transport mechanisms (a) SC emission, (b) PF emission, and (c) FN tunneling.

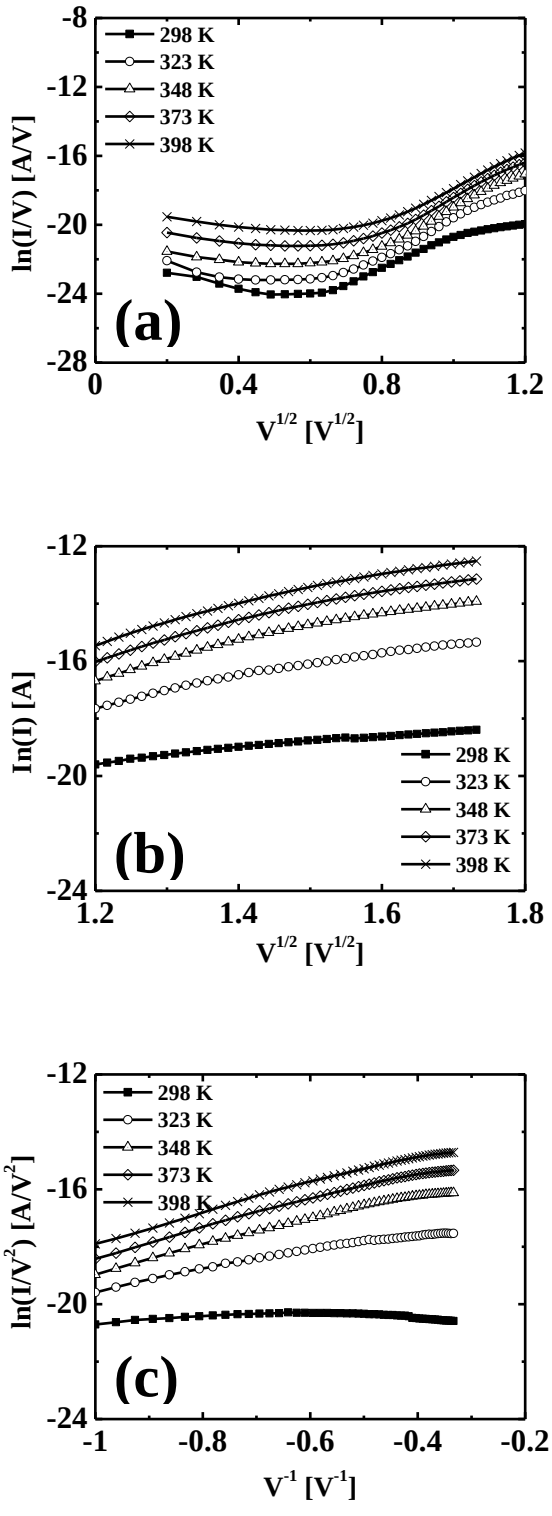


Fig. 4-5 (a) PF emission, (b) SC emission, and (c) FN tunneling plots for the fabricated diode with HfN gate insulator.

4.4 Time dependent dielectric breakdown characteristics

Of all the reliability issues associated with high-k dielectrics, Time dependent dielectric breakdown (TDDB) has been most intensively studied. TDDB is a failure mechanism in MOSFETs, when the gate oxide breaks down as a result of long-time application of relatively electric field. The breakdown is caused by formation of a conducting path through the gate oxide to substrate due to electron tunneling current, when MOSFETs are operated close to or beyond their specified operating voltages. Breakdown is said to occur when the voltage across the dielectric suddenly drops. This test is frequently referred to as the constant voltage time to breakdown test shown in Fig. 4-6.

When we apply the constant voltage, current and times are recorded until breakdown. Results from the test indicate that the time to breakdown is dependent on the value of the current density $J_{inj}=I_{inj}/A$, where the A_{inj} and J_{inj} are an injected current and current density, respectively. When a constant voltage is applied, Q_{BD} can be determined by equation 4.5.

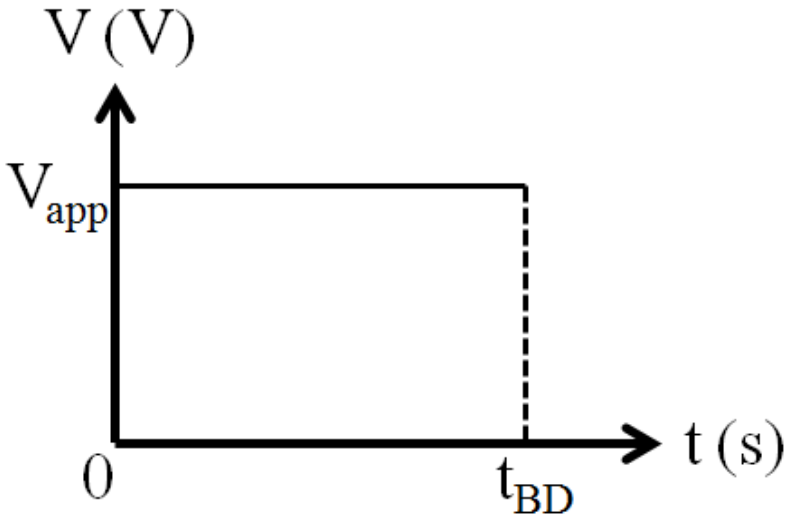


Fig. 4-4 Technique for obtaining the time to breakdown by applying constant voltage.

$$Q_{BD} = \int_0^{t_{BD}} J_{inj}\, dt \qquad (4.5)$$

The reliability of high-k gate dielectrics is dominated by the breakdown of the interfacial layer rather than the high-k layer itself [10]. However, there is no interfacial layer between the HfN gate insulator and Si substrate. Therefore, we evaluated the TDDB characteristic for the HfN gate insulator compared with SiN gate insulator formed on Si directly using a constant voltage stress method at room temperature. A. Nakajima et al. reported TDDB characteristic for SiN formed by atomic layer deposition (ALD) [11]. Figure 4-7 shows the TDDB characteristics for Al/HfN/p-Si(100) at 14.2 MV/cm and 20 MV/cm. Under constant dielectric field (14 MV/cm) stressing for ALD-SiN gate insulator (EOT = 2.6 nm), the breakdown occurred after stressing for 120 s. At the same electric field, there was no breakdown for the HfN film. Moreover, the breakdown did not occur at the high electric filed. The calculated Q_{inj} at 14.2 and 20 MV/cm for 1000 s were 52 and 132 C/cm^2, respectively. For the ALD-SiN film, the Q_{BD} was 8-30 C/cm^2. Comparing with this result, the HfN gate insulator showed better TDDB characteristic. Generally, in the oxide high-k dielectrics, the accumulation and link-up of defects inside oxide high-k dielectric under a constant voltage stress causes the formation of a conductive percolation path which is due to randomized trapping and detrapping of electrons at oxygen vacancy [12]. In case of nitride dielectrics, however, there is no oxygen vacancy that means no change to occur breakdown due to oxygen vacancy. For ALD-SiN, it has better stability of Si-N bonds compared to other SiN. Therefore, the interface trap density of ALD-SiN is smaller than that of the SiO_2 near the conduction band edge. However, the small amount of stress induced leakage current is believed to be caused by the trap in the

ALD-SiN bulk region [11]. On the other hand, as mentioned in section 4.2.3, the HfN film is stable. This is the reason that the HfN gate insulator showed better TDDB characteristic.

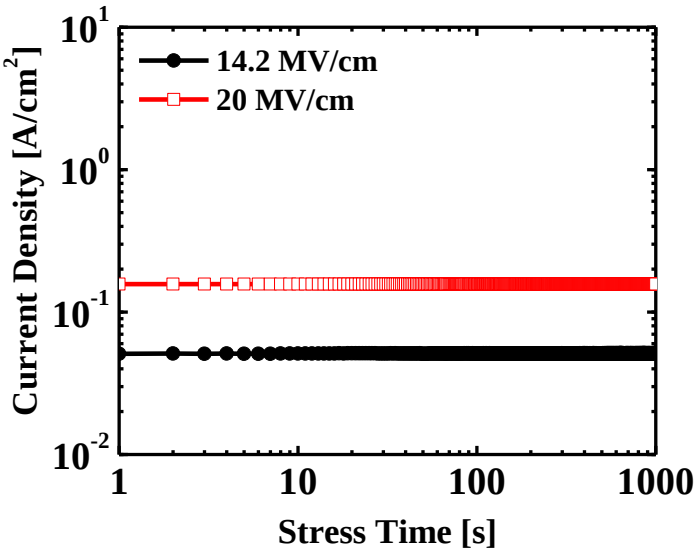


Fig. 4-7 TDDB characteristics at 14.2 and 20 MV/cm for 1000 s.

4.5 Reliability for high electric field bias

A popular method of measuring the neutral trap density buildup is to measure the stress-induced leakage current (SILC), which is widely accepted to be due to trap-assisted tunneling [14-16]. SILC is therefore directly linked to the trap density in the oxide. Furthermore, SILC is important from the reliability point of view when studying the degradation of the insulating films during high-field stress.

Figure 4-8 shows the behavior of SILC, which is the difference in gate leakage current between the before- and after-stressed devices. The 20 MV/cm of constant electric field was biased for 1000 s at room temperature. As shown in Fig. 4-8, even after constant voltage stress, no significant stress induced leakage current was observed. This is consistent with the low charge trapping rate for room temperature.

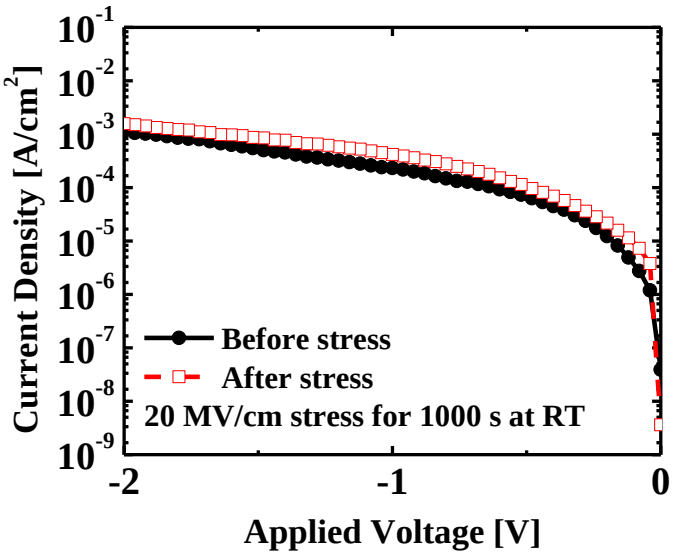


Fig. 4-8 J-V curves before and after 20 MV/cm stress for 1000 s.

4.5 Summary

In this chapter, the reliability for hafnium nitride gate insulator was discussed. The E_A from the measurement temperature dependence of leakage current density, carrier transport mechanism, TDDB characteristic, and SILC was discussed. The obtained results can be summarized as follows.

- Temperature effect on the electrical properties was evaluated. From the measurement temperature dependence of J-V characteristics, the E_A was calculated. The E_A was 1.6 eV for the HfN film. It was found that the HfN film is stable and has lower traps.

- The main transport mechanisms for the diode with the HfN gate insulator are SC emission and FN tunneling. PF emission is not responsible for the diode with the HfN gate insulator. Furthermore, as increasing the measurement temperature, the carrier transport mechanism was not changed.

- TDDB characteristics for Al/HfN/p-Si(100) with the 0.6 nm EOT at 14.2 MV/cm and 20 MV/cm were evaluated. Comparing the SiN film, the HfN gate insulator showed better TDDB characteristic.

- SILC was also investigated for the reliability of the 4 nm thick HfN film. After constant voltage stress about 20 MV/cm for 1000 s, no significant stress induced leakage current was observed. This is consistent with the low charge trapping rate for room temperature.

References

[1] T. Kurose, T. Uchikawa, and S. Ohmi, "ECR Ar/O_2 plasma oxidation of HfN thin films for high dielectric HfO_xN_y formation", *Trans. Mat. Res. Soc. Japan*, vol. 30, pp. 209-212, 2005.

[2] S. Ohmi, T. Kurose, and M. Sato, *"*Ultrathin HfO_xN_y gate insulator formation by electron cyclotron resonance Ar/N_2 plasma nitridation of HfO_2 thin films*", IEICE Trans. Electron*, vol. E89-C, pp. 596-601, 2006.

[3] T. Sano and S. Ohmi, "HfO_xN_y thin-film formation on three-dimensional Si structure utilizing electron cyclotron resonance sputtering", *Jpn. J. Appl. Phys.*, vol. 48, pp. 05DB04-1-4, 2009.

[4] N. Uang, W. K. Henson, and J. J. Wortman, "Analysis of tunneling currents and reliability of NMOSFETs with sub-2 nm gate oxides", *Tech. Dig., Int. Electron Devices Meet*, pp. 453-456, 1999.

[5] S. H. Lo, D. A. Buchanan, Y. Taur, and W. Wang, "Quantum-mechanical modeling of electron tunneling current from the inversion layer of ultra-thin-oxide nMOSFET's", *IEEE Eletron Device Lett.*, vol. 18, pp. 209-211, 1997.

[6] G. Timp, A. Agarwal, F. H. Baumann, T. Boone, M. Buonanno, R. Cirelli, V. Donnelly, M. Foad, D. Grant, M. Green, H. Gossmann, S. Hillenius, J. Jackson, D. Jacobson, R. Kleiman, A. Kornblit, F.Clemens, J. T. C. Lee, W. Mansfield, S. Moccio, A. Murrell, M. O'Malley, J. Rosamilia, J. Sapjeta, P. Silverman, T. Sorsch, W. W. Tai, D. Tennant, H. Vuong, and B. Weir, "Low leakage, ultra-thin gate oxides for extremely high performance sub-100 nm nMOSFETs", *Tech. Dig., Int. Electron Devices Meet*, pp. 930-932, 1997.

[7] C. C. Chen, C. Y. Chang, C. H. Chien, T. Y. Huang, H. C. Lin, and M. S. Liang,

"Temperature-accelerated dielectric breakdown in ultrathin gate oxides", *Appl. Phys. Lett*., vol. 74, pp. 3708-3710, 1999.

[8] C. J. Schug, A. C. Lilly, Jr., and D. A. Lowitz, "Schottky Currents in Dielectric Films", *Phys. Rev. B*, vol. 1, no. 12, pp. 4811-4816, 1970.

[9] W. Y. Jeong and K. M. Yi, "Speckle Defect by Dark Leakage Current in Nitride Stringer at the Edge of Shallow Trench Isolation for CMOS Image Sensors", *IEEE Trans. Electr. Electron. Mater.*, vol. 10, no. 6, pp. 189-192, 2009.

[10] R. Degraeve, B. Kaczer, M. Houssa, G. Groesenken, M. Heyns, J. S. Jeon, and and A. Halliyal, "Analysis of high voltage TDDB measurements on Ta_2O_5/SiO_2 stack", *Tech. Dig., Int. Electron Devices Meet*, pp. 327-330, 1999.

[11] A. Nakajima, H. Ishii, T. Kitade, and S. Yokoyama, "Atomic-Layer-Deposited Ultrathin Si-Nitride Gate Dielectrics - A Better Choice for Sub-tunneling Gate Dielectrics -", *Tech. Dig., Int. Electron Devices Meet*, pp. 28.2.1-4, 2003.

[12] X. Wu, D. B. Migas, X. Li, M. Bosman, N. Raghavan, V. E. Borisenko, and K. L. Pey, "Role of oxygen vacancies in HfO_2-based gate stack breakdown", *Appl. Phys. Lett*., vol. 96, pp. 172901-1-3, 2010.

Chapter 5

Fabrication of MISFET with HfN gate insulator

In this chapter, the fabrication of metal-insulator-semiconductor field effect transistor (MISFET) using HfN gate insulator and its electrical properties are discussed. First, the etching rate for the HfN should be investigated. Finally, the characterization of electrical properties for the fabricated MISFET will be introduced.

5.1 Introduction

Purpose of this study is to fabricate and evaluate a metal-insulator-semiconductor field effect transistor (MISFET) with ultra thin hafnium nitride (HfN) gate insulator. In chapter 3 and 4, we investigated MIS capacitors using HfN gate insulator, and it showed good electrical properties such as 0.5 nm EOT with sufficiently low leakage current density and interface trap density.

In this chapter, we fabricate and evaluate a MISFET with HfN gate insulator. First, the etching rate for the HfN should be investigated. And then, the characterization of electrical properties for the fabricated MISFET will be introduced.

5.2 Fabrication process

We fabricated the MISFET with 4 nm-thick HfN film gate insulator. The fabrication schematic is shown in Fig. 5-1. In appendix A, the used masks are illustrated. The fabrication process is explained as follow. The detailed fabrication process with figures is shown in appendix B.

Fabrication process of MISFET with HfN gate insulator

Substrate : SiN(80 nm)/SiO_2(50 nm)/p-Si(100), $N_A = 1 \times 10^{15}$ cm^{-3}

(1) Activation area patterning (MASK #1)

(2) SiN remove by ICP-RIE

- CF_4/O_2 : 50/10 sccm, 300 s

(3) Channel stopper implantation using BF_3 gas

- Dose : 1×10^{14} cm^{-3}, Acceleration energy : 100 keV

(4) Wet oxidation for field oxide (LOCOS)

- 1150^{o}C/30 min

(5) SiN remove by H_3PO_4 @160^{o}C

(6) Wet oxidation to protect S/D

- 850^{o}C/5 min

(7) S/D diffusion region patterning (MASK #2)

(8) S/D implantation using PH_3 gas

- Dose : 5×10^{15} cm^{-3}, Acceleration energy : 20 keV

(9) O_2 ashing by ICP-RIE

- O_2 : 50 sccm, 300 s

(10) HfN film deposition

- Thickness : 4 nm, FGA : 400^{o}C/30 min

(11) Al deposition to protect the insulator

(12) Contact hole patterning (MASK #3)

(13) Al remove (contact hole region) by H_3PO_4/HNO_3 = 50 ml : 3 ml @40^{o}C

(14) HfN remove (contact hole region) by 1% DHF

(15) Remove PR by acetone

(16) Al deposition for electrode pad

(17) Pad electrode patterning (MASK #4)

(18) Al remove by H_3PO_4/HNO_3 = 50 ml : 3 ml @40^{o}C

(19) Remove PR by acetone

(20) Al deposition (back side)

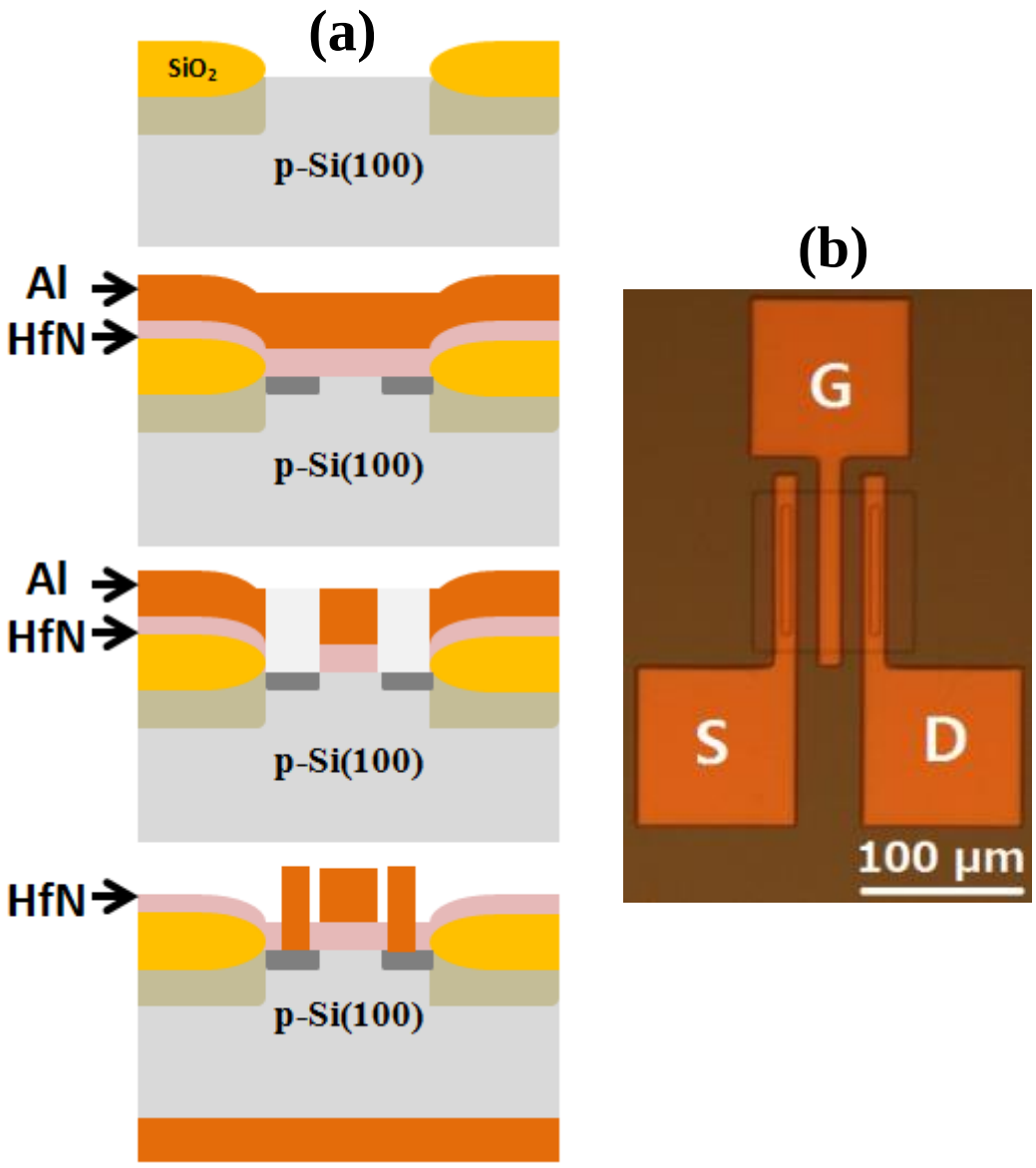


Fig. 5-1 (a) Schematic of MISFET fabrication process and (b) microscope image for the fabricated MISFET.

5.3 Investigation of etching rate for HfN film

Before the fabrication of MISFET, the etching rate for the HfN film should be investigated. First, the 4 nm-thick HfN film was deposited by ECR plasma sputtering in Ar/N_2 ambient. At that time, the pre-sputtering was carried out before the deposition of the HfN film using Ar gas for 10 min. The post deposition anneal (PDA) was also carried out at 400^oC for 30 min in forming gas ($N_2/4.9\%H_2$) ambient for comparison utilizing RTA system. The flow rate of gases was approximately 1 SLM. The HfN film can be etched by DHF or a mixed solution ($HF : H_2O_2 : H_2O = 1 : 2 : 40$) [1]. In this time, the HfN film was etched by 1% DHF. The HfN films were dipped in 1% DHF until the surface became hydrophobic. The result is tabulated in Table 5-1. After 15 s, the surface became hydrophobic. The HfN film was etched perfectly by 1% DHF for 15 s. To confirm this result, we deposited the 4 nm thick HfN film and then etched for 5 - 25 s. Next, the top and bottom Al electrodes were evaporated. Finally, we compared J-V characteristics with as-cleaned sample (do not deposit the HfN film). The schematic and J-V characteristics showed in Fig. 5-2 and 5-3, respectively. As shown in Fig. 5-3, after 15 s etching, the currents densities were almost same with as-cleaned sample. However, the current densities were little bit different due to the effect of DHF in low electric field. From J-V characteristics, we confirmed the etching condition of the 4 nm thick HfN film. Using this condition, we fabricated the MISFET with 4 nm thick HfN film gate insulator.

Table 5-1 Etching rate for the HfN film.

Etching time by 1% DHF	5 s	10 s	15 s	20 s	25 s
Surface property	hydrophilic	hydrophilic	hydrophobic	hydrophobic	hydrophobic

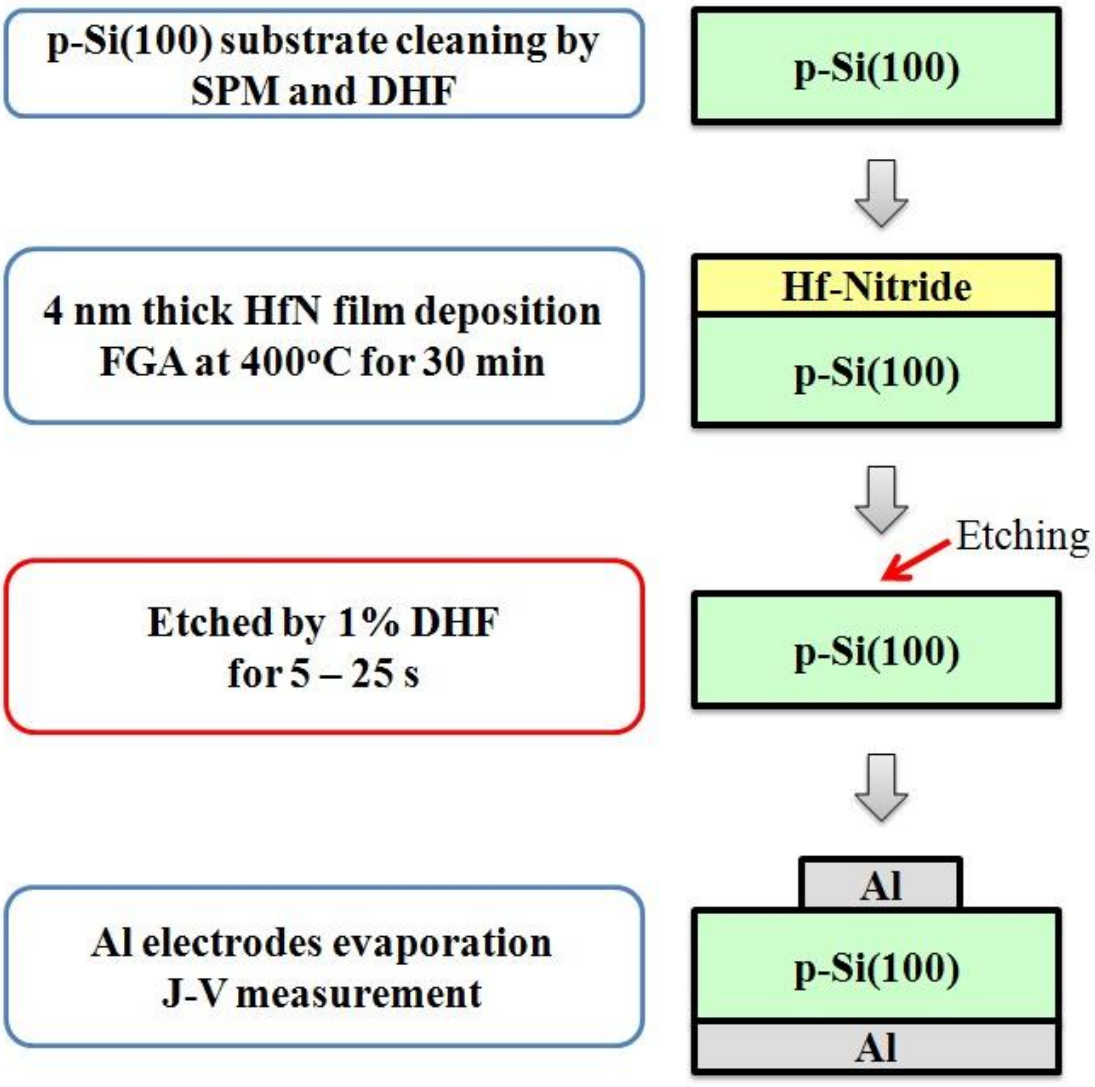


Fig. 5-2 Schematic of etching process for the 4 nm-thick HfN film

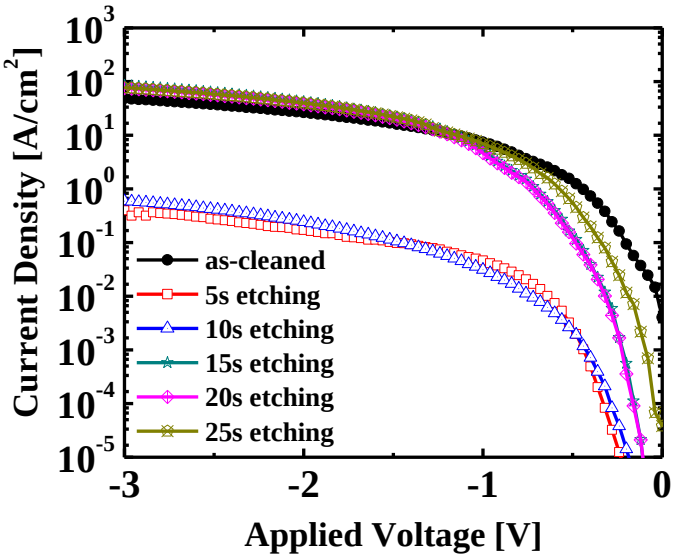


Fig. 5-3 J-V characteristics with various etching conditions.

5.4 Device characteristics

First, the typical I_D-V_D characteristic of the fabricated MISFET is shown in Fig. 5-4. It is a first report of the MISFET characteristics with the HfN gate insulator.

Next, the I_D-V_G characteristic with W/L = 90/5 μm are shown is Fig. 5-5(a). Furthermore, the C-V characteristic is also shown in Fig. 5-5(b). The C-V characteristic was obtained in the test element group (TEG) of the same sample. The EOT calculated at 100 kHz was 0.7 nm. This value is lower compared to the result in chapter 3. Because, the MISFET was fabricated using LOCOS. It means that the activation region is surrounded by SiO_2. TEG is also located in the same place. Therefore, the value of EOT was affected.

Using this capacitance, the slope of the $I_D^{1/2}$-V_G, and equation 5.1, the saturation mobility was calculated [2].

$$\mu_{sat} = a^2 \times \sqrt{\frac{2L}{WC_{ox}}} = a^2 \times \sqrt{\frac{2L^2}{C_{measured}}} \tag{5.1}$$

The saturation mobility, On/Off ratio, and subthreshold swing at W/L = 90/5 μm were 32.4 cm^2/Vs, 10^4, and 180 mV/dec., respectively. Furthermore, the field-effect mobility in the linear regime is extracted from the transconductance, which is defined as

$$g_m = \frac{\partial I_D}{\partial V_G} \tag{5.2a}$$

$$g_m = \frac{I_{D0} - I_{D2}}{V_{G0} - V_{G2}} \ (\text{At } V_{G1}) \tag{5.2b}$$

For small V_D, the mobility in the linear regime is calculated from the relationship.

$$\mu_{lin} = \frac{Lg_m}{WC_{ox}V_D} \tag{5.3}$$

The mobility in the linear regime was 63.5 cm^2/Vs. At low effective fields, carrier mobility is dominated by Coulomb scattering, which is more effectively screened at higher effective fields. At moderate effective fields, phonon scattering determines the mobility. Finally, in the high-effective field regime, surface roughness scattering limits the carrier mobility. The universal nature of the carrier mobility is attributed to the phonon and surface roughness mobilities. However, these values are not sufficient. Actually, the source and drain region should be overlapped with gate. For this reason, the calculated value became lower. Therefore, the effective gate length should be considered to obtain accurate value.

To calculate the effective gate length, the parameter extraction occurred. We measured the I_D-V_D characteristics with various gate lengths from 10 to 2μm. Figure 5-6 shows the equivalent circuit of n-MISFET. Using this schematic, the effective channel length is given by

$$L_{chan} = L_{MASK} - 2L_{overlap} \tag{5.4}$$

where L_{MASK} is a design value and $L_{overlap}$ is a overlapped length between S/D region and gate. From Fig. 5-6, the effective can be calculated by

$$R_{measured} = \frac{V_{DS}}{I_{DS}} + R_{S/D} = A \cdot \left(L_{MASK} - 2L_{overlap}\right) + R_{S/D} \tag{5.5}$$

where A is a constant and $R_{S/D}$ is a resistivity of S/D. We already measured the I_D-V_D characteristics with various gate lengths from 10 to 2 μm. The $R_{S/D}$ can be obtained

from the approximation slope of the measured values with various gate lengths. Figure 5-7 shows the $R_{measured}$-L_{MASK} plot of the MISFET. From 10 to 2 μm, the gradual channel approximation (GCA) can be applied. Therefore, we can obtain accurate value of $L_{overlap}$. From Fig. 5-7, it was found that the $2L_{overlap}$ was 1 μm. Effective channel length was reduced about 1μm due to the lateral diffusion of the source/drain dopant ions.

Next, we compared the I_D-V_G characteristics for W/L = 90/10 and 90/5 μm as shown in Fig 5-8. As increased V_D from 0.05 to 1 V, off-current was increased. For the reason, on/off ratio also was decreased. The electric field induced from drain affected to the off-current. When the gate voltage is below V_{th}, the p-Si substrate forms a potential barrier between n^+ source and drain and limits the electron flow from source to drain. In the long-channel case, the increase in depletion layer region width of the drain junction will not affect the potential barrier height. Nevertheless, when the channel length is short enough, the increase in drain voltage decreases the potential barrier height. As a result, subthreshold current increases [2]. Therefore, in case of W/L = 90/5 μm, the subthreshold current increased larger compared to W/L = 90/10 μm.

Figure 5-9 shows the I_G-V_G characteristics for W/L = 90/10 and 90/5 μm with various drain voltages. When the drain voltage increased, the gate currents also increased. Especially, the gate current increased dramatically at the V_D = 1 V. It is related to the result of subthreshold current. As the drain voltage increased, the drain and gate currents increased. Fig. 5-10 shows log(I_D)-V_G and g_m-V_G characteristics against V_G for the present device at V_D of 1 V. The V_{th} was 0.05 V. The On/Off ratio and subthreshold swing at W/L = 90 μm/5 μm were ~10^3 and 200 mV/dec., respectively. In addition, maximum drain-source saturation current ($I_{DS,sat}$) and peak extrinsic

transconductance (eq. 5.2b) were 20.2 μA/μm and 20.5 mS/mm, respectively. We obtained $R_{S/D}$ = 36 kΩ-μm from Fig. 5-7. This high value leads to the reduction of electrical properties. With relatively refinements to the gate-to-channel separation, reduction of S/D resistance, and optimized fabrication process, the improvement of electrical properties should be expected.

In case of diode with HfN gate insulator, the electrical properties are better compared with other insulator. However, after applying to the MISFET, the electrical properties fell short of the expectation. Therefore, the overall process needs to consider and fabrication process should be carried out more carefully.

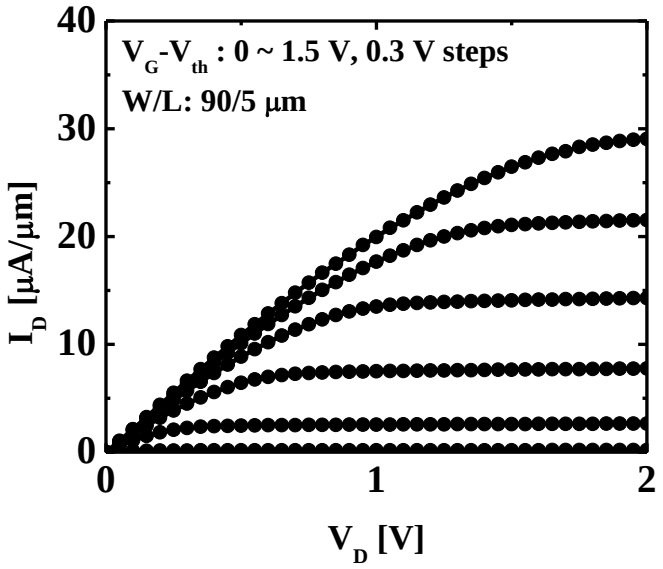


Fig. 5-4 I_D-V_D characteristic of the fabricated MISFET.

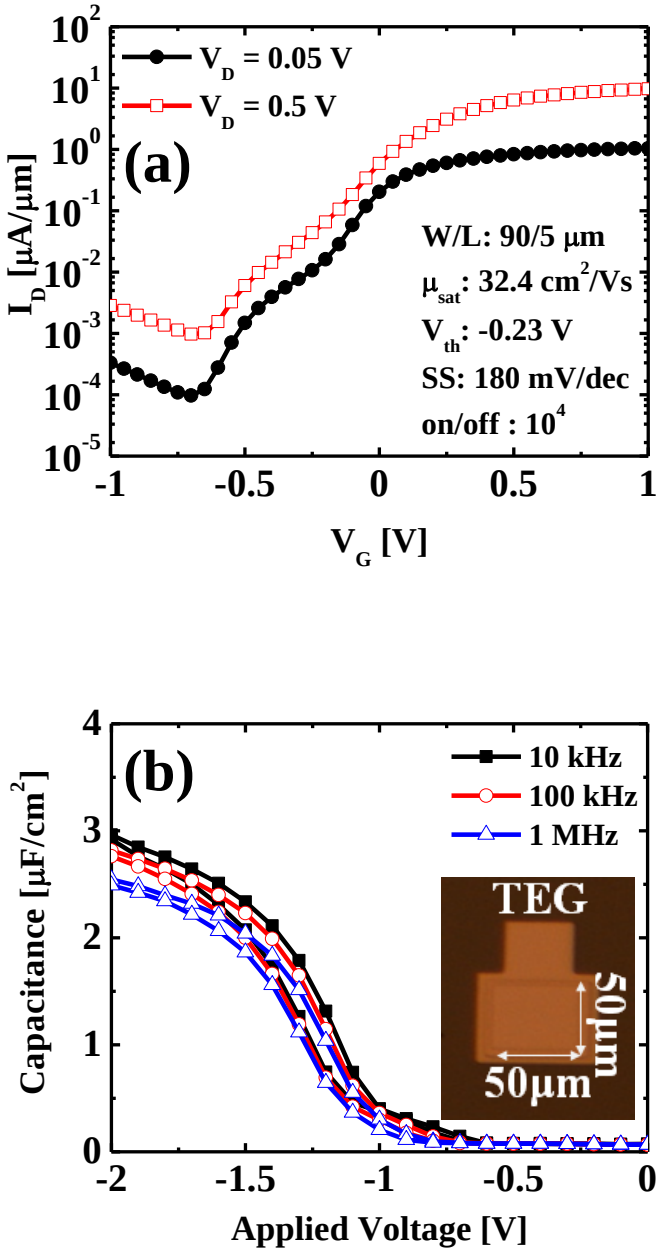


Fig. 5-5 (a) I_D-V_G characteristic of the fabricated MISFET and (b) C-V characteristic in the TEG of the same sample.

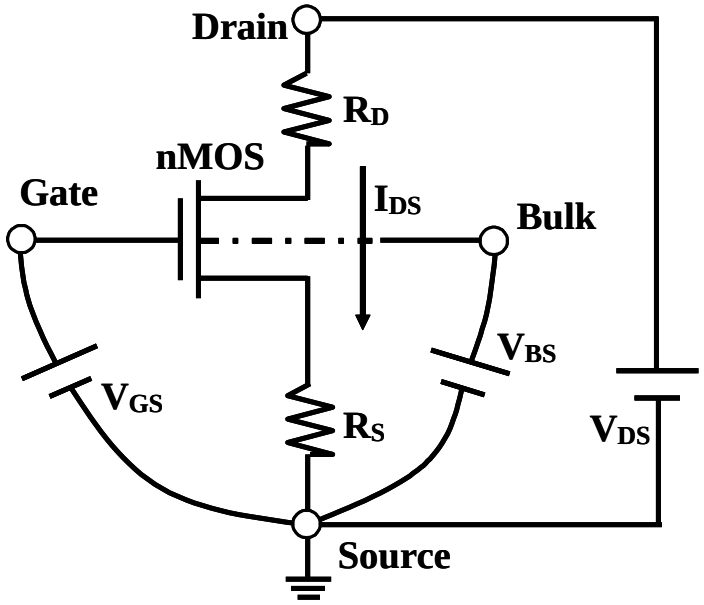


Fig. 5-6 Equivalent circuit of n-MISFET.

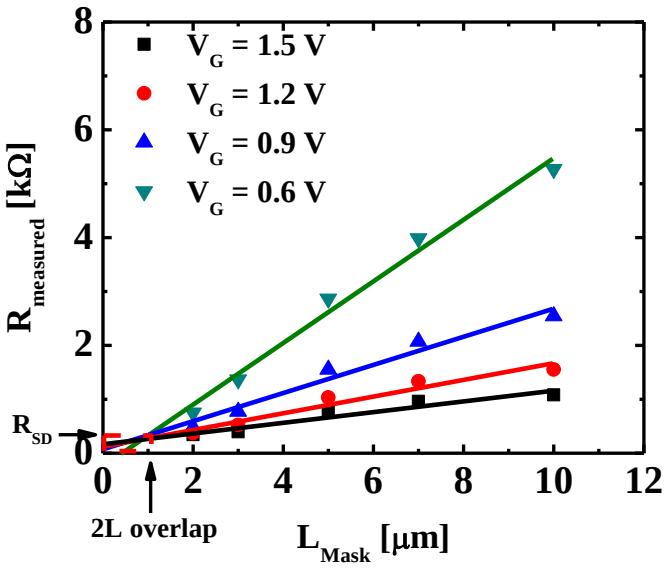


Fig. 5-7 $R_{measured}$-L_{MASK} plot of the MISFET.

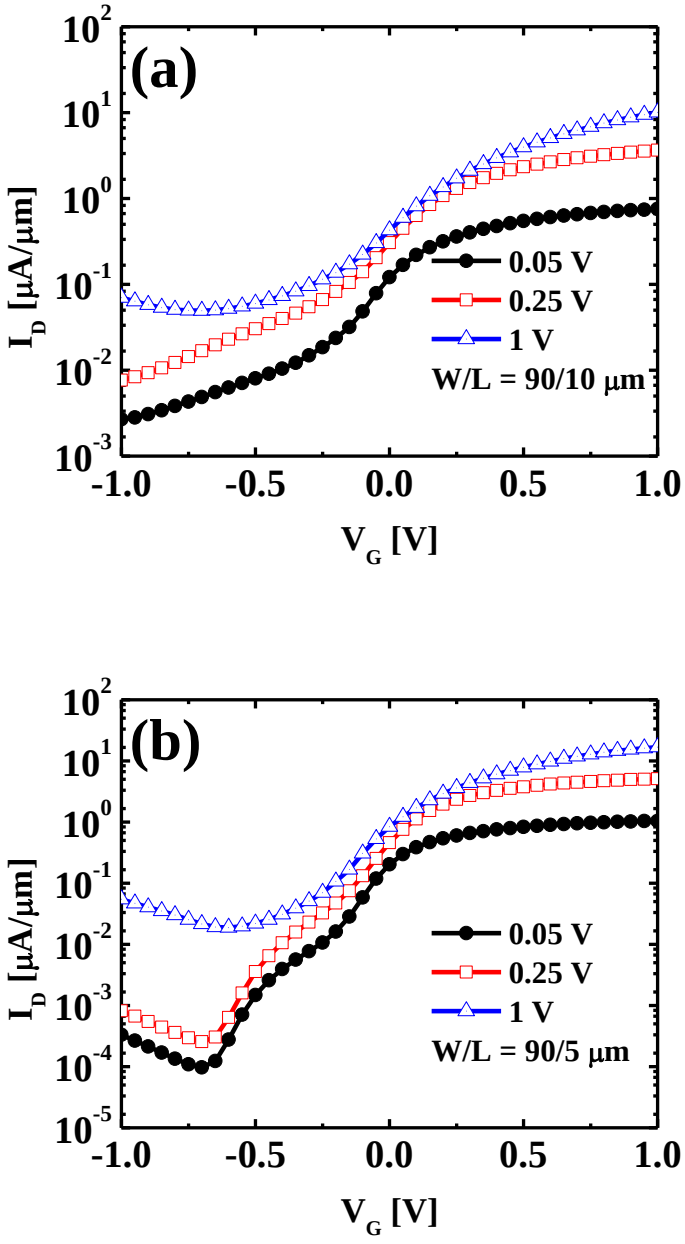


Fig. 5-8 I_D-V_G characteristics for (a) W/L = 90/10 and (b) 90/5 μm.

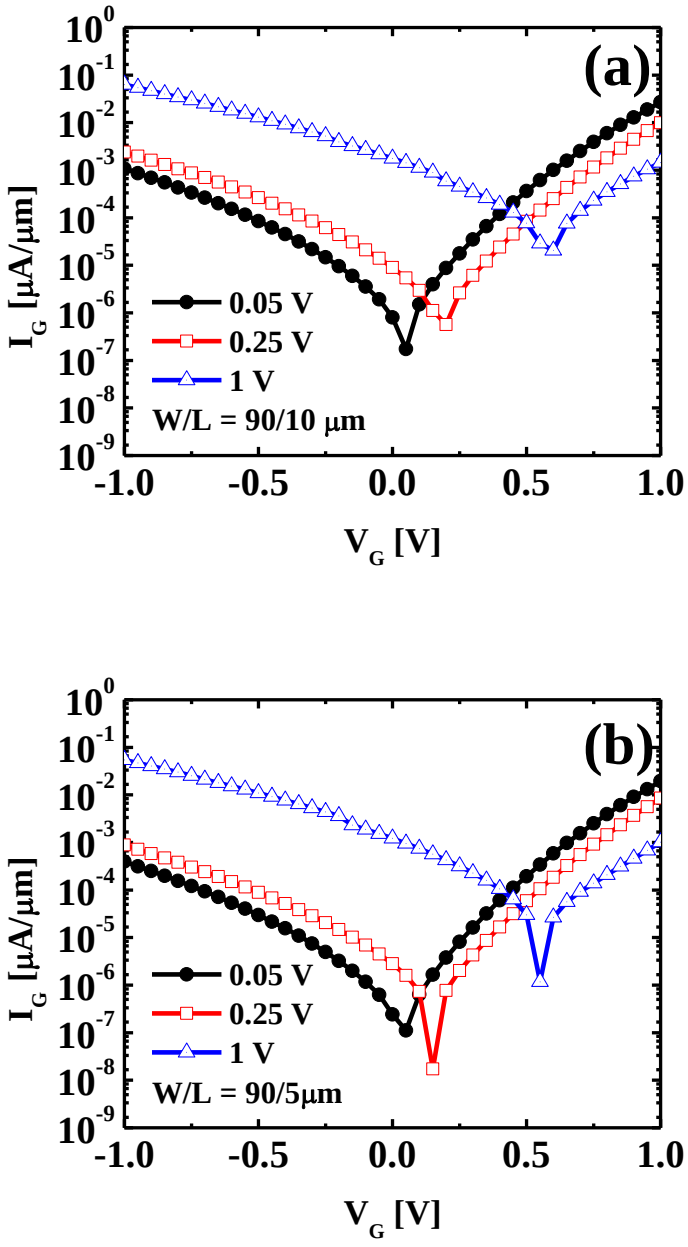


Fig. 5-9 I_G-V_G characteristics for (a) W/L = 90/10 and (b) 90/5 μm.

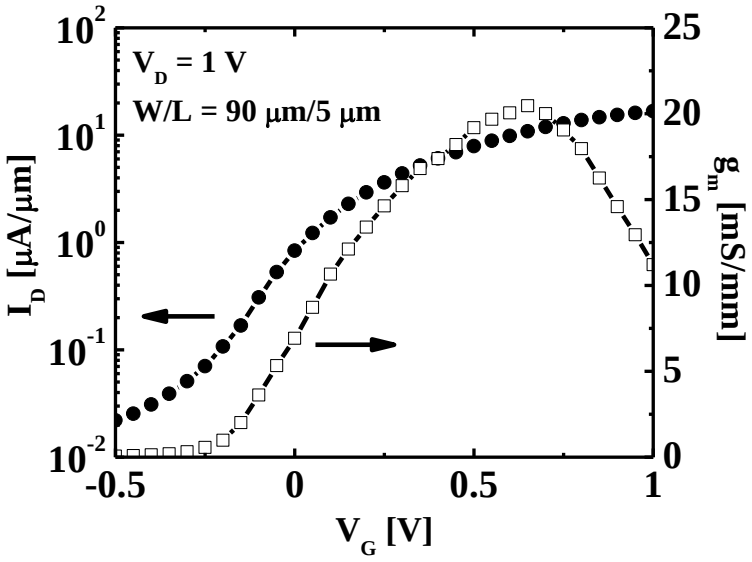


Fig. 5-10 Log-scale I_D-V_G and g_m-V_G characteristics of the MISFET (W/L = 90 μm/5 μm) with HfN gate dielectric.

5.5 Summary

The MISFETs with 4 nm thick HfN gate insulator were fabricated for the first time. Moreover, the etching rate for the HfN film was investigated. The obtained results are summarized as follows.

- The etching rate for the HfN film was investigated. In this time, the HfN film was etched by 1% DHF. After etching for 15 s, it was found that the HfN film was etched perfectly by 1% DHF.

- The MISFETs with 4 nm thick HfN gate insulator were fabricated and evaluated at first time. In the I_D-V_D characteristic, it was found that the MISFETs showed a traditional operation. However, the saturation mobility, On/Off ratio, and subthreshold swing at W/L = 90/5 μm were 63.5 cm^2/Vs, 104, and 180 mV/dec., respectively. In particular, the n-MISFET exhibits $I_{DS,sat}$ = 20.2 μA/μm and g_m = 20.5 mS/mm. The improvement of fabrication process will realize good device characteristics.

References

[1] C. S. Lai, S. K. Peng, T. M. Pan, J. C. Wang, and K. M. Fan, "Work Function Adjustment by Nitrogen Incorporation in HfN_x Gate Electrode with Post Metal Annealing", *Electrochem. Solid-State Lett.*, vol. 9, no. 7, pp. G239-G241, 2006.

[2] S. M. Sze, "Semiconductor Devices, Physics and Technology", 2nd, John Wiley & Sons, 2001.

Chapter 6

Conclusions

In this chapter, the results obtained in this study are summarized. The meanings and significance of this study are clearly elucidated from the obtained results. And then, future prospects of this study are also pointed out to help one improve the device performances.

6.1 Main results obtained from this study

Recently, the scaling of equivalent oxide thickness (EOT) is a great challenge in the complementary metal oxide semiconductor (CMOS) technology. For a small EOT, the use of high-*k* gate dielectrics which have high dielectric constant than that of SiO_2 has been required. However, most of the high-k dielectrics contain oxygen, which leads to the interfacial layer formation. It leads to the limitation of EOT scaling down. Therefore non oxygen gate insulator should be researched. That is, the object of my study was fabrication of ultrathin HfN gate insulator. In this thesis, in order to fabricate devices with ultrathin HfN gate insulator, a number of trial-and-errors-approaches were performed in fabrication processes and related technologies were proposed. The obtained results from this study are summarized as follows.

- The HfN films were deposited by ECR plasma sputtering method with various Ar/N_2 flow ratio. From the C-V and J-V characteristics, we confirmed that the deposited HfN film showed insulating property. At Ar/N_2 = 20/8 sccm, the capacitance was the highest in accumulation and the leakage current was low enough.

- The effect of hydrogen annealing for HfN gate insulator was investigated. The capacitance was increased and the hump was disappeared by FGA compared to nitrogen annealing. The EOT was 1.12 at 400^oC FGA for 30 min. However, it was found that there is an interfacial layer after FGA.

- We investigated the dependence of deposition gas pressure and pre-sputtering condition. From Ar pre-sputtering, the EOT of 0.6 nm was obtained. Through the

cross-sectional TEM image, the thickness of the 400^{o}C FGA HfN film was 4 nm. We confirmed no interfacial layer also. The relative dielectric constant for 400^{o}C FGA sample was obtained as 26. The obtained value of the relative dielectric constant is closed to the reported value. The D_{it} was as low as an order of 10^{11} $cm^{-2}eV^{-1}$.

- Atomic concentrations for Hf, Si, N, and O were calculated by XPS the depth profile of. It was found that less than 5% oxygen occupied in the film. In the HfN film, the atomic concentration ratio of hafnium and nitrogen was confirmed as 1:1.2 by the XPS depth profile.

- In order to reduce EOT for HfN gate insulator, we investigated dependence of film thickness through deposition time from 60 s to 15 s. As decreased the deposition time, the EOT of 0.5 nm was obtained at 500^{o}C FGA for 20 min.

- From the measurement temperature dependence of J-V characteristics, the E_A was calculated. The E_A was 1.6 eV for the HfN film. It was found that the HfN film is stable and has lower traps.

- The main transport mechanisms for the diode with the HfN gate insulator are SC emission and FN tunneling. PF emission is not responsible for the diode with the HfN gate insulator. Furthermore, as increasing the measurement temperature, the carrier transport mechanism was not changed.

- TDDB characteristics for Al/HfN/p-Si(100) at 14.2 MV/cm and 20 MV/cm were

evaluated with the 0.6 nm EOT HfN film. Comparing the SiN film, the HfN gate insulator showed better TDDB characteristic. Furthermore, after constant voltage stress about 20 MV/cm for 1000 s, no significant stress induced leakage current was observed.

- The etching rate for the HfN film was investigated. In this time, the HfN film was etched by 1% DHF. After etching for 15 s, it was found that the HfN film was etched perfectly by 1% DHF.

- The MISFETs with 4 nm-thick HfN gate insulator were fabricated and evaluated at first time. In the I_D-V_D characteristic, it was found that the MISFETs showed a traditional operation. The saturation mobility, On/Off ratio, and subthreshold swing at W/L = 90/5 μm were 63.5 cm^2/Vs, 10^4, and 180 mV/dec., respectively.

All the results briefed above are demonstrated in the devices with ultrathin HfN gate insulator. Finally, it can be concluded from the results that this HfN gate insulator is a promising candidate for the next generation CMOS application.

6.2 Future prospects

In this study, the ultrathin HfN gate insulator showed good electrical properties. Above all, 0.5 nm thick EOT was obtained using nitride insulator in the world's first. This point is very encouraging. And it shows great promise in the high-k field.

From this result, a few proposals are addressed.

- Recently, the interface roughness between gate insulator and silicon substrate is one of the issues in the MOSFETs as well as the interface roughness between gate insulator and electrode. Therefore, interface roughness should be investigated. Furthermore, as improving the roughness of the film, the interface trap density will be deceased.

- When the HfN film was annealed over 600^{o}C, the EOT was increased. It means that the thermal stability should be improved. HfN electrode has a superior thermal stability. Therefore, it is expected that HfN/HfN/Si structure will show good electrical properties. The former HfN is a metal, and the latter HfN is an insulator.

- The 0.5 nm EOT was achieved using ECR plasma sputtering. The value is a requested one in 2022 from the ITRS. However, the fabricated device is 2-dimensional structure. Therefore, the HfN gate insulator should be investigated on 3-dimensional structure.

Acknowledgement

First of all, the author would like to thank his supervisor at Tokyo Institute of Technology (TIT), Associate Professor Shun-ichiro Ohmi for his support, excellent guidance, and continuous encouragement throughout my doctoral course. He gave me a precious chance to study in Japan. The author also would think that the basic attitudes and the ways of thinking as a researcher, which have been educated by him. He also gave me useful advice from his experience and knowledge. The author thinks that it was impossible to obtain doctor's degree without his advice. Sometimes, I really did not want to talk him because of my low confidence and knowledge. However, he had been pushed my back without giving up. The author also would like to thank Professor B. E. Park (supervisor at University of Seoul in the author's master course) who recommended continuing study in Japan and introduced to Associate Professor Shun-ichiro Ohmi. He always gave helpful advice with his full of knowledge in the major and teaching. Sometimes, when he came to Japan, he always visit to me and made me confident. The author would like to thank Professor Hiroshi Ishiwara and Professor Eisuke Tokumitsu for their excellent advice and useful discussion. The author also would like to thank Professor Jun-ichi Hanna, Professor Kazuo Tsutsui, Associate Professor Masahiro Watanabe, Associate Professor Tomoyuki Miyamoto, and Dr. Masaru Shimada for reviewing this thesis with their clear directions and favorable discussions. The author would like to thank Associate Professor Sung-Min Yoon (Kyounghee University) for useful advice. The author would like to thank Professor Hiroshi Iwai and Associate Professor Kuniyuki Kakushima for helpful comments. The author would like to thank Mr. D. Shoji for his support. The author would like to thank Dr. Shun Koh (Tokyo Electron) and Mr. Jumpei Ishikawa (Olympus)

for training experimental skills. Especially, the author would like to thank Dr. Takahiro Sano (Fuji Film) for his special advice and help. The author would like to thank Dr. Joo-won Yoon (Samsung Display), Dr. Jeong-hwan Kim (Samsung Display), and Dr. Gwang-gun Lee (Samsung Display) for kind discussion and support. When the author came in Japan, they gave so many helps. The author would like to thank all members Dr. Min Liao, Dr. Yoshiaki Kikuchi (Sony), Mr. Yuichiro Kimura (NTT), Mr. Takato Ohnishi (Panasonic), Mr. Kousuke Kamino (Sony), Mr. Yasuhiko Yoshimura, Mr. Jun Arima (TDK), Mr. Kazuaki Takayama (Nippon Signal), Mr, Masayuki Takahashi, Mr. Nitthi Atthi, Mr. Kousuke Yuzawa, Ms. Elham Heidari, Mr. Akihiro Yoshimi, Mr. Wu Xiaopeng, Mrs. Tomoko Mizutani and Mrs. Mami Goto in Ohmi laboratory. Every member is very kind and nice. The author did not mention above, the author really would like to thank Dr. Younguk Song (Samsung LSI). Actually, the author gave many discussions and help for him. However, he also did in like manner. And the author waits for his wedding day. The author would appreciate to Mr. Deahee Han for his kind friendship and active discussions. The author cannot stop appreciating to many friends, senior and junior in Korea. Especially, the author would like to thank Mr. Hyungjin Park, Mr. Wooyeol Kim, and Mr. Yeonghyeok Kim for their friendship. Moreover, the author would like to thank Ms. Jinsook Ryu (LGE) for her support and encouragement.

Finally, the author would like to give thanks his parents - Father: Jinnyeon Han, Mother: Jongak Jeong - and Sister Mijeong Han for supporting him to keep studying until now. And the author would like to give thanks my Ms. Youjin Kim and pretty Yoreum for their love and love. Without their support, it could have not been here and obtained the precious chance of studying in Japan.

Publication lists

Papers

[1] **Huiseong Han** and Shun-ichiro Ohmi,
"Hafnium-Nitride Gate Insulator Formed by Electron Cyclotron Resonance Plasma Sputtering", *IEICE Electron. Exp.*, **9**, 16, pp. 1329-1334, 2012.

[2] **Huiseong Han**, Daehee Han and Shun-ichiro Ohmi,
"Potential of MISFET with HfN gate dielectric formed by ECR plasma sputtering", *IEEE Electron. Lett.*, **49**, 7, pp. 500-501, 2013.

Domestic conferences and symposium

[1] **H. S. Han**, T. Sano, Y. U. Song, and S. Ohmi,
"Electrical Properties of Hf/HfSiON/p-Si(100) Structure MIS Capacitor by Using ECR-Sputtering", *The 57th JSAP Spring Meeting*, 19a-P11-23, p. 13-105, 2010.

[2] **H. S. Han** and S. Ohmi,
"Effect of Post Deposition Annealing on Electrical Characteristics of Hf-Nitride Gate Insulator", *2011 G-COE PICE International Symposium*, 2011.

[3] **H. S. Han** and S. Ohmi,
"Electrical Properties of Hf-Nitride Insulator Formed by ECR-Sputtering", *The 58th JSAP Spring Meeting*, 25p-KW-17, 2011.

[4] **H. S. Han** and S. Ohmi,
"Effect of FGA on Electrical Characteristics of HfxNy Insulator", *The 72th JSAP Fall Meeting*, 31p-Q-4, p. 13-068, 2011.

[5] **H. S. Han** and S. Ohmi,
"Evaluation of ultra-thin HfN gate dielectric for low EOT", *The 59th JSAP Spring*

Meeting, 17p-A4-3, p. 13-084, 2012.

[6] **H. S. Han** and S. Ohmi,
"Reliability of HfN Gate Insulator formed by ECR-sputtering", *The 73th JSAP Spring Meeting*, 11a-PB1-11, p. 13-053, 2012.

[7] **H. S. Han** and S. Ohmi,
"Hafnium-Nitride Formation as a Gate Dielectric toward Equivalent Oxide Thickness of 0.5 nm or below", *IEEE EDS WIMNACT 37*, 2013.

[8] D. H. Han, **H. S. Han**, and S. Ohmi,
"Impact of Si surface roughness on MOSFET performance with ultra-thin HfON gate insulator formed by ECR plasma oxidation of HfN", *The 73th JSAP Spring Meeting*, 11a-F8-5, p. 13-035, 2012.

Related research

Papers

[1] **Hui-Seong Han**, Ho-Seung Jeon, Gwang- Geun Lee, Kwi-Jung Kim and Byung-Eun Park,
"Electric Properties of PVDF-TrFE (75/25) Thin Films with a Lanthanum Zirconium Oxide Buffer Layer for FeRAM", *J. Korean Phys. Soc*. **55**, pp. 898-901, 2009.

[2] Gwang-Geun Lee, **Hui-Seong Han**, Yun-Soo Choi, Byung-Eun Park,
"Electrical properties of metal-ferroelectric- insulator-semiconductor field effect transistors (MFIS-FETs) using the polyvinylidene fluoride trifluoroethylene (P(VDF-TrFE))/ZrO_2/Si structure", *Journal of the Ceramic Society of Japan*, **118**, 1383, pp. 1013-1016, 2010.

International conferences

[1] **Hui-Seong Han**, Gwang-Geun Lee, Ho-Seung Jeon, and Byung-Eun Park,
"The Electrical Properties with Thickness Variation of Au/PVDF-TrFE/LaZrOx/Si(100) Structure", *20 th International Symposium of Integrated Ferroelectrics*, 4-382-P, 2008.

[2] **Hui-Seong Han**, Kwi-Jung Kim, Ho-Seung Jeon, and Byung-Eun Park,
"Electrical Properties of Au/PZT/LaZrOx/Si Structure",
9 th European Conference on Applications of Polar Dielectrics, P60, 2008.

[3] **Hui-Seong Han**, Ho-Seung Jeon, Kwi-Jung Kim, and Byung-Eun Park,
"Electrical Properties of MFIS-FET with PVDF-TrFE (75/25) Thin Film", *The 7th Korea-Japan Conference on Ferroelectricity*, P-08-28, 2008.

Appendix A Mask for MISFET

Mask #1

Activation Region

100 μm x 100 μm

Gate width

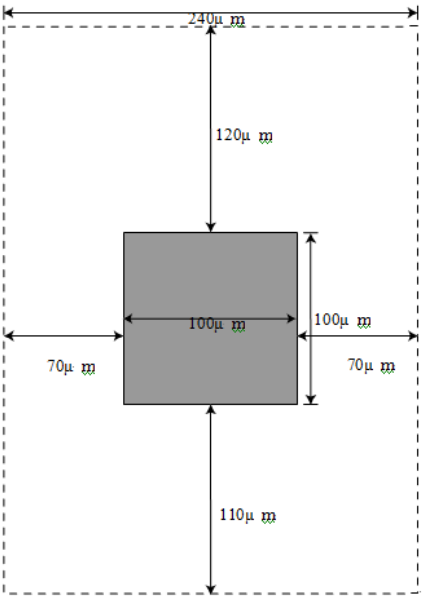
100 μm

Gate length

1, 2, 3, 5, 7, 10μm

— Mask #1

····· Device size



Mask #1 for MISFET

Mask #2

Activation Region

100 μm x 100 μm

Gate width

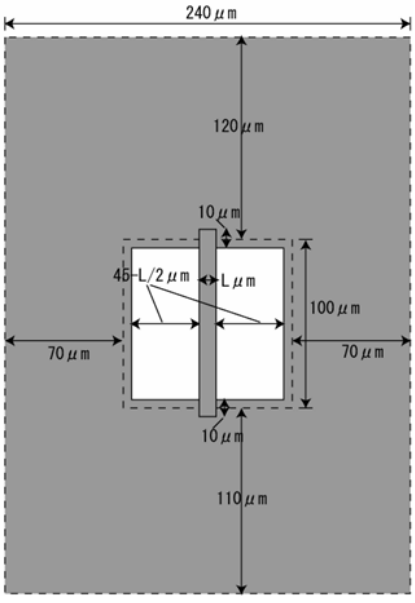
90 μm

Gate length

1, 2, 3, 5, 7, 10μm

— Mask #2

····· Mask #1



Mask #2 for MISFET

Mask #3

Activation Region

100 μm x 100 μm

Gate width

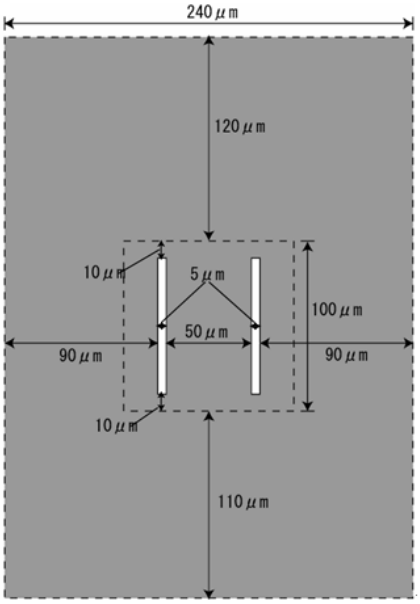
90 μm

Gate length

1, 2, 3, 5, 7, 10μm

— Mask #3

····· Mask #1



Mask #3 for MISFET

Mask #4

Activation Region

100 μm x 100 μm

Gate width

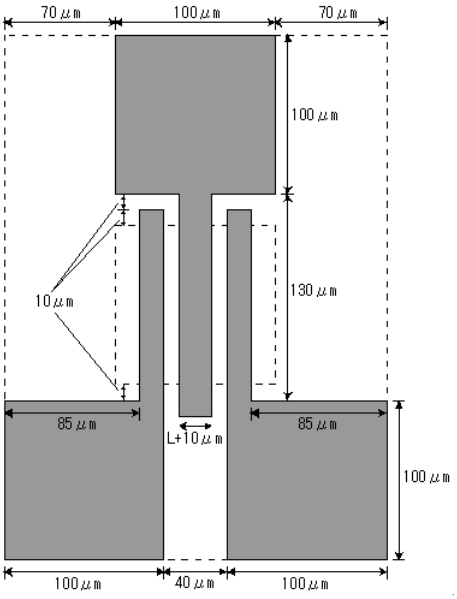
100 μm

Gate length

1, 2, 3, 5, 7, 10μm

— Mask #4

····· Mask #1



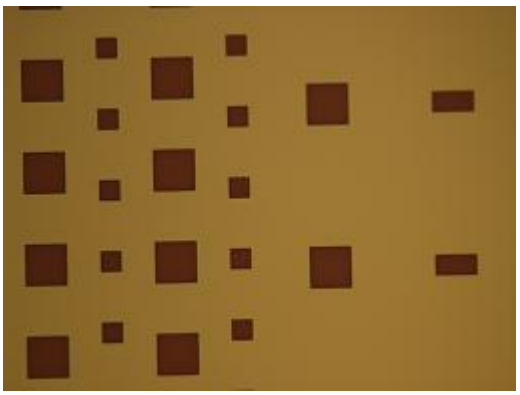
Mask #4 for MISFET

Appendix B Planar MOSFET process

Substrate: SiN(80 nm)/SiO_2(50 nm)/p-Si(100) $N_{sub}=10^{15}$ cm^{-3}

1. SPM, DHF cleaning

2. Activation area patterning (Mask #1)



3. SiN removal by ICP-RIE

   CF_4/O_2: 90/10 sccm

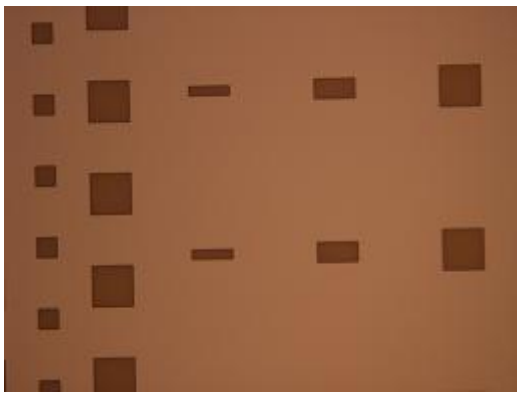
   Etching time: 30 s

4. Channel stopper implantation

   Source gas: BF_3

   Dose: 1 x 10^{14} cm^{-2}

   Beam energy: 100 keV



5. SPM, DHF cleaning

6. Wet oxidation for field oxide

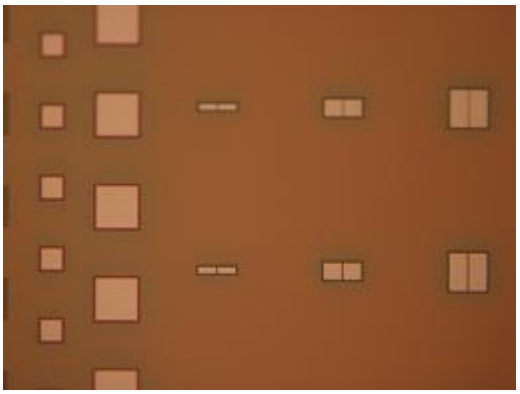
   1150°C/30 min

7. SiN removal

   H_3PO_4 @ 160°C/20 min

8. SiO_2 removal

   DHF: 15 min



9. Wet oxidation for field oxide

   850°C/10 min

10. S/D diffusion region patterning (Mask #2)

11. S/D diffusion region implantation

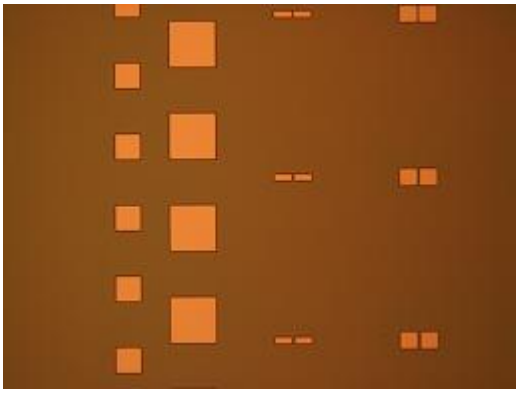
   Source gas: PH_3

   Dose: 5 x 10^{15} cm^{-2}

Beam energy: 20 keV

12. photo-resist removal

SPM: 10min, rinse: 10min



13. O_2 ashing by ICP-RIE

O_2: 40 sccm/20 min

14. SPM, DHF cleaning

15. Activation annealing in RTA

N_2: 0.8 sccm @ 1000^{o}C/2 min

16. SiO_2 removal

DHF: 3 min

17. HfN (4 nm) deposition by ECR-sputtering

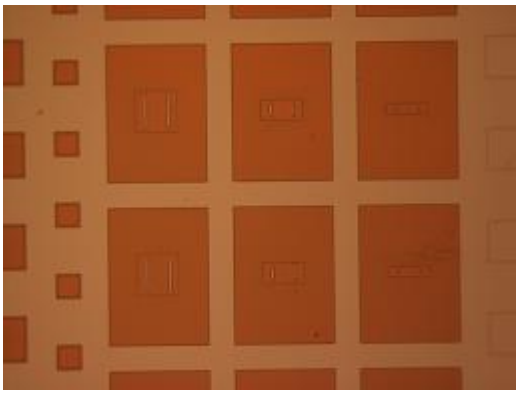
Ar/N_2: 20/8 sccm, 0.19 Pa

Micro-wave/RF: 500/500W

Deposition time: 1 min

18. FGA in RTA

N_2/4.9%H_2:1 L/min @ 400^{o}C/30 min



19. Al evaporation

20. Contact holes patterning (Mask #3)

21. Al removal

H_3PO_4 50 ml + HNO_3 3 ml @ RT

Etching: 2 min, rinse: 10 min

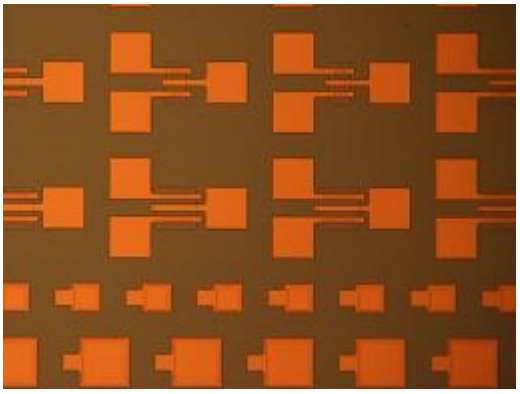
22. HfN removal by DHF

Etching: 40 sec, rinse: 10 min

23. photo-resist removal

Acetone: 3 min, methanol: 3 min, rinse: 3 min

24. Al evaporation



25. Electrode pad patterning (Mask #4)

26. Al removal

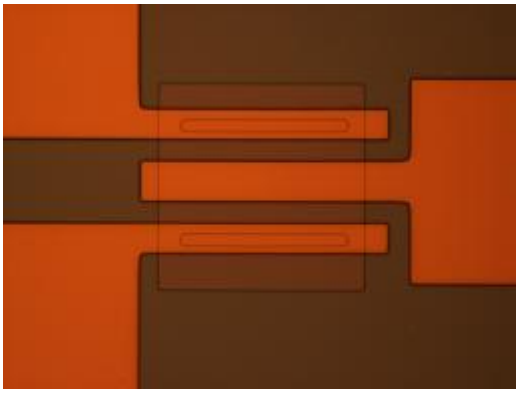
H_3PO_4 50 ml + HNO_3 3 ml @ RT

Etching: 4 min, rinse: 10 min

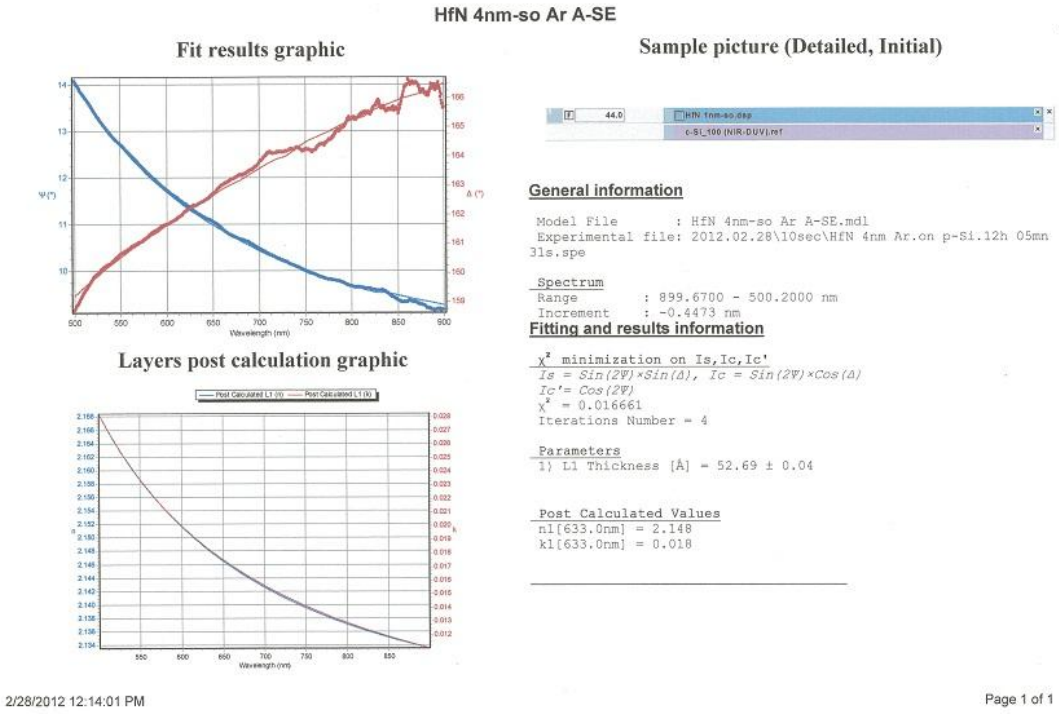
27. photo-resist removal

Acetone: 3 min, methanol: 3 min, rinse: 3 min

28. Al evaporation



Appendix C Ellipsometry result



HfN 4nm-so Ar A-SE

Fit results graphic

Sample picture (Detailed, Initial)

Layers post calculation graphic

General information

Model File : HfN 4nm-so Ar A-SE.mdl
Experimental file: 2012.02.28\10sec\HfN 4nm Ar.on p-Si.12h 05mn 31s.spe

Spectrum
Range : 899.6700 - 500.2000 nm
Increment : -0.4473 nm

Fitting and results information

χ^2 minimization on Is,Ic,Ic'
Is = Sin(2Ψ)×Sin(Δ), Ic = Sin(2Ψ)×Cos(Δ)
Ic'= Cos(2Ψ)
χ^2 = 0.016661
Iterations Number = 4

Parameters
1) L1 Thickness [Å] = 52.69 ± 0.04

Post Calculated Values
n1[633.0nm] = 2.148
k1[633.0nm] = 0.018

2/28/2012 12:14:01 PM

Page 1 of 1

Ellipsometry for the HfN film.

Appendix D Characteristics for the Hf/HfON/p-Si(100) diode

We investigated Hf/HfON/p-Si(100) diodes to apply n-MISFET. The Hf electrode was deposited by RF and ECR sputter. To confirm the Hf electrode property, we also investigated Al/HfON/p-Si(100) diode for comparison. Figure D-1 shows C-V characteristics for Al/HfON/p-Si(100) and Hf/HfON/p-Si(100) structure. In case of Hf/HfON/p-Si(100) structure, the EOT became larger than that of Al/HfON/p-Si(100) structure. Hf is easy to oxidize in air. Therefore, the reduction of capacitance was due to it. To prevent oxidization of Hf electrode, we used HfN electrode as a capping layer on Hf electrode. The HfN thickness was 50 nm. Furthermore, to confirm the work function modulation by Hf electrode, Hf thickness was changed from 5 to 20 nm. All films were deposited by ECR plasma sputtering and the samples were annealed at 800^{o}C for 1 min in nitrogen ambient. Especially, HfN film was deposited at sputtering gas pressure of 0.19 Pa (Ar/N_2 : 20/0.8 sccm) at room temperature. Figure D-2 shows the C-V characteristics with various Hf thickness for the HfN/Hf/ HfON/p-Si(100) structure. As increasing the Hf thickness, the C-V curves were shifted toward negative direction. It means that the work function is able to be modulated by Hf electrode thickness. However, despite of HfN electrode capping, the electrical properties were not improved. Table D-1 shows the resistance of HfN electrode with various Hf thicknesses. As shown in Table D-1, the resistance of HfN electrode was higher than that of Hf electrode. The reduction of capacitance was due to the high resistance of the electrode.

Table D-1 The resistance of HfN electrode with various Hf thicknesses.

(nm)	HfN/Hf 50/20	HfN/Hf 50/15	HfN/Hf 50/10	HfN/Hf 50/5	Hf 50
Sheet Resist (ohm/sq)	118	140	133	154	31
Resistance (μohm/cm)	826	914	800	848	157

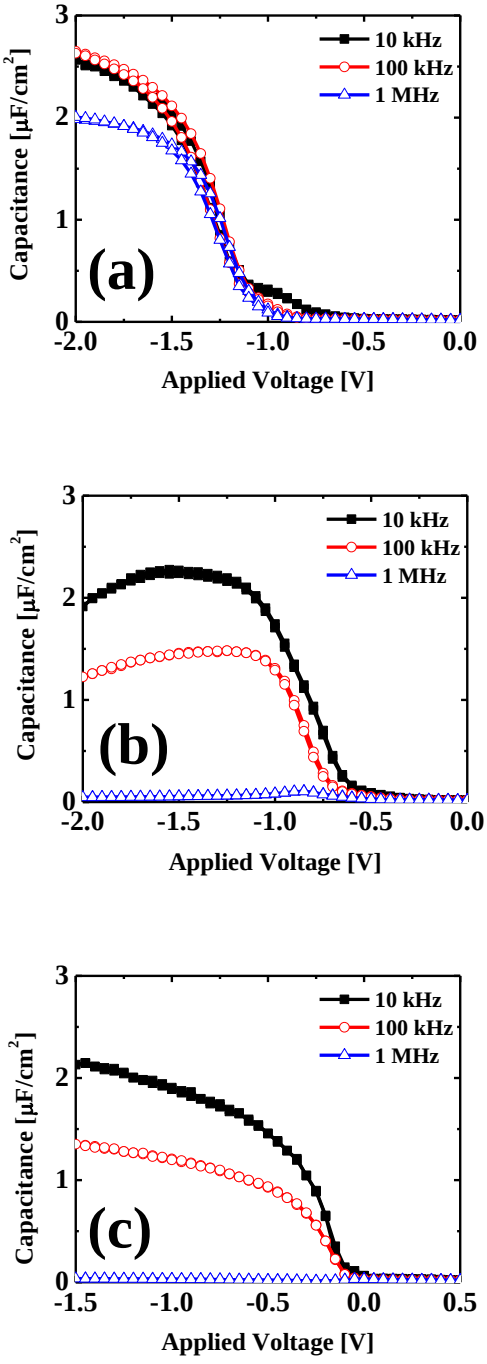


Fig. D-1 C-V characteristics for (a) Al/HfON/p-Si(100), (b) Hf/HfON/p-Si(100) by rf, and (c) Hf/HfON/p-Si(100) structure by ECR sputter.

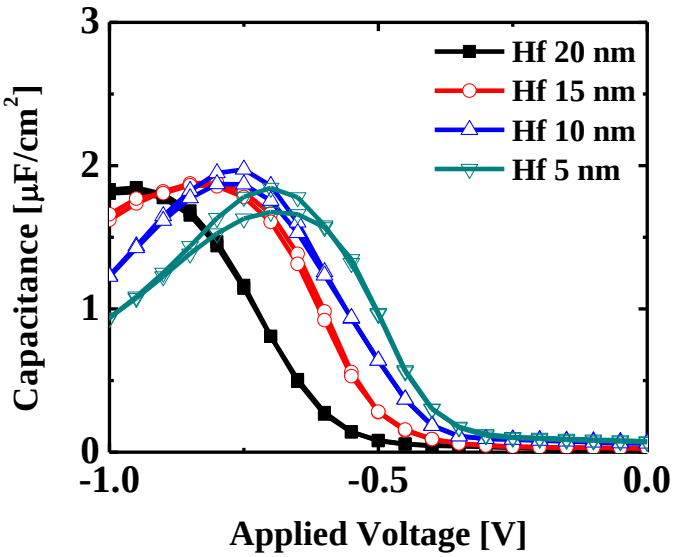


Fig. D-2 C-V characteristics with various Hf thickness for the HfN/Hf/ HfON/p-Si(100) structure.