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Study of Si Grating Couplers toward 3-Dimensional Optical Interconnect

by

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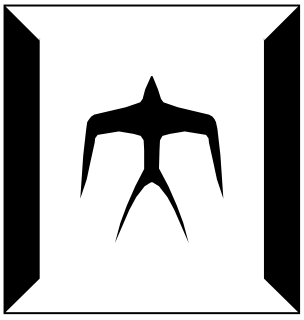

A DOCTORAL DISSERTATION

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Chapter 1

Introduction

1.1 Introduction

There were several innovative changes in modern history. The agricultural revolution in 17~18 century provide us enough foods and promote accumulation of wealth. These changes then lead to the industrial revolution which was transition to the mass production and consumption. Now, we are in the smart revolution. Communication technology provided us the connection to the internet through such as fiber to the home (FTTH) or the mobile network. In addition, since Apple Inc. brought their first smart phone into the market in 2007, access to the internet became more easier from anywhere all around the world at any time only with a few touches through mobile communications.

Before the smart revolution, the major media for wire and wireless communications were text or voice data such as an e-mail or a phone call. These media typically use small amount of data however, rapidly growing number of those media and appearance of the new communication means such as video calls or social network services caused more

traffic on the network. Moreover, video sharing services as represented by YouTube and live streaming videos are making tremendous traffic on the internet. In order to cover the ever increasing traffic on the internet, optical fiber cables have played a backbone of the communication system for about half century. Almost all of the Long distance communications are now been covered by the optical communication.

In the aspect of the individual devices, the performance of the processor LSI have increased year by year. The channel length of the transistor has been continuously shrunk which resulted acceleration of processing speed for more than 40 years, known as the scaling law. Now, the channel length is getting closer to the atomic level and among others the delay in the global wires, which is the side effect of the scaling law, become bottle-neck on the device speed and they are getting worse after every technology generation. There is no doubt that people still request higher speed and low power consuming devices. In order to satisfy these demands, we should arrange some innovations in to the current electronic devices. Optical interconnect can be a long-term solution for the speed limitation in global wires. Well established long-distance technology of optical fiber communication should be effectively utilized for short-distance optical interconnect.

In this chapter, optical interconnect for the long-distance communication and the short-distance connection will be explained. A brief view of recently emerging on-board optical interconnect for data-centers and on-chip optical interconnect for future development will also be reviewed. Then, photonic devices based on silicon photonics will be introduced for the optical interconnect application. a-Si:H and it's devices will be given including nonlinear phenomenon and three-dimensional integration. Finally, objective and outline of this thesis will be presented.

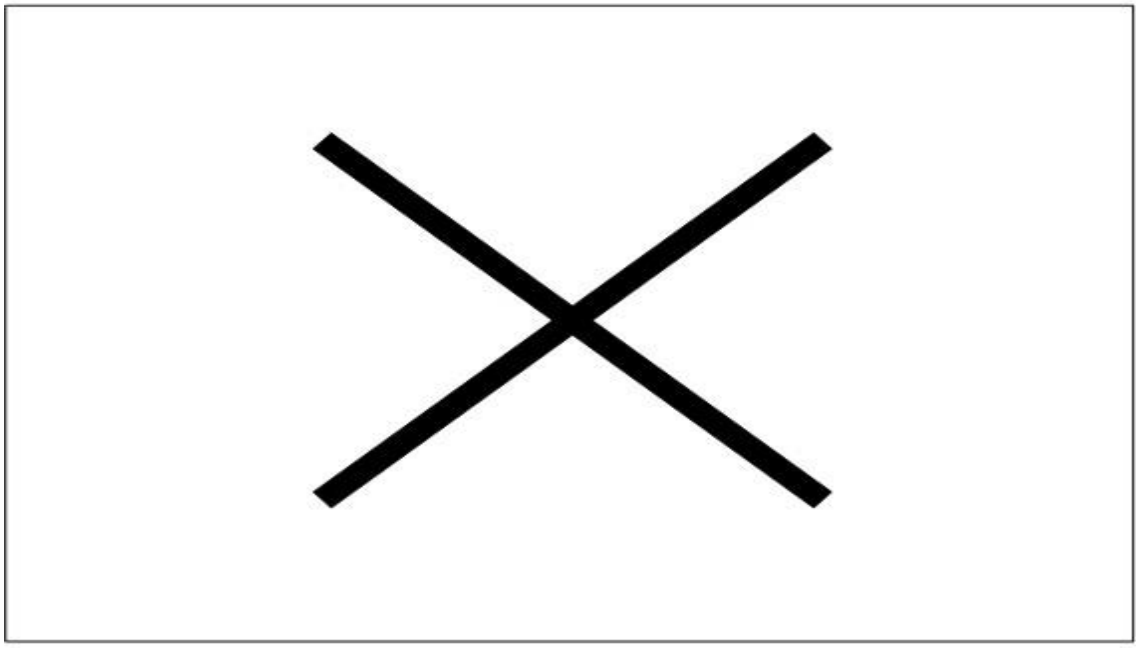


Figure 1. 1 Scaling parameters of electrical wires (K. C. Saraswat, 1982) [1]
(S: Scaling factor, SC: Chip size scaling factor)

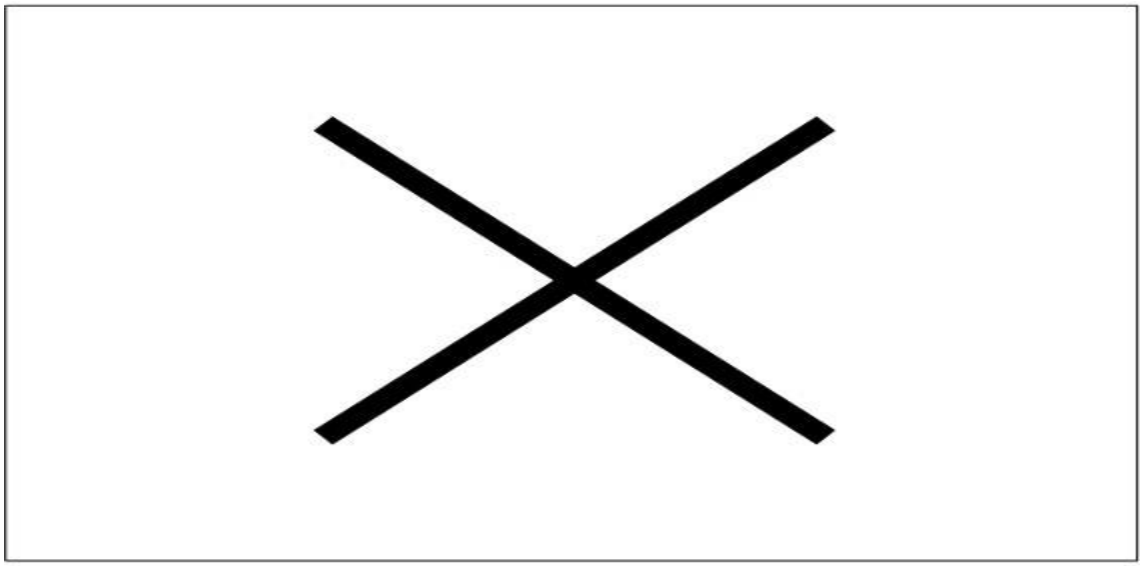


Figure 1. 2 Delay for local and global wiring versus technology node (ITRS, 2001)[7]

1.2 Optical interconnect

As mentioned in section 1.1, current electronic devices are facing limitation in performance improvement. Main reason for this limitation is rooted in the transmission

delay called represented as RC time constant. Figure 1. 1 shows cross section of MOS transistors with parasitics and interconnection parameters including time delay constant expressed by scaling factor (S) and chip size scaling factor (Sc) [1]. For the local wires, the wire length is scaled by Sc so that the RC time constant remains 1. In terms of global wires, however, the entire chip size is not scaled. Instead, unoccupied area which was left by shrunk of the scaling of original chip will be used as multi-core integration [2, 3] or integration of additional functioning devices such as 3G/4G modems or voltage regulator etc [4-6]. Consequently, the RC time constant for global wires is increasing with further shrink of technology node since the length of interconnection will not be scaled. Relative delay at local and global wires at each technology node is shown in Figure 1. 2 [7]. Even with repeaters, the delay at the global wire is consistently increases and moreover, additional power should be dissipated by the repeaters. Using low k (dielectric constants) materials to minimize the capacitance of the electrical wires has been carried out as called as more Moore approach though, the progress was slowed down due to the manufacturing cost and reliability etc [7, 8]. Differential transmission line interconnects was proposed and showed improved delay characteristics, but is has been seldom used in industrial applications [9].

There are some alternatives to the conventional electrical wires for the interconnection. Carbon-nanotube (CNT), graphene or optical interconnect would be the most potential candidates. Metallic characteristics of CNTs have been regarded as an ideal interconnection material though, their high intrinsic resistance and low producible-density are obstacles to the interconnect application [10]. The situation for graphene interconnect is much like CNTs and there are still lots of challenges for the practical use [11]. Other than the more Moore approach, as called as more than Moore approach, three dimensional (3D) stacking is one of possible solution in some cases. By using through silicon via (TSV), multi-stacking of electronic chips would be long-term solution by cutting down the length of the interconnection especially for the memory-CPU interconnection [12-14].

Optical interconnect will be one of the most possible solution for the high speed

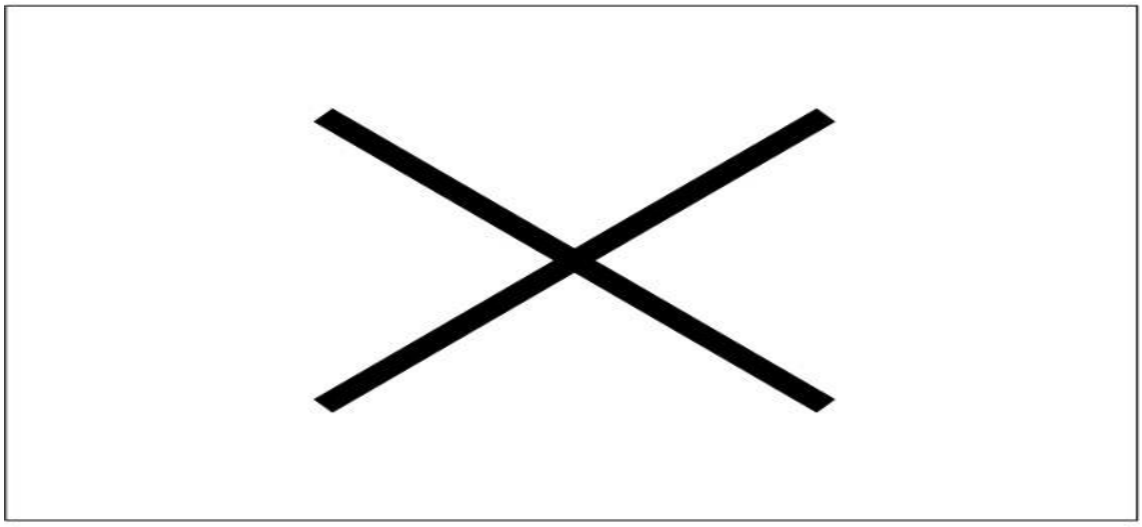


Figure 1. 3 (a) Latency and (b) energy per bit in terms of wire length for the 22-nm technology node. (K.H. Koo, 2009) [15]

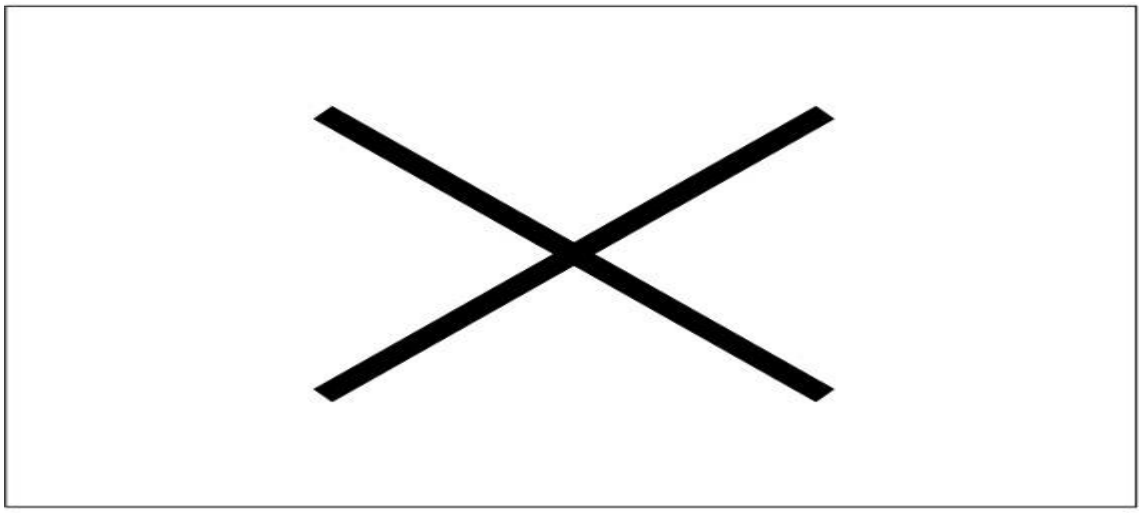


Figure 1. 4 Power efficiency of the supercomputer (TOP 20 in June 2014) (TOP 500) [16]

interconnection. Increase of signal delay in optical solution is basically proportional to the transmission length contrary to the electrical wires which are proportional to the square of the transmission length. Thus, optical interconnect have strength in the advanced technology nodes or long-distance interconnect. Given the above considerations, it might be obvious to think as optical solution, which has been used for long-distance communication, substitutes electrical interconnect along with advances in

technology (in other words, faster transmission speed).

The above explanations were focused on the global wires on chip. However, the situation for longer reach interconnections are more desperate. The longer the interconnection distance, faster the RC limitation will come to the threshold. There would be no objection that the replacement of electrical interconnect by optical interconnect at longer distance (> 1 m) will come to reality. The question is how short links can be replaced by optical interconnect. Comparison of delay and energy per bit of electrical and optical wires are shown in Figure 1. 3 [15]. If we assume the technology node as 22-nm, optical interconnect becomes favorable at mm order of transmission length in terms of latency and power dissipation. The following will summarize the recent issues on the optical interconnect from longer distance to the short distance such as on-chip interconnect.

1.2.1 Board-to-board optical interconnection

Recent research applications in the field of optical interconnect are focused on supercomputers and data-centers. Interconnect links in this field is < 100 m. Unlike the consumer level microprocessor for personal computers, adding more cores are not efficient as expected any more since there are too much cores already. The communication bandwidth between cross-nodes and also, system architecture will limit the total performance of the supercomputer which is called as Amdahl's law [16]. Power consumption at the exponentially increasing cross-node interconnections is also an inevitable problem. TOP 500 org. provides worlds ranks of supercomputers listed by their performance or power efficiency etc [17]. Power efficiency of world's top-20 supercomputers is plotted in the Figure 1. 4. Green circles are supercomputers with optical interconnect and orange diamonds are without optical interconnect.

US's Defense Advanced Research Projects Agency launched project of exascale computing system in 2008. In their report, power was mentioned as the major concern for the realization of exascale computer by 2020 [18]. Introducing optical modules into the

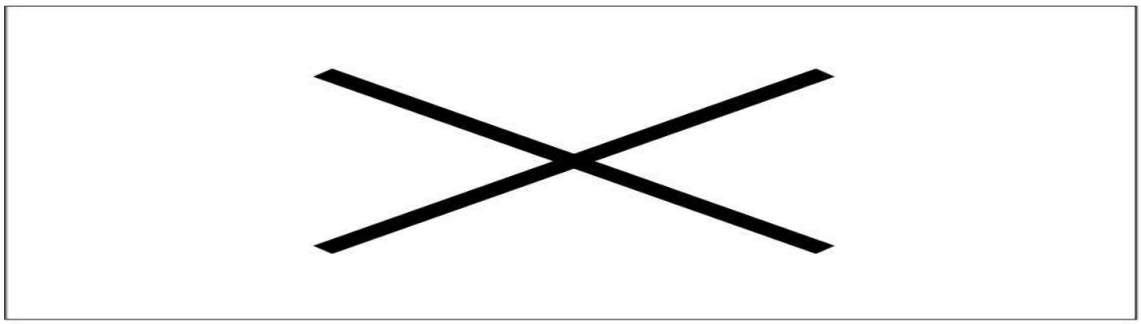


Figure 1. 6 Schematic of Light Peak hardware prototype. (Intel corp.) [22]

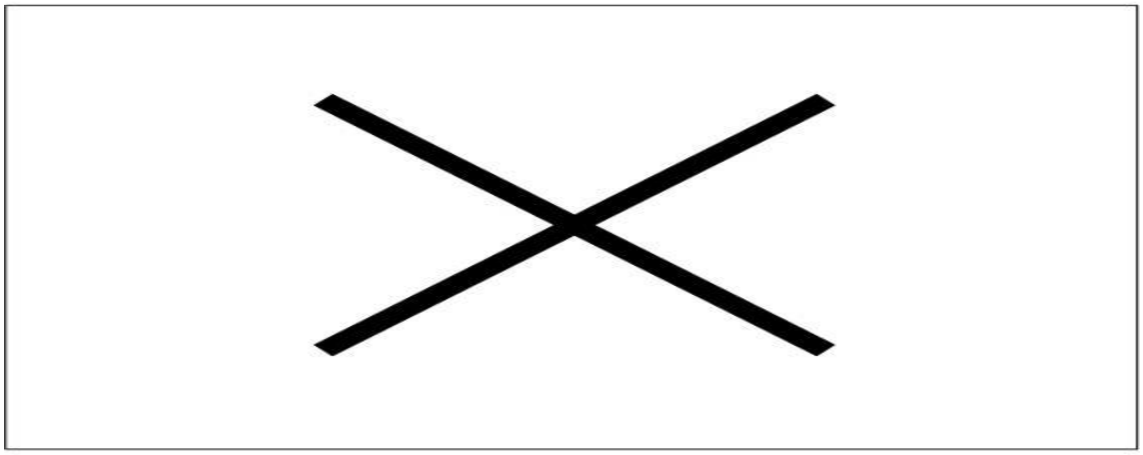


Figure 1. 5 Concept image of photonics-electronics convergence system for inter-chip interconnects. (Y. Arakawa et al.) [24-26]

exascale interconnect is also the solution for power issue. The state-of-the-art optical interconnect demonstrated by IBM corp. recorded 1~3 pJ/bit for <100 m interconnection links [19-21]. 850 nm VCSELs and multimode fibers were used for the cost effective system in the demonstration.

1.2.2 On-board optical interconnection

Interconnection links below 10 meters will be the next business area of optical interconnect. Intel corp. announced new serial bus interface named Light Peak in 2009 (Figure 1. 6) [22, 23]. Light Peak also covers link length more than 50 meters and Intel insisted that the Light Peak will utilize silicon photonics technology (details about silicon photonics will be explained in chapter 1.3) for faster I/O data rate. Light Peak was

renamed after commercialized as Thunderbolt in 2011. Latest version of Thunderbolt can support 20 Gbps for 2 channel data transmission.

Another approach was made by PETRA in 2010 as shown in Figure 1. 5. Lasers and optical splitters, modulators, waveguides and photodetectors were integrated on a single silicon on insulator (SOI) substrate, targeting for chip to chip interconnection such as between CPU-CPU, CPU-memory or CPU-storage [24-26].

As a waveguide material for on-board interconnection, polymer is very attractive. It is cost effective since it can utilize printed circuit board (PCB) fabrication technology and has very low lose <0.05 dB/cm [27-29]. 12.5 Gbps signal transmission through 100-cm propagation length was demonstrated.

1.2.3 On-chip optical interconnection

For optical interconnect, shorter interconnection length means tight budget will be requested in order to compensate the OE and EO conversion loss and delay. Requirements for on-chip optical interconnect were suggested by D. Miller in 2009 [30]. Energy target of on-chip optical interconnect is ~30 fJ/bit in 2022 and it will lower than 10 fJ/bit in the later years.

Thus, if we consider directly modulated lasers, allowed energy is about 2–10 fJ/bit. It means the volume of the quantum well should be less than 10 μm^2. Recently, membrane-type lateral-current-injection laser achieved lasing threshold of 700-μA and energy efficiency of 45 fJ/bit was estimated by numerical analysis [31, 32]. Another approach was done by using photonic crystals for the higher light confinement in the laser cavity. Threshold current of 4.7 μA was achieved and by directly modulating injection current to the laser, energy efficiency of 4.4 fJ/bit was demonstrated [33, 34]. Theses lasers have shown their potential for on-chip interconnection application though, there are still challenges of more power-efficient operation or optimization of output power.

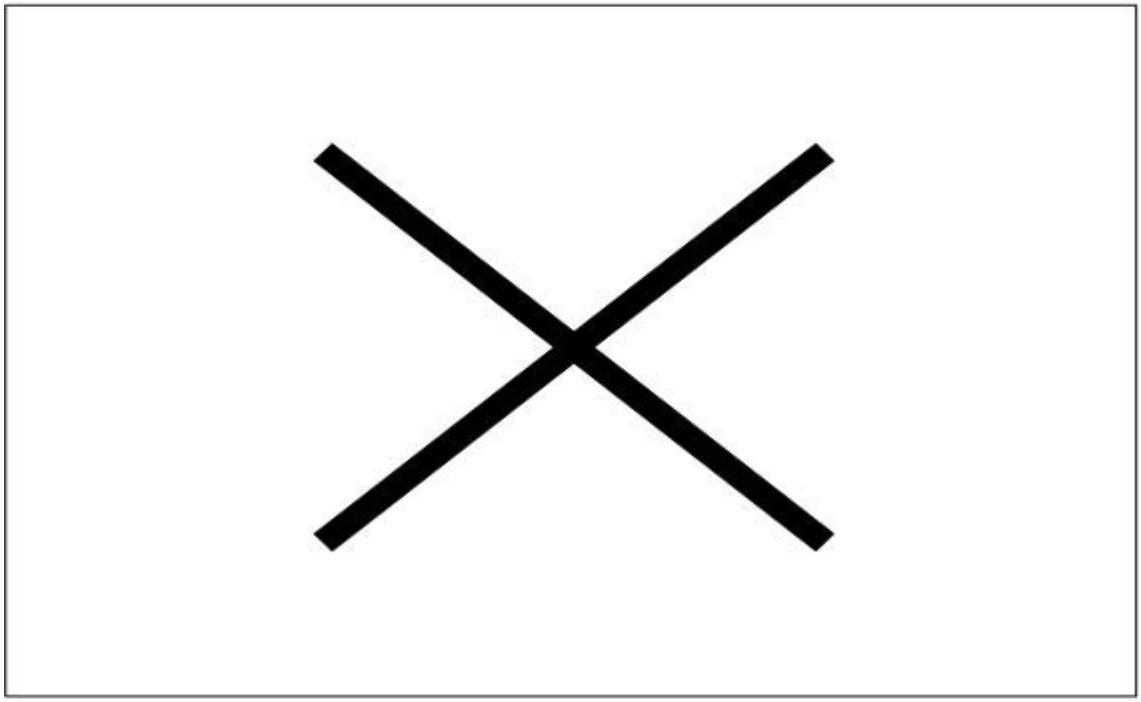
Light source could also be combination of off-chip laser with on-chip modulators. We can minimize the effort of controlling temperature fluctuations caused by electrical

components on the chip by separating lasers. In this case, coupling loss reduction of off-chip laser to the on-chip modulator and modulators with efficiency of less than 10fJ/bit are necessary. In order to achieve 10fJ/bit modulation efficiency, modulators with Franz-Keldysh effect [35] or quantum-confined Stark effect (QCSE) [36, 37] may meet the requirements. These effect shows very strong absorption coefficient which is suitable for high-speed and low-power consumption modulation. Without these electric field induced effects though, there were also remarkable reports using the carrier-depletion type modulators operating at near 10fJ/bit [38-40].

For the detectors, required capacitance was calculated to be a few femtofarads. This can only be achieved by the detector area of a few square μm. Fairly efficient detectors with waveguide integrated Ge photodetectors [41, 42] or MSM type detectors with capacitance of 10fF [43] has been demonstrated. Plasmon enhanced photodectors [44, 45] and optical antennas [46] are also attractive in achieving ultra-low device volume.

There is also another estimation of requirement for on-chip optical interconnect [47]. The idea of the minimum operation power for each devices were quiet close with the values in Ref. [30] as shown in Table 1. 1.

Table 1. 1 Device requirement for sub 100fJ/bit CMOS photonic interconnect
(S. Manipatruni et al., 2013) [47]



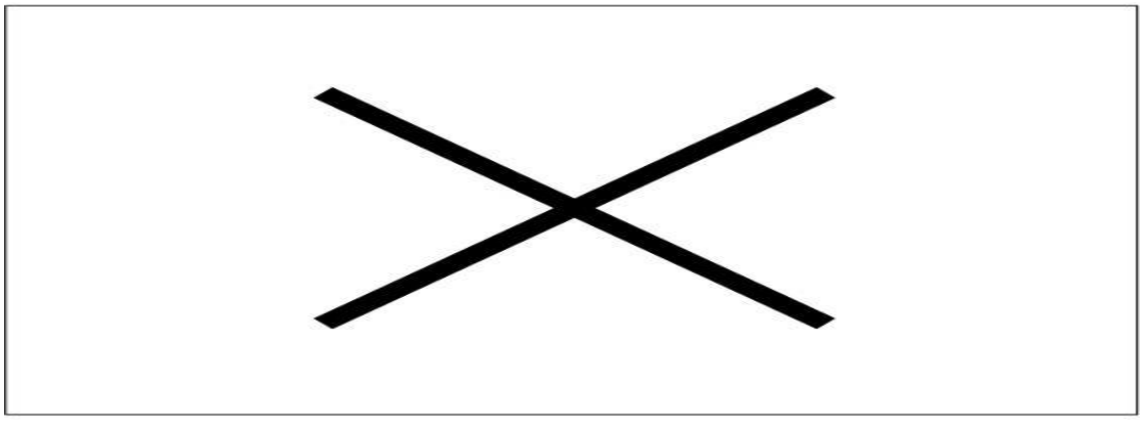


Figure 1. 7 Number of published articles includes the term "silicon photonics" searched by google scholar.

1.3 Silicon photonics

Silicon (Si) has been a major material for current electronic industry because of not only its capability as a transistor but the mass production possibility or the material cost itself. 300 mm wafers are already in production now and global investments has been made to shift smoothly toward 450 mm wafers [48].

Optical components made by Si were suggested and demonstrated first by R. Soref in 1986 operating at the optical communication wavelength of 1.3 and 1.55 μm [49]. Si is transparent through 1.3 μm to 1.55 μm and can easily obtain high refractive-index difference by pairing with SiO_2 enabling nano-scale dimension of 220 nm×500 nm waveguides, which are called as Si wire waveguide. Matured technologies earned by electronic-device development such as nano-structure fabrication process and metal contact know-hows are also merits of using silicon as a core material for optical components. The thickness of SiO_2 under the Si layer needed to be more than 2 μm in order to avoid the crosstalk from the Si substrate so typical optical devices are fabricated on SOI with thick SiO_2.

Researches on the silicon photonics has started with full force in early 2000s. Fig. 1.7 shows number of published articles searched by google scholar including the term "Silicon photonics". The number of published articles drastically increases since 2004. Since then, silicon photonics has been studied in various fields such as optical interconnect, optical routers [50], biosensing [51, 52], and even for mid-infrared device applications [53].

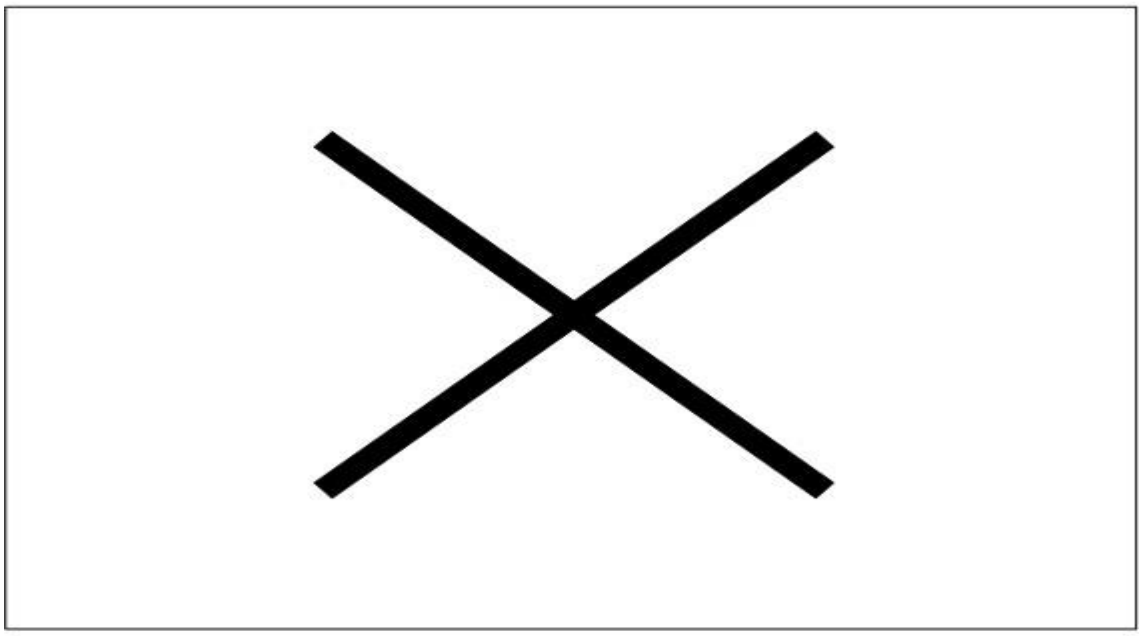


Figure 1. 8 Si waveguides (a) Si wire waveguide (out group) **(b) Si slot waveguide** (out group) **(c) Si photonic crystal waveguide** (T. Baba et al., 2014) [58] **(d) Si subwavelength waveguide** (x. Guan et al., 2014) [57]

1.3.1 Waveguides

The most basic component for silicon photonics is waveguide.

The propagation loss of the Si wire waveguide has been improved constantly from tens of dB/cm to 0.45±0.12 dB/cm (top record) by reducing sidewall roughness with higher node technology [54]. There are also other ways to reduce the propagation loss of the Si wire waveguides. By depositing mid-indexed material at the interface of the Si and SiO_2, reduction of scattering loss was observed [55]. Another approach is using multimode or ridge waveguides. The waveguide width of those are relatively wider than the Si wire waveguide so the optical confinement at the interface between Si and SiO_2 is small, which results in low propagation loss [56]. Besides Si wire waveguides which was mentioned earlier, there are several types of waveguides such as slot waveguides, photonic crystal (PhC) waveguides, and subwavelength grating type waveguides [57], etc. Si slot waveguides can confine light strongly into the cladding material. It can provide novel functions like athermal operation in wavelength filters [58, 59], biosensing [60], etc. PhC waveguides can control the group index of the waveguide for a wide range. The group index of the usual Si wire waveguide is around 4 to 4.5 instead, that of PhC can be increased as 60 as a result of slow light effect. PhC waveguides have many potentials to

be applied as optical memories [61], sensing, modulators [62, 63], etc.

1.3.2 Devices in silicon photonics

Si has poor light emitting efficiency as it is an indirect bandgap material. Germanium (Ge) attracted much attention for its possibility of direct-bandgap light emitting property. Still though, much efforts should be done for increasing light emitting efficiency and bringing peak wavelength from longer than 1.6 μm to near 1.55 μm [64, 65].

In order to obtain high efficient optical source, many researchers are using wafer bonding of III-V material on the Si substrate which is called as hybrid integration. Such a III-V/Si hybrid lasers was proposed and demonstrated since 1993 [66-69]. In our group, we also demonstrated the first III-V/Si hybrid DFB laser in 2006 and engaged on the enhancement of high-optical output hybrid lasers so far [70, 71].

Ge is the key material of photodetectors for the silicon photonics. Epitaxially grown Ge on Si can effectively absorb light from 1.3 μm to 1.55 μm wavelength range. There are some types of photodectors depending on their operation mechanism. Metal-semiconductor-metal (MSM) photodectors have relatively small capacitance and simple fabrication process, but on the other hand, p-i-n photodetectors are usally have small dark-current than MSM photodectors. Typical Ge photodetors shows responsivity of 0.8~1 A/W and up to 40 Gbps operation speed [41, 42, 72, 73]. Other than those photodetectors, avalanche photodiode (APD) photodetectors also have been demonstrated however [74, 75], they have weakness on the power consumption if we consider the application for the optical interconnect.

For the effective coupling between waveguides and photodetectors, waveguide-integrated Ge photodetectors were widely researched for optical interconnect application [76, 77]. Plasmon enhanced photodectors are also attractive issues in minimize the capacitance and power consumption [78, 79].

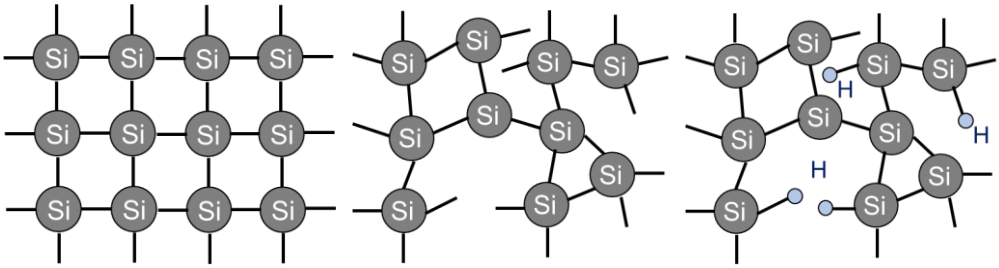
Modulators in optical interconnect will be needed when the light source is located out of the chip. CW light will be modulated into optical data by electrical signal on the chip. In this case, multi-level modulation with wavelength division multiplexing (WDM) is also possible for high spectral efficiency modulation [80-82].

There are several kinds of modulation method in Si photonics. The simplest way is to use high thermo-optic (TO) coefficient of Si [83] however, these micro-heater based modulators are limited by μs order of switching time and consume much power. Therefore, these are usually used as a switching devices where does not require high speed responses.

For higher modulation speed, electrically driven Si modulators using carrier

depletion or accumulation of free carriers in Si rib waveguides has been widely investigated. So far, up to 50 Gbps operation has been reported [39, 84, 85]. These modulators are typically based on mach-zehnder-interferometer (MZI) and occupies large spaces since it requires long interaction length. Ring-resonator type Si modulators usually have low power consumption and small foot-print but also have disadvantage as narrow bandwidth [86].

Recent topics on modulators are Franz-Keldysh effect [35] or QCSE effect [36, 37] based Ge on Si modulators and PhC modulators based on slow light effect [62] for further energy-effective modulation and small foot-print. Electro-optic modulator using nonlinear effect of polymer material is also a promising way in achieving high speed and low power consumption device [87].



(a) **(b)** **(c)**

Figure 1. 9 Various types of Si (a) crystalline silicon (b) amorphous silicon (c) hydrogenated silicon.

1.4 Hydrogenated amorphous silicon

Optical devices of silicon photonics are typically fabricated on a SOI substrate. Thus, if we consider on-chip optical interconnect, the optical components should be fabricated on the same plane with transistors which means optical components will be fabricated in the front-end process. However, required thickness of SiO_2 (or other insulators) layer is getting thinner and thinner for transistors while the optical components need at least 2~3 μm for optical isolation. Even more, micro-processors for personal computers use bulk silicon as a substrate.

Therefore, integration of optical components by back-end process would be a good choice. Integration by back-end process means optical components will be formed at the time after fabrication process of logic layers are done. In this case, if we do not stick on the crystalline silicon (c-Si) of SOI for the optical devices, amorphous silicon (a-Si) can alternate c-Si and getting harmony between electrical and optical devices. a-Si has been used and studied as a thin film transistor [88] and solar cells [89] for more than 40 years. Physics of a-Si, deposition conditions as well as optical properties have already been extensively investigated.

a-Si can be deposited at low temperature around 300℃ by plasma-enhanced chemical-vapor-deposition (PECVD). Figure 1. 9 illustrates three types of Si. c-Si is well arranged and has only few defects. On the other hand, arrangement of Si is random and has some defects in a-Si. Si have 4 valence electrons and thus, requires 4 neighboring

atoms to share their electrons each other. When there was no electron to share with, unoccupied electron remains as a dangling bond. This dangling bond is very unstable so it tends to absorb light [90-92]. Hydrogen diffusion during the deposition of a-Si will replace weak Si-Si bonds and bond with Si instead of the dangling bonds [93]. Thus, hydrogenated amorphous silicon (a-Si:H) means such an a-Si which contains hydrogen atoms in it. The propagation loss of the a-Si:H waveguide was more than 30 dB/cm in early 2000, and it decreased constantly to 1.2 dB/cm in 2012 [94-97]. One of the major benefits of using a-Si:H is, if we alternatively deposit the a-Si:H layer along with SiO_2, multi-layered waveguides can easily be obtained. Higher transmission density of optical interconnect will be a significant advantage for future requirements of LSIs.

There is another material which can be deposited under low temperature. SiN can also be deposited by PECVD at 300℃ and transparent through 1.3 μm to 1.55 μm. As the refractive index of SiN is about (vary with deposition condition) 1.8~2.0 which is smaller than that of a-Si:H (3.4~3.6) and thus, the dimension or the bending radius of the SiN waveguides will become larger [98, 99].

Details about deposition conditions of a-Si:H used in this thesis will be explained in chapter 2.

1.4.1 On-chip 3D integration of a-Si:H layers for optical interconnect

In this section, multi-stacking of a-Si:H layers toward 3D optical interconnection will be discussed. There are two main advantages in 3D integration of optical circuit. Transmission density as described earlier and reduction of waveguide crossings. When we consider on-chip optical interconnect, the size of the optical circuits will be limited by the size of LSI chip. Therefore, the transmission density of the optical interconnect should cover the entire bandwidth of the LSI chip. D. Miller estimated required pitch of waveguides for on-chip optical interconnect [30]. In the paper, the required pitch was calculated as 1.3 μm in the extreme case of the 2022 chip with constant bytes/FLOP

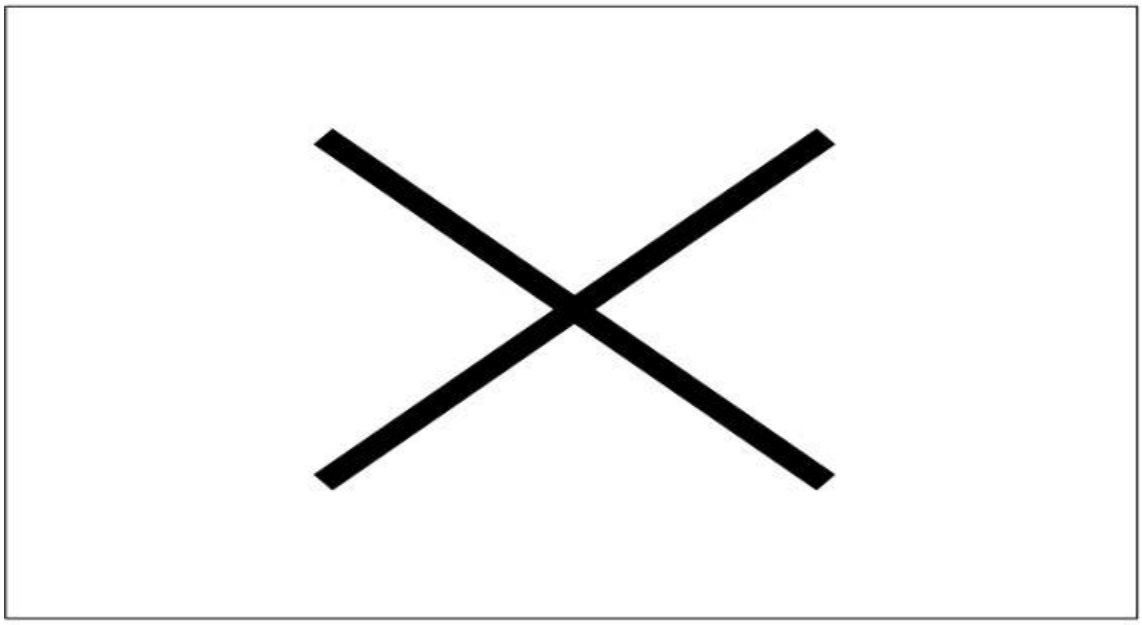


Figure 1. 10 Maximum possible network-level insertion loss by component for varying sizes of the Torus and Non-Blocking Torus. (J. Chan et al., 2010) [103]

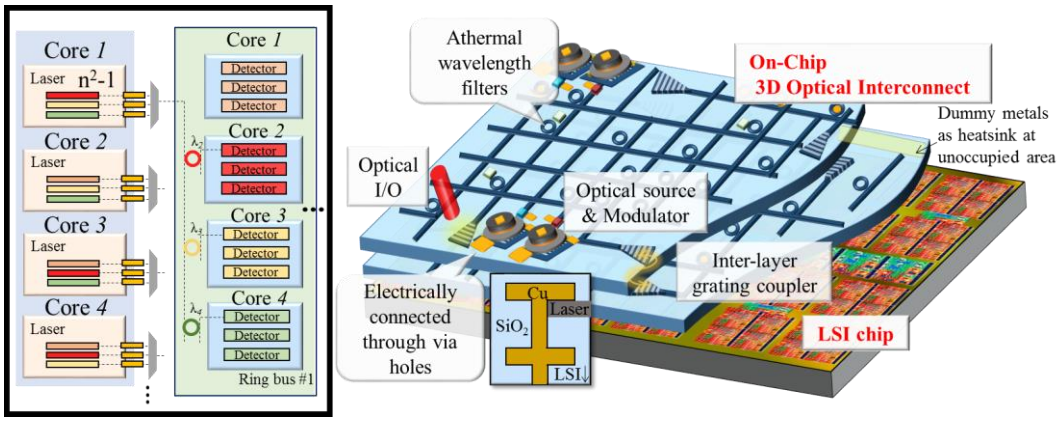


Figure 1. 11 On-chip 3D optical interconnect.

scaling. Later than 2022, the required density of the waveguide will grow more and more to force 3D-stacking of the optical circuit.

The other advantage is reduction of waveguide crossings. When the system become more complex with increasing technology nodes, the waveguide crossings will

continuously grows to the significant level. Researches on the low-loss waveguide crossings has been demonstrated by many researchers [100-102] , and the lowest crossing loss was 0.02 dB/cross. Even in the case of 8×8 topologies, there will be 1080 waveguide crossings and the loss of the waveguide crossing cannot be ignored even though we assume the loss of the waveguide crossing as 0.01 dB/cross [103]. It is needless to say that the ratio of crossing losses in the total insertion loss is increasing with system size (Figure 1. 10). These waveguide crossings can be avoided by 3D integration.

Figure 1. 11 illustrates the schematics of on chip 3D optical interconnects. Optical sources and other optical devices will be integrated on a LSI chip. These components can be monolithically or simply integrated by flip chip bonding technology and will play a photonic network such as ring buses between processor cores. In the photonic network, switch arrays will route the optical passes within the ring buses. Dummy metals created during the multi-stacking process can also be used as heatsink for the generated heat from the logic layer. In this thesis, the optical devices for the 3D optical interconnects including vertical coupler between multi-layered waveguides, fiber couplers, and optical sources will be discussed.

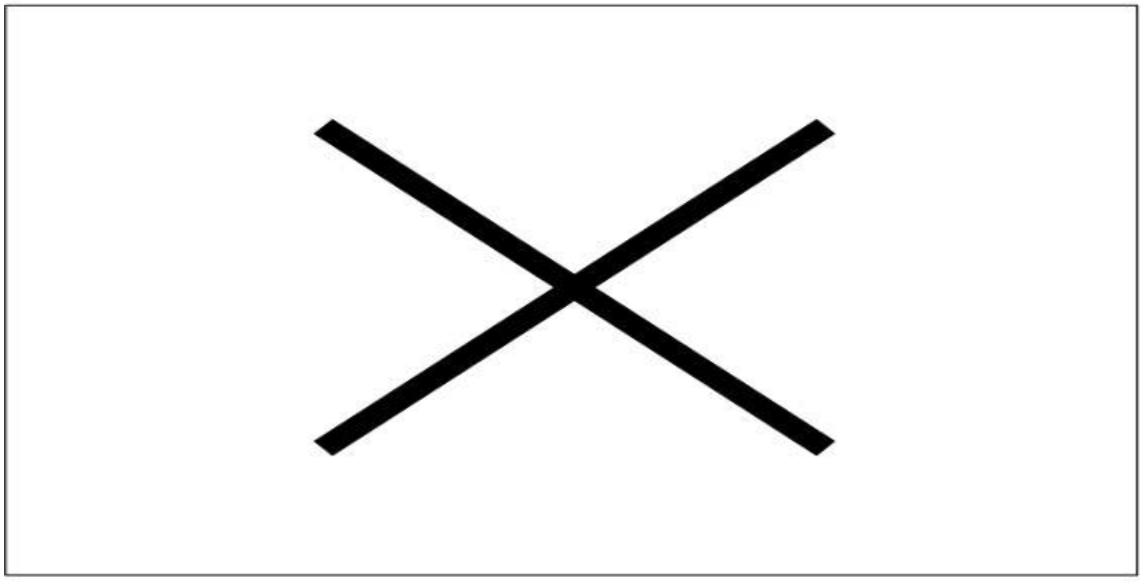
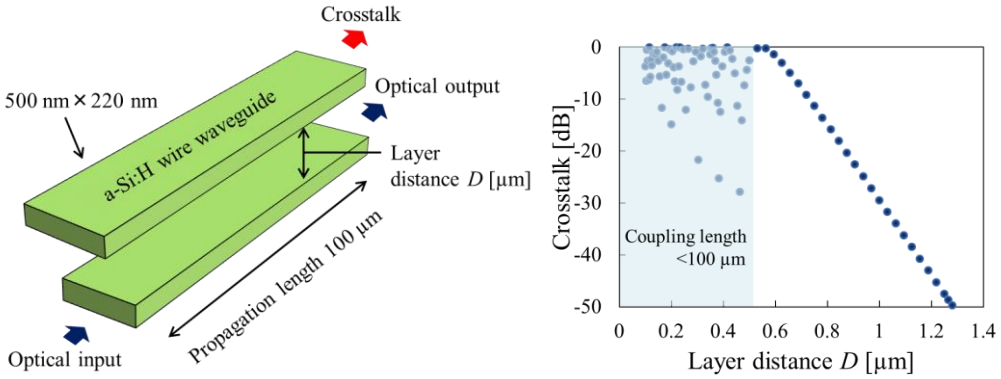


Figure 1. 12 Pattern diagrams of 3D crossing photonic wire waveguides.
(Furuya et al., 2012) [97]

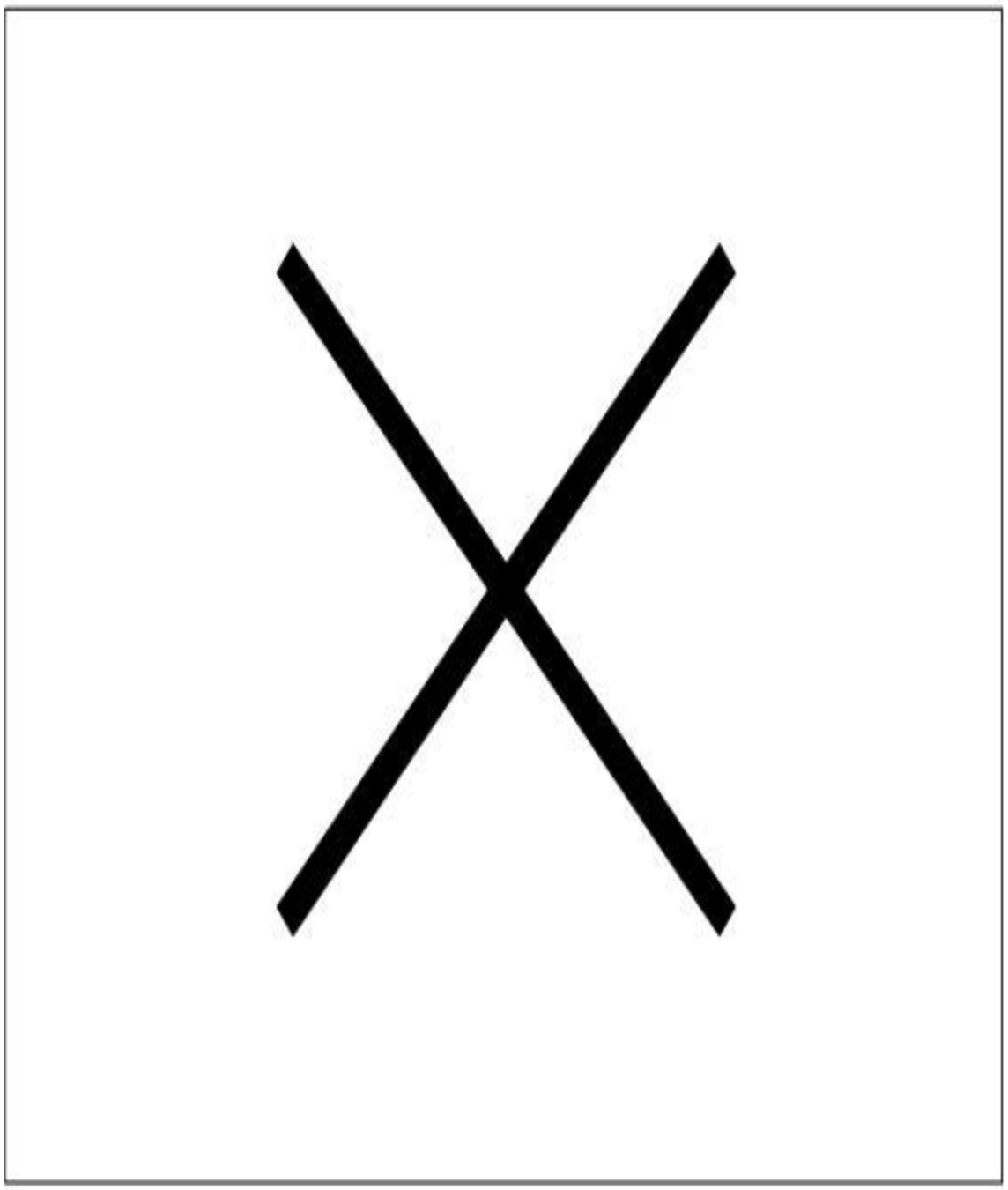


(a) **(b)**

Figure 1. 13 (a) Vertically stacked waveguides propagate in the same direction. (b) Crosstalk as a function of inter-layer distance *D* when the propagation length is 100 μm.

1.4.2 Inter-layer vertical couplers

The vertical coupler between multi-layered waveguides is essential for the 3D optical interconnect. Coupling efficiency and available inter-layer-distance should be considered in designing vertical couplers. When the inter-layer distance is too close, crosstalk



(f) Inter-layer grating coupler (S. Ura, 2002) [112]

Figure 1. 14 Inter-layer optical couplers

between the waveguides on upper and under layer become critical. The crosstalk between two waveguides was numerically analyzed by Furuya et al. as shown in Figure 1. 12 [97]. If the two waveguides are orthogonal to each other, the crosstalk is less than -50 dB at the

inter-layer distance of 400 nm. If the two waveguides are crossed with an angle of 30°, the crosstalk is less than -50 dB when the inter-layer distance is more than 900 nm. As an even worse case, when the two waveguides are parallel to each other as shown in Figure 1. 13, the inter-layer distance of 1 μm is needed for the -30 dB isolation. Based on these analysis we decided to design the inter-layer distance of 3D optical interconnect as 1 μm.

Vertical connections in optical links are not as easy as in electrical connections such as through silicon via [104, 105]. Unlike electrical connection, bending loss will extremely increase at a right angle.

There are several reports of vertical couplers between multi-stacked optical waveguides as shown in Figure 1. 14. The simplest way to achieve vertical coupling is to use direction-coupler structure [106, 107]. R. Sun et al., demonstrated vertical coupling between c-Si waveguides and a-Si:H waveguides with coupling loos of 0.2 ± 0.05dB. High coupling efficiency can be obtained with directional-coupler structure however, the inter-layer distance is limited to be around hundreds of nm. This eventually leads to the crosstalk between multi-layered waveguides. For the practical use, multi-stacks of vertical couplers will be needed in order to avoid the crosstalk [107].

Vertical coupling using secondary-core is similar to the directional-coupler structure except the refractive index of secondary-core is lower than the multi-layered waveguide cores. At the inter-layer distance of 0.6 μm, 1.8 dB of insertion loss was estimated in secondary-core structure inter-layer coupler [108].

The other approach for coupling between the longer inter-layer distances is to use grating coupler. Grating couplers for compact silicon waveguides were demonstrated by Ghent group in early 2000s and after that, many research groups reported grating couplers as an optical coupler between single-mode-fiber and in-plane waveguides [109, 110]. Because it uses diffraction of light from the gratings unlike evanescent light of directional-coupler structure, light coupling between more than a few μm is possible. By using vertically stacked grating couplers, inter-layer coupling can be realized [111]. A similar approach but using another materials (mainly SiO_2) for shorter wavelength was reported in 2002 [112, 113]. We proposed and demonstrated the inter-layer grating couplers since 2012. The details of the inter-layer grating couplers will be presented in chapter 2 and 3.

	~2000	2005	2008	2009	2010	2011	2012	2013	2014
World a-Si WG loss / Inter layer coupler	30 dB/cm [93]	5.0 dB/cm [94]	Directional coupler [105]	3.5 dB/cm [95]			1.2 dB/cm [96]	Second core coupler. [107] Inter-layer grating couplers. [111]	
				J. Kang →					
Laboratory			~12 dB/cm (~3rd layer)	~6 dB/cm (2nd layer)		2nd layer: 3.8 dB/cm 3rd layer: 3.7 dB/cm	Inter-layer grating couplers	Inter-layer grating couplers with metal mirrors	Apodization of grating

1.5 Objectives and outline of this thesis

The objectives of this thesis are to establish the multi-staking process of the a-Si:H waveguides and optical connection of those multi-layered waveguides needed for realization of 3D optical interconnect. Studies regarding propagation-loss properties in multi-layered a-Si:H waveguides were insufficient and the fabrication process was not established yet in 2009. In our group, the propagation loss of a-Si:H waveguides were 10.2 and 12.0 dB for 2nd and 3rd layer waveguide, respectively at the end of 2008. In this thesis, improvement of the propagation loss in the multi-stacked waveguides were investigated and further, vertical coupling between those multi-layered waveguides was designed and demonstrated. For the fine isolation between the multi-layered waveguides, the inter-layer distance was set to be more than 1 μm. In order to achieve that inter-layer distance, vertical coupling using stacked grating couplers were proposed and designed in this thesis. The main objectives of this thesis are as follows.

(1) Establish the multi-staking process of the a-Si:H waveguides
   (a) Revealing loss mechanism in the multi-stacked a-Si:H waveguides
   (b) Low-loss multi-layered a-Si:H waveguides

(2) Design and demonstration of vertical coupling between multi-layered waveguides.
   (a) Design and fabrication of high coupling efficiency in the inter-layer coupler.

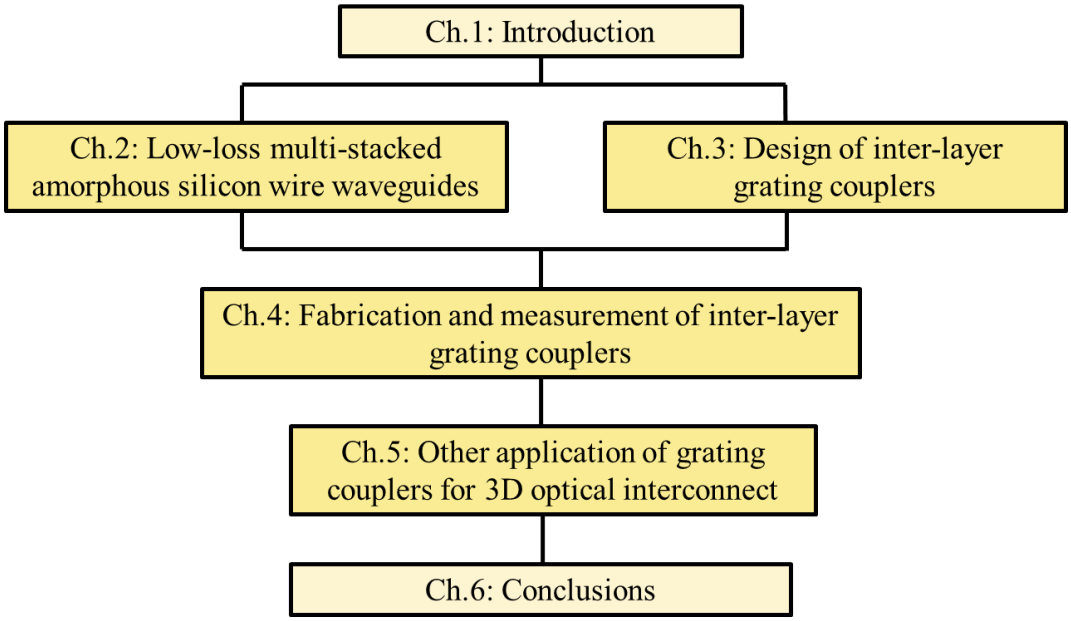


Figure 1. 15 Outline of this thesis

(b) Inter-layer distance independent operation.

(3) Other applications.

(a) Fiber to the waveguide grating coupler.

(b) Integration of VCSEL on Si substrate.

The outline of my thesis is shown in Figure 1. 15. In chapter 2, details about deposition conditions of a-Si:H film will be shown. The relationship between the surface roughness and deposition pressure will be investigated. Further, the surface roughness and the propagation loss will be evaluated. In chapter 3, design of inter-layer grating couplers will be presented. In order to achieve high coupling efficiency, metal mirrors will be introduced to the inter-layer grating coupler. Then, apodization of gratings for the Inter-layer distance free operation will be presented. Based on the fabrication process of chapter 2 and simulation results chapter 3, the inter-layer grating coupler will be fabricated and the measurement results of inter-layer grating couplers can be found in chapter 4. In chapter 5, other applications of grating couplers for 3D optical interconnect

including single-mode-fiber to the waveguide couplers or coupler between VCSELs and Si waveguides will be given.

Finally, the summary of this thesis will be presented in chapter 6.

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Chapter 2

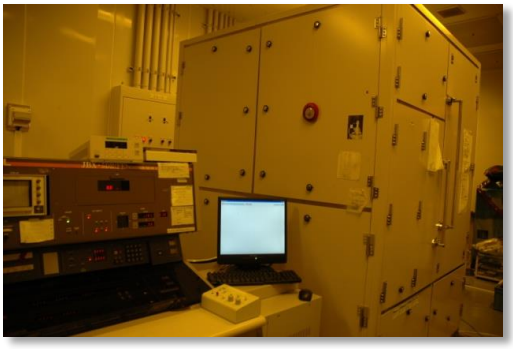
Low-loss multi-stacked amorphous silicon wire waveguides

2.1 Introduction

Low temperature deposition of a-Si:H enables 3D integration of optical interconnects. As a core material for optical waveguides, a-Si:H is transparent through 1.3 μm 1.55 μm depending on the deposition condition. Until late 2000s, low-loss amorphous silicon waveguides with propagation loss of 3~5 dB/cm have been demonstrated [1-4]. However,

these reports considered only the material loss related with the dangling bonds or hydrogen content in a-Si:H.

If we consider multi-stacking of a-Si:H waveguides, the accumulation of surface roughness degradation will be a critical issue. First, major equipment used for the fabrication process in this thesis will be introduced briefly. Then, improvement of the surface roughness by changing the deposition condition will be explained in chapter 2.3. Then, the propagation loss of the multi-layered waveguides will be presented in chapter 2.4. Finally, the relationship between the propagation loss of the a-Si:H waveguides and the surface roughness will also be revealed in chapter 2.4.4.



(a)

(b) (c)

Figure 2. 1 (a) JBX-5FE and (b), (C) JBX-6300FS for EBL

Table 2. 1 EBL system

System	JBX-5FE	JBX-6300FS
Electron gun	ZrO/W thermal-field type	ZrO/W Shottky type
Writing method	Spot beam	
Accelerating voltage	25keV/50keV	25keV/50keV/100keV
Beam current	20 pA ~ 20 nA	
Beam size	~ 5nm (@ 50 kV)	
Scan speed	Up to 12 MHz	Up to 50MHz

2.2 Fabrication equipment

Before to mention about the a-Si:H film, major equipment for the fabrication process used in this thesis will be introduced here. The major machines include electron beam lithography (EBL) systems, inductively-coupled-plasma reactive-ion-etching (ICP-RIE) machine and conventional reactive-ion-etching (RIE) machines for dry etching, plasma-enhanced chemical-vapor-deposition (PECVD) machines for SiO_2 and a-Si:H deposition.

2.2.1 Electron beam lithography (EBL) system

Nano-scaled dimensions of silicon photonics devices are very sensitive to the fabrication errors. High technology node might be needed to fabricate these devices though, cost of the masks for lithography are getting expansive [5, 6]. EBL is very cost effective and efficient for the arbitrary pattering in the fields of R&D.

In this thesis, two types of EBL systems, which were JEOL JBX-5FE and JBX-6300FS, were used as shown in Figure 2. 1. The beam size of the EBL is depend on the beam current and accelerating voltage. Lower beam current and higher accelerating voltage makes the beam size smaller. Because the beam size and the exposure time are in trade off, the accelerating voltage was fixed to 50keV in our group and. The beam current of 100 pA was used in pattering the photonic devices. The minimum beam-shot pitches were 1.25 nm for JBX-5FE and 0.25 nm for JBX-6300FS. In the typical waveguide patterns, the shot pitches of 2.5 nm and 2.5~3 nm for JBX-5FE and nm for JBX-6300FS, respectively were used, which means the resolution of the pattern.

Generally, there is electron scattering and interference effect as called the proximity effect in the EBL process of these nano-scaled structures. For minimize the proximity effect, the proximity effect correction technology is widely used in the field of lithography process and also been tested in our group.

(a) (b)

Figure 2. 2 (a) Conventional RIE and (b) ICP-RIE system

Table 2. 2 Conventional RIE recipe for Si etching

RF power [W]	CF_4 [sccm]	Pressure [Pa]	Time [min]
20	5	0.01	32

Table 2. 3 ICP-RIE recipe for Si etching (CF_4 gas only)

ICP power [W]	Bias power [W]	CF_4 [sccm]	SF_6 [sccm]	Pressure [Pa]	Time [min]
5	75	10	0	0.02	42

Table 2. 4 ICP-RIE recipe for Si etching (CF_4 + SF_6 gas)

ICP power [W]	Bias power [W]	CF_4 [sccm]	SF_6 [sccm]	Pressure [Pa]	Time [min]
1	50	1	8	<0.01	26

Table 2. 5 Deposition recipe of SiO_2 #1

RF power [W]	Temperature [°C]	O_2 [sccm]	TEOS [sccm]	Pressure [Pa]	Deposition rate [nm/min]
250	300	300	4	130	50~60

Table 2. 6 Deposition recipe of SiO_2 #2

RF power [W]	Temperature [°C]	O_2 [sccm]	TEOS [sccm]	Pressure [Pa]	Deposition rate [nm/min]
70	280	233	3	30	45~50

2.2.2 Dry etching system

There are two method in shaping the semiconductors. Wet and dry process can shape the semiconductors depend on the masks made by lithography. As an anisotropic etching method [7, 8], dry etching system has been widely used for optical devices.

Two types of RIE system were used in this thesis as dry etching process. A conventional RIE system (RIE-10NR, SAMCO) and an ICP-RIE system (RIE-101iPH, SAMCO) are shown in Figure 2. 2. Low process pressures can be applied by using ICP-RIE that assists the directionality of the ion flux in the chamber, and moreover, these characteristics lead to better vertical shapes during etching process [9].

Recipes used for Si etching process are listed in Table 2.2, 2.3 and 2.4.

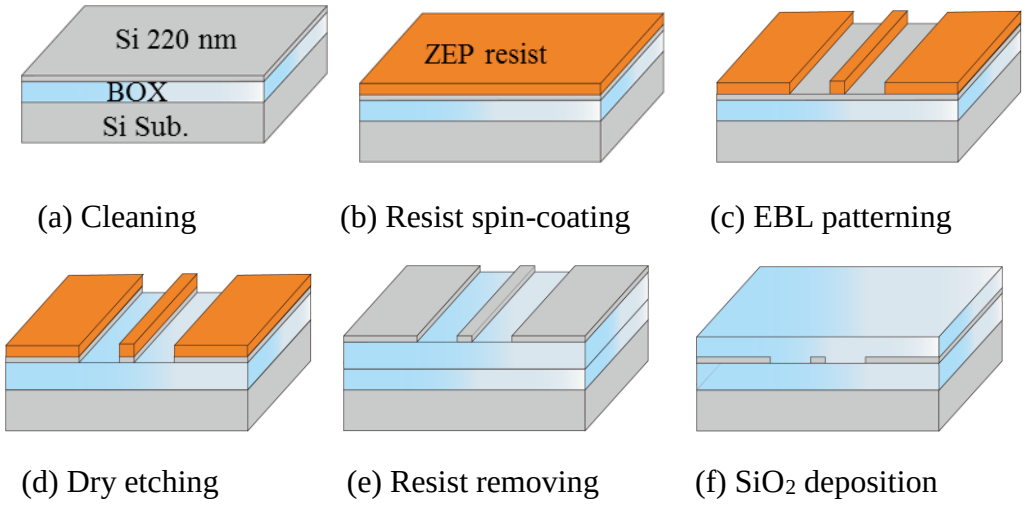


Figure 2. 3 Fabrication flow of the Si waveguide patterns

2.2.3 Plasma-enhanced chemical-vapor-deposition (PECVD)

PECVD machines are used to deposit SiO_2 and a-Si:H. As mentioned in chapter 1, thin semiconductor flims can be deposited by PECVD. In this section, only the PECVD machines for the SiO_2 deposition will be explained here. Recipes of the PECVD for a-Si:H deposition will be presented in chapter 2.3.

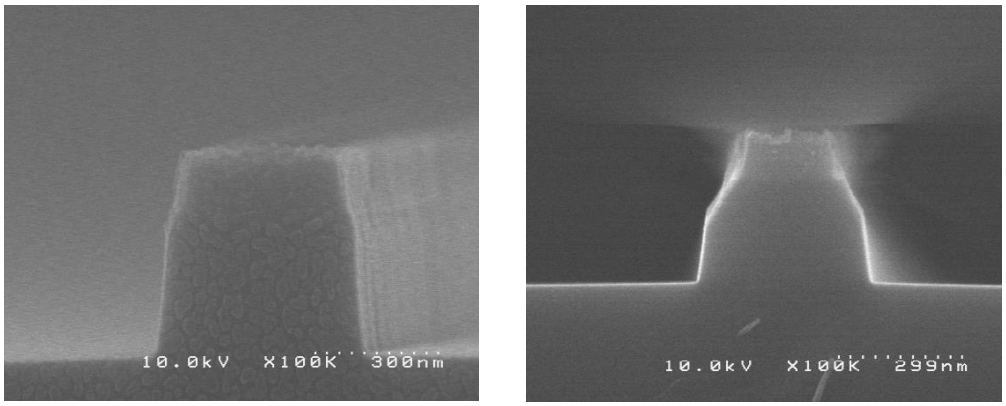
Two types of deposition recipes are listed in Table 2. 5 and Table 2. 6.

2.2.4 Fabrication process of Si waveguide patterns

The fabrication process of the Si waveguide patterns is shown in Figure 2. 3. The first process is to clean the surface of a chip or a wafer. The surface of c-Si and a-Si:H layer is cleaned by the cleaning process #1 as shown in Table 2. 7. Then, ZEP resist was spin-coated to the thickness of 700 nm. Double-layered positive resist Zeon ZEP520A and ZEP520A with a C_{60}-containing micro-composite were used in order to enhance the etching selectivity between the resist and Si-film [10]. These double-layered resist was

Table 2. 7 Cleaning process #1

Procedure	Condition
Ultrasonic cleaning (D.I. water)	1 min. 40% × 1 time
Acetone boiling	5 min. 110°C × 3 times
Ultrasonic cleaning (Acetone)	2 min. 40% × 2 times
Methanol rinse	3 times
D.I. water rinse	3 times
Ultrasonic cleaning (D.I. water)	1 min. 40% × 1 time
Ultrasonic cleaning (98% H_2SO_4)	2 min. 40% × 1 time
D.I. water rinse	3 times
1% BHF	A few sec.
D.I. water rinse	3 times



(a) ZEP-520A + 0.1wt% F301 (b) Original ZEP-520A

Figure 2. 4 Cross-sectional SEM images after ICP-RIE etching process.

substituted by sing-layered ZEP520A resist with 0.1wt% fullerence derivative (nanom spectra F301, Frontier carbon Co.) which can be easily resolved to the anisole since 2012. The spin-coat was two stepped process consisting 1st step of 500 rpm for 3 seconds and

2^{nd} step of 1300 rpm for 60 seconds. Next, the resist was prebaked in the 180°C hot-oven for 20 minutes. Then the EBL exposure was carried out with JEOL JBX-5FE and JBX-6300FS. Because we used the positive resist, the exposed area was both sides of the waveguides with exposure amount of around 130 μC/cm^2. After the EBL exposure, the resist was developed for 60 seconds by ZED-N50 and rinsed by isopropanol for 30 seconds. After the development, the Si waveguide patterns were formed by conventional RIE or ICP-RIE. Figure 2. 4 shows the cross-sectional SEM images of ZEP-520A+0.1wt% F301 and original ZEP-520A after ICP-RIE etching process. Improvement of etching selectivity can be confirmed when mixture of 0.1wt% F301 and ZEP-520A was used. After the RIE process, residual resist was removed by O_2 plasma and ZEP remover (ZDMAC, ZEON). Then the waveguides were buried by 1-μm-thick SiO_2 deposited by PECVD. Finally the waveguides were diced out.

Figure 2. 5 PECVD equipment for a-Si:H deposition

2.3 Low temperature deposition of a-Si:H flim

As mentioned in chapter 1.4, a-Si:H can be deposited at the temperature of 300°C which is compatible with CMOS back-end process. Image of PECVD equipment (Sumitomo Precision Products Co., ltd.) used to deposit a-Si:H film in this thesis is shown in Figure 2. 5.

2.3.1 Deposition condition of a-Si:H film by PECVD

The properties of deposited a-Si:H film is determined by the deposition condition. The initial deposition-condition used in our group is as in Table 2. 8. We used mixture of SiH_4 and Ar gases for the deposition. Adding Ar in the deposition process assumes to make a-Si:H more stable and higher hydrogen content can be expected [11-13].

Table 2. 8 Initial deposition condition

Gas flow	Pressure	Temperature	Power	Deposition rate
SiH_4: 100 sccm Ar: 100 sccm	130 Pa	Top : 250°C Bottom: 300°C	100 W	~130 nm/min

Table 2. 9 Deposition conditions of a-Si:H I

Recipe #	Gas flow (sccm)	Pressure (Pa)	Temperature (°C)	Power (W)
1	SiH_4: 100	130	Top : 250	100
2	Ar: 100		Bottom: 300	50
3	SiH_4: 50	130	Top : 250	100
4	Ar: 100		Bottom: 300	50
5	SiH_4: 100	130	Top : 250	100
6	Ar: 200		Bottom: 300	50
7	SiH_4: 100	50	Top : 250	100
8	Ar: 0		Bottom: 300	50
9	SiH_4: 100	50	Top : 250	100
10	Ar: 100		Bottom: 300	50
11	SiH_4: 50	50	Top : 250	100
12	Ar: 100		Bottom: 300	50
13	SiH_4: 50	50	Top : 250	100
14	Ar: 200		Bottom: 300	50
15	SiH_4: 50	50	Top : 250	100
16	Ar: 0		Bottom: 300	50
17	SiH_4: 100	130	Top : 250	100
	Ar: 100		Bottom: 250	

The recipe #1 was provided as a recipe for low optical absorption when the PECVD equipment was introduced. This recipe #1 was used as an initial recipe here. In Figure 2. 6, the refractive index and the extinction coefficient of deposited a-Si:H film is shown. At the wavelength of 1.55 μm, the refractive index was 3.48 and the material loss was extremely low as below the measurement limit.

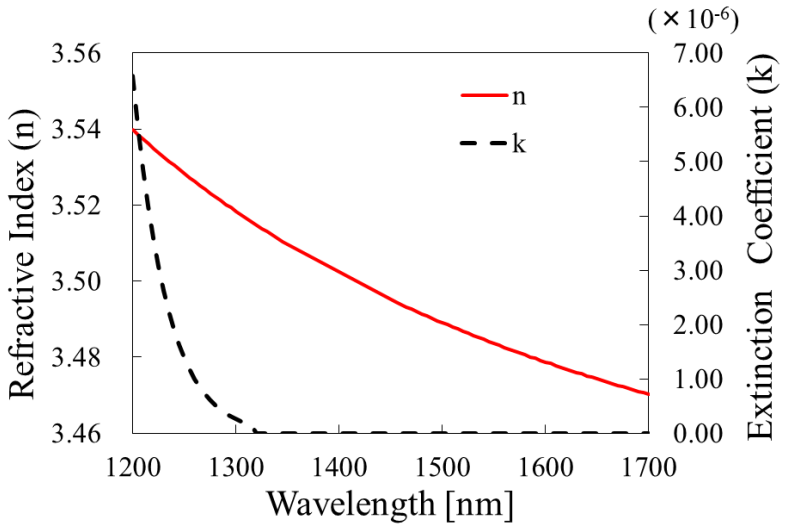
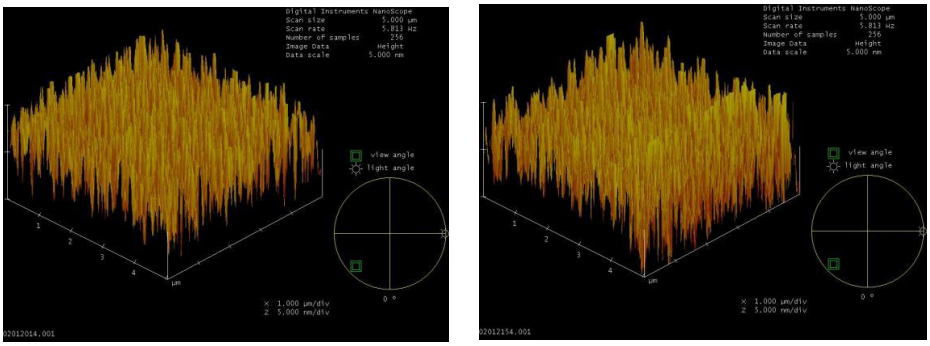


Figure 2. 6 Refractive index and extinction coefficient of deposited a-Si:H flim measured by ellipsometer (recipe #1)

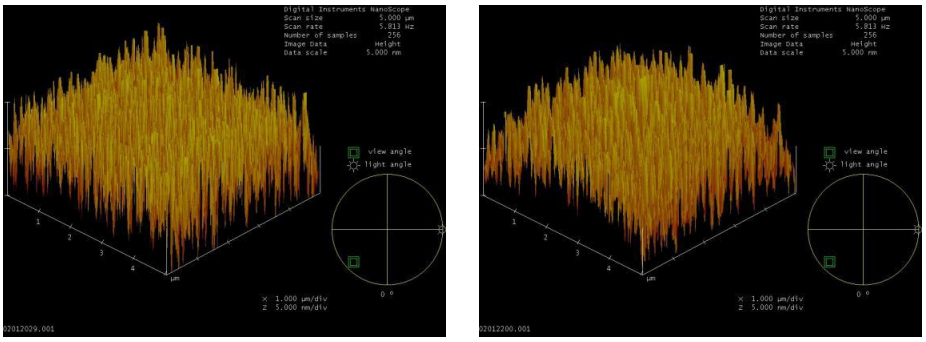
Here, we changed several parameters of deposition condition (Gas flow rate, deposition pressure, deposition temperature, Plasma power) and investigated root mean square (RMS) values of surface roughness measured by AFM. All the a-Si:H films were deposited on the 1-μm-thick SiO_2 which was deposited on the Si substrate and the deposition time for all the recipe here were fixed to 3 min. The specific parameters of deposition conditions are listed in Table 2. 9.

Purpose of this experiment is to investigate which parameter will affect the surface roughness and find the deposition condition of lower surface roughness. The RMS value of the surface roughness was measured in the area of 1.0 μm^2 and averaged by 2 samples.

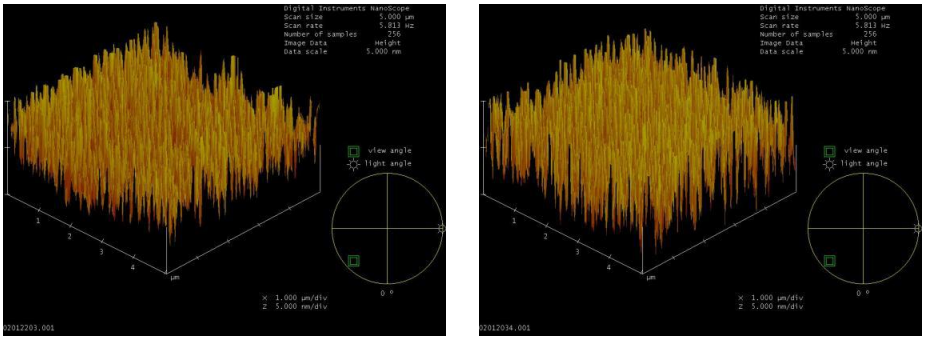
Figure 2. 7 shows the measured RMS values by AFM for each sample. These data will be grouped with similar conditions as shown in Figure 2. 8 and Figure 2. 9.



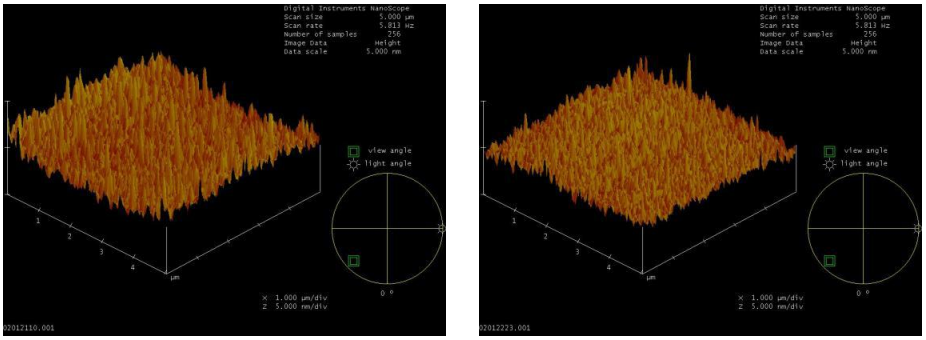
Recipe #1 RMS 1.861 nm Recipe #2 RMS 1.588 nm



Recipe #3 RMS 2.093 nm Recipe #4 RMS 1.496 nm

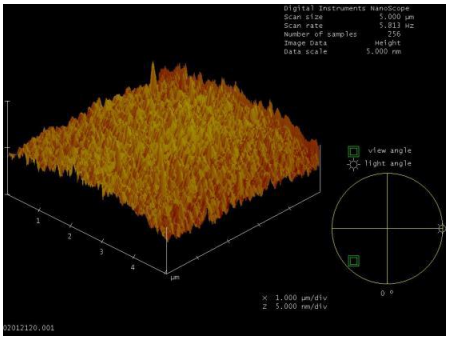


Recipe #5 RMS 2.157 nm Recipe #6 RMS 1.457 nm

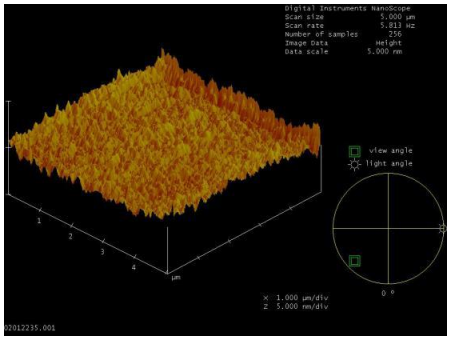


Recipe #7 RMS 0.602 nm Recipe #8 RMS 0.485 nm

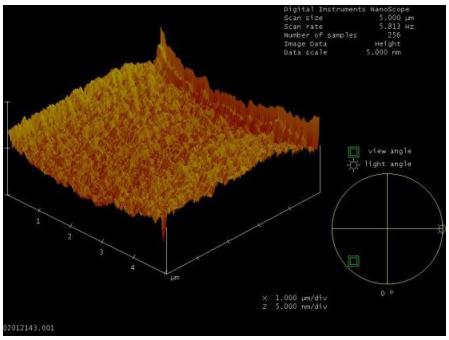
Figure 2.7 Measured RMS values.



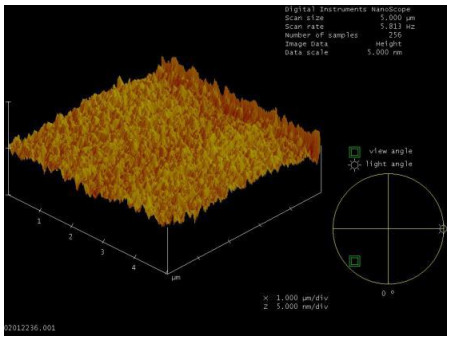
Recipe #9 RMS 0.431 nm



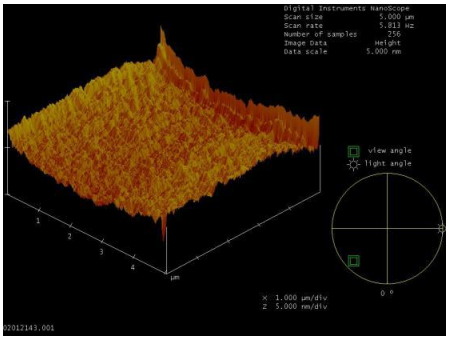
Recipe #10 RMS 0.326 nm



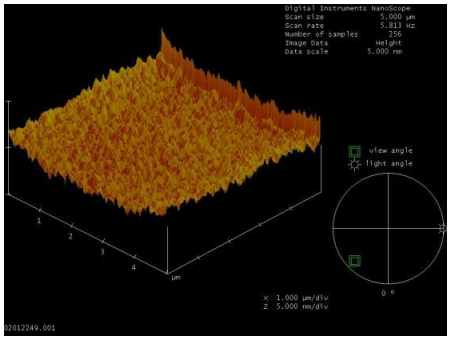
Recipe #11 RMS 0.267 nm



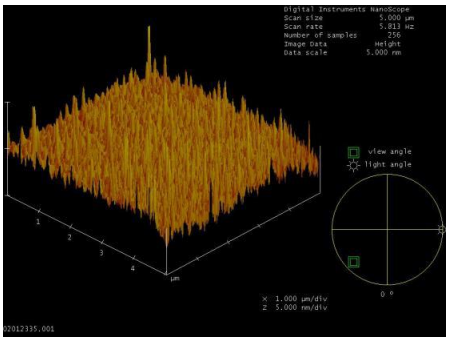
Recipe #12 RMS 0.357 nm



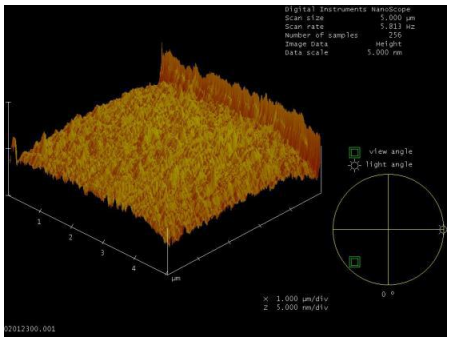
Recipe #13 RMS 2.157 nm



Recipe #14 RMS 1.457 nm

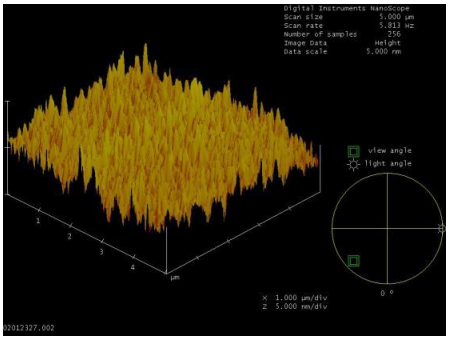


Recipe #15 RMS 0.602 nm



Recipe #16 RMS 0.485 nm

Figure 2.7 Measured RMS values.



Recipe #17 RMS 0.921

Figure 2. 7 Measured RMS values.

Figure 2. 8 (a) shows the surface roughness dependence on SiH_4 flow rate, pressure and plasma power when the Ar flow rate is 100 sccm. The surface roughness was not strictly affected by SiH_4. This may be caused as there is already sufficient supply of SiH_4 atoms in the chamber with more than SiH_4 flow rate of 50 sccm. High plasma power tends to have high surface roughness at the high deposition pressure. At the lower deposition pressure, the surface roughness was drastically improved from more than 1.5 nm with 130 Pa to less than 0.5 nm. This can be attributed to increases in the migration length at lower deposition pressures. These effect can also be confirmed in Figure 2. 8 (b) and (c).

Figure 2. 8 (b) shows surface roughness dependence on Ar flow rate, pressure and plasma power when SiH_4 flow rate is 100 sccm. At the lower deposition pressure, the surface roughness improves slightly with additional Ar flow. Higher Ar concentration may cause lower hydrogen content in the a-Si:H film though.

The temperature dependence of the surface roughness is shown in Figure 2. 9. The surface roughness of a-Si:H film deposited at 250°C shows half of 300°C one. At the lower temperature, the decomposition of the SiH_4 become difficult and thus the deposition rate will be slow down. Deposited a-Si:H at the slow deposition rate usually has lower surface roughness. However, deposited a-Si:H film at a low temperature could

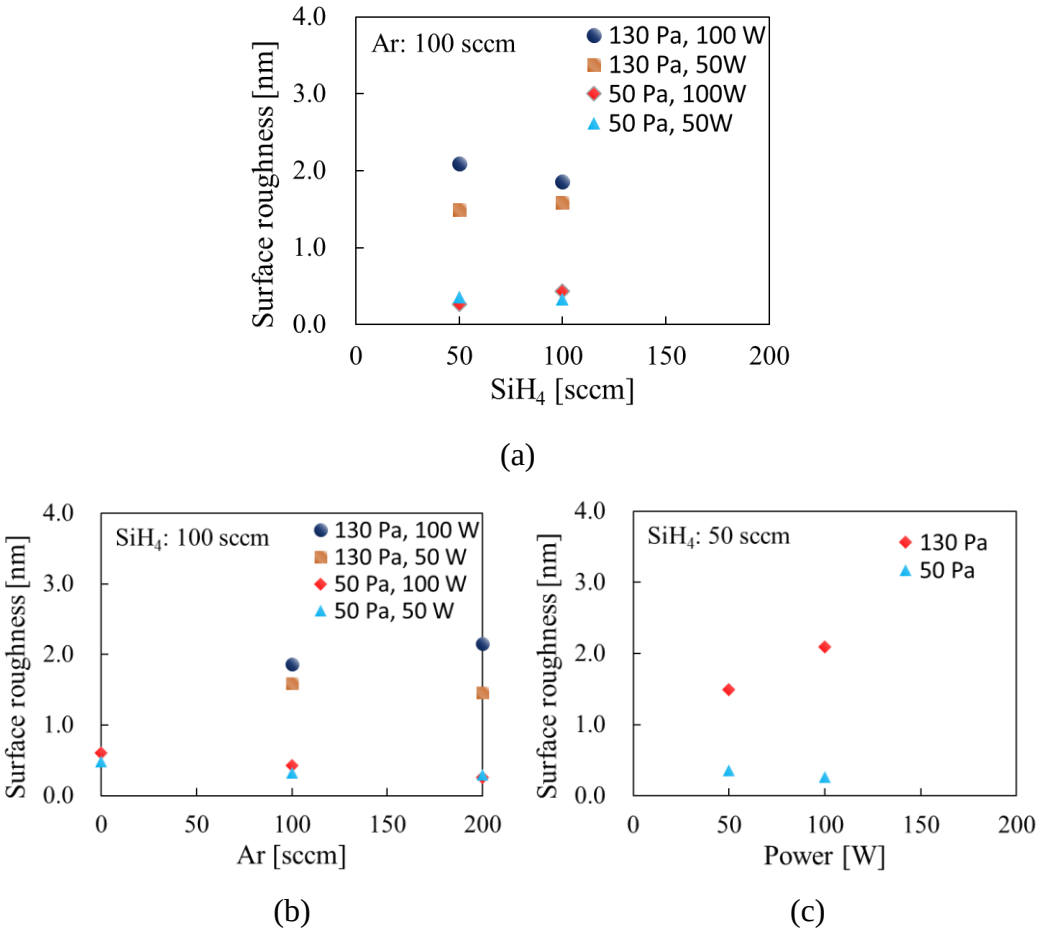


Figure 2. 8 Surface roughness dependence on (a) SiH_4 flow rate, pressure and plasma power when Ar flow rate is 100 sccm (b) Ar flow rate, pressure and plasma power when SiH4 flow rate is 100 sccm (c) power and pressure

be unstable under thermally environment such as on-chip application.

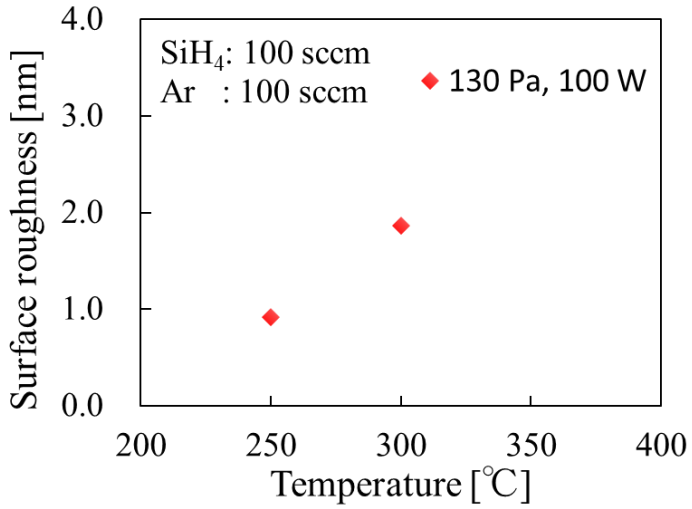


Figure 2. 9 Deposition temperature dependence of surface roughness.

2.3.2 Deposition pressure dependence of surface roughness

In chapter 2.2.1, the most significant effect to the surface roughness was obtained by deposition pressure. Therefore, here we will take a close look on the effect of deposition pressure to the surface roughness.

Table 2. 10 Deposition condition of a-Si:H film II

Recipe #	Pressure (Pa)	Deposition time
18	130	1min 50 sec
19	90	4 min 55 sec
20	50	8 min
21	30	9 min 33sec

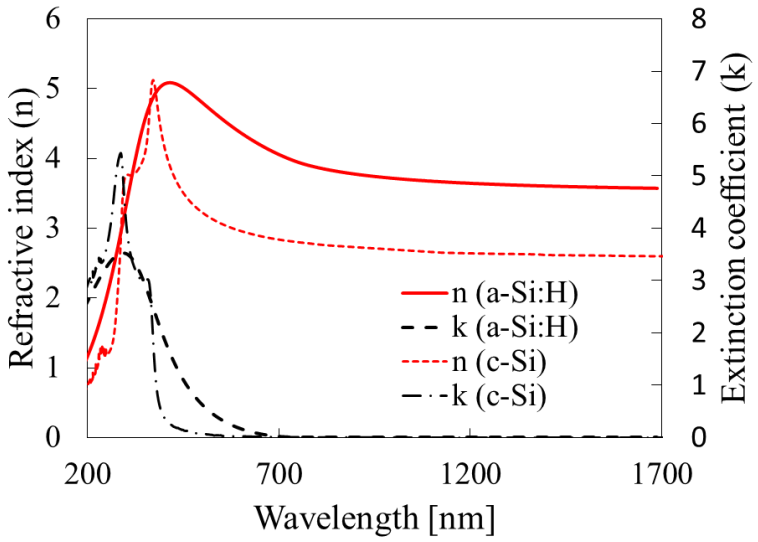


Figure 2. 10 *n*, *k* data of deposited a-Si:H (recipe #21) measured by ellispometer.

**n*, *k* data of c-Si was from Ref [14]

In order to compare the surface roughness at the same deposited thickness, the deposition time was controlled to have the thickness around 220 nm. The deposition pressure was ranged from 130 Pa to 30 Pa and the details of deposition condition including deposition time are in Table 2. 10.

The surface roughness was improved with lower deposition pressure. When the deposition pressure was 30 Pa, the surface roughness was 0.30 nm which was more than 3 times better value compared to the initial condition of 1.06 nm at 130 Pa.

In addition to the above results, if we compare the recipe #9 and #20, the difference in deposition condition was deposition time. Recipe #9 showed the surface roughness value of 0.43 nm which was smaller than 0.78 nm of the recipe #20. The surface roughness was increased with longer deposition time.

Figure 2. 10 shows the refractive index and extinction coefficient of the deposited a-Si:H (recipe #21) and c-Si as a reference [14]. The refractive index was 3.58 at the wavelength of 1.55 μm and shows very small extinction coefficient over the wavelength of 700 nm. Refractive index was increased by 0.1 than the recipe #1. High refractive index

usually means low hydrogen content or high defect densities in the a-Si:H flim, ellipsometry measurement showed low extinction coefficient [13, 15, 16].

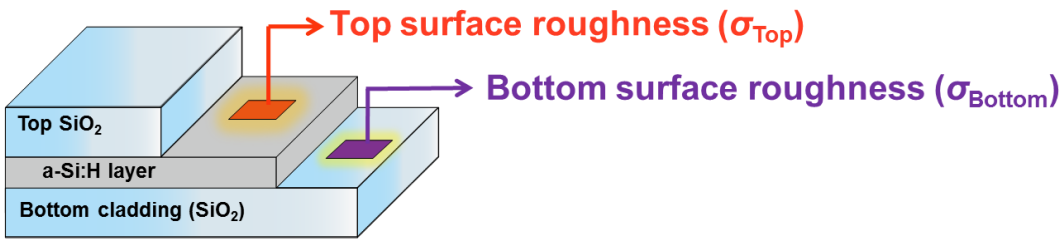


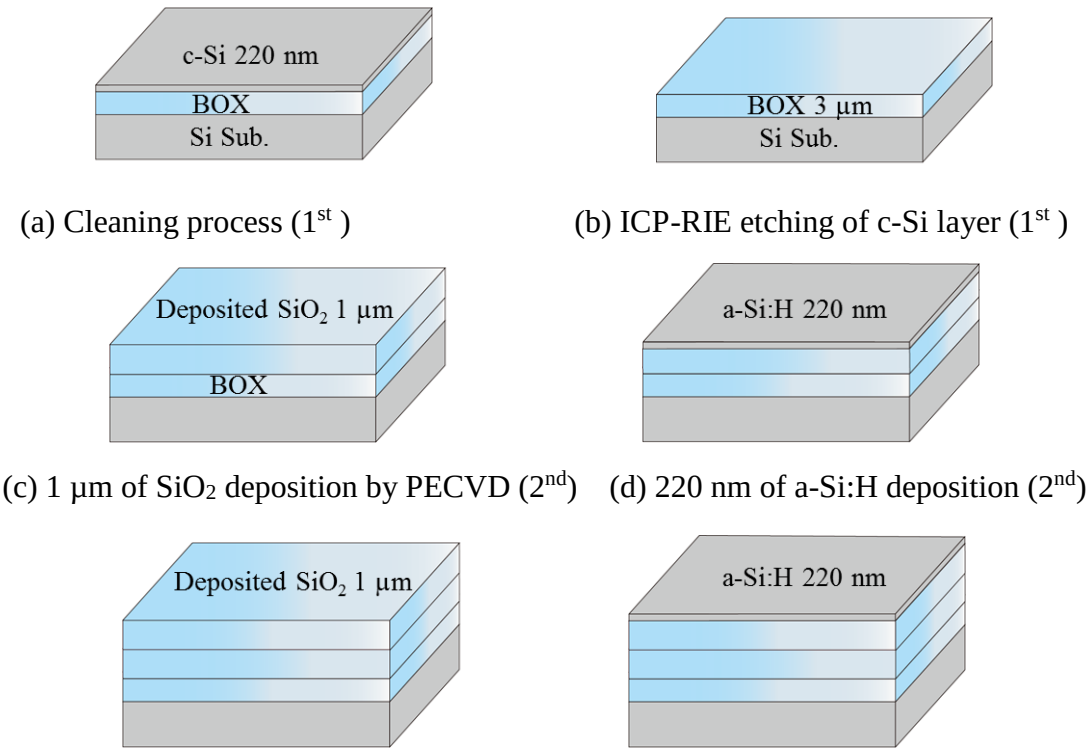
Figure 2. 11 Top and bottom surface roughness of the a-Si:H film.

2.4 Surface roughness and propagation loss in multi-layered a-Si:H

2.4.1 Surface roughness of multi-layered a-Si:H film

As the a-Si:H film have low material loss, the surface roughness are the key issues on the 3D optical integration in terms of the propagation loss. Such a 3D integration of a-Si:H waveguides can be achieved by stacking a-Si:H film and SiO_2 alternately. Thus, we should take a look at not only the surface roughness of the a-Si:H but also that of SiO_2. The surface roughness of the SiO_2 will be the bottom surface roughness of the a-Si:H layer. These are illustrated in Figure 2. 11. The surface roughness of the a-Si:H layer is expressed as σ_{Top} and the surface roughness of the SiO_2 is expressed as σ_{Bottom}.

The deposition conditions for a-Si:H layer used here were recipe #1 and #21. In this experiment, a-Si:H layers was stacked up to 3rd layer. The fabrication process is explained in Figure 2. 12. Figure 2. 12 (a) and (b) illustrates the fabrication process of samples for σ_{Top} and σ_{Bottom} measurement. Multi-stacked a-Si:H layers were fabricated on SOI wafer consisting of a 3-μm buried oxide (BOX) layer and a 220-nm c-Si layer. The SOI wafer was diced out from the 6 inch wafer to the 1×1.6 cm^2 with deposited 100-nm-thick SiO_2 cover layer. After removing the SiO_2 layer by 7% BHF, the SOI chip was cleaned by the cleaning process #1. The surface roughness of the c-Si layer was measured as σ_{Top} of the 1st layer. Then, c-Si layer of another chip, processed as described above, was etched by



(a) Cleaning process (1st) (b) ICP-RIE etching of c-Si layer (1st)

(c) 1 µm of SiO_2 deposition by PECVD (2nd) (d) 220 nm of a-Si:H deposition (2nd)

(e) ICP-RIE etching and SiO_2 deposition (3rd) (f) 220 nm of a-Si:H deposition (3rd)

Figure 2. 12 Samples for surface roughness measurement.

Table 2. 11 Surface roughness of each layer (RMS value)

Measured point	1st layer	2nd a-Si:H layer		3rd a-Si:H layer	
	Crystalline Si (c-Si)	130 Pa	30 Pa	130 Pa	30 Pa
σ_{top} (nm)	0.17	1.06	0.30	1.03	0.52
σ_{bottom} (nm)	0.18	0.24	0.24	0.37	0.36

ICP-RIE. Etching recipe with CF_4 gas of ICP-RIE was also used for the waveguide formation in chapter 2.3.2. In this experiment, the surface roughness of the exposed BOX layer was assumed to be σ_{Bottom} of the 1st c-Si layer.

σ_{Top} and σ_{Bottom} for the 2nd a-Si:H layer were then measured by samples illustrated in

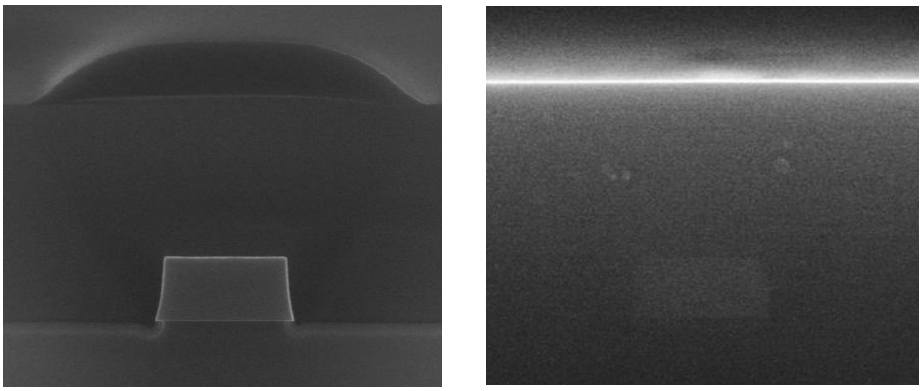
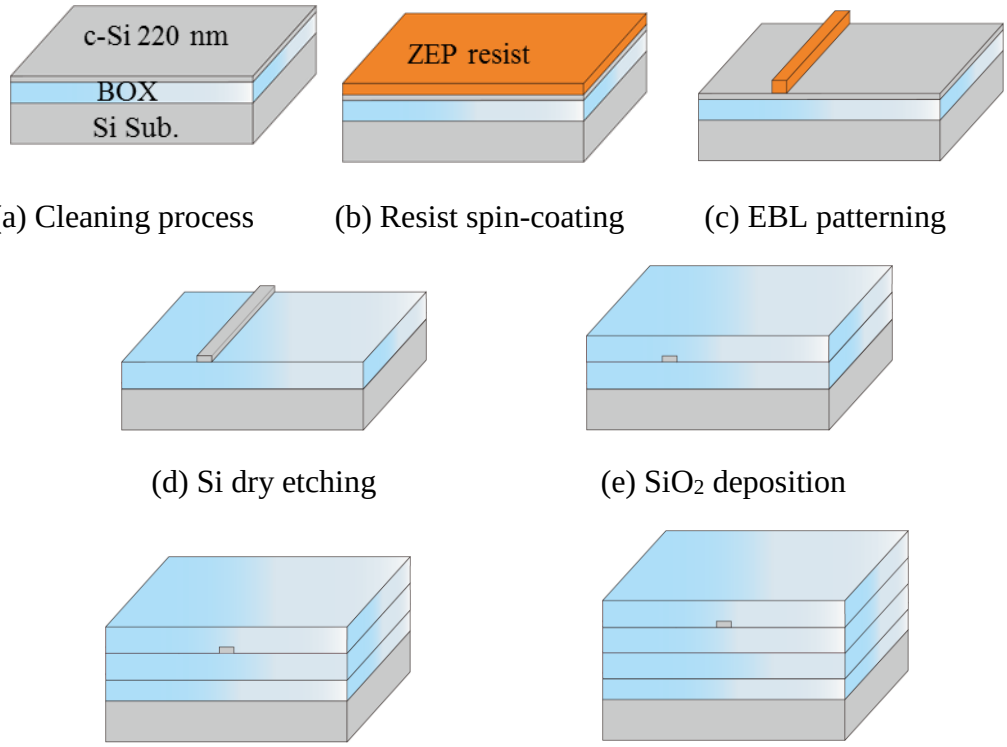


Figure 2. 13 Before and after the CMP process.

Figure 2. 12 (c) and (d). 1-μm-thick SiO_2 layer was deposited on the BOX layer. The surface roughness of this SiO_2 layer is σ_{Bottom} of 2nd a-Si:H layer. Then, 220-nm-thick a-Si:H layer was deposited as a 2nd layer. The surface roughness of the 2nd a-Si:H layer was taken as a σ_{Top} of the 2nd a-Si:H layer.

σ_{Top} and σ_{Bottom} of the 3rd a-Si:H layer were obtained by repeating the above process as done in 2nd a-Si:H layer. All the measured σ_{Top} and σ_{Bottom} of each layer are summarized in Table 2. 11. The surface roughness of the 1st layer were lowest in this experiment. σ_{Top} was 0.17 nm and σ_{Bottom} of 1st c-Si layer was 0.18 nm. Then, σ_{Bottom} of 2nd a-Si:H layer was 0.24 nm which was slightly increased than the σ_{Bottom} of c-Si layer. σ_{Bottom} of the 2nd a-Si:H layer was clearly distinguished by the deposition condition as noted in chapter 2.2. When the deposition pressure was 30 Pa, the surface roughness was 40~50% higher after the deposition of the a-Si:H layer and approximately twice and thrice that of the c-Si layer after the deposition of the second and third a-Si:H layers, respectively.

In addition to this, higher σ_{Bottom} of the 3rd a-Si:H layer than the 2nd a-Si:H layer indicated the accumulation of the surface roughness. If we consider the multi-stacking of the a-Si:H layer more than 3rd layer, improvement of the surface roughness by CMP will be needed [17-19]. By the CMP process, the surface roughness can be improved to the level of c-Si and the uniform surface at any layers can also be obtained for multi-stacked layers. Figure 2. 13 shows before and after the CMP process of waveguides buried by SiO_2. Measured surface roughness was 0.31~0.39 nm which is comparable to that of 0.36 nm of σ_{Bottom} at 3rd layer.



(a) Cleaning process (b) Resist spin-coating (c) EBL patterning

(d) Si dry etching (e) SiO_2 deposition

(f) 2nd layer a-Si:H waveguide (g) 3rd layer a-Si:H waveguide

Figure 2. 14 Fabrication process of multi-layered a-Si:H waveguides

2.4.2 Fabrication of multi-layered Si waveguides

As a next step after confirming the surface roughness of the multi-stacked a-Si:H layers, multi-layered a-Si:H waveguides have been fabricated. In this experiment, the material for 1st layer waveguide was c-Si in order to simplify the fabrication process. The fabrication process is similar to the fabrication process used for making samples of surface roughness measurement shown in Figure 2. 12 except waveguide formation. Fabrication process of multi-layered waveguides are presented in Figure 2. 14.

For the simple fabrication process, 1st layer c-Si waveguides, 2nd layer a-Si:H waveguides and 3rd layer a-Si:H waveguides were fabricated on the separate chips. And we used conventional RIE and ICP-RIE with CF_4 gas.

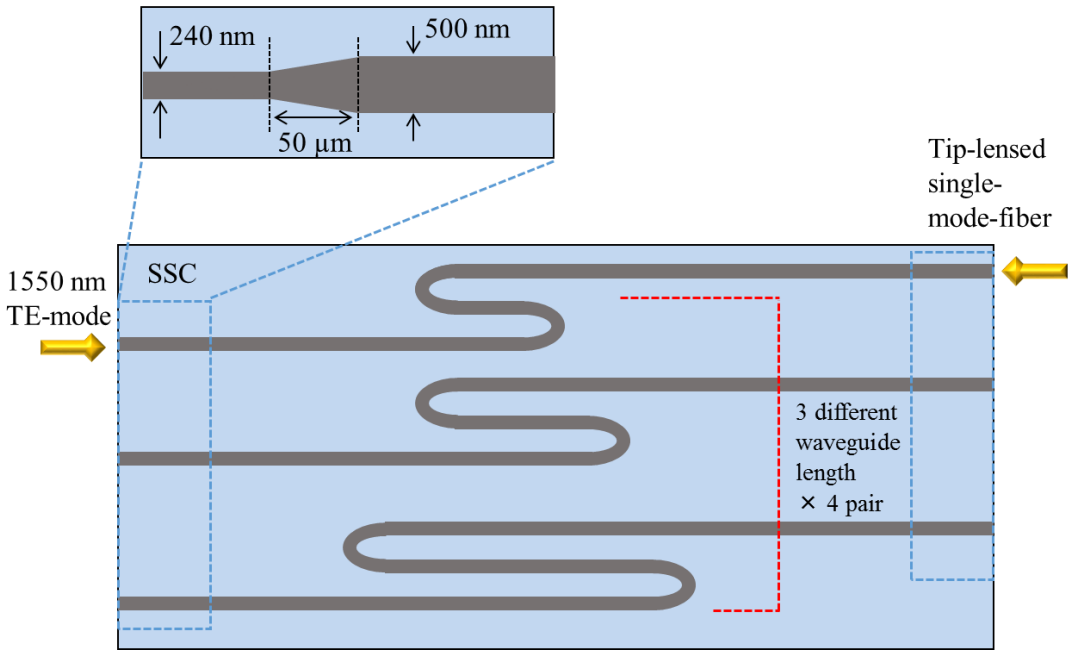


Figure 2. 16 Schematics of waveguide pattern for propagation loss measurement

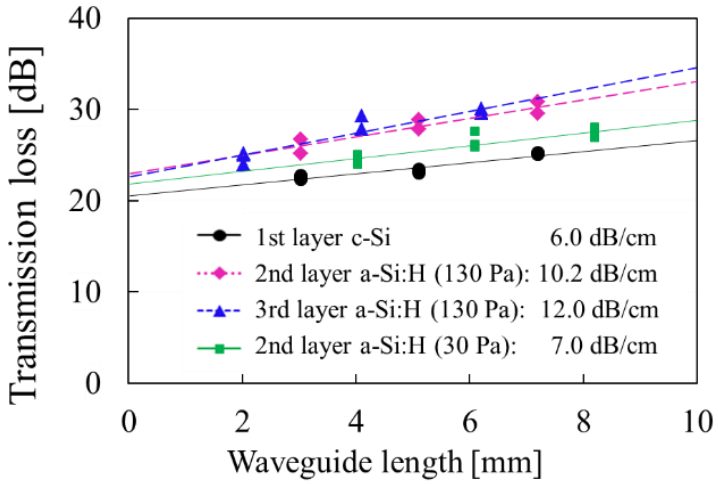


Figure 2. 15 Measured transmission losses against the propagation length of RIE-etched waveguides

2.4.3 Loss property of multi-layered Si waveguides

In this section, the measured propagation losses will be presented here. The propagation loss was estimated from the transmittance 4 pairs of three waveguides with

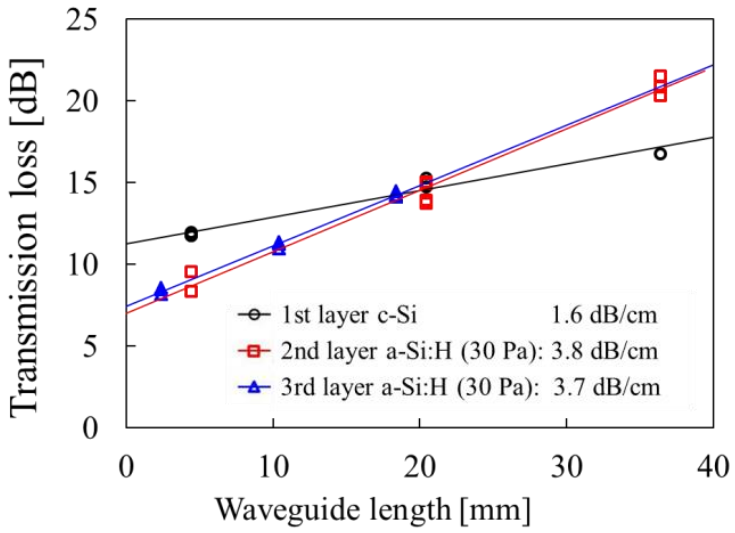
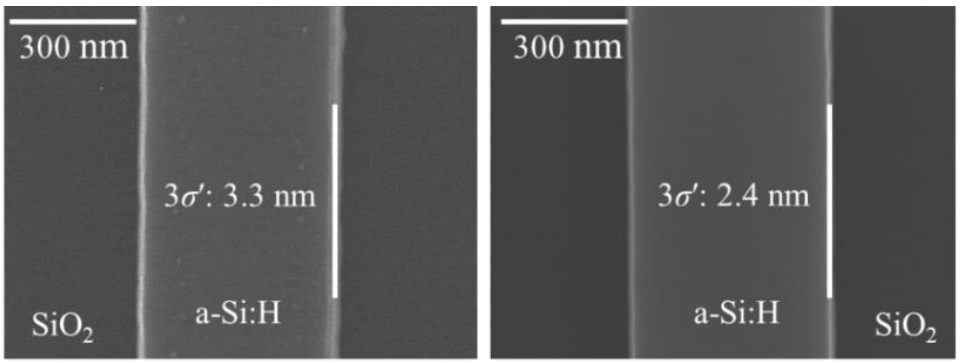


Figure 2. 17 Measured transmission losses against the propagation length of ICP-RIE-etched waveguides

different lengths. 2 kinds of deposition pressure of a-Si:H layer (30 Pa, 130 Pa) and 2 types of etching system (conventional RIE, ICP-RIE) were used.

Figure 2. 16 illustrates the schematics of the waveguide pattern for the propagation loss measurement. In order to achieve high coupling efficiency between tip-lensed single-mode-fibers and waveguides, inverse tapered type spot-size converters (SSC) are introduced between fibers and Si wire waveguides [20]. The input light was transverse electron (TE) polarized at C-band (1.55 μm). The coupling loss of 3 to 5dB/facet was obtained with this SSC compared to that of 10 to 12dB/facet without any SSC. After the input light coupled to the SSC, light was transferred to the 500-nm-wide Si wire waveguide through 50-μm-long linearly tapered mode-converter.

The propagation losses of the 1st layer c-Si (circles), the 2nd (squares) and the 3rd (diamonds) a-Si:H waveguides deposited at 130 Pa were 6.0 dB/cm, 10.2 dB/cm, and 12.0 dB/cm, respectively. The intercept of the transmission loss for each waveguide was higher than 20dB since SSC were not introduced for the conventional RIE-etched waveguides. The propagation losses of a-Si:H waveguides deposited at 130 Pa were nearly 2 time worse than that of c-Si waveguide. The propagation loss of the 2nd layer a-



(a) (b)

Figure 2. 18 Top view of SEM images of waveguides formed by (a) conventional RIE and (b) ICP-RIE

Table 2. 12 Propagation losses of multi-layered a-Si:H waveguides

Etching method	1st layer	2nd layer		3rd layer	
	(c-Si)	Pressure 130 Pa	Pressure 30 Pa	Pressure 130 Pa	Pressure 30 Pa
Con. RIE (dB/cm)	6.0	10.2	7.0	12.0	-
ICP-RIE (dB/cm)	1.6	-	3.8	-	3.7

Si:H waveguide deposited at the pressure of 30 Pa (tirangles) was 7.0 dB/cm. Even at the same 2nd layer, the propagation loss reduced from 10.2 dB/cm to 7.0 dB/cm by reducing the deposition pressure. It is because the scattering loss caused by the surface was reduced by improved surface roughness of a-Si:H layer. There was only 1 dB/cm difference between the 1st c-Si layer waveguide and the 2nd a-Si:H layer, which mean the quality of the a-Si:H is as high as c-Si.

For the waveguides formed by ICP-RIE system, the deposition pressure of 30 Pa only was used for a-Si:H. Figure 2. 17 shows measured propagation losses of the waveguides formed by ICP-RIE system.

The propagation losses of the 1st layer c-Si waveguide (circles) and the 2nd (squares) and 3rd layer (triangles) a-Si:H waveguides were measured to be 1.6 dB/cm, 3.8 dB/cm and 3.7 dB/cm, respectively. The propagation losses were under 4 dB/cm even with 3rd layer a-Si:H waveguide. Although the width of ICP-RIE-etched waveguides was wider (500 nm) than that (450 nm) for RIE-etched waveguides, the contribution for loss property was as low as 0.1 dB/cm. Therefore, the additional 3~4 dB/cm improvements were obtained mainly thanks to reduced sidewall roughness [21, 22]. Top view of scanning electron microscope (SEM) images of a-Si:H waveguide formed by conventional RIE and ICP-RIE are shown in Figure 2. 18. From the SEM images, the sidewall roughness (3σ' values) were measured as 3.3 nm and 2.4 nm respectively. And the scattering loss at the sidewall, α_{sidewall}, as a function of sidewall roughness, σ_{sidewall}, can be expressed as follows.

$$\alpha_{sidewall} = \frac{\sigma_{sidewall}^2}{\sqrt{2}k_0 d^4 n_1} gf \quad \text{.....(2.1)}$$

k_0 is the free-space wave-vector, d is the half width of the waveguide, and n_1 is the index of the waveguide core. g and f are functions of various parameters defined by Payne and Lecey [23, 24].

As a summary, all the propagation losses of multi-layered a-Si:H waveguides and c-Si waveguides are listed in Table 2. 12.

2.4.4 Relationship between surface roughness and propagation loss

In this section, the relationship between the surface roughness and the propagation loss will be discussed using the measured data in chapter 2.3.3. The scattering loss at the surface, α_{surface}, of the waveguides can be expressed using Tien's formula as [25-27]

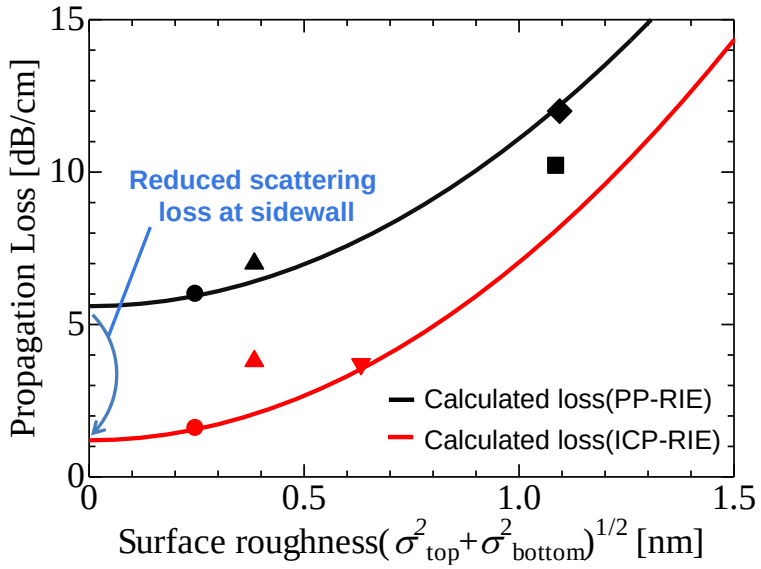


Figure 2. 19 Measured loses and calculated propagation losses against the surface roughness of the multi-layered c-Si and a-Si:H waveguides.

$$\alpha_{surface} = B^2\left(\frac{\cos^3\theta}{2\sin\theta}\right)\left(\frac{1}{h+\frac{1}{p}+\frac{1}{q}}\right) \quad \text{(2.2)}$$

$$B = \left(\frac{4\pi}{\lambda}\right)\left(\sigma^2_{top}+\sigma^2_{bottom}\right)^{\frac{1}{2}} \quad \text{(2.3)}$$

Here, θ is the angle of the propagation of rays in the waveguide; $1/p$ and $1/q$, are the penetration depths of the mode into the cladding (1/e width of the electric field); the values for θ, p and q were calculated by finite difference method; and h is the waveguide thickness. The sidewall roughness was assumed to be 3.3 nm (3σ' value) for the waveguides formed by conventional RIE and 2.4 nm (3σ' value) for the waveguides formed by ICP-RIE. The scattering loss at the sidewall was assumed to be 5.6 dB/cm (RIE) and 1.2 dB/cm (ICP-RIE) which is the value when the scattering loss at the surface is not exist.

The measured propagation losses against the sum of the RMS values of the top and bottom surface roughness values $(\sigma^2_{Top} + \sigma^2_{Bottom})^{1/2}$ is plotted in Figure 2. 19. The black line in the figure shows the calculated results of the scattering loss after consideration of

the surface roughness and the sidewall roughness. The plots of the measured propagation values agreed well with calculation results. This indicates that the primary cause of the propagation loss difference between the c-Si and a-Si:H waveguides is the scattering loss from the surface and not from the material absorption of a-Si:H.

2.5 Conclusion

In this chapter, fabrication process of Si waveguides pattern and multi-stacking of the Si waveguides were discussed. The propagation loss of the Si waveguides is severely depend on the fabrication process since it has strong confinement inside the waveguide core. Thus, the fabrication process was optimized and conducted by following the process recipes in chapter 2.2.

For the multi-stacked low loss a-Si:H waveguides, the deposition condition dependence of the surface roughness of the a-Si:H film was also investigated. As a parameter, deposition pressure, SiH_4 or Ar concentration, deposition temperature and applied power were carefully examined. The most influential factor was the deposition pressure. The deposition pressure of the initial recipe was 130 Pa and by the deposition pressure of 30 Pa, the surface roughness of the 2nd layer a-Si:H was improved from 1.06 nm to 0.30 nm. Even at the 3rd layer, the surface roughness was 0.52 nm.

Next, the propagation loss of the multi-layered waveguides were measured by TE-polarized light at C-band range. The propagation losses of the 1st layer c-Si, the 2nd and the 3rd layer a-Si:H waveguides deposited at 130 Pa were 6.0 dB/cm, 10.2 dB/cm, and 12.0 dB/cm, respectively. The propagation loss of the 2nd layer a-Si:H waveguides deposited at 30 Pa was 7.0 dB/cm. Improvement of the surface roughness showed the reduced propagation loss. Further, by introducing ICP-RIE system for the waveguide formation, the propagation losses were measured to be 1.6 dB/cm, 3.8 dB/cm and 3.7 dB/cm, for 1st layer c-Si waveguide, the 2nd and the 3rd layer a-Si:H waveguides, respectively.

Finally, the relationship between the surface roughness and the propagation loss was discussed numerically. From these results, it can be found that the primary reason of the propagation loss in a-Si:H waveguides is result of the scattering loss at the surface, not by the material loss of a-Si:H.

For further improvement of the surface and the sidewall roughness of the a-Si:H, roughness smoothing technics such as wet treatment [28] or introducing inter cladding layer would be effective for low-loss a-Si:H multi-layered waveguides [29].

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Chapter 3

Design of inter-layer grating couplers

3.1 Introduction

To realize 3D optical interconnects, not only the multi-stacking technology of a-Si:H waveguides as described in chapter 2 but the vertical couplers between multi-layered waveguides are also necessary. As mentioned earlier in chapter 1.4.2, the inter-layer

distance must be maintained around 1 μm in terms of optical isolation. As a solution for this coupling distance, inter-layer grating couplers were proposed in this chapter. Not like the directional coupler type vertical couplers or other vertical couplers using evanescent light for the coupling mechanism, light diffracted by the grating couplers will radiate more than tens of μm and then can be coupled by the same grating coupler at an ideal condition.

Remaining problem is how to design the grating couplers. There are many parameters for designing the grating couplers even if we consider only the gratings, for example; grating period, depth, duty ratio and number of periods.

The coupling efficiency is another problem. Typical grating couplers for fiber to waveguide connection have relatively low coupling loss higher than 3dB [1-3].

In this chapter, designing procedures of inter-layer grating couplers will be presented with 3 models. First, inter-layer grating couplers with simple structure will be explained. Then in order to improve the coupling efficiency, inter-layer grating couplers with metal mirrors will be presented. Finally, inter-layer distance-independent operation of inter-layer grating couplers by apodization of grating will be explained.

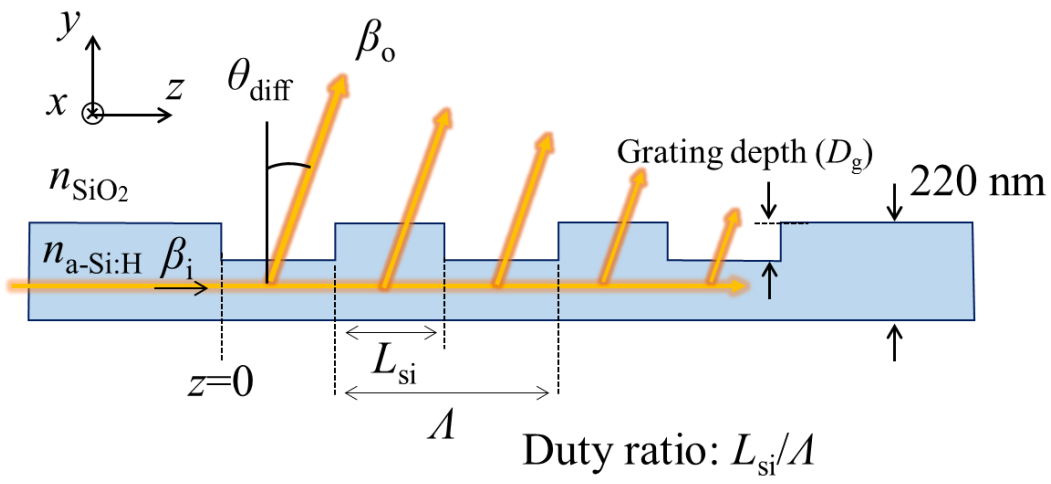


Figure 3. 1 Diffraction of light by grating

3.2 Basic Principles of grating couplers

Just like it sounds, grating couplers are using gratings. The grating coupler was firstly proposed by M. Dakss et al. in 1970 on a glass film as surface plasmon polariton wave is guided by metal gratings [4, 5]. If the light propagate through grating then, it will diffracted to the certain direction depending on the grating period. In other words, certain diffraction angle can be achieved by changing the grating period. When the grating period in optical length is equal to the quarter of the wavelength, the grating will act like a distributed bragg reflector (DBR) [6]. There are many reports dealing with the gratings or grating couplers numerically [7-10]. In addition to these reports, general idea of the grating couplers will be introduced here.

Figure 3. 1 illustrates the diffraction of light caused by the grating. Input light propagate with a propagation constant of β_i and diffracted light with a diffraction angle of θ_{diff} by the grating (grating period: Λ) has a propagation constant of β_o. $n_{a\text{-}Si:H}$ and n_{SiO2} are the refractive indices of waveguide core and cladding layer, respectively. The duty ratio of the grating was defined as L_{Si}/Λ and Lsi is the length of the Si region which was not etched. The phase matching condition between the diffracted light from the grating next to each other is described as

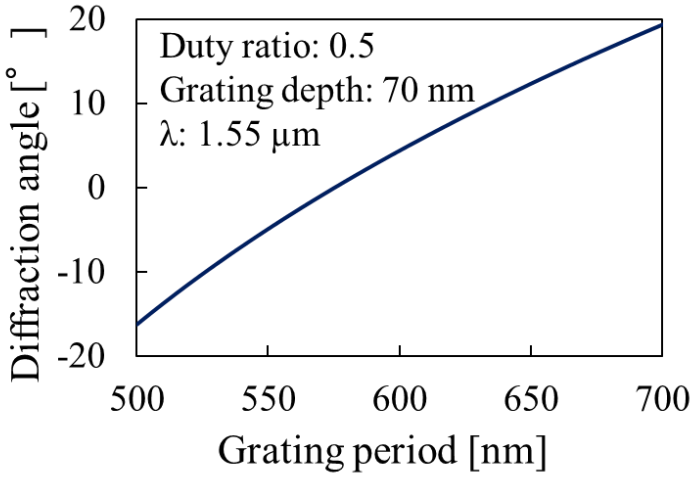


Figure 3. 2 Calculated diffraction angle against grating period. Parameters used in this calculation were brought from the values of a-Si:H grating coupler.

$$\beta_0 \Lambda \sin\theta_{diff} = \beta_i \Lambda + 2\pi m \quad \text{.....(3.1)}$$

m is the number of the diffraction order. The eq (3.1) can also be written as

$$n_{clad} \sin\theta_{diff} = n_{eq} + \frac{\lambda}{\Lambda} m \quad \text{.....(3.2)}$$

λ is the wavelength of the light and n_{eq} is the equivalent refractive index of the light in the waveguide. The -1 order of the diffracted light is usually used for the grating coupler and the grating coupler in this thesis also used diffraction order of -1. Higher order diffractions will occur with a longer grating period.

3.2.1 Grating period and diffraction angle

From the Eq. (3.2), the relationship between the grating period and the diffraction angle is expressed as

$$\theta_{diff} = \arcsin\left(\frac{n_{eq}}{n_{clad}} + \frac{\lambda}{\Lambda n_{clad}} m\right) \quad \text{.....(3.3)}$$

Although the Eq. (3.1), (3.2), and (3.3) are based on the approximation, basic relationship between each parameters can be understood from these equations. In this

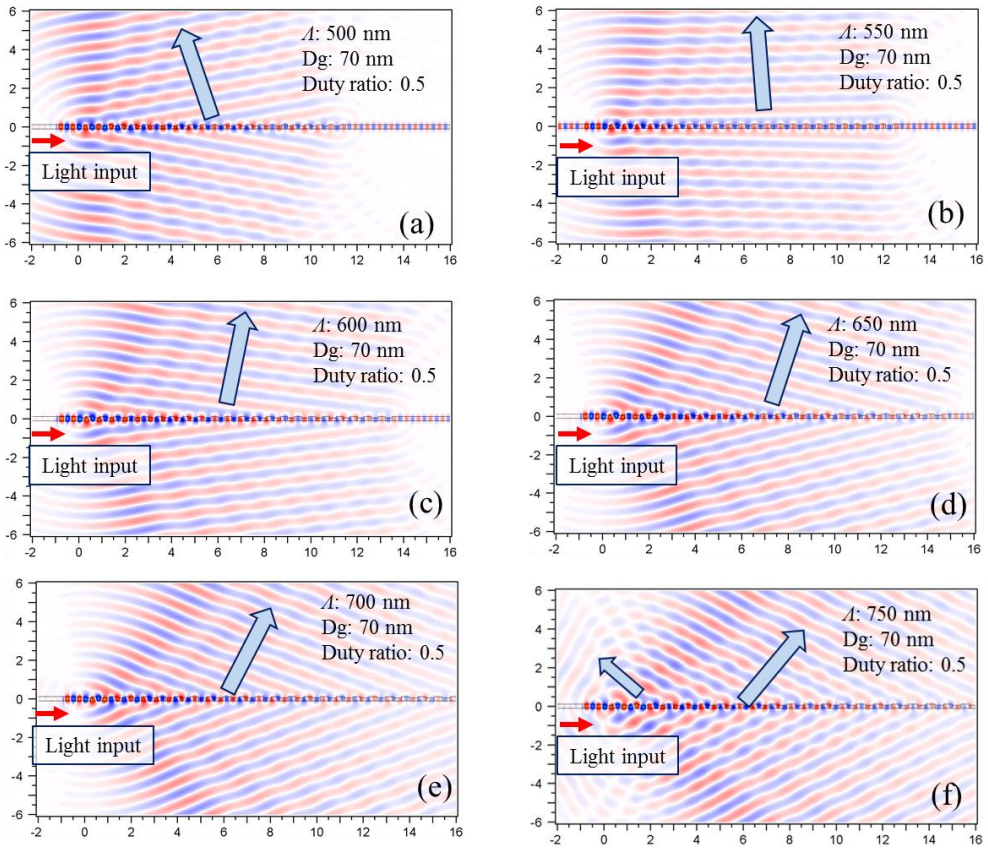


Figure 3. 3 Electric field distribution of diffracted light for various grating periods at λ=1.55 μm.

chapter, the wavelength λ is fixed to 1.55 μm for optical communication application unless mentioned.

Figure 3. 2 shows the calculated diffraction angle from the Eq. (3.3) using values of the a-Si:H grating coupler. Diffraction angle of 0° means the light diffracted perpendicular to the propagation direction. As the grating period increases, the diffraction angle also increases. The electric field distribution simulated by 2D finite-difference time-domain (FDTD) are given in Figure 3. 3. The grating periods were from 500 nm to 750 nm which were correspond from (a) to (f) and the duty ratio of the grating was 50% for all the simulation here. Light input was from the left side and propagate through the grating which was at the center of the images. Additionally, when the Λ exceeded 750 nm, higher order diffraction was occurred at the opposite direction of the lower order diffraction.

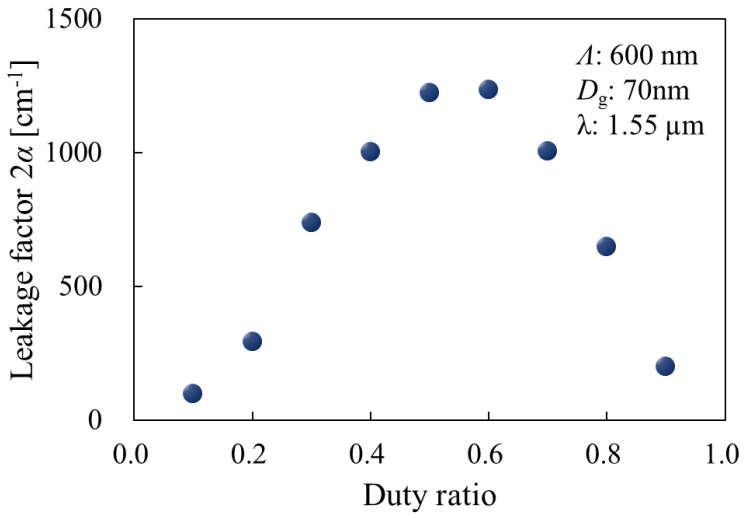


Figure 3. 4 Leakage factor against duty ratio.

3.2.2 Power leakage factor of grating

How much power will be diffracted by a grating coupler is depend on the grating structure. Duty ratio, grating depth D_g are the main parameters of the unit leakage factor, 2α. In this section, the unit leakage factor will be calculated and discussed with simulation results.

Figure 3. 4 shows the relationship between the leakage factor and the duty ratio. Depending on the duty ratio, the leakage factor behaved periodically. When the duty ratio was less than 0.5, the leakage factor become higher with larger duty ratio. By using this region, the output light profile can be gradually modulated which is called as apodization. The apodization of grating will be further discussed in chapter 3.5 and chapter 5.2. Then, the leakage factor started to decreases with larger duty ratio from 0.6 to 0.9.

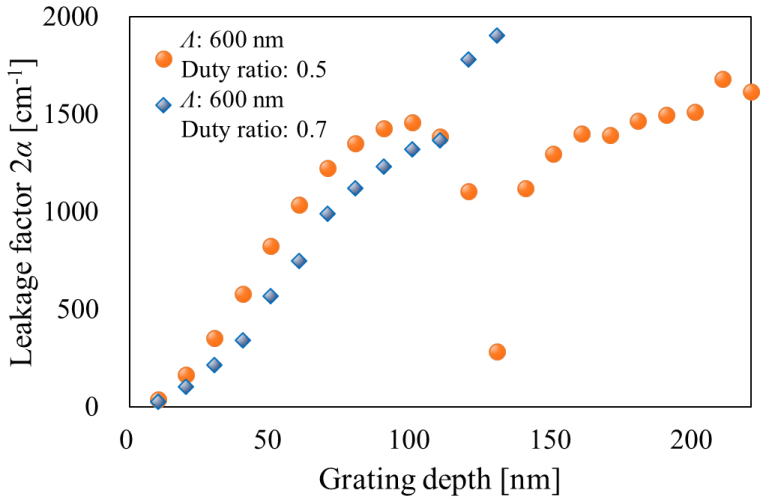


Figure 3. 5 Leakage factor against grating depth D_g.

In addition to the duty ratio, grating depth also affects the leakage factor as shown in Figure 3. 5. The leakage factor was increased when the grating depth was between 10 nm to 100 nm. When the grating depth was 130 nm and the duty ratio was 0.5, the leakage factor showed steep drop. It was caused by increased backward reflection (0-order grating) suppressed -1 order diffraction of the grating coupler since the period of the grating became 2 times of that of DBR.

Basically, wider range of the leakage factor allows more flexible design of gratings, however if the duty ratio is close to 1 so that the groove length of the grating is too short, the depth of the grating would be hard to control by the RIE lag. Therefore, the grating depth and the duty ratio of the grating should be optimized considering the leakage factor and fabrication feasibility.

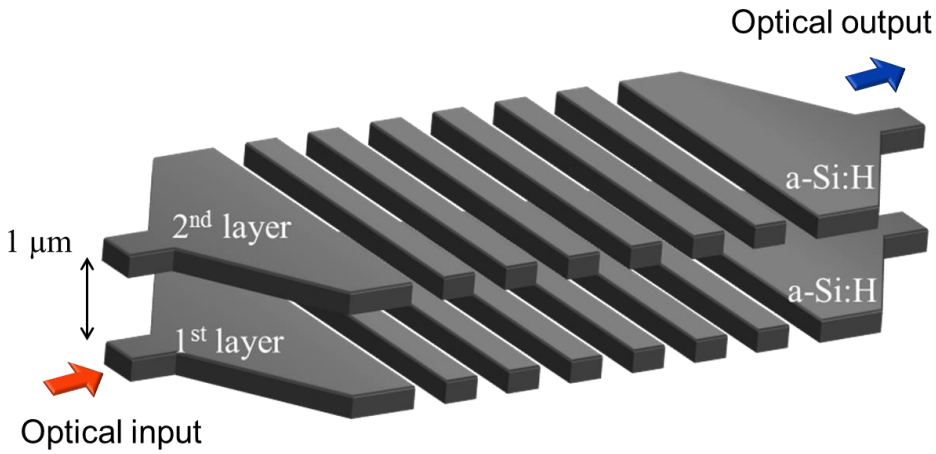


Figure 3. 6 Inter-layer grating coupler

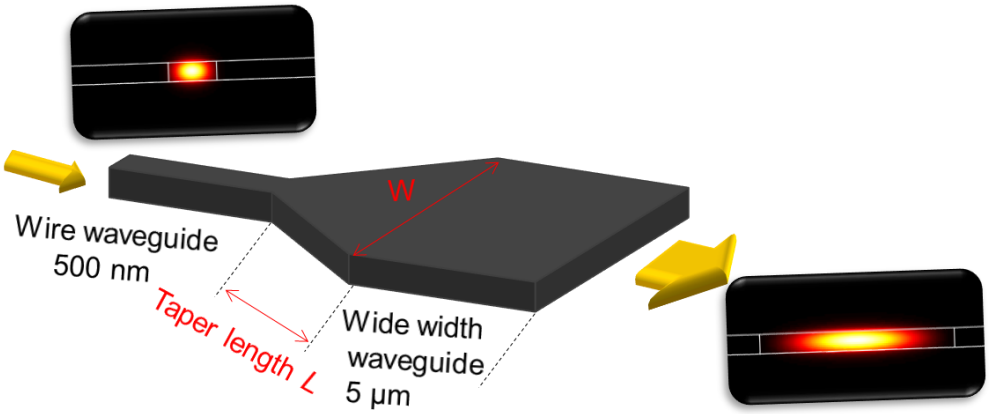


Figure 3. 7 Image of the taper between the wire waveguide and wide-width waveguide.

3.3 Inter-layer grating couplers without metal mirrors

As previously mentioned, double stacked grating couplers were proposed as a vertical coupler in multi-layered waveguides. The schematic of the inter-layer grating couplers are illustrated in Figure 3. 6. A 500-nm-wide a-Si:H wire waveguide was sued as a input of the grating couplers. The gratings were at the center of the grating couplers and the waveguide width of the grating region was 5 μm in order to improve the tolerance in alignment mismatch. A linearly tapered 200-μm-long structure was employed between

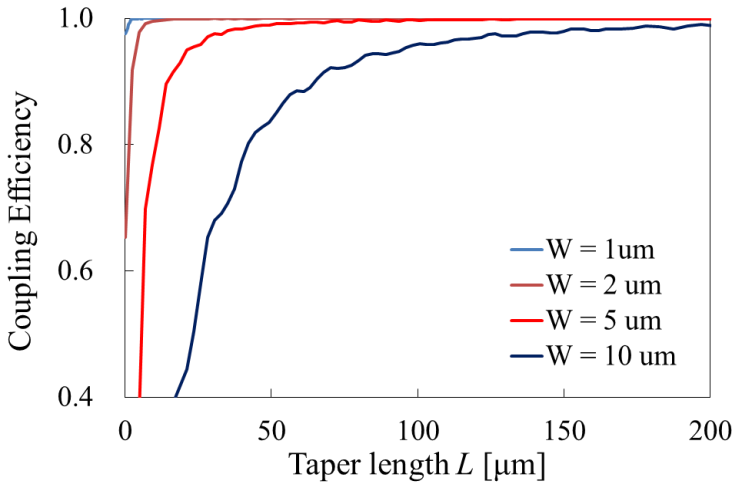


Figure 3. 8 Coupling efficiency of the taper between a-Si:H wire waveguides and wide waveguides

the wire waveguides and the 5-μm-wide waveguides to avoid reflection and excite only the fundamental mode in the wide waveguides as shown in Figure 3. 7. The coupling efficiency between the wire waveguides and the 5-μm-wide waveguides was saturated at the taper length longer than 50 μm (Figure 3. 8).

The gratings were designed according to a 3D FDTD simulation by monitoring the coupling efficiency of the inter-layer grating couplers. In this simulation, the refractive indices of a-Si:H and SiO_2 were set to be 3.48 and 1.45, respectively. The inter-layer grating couplers were assumed to be embedded by SiO_2 and the Si substrate under the inter-layer grating couplers or air cladding over the inter-layer grating couplers were not included in the simulation area in order to reduce the calculation time.

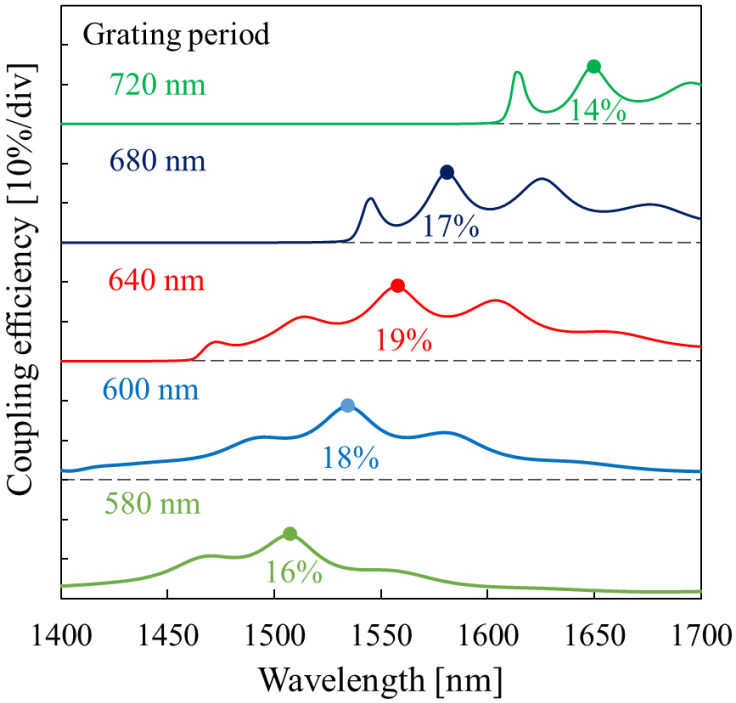


Figure 3. 9 Wavelength dependence of calculated coupling efficiency of the inter-layer grating couplers for various grating periods.

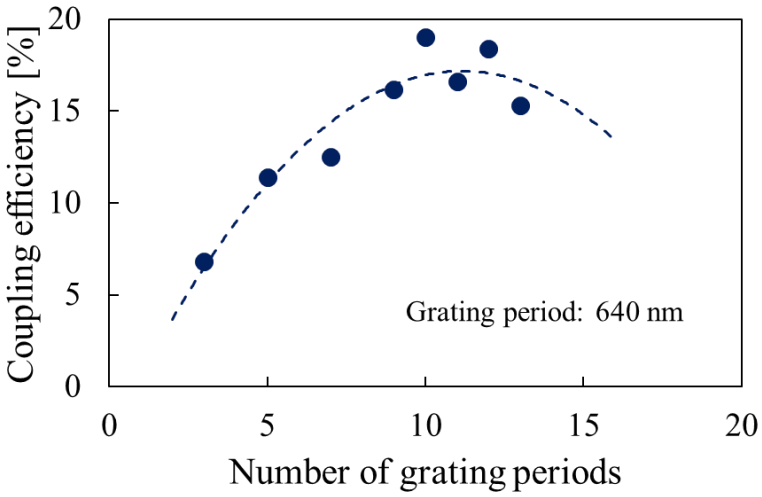


Figure 3. 10 Number of grating periods dependence of coupling efficiency.

3.3.1 Design of inter-layer grating couplers

Figure 3. 9 shows the wavelength dependence of the simulated coupling efficiency for 10 gratings with various periods. The grating periods were varied from 580 nm to 720 nm (duty: 50%). A red shift of the peak wavelength was observed with longer grating periods. The coupling efficiency also varied with the grating period, reaching a maximum coupling efficiency of 19% with a grating period of 640 nm. In each spectrum, there are several peak positions that can be explained by resonance between the full-etched gratings. These can be suppressed by changing the design of the grating.

The coupling efficiency is plotted against the number of grating periods at a wavelength of 1.55 μm in Figure 3. 10. The number of grating periods was varied from 3 to 13. Given that the light input is first coupled to another layer and then re-radiated by the gratings. The coupling efficiency depends on the number of grating periods but have a peak value at 10 gratings.

3.3.2 Misalignment tolerance

In order to confirm the fabrication tolerance, coupling efficiency difference by the shift of the inter-layer grating couplers were simulated here. The tolerance along to the propagation direction of the light and orthogonal to the propagation direction are shown in Figure 3. 11. The square and the circle plots are coupling efficiency differences caused by misalignment in the propagation direction and the orthogonal direction, respectively. There was only 1 dB difference in the orthogonal direction even with the misalignment of up to 1 μm and it was resulted from the widened waveguide width at the grating region. At the propagation direction, the coupling efficiency difference was much larger than the orthogonal direction, which was about 2.3dB at the misalignment of 1 μm. To keep less than 1dB degradation, the misalignment should be below 300 nm. By introducing shallow etched gratings, improvement of the misalignment tolerance can be expected since the

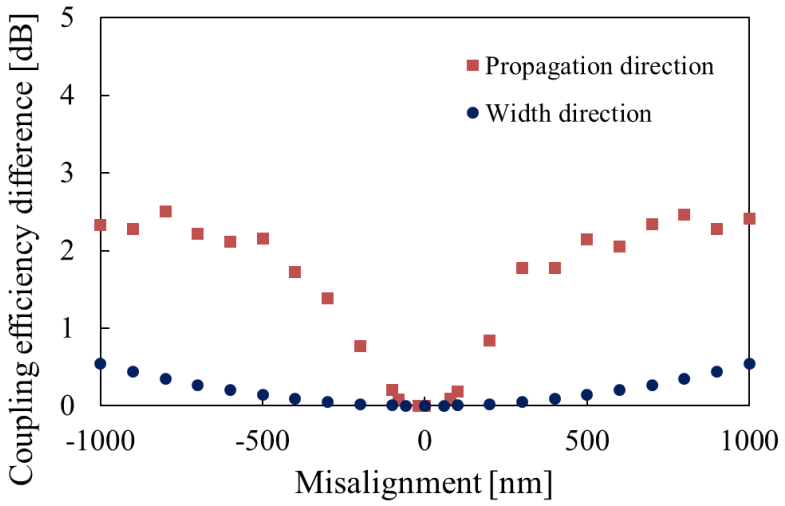


Figure 3. 11 Misalignment tolerance of the coupling efficiency.

Squares: Propagation direction, Circles: Orthogonal direction.

leakage factor of the shallow etched gratings will be lower than fully etched gratings and it will lead to the increased number of grating periods.

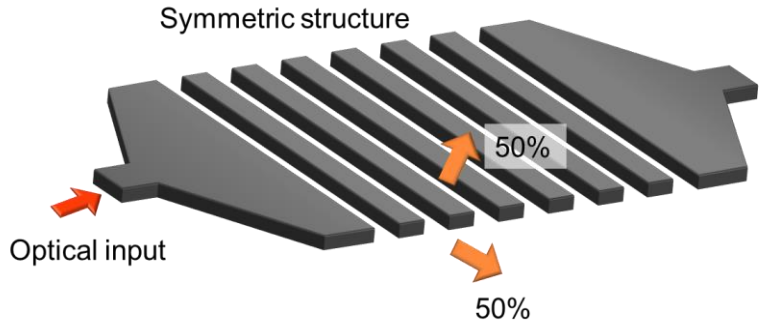


Figure 3. 13 Diffraction of light at the grating coupler when the structure is symmetric.

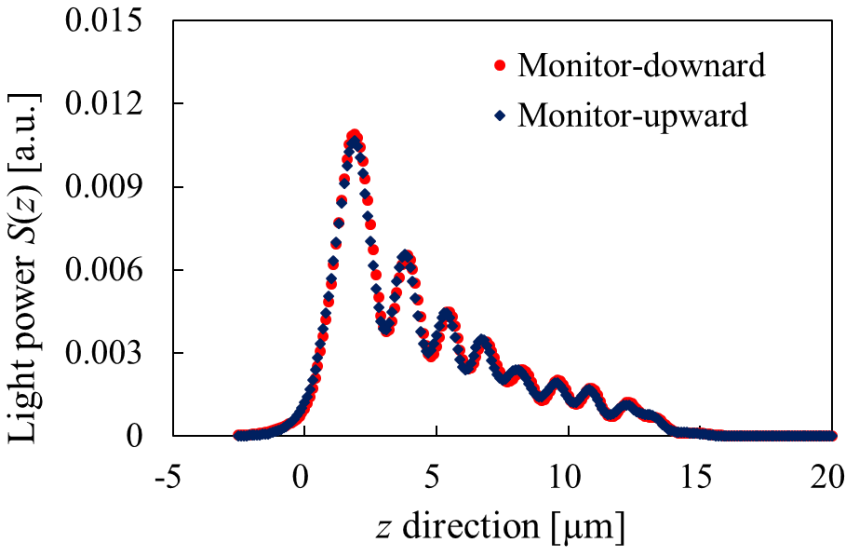


Figure 3. 12 Power distribution of diffracted light from grating.

3.4 Inter-layer grating couplers with metal mirrors

The coupling efficiency of the inter-layer grating couplers designed in chapter 3.3 was less than 20% even at the peak position. The reason of the low coupling efficiency was the symmetric structure of the grating couplers as shown in Figure 3. 13. When the input light was diffracted by the grating, the symmetric structure of the grating forced the light to be diffracted at the same ratio to the upward and downward. A similar procedure occurs at the other side of the inter-layer grating couplers. 50% of the received light at

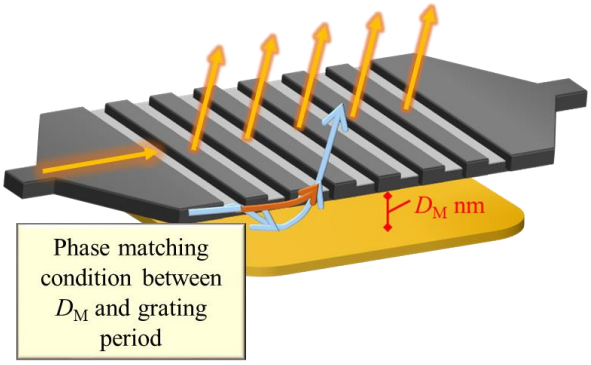


Figure 3. 14 Grating coupler with metal mirror.

the other side will not be coupled to the grating coupler so that the coupling efficiency will be limited by 25% at the worst case. In order to improve the coupling efficiency, double-etched gratings or poly-silicon overlay patterns had been reported to break the symmetric structure [11, 12].

Even with shallow etched gratings, which meant the structure was not symmetric anymore, the situation was not changed drastically. The power distribution of the diffracted light, $S(z)$, with shallow etched gratings is shown in Figure 3. 12. Red circles were power of the diffracted light heading upward and blue diamonds were that of downward. These plots also indicate that the light is diffracted upward and downward in halves.

In order to prevent the diffracted light being wasted, a metal mirror was introduced to the grating coupler as illustrated in Figure 3. 14. D_M is the distance from the metal mirror to the grating. Because there is a phase matching condition between the light passed through one period of grating and the reflected light from the metal mirror after diffracted from the grating, the power of the diffracted light become highest when the phase matching condition is satisfied. The phase matching condition can be approximately expressed as Eq. (3.4).

$$2D_M\beta_{SiO2}\cos\theta_0+\frac{\beta_{Si}d}{\cos(\frac{n_{SiO2}}{n_{Si}}\arcsin\theta_0)}+\Phi_M=2N\pi \quad (\mathrm{N}=1,2,3,\cdots) \quad \cdots\cdots\cdots\cdots (3.4)$$

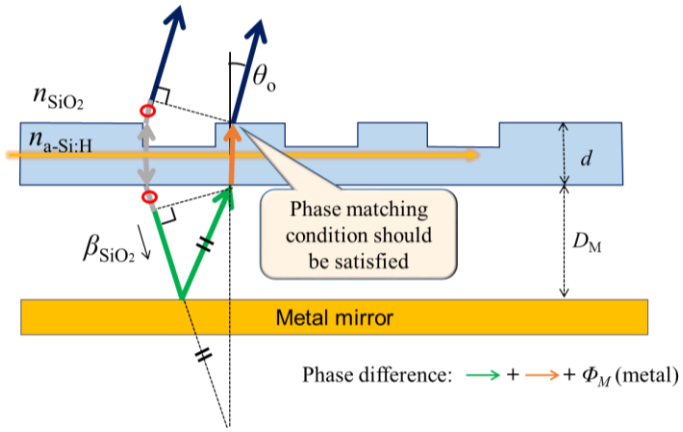


Figure 3. 15 Diffracted light power distribution with metal mirror.

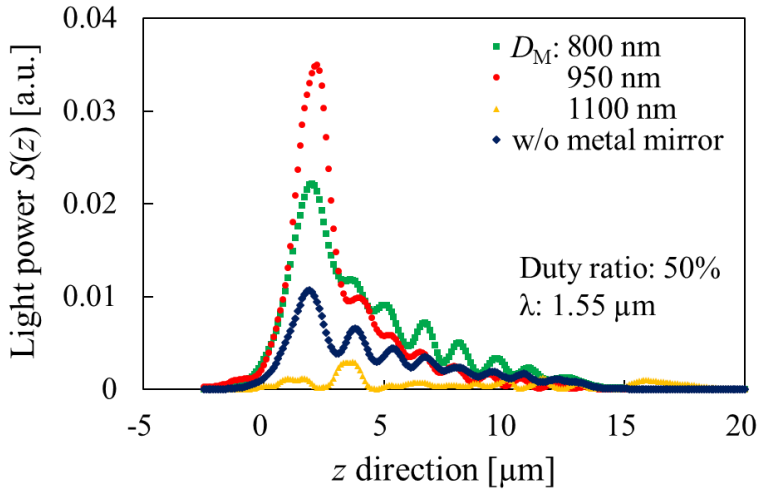


Figure 3. 16 Diffracted light power distribution with metal mirror.

β_{Si} and β_{SiO2} refer the propagation constant in the Si film and SiO_2, respectively. N is an integer number and Φ_M, which is 3rd term on the left side of the Eq. (3.4), means phase shift by the metal mirror. Φ_M can be expressed as Eq. (3.5) [13]. The illustration which expresses the Eq. (3.4) is shown in Figure 3. 15.

$$\Phi_M = \frac{\mathrm{Im}(r)}{\mathrm{Re}(r)},$$

$$r = \frac{n_{SiO2}\cos\theta_o - \sqrt{(\frac{n_{metal}}{n_{SiO2}})^2 - \sin^2\theta_o}}{n_{SiO2}\cos\theta_o + \sqrt{(\frac{n_{metal}}{n_{SiO2}})^2 - \sin^2\theta_o}} \quad \text{.....(3.5)}$$

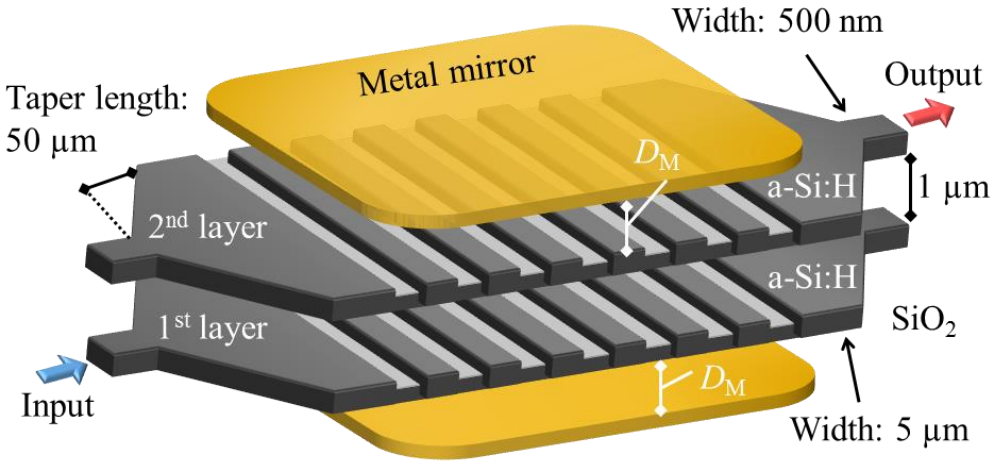


Figure 3. 17 Schematic image of inter-layer grating couplers with metal mirrors.

Figure 3. 16 shows the diffracted light power distribution with metal mirror when D_M is 800 nm, 950 nm or 1100 nm. The light power of the first peak is about 2 and 3 times larger than that of without mirror when D_M is 800 nm and 950 nm, respectively. If D_M is 1100 nm, the phase does not match any more and the leakage factor becomes very small. In addition to this, the diffraction angle is also changed slightly depending on the phase matching condition. Therefore, D_M should be carefully designed according to desired leakage factor or diffraction angle, etc.

The material for the metal mirror can be any metals if only they can provide high reflectivity at 1.55-μm-band. Au was used in this thesis since it was one of the available recipes in our group though, Al, Cu, Ag and Au can be used as the metal mirror. In particular, Al or Cu are CMOS compatible and cost effective material since they are commonly used in CMOS process such as damascene or dummy metal process [14, 15].

Figure 3. 17 illustrates the schematic image of the inter-layer grating couplers with metal mirrors. The inter-layer grating couplers consist of three parts: a taper section for smooth connection between the wire waveguides and wide-width waveguides, two-layered grating couplers, and metal mirrors. The tapers were between the wire and the wide-width waveguides as it was in chapter 3. A 50-μm-long linear taper was used here.

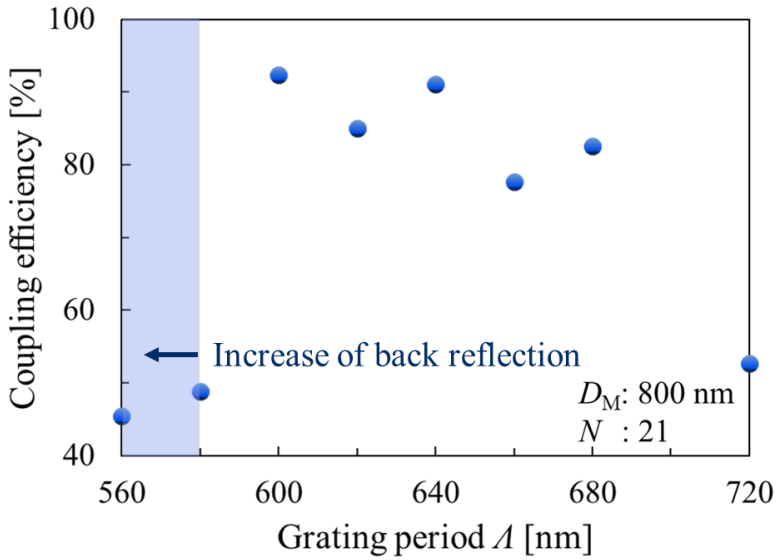


Figure 3. 18 Grating period dependence of coupling efficiency.

For the grating section, shallow etched (70-nm deep) gratings were used in order to suppress the backward reflection and leakage factor of the grating. Longer grating length and thus, improved fabrication tolerance can be expected with lowered leakage factor compared to the full-etched grating couplers. There was no offsets between the 1st and 2nd layer gratings also for the simple calculation. The inter-layer grating couplers were optimized by 3D FDTD simulations with 3 main parameters: grating period (Λ), the number of grating periods (N), and the distance from the gratings to the metal mirrors (D_M). The wavelength and the polarization were fixed at 1.55 μm, and only the TE-mode was considered in the simulations. The refractive indices of a-Si:H and SiO_2 were set to be 3.48 and 1.45, respectively,.

3.4.1 Design of inter-layer grating couplers with metal mirrors

Figure 3. 18 shows the grating period dependence with various grating periods ranging from 560 nm to 720 nm. Uniform gratings with duty cycle of 50% (in physical length) were used in order to simplify the calculation steps. In this calculation, D_M and N were

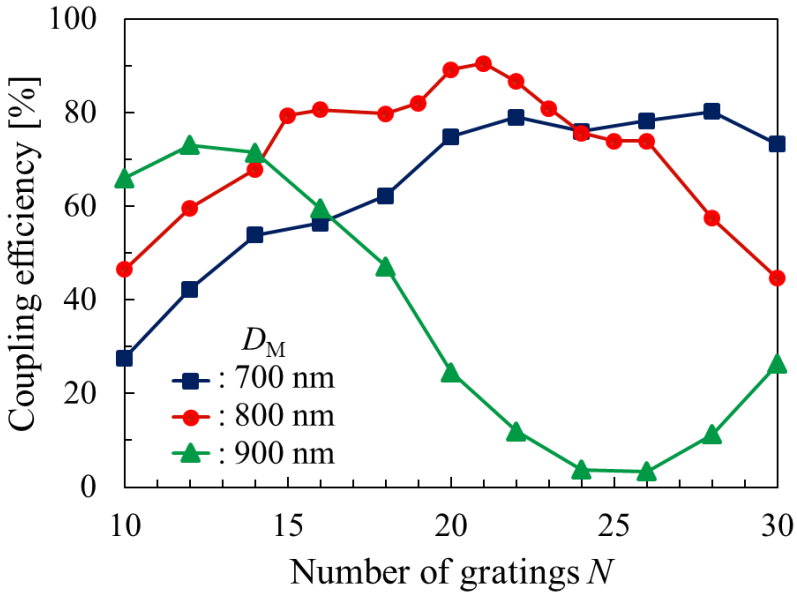


Figure 3. 19 Coupling efficiency as a function of number of grating periods for different metal distances.

fixed to be 800 nm and 21, respectively. The coupling efficiency of 92% and 90% were obtained at Λ of 600 nm and 640 nm, respectively, while it decreases at Λ of 620 nm because of the mismatch in mode profile between the diffracted light and the gratings deriving from the different diffraction angle. With a longer grating period, the peak wavelength of the coupling efficiency shifts to the longer wavelength. For the grating periods shorter than 580 nm, the backward reflection was increased and showed lower coupling efficiency. In this simulation, Λ of 640 nm was chosen instead of 600 nm in order to avoid the backward reflection in the case of the deviation in duty cycle or the thickness of the a-Si:H layer occurred due to the fabrication errors and the actual refractive-indices were different from those of used. Of course, if the grating periods is close to the backward reflection condition, the coupling efficiency will drop at the longer wavelength.

The second parameter is the number of grating periods N. The same N was used for both the 1st and the 2nd layer gratings. As N increases, the power transferred to the other side of the grating couplers will increase gradually and then, light will return to the original

grating coupler as it was in chapter 3.3. Figure 3. 19 shows N dependence of the coupling efficiency for three different D_M. Blue squares: D_M= 700 nm, red circles: D_M= 800 nm, and green triangles: D_M= 900 nm. The coupling efficiency has a peak at a certain number of grating periods as mentioned before. The highest coupling efficiency was obtained when D_M and N are 800 nm and 21, respectively. The coupling efficiency for different D_M takes a peak value at a different number of grating periods due to the phase matching condition between the light diffracted from the gratings and reflected light from the metal mirrors. Therefore, when the effective length of the light path, which is determined by the D_M value and the diffraction angle of the gratings, matches to the wavelength of the light, the peak coupling efficiency can be obtained.

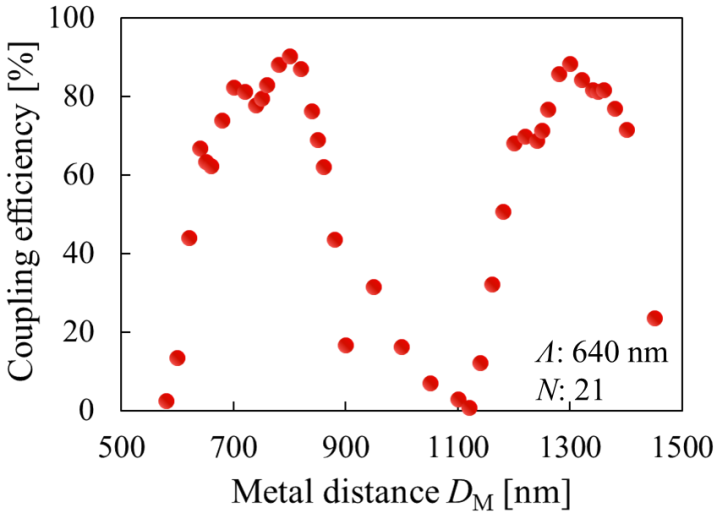


Figure 3. 20 Distance from the metal to the grating dependence of the coupling efficiency.

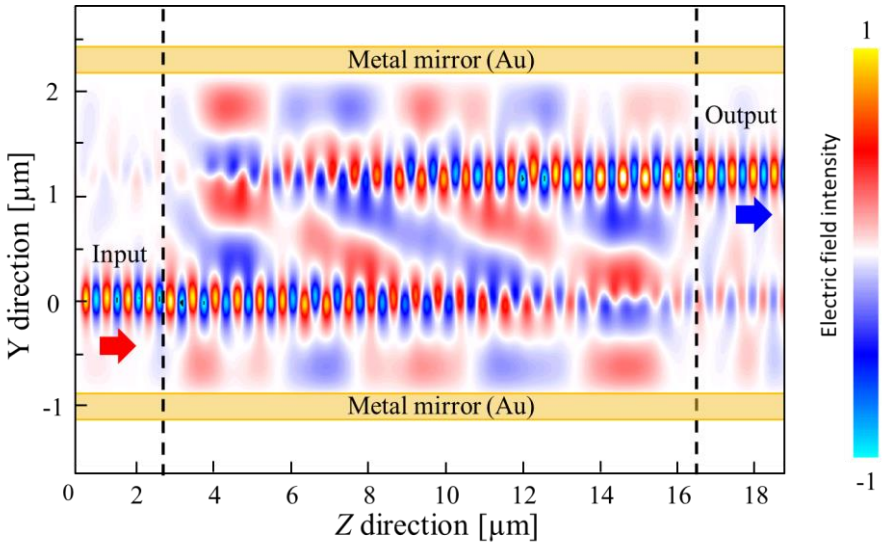


Figure 3. 21 Cross-sectional electric field distribution of the inter-layer grating couplers with metal mirrors.

Figure 3. 20 shows the D_M dependence of the coupling efficiency, where the grating period Λ and the number of the grating periods N are fixed to 640 nm and 21, respectively. The coupling efficiency showed periodic changes and took peak values at D_M of 800 nm

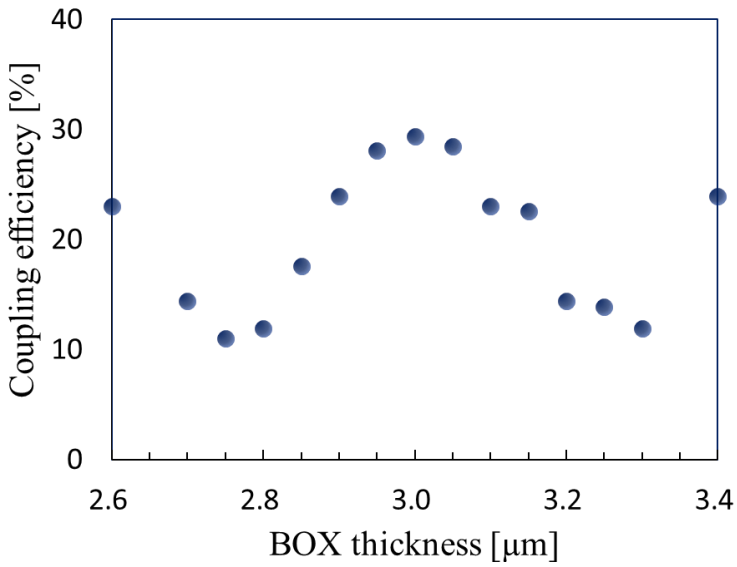


Figure 3. 22 Coupling efficiency of inter-layer grating couplers without metal mirrors as a function of BOX thickness.

and 1300 nm. In contrast, the coupling efficiency approaches 0% when D_M is 600 nm or 1100 nm. Hence, D_M is the key issue to control in the inter-layer grating couplers as explained with Eq. (3.4).

Figure 3. 21 shows the electric-field distribution (Specifically that of E_X, which is oriented along the orthogonal direction) with the parameters of Λ: 640 nm, N: 21 and D_M: 800 nm. The light input was from the left end of the 1st layer waveguide and output was at the right end of the 2nd layer waveguide. The X, Y, and Z directions were the orthogonal, vertical, and propagation directions, respectively. Diffraction angle of the beam was about 8 degree in this simulation.

3.4.2 Effect of metal mirrors

In order to confirm the contribution of the metal mirrors to the device performance, the coupling efficiency of the inter-layer grating couplers without metal mirrors was calculated. For the comparison, we used the same gratings (Λ: 640 nm, N: 21) and inter-

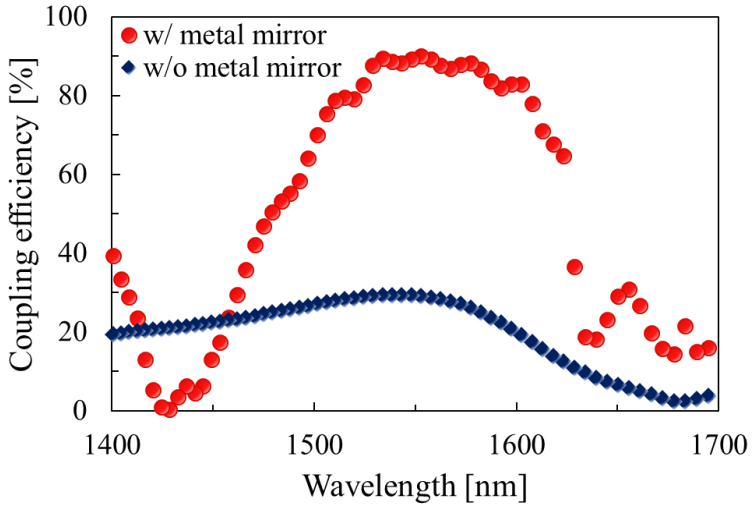


Figure 3. 23 Wavelength dependence of inter-layer grating couplers with and without metal mirrors (*Λ*: 640 nm, *N*: 21, D_M: 800 nm).

layer distance of 1 μm. In the case without metal mirrors, the reflection from the substrate under the BOX layer instead of the metal mirrors was considered in the simulation. For the phase condition of the reflected light, we varied the BOX thickness around 3 μm which thickness is a typical value for the photonic devices.

Figure 3. 22 shows the coupling efficiency as a function of the BOX thickness. Although the coupling efficiency can be further increased with optimization of the gratings, the maximum coupling efficiency of 30% can be obtained when the BOX thickness was 3 μm. The coupling efficiency of the inter-layer couplers with and without metal mirrors are shown in Figure 3. 23. By introducing the metal mirrors, the coupling efficiency was increased to 3 times higher value (90%) and the -1dB (coupling efficiency > 80%) bandwidth became 80 nm (from 1520 nm to 1600 nm), which can cover the full C-band wavelength range.

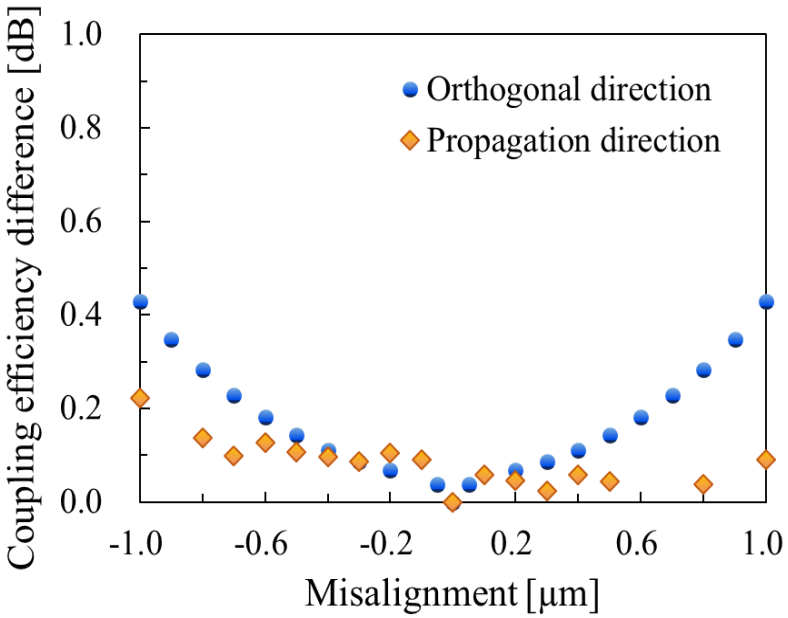


Figure 3. 24 Deviation of the coupling efficiency as a function of the misalignment in the propagation direction and the orthogonal (width) direction.

3.4.3 Misalignment tolerance

Because each part of the inter-layer grating couplers will be fabricated monolithically on a single substrate, the alignment between the gratings on each layer is difficult to correct after the fabrication stage. Therefore, tolerance to misalignment is important from a practical point of view. Tolerance to misalignment in the vertical direction was already discussed in terms of the parameter D_M (the thickness of the SiO_2). Here, we will consider the in-plane misalignment, in both the propagation direction and the orthogonal direction. As can be seen in Figure 3. 24, the deviation of the coupling efficiency is below 0.5dB even with a 1-μm misalignment for both the propagation and the orthogonal (width) directions. In addition, the coupling tends to be more tolerant to misalignment in the propagation direction, due to the larger dimension of the gratings in that direction, which was a length of ~13.5 μm compared to a width of 5-μm. This result can also be compare with the result of the inter-layer grating couplers in Figure 3. 11. 10 times better tolerance was obtained with shallow-etched 21 gratings than full-etched 10 gratings.

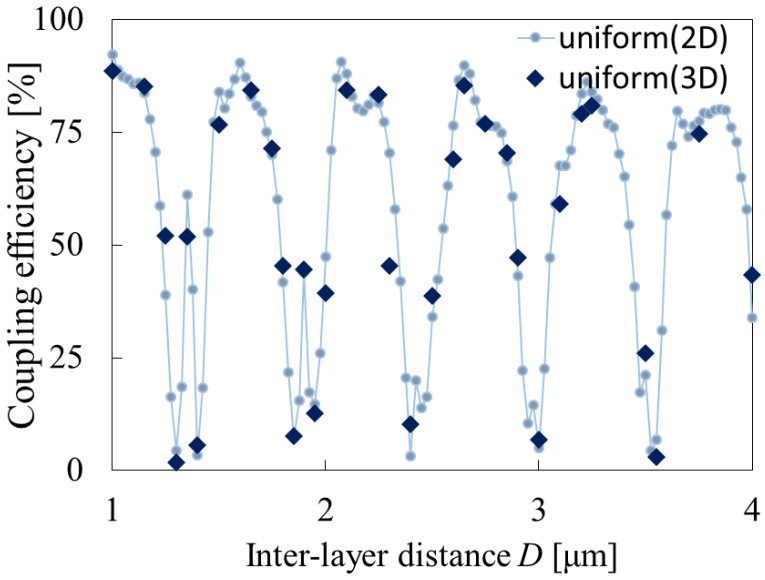
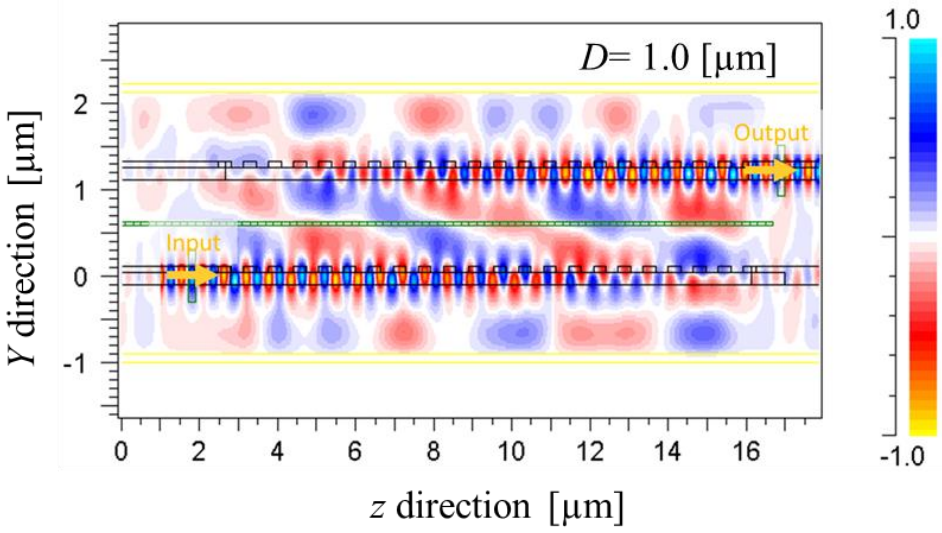


Figure 3. 25 Coupling efficiency as a function of inter-layer distance.

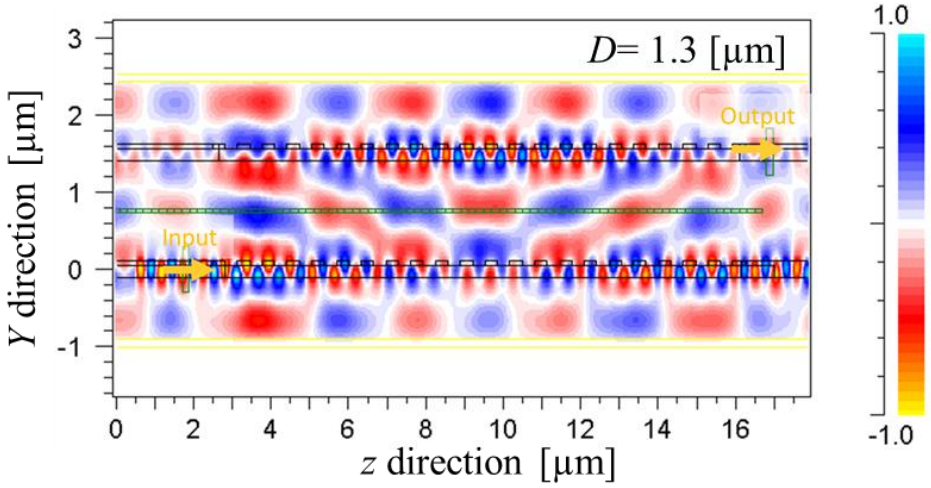
3.5 Inter-layer apodized grating couplers with metal mirrors

The inter-layer grating couplers with metal mirrors designed in chapter 3.4 can obtain 90% of the coupling efficiency at 1 μm inter-layer distance. If the coupling efficiency is maintained at the longer inter-layer distance, the inter-layer grating couplers can be used not only for the adjacent layer but also between far distant layers, for example coupling between the 1st layer and the 3rd layer. This inter-layer independent vertical coupler can further increase the flexibility of the 3D optical interconnects. The data presented in chapter 3.5 were mainly conducted by Y. Kuno.

Figure 3. 25 shows the coupling efficiency of the inter-layer grating couplers with metal mirrors as a function of the inter-layer distance. 2D and 3D simulations are plotted in it. The coupling efficiency showed periodic change according to the inter-layer distance. At the inter-layer distance of 2 μm, the coupling efficiency went down to less than 10%. In order to verify the reason of the inter-layer distance, the power distribution of the diffracted light inside the cladding layer was investigated. Figure 3. 26 shows the electric field distribution of the inter-layer grating couplers with metal mirrors when the inter-



(a)



(b)

Figure 3. 26 Electric field distribution of the inter-layer grating couplers with metal mirrors when the inter-layer distance is 1.0 μm and 1.3 μm.

layer distance is 1.0 μm or 1.3 μm. When the inter-layer distance was 1.3 μm, the input light was once coupled to the other side of the grating coupler and then, most of the power came out from the output waveguide of the 1st layer. The power distribution inside the cladding layer between the 1st and 2nd layer grating couplers are shown in Figure 3. 27. Figure 3. 27 (a) is the power distribution when the 2nd layer grating coupler is not exist.

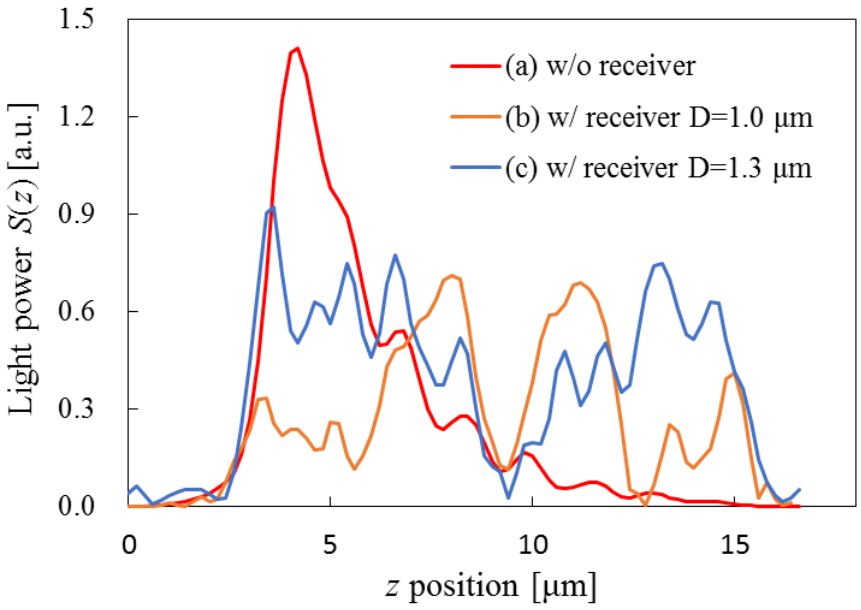


Figure 3. 27 Power distribution inside the cladding layer.

Without the 2nd layer grating coupler, the power density attenuated gradually. However, in the case of the 2nd layer grating coupler was exist, the power distribution produced symmetric configuration along the propagation direction. This is caused by the interference between the diffracted light and the light which was returned or reflected from the other side of the grating coupler. As the diffracted light propagated with a certain angle, the appearance of the interference was varied with each inter-layer distance.

3.5.1 Apodization of grating

As described earlier, in order to realize inter-layer distance-independent operation in grating couplers, returned or reflected light from the other side of the grating couplers should be suppressed. The reason for those retuned or reflected light was in the mismatch between the 1st layer grating coupler and the 2nd layer grating coupler as illustrated in Figure 3. 28. In the case of uniform gratings used in a grating coupler, the profile of output power of the 1st layer grating coupler, $S(z)$, and the 2nd layer grating coupler, $S'(z)$ was not

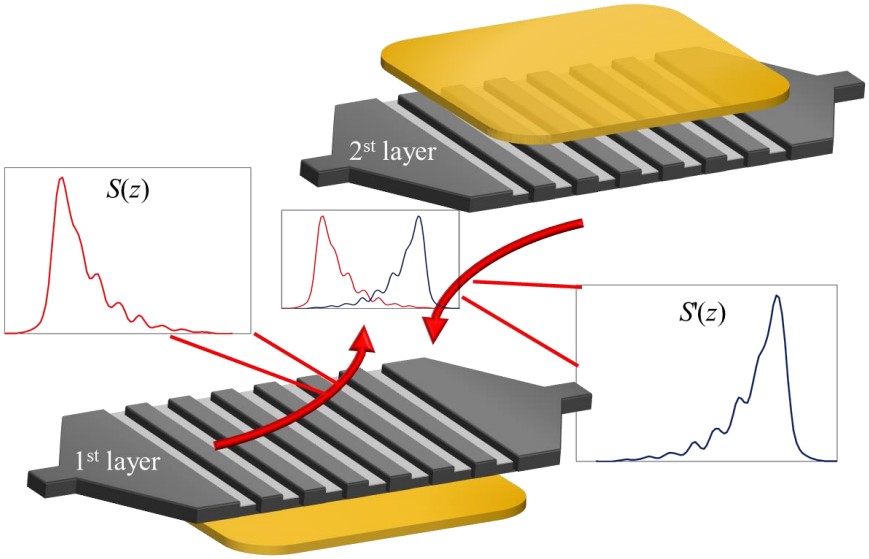


Figure 3. 28 Mismatch in output power profile between the 1st and 2nd layer grating coupler.

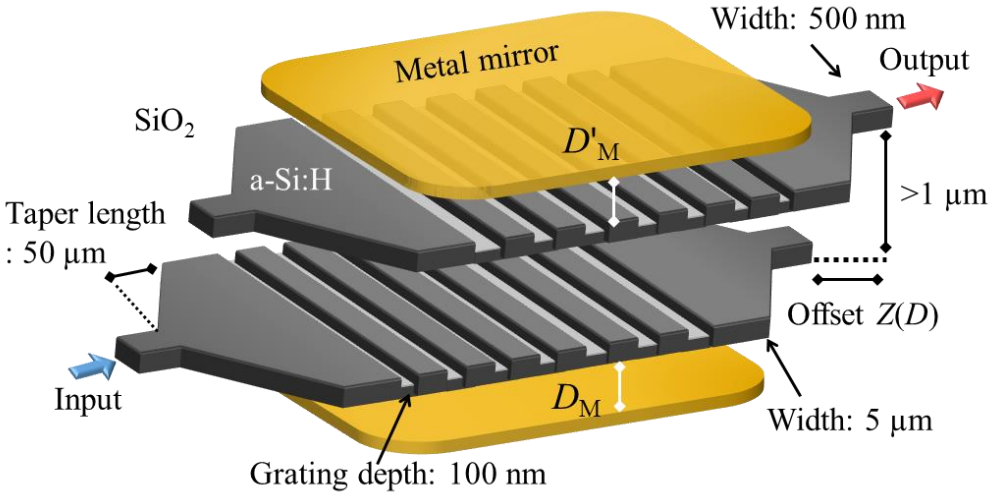


Figure 3. 29 Inter-layer apodized grating couplers with metal mirrors.

matched since the output power distribution was asymmetric. Therefore, $S(z)$ is need to be shaped as a symmetric distribution in achieving inter-layer distance independent coupling.

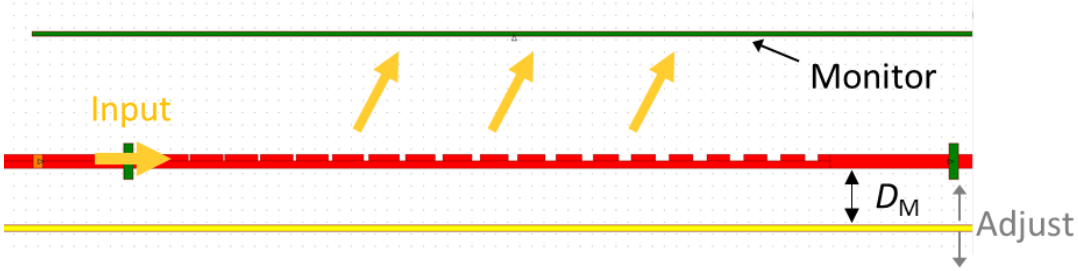


Figure 3. 30 Simulation model for determining D_M.

Apodization of grating is widely used to shape the output power distribution to Gaussian or fiber mode profile for fiber-to-waveguide grating couplers [11, 16, 17]. The meaning of apodization here is to shape the output mode-profile of the grating coupler by tuning the grating; for example, the grating period, duty ratio, or the grating depth. Not like the apodization of gratings in the fiber-to-waveguide application, the output profile of the grating in the inter-layer coupler does not need to be shaped to a certain profile like Gausian or fiber mode. Instead, any symmetric distribution would suppress the reflections and achieve the inter-layer independent coupling.

Figure 3. 29 illustrates the schematic image of the inter-layer grating couplers with metal mirrors. The first step of designing apodized grating was to decide the depth of the grating. In order to keep the number of grating periods close to 21 which was designed at chapter 3.4, the depth of the grating was set to be 100 nm to achieve the desired leakage factor. Then, the distance from the bottom metal mirror to the 1st layer grating, D_M, was determined regarding the leakage factor using a simulation model illustrated as Figure 3. 30. Total radiated power to the upper side was monitored while changing the D_M. When D_M was 940 nm, the total radiated power became maximum as shown in Figure 3. 31. In this simulation, D_M for the largest radiated power varies with the diffraction angle, so the grating period should be arranged to get the desired diffraction angle. Target of the diffraction angle was 10° in this simulation. In addition, D'_M, which is the distance from the top metal mirror to the 2nd layer grating, was also determined as done at D_M. Because the gratings were etched on the surface of the waveguides, there were difference in the

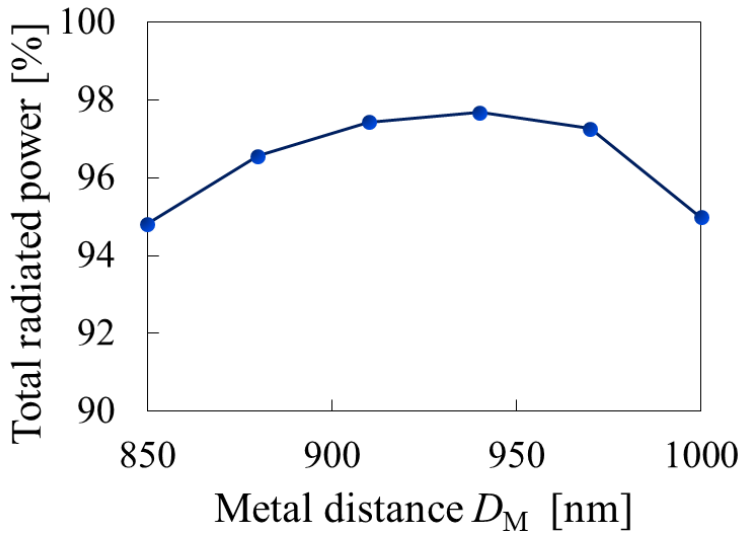


Figure 3. 31 Total radiated power dependence on D_M.

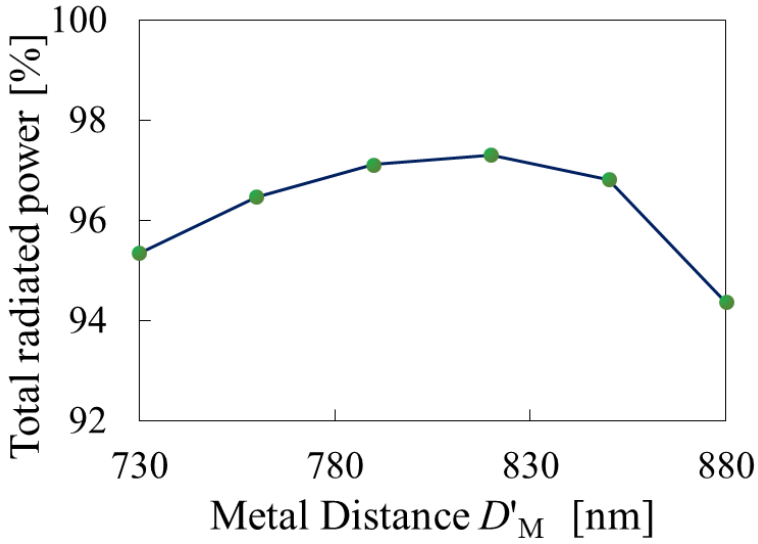


Figure 3. 32 Total radiated power dependence on D'_M.

length of the optical path between D_M and D'_M. $D`_M$ showed shorter optimized length of 820 nm compare to 940 nm for D_M as shown in Figure 3. 32.

Next step is to tune the grating period and the duty ratio. To begin with, required leakage factor for the target power profile $S'(z)$ could be calculated using the results shown in chapter 3.2.2 (Figure 3. 4) and following equation.

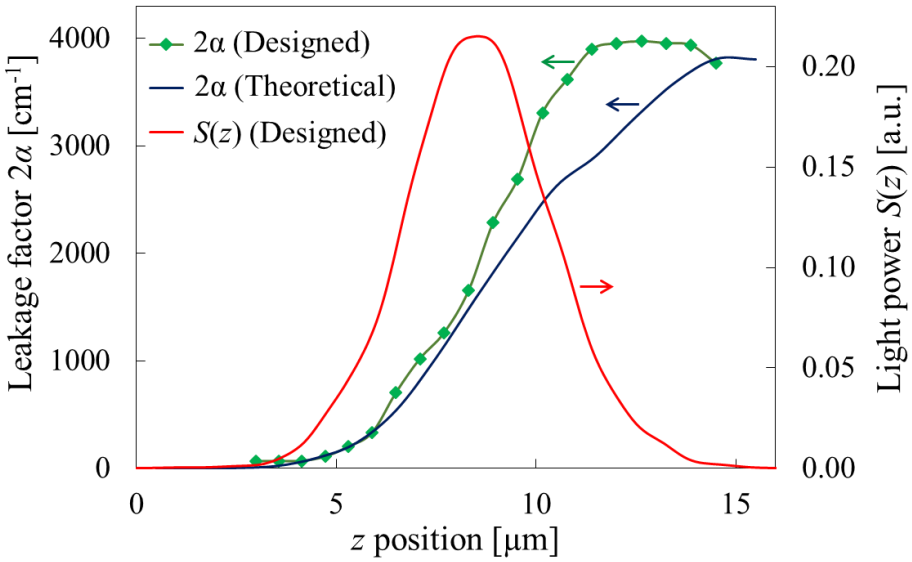


Figure 3. 33 Designed *S*(*z*) and 2*α* used for the grating.

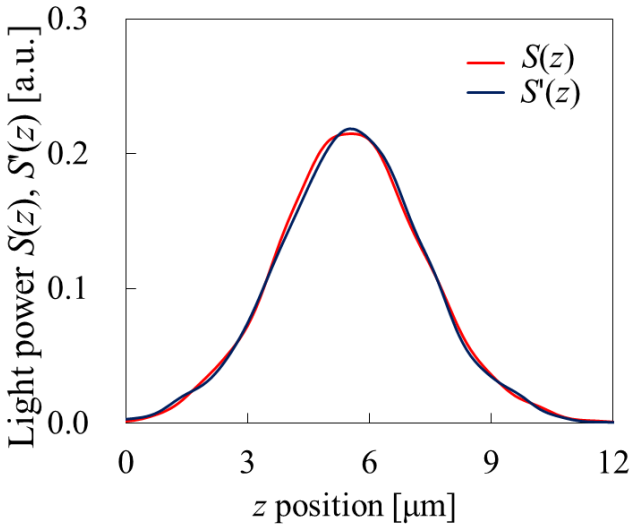


Figure 3. 34 Designed *S*(*z*) and *S*'(*z*).

$$2\alpha(z) = \frac{S(z)}{1 - \int_0^z S(t)dt} \quad \text{.....(3.5)}$$

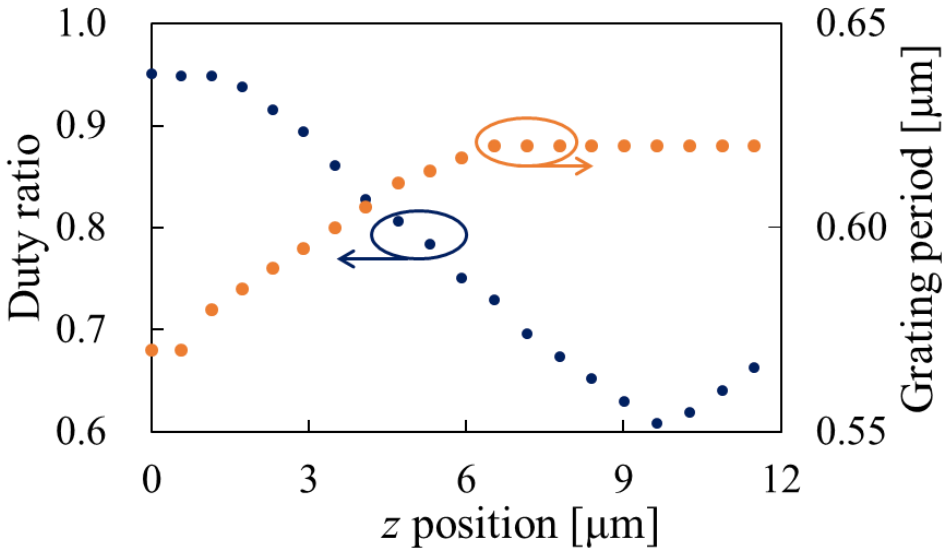
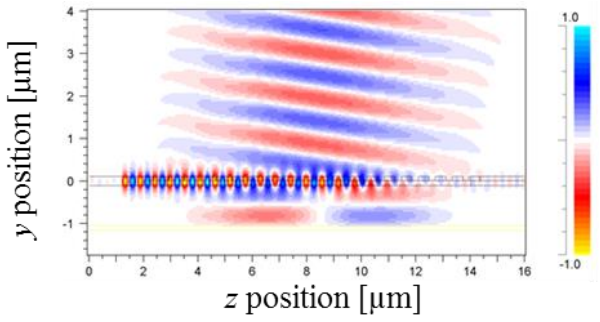


Figure 3. 35 Grating period and duty ratio of designed grating.

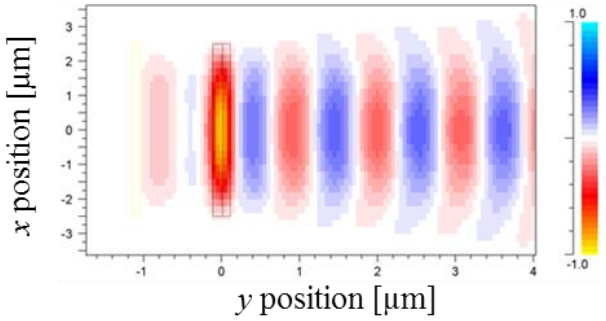
In fact, 2α calculated in the condition of uniform gratings was different with that of calculated in the apodized grating. Therefore, the obtained $S(z)$ will be slightly different when 2α, which was calculated in the condition of uniform gratings, was used for the grating period. Figure 3. 33 shows the designed $S(z)$, 2α, and 2α (theoretical) calculated from the designed $S(z)$. As mentioned earlier, the designed 2α was different from the theoretical 2α and required slightly higher values. Figure 3. 34 shows designed $S(z)$ and $S'(z)$. As the diffraction profile was symmetric, both profiles matched well each other.

The grating period and duty ratio of the designed grating are shown in Figure 3. 35. The duty ratio was gradually increased to satisfy the profile of the leakage factor, $2\alpha(z)$, as calculated in Figure 3. 33. The grating period was also gradually increased in order to maintain the diffraction angle. If the grating period is constant, the optical length of the grating period will be shortened since the length of the etched waveguide, which has low equivalent refractive index, is lengthened. The smallest length of groove was about 30 nm and the largest length of groove was about 240 nm.

Finally, the electric filed distribution of the radiated light in y-z and x-y planes are shown



(a)



(b)

Figure 3. 36 Electric field distribution of y-z and x-y plane.

in Figure 3. 36. The diffraction angle was estimated to be 11° from the image.

3.5.2 Coupling efficiency

In this section, the coupling efficiency of the inter-layer apodized grating coupler will be discussed. The main reason for introducing apodized grating was inter-layer distance independent operation of inter-layer grating couplers. As the diffraction angle of the designed gratings was 11°, the inter-layer distance needed to be shifted (*z* position offset) according to the inter-layer distance. Figure 3. 37 shows *z* position offset dependence of the coupling efficiency with various inter-layer distance ranging from 1 to 3 μm. Approximately 0.2 μm of offset was needed for the additional 1 μm inter-layer distance.

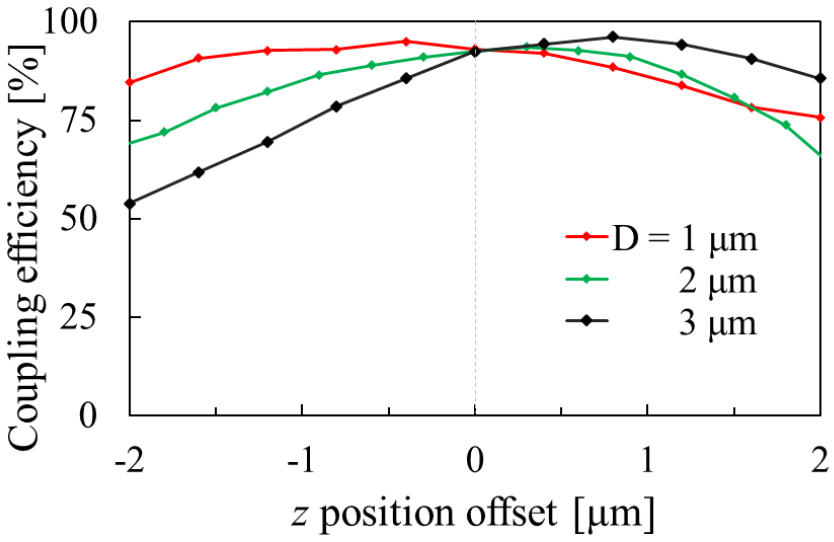


Figure 3. 37 Coupling efficiency and offset for various inter-layer distance *D*.

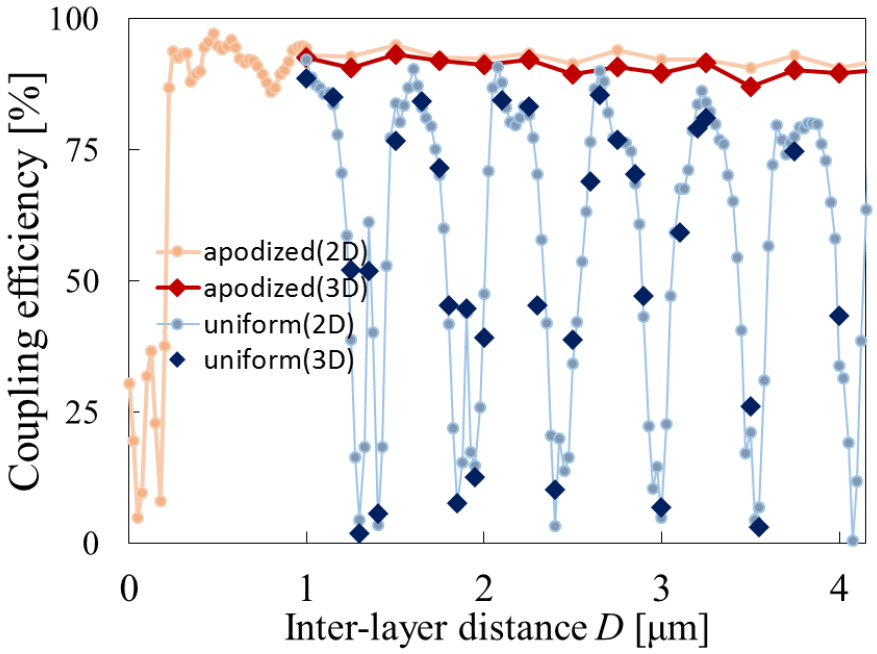


Figure 3. 38 Coupling efficiency of apodized and uniform inter-layer grating

Figure 3. 38 shows the coupling efficiency of the apodized and uniform (designed at chapter 3.4) inter-layer grating couplers as a function of the inter-layer distance. For the apodized inter-layer grating couplers, 0.2 μm offset was introduced for every 1 μm inter-layer distance. The inter-layer distance independent characteristics was confirmed owing

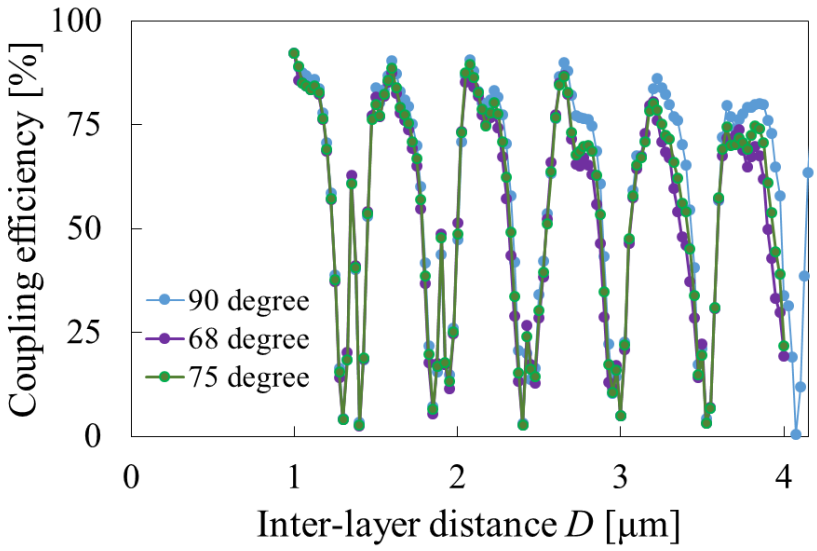


Figure 3. 39 Coupling efficiency of apodized and uniform inter-layer grating couplers as a function of inter-layer distance.

to the apodization of the gratings. In the case of apodized grating (2D-simulation) with the inter-layer distance ranging from 0~1 μm is also shown in Figure 3. 38. When the inter-layer distance was less than 0.2 μm, overlapping of the evanescent light caused light transferring between the upper and under layer waveguides as a directional coupler. There was no offset for the uniform inter-layer grating couplers in the result of Figure 3. 38. Therefore, we also investigated the coupling efficiency of the uniform inter-layer grating couplers with offset assuming the radiation angles as 68, 75, 90 degree (Figure 3. 39). The result was that there was no significant changes with offset in the coupling efficiency in the case of uniform gratings. Figure 3. 40 shows the electric field distribution of apodized grating couplers at the inter-layer distance of 2 μm. Light input was from the lower left and output was at the upper right. Interference between the light from the 1st layer grating coupler and from the 2nd layer grating coupler was mostly suppressed.

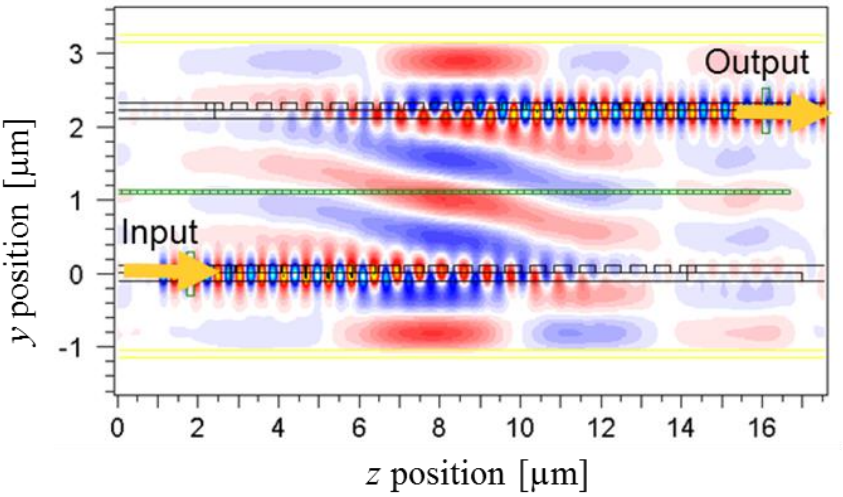


Figure 3. 40 Electric field distribution of apodized inter-layer grating couplers at inter-layer distance of 2 μm.

3.5.3 Misalignment tolerance

In this section, misalignment tolerance for the propagation direction, orthogonal direction, and D_M, D'_M will be reviewed. Figure 3. 41 shows the coupling efficiency difference caused by misalignment for the propagation direction and the orthogonal (width) direction. The deterioration of the coupling efficiency was less than 0.4dB for both the propagation and the orthogonal direction. It seems the tolerance of misalignment on the propagation direction is depend on the total length of the grating (<12 μm), which

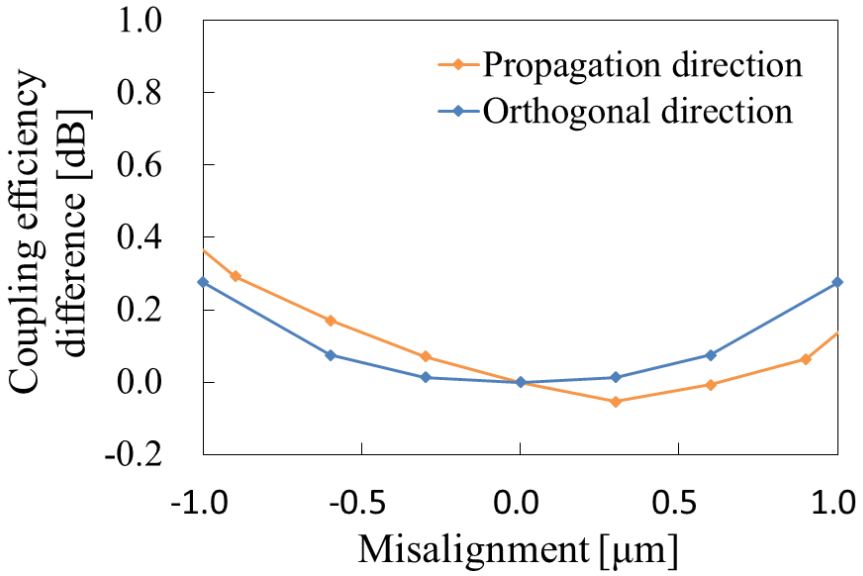


Figure 3. 41 Coupling efficiency difference caused by misalignment for propagation direction and orthogonal direction.

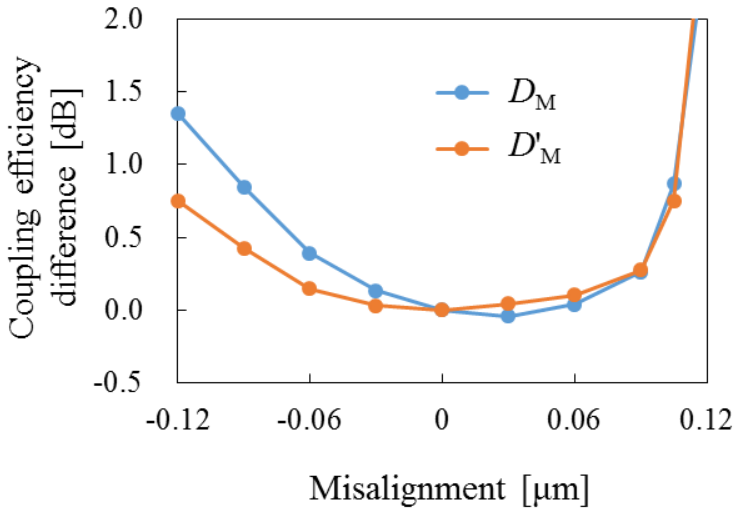


Figure 3. 42 Coupling efficiency difference caused by misalignment of D_M and D'_M.

was slightly decreased value (<13.5 μm) compared to the uniform grating designed in chapter 3.4.

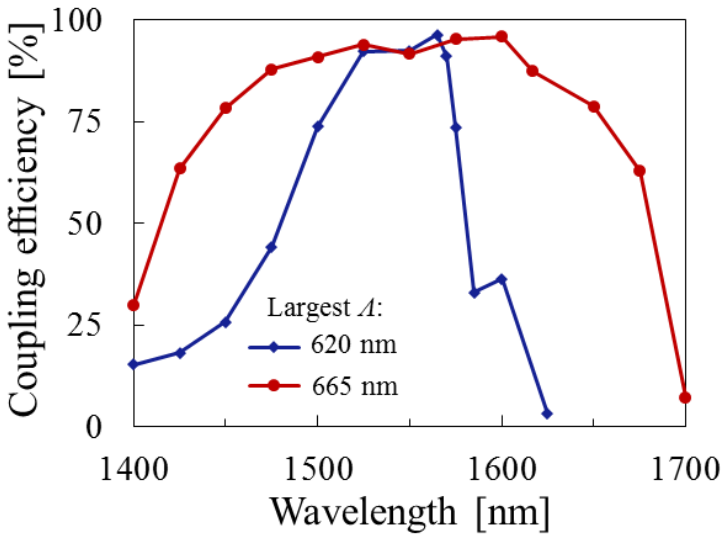


Figure 3. 43 Wavelength dependence of the apodized inter-layer grating couplers.

The coupling efficiency difference depend on the misalignment of D_M and D'_M are shown in Figure 3. 42. High accuracy of controlling D_M and D'_M was required, for example, the coupling efficiency was degraded 0.5dB only for 100 nm of misalignment. In practice, D_M and D'_M are depend on the CMP process for inter-layer grating couplers. Details about the CMP process will be presented in chapter 4.

3.5.4 Wavelength dependence of coupling efficiency

The wavelength dependence of the apodized inter-layer grating couplers with metal mirrors is shown in Figure 3. 43. When the largest Λ was 620 nm, which was designed in chapter 3.5.1, the coupling efficiency exceeded 80% for the wavelength range from 1510 nm to 1570 nm. 60 nm of wavelength is fairly good enough though, further improvement of the wavelength bandwidth could be obtained by increasing Λ. The reason of the coupling efficiency drop was radiation efficiency and mode mismatching caused by the diffraction angle. At the longer wavelength (more than 1570 nm in the largest Λ of 620nm case), the back reflection started to increase and the ratio of the -1 order diffraction was decreased. At the shorter wavelength (less than 1510 nm in the largest Λ of 620nm case),

change of the diffraction angle resulted in the decrease of overlap between the $S(z)$ and $S'(z)$. These issues can be moderated by adopting a longer grating period which means the length of the mode profile will become longer. Therefore, in order to improve the coupling efficiency, the apodized inter-layer grating couplers were redesigned with longer Λ. The wavelength dependence of the coupling efficiency is also in Figure 3. 43. More than 80% of the coupling efficiency can be obtained within the wavelength range of 200 nm. Although the diffraction angle will also increase along with Λ, this approach can also be used for the fiber-to-waveguide grating couplers.

3.6 Conclusion

In this chapter, theoretical analysis and design of the inter-layer grating couplers were given. Grating couplers can achieve vertical coupling with a distance of more than a few-μm. At the beginning of this chapter, basic characteristics of grating coupler was investigated. The relationship between the grating period and the diffraction angle was theoretically studied. The power leakage factor was affected by the grating depth and duty ratio of grating.

Then, the inter-layer grating couplers were designed at the inter-layer distance of 1 μm. Since it was first trial of designing multi-layered structure, fully etched gratings were introduced for the simple structure. The coupling efficiency of 19% was achieved at the grating period of 640 nm with 10 gratings.

Next, in order to increase the coupling efficiency, metal mirrors were introduced to the inter-layer grating couplers. The phase matching condition of the distance of the metal mirror to the grating was investigated and it was designed to be 800 nm. The depth of the gratings were changed to 70 nm and 10 gratings with the grating period of 640 nm was used for the inter-layer grating couplers. As a result, more than 80% of the coupling efficiency was obtained at the wavelength range from 1520 to 1600 nm (1dB bandwidth of 80 nm). In addition to this, the coupling efficiency difference of misalignment were less than 0.5dB for both the propagation direction and the orthogonal direction.

Finally, apodization of gratings was introduced to the inter-layer grating couplers for the inter-layer distance independent operation. The output mode-profile of the grating couplers were tuned to be symmetric shape in propagation direction. The distance from the metal mirror to the 1st and the 2nd layer were optimized to achieve high radiation efficiency and were designed as 940 nm and 820 nm, respectively. The coupling efficiency of more than 90% was maintained within the inter-layer distance of 4 μm. The wavelength dependence of the inter-layer apodized grating couplers showed fairly good characteristics. At the wavelength range from 1510 nm to 1570 nm, the coupling efficiency exceeded 80%. For further improvement of the wavelength dependence of

coupling efficiency, longer grating period was adopted to gratings and the 1dB bandwidth was broadened to 200 nm.

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Chapter 4
Fabrication and measurement of inter-layer grating couplers

4.1 Introduction

In this chapter, the experimental results of the inter-layer grating couplers will be presented. The structure of the inter-layer grating couplers consist of vertically stacked layers such as a-Si:H, SiO_2, and metals. Therefore, alignment of patterns between each layers is important for maintaining the device performance. In addition to this, the thickness control of each layer is also critical to the device performance and moreover, the thickness control is not possible anymore after stacking another layer on it. Further,

as the waveguide patterns are formed directly above the waveguide patterns on the under layer, CMP process is necessary in order to planarize the surface. Brief explanation and the SEM and optical microscope images of fabricated devices will also be presented. The inter-layer grating couplers were fabricated based on the device design described in chapter 3.

In the last half of this chapter, the measurement results including the coupling efficiency and signal transmission through the inter-layer grating couplers will be given.

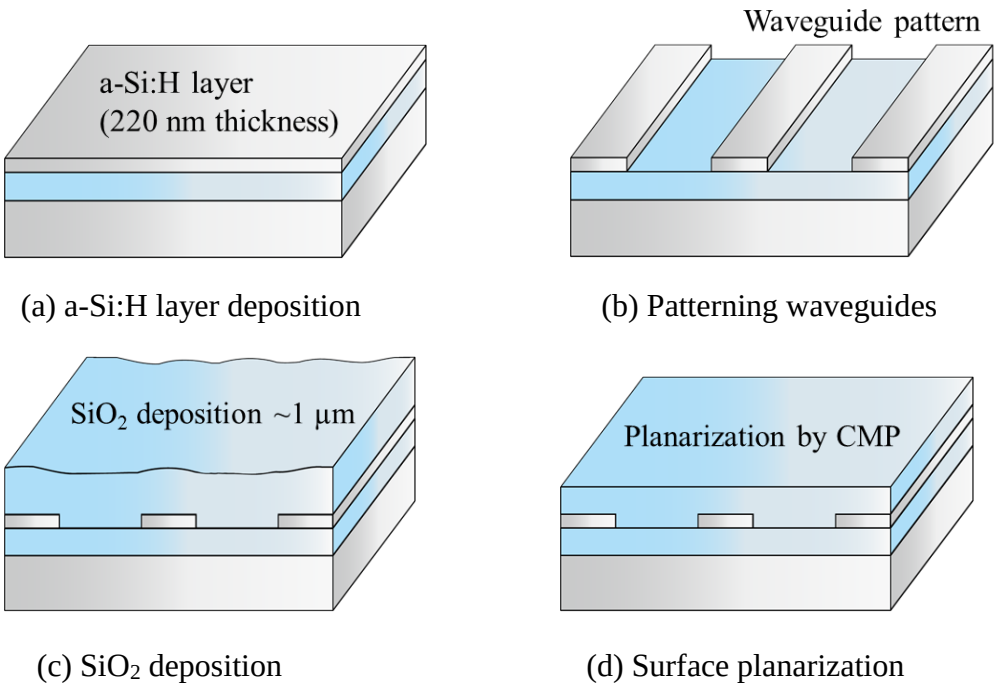


Figure 4. 1 Surface planarization by CMP process.

Figure 4. 2 CMP system (MAT Inc.)

4.2 Fabrication process

4.2.1 Surface planarization by CMP process

CMP process was added to the fabrication process of the surface roughness measurement of multi-stacked a-Si:H layers in chapter 2. The waveguide patterns

Table 4. 1 CMP process recipe.

	Flow rate (ml/min)	Platen speed (rpm)	Head speed (rpm)	Polishing rate (nm/min)
Slurry 1	100	40	25	50~60 nm/min
Slurry 2	100	40	25	~10 nm

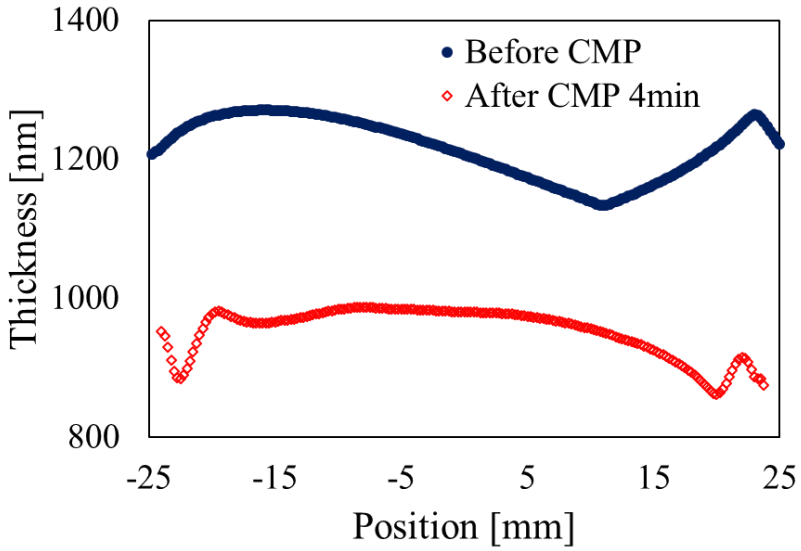


Figure 4. 3 SiO_2 thickness before and after CMP process.

including gratings or metal mirrors, were buried by SiO_2 as a cladding layer and upper layer were stacked on them. Before the deposition of a-Si:H layer, the surface was planarized by CMP process as shown in Figure 4. 1. Without CMP process, the uneven surface will cause significant optical loss. CMP system used in this experiment is shown in Figure 4. 2.

In order to check the thickness distribution of SiO_2 after CMP process, about 1 μm of SiO_2 was deposited on the 2-inch Si wafer and planarized by CMP process. Before and after the CMP process, the thickness of the SiO_2 was measured by ellipsometry. The condition for the CMP process is shown in the Table 4. 1. CMP process was done by 2

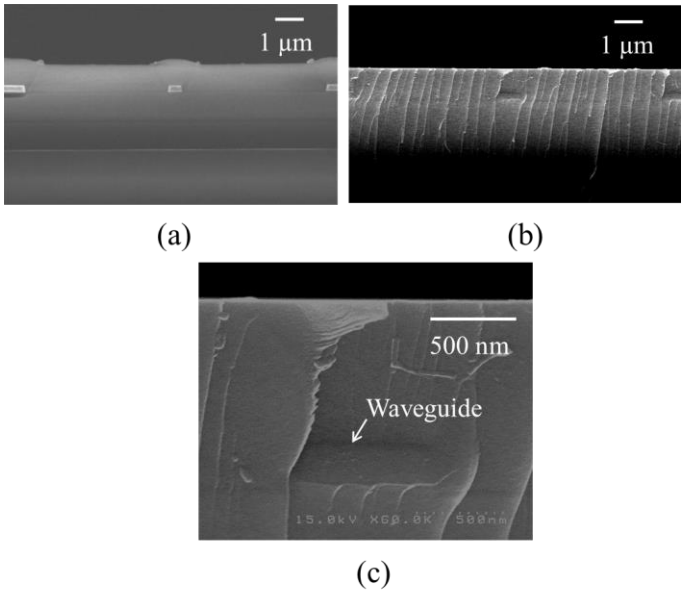
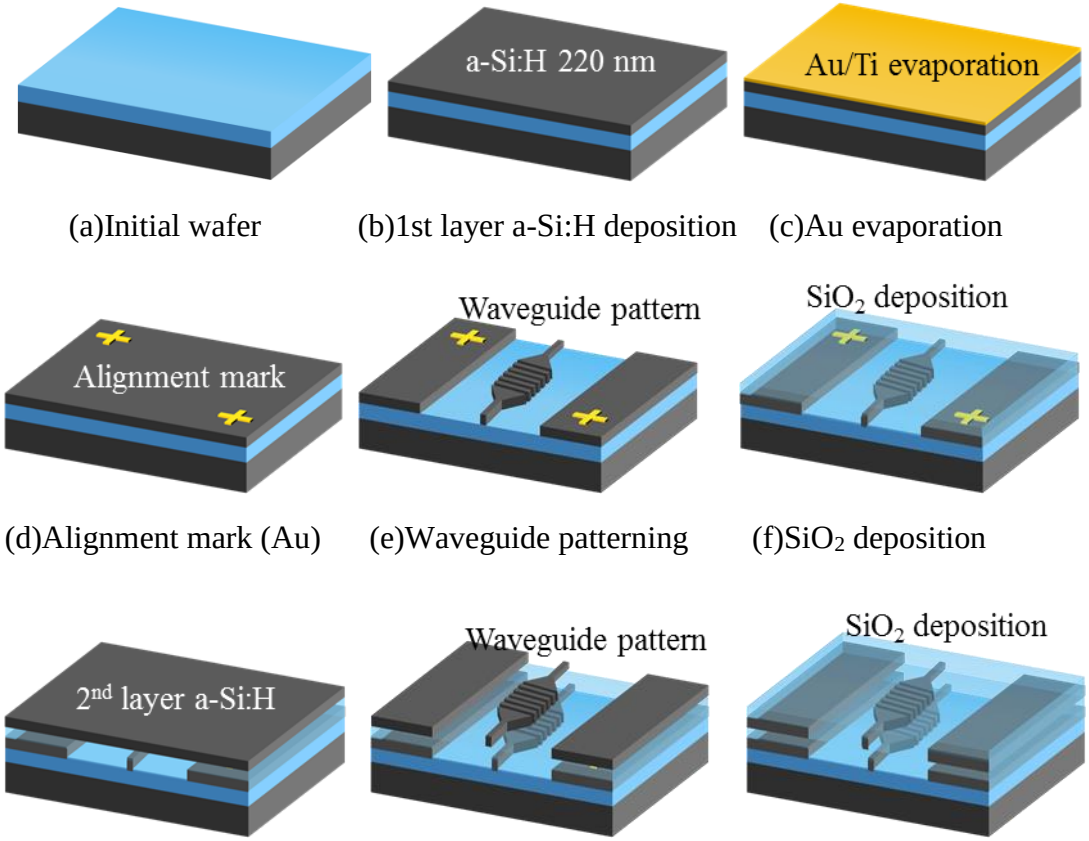


Figure 4. 4 Cross-sectional SEM image of a waveguide pattern embedded by SiO_2. (a) before CMP process (b) after CMP process (c) enlarged image of after CMP process

steps; 1st step for planarization with high polishing rate (Slurry 1: Semi-sperse 25, Cabot Microelectronics) and 2nd step for roughness reduction with low polishing rate (Mixed liquid of CMS8401 and CMS8452 with H_2O and H_2O_2, JSR Corp.). In another experiment, the surface roughness after the 1st step was measured as 0.48~0.57 and the surface roughness after the 2nd step was measured as 0.31~0.39. The thickness of SiO_2 before and after the 1st step CMP process for 4 minute are shown in Figure 4. 3. The thickness difference of within ±10 mm area of the 2 inch wafer was less than 30 nm. This result will further improved when larger wafers are used, such as 12-inch wafers which are commonly used for the micro-processor fabrication process at present. Besides, the thickness distribution will be much smaller since the fabricated inter-layer grating coupler will be formed within 5×5 mm^2 area.

Figure 4. 4 shows the cross-sectional SEM image of a waveguide pattern embedded by SiO_2. Fig. 4.4 (a), (b), and (c) are before the CMP process, after the CMP process, and



(a)Initial wafer (b)1st layer a-Si:H deposition (c)Au evaporation

(d)Alignment mark (Au) (e)Waveguide patterning (f)SiO_2 deposition

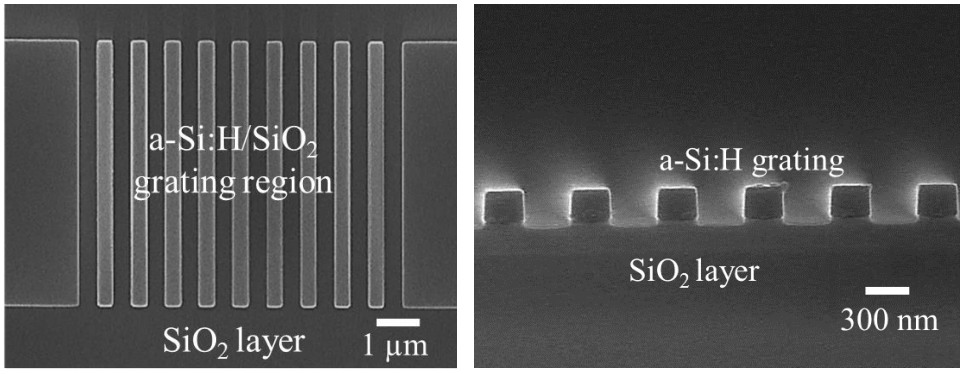
(g)2nd layer a-Si:H deposition (h)Waveguide patterning (i)SiO_2 deposition

Figure 4. 5 Fabrication process of inter-layer grating couplers without metal.

enlarged cross-sectional image of waveguide after the CMP process. The surface over the waveguide was uneven before the CMP process and flat surface was achieved after CMP process.

4.2.2 Inter-layer grating couplers without metal mirrors

The fabrication process of the inter-layer grating couplers are shown in Figure 4. 5. The initial wafer was 2-inch Si wafer covered with 3-μm-thick thermal SiO_2. Films of 100-nm-thick SiO_2 and 220-nm-thick a-Si:H were deposited by PECVD at the temperature of 300℃. 100 nm of SiO_2 was deposited as an intermediate layer since a-



(a) (b)

Figure 4. 6 Top and cross-sectional SEM images of a-Si:H grating for inter-layer grating couplers without metal mirror.

Si:H layer on the thermal SiO_2 was unstable. Without the intermediate layer, the a-Si:H layer was pilled off by the strong compressive stress [1, 2]. A few seconds of BHF wet treatment or RIE etching were also effective for the relaxation of the stress. Then, Ti and Au were evaporated and alignment marks for EB lithography were formed by lift-off process on the surface of the 1st a-Si:H layer. The waveguides and grating patterns were formed by using EB lithography with a double-layered ZEP resist and ICP-RIE. The top and cross-sectional SEM images of the grating are shown in Figure 4. 6 (a) and (b), respectively. The number of grating was 10 and the grating period was 640 nm as designed in chapter 3.3.1. After patterning the waveguides and grating, SiO_2 was deposited and flattened by a CMP process. The SiO_2 thickness was controlled to 1 μm as an inter-layer distance by additional deposition of SiO_2. Then, 200-nm-thick a-Si:H layer was deposited as the 2nd layer and patterned in a similar manner of the 1st layer. After covering the 2nd a-Si:H layer with SiO_2, the surface was flattened again by CMP process.

An optical microscope image of the fabricated device is shown in Figure 4. 7(a). The 1st layer wire waveguide and the 2nd layer wire waveguides were overlapped at the left center of the figure, and then the width of both waveguides were widened to 5 μm through 200-μm-long linearly tapered structure. Light coupling by the gratings occurred at the

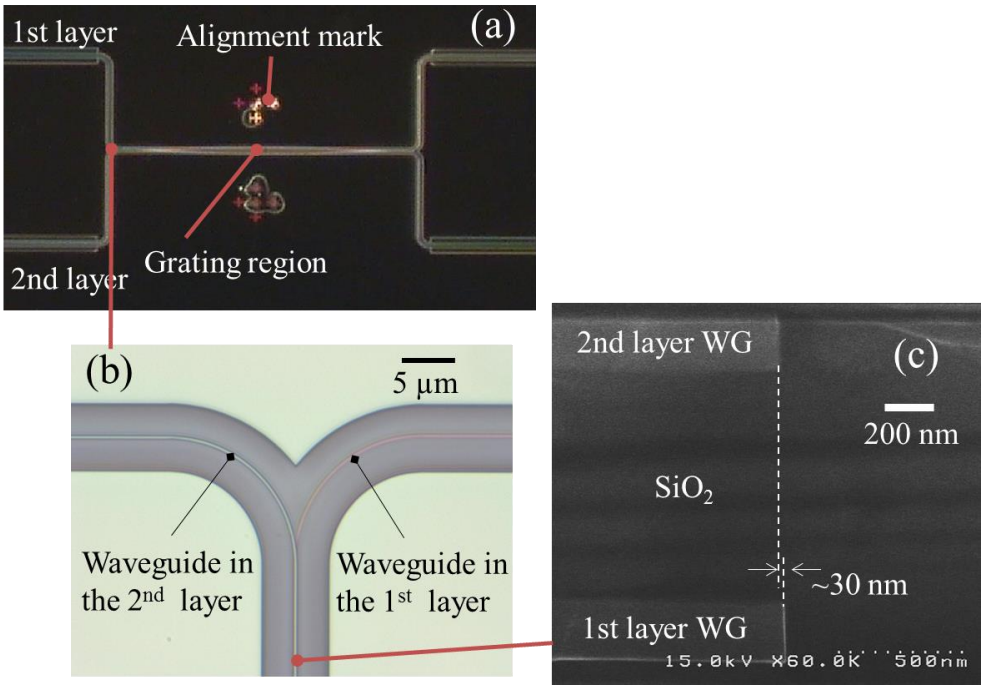
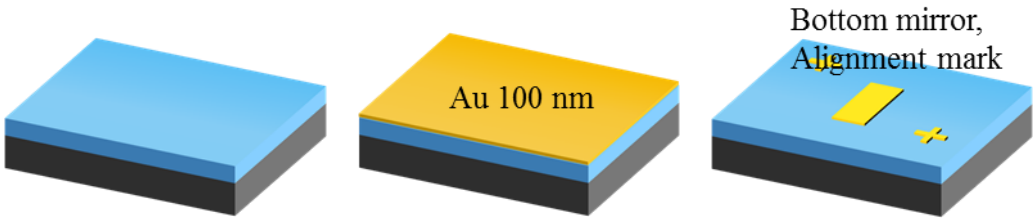
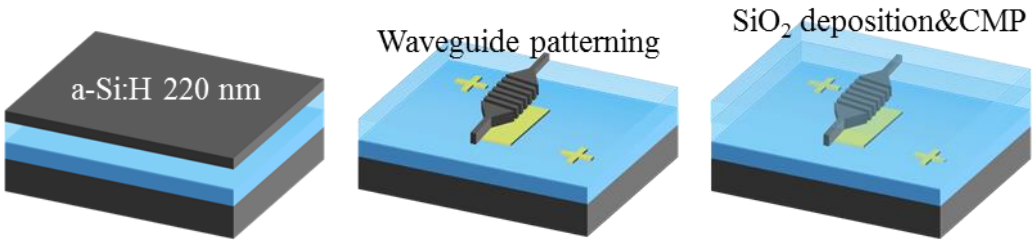


Figure 4. 7 Optical microscope and SEM images of fabricated inter-layer grating couplers without metal mirrors.

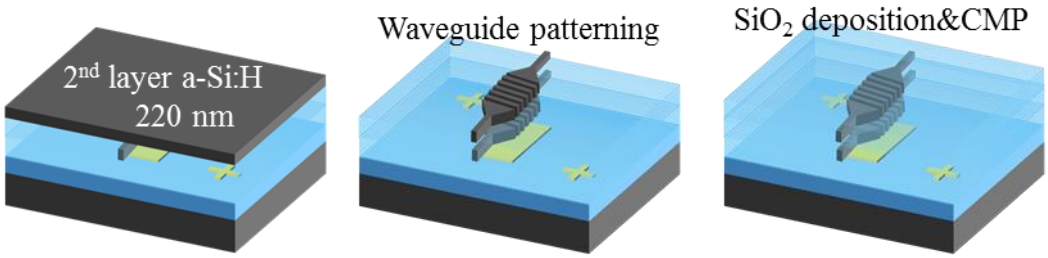
center of the figure. The cross marks in the figure were used as alignment marks during the EB lithography process. The enlarged top view at the point of overlapped a-Si:H wire waveguides is shown in Figure 4. 7 (b). The 1st layer wire waveguide was from the right side of the figure and the 2nd layer wire waveguide was from the left side of the figure. Both the wire waveguides were overlapped with a very high accuracy. Figure 4. 7 shows the cross-sectional SEM image of the overlapped waveguides. From the SEM image, the misalignment of the multi-layered waveguides was less than 30 nm. The coupling efficiency deterioration caused by the 30 nm of misalignment will be less than 0.001dB which was obtained in chapter 3.3.2.



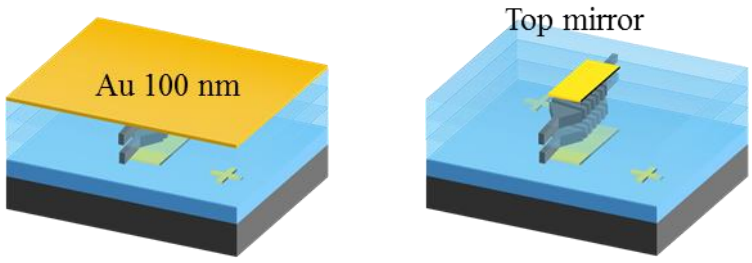
(a) Initial wafer (b) Au evaporation (c) Bottom mirror, Alignment mark



(d) a-Si:H layer deposition (e) Waveguide patterning (f) SiO2 deposition&CMP



(g) 2nd a-Si:H layer (h) Waveguide patterning (i) SiO_2 deposition&CMP



(j) Au evaporation (k) Top mirror formation

Figure 4. 8 Fabrication process of inter-layer grating couplers with metal mirrors.

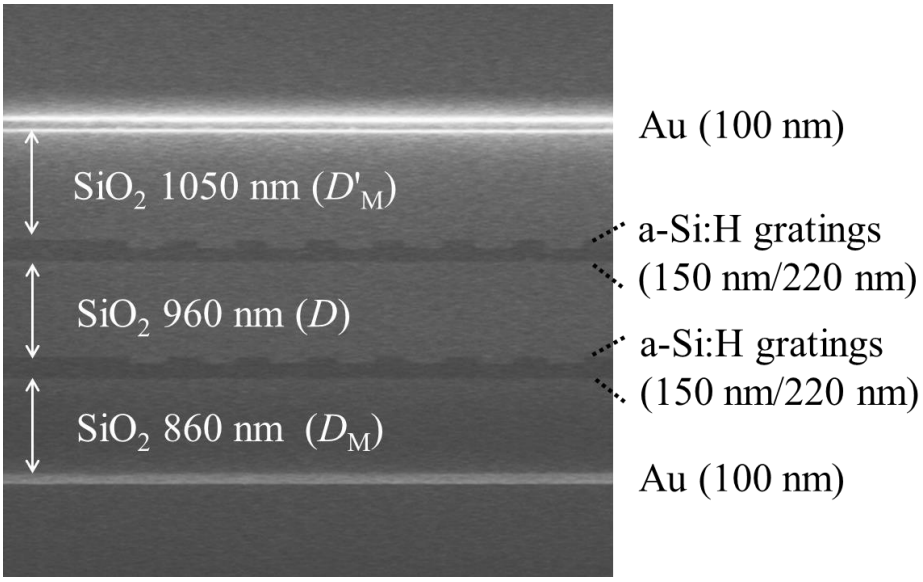


Figure 4. 9 Cross-sectional SEM image of the fabricated inter-layer grating couplers with metal mirrors. Sample #1.

4.2.3 Inter-layer grating couplers with metal mirrors

In this section, the fabrication process of the inter-layer grating couplers with metal mirrors will be presented. The main difference in structure between the w/ and w/o metal mirrors were metal mirrors at the upper and under the grating couplers and the depth of the grating. The fabrication process of the inter-layer grating couplers with metal mirrors is illustrated in Figure 4. 8.

A 2-inch Si substrate covered with 3-μm-thick layer of thermal oxide (SiO_2) was prepared as the initial wafer. The first step was evaporation of a 100-nm-thick Au film on the thermal SiO_2 and lift-off. Alignment marks for EB lithography and the bottom mirrors were formed by Au. The Au patterns were buried by deposition of SiO_2 at the process temperature of 300℃. Then the surface of the SiO_2 was flattened by a chemical mechanical polishing (CMP) process. The thickness of the SiO_2 was controlled to be equal the target value of 800 nm by the second deposition of SiO_2. As the core of the 1st layer, a 220-nm-thick layer of a-Si:H was deposited by PECVD. Patterning was carried out by employing two steps of EB lithography for waveguides and gratings, and an ICP-

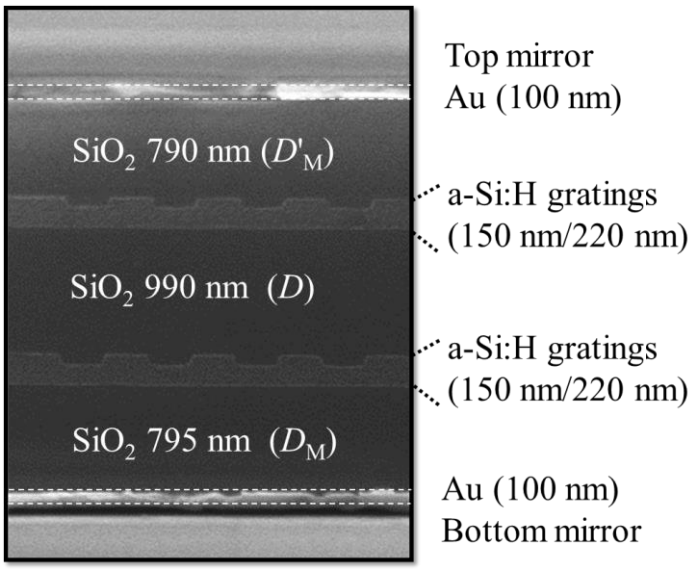


Figure 4. 10 Cross-sectional SEM image of the fabricated inter-layer grating couplers with metal mirrors. Sample #2.

RIE system. The waveguide patterns were buried by SiO_2 deposition, and the CMP process was again carried out, followed by SiO_2 deposition to the thickness of 1 μm (corresponds to the inter-layer distance). For the 2nd layer, a 220-nm-thick a-Si:H film was deposited and patterned, as was done for the 1st layer. Next, SiO_2 deposition and the third CMP treatment were performed to the thickness of 800 nm. The final step is to form the upper mirrors in the same way that the bottom mirrors were formed. At the first trial of this fabrication process, differences of SiO_2 thickness from the designed structure were found to be a problem. The cross-sectional SEM image of the fabricated device (Sample #1) is shown in Figure 4. 9. Multi-stacked structure of a-Si:H waveguides with gratings and metal mirrors were confirmed though, the thickness of D_M, D'_M, and D were different from the target values of 800 nm, 800 nm, and 1000 nm, respectively. Deterioration of the coupling efficiency can be expected by these differences.

In order to minimize the thickness differences between the fabricated thickness and the target values, the inter-layer grating couplers with metal mirrors were fabricated again (Sample #2) with monitoring all the thickness by a reflective film thickness monitor (FE-300, Otsuka Electronics. Co. Ltd.). Figure 4. 10 shows the cross-sectional SEM image of

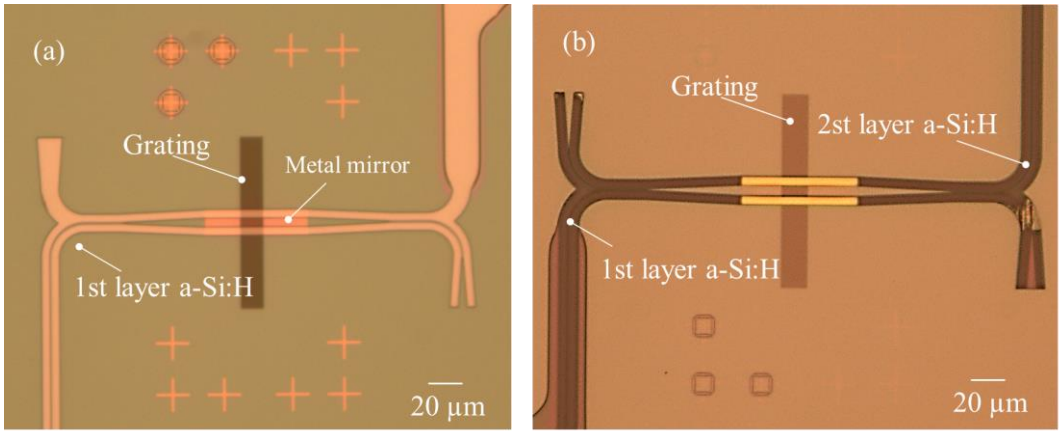


Figure 4. 11 Optical microscope images of the inter-layer grating couplers with metal mirrors. Sample #2. (Left: After 1st layer waveguide patterning, right: after TOP metal mirror formation)

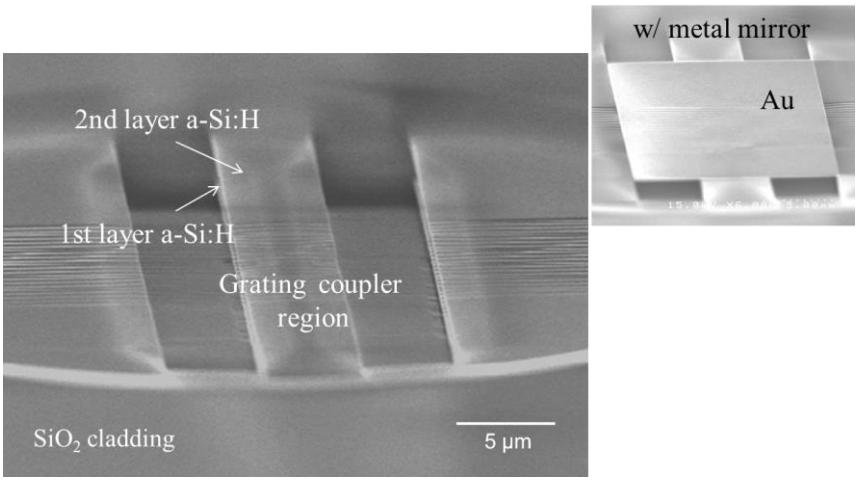


Figure 4. 12 Top SEM image of the inter-layer grating couplers with metal mirrors.

the fabricated inter-layer grating couplers (Sample #2). From the SEM image, the DM values for the 1st and the 2nd layers were measured to be 795 nm and 790 nm, respectively. The deviation of the thickness was ~10 nm (target thickness: 800 nm) including the inter-layer distance of 990 nm, which was only 10 nm thinner than the target value.

Figure 4. 11 shows the optical microscope images of the inter-layer grating couplers with metal mirrors of sample #2. Figure 4. 11 (a) was after the 1st layer waveguide formation and Figure 4. 11 (b) was after the top mirror formation. In order to reduce the exposure time, only the output ports of the grating couplers were formed and the light passed through the gratings were thrown out. Finally, the top SEM image at the grating region is shown in Figure 4. 12. As the grating couplers were buried by SiO_2, BHF wet etching were applied to remove the SiO_2. Upper right SEM image is before the removal of the top metal mirror, and center image is after the removal. The gratings were in the center of the image.

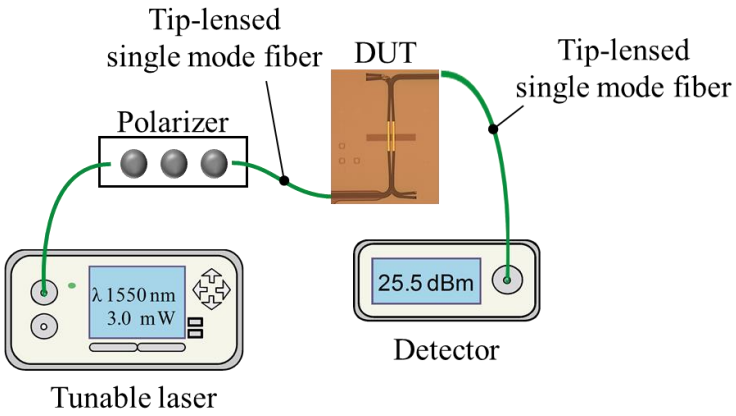


Figure 4. 13 Measurement setup for the coupling efficiency measurement.

4.3 Coupling efficiency measurement

4.3.1 Measurement system

The measurement system for the coupling efficiency measurement is shown in Figure 4. 13. A tunable laser diode was used as a light source and the light was then fixed as TE-polarized wave. The light input to the waveguides was from the tip-lensed single-mode-fiber through the back inverse tapered type SSCs which were also mentioned in chapter 2.4.3. The output from the inter-layer grating couplers were then coupled to the fiber and detected by a wide-band power detector.

4.3.2 Inter-layer grating couplers without metal mirrors

The transmission spectra of the inter-layer grating couplers without metal mirrors is shown in Figure 4. 14. The power transmitted between the 1st and 2nd layers is plotted as open circles (red) and that which passes through the gratings of the 2nd layer is plotted as open diamonds (blue). The losses, including the propagation loss and coupling loss from the single-mode-fibers to the waveguides, was approximately 6 dB. The maximum

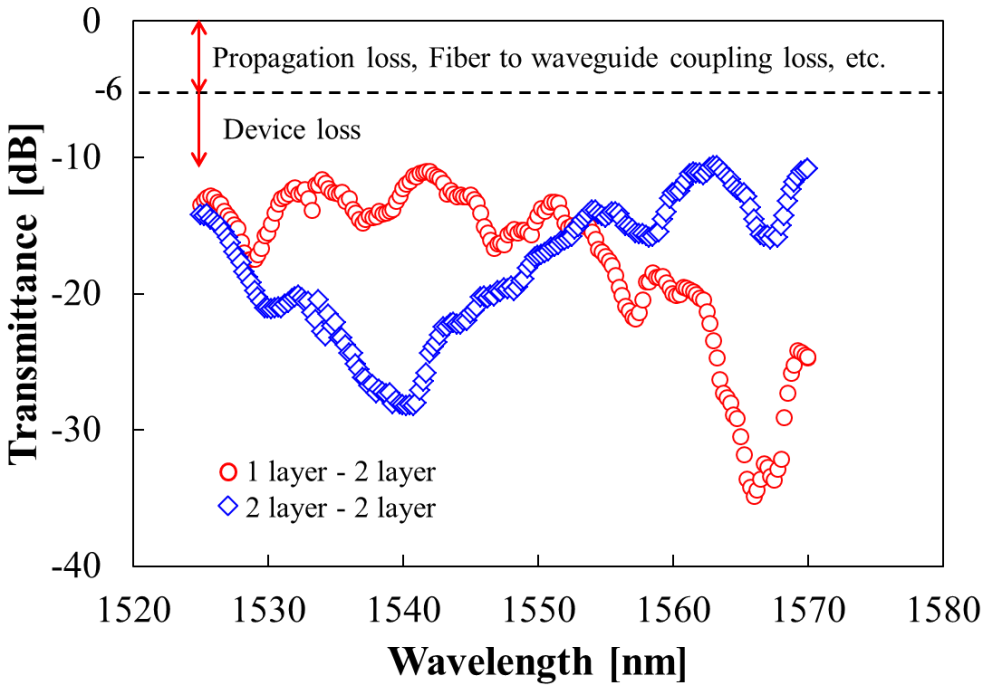


Figure 4. 14 Measured transmitted spectra of fabricated inter-layer grating couplers without metal mirrors.

coupling efficiency was estimated to be around 22% by subtracting 6dB from the measured data. This coupling efficiency is 3% higher than that obtained from the simulation results in chapter 2.4.2. This discrepancy can be attributed to the light reflected from the bottom boundary between the Si substrate and SiO_2 and from the top boundary between SiO_2 and air, which was not considered in the simulation. The transmitted spectra indicated resonance-like ripples with a period of approximately 9.5 nm, which corresponds to a resonant cavity length of around 40–50 μm. Given that the above resonance matches the distance between both ends of the tapered waveguides, the ripples can be reduced by introducing a more efficient tapered structure.

In the current symmetric structure with fully-etched gratings, the ratio of the light radiated upward to that radiated downward should be 1. This means that more than half of the light was wasted for each grating coupler. Therefore, 25 % is the maximum

coupling efficiency that can be achieved by the paired grating coupler.

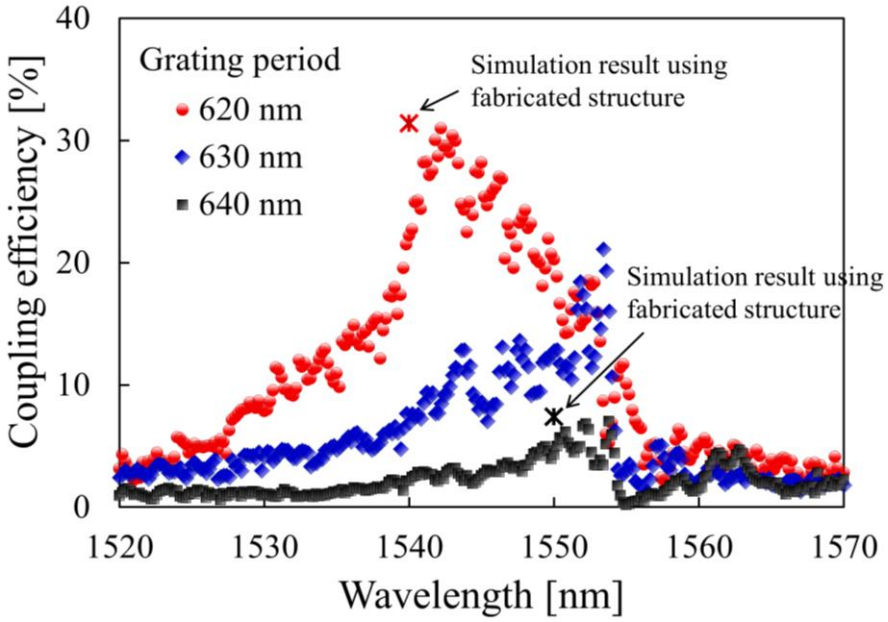


Figure 4. 15 Measured wavelength dependence of coupling efficiency for various grating periods. Sample #1.

4.3.2 Inter-layer grating couplers with metal mirrors

In this section, the coupling efficiency of the inter-layer grating couplers with metal mirrors will be presented. There were two samples (Sample #1 and sample #2) as explained in chapter 4.2. The measured coupling efficiency of the sample #1 with 3 kinds of grating periods is shown in Figure 4. 15. Red circles, blue diamonds, and black squares represent 620 nm, 630 nm, and 640 nm, respectively. The peak coupling efficiency was about 31% at the grating period of 620 nm. And the peak coupling efficiency of the higher grating periods showed the peak position at the higher wavelength. The reason of the lower coupling efficiency than the designed values were the thickness difference as mentioned at chapter 4.2.3. In the additional simulation under the condition of actual fabricated structure, the maximum coupling efficiency was degraded to 31.2% with a grating period of 620 nm at the wavelength of 1540 nm, and 7.9% with a grating period of 640 nm at the wavelength of 1550 nm. These results were well agreed with the

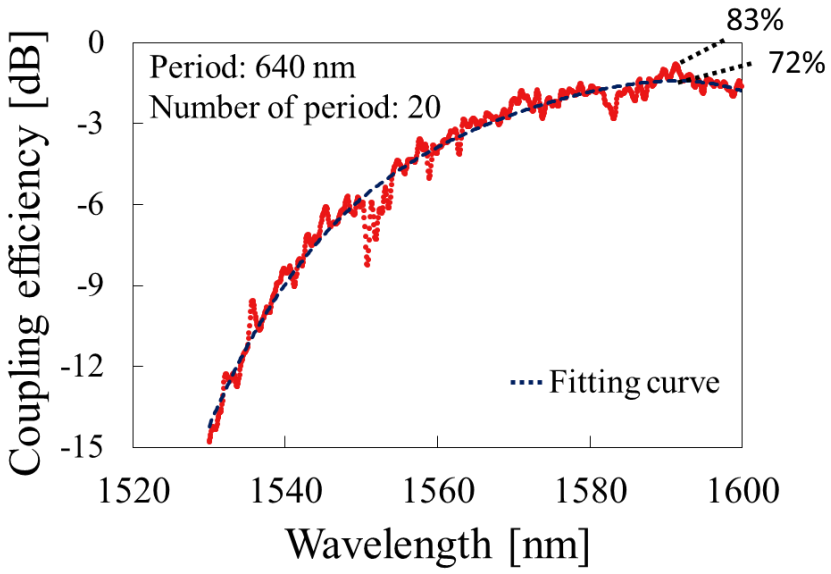


Figure 4. 16 Measured wavelength dependence of coupling efficiency for various grating periods. Sample #2.

measured results and thus, further improvement of the coupling can be realized with accurate control of SiO_2 thickness.

Next, the coupling efficiency of the sample #2 is shown in Figure 4. 16. In this measurement, amplified spontaneous emission light source, polarize splitter, and spectrum analyzer were used instead of the tunable laser, polarizer, and photodetector. The mean value of measured transmittances within the 1st to the 1st layer and 2nd to the 2nd layer which was fabricated without grating couplers separately but on the same chip. Then, the transmittance between the input to the 1st layer and the output from the 2nd layer with the grating couplers were also measured. The coupling efficiency was calculated by subtracting the mean value from the measured transmittance of the inter-layer grating couplers.

The spectral property of the coupling efficiency of the inter-layer grating couplers with 20 gratings is shown in Fig. 10. The peak coupling efficiency of 83% was obtained at the wavelength of 1590 nm with N= 20, whereas N= 21 is the optimum value as

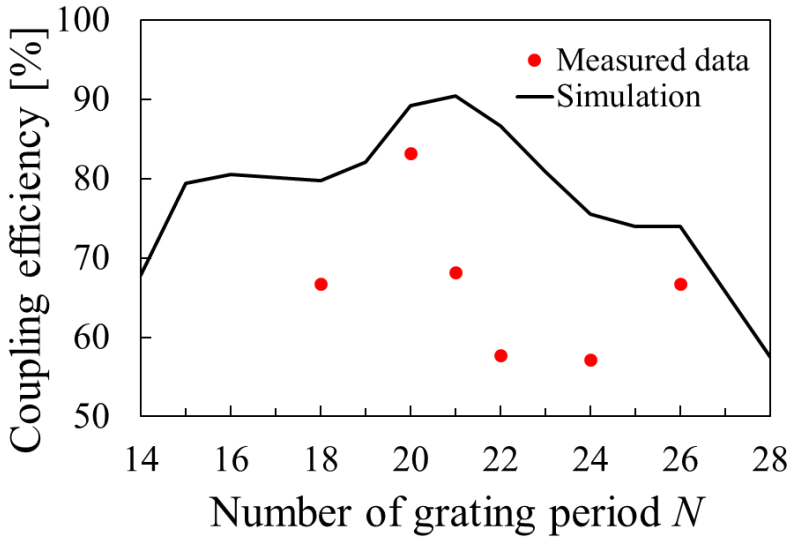


Figure 4. 17 Coupling efficiency as a function of number of grating period. Sample #2.

described in chapter 3.4.1. The 3-dB bandwidth was more than 40 nm, which was limited by the output wavelength range of the light source.

Figure 4. 17 shows the coupling efficiency as a function of number of grating period of the sample #2. The measured coupling efficiency were plotted as red circles and the black line is simulated result. Overall measured coupling efficiency were slightly below the simulation result though, the measured data showed more than 50% of coupling efficiency.Figure 4. 15

4.3.3 High-speed data transmission through inter-layer grating couplers

In this section, high-speed data transmission through the inter-layer grating couplers was demonstrated. The measurement setup is as shown in Figure 4. 18. The inter-layer grating couplers are basically passive devices so the signal degradation was hard to

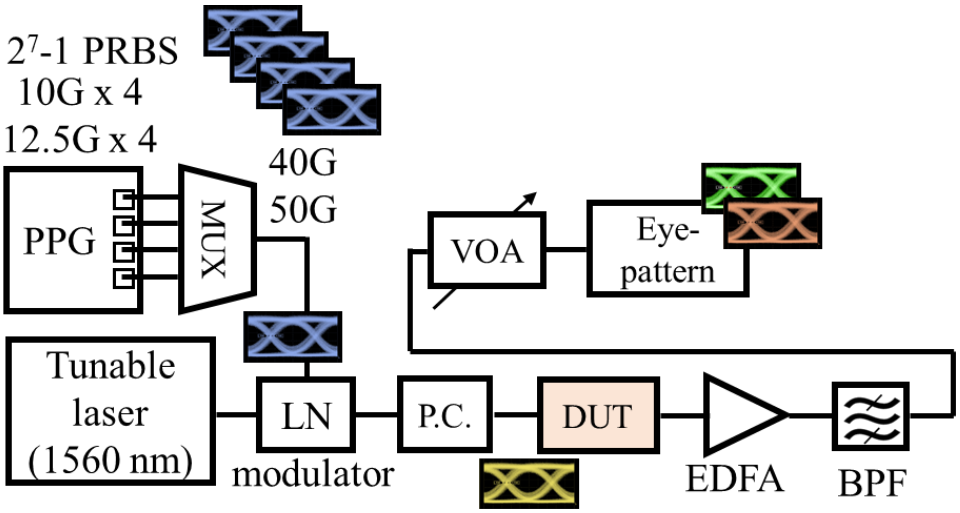


Figure 4. 18 Measurement setup for high-speed data transmission.

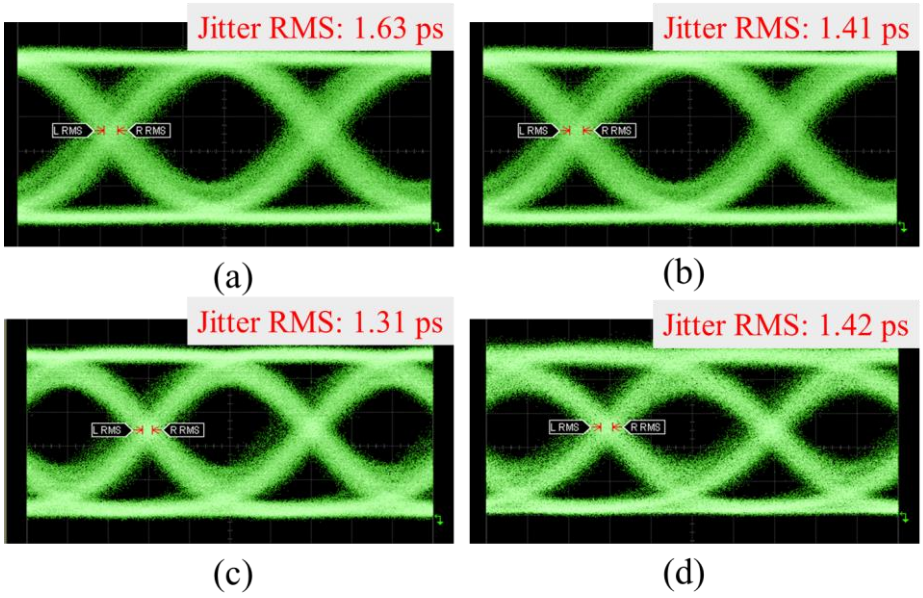


Figure 4. 19 Measured eye patterns for 40 Gbps: (a) F-to-F and (b) DUT.

Measured eye patterns for 50 Gbps: (c) F-to-F and (d) DUT.

imagine though, high-rate data signals could be affected by the reflection and interference at the metal mirrors. In order to investigate the performance of the inter-layer grating couplers, optical signals modulated with 2^{-7} pseudo-random binary sequence (PRBS)

patterns were used as input. The sample #2 was used for this experiment. The measured wavelength was set at 1560 nm due to the operating limits of our Erbium-doped fiber amplifier. The eye diagrams with the device under test (DUT) and without the DUT, which means just fiber-to-fiber (F-to-F) as a reference, at data rates of 40 Gbps and 50 Gbps are shown in Figure 4. 19. Clear eye openings were observed with our device compared to those of the F-to-F, even with a data rate of 50 Gbps. The jitter RMS values of the F-to-F and DUT configurations were 1.63 ps (Figure 4. 19 (a)) and 1.41 ps (Figure 4. 19 (b)), respectively, for 40 Gbps and 1.31 ps (Figure 4. 19 (c)) and 1.42 ps (Figure 4. 19 (d)), respectively, for 50 Gbps. There was no noticeable difference of the jitter values for each data speed. These experiments proved that multiple reflections by the mirrors above and below the couplers did not cause any degradation of the signal transmission.

4.4 Conclusion

In this chapter, the fabrication process of the inter-layer grating couplers and the measurement result of the coupling efficiency and the high-speed data transmission were given.

CMP process was introduced to maintain the flatness and the roughness of the surface in multi-layered structure. The CMP process consisted of 2 steps. The surface roughness after the 1st step was 0.48~0.57 and it improved to be 0.31~0.39 after the 2nd step. The thickness difference at the area within ±10 mm was less than 30 nm.

Then, the fabrication processes of the inter-layer grating couplers with and without the metal mirrors were explained. From the images of the fabricated devices, the misalignment at the EB lithography was less than 30 nm.

The coupling efficiency was measured as about 22% without metal mirrors which was limited by the radiated light to the opposite direction. By introducing metal mirrors, high coupling efficiency of 90% was expected at a numerical simulation. There were two samples of the inter-layer grating couplers with metal mirrors of which the thickness difference were less than 250 nm or 10 nm. The coupling efficiency of the former sample was measured as 31% at the peak position and that of the latter was measured to be 83%.

Finally, high-speed data transmission was demonstrated in order to confirm the performance of the inter-layer grating couplers with metal mirrors. Clear eye openings were observed at the data rates up to 50Gbps.

Reference

[1] K. Ozawa, N. Takagi, and K. Asama, "Effect of deposition conditions on intrinsic stress in a-Si: H films," *Japanese journal of applied physics*, vol. 22, p. 767, 1983.

[2] J. Dutta, U. Kroll, P. Chabloz, A. Shah, A. Howling, J. L. Dorier, *et al.*, "Dependence of intrinsic stress in hydrogenated amorphous silicon on excitation frequency in a plasma‐enhanced chemical vapor deposition process," *Journal of applied physics*, vol. 72, pp. 3220-3222, 1992.

Chapter 5
Other application of grating couplers for 3D optical interconnect

5.1 Introduction

So far, multi-stacking of the a-Si:H layers and the inter-layer grating couplers for the vertical coupling have been discussed toward 3D optical interconnect. Other than those above, as the essential components for the 3D optical interconnect there are other devices such as optical sources, modulators, and detectors.

In this chapter, as the other application of the grating couplers, fiber-to-waveguide grating coupler and integration of VCSELs on the Si substrate will be presented. The

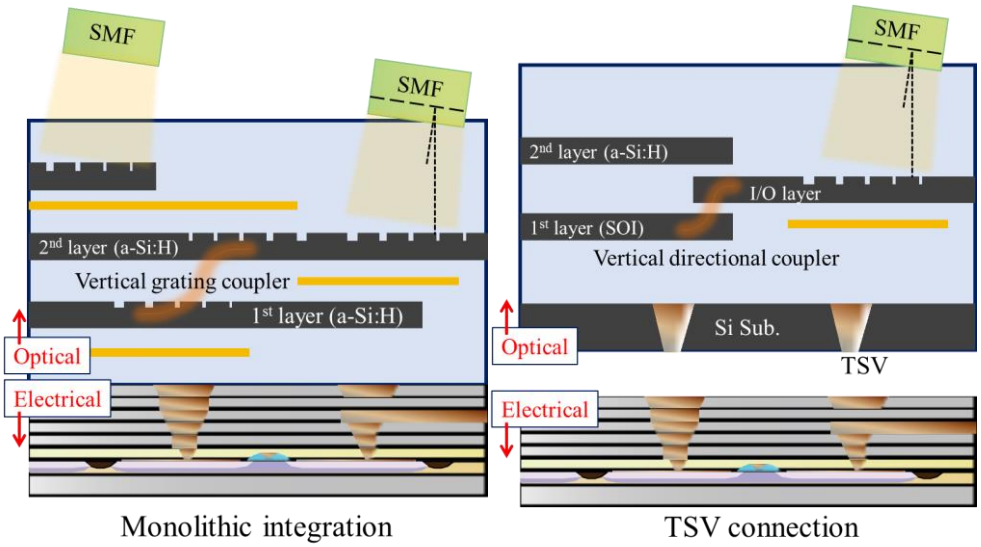


Figure 5. 1 Schematic illustration of 3D optical interconnect on LSI chip.

grating coupler for a single-mode-fiber (SMF) could be used as an I/O of the optical interconnect. The schematic illustrations of the 3D optical interconnect on LSI chip are shown in Figure 5. 1. Depending on the demands of the application, the optical interconnect can be integrated by monolithic approach on the LSI chip or TSV using the SOI substrate. The former is a cost effective way of integrating optical interconnect by back-end process. Low temperature grown germanium photodetectors or modulators and a-Si:H modulators using the thermo-optic effect can be an attractive candidate [1-3]. Integration of 3D optical interconnect on the SOI wafer could also be a powerful solution. Two wafers of electronic and optical circuits is needed though, the device performance of each wafer can be maximized by this approach.

Generally, grating couplers for the fiber connection show the coupling efficiency of up to 70% [4-6]. One of the limiting factor of the coupling efficiency is radiated light to the opposite direction as discussed at the inter-layer grating couplers. Metal mirrors are also effective way to improve the coupling efficiency, and the first half of this chapter will focused on the grating coupler for the fiber coupling.

The last half of this chapter is about the integration of VCSELs on Si substrate. If we consider devices are usually functioning on the 2D-plane, in-plane conversion of output

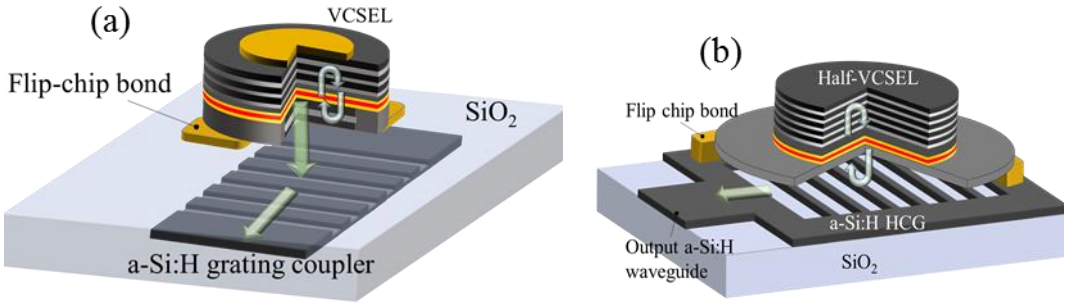
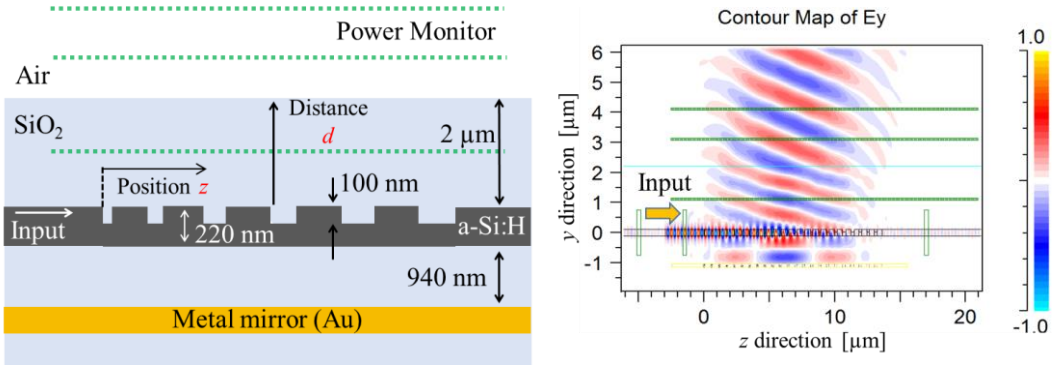


Figure 5. 2 Integration of VCSELs on Si substrate.

beam direction of the VCSEL is necessary since the output from the VCSEL is along the vertical direction.

Figure 5. 2 shows two ways of guiding output-light from VCSELs to the Si waveguides. Approach (a) is using grating coupler and a flip-chip bonded VCSEL. In order to suppress the reflection from the grating coupler, the VCSEL is need to be bonded with a tilt. The other approach is using high contrast grating (HCG) on the Si substrate. High reflectivity can be obtained by the HCG and rest of the light will coupled to the output Si waveguide [7-9]. At the last half of this chapter, the design of the HCG and output waveguide will be presented.



(a) (b)

Figure 5. 3 Simulation model for output mode profile calculation of grating coupler.

5.2 Single-mode-fiber to the waveguide grating coupler

The output distribution of grating coupler for the SMF is need to be optimized to the mode profile of the SMF. The SMF used here was SMF-28 (Corning), and the mode filed diameter was 10.4 μm at the wavelength of 1550 nm. Details of optimization procedure of grating coupler will be given in next section.

5.2.1 Design of apodized grating coupler

The target of the fiber grating coupler designed here was aiming I/O of the 3D optical interconnect. Thus, the waveguide thickness, the grating depth, D_M was fixed as 220 nm, 100 nm, and 940 nm, respectively, in order to coordinate with the dimensions used in the chapter 3.5. Then, the output mode profile of the grating coupler was simulated with various grating periods and the duty ratio of the gratings by 2D-FDTD. For more accurate simulation, measured refractive indices of the a-Si:H and the SiO_2 were used in this simulation. The simulation model for the output power mode profile $S(z)$ of the grating coupler and electric field distribution are shown in Figure 5. 3. d denotes the distance

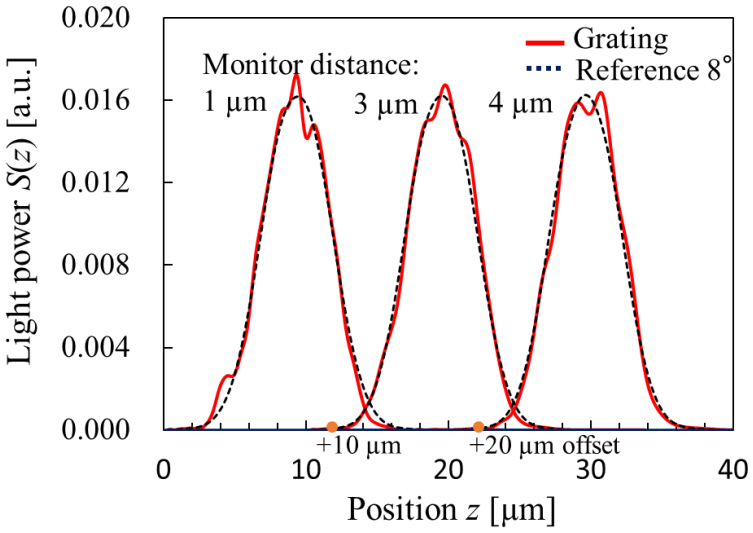


Figure 5. 4 Output light power distribution from the grating coupler and reference power distribution.

from the waveguide and *z* denotes the distance from the first grating. The input was from the bottom-left of the image (Figure 5. 3 (a)). Three different *S*(*z*) at *d* = 0, *d* = 3, and *d* = 4 were monitored in order to check the diffraction angle related changes in the output mode profile. Even if the *S*(*z*) was matched with the fiber mode profile at a certain *d*, the coupling efficiency would be low when the diffraction angle was not constant at any grating. Figure 5. 4 shows the output power distribution from the grating coupler and the mode profile of SMF as a reference at the tilt angle of 8°. The output power distribution showed good agreement at any *d* simulated here. In the case of the output power was weaker than the reference, the duty ratio needed to be decreased in order to increase the leakage factor of the grating. If the diffraction angle of the output power was smaller, which meant the output power distribution shifted to the left, the grating period needed to be increased.

Figure 5. 5 shows the duty ratio and the grating period as a function of the position *z*. The duty ratio of more than 0.9, which corresponded to 50 nm of groove length, was

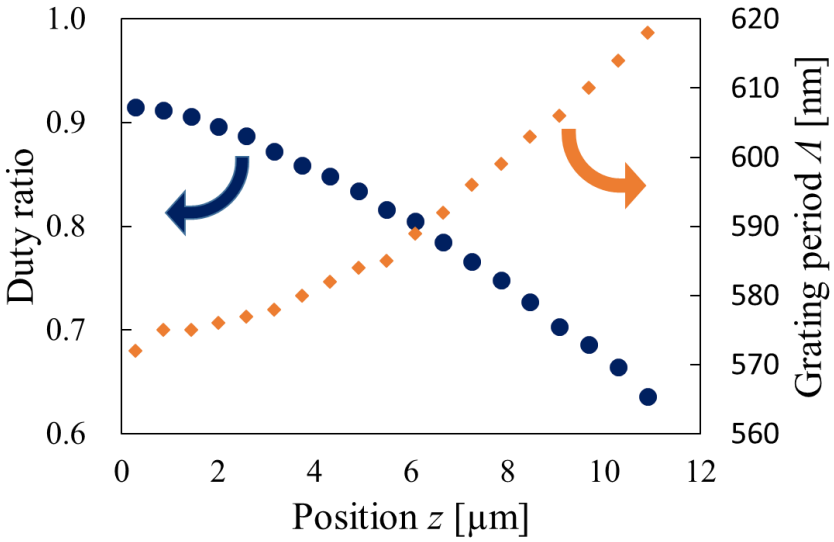


Figure 5. 5 Duty ratio and grating period of designed apodized grating coupler.

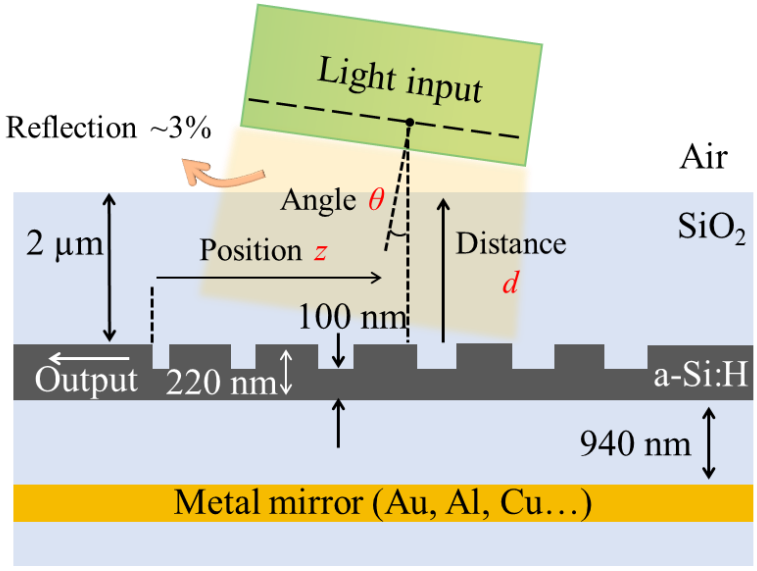


Figure 5. 6 Simulation mode for coupling efficiency calculation.

used at the beginning of the grating and then, the duty ratio gradually decreased to less than 0.64, which corresponded to 225 nm at the end of the grating. In fact, the length of the etched waveguide at the first grating (50 nm) was too small if we consider the fluctuation of the width at the EB lithography or RIE etching. Fluctuation of the depth of the grating was also one of the critical issues caused by RIE lag [10]. For those reasons

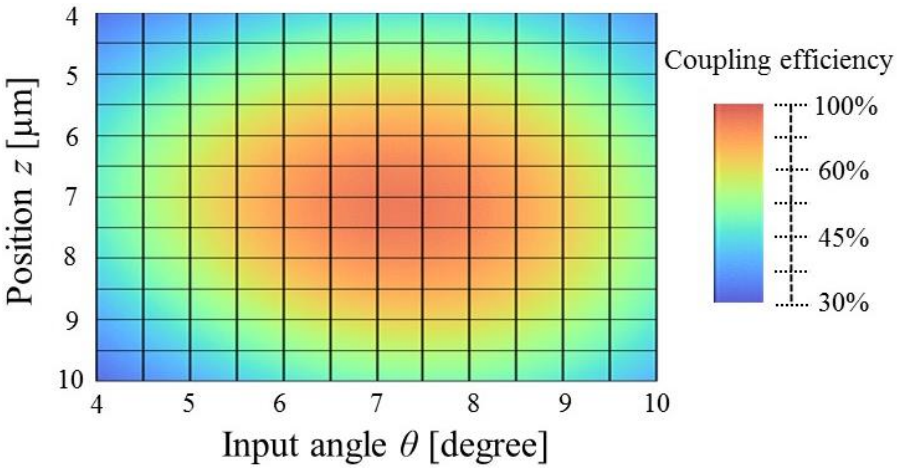


Figure 5. 7 Coupling efficiency dependence on the input angle θ and fiber position *z*.

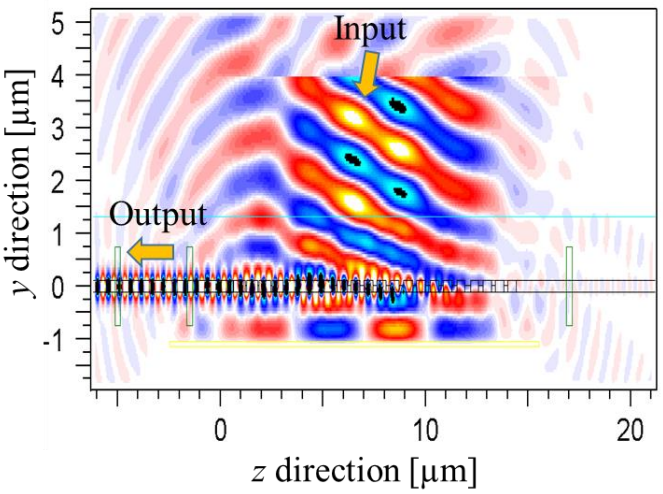


Figure 5. 8 Electric field distribution of the fiber-grating coupler (Fiber input).

above, the minimum groove length of 50 nm would not be realistic value, however, the coupling efficiency of the designed grating coupler was simulated further in order to confirm the designing method of grating used here.

Figure 5. 6 illustrates the simulation model of the coupling efficiency calculation. Instead of the light input from the waveguide, fiber mode input was at the top of the

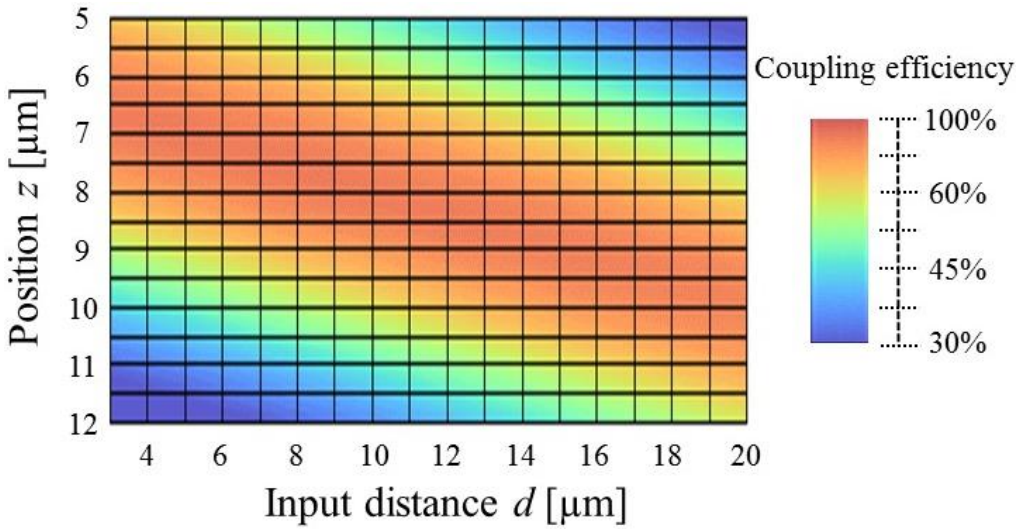


Figure 5. 9 Input distance dependence of coupling efficiency.

grating with an angle θ. About 3% of the input light was reflected at the boundary between the air and the SiO_2 cladding.

The coupling efficiency dependence on the fiber position z and fiber angle θ is shown in Figure 5. 7. Highest coupling efficiency was 95.0% at z= 6.5 μm, θ= 7.5° in the 2D simulation. More than 80% of the coupling efficiency was obtained with z in the range of 6 to 7.5 μm and 6.5 to 8°. If we consider the reflection at the air-SiO_2 boundary, the output mode profile of the grating coupler assumed to be extremely close to the fiber mode-profile.

Then, the coupling efficiency as a function of the distance of the input from the grating and the position of the fiber was investigated as shown in Figure 5. 8. The input distance was varied from 3 μm to 20 μm. As the output light from the grating coupler was radiated with an angle of 7~8°, the position of the fiber should be shifted according to d. The peak coupling efficiency at d= 10 μm, z= 8 μm, was 94.3% and 92.9% of coupling efficiency was obtained even at d= 20 μm, z= 9.5 μm.

Above results were using 2D-FDTD, so the beam broadening or the mode mismatches at the width direction was not considered in the simulation. In order to verify

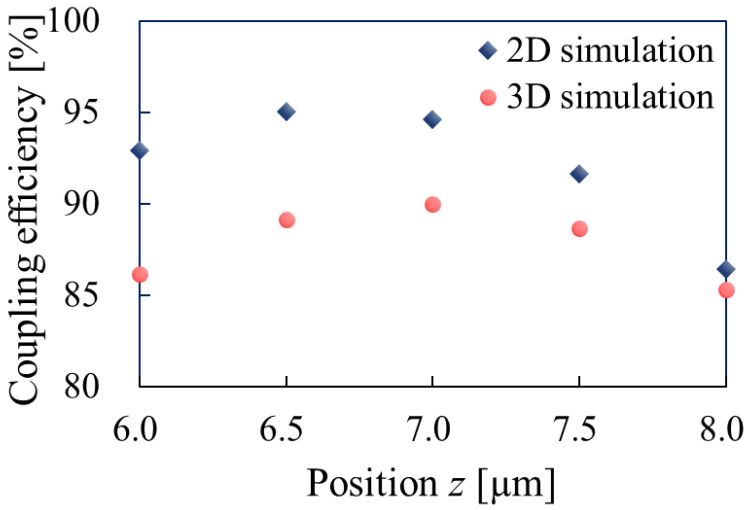


Figure 5. 10 Coupling efficiency calculation by 2D and 3D simulations.

the difference between the 2D and the 3D simulations, the coupling efficiency calculation by 3D-FDTD simulation was carried out with the same structure used at 2D simulation.

Figure 5. 10 shows the coupling efficiency at θ= 7.5° which was calculated by 2D and 3D simulations. The waveguide width in the 3D simulation was 12 μm. There were 5~6% difference between the coupling efficiency calculated by 2D and 3D simulations. It was resulted from that the designed grating coupler was not apodized along the width direction not like the fiber mode-profile. These mismatch can be diminished by introducing focusing grating [11], which can be obtained by curving the grating lines.

5.2.2 Grating coupler with holes

The minimum groove length of the designed apodzied grating coupler in chapter 5.2.1 was 50 nm and 9 grating periods from the front were less than 100 nm. Since the fabrication of 50 nm groove was not realistic in our fabrication process, more practical structure was considered in this section. Target of the redesign was to make the minimum groove length of the grating coupler to be more than 100 nm. In order to achieve the

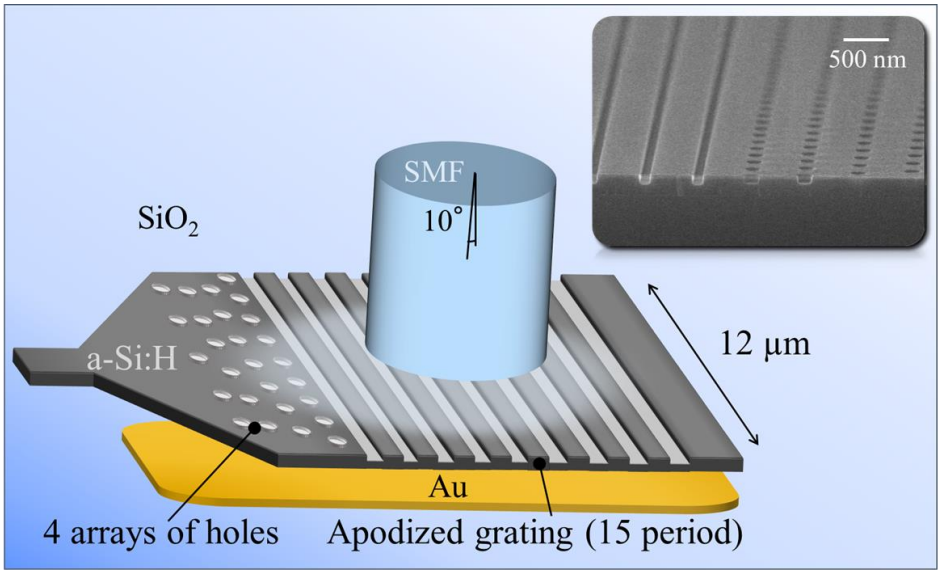


Figure 5. 11 Apodized grating coupler with holes for fiber connection.

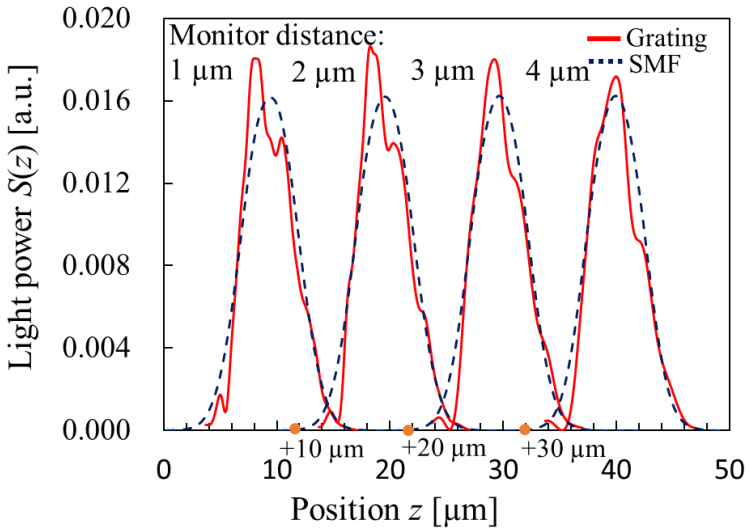


Figure 5. 12 Light power distribution of grating coupler with holes.

minimum groove length, holes, which were similar to PhCs, were introduced instead of usual grooves for the grating. The diameter of the holes was decided to 150 nm considering the fabrication feasibility.

Figure 5. 11 illustrates the schematic image of the apodized grating coupler with holes for fiber connection. 4 periods of grating from the front were substituted by 4 arrays

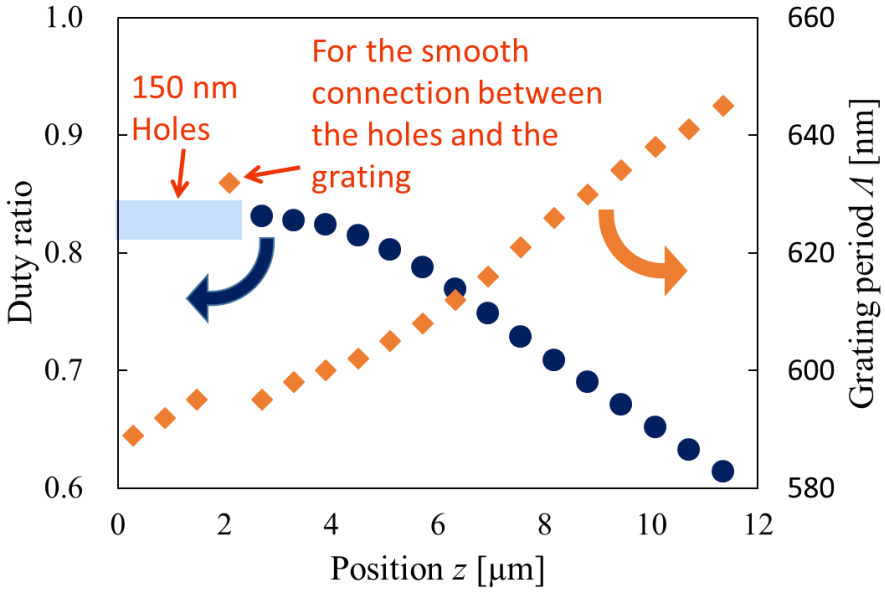


Figure 5. 13 Duty ratio and the grating period

of holes. The minimum groove length was 100 nm and the angle of the input fiber was increased to 10° from 8° in this design. The waveguide width was 12 μm.

Figure 5. 12 shows the light power distribution $S(z)$ of the grating coupler with holes. The power distribution was slightly higher at the front of the grating coupler and slightly lower at the back side of the grating.

The duty ratio of the grating and the grating period of the fiber grating coupler with holes is shown in Figure 5. 13. As holes were used at the front 4 arrays, the duty ratio was not plotted in the figure. Instead, the distances between the each hole in the same array, were 460 nm, 440 nm, 420 nm, and 400 nm. The length of the first groove was 100 nm and that of the last (15^{th}) groove was 249 nm. The grating period was ranging from 590 nm to 645 nm. The grating period of the 4^{th} array of holes was longer than before or after the 4^{th} array for the smooth connection between the holes and the grating. Without this modification, high reflection back to the input port at the boundary between the holes and grating was occurred.

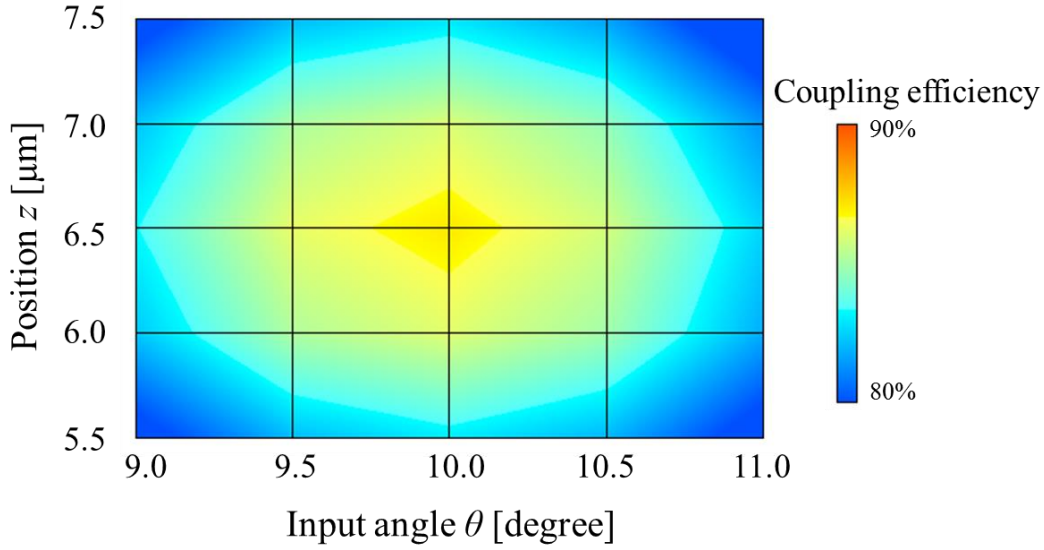


Figure 5. 14 Coupling efficiency of the grating coupler with holes for various input angles θ and fiber position z.

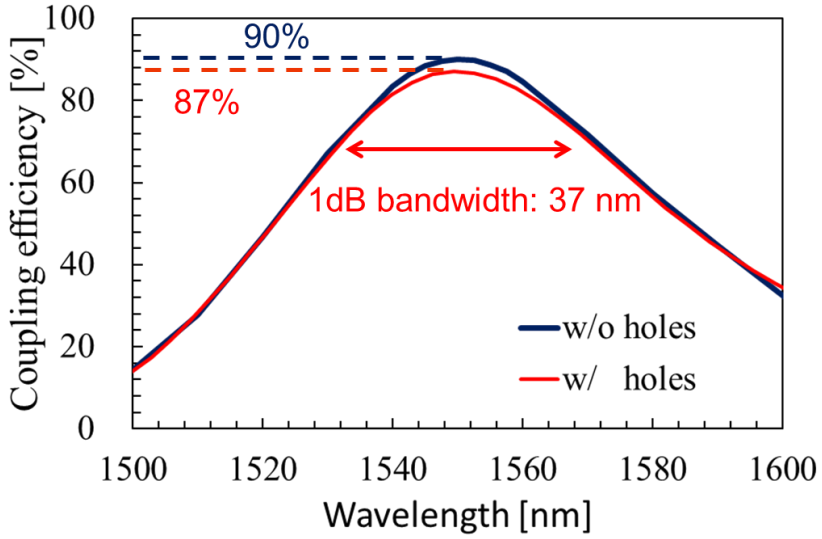
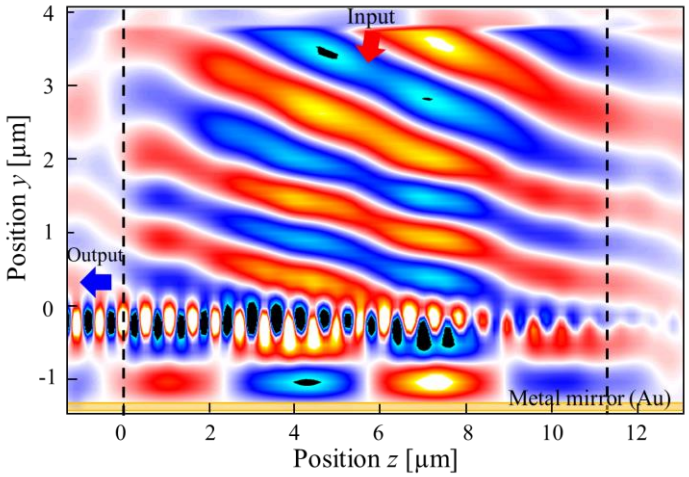


Figure 5. 15 Wavelength dependence of fiber grating coupler with holes.

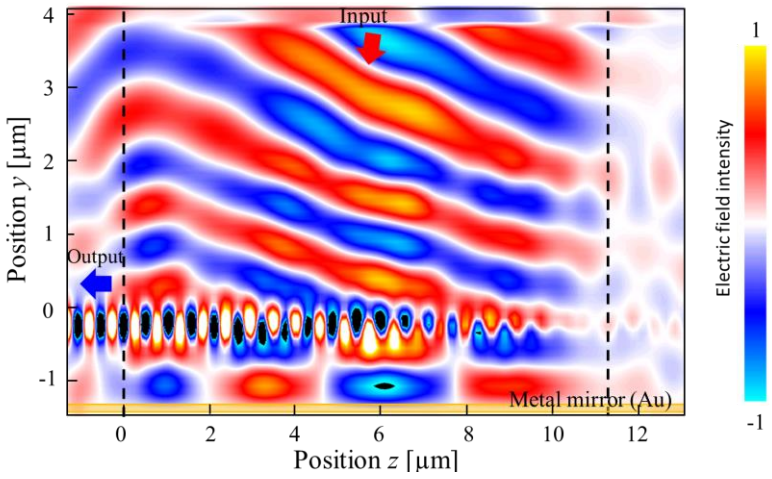
Figure 5. 14 shows the wavelength dependence of the grating coupler with holes. The fiber distance d was 4 μm in this simulation. The peak coupling efficiency was 87.1% at the input angle θ of 10° and the fiber position z of 6.5 μm. The coupling efficiency

exceeded 80% within 1 μm shift of the position *z* from 6.5 μm or 1° changes of the input angle θ from 10°.

Figure 5. 15 shows the coupling efficiency of the fiber grating coupler without and with holes as a function of wavelength. Blue line is without holes and red line is with holes. The peak coupling efficiency of 90% and 87% were obtained at the wavelength of 1.55 μm as designed without and with holes, respectively. In the case of the grating coupler with holes, 1dB bandwidth of the coupling efficiency was 37 nm and 3dB bandwidth was 71 nm. Even the 1dB bandwidth can cover the c-band.



(a) With holes

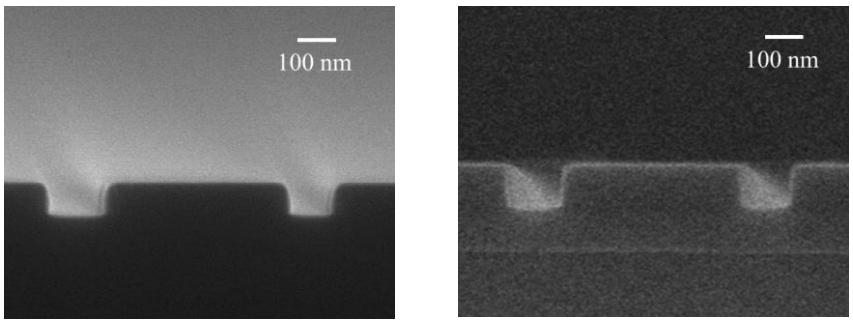


(b) Without holes

Figure 5. 16 Electric field distribution of fiber grating coupler with and without holes.

Figure 5. 16 shows the electric field distribution of the fiber grating coupler (a) with and (b) without holes.

Without holes means the first 4 arrays of holes are not etched in the designed grating coupler with holes. The coupling efficiency of the fiber grating coupler without holes was 80.6% which was about 7 % lower than that of with holes. Reflection at the front of the grating coupler can be seen since the mode mismatching was occur without holes.



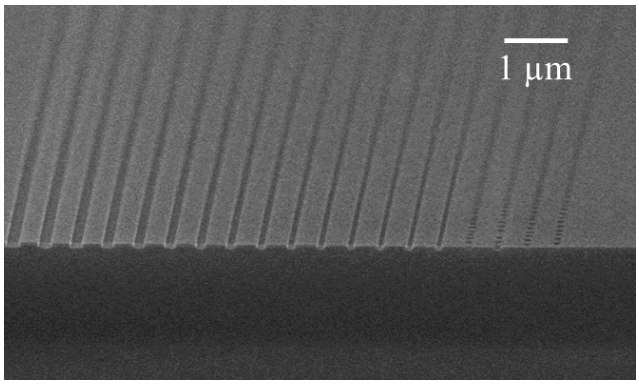
(a) Without SiO2 intermediate layer (b) With SiO2 intermediate layer

Figure 5. 17 Cross-sectional SEM images of grating.

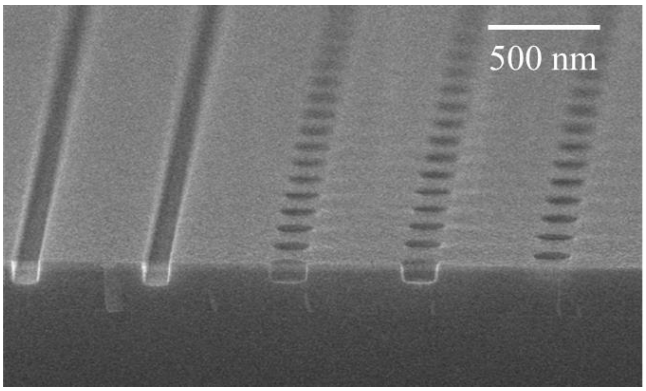
For the further improvement of the coupling efficiency, 2 ways can be considered. Because the light power distribution from the grating coupler was higher than the fiber mode profile as shown in Figure 5. 12, it is important to lower the leakage factor of the front of the grating coupler. In the condition of the minimum groove length fixed as 100 nm, introducing more arrays of holes can be effective. Or the second approach is to change the grating depth to less than 100 nm. Overall leakage factor of the grating will be lowered since the highest leakage factor was shown at 100 nm of grating depth. In this case, the inter-layer apodized grating coupler with metal mirrors should be also redesigned with the new grating depth.

5.2.3 Fabrication of grating with holes

In this section, the fabrication of grating with holes will be presented. Basic fabrication process was almost same with that of uniform grating. The only difference is 60 nm of SiO_2 intermediate layer was introduced between a-Si:H layer and ZEP resist.



(a)



(b)

Figure 5. 18 SEM images of (a) fabricated gratings with holes, and (b) enlarged image.

Figure 5. 17 shows the cross-sectional SEM images of the grating fabricated with and without the SiO_2 intermediate layer. The sidewall angle was close to 90° with the SiO_2 intermediate layer. Figure 5. 18 shows the SEM images of fabricated grating with holes by utilizing the fabrication process above. The groove length of 100 nm was successfully fabricated and 150-nm-diameter holes were also formed at the same time.

5.2.4 Fabrication process of grating coupler with holes

The grating coupler with holes was fabricated based on the design described in section 5.2.2. The fabrication process of the grating coupler with holes are illustrated in Figure 5. 19. The initial wafer was 2-inch Si wafer with 3-μm-thick layer of thermal SiO_2. The first

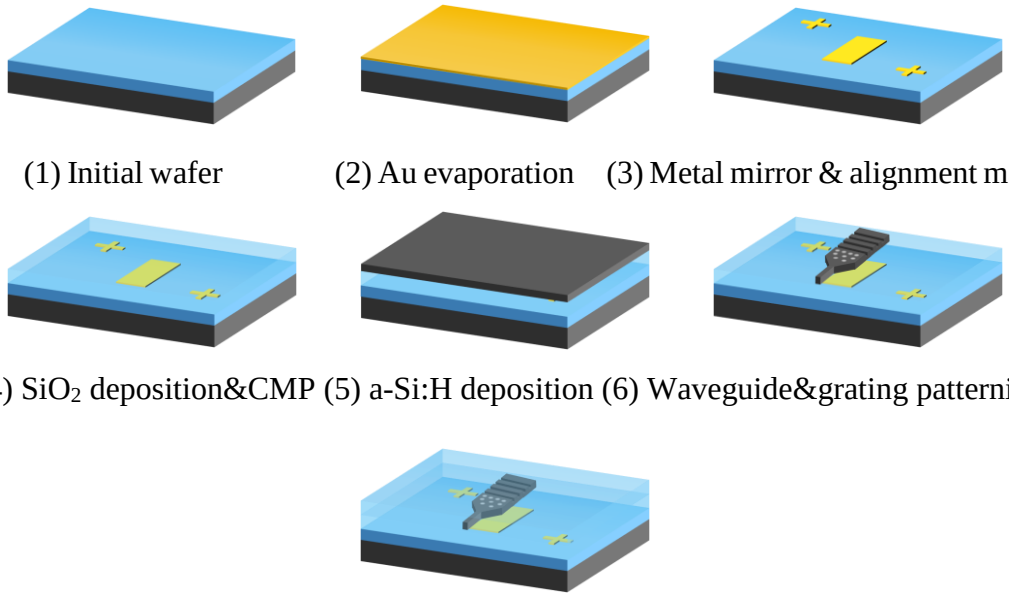


Figure 5. 19 Fabrication process of apodized grating coupler with holes

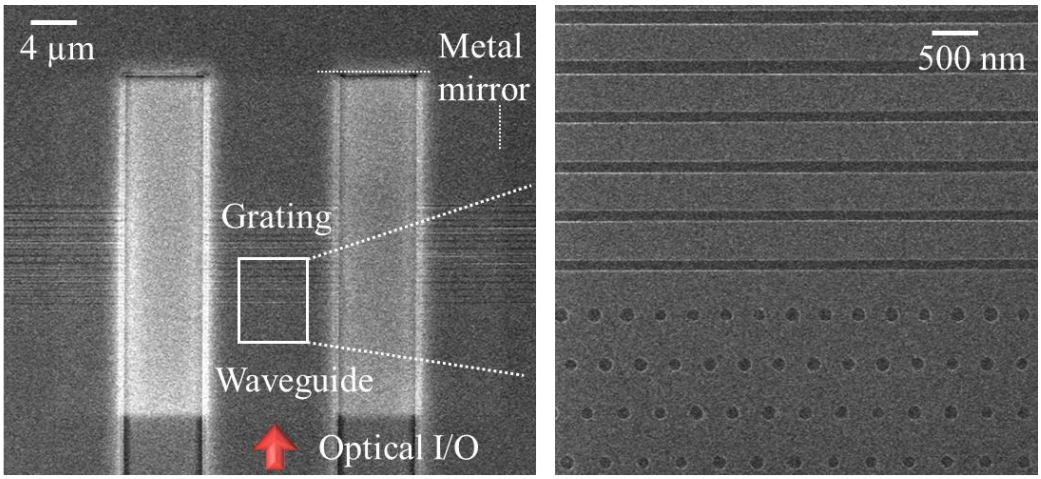


Figure 5. 20 Top SEM image of apodized grating and its enlarged image.

step was evaporation of a 100-nm-thick Au film (other metals such as Al can be used) on the SiO_2 and the metal mirror and alignment mark for EB-lithography was formed by lift-off. The Au patterns were buried by SiO_2 and then flattened by chemical mechanical polishing (CMP) process. The thickness of SiO_2 was controlled targeting 940 nm and then, 220-nm-thick a-Si:H layer was deposited on the SiO_2 at 300℃. The apodized grating with holes and waveguide patterns were formed by EB lithography and ICP-RIE

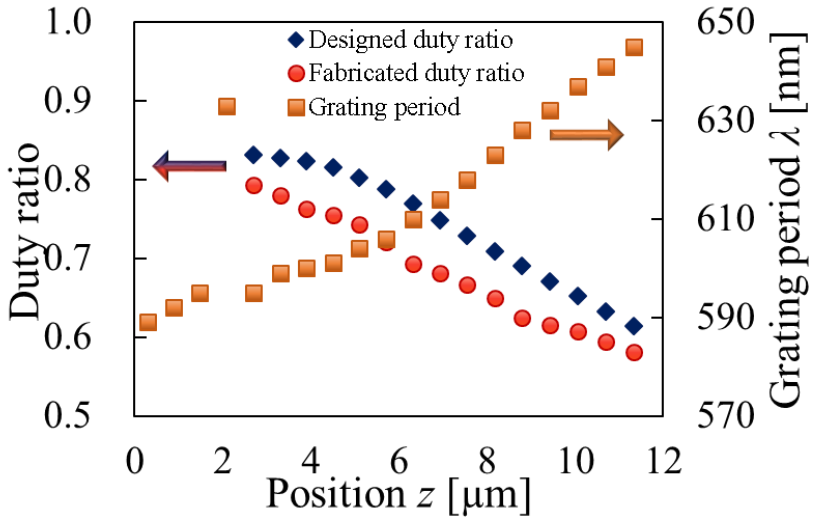


Figure 5. 21 Duty ratio and grating period of designed and fabricated apodized grating coupler

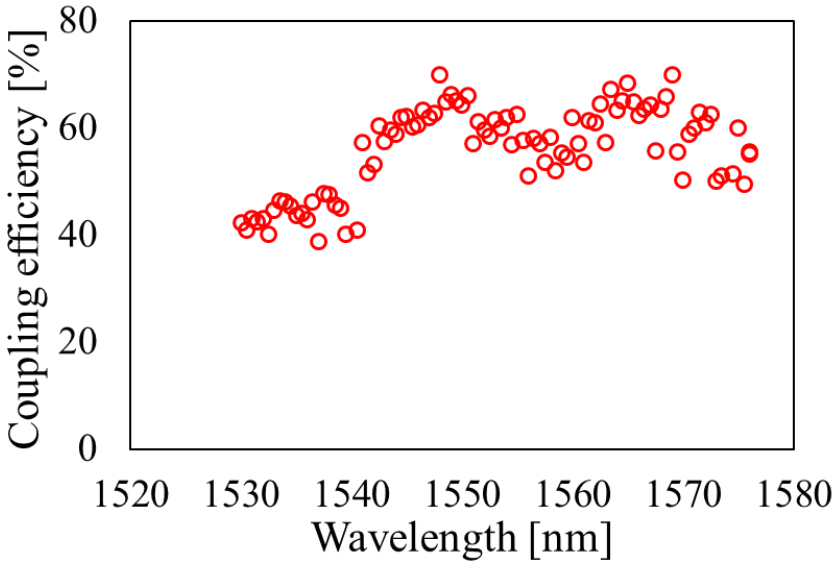


Figure 5. 22 Measured coupling efficiency of apodized grating coupler with metal mirror

process. Finally, 2 μm of SiO_2 overcladding layer was deposited and flattened again by CMP process. After the fabrication process, the thickness of DM was confirmed to be 915 nm.

Figure 5. 20 shows the top SEM image of the apodized grating placed above the metal mirror which can be seen through the waveguide patterns and the grating was

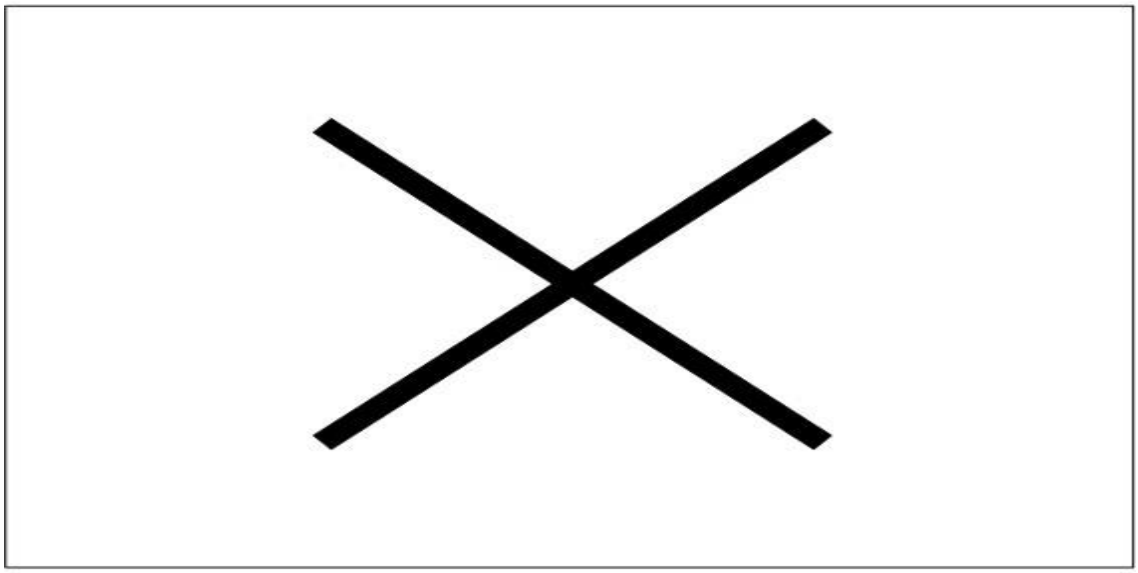


Figure 5. 23 Long wavelength VCSEL (*N. Nishiyama et al.*, Corning Inc. 1999) [18]

located at the center of the metal mirror. The duty ratio of the fabricated apodized grating is plotted in Figure 5. 21. There is 2~8% difference in the designed and fabricated values of duty ratio.

The measured coupling efficiency of the apodized grating coupler with the metal mirror is shown in Figure 5. 22. The coupling efficiency of the fabricated apodized grating coupler with the metal mirror was calculated by fiber to fiber transmission through a pair of grating couplers. The peak coupling efficiency was 70%, which was smaller than the designed coupling efficiency. This can be explained by that the duty ratio of the fabricated grating was slightly different from the target value. Higher coupling efficiency can be expected with correct groove-lengths control of apodized grating by adjusting the exposure amount in the EB lithography. Even though, the monolithically stacked a-Si:H grating coupler was successfully demonstrated with the metal mirror which is promising for the realization of 3D optical interconnect.

5.3 Integration of optical source

As an optical source for silicon photonics, hybrid semiconductor lasers based on III-V materials have been widely researched as explained in chapter 1.3.2. In this section, VCSELs will be discussed as an optical source for silicon photonics. Relatively low price than other in-plane semiconductor lasers and its mass production capability made the

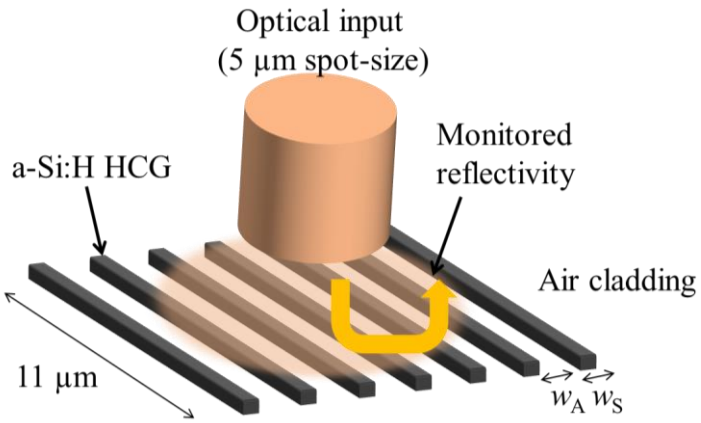


Figure 5. 24 Model for reflectivity simulation of HCG.

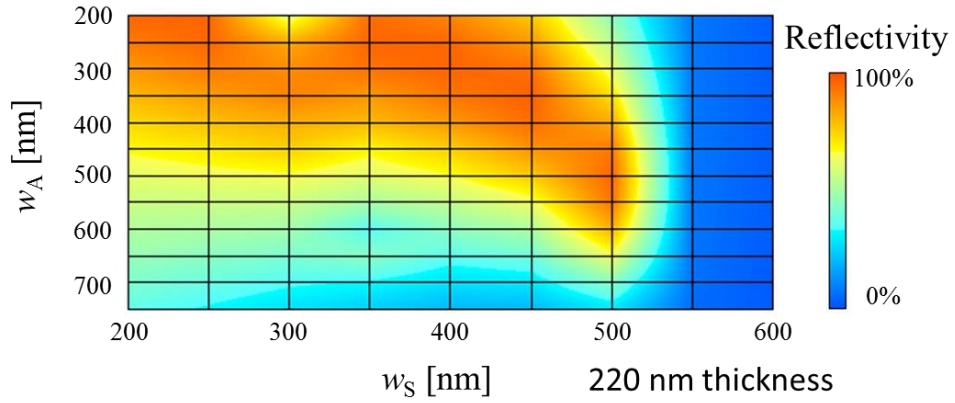
VCSELs more useful in many fields. VCSELs are being broadly used not only in the fields of short-range optical communications [12-14], laser printers, or computer mice [15], etc.

5.3.1 VCSELs operating at long wavelength

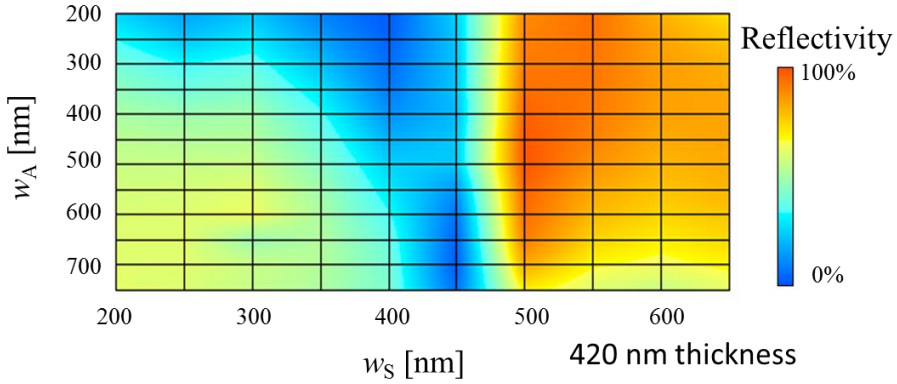
Typically, VCSELs are fabricated on the GaAs substrates and emit lights for the wavelength range from 850 to 980 nm. But, if we consider integration of VCSELs on the devices of silicon photonics, wavelength of 1.3 µm or 1.55 µm is recommended. For the long wavelength VCSELs, GaInNAs quantum wells (QWs) on GaAs substrate or AlGaInAs QWs on InP substrate have been reported [16-18]. In this section, wavelength of 1.55 µm VCSELs consisting of AlGaInAs-InP DBRs and AlGaInAs QWs as shown in Figure 5. 23 (Corning Inc.) will be considered as an integrated VCSELs on Si substrate.

5.3.2 Design of high reflectivity HCG structure

As shown in Figure 5. 2, half VCSEL will be used in this section. The reflectivity of the one side mirror was 99.9%. HCG structure made on the Si surface was assumed to be



(a) HCG thickness: 220 nm



(b) HCG thickness: 420 nm

Figure 5. 25 Calculated reflectivity of HCG.

used as the other side of the mirror. As a reflectivity of the HCG, more than 99.5 was needed in order to achieve the high performance operation of the VCSEL. Simulation model for the reflectivity calculation of HCG is shown in Figure 5. 24. The input was Gaussian beam of 5-μm-spot-size assuming the spot-size of the half VCSEL. In this simulation, the HCG thickness of 220 nm and 420 nm was simulated with 2 parameters; w_S and w_A. w_S is the length of the Si and w_A is the length of the air cladding. Figure 5. 25 shows the calculated reflectivity of HCG with thickness of (a) 220 nm and (b) 420 nm. When the thickness was 220 nm, the highest reflectivity of 96.4% was obtained at the w_S: 450 nm and w_A: 600 nm. In the case of the thickness was 420 nm, the highest reflectivity of 98.9% was obtained at the w_S: 500 nm and w_A: 450 nm. The reflectivity was further

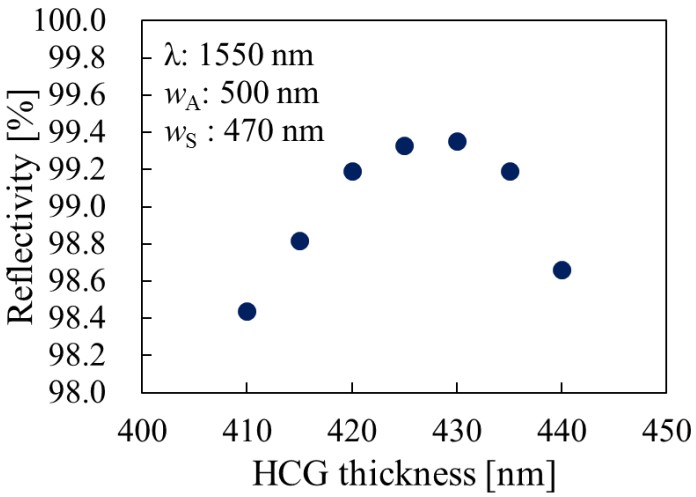


Figure 5. 26 Calculated reflectivity of HCG as a function of HCG thickness.

improved by varying the thickness of the HCG. The highest reflectivity of 99.4% was obtained when the HCG thickness was 430 nm as shown in Figure 5. 26.

5.4 Conclusion

In this chapter as other applications of the grating couplers for 3D optical interconnect, fiber grating coupler and integration of light source was discussed.

First, as an optical I/O for the 3D optical interconnect, fiber grating coupler was designed. Apodization of the grating coupler was done by 2D simulations and the output mode profile of the grating coupler was well matched with the fiber-mode profile. The metal mirror was used for the high coupling efficiency and the distance from the metal mirror to the grating was 940 nm. The depth of the grating was 100 nm and input fiber angle was 8°. The minimum groove length of the designed grating coupler was 50 nm. The coupling efficiency of 94.6% was obtained by 2D-FDTD simulation and 90.0% of coupling efficiency was obtained by 3D-FDTD simulation.

Then, more practical structure of which the minimum groove length was 100 nm, was designed with 4 arrays of holes at the front of the grating coupler. The coupling efficiency of the grating coupler with holes was 87.1%. In the case of the same design without holes, the coupling efficiency was dropped to 80.6%. The coupling efficiency difference of 6.5% was come from the 4 arrays of holes.

Last of this chapter was focused on the integration of long-wavelength VCSEL to the Si substrate. The structure was to use half VCSEL over the HCG reflector formed by Si. The highest reflectivity was 98.9% which was slightly lower than the target reflectivity of 99.4%. Higher reflectivity can be expected with further optimized structure by fine tuning of w_S and w_A.

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Chapter 6
Conclusion

The main objective of this thesis is to realize the 3D optical interconnect based on the a-Si:H multi-stacked waveguides. In order to achieve vertical coupling between the multi-layered waveguides, the inter-layer grating couplers were proposed and designed in this thesis. High coupling efficiency exceeds 80% was also demonstrated. Those inter-layer grating couplers can achieve vertical coupling at long distance more than 1 μm. The distance is not possible to achieve by a directional coupler type reported in 2008. The available inter-layer distance of the directional coupler type vertical coupler is less than 500 nm since it requires overlap of the evanescent light between multi-layered waveguides if we consider the coupler length of ~200 μm.

Grating couplers had been used typically as a coupler between fibers and waveguides at the start of this thesis. Therefore, in order to investigate the characteristics of stacked grating couplers as the inter-layer coupler following issues were studied and demonstrated in this thesis.

(1) Establishments of fabrication process for low-loss multi-stacked a-Si:H waveguides
  (a) Deposition condition of low-loss a-Si:H film for multi-stacked waveguides
  (b) Surface roughness of multi-stacked waveguides
  (3) Propagation loss of multi-stacked waveguides.

(2) Demonstration of the inter-layer grating couplers
  (a) Inter-layer grating couplers without metal mirrors.
  (b) Inter-layer grating couplers with metal mirrors.
  (c) Inter-layer apodized grating couplers with metal mirrors.

The summaries of each chapter are as follows.

In chapter 1, as an introduction of this thesis, interconnection fulfilled by optical devices was explained. Conventional electrical interconnect are now approaching their performance limit as the speed and amount of the transmitted data are grown and will grow constantly. Instead of the conventional electrical interconnect, optical interconnect can provide a high speed and low power-consumption solution.

Already, board-to-board interconnection was commercialized toward supercomputers and data-centers and on-board or even for on-chip interconnection are now studied intensively. As an on-chip and on-board interconnection, silicon photonics attracted much attention for its characteristics such as small foot print, cost effective and CMOS compatible process, etc. If we consider on-chip optical interconnect using silicon photonics, back-end process compatibility is necessary for monolithic integration of optical devices on LSI chip.

Among the Si materials such as c-Si and poly-Si, only a-Si:H is back-end process compatible material since it can be deposited at 300℃. Moreover, by stacking a-Si:H and SiO_2 alternatively, multi-layered optical interconnect can easily be realized for higher transmission density. The advantages of multi-stacking of optical interconnect including issues regarding transmission density and waveguide crossings were introduced in the chapter 1.

In chapter 2, establishment of the fabrication process and demonstration of low-loss multi-stacked waveguides were presented. a-Si:H tends to have high absorption loss when there are defects or dangling bonds in the a-Si:H film, depending on the deposition condition. Further, in order to achieve low-loss a-Si:H waveguides at the multi-stacked waveguides, the surface roughness of a-Si:H film is also important. The accumulation of the surface roughness at multi-stacked waveguides could raise high scattering loss.

Various parameters of deposition condition were investigated for the low surface roughness. The deposition pressure was the key factor for low surface roughness, and by reducing the process pressure from 130 Pa to 30 Pa, the surface roughness was improved

from 1.06 nm to 0.30 nm. Even the 3rd layer showed the surface roughness of 0.52 nm. Next, the propagation loss of the multi-layered waveguides were measured.

The propagation loss of the 1st layer c-Si, the 2nd and the 3rd layer a-Si:H waveguides deposited at 130 Pa were 6.0 dB/cm, 10.2 dB/cm, and 12.0 dB/cm, respectively. The propagation loss of the 2nd layer a-Si:H waveguide was improved as 7.0 dB/cm thanks to the decreased surface roughness. Further improvement was achieved by introducing ICP-RIE system, and the propagation loss of 1st c-Si, the 2nd and the 3rd layer a-Si:H waveguides deposited at 30 Pa were 1.6 dB/cm, 3.8 dB/cm, and 3.7 dB/cm, respectively. These results also showed good agreements in the numerical analysis based on the relationship between the surface roughness and the propagation loss.

In chapter 3, the inter-layer grating couplers were numerically studied. First, numerical calculation of diffraction by gratings including the diffraction angle determined by grating period, or power leakage factor related with duty ratio and grating depth were presented.

As a vertical coupler between multi-layered waveguides, inter-layer grating coupler without metal mirrors were designed. The layer-distance was fixed to 1 μm as the minimum layer-distance concerning the optical crosstalk between multi-layered waveguides and crossings. Full etched gratings were used for this design in order to simplify the structure since it was the first trial of a multi-layered device. The peak coupling efficiency of the designed inter-layer grating couplers was 19% at the grating period of 640 nm with 10 gratings.

Then, in order to increase the coupling efficiency, metal mirrors were introduced to the inter-layer grating couplers. Radiated light to the opposite side of the grating coupler can be reflected by the metal mirrors when the phase matching condition was satisfied. The distance from the metal to the grating was 800 nm for this case. The depth of the grating was changed to 70 nm and the number of gratings were 21. At the grating period of 640 nm, the peak coupling efficiency of 90% was estimated. More than 80% of coupling efficiency was obtained in the wavelength range from 1520 to 1600 nm. The

difference on the coupling efficiency caused by misalignment were less than 0.5dB for both the propagation direction and the orthogonal direction. In particular, the improved misalignment tolerance was caused by the changing the grating depth to 70 nm which led the longer grating length.

Finally, inter-layer apodized grating couplers with metal mirrors were designed for the layer-distance independent operation. The output mode-profile of the grating coupler were tuned to be symmetric shape in propagation direction. By this, the reflection and interference between the 1st and the 2nd layer grating couplers were suppressed. The distance from the 1st or 2nd layer grating to the metal mirrors were optimized as 940 nm and 820 nm, respectively. The coupling efficiency of more than 90% was maintained within the inter-layer distance up to 4 μm. More than 80% of coupling efficiency was obtained at the wavelength range from 1510 nm to 1570 nm, which was further increased to more than 200 nm by introducing a longer grating period.

In chapter 4, the experimental results including fabrication and coupling efficiency measurement of the inter-layer grating couplers and high-speed data transmission through inter-layer grating couplers were demonstrated.

Based on the established fabrication process in chapter 2, the inter-layer grating couplers without and with metal mirrors were fabricated. CMP process was introduced to maintain the flatness and the roughness of the surface in multi-layered structure. The surface roughness less than 0.4 nm was obtained with SiO_2 surface.

Then, the fabrication process of the grating couplers were explained. The misalignment by the EB lithography was less than 30 nm from the SEM images. The coupling efficiency of 22% (Simulation: 19%) was measured by the inter-layer grating couplers without metal mirrors. The measured coupling efficiency was 3% higher than the simulation results since the reflections from the air cladding and Si substrate were not included in the simulation model.

For the inter-layer grating couplers with metal mirrors, there were 2 samples fabricated here. The first sample showed thickness differences up to 250 nm from the

design values, and the peak coupling efficiency was 31% which was much lower than the simulated value of 90%. The second sample was fabricated with the thickness difference within 10 nm from the target value and the peak coupling efficiency was 83%.

Finally, high-speed data transmission through the inter-layer grating couplers with metal mirrors was demonstrated. Clear eye openings were confirmed at the data rates up to 50Gbps which indicated there was no degradation of signal even with reflections at the metal mirrors.

In the chapter 5, other application of grating couplers for 3D optical interconnect were presented. As an optical I/O of the 3D optical interconnect, a grating coupler for the fiber to waveguide connection was designed. The output mode profile of the grating was apodized to match the profile of the fiber mode-profile. The metal mirrors was also used for the high coupling efficiency and the distance from the grating to the metal mirror was 940 nm. The grating depth of 100 nm was used with 19 gratings and the input fiber angle was 8° in this simulation. The minimum groove length was 50 nm which was too small in consideration of fabrication accuracy or the RIE lag though, the coupling efficiency of 94.6% was obtained by 2D-FDTD simulation and 90.0% by 3D-FDTD simulation.

Next, 4 arrays of holes were introduced instead of gratings of short groove length for the practical structure considering the fabrication process. The minimum groove length of 100 nm was successfully designed with 150 nm of the hole diameter. The coupling efficiency was 87.1% and in the case of the same design without holes which only had 15 grating periods, the coupling efficiency was dropped to 80.6%. Based on the above designed grating with holes, the fiber grating coupler was fabricated. The distance from the metal mirror to the grating was 915 nm and there was 2~8% difference in the designed and fabricated values of duty ratio which were responsible for the slightly-low measured coupling-efficiency of 70%.

Then, the integration of long-wavelength VCSEL on the Si substrate was considered for the light source of the 3D optical interconnect. The target design was to use Si HCG as a reflector of one side mirror of VCSEL. The structure of HCG was not fully optimized

yet, the reflectivity of 99.4% was obtained in the 3D-FDTD simulation. It was slightly lower than the desired reflectivity of more than 99.5% though, higher reflectivity could be achieved by optimizing the HCG structure.

Through this entire thesis, the possibility of the a-Si:H optical devices as a 3D optical interconnect have been discussed. Highly efficient inter-layer grating couplers will boost the performance of the 3D optical interconnect as a basis. The numerical and experimental analysis of the grating coupler including apodization and metal mirror associated characteristics will also be beneficial to the other applications such as fiber-to-waveguide coupler presented here.

In order to realize the 3D optical interconnects however, there are some remained issues. The inter-layer apodized grating couplers with metal mirrors, grating couplers for coupling between fibers and wire waveguides, and integration of VCSEL on a Si substrate, were numerically analyzed but not yet demonstrated. It needs to be confirmed whether the experimental results match with the theoretical expectations. Furthermore, other devices which was not included in this thesis such as monolithically integrated photodetectors, optical modulator, and other passive or active optical devices should be developed considering the fabrication-process compatibility for the monolithic integration on a LSI chip.

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Publication list

(1) ***Journal Papers***

1. **J. Kang**, Y. Atsumi, M. Oda, T. Amemiya, N. Nishiyama, and S. Arai, "Low-loss Amorphous Silicon Multilayer Waveguides Vertically Stacked on Silicon-on-Insulator Substrate", *Jpn. J. Appl. Phys.*, Vol. 50, No. 12, p 120208, Nov. 2011.

2. **J. Kang**, Y. Atsumi, M. Oda, T. Amemiya, N. Nishiyama, and S. Arai, "Layer-to-Layer Grating Coupler based on Hydrogenated Amorphous Silicon (a-Si:H) for 3D Optical Circuits", *Jpn. J. Appl. Phys.*, Vol. 51, No. 12, p 120203, Nov. 2012.

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(2) ***International Conferences***

1. **J. Kang**, K. Inoue, Y. Atsumi, N. Nishiyama, and S. Arai, "Loss Measurement of Multiple Layer a-Si Waveguides." *2010 Int. Conf. Solid State Devices and Materials (SSDM 2010)*, D-8-2, Tokyo (Japan), Sep. 2010.

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3. **(Invited) J. Kang**, N. Nishiyama, Y. Atsumi, T. Amemiya, and S. Arai, "Multi-stacked silicon wire waveguides and couplers toward 3D optical interconnects," *OPTO2013 (part of SPIE Photonics West 2013)*, SPIE 8630-7, San Francisco (USA), Feb. 2013.

4. **J. Kang**, Y. Atsumi, T. Sifer, Y. Hayashi, T. Amemiya, N. Nishiyama, and S. Arai, "Inter-Layer Grating Coupler with Metal Mirrors for 3D Optical Interconnects," *The 10th Conference on Lasers and Electro-Optics Pacific Rim (CLEO-PR 2013)*, MM1-5, Kyoto (Japan), Jul. 2013.

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(3)***Meeting Reports and Symposia***

1. **J. Kang**, Y. Atsumi, M. Oda, N. Nishiyama, and S. Arai, "Low-loss multiple-stacked amorphous silicon wire waveguide on SOI" *Technical Meeting of IEICE, SiPH 2009*, Tokyo (Japan), P-20, Nov. 2011.

2. **J. Kang**, Y. Atsumi, M. Oda, N. Nishiyama, and S. Arai, "Low-loss Amorphous Silicon Wire Waveguides Multilayer Stacked on SOI," *The 1st International Symposium on Photonics and Electronics Convergence, ISPEC2011*, P-34, Tokyo, Japan, Nov. 2011.

3. **J. Kang**, Y. Atsumi, M. Oda, T. Amemiya, N. Nishiyama, and S. Arai, "Metal mirror assisted grating couplers between multilayered waveguides toward 3D optical interconnects" *Technical Report of IEICE*, OPE2011-146, pp. 27-32, Tokyo (Japan), Dec. 2011.

4. **J. Kang**, Y. Atsumi, T. Sifer, Y. Hayashi, T. Amemiya, N. Nishiyama, and S. Arai, "High Efficient Layer-to-Layer Si Grating Coupler Sandwiched by Metal Reflectors for Intra-chip Interconnection," *The 2nd International Symposium on Photonics and Electronics Convergence, ISPEC2012*, P38, Dec. 2012.

5. **J. Kang**, Y. Atsumi, Y. Hayashi, J. Suzuki, Y. Kuno, T. Amemiya, N. Nishiyama, and S. Arai, "High Efficiency Inter-Layer Amorphous Silicon Grating Couplers with Metal Mirrors for On-Chip 3D Interconnects," *The 2nd International Symposium on Photonics and Electronics Convergence, ISPEC2013*, P-43, Tokyo, Japan, Nov. 2013.

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8. Y. Atsumi, M. Oda, **J. H. Kang**, N. Nishiyama, and S. Arai, "Athermal Wavelength Filters toward Photonic Integrated Circuits" *The 1st International Symposium on Photonics and Electronics Convergence, ISPEC2011*, Tokyo, Japan, P-20, Nov. 2011.

9. M. Oda, Y. Atsumi, **J. Kang**, N. Nishiyama, and S. Arai, "L Wide-gap Athermal Si-Slot Wavelength Filters Embedded with Benzocyclobutene," *Technical Meeting of IEICE, SiPH 2011*, Tokyo, Japan, P17, Nov. 2011.

10. Y. Hayashi, R. Osabe, K. Fukuda, Y. Atsumi, **J. Kang**, N Nishiyama, S. Arai, "GaInAsP/SOI Hybrid Laser by N_2 Plasma Activated Low Temperature Bonding," *The 2nd International Symposium on Photonics and Electronics Convergence, ISPEC2012*, P39, Dec. 2012

11. Y. Atsumi, T. Sifer, **J. Kang**, N. Nishiyama, and S. Arai, "Wavelength Trimming of Athermal Si Slot Wavelength Filters using Deep-ultraviolet Exposure" *The 2nd International Symposium on Photonics and Electronics Convergence, ISPEC2012*, P40, Dec. 2012.

12. Y. Hayashi, R. Osabe, K. Fukuda, Y. Atsumi, **J. Kang**, N Nishiyama, S. Arai, "III-V/Si Direct Bonding by N_2 Plasma Surface Activation and Its Application to Hybrid Laser," *Technical Report of IEICE, LQE2012-129*, pp. 35-40, Dec. 2012

13. Y. Atsumi, **J. Kang**, Y. Hayashi, J. Suzuki, N. Nishiyama, and S. Arai, "Humidity Tolerance of Athermal Si-Slot Wavelength Filters Embedded with Polymer" *The 3rd International Symposium on Photonics and Electronics Convergence, ISPEC2013*, P4, Nov. 2013

14. T. Amemiya, T. Kanazawa, A. Ishikawa, **J. Kang**, N. Nishiyama, Y. Miyamoto, T Tanaka, and S. Arai, "Permeability control on InP-based photonic integration platform using metamaterial," *Technical Report of IEICE*, OPE2013-146, pp. 45-50, Tokyo (Japan), Dec. 2013.

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(4)***Domestic Conferences***

1. **J. Kang**, Y. Atsumi, M. Oda, N. Nishiyama, and S. Arai, "Low-Propagation Loss-Properties of Multiple-Layer Amorphous Si Wire-Waveguides," *The 58th Spring Meeting, 2011; The Japan Society of Applied Physics and Related Societies*, 24-KB-9, Kanagawa, Mar. 2011.

2. **(Invited) J. Kang**, Y. Atsumi, M. Oda, N. Nishiyama, and S. Arai, "Optical Waveguide Fabrications toward On-Chip Optical Wiring," *The 2012 IEICE Society Conference*, C-3-50 Sapporo, Sep. 2011.

3. **J. Kang**, Y. Nishikawa, Y. Atsumi, M. Oda, T. Amemiya, N. Nishiyama, and S. Arai, "Grating Couplers between Multilayer Amorphous Silicon Waveguides," *The 2012 IEICE General Conference*, C-3-38, Okayama, Mar. 2012.

4. **J. Kang**, Y. Atsumi, T. Sifer, T. Amemiya, N. Nishiyama, and S. Arai, "Metal Mirror Reinforced Grating Couplers between Multilayer Amorphous Silicon Waveguides," *The 2012 IEICE Society Conference*, C-3-59, Toyama, Sep. 2012.

5. **J. Kang**, Y. Atsumi, T. Sifer, Y. Hayashi, T. Amemiya, N. Nishiyama, and S. Arai, "Metal Mirror Reinforced Grating Couplers between Multilayer Amorphous Silicon Waveguides", *The 2013 IEICE General Conference*, C-3-41, Gifu, Mar. 2013.

6. **J. Kang**, Y. Atsumi, Y. Hayashi, J. Suzuki, Y. Kuno, T. Amemiya, N. Nishiyama, and S. Arai,

"Grating Couplers between Multilayer Amorphous Silicon Waveguides with Metal Mirrors", *The 2013 IEICE Society Conference*, C-3-14, Tokushima, Sep. 2013.

7. **J. Kang**, Y. Kuno, Y. Hayashi, J. Suzuki, T. Amemiya, N. Nishiyama, and S. Arai, "Numerical Analysis of Apodized Grating Coupler Loaded with Metal Mirror for Optical Fiber Connection," *The 2014 IEICE Society Conference*, C-3-49, Fukuoka, Sep. 2014.

8. Y. Atsumi, J. Kang, Y. Maeda, M. Oda, N. Nishiyama, and S. Arai, "Loss Reduction of Si-Slot Ring Resonator Embedded with Benzocyclobutene", *The 71th Fall Meeting, 2010; The Japan Society of Applied Physics and Related Societies*, 14-G-16, Nagasaki, Sep. 2010.

9. T. Shindo, T. Okumura, H. Ito, T. Koguchi, Y. Atsumi, **J. Kang**, R. Osabe, N. Nishiyama, and S. Arai, "Lateral Current Injection DFB Laser with a-Si Surface Grating", *The 71th Fall Meeting, 2010; The Japan Society of Applied Physics and Related Societies*, 16p-H-11, Nagasaki, Sep. 2010.

10. Y. Atsumi, M. Oda, **J. Kang**, N. Nishiyama, and S. Arai, "Broad-gap Athermal Si-Slot Mach-Zehnder Interferometer Embedded with Benzocyclobutene", *The 58th Spring Meeting, 2011; The Japan Society of Applied Physics and Related Societies*, 24a-KB-8, Kanagawa, Mar. 2011.

11. Y. Atsumi, M. Oda, **J. Kang**, N. Nishiyama, and S. Arai, "Wide-gap Athermal Si-Slot Ring resonator Embedded with Benzocyclobutene", *The 72th Fall Meeting, 2011; The Japan Society of Applied Physics and Related Societies*, 21-ZN-9, Yamagata, Aug. 2011.

12. M. Oda, Y. Atsumi, **J. Kang**, T. Koguchi, T. Amemiya, N. Nishiyama, and S Arai, "Signal Transmission Characteristics through an Athermal Mach-Zhender Interferometer by Si-Slot Waveguide Embedded with Benzocyclobuten", *The 2011 IEICE Society Conference*, C-3-49, Sapporo, Sep. 2011.

13. M. Oda, Y. Atsumi, T. Sifer, **J. Kang**, T. Amemiya, N. Nishiyama, and S Arai, "Wavelength Drop Filter by Athermal Si-Slot Ring Resonator Embedded with Benzocyclobutene", *The 2012 IEICE General Conference*, C-3-39, Okayama, Mar. 2012.

14. E. Murai, T. Amemiya, T. Shindo, **J. Kang**, S. Myoga, N. Nishiyama, and S. Arai, "InP-based Plasmonic Waveguide with Side Metal Layer for Tight Confinement", *The 2012 IEICE General Conference*, C-3-91, Okayama, Mar. 2012.

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16. Y. Hayashi, R. Osabe, K. Fukuda, Y. Atsumi, **J. Kang**, N. Nishiyama, and S. Arai, "A GaInAsP/Si Hybrid Fabry-Perot Laser Using Activated Bonding", The 73th Fall Meeting, 2012; *The Japan Society of Applied Physics and Related Societies*, 12a-C6-8, Ehime, Sep. 2012.

17. T. Sifer, Y. Atsumi, M. Oda, **J. Kang**, N. Nishiyama, and S. Arai, "UV exposure wavelength trimming of an athermal Si slot ring resonator", T*he 73th Fall Meeting, 2012; The Japan Society of Applied Physics and Related Societies*, 12p-C5-17, Ehime, Sep. 2012.

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19. E. Murai, T. Amemiya, T. Shindo, **J. Kang**, S. Myoga, N. Nishiyama, and S. Arai, "Bending Properties of InP-based Plasmonic Waveguide with Side Metal Layer", *The 73th Fall Meeting, 2012; The Japan Society of Applied Physics and Related Societies*, 13p-C5-14, Ehime, Sep. 2012.

20. T. Amemiya, T. Kanazawa, A. Ishikawa, S. Myoga, E. Murai, T. Shido, **J. Kang**, N. Nishiyama, Y. Miyamoto, T. Tanaka, and S. Arai, "Optical Waveguide Analysis with Nano-scale Metal Structure", *The 60th Spring Meeting, 2013; The Japan Society of Applied Physics and Related Societies*, 29-B3-14, Kanagawa, Mar. 2013.

21. J. Suzuki, Y. Hayashi, Y. Atsumi, **J. Kang**, N. Nishiyama, and S. Arai, "Influence of High Temperature Process to GaInAsP/SOI Hybrid Laser Structure with AlInAs Oxidation Current Confinement Layer," *The 74th Fall Meeting, 2013; The Japan Society of Applied Physics and Related Societies*, 19a-P2-1, Kyoto, Sep. 2013.

22. Y. Atsumi, **J. Kang**, Y. Hayashi, J. Suzuki, N. Nishiyama, and S. Arai, "Evaluation of Humidity Protection for Athremal Si-Slot Wavelength Filters Embedded with Polymer", *The 2013 IEICE Society Conference*, C-3-11, Fukuoka, Sep. 2013.

23. Z. Gu, T. Amemiya, A. Ishikawa, J. Suzuki, E. Murai, **J. Kang**, T. Hiratani, N. Nishiyama, T. Tanaka, and S. Arai, "Analysis of Transmission Characteristics between Si chips with Photonic Wire Bonding," *The 61th Spring Meeting, 2014; The Japan Society of Applied Physics and Related Societies*, (to be presented) Kanagawa, Mar. 2014.

24. Y. Kuno, **J. Kang**, Y. Atsumi, Y. Hayashi, J. Suzuki, T. Amemiya, N. Nishiyama, and S. Arai, "Apodized Grating Couplers between Si Multilayer Waveguides with Metal Mirrors," *The 2014 IEICE General Conference*, C-3-12, Niigata, Mar. 2014.

25. J. Suzuki, Y. Hayashi, Y. Kuno, **J. Kang**, T. Amemiya, N. Nishiyama, and S. Arai, "Investigation of Etching Process of III-V Layer toward III-V/SOI Hybrid Devices By using Plasma Activated Bonding," *The 75th Fall Meeting, 2014; The Japan Society of Applied Physics and Related Societies*, 18a-A18-3, Sapporo, Sep. 2014.

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27. K. Miura, T. Hirasawa, **J. Kang**, Y. Shoji, Y. Okada, H. Yokoi, N. Nishiyama, S. Arai, and T. Mizumoto "a-Si:H Waveguide Optical Isolator on Magneto-Optical Crystal," *The 75th Fall Meeting, 2014; The Japan Society of Applied Physics and Related Societies*, 18a-A18-7, Sapporo, Sep. 2014.

28. Y. Kuno, **J. Kang**, Y. Atsumi, Y. Hayashi, J. Suzuki, T. Amemiya, N. Nishiyama, and S. Arai, "Apodized Grating Couplers between Si Multilayer Waveguides with Metal Mirrors," *The 2014 IEICE Society Conference*, C-3-50, Tokushima, Sep. 2014.

29. (Invited) T. Amemiya, T. Kanazawa, A. Ishikawa, **J. Kang**, Z. Gu, N. Nishiyama, Y. Miyamoto, T. Tanaka, and S. Arai, "Metamaterial-loaded Optical Modulator by the Control of "Permeability"," *The 2014 IEICE Society Conference*, C-4-12, Tokushima, Sep. 2014.

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31. Y. Hayashi, J. Suzuki, S. Inoue, **J. Kang**, Y. Kuno, T. Amemiya, N. Nishiyama, and S. Arai, "GaInAsP/SOI Hybrid Laser with Ring-resonator-type Reflector Fabricated by Plasma Activated Bonding," *The 2014 IEICE Society Conference*, C-4-15, Tokushima, Sep. 2014.