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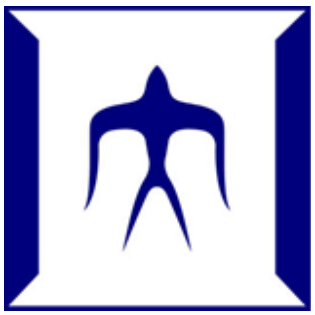

Reliability-Enhanced Low-Power High-Data-Rate 60-GHz Transceivers in CMOS Technologies

by

Rui Wu

A Ph. D. dissertaion submitted in partial satisfaction of the requirements for the degree of

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in

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of

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Supervised by

Prof. Kenichi Okada and Prof. Akira Matsuzawa

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To my parents,

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Abstract

This dissertation presents a study of reliability enhancement and power reduction solutions for 60-GHz high-data-rate transceivers in CMOS technologies.

Starting from the discussion for the key requirements of wireless transceivers in future radio access network, it shows that 60-GHz CMOS transceiver would be one of the most promising candidates with some significant challenges ahead such as hot-carrier-injection (HCI) reliability issues and low power consumption requirement.

To address the HCI issues for 60-GHz applications, a transistor-level study of HCI physical mechanism and lifetime characterization methods under DC and RF stress have been conducted. Based on the acquired knowledge, the reliability model of transistors under AC-mode HCI stress is derived to provide a valuable solution of HCI damage alleviation by limiting the operation period of high output power condition.

The proposed solution, which is realized by using variable-supply-voltage, provides a way to output superior power with high linearity and efficiency in a carefully restricted time period while satisfying the lifetime requirement. The lifetime of the implemented example PA can be improved to over 10 years with the careful arrangement of various operation supply voltages. On the other hand, the power amplifier is still able to provide 13.2 dBm saturation power, 10.2 dBm power at 1-dB compression point and 15.0% peak power-added efficiency at 60 GHz for high supply voltage (V_{PA} = 1.0 V).

Furthermore, based on the research of HCI damage mechanism, a 60-GHz CMOS transceiver with HCI damage healing function is realized by using charge ejection technique, which guarantees longer operation lifetime with high output power. The HCI-healing technique introduced in this dissertation further relieves the trade-off between the HCI reliability and the system performance. The implemented transceiver using the proposed HCI-healing technique achieves over 81-year lifetime without sacrificing the output power and efficiency. The transceiver demonstrates an output power of 9.3 dBm at TX EVM = -21 dB and 3.9% TX efficiency.

For the power consumption reduction of the 60-GHz CMOS transceiver, it is known that the wake-up receiver is one of the most applicable choices to systematically reduce the power consumption over time. Conventional wake-up receivers using either the 60-

GHz band or lower frequency bands share the same issue of needing bulky components, which significantly increases the chip area and implementation cost. By reusing the 60-GHz LNA gain stages, the proposed 60-GHz wake-up receiver in this dissertation occupies an area overhead of only 0.015 mm^2 and does not need extra antennas or switches to be integrated with the 60-GHz multi-Gb/s transceiver.

Besides reducing the time-averaged power consumption of the 60-GHz transceiver by the duty cycle control scheme, The energy efficiency potential of the 60-GHz high-data-rate transmitter is explored in this dissertation. The 60-GHz CMOS transmitter adopting the simple modulation schemes is designed and implemented using wideband and power-saving techniques, which guarantees the low-power and high-data-rate characteristic (high energy efficiency). An energy efficiency of 3.4 pJ/bit is achieved in BPSK with the 3-dB bandwidth of 9 GHz. The data rate (5 Gb/s) is mainly limited by the maximum sampling frequency of the AWG and the insufficient local oscillator signal power.

At last, this dissertation is concluded with the insight that the combination of the proposed techniques and solutions in this research can help to achieve the reliable low-power high-data-rate 60-GHz transceivers in CMOS processes. Future researches are also discussed in the end of this dissertation.

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Chapter 1

Introduction

In the not far future, we will enter a society, in which anything that benefits from a connection will be connected. It is so called the networked society. This society will has two prominent characteristics: the exponential growth in the traffic volume and massive growth in connected devices, as shown in Fig. 1.1. Those characteristics raise the requirements for future radio access network, which include a) the capability of supporting data traffic explosion (*e.g.* 1000 × capacity/km^2); b) the increase of quality of experience (QoE) for various applications (*e.g.* 10-100× data rates, reduced latency, and terminal battery saving); c) massive device connectivity (*e.g.* 100× connected devices); d) intelligent network with low cost and high robustness (*e.g.* suitable for diverse environment). Therefore the key requirements for wireless transceivers in the future will be high data rate, low cost, high robustness, and low power consumption.

So what are the solutions for those requirements? With the evolution of communication technologies, wireline communications can achieve hundreds of gigabits per second (Gb/s) data rate nowadays [1–4]. While the data rate of wireless communications

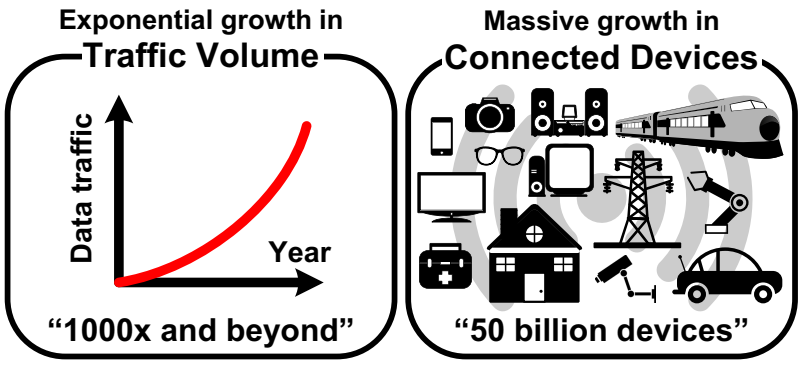


Figure 1.1: The networked society.

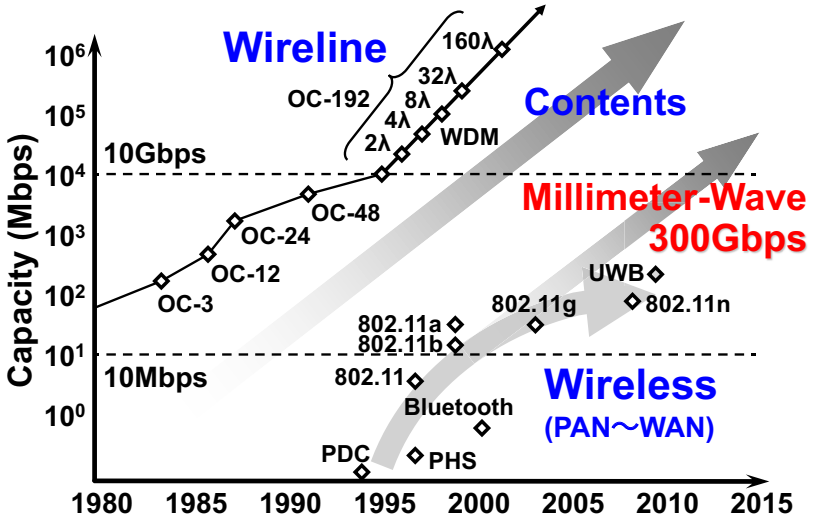


Figure 1.2: The conceptual trend of communication data rate.

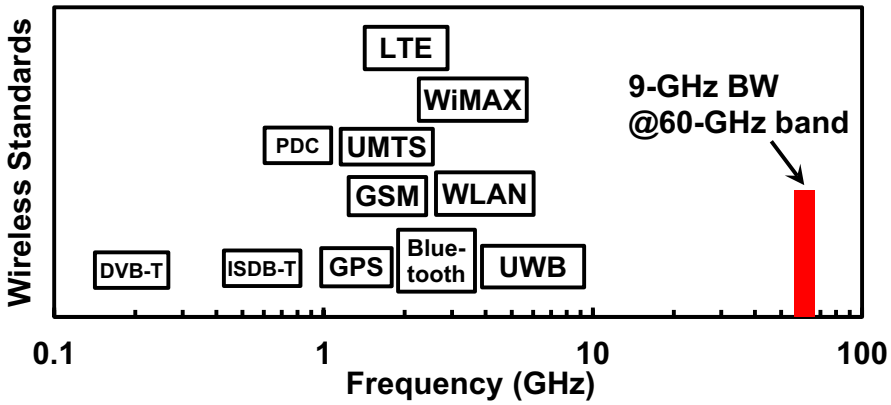


Figure 1.3: The wireless standards at different frequency bands.

using low frequency bands, such as 2.4-GHz band and 5-GHz band, seems to be saturated around hundreds of megabits per second (Mb/s) [5–7], as depicted in Fig. 1.2. One of the most important reasons is due to the crowded frequency band at low frequencies (frequencies below 10 GHz), which limits the possible bandwidth for the multi-Gb/s wireless communication, as illustrated in Fig. 1.3. Fortunately, millimeter-wave (mmW) band, which has much less standards and wider available frequency bands, is one of the most promising candidates for high-data-rate (multi-Gb/s) wireless communications. Especially, it is predicted that 60-GHz band as the beginning of a trend of escalating carrier frequencies has the potential of delivering unprecedented data rates [8–11], which allows uncompressed high-definition media transfers, sensing and radar applications, and virtually instantaneous access to massive libraries of information. Moreover, advances

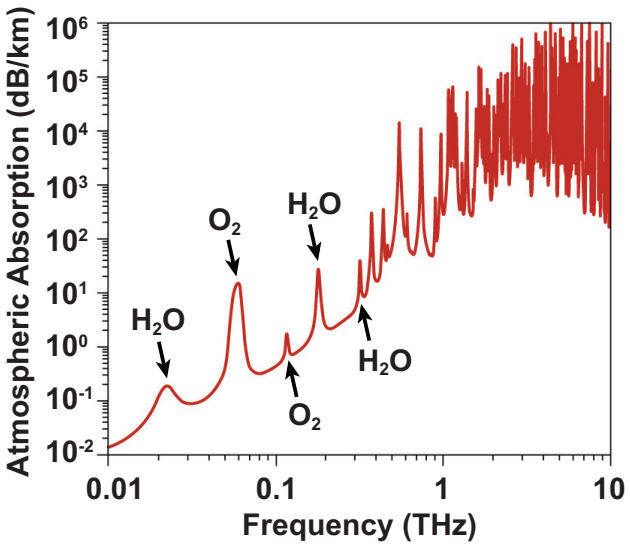


Figure 1.4: The attenuation across the electromagnetic spectrum at sea level for standard atmosphere (7.5 gm/m^3 water vapor) and 20 °C.

in complementary metal-oxide-semiconductor (CMOS) processes allow for the low-cost low-power implementation of the 60-GHz transceiver system on a chip (SoC) [12–15]. In addition, antenna size scales with frequency and becomes much smaller at 60-GHz band enabling full on-chip integration, which can improve the design flexibility and reduce the parasitic components and cost. Today, we are at the dawn of a new age of massively broadband devices fabricated in CMOS processes, which operate at carrier frequencies around 60 GHz.

1.1 60-GHz Frequency Band

1.1.1 Millimeter-Wave Propagation

The radio propagation channel must be understood for proper design and deployment of wireless communication devices at 60 GHz. The laws of physics say that the higher the frequency, the shorter the transmission range for a given power. It is known that the free space path loss (FSPL) is more severe at 60-GHz band than at lower frequency band according to the equation shown below (*e.g.* 20 dB larger loss due to the order of magnitude increase in carrier frequency).

$$\text{FSPL (dB)} = 20\log_{10}(d) + 20\log_{10}(f) + 20\log_{10}(\frac{4\pi}{c}) \tag{1.1}$$

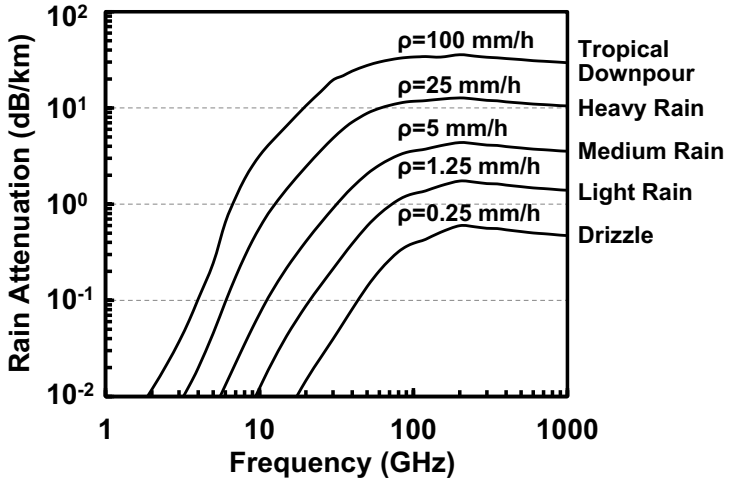


Figure 1.5: The predicted rain attenuation based on LP distribution for different rainfall rates (ρ) at 20 °C.

Table 1.1: Partition Losses (Loss in Excess of Free Space) at 60 GHz in a Building of Virginia Tech

Material	Drywall	Office Whiteboard	Clear Glass	Mesh Glass	Clutter
Average Measured Attenuation (dB)	6.0	9.6	3.6	10.2	1.2
Measurement Standard Deviation (dB)	3.4	1.3	2.2	2.1	1.8
Normalized Average Attenuation (dB/cm)	2.4	5.0	11.3	31.9	–

where d is the propagation distance in meters. f is the signal frequency in hertz. $c \approx 3 \times 10^8$ is the speed of the electromagnetic wave in air. For example, the loss with 10-meter distance at 60 GHz is 88 dB, while it is 68 dB at 6 GHz.

Furthermore, the atmosphere absorbs millimeter waves, restricting their range. Oxygen (O_2) absorption is especially large at 60 GHz as shown in Fig. 1.4 [16]. The oxygen in the air attenuates the 60-GHz electromagnetic wave at a rate close to 20 dB/km. By comparison, the atmospheric absorption in sub-6GHz bands encounters less than 0.01-dB/km attenuation. Rain, fog, and any moisture in the air make millimeter-wave signal attenuation very high. The interaction between water drops and radio waves cause an attenuation which depends on the size and shape of the water drops. Fig. 1.5 shows the predicted values of rain attenuation based on Laws and Parsons (LP) distribution at 20 °C [17]. The specific rain attenuation at 60 GHz for a rainfall rate of 25 mm/h (heavy rain) is about 10 dB/km.

In addition, common building materials have even higher loss at 60 GHz according to C. Anderson *et al.* [18]. Table 1.1 from literature [18] shows the measured partition losses (loss in excess of free space) at 60 GHz for different building materials.

Although high attenuation is undesirable in communication systems seeking for long range, communications over short distances can benefit from it. For example, the high attenuation cuts down on interference from other nearby radios. Therefore, a more efficient way of using the allocated spectrum (space division multiplexing) can be achieved. Moreover, the high-gain antennas, which are normally used to compensate the path loss, are highly directional. Those antennas can mitigate the interference and provide security that prevents signals from being intercepted. Another consequence is a less harsh multi-path environment compared to lower frequencies because of the high attenuation.

1.1.2 Regulations and Standards for 60-GHz Wireless Communications

Knowing the attractive features of the 60-GHz band, the governments across the world have been making efforts to facilitate the commercialization of the 60-GHz spectrum. In 2001, the Federal Communications Commission (FCC) allocated 7 GHz of a continuous spectrum (from 57 GHz to 64 GHz) for unlicensed wireless communications in USA [19]. Canada regulations, enforced by Industry Canada Spectrum Management and Telecommunications (IC-SMT), are harmonized with those of the USA [20].

In 2000, the Ministry of Public Management, Home Affairs, Posts and Telecommunications of Japan issued 60 GHz radio regulations for unlicensed uses in 59 GHz–66 GHz. The available 60-GHz bandwidth is extended to 9 GHz (57 GHz–66 GHz) later [21].

Australia followed the international trend and regulated 60-GHz band (59.4 GHz–62.9 GHz) in 2005.

In 2009, the European Commission (EC) amended a prior decision on the harmonization of the radio spectrum for use by short range devices [22]. It puts into force the harmonized European standard ESTI EN 302 567 which allocates the 9 GHz frequency band from 57 GHz to 66 GHz for unlicensed use all over the European Union.

Fig. 1.6 summarizes the regulations of the 60-GHz band in the regions mentioned above. It can be observed that a maximum of 9-GHz unlicensed bandwidth is available around 60 GHz for short-range high-data-rate wireless communications.

Besides the efforts from the governments, there are many standardization and commercialization efforts underway by the engineering community for 60-GHz wireless personal/local area network (WPAN and WLAN). Several 60 GHz standards, including IEEE 802.15.3c [23], IEEE 802.11ad [24], WiGig [25], WirelessHD [26,27], and ECMA 387 [28],

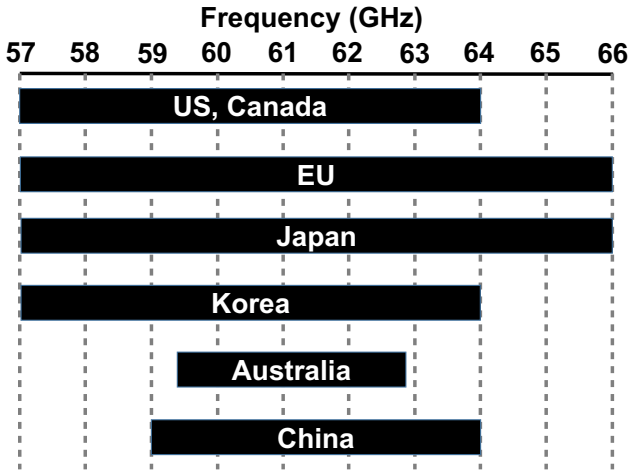


Figure 1.6: The regulations of the 60-GHz band in the selected regions.

are all targeting short-range 60-GHz networks.

The IEEE 802.15.3c mmW standard is an amendment to the IEEE 802.15.3 standard. The IEEE 802.15.3c standard supports data rates in excess of 5 Gb/s, beamforming to improve range, data aggregation schemes to improve medium-access layer (MAC) efficiency, and subpacket acknowledgement to reduce retransmission overhead. Three physical layer (PHY) modes are used in the IEEE 802.15.3c standard: single-carrier (SC) mode for low power and complexity, high-speed interface mode using OFDM for low-latency bidirectional data transfer, and an audio/video mode for uncompressed HD audio and video streaming. As spectrum allocation is inconsistent internationally, a very important point within the PHY layer description is the definition of communication channels that represent a good compromise between the different regional regulations. The channels defined in the IEEE 802.15.3c standard is given in Fig. 1.7 and Table 1.2. It can be seen that the 60-GH band is divided into four channels with the Nyquist bandwidth (BW) of 1.76 GHz for each channel. The carrier frequencies of neighboring channels are separated by 2.16 GHz. Depending on the regional frequency allocation, only a part of these channels can be used. It is also worthy of knowing that the other standards introduced in the following are either inspired by IEEE 802.15.3c, or exhibit similar properties. In particular, the channel frequencies are the same for all published specifications and all MAC layers implement beam steering.

In order to provide the industry support and an easy marketing name, the wireless gigabit (WiGig) alliance has worked closely with the IEEE 802.11ad technical group on developing the standards. Therefore, the WiGig MAC/PHY specification aligns with the 802.11ad standard. It supplements the IEEE 802.11 MAC layer and is backward compatible to the IEEE 802.11 standard. The PHY layer is supporting both low power

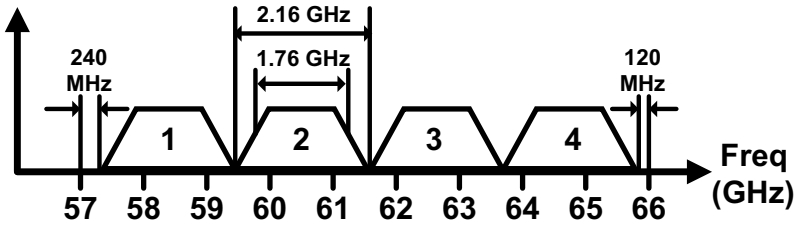


Figure 1.7: The four channels defined by the IEEE 802.15.3c standard.

Table 1.2: Channel definitions in IEEE 802.15.3c standard

Channel Number	Low Freq. (GHz)	Center Freq. (GHz)	High Freq. (GHz)	Nyquist BW (GHz)	Roll-Off Factor
1	57.24	58.32	59.40	1.76	0.25
2	59.40	60.48	61.56	1.76	0.25
3	61.56	62.64	63.72	1.76	0.25
4	63.72	64.80	65.88	1.76	0.25

and high performance devices, while data transmission modes is up to 7 Gb/s. Distance in excess of 10 m are expected due to the use of highly directive antennas and beam forming.

The WirelessHD standard is focused on the delivery of high quality, uncompressed audio/video content with data rates up to 28 Gb/s. A range of at least 10 m is achieved by employing highly directive smart antenna technology and exploiting Non Line of Sight (NLOS) communication.

The ECMA-387 standard is intended to facilitate bulk and streaming data transfer for three device types: (a) high-end video/audio streaming devices for operation over a distance up to 10 m with LOS or NLOS links; (b) economical data/video devices for LOS operation up to 3 m; (c) very inexpensive data-only devices for LOS operation over a 1-m range. The single channel data rate is up to 10 Gb/s. If higher data rate is required, the standard supports channel bonding, which permits the usage of multiple channels in parallel. The standard also provides the framework for high definition media interface protocol adaptation layer (HDMI PAL) in which a 60-GHz wireless device may operate as an intermediate network node between source and sink.

1.1.3 Application Scenarios

The government agreement on spectrum allocation and standardization efforts of the engineering community illuminate a future where today's books and paper media, along with computer hard drives and magnetic media are replaced by the cloud or other large data repositories. Those data sources will be wirelessly accessed by silicon-based electronic devices which are extremely inexpensive to fabricate. Literature [29] shows the anticipated future offices in the next decade, where massively broadband wireless connectivity replaces and transforms traditional paper media and magnetic data storage devices. For example, today's wired Internet port will likely become a tether-less wireless-to-fiber connection. Book and content publishers may become web providers and purchasers of silicon chips or low-cost radio frequency (RF) tags that contain various media content. The carbon footprint and power consumption of Internet data centers will be reduced as low-power wireless chip-to-chip communications replace cables, and permit novel cooling architectures and new flexibility in equipment configuration. Future researchers will have to develop entirely new strategies for circuit implementation, channel coding, data compression, interference mitigation, antenna beamforming, network addressing, and spectral usage to take advantage of massive available bandwidths, lower power requirements of devices, and the ever-present Internet.

1.2 The Effects of CMOS Process Scaling

The mm-Wave front-end shall be integrated together with digital circuitry on the same chip to minimize size and reduce packaging effort and cost. This mandates the use of a CMOS-based technology, which is the only means of efficiently implementing very complex digital circuits. Thus, either CMOS or BiCMOS are potential technologies for the realization of the 60GHz radio interface. Other reasons to favor (Bi)CMOS over competitors like the compound semiconductor technologies such as gallium arsenide (GaAs) and Indium Phosphide (InP) include the potential for low power consumption, small circuit size, low cost in mass production and the transit frequency (f_t)/maximum oscillation frequency (f_{max}) that can be achieved with recent (Bi)CMOS technologies. According to Axiom Microdevices, the cost per unit area of a GaAs process is about 5 times higher that that of a corresponding 0.13 μm CMOS process. Driven by the mass market of digital consumer electronics, the CMOS process keeps scaling down to deep sub-micron. The transit frequency and maximum oscillation frequency of CMOS transistors reach hundreds of gigahertz, which allows the low-cost monolithic-integration of 60-GHz circuitry in the CMOS process, as depicted in Fig. 1.8. Moreover, the supply voltage is scaled

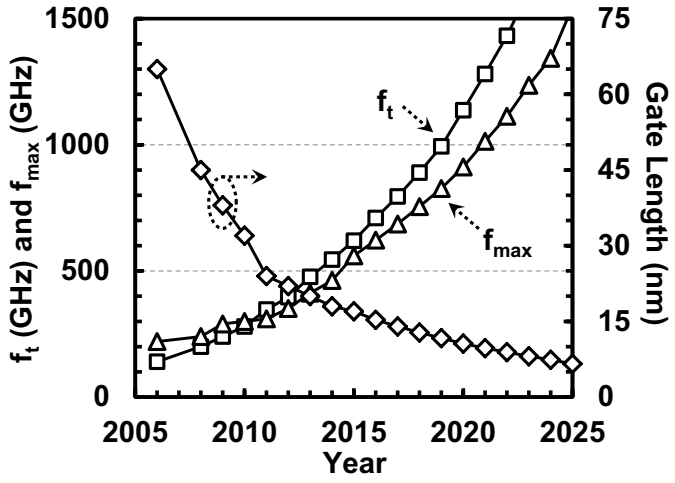


Figure 1.8: Roadmap for CMOS transistor gate length, f_t, and f_{max} according to ITRS 2013 and before.

down with the shrinking of transistor gate length due to reliability considerations, which could lead to order of magnitude of reduction in total power consumption of the system.

When it comes to the choice between CMOS and BiCMOS technology, it has to be noted that both recent CMOS and SiGe BiCMOS technologies exhibit the necessary performance for RFIC design at 60GHz. In the latter case this becomes possible due to the use of powerful bipolar transistors that exhibit much higher unity gain frequencies as the field-effect transistors of the CMOS technology they are implemented in. However, there are different arguments that support the use of standard CMOS instead of BiCMOS technology. First of all, nano-scale CMOS RFICs usually dissipate less power with respect to RFICs of same performance employing bipolar transistors. Secondly, the performance of the CMOS transistors in a BiCMOS process is clearly inferior to the performance of the available bipolar transistors. Thus, while for example a 130nm SiGe BiCMOS process exhibits mm-wave performance comparable to a 65nm CMOS technology, the digital circuitry on the same chip will suffer from lower performance, higher power consumption and larger circuit size. These reasons, and a potential cost advantage if the number of fabricated circuits is very large as in the case of consumer applications, makes CMOS technology the first choice for the 60GHz radio interface.

To allow the design of high performance, low power circuits at 60 GHz, the advanced CMOS technology with smaller gate length is desirable. Because its transistor's cutoff frequencies and maximum oscillation frequency are higher than the desired operating frequency, which offers higher power gain for a single stage. Consequently, the power consumption and circuit size can be reduced because of the decreasing of gain stage numbers. Although many advantages are expected and observed with the CMOS process scaling,

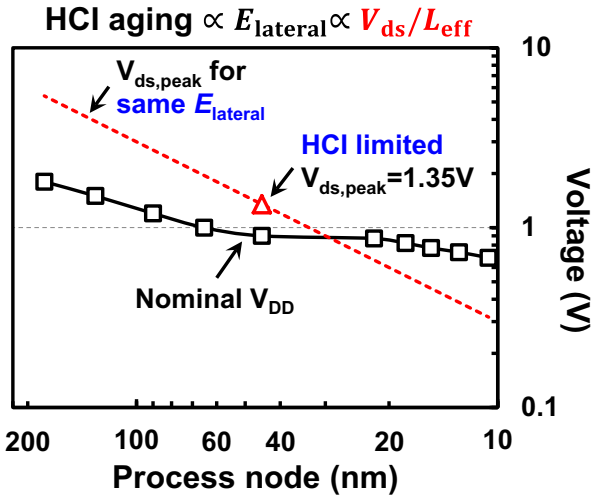


Figure 1.9: HCI issues with the scaling of transistor gate length.

there are new challenges arisen with scaling which need to be addressed and taken into consideration for 60-GHz design.

Firstly, hot-carrier-injection (HCI) reliability issues in the CMOS process become more severe with the downscaling of the transistor gate length. It is because the main source of the HCI damage is the strong lateral electric field built in the transistor channel. With the shrinking of the channel length, the electric field in the channel becomes stronger under a certain bias condition, as demonstrated in Fig. 1.9. The nominal supply voltage is from ITRS 2013 and before. The HCI limited peak drain voltage ($V_{\mathrm{ds,peak}}$) for a 45nm CMOS process is the measured maximum drain voltage for 10-year lifetime when RF stress signal is applied to the drain terminal of the transistor and DC signal is at gate terminal [30]. The DC bias for the drain and source of the transistor are 1.0 V for the measurement. The red dashed line indicates the estimated drain voltage values for same peak electric field at different process node. Although the estimation is under extreme conditions and the electric field also depends on other parameters such as doping levels and junction profiles. This figure shows the trend that HCI issues become more sever with the rapid scaling of the gate length and the slow decreasing of the supply voltage due to the non-scalability of the sub-threshold slope. It is also give us a insight that the process node smaller than 30 nm may not be suitable for RF applications due to the strongly increased lateral electric field. Furthermore, the reduction of the supply voltage and output voltage swing due to reliability issues will cause the degradation of output power or efficiency. The degradation of output power ($P = V \times I$) is straight-forward. With the decreasing of the output voltage swing, the output power is decreased with the same current value. If the current value is increased to maintain the output power, the optimum load impedance for

maximum output power ($Z = V/I$) is decreased accordingly. This will raise the impedance transformation ratio in the output matching network, which causes large loss in the matching network. Therefore, the system output power and efficiency are degraded. The HCI effects are dominant for the reliability of the standard CMOS transistors in large-signal operation mode, which are generally used to realize power amplifiers (PAs). The detailed researches and solutions for HCI issues in the design of 60-GHz transceivers is elaborated in the following chapters of this dissertation.

Secondly, the low-gain and low-efficiency issues of CMOS on-chip antennas are exacerbated in the advanced CMOS process. The low gain and low efficiency of the CMOS on-chip antenna is mainly originated from the high doping concentration (low resistivity) of the substrate which is used to avoid latch-up of digital components. The doping concentration is getting higher in the advanced CMOS process, which is generally used to implement 60-GHz transceivers. However, if high gain antennas can be fabricated on chip in 60-GHz band, the benefits of cost reduction and improved design flexibility will be extremely attractive. The researches with regard to gain enhancement of the CMOS on-chip antenna is discussed in detail in the following chapters.

Last but not least, the supply voltage scaling reduces the signal swing and degrades signal to noise ratio (SNR) of analog circuits. Moreover, the phase noise of oscillators is degraded by supply voltage reduction which negatively affect system performance.

1.3 Challenges for 60-GHz CMOS Transceiver Design

Considering the implementation of the 60-GHz CMOS transceivers for the short-range wireless communication, high-data-rate capability, low cost (and hence small circuit size), high reliability, very low power consumption, and high integrability are the key requirements. To achieve those requirements, new challenges are introduced consequently.

It is well-known that the parasitics have large effect on the device performance at 60-GHz frequencies. Unfortunately, foundries do not yet provide process design kits (PDKs) supporting 60-GHz frequencies. Therefore, device modeling for 60-GHz circuit design is indispensable. To accurately model the devices, test elementary group (TEG) of passive and active devices including pads and interconnects have to be implemented before circuit design [31,32]. De-embedding is needed to correctly obtain the performance of the device removing the effects of extra text fixtures [33].

The maximum available gain (MAG) of the transistor is inversely proportional to the operation frequency. More stages and power consumption are demanded to reach a certain gain value at 60 GHz than at low frequencies. Customized transistor layout and new circuit design techniques are necessary to improve the gain of the 60-GHz amplifier with

low power consumption [34].

Low complexity of the transceiver topology is desired to decrease the circuit size and power consumption, which normally means low spectrum usage efficiency. However, to achieve very high data-rates (severl tens of Gb/s or even higher), the spectrum needs to be used efficiently even though ultra-wide bandwidth is available in the 60-GHz band. Trade-offs between the system complexity and achievable data rate are required to be examined carefully for specific applications.

Besides high-gain antennas/antenna arrays and power combining technique, high output power for a single power amplifier is desired to overcome the considerably high path loss at 60-GHz band. However, the deteriorated HCI reliability performance of the advanced CMOS transistor degrades the output power of the 60-GHz power amplifier, and therefore the operation lifetime. New techniques and solutions are required to achieve longer operation lifetime of the 60-GHz transmitter with high output power.

The ultra-wideband (around 9 GHz) requirement of 60-GHz transceivers makes the low-power implementation of the wideband wireless system challenging. It is difficult to maintain the gain flatness over a wide bandwidth across the front-end, which is important for the error vector magnitude (EVM) performance. The wideband RF/analog wireless signals generally need to be converted to the digital domain by high-speed analog-to-digital converter (ADC), which is not easy to be achieved with low power consumption for moderate-resolution ADCs (6–10 bit).

The quality factor of circuit components (especially varactors) drops enormously at 60-GHz band, which leads to the difficulties of direct generation of low phase noise 60-GHz local oscillator (LO) signal. Therefore, traditional design techniques becomes difficult to implement the required low phase noise LO with low power consumption. Different approaches are needed to overcome this issue.

1.4 Overview of This Thesis

This thesis focuses on the research of HCI reliability enhancement and power reduction solutions for 60-GHz multi-Gb/s short-range transceivers in CMOS processes, which are key challenges/requirements for wireless transceivers in future radio access network. It is also worthy of noting that the solutions and techniques developed in this research can be easily merged with each others. Therefore, high reliability and low power consumption characteristics can be achieved simultaneously for the 60-GHz high-data-rate CMOS transceiver.

The thesis is organized as shown in Fig. 1.10. In the beginning, the HCI phenomena and issues in the CMOS process are briefly reviewed in Chapter 2. Then, the aging

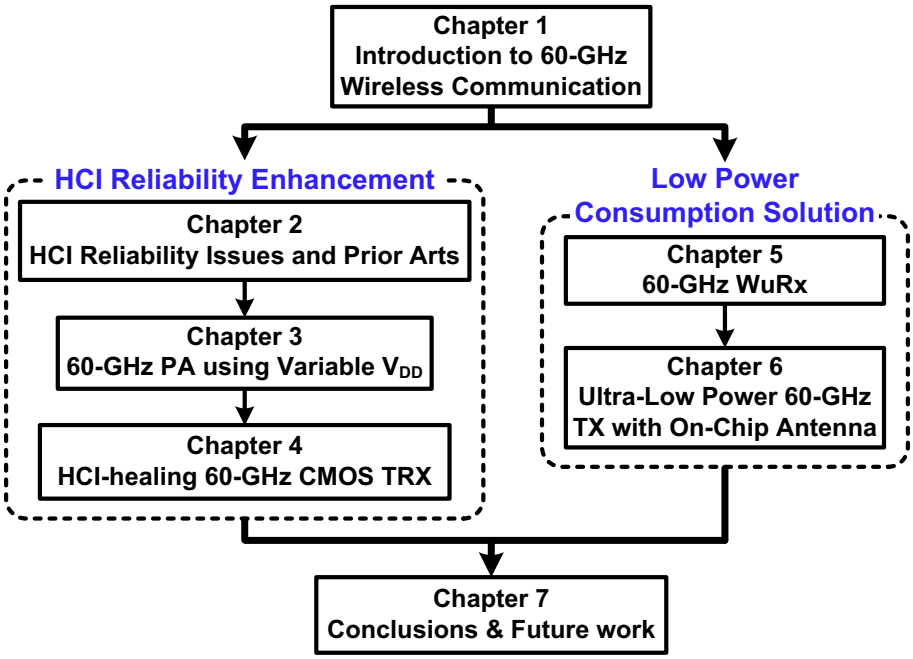


Figure 1.10: Organization of this dissertation

model for AC stress on the transistor is detailed and extended to the dynamic operation situation. Chapter 3 explains the proposed variable-supply-voltage PA for the 60-GHz application, which alleviates the HCI damage and therefore improves the reliability. To further enhance the HCI reliability, a HCI-healing 60-GHz CMOS transceiver is designed and implemented, which is described in Chapter 4. Chapter 5 introduces a systematic and area-efficient power reduction solution using 60-GHz wake-up receiver (WuRx) for the 60-GHz multi-Gb/s transceiver. The design of a ultra-low power 60-GHz transmitter with a gain-enhanced on-chip antenna is elaborated in Chapter 6. Finally, the conclusions are drawn for this thesis in Chapter 7. Future works are also discussed for possible improvements to the research.

Chapter 2

Hot-Carrier-Injection Reliability Issues in CMOS Transistors

It is known that the physical phenomena mostly responsible for the advanced CMOS transistor degradation are hot carrier injection (HCI), negative bias temperature instability (NBTI), and gate oxide breakdown [35]. NBTI, which is prominent in PMOS devices, occurs due to the generation of the interface traps at the Si/SiO_2 interface when a negative gate bias is applied to the PMOS [36]. It manifests itself as a degradation in the threshold voltage (V_{th}) of the PMOS transistor. Because of the low gain property of the PMOS transistor at the 60-GHz frequencies, the NMOS transistor is widely used for the circuit design and implementation. Therefore, the degradation caused by NBTI is not investigated thoroughly in this thesis. The gate oxide breakdown is the sudden formation of a

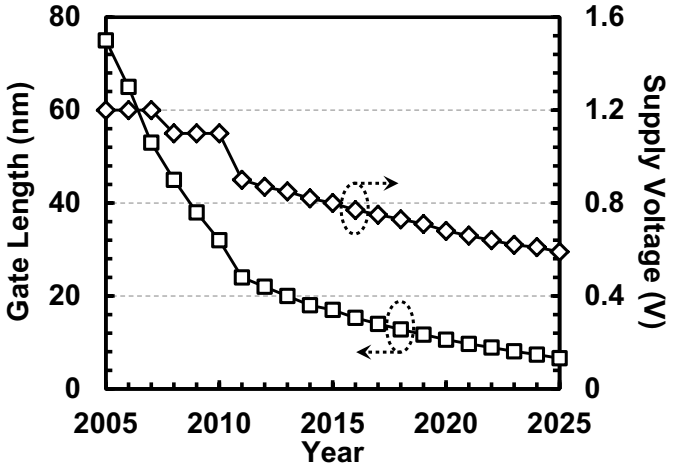


Figure 2.1: The downscaling of the the supply voltage and gate length for RF/AMS CMOS processes according to ITRS2013 and before.

conductive path in the gate-oxide of a MOS device as result of a high gate voltage. The typical electric field value for gate oxide breakdown due to Fowler-Nordheim tunneling is around 10 MV/cm [37]. This corresponds to approximately 2.5-V gate voltage for the gate oxide thickness of 2.5 nm used in a normal 65-nm CMOS process, which is far larger than the normal operation voltage for the 60-GHz circuits. Hence, this research does not focus on the reliability issue induced by gate oxide breakdown. However, the HCI issues, which are induced by the high electric field across the channel of the MOSFET, are becoming a major concern for the high-frequency applications with the MOS channel length downscaling. It can be observed through the trend of the downscaling of the supply voltage (V_{DD}) and gate length (L) as depicted in Fig. 2.1. The downscaling of the supply voltage is not as fast as the shrinking of the gate length. The ratio of V_{DD}/L is actually increasing with the process downscaling, which indicates a stronger lateral electric field in the channel and degrades the HCI reliability performance.

2.1 Hot-Carrier-Injection Phenomenon

The hot-carrier phenomenon appears when a large voltage drop across the pinch-off region of the MOSFET results in a high lateral electric field close to the drain terminal. The carriers which traverse this high electric field and gain considerably higher energies than the equilibrium thermal energy in the semiconductor lattice are so-called hot carriers. Under the influence of the lateral field effect, a fraction of those hot carriers interacts with the interfacial layer enabling a transfer of energy. Several mechanisms [38] can explain such interactions. Some of the most important mechanisms are listed here and illustrated in Fig. 2.2.

(a) channel hot-electron (CHE) injection, which is composed of ”lucky electrons” and occurs mainly at $V_D = V_G$ conditions. Lucky electrons are those which gain sufficient energy to surmount the barrier between Si and SiO_2 without suffering an energy-losing collision in the channel. Those hot electrons are injected into the gate oxide, producing a small gate current (I_G)

(b) drain avalanche hot-carrier (DAHC) injection, which is due to impact ionization of channel current near the drain. In this mode, some hot carriers in the channel cause impact ionization, thereby generating a new electron hole pair. As a consequence some holes may flow towards the substrate contact, thereby contributing to a measurable substrate current (I_{sub}). The maximum I_{sub} normally occurs around $V_G = V_D/2$ condition. Both of the hot electrons and hot holes can be injected into gate oxide causing small gate current and generating defects. The carriers injected in the gate oxide can either contribute to the gate leakage current or generate defects by Si-H bond dissociation in a region closed

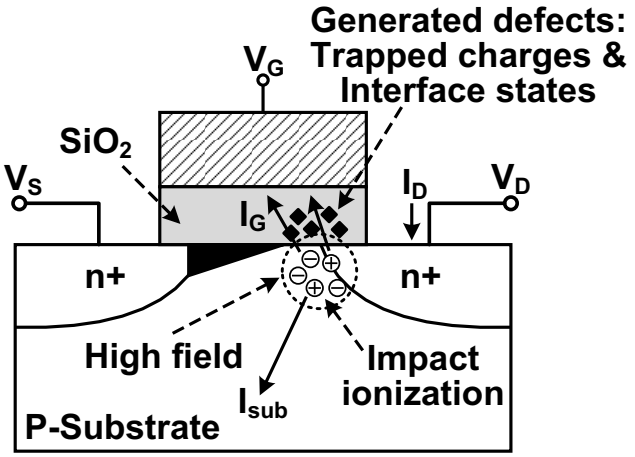


Figure 2.2: The hot-carrier injection mechanism.

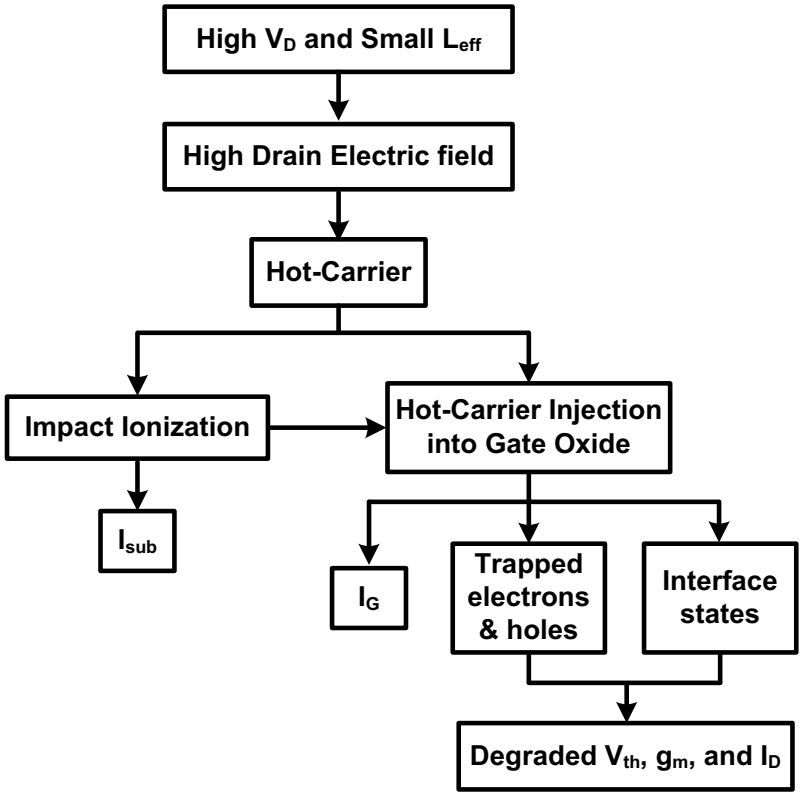


Figure 2.3: Summary of hot-carrier generation and degradation in MOSFETs.

to the gate/oxide interfacial layer. Several types of bonds excitations can occur depending on the energy (voltage) and the flow (current) of carriers. Three main bonds excitations are highlighted in [39].

(a) Single Vibrational Excitation (SVE) is related to higher energetic carrier that has

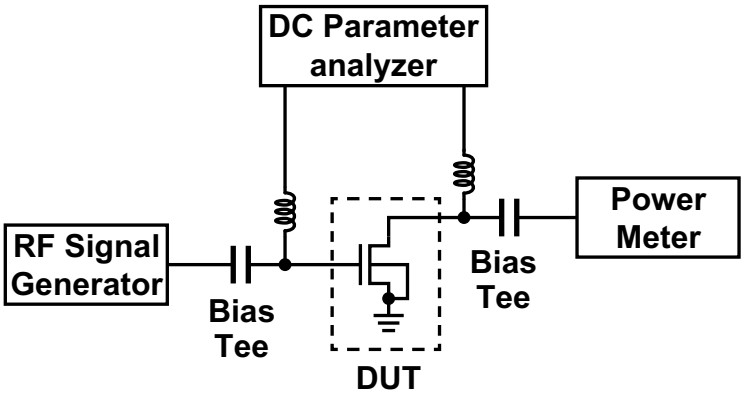


Figure 2.4: Transistor lifetime measurement setup.

enough energy to break Si-H bond. (high energy)

(b) Electron Electron Scattering (EES) is due to energy exchange between two carriers. One carrier promotes the other into higher energy and allows Si-H breaking. (medium energy)

(c) Multiple Vibrational Excitation (MVE) is due to a series of low energetic carriers that accumulate enough energy to break Si-H bond. (low energy)

The trapped charges and generated defects will modify the electric field at the Si-SiO_2 interface and hence the electrical characteristics of the MOSFET, such as threshold voltage (V_{th}), channel carrier mobility (μ), unit-area gate oxide capacitance (C_{ox}), and therefore drain current (I_D).

Fig. 2.3 summaries the hot-carrier generation and degradation in MOSFETs.

2.2 The Lifetime Characterization of 65 nm NMOSFETs

To gain quantity insights of the hot-carrier-induced effects on MOSFETs, DC and RF stress lifetime measurements have been conducted using the setup shown in Fig. 2.4. The DC parameter analyzer is used to provide stress voltages for the DC lifetime measurement and bias voltages for the RF lifetime measurement. The RF signal generator is utilized to apply RF stress signal on the Device Under Test (DUT). The power meter and the DC parameter analyzer are used to monitor the RF stress levels and DC parameters, respectively. The lifetime measurement conditions are summarized in Table 2.1.

The DC stress lifetime measurement is performed by the following method [30, 40], as depicted in Fig. 2.5.

Table 2.1: Description of Lifetime Measurement Conditions.

	Stress	Recording
DC lifetime Meas.	DC	DC
RF lifetime Meas.	DC+RF	DC

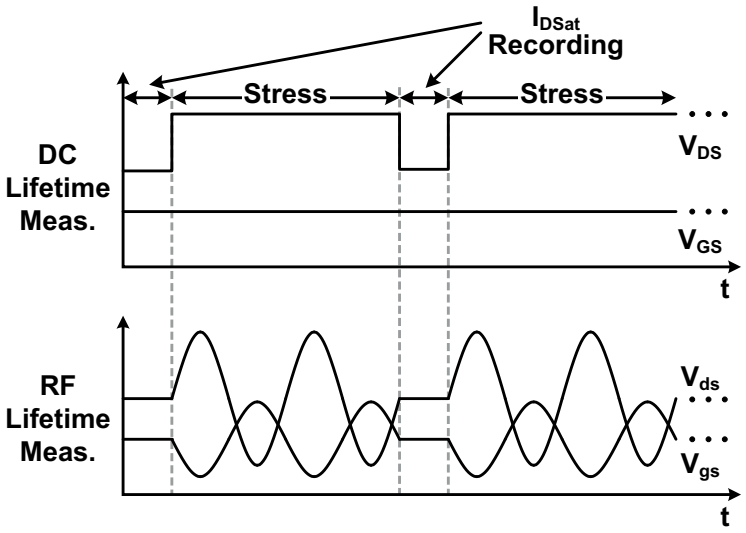


Figure 2.5: Transistor lifetime measurement procedure.

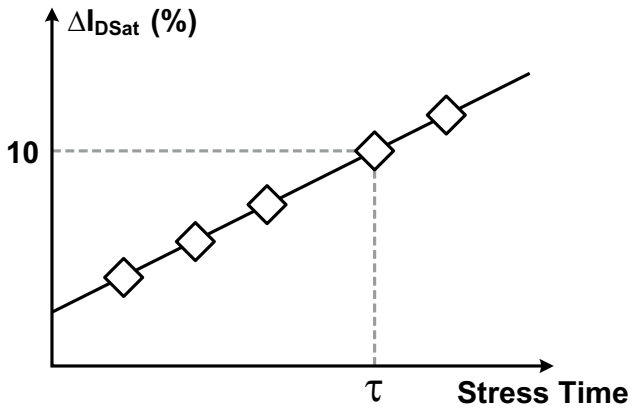


Figure 2.6: The sketch of transistor lifetime (τ) definition with measured (symbol) and estimated (solid line) data.

a) At the beginning of the measurement, the unstressed saturation drain current (I_{DSat}) of the DUT is record under a certain gate and drain bias voltage.

b) Then the drain bias voltage of the DUT is increased to accelerate the occurrence of

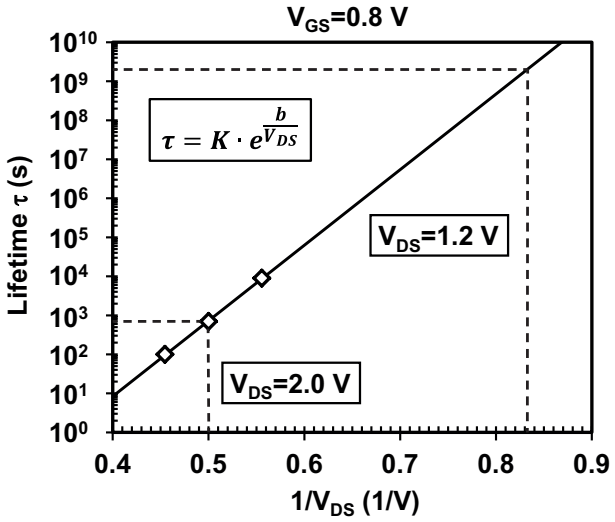


Figure 2.7: Measured (diamond symbol) and estimated (solid line) lifetime of standard 65 nm NMOSFETs versus $1/V_{\mathrm{DS}}$ at $V_{\mathrm{GS}} = 0.8\,\mathrm{V}$.

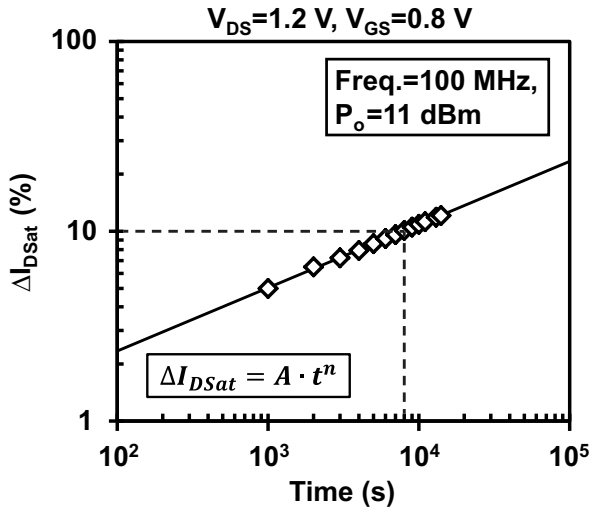


Figure 2.8: Measured (diamond symbol) and estimated (solid line) saturation drain current degradation of standard 65 nm NMOSFETs under RF stress condition of $P_{\mathrm{o}} = 11\,\mathrm{dBm}$, frequency = 100 MHz at $V_{\mathrm{DS}} = 1.2\,\mathrm{V}$, $V_{\mathrm{GS}} = 0.8\,\mathrm{V}$.

HCI effects, which is called stress period.

c) After the stress period, the drain bias voltage of the DUT is decreased to the original value. The degraded I_{DSat} is record accordingly, which is called recording period.

d) The alteration of the stress and recording period is repeated until the lifetime of the DUT is observed or can be predicted by the record data. The lifetime (τ) is generally defined as the time when the record I_{DSat} decreases by 10% from the unstressed value, as illustrated in Fig. 2.6.

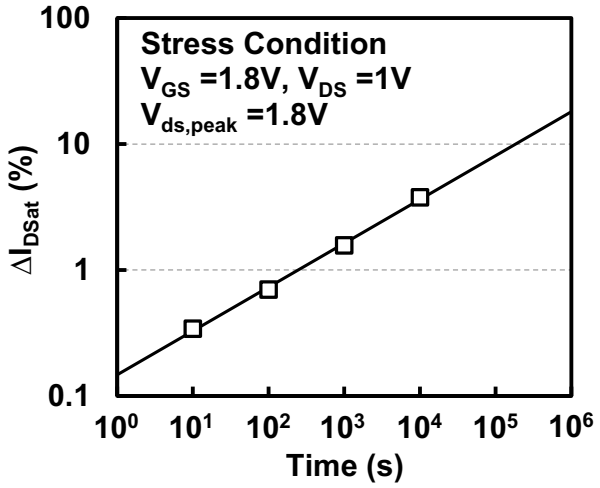


Figure 2.9: Measured (diamond symbol) and estimated (solid line) saturation drain current degradation of standard 40 nm NMOSFETs under RF stress.

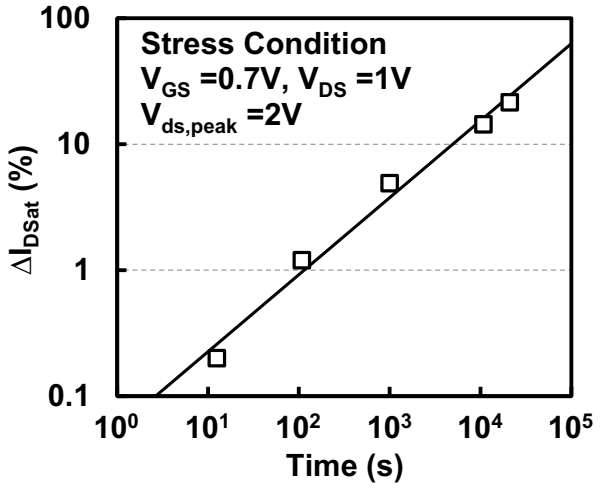


Figure 2.10: Measured (diamond symbol) and estimated (solid line) saturation drain current degradation of standard 45 nm NMOSFETs under RF stress.

The procedure of the RF stress lifetime measurement is similar to the DC one except that the RF signal generator provides a stress signal at the gate of the DUT resulting the stress signal at drain terminal during stress period. In addition, the DC parameter analyzer supplies the same bias voltages for both recording and stress period of the RF lifetime measurement. The waveforms of the RF stress signals are extracted by carefully modeling the transistors and de-embedding the influence of the pads and connection metal lines [33, 41, 42]. Therefore, the relationship between the RF stress lifetime and stress waveforms can be investigated.

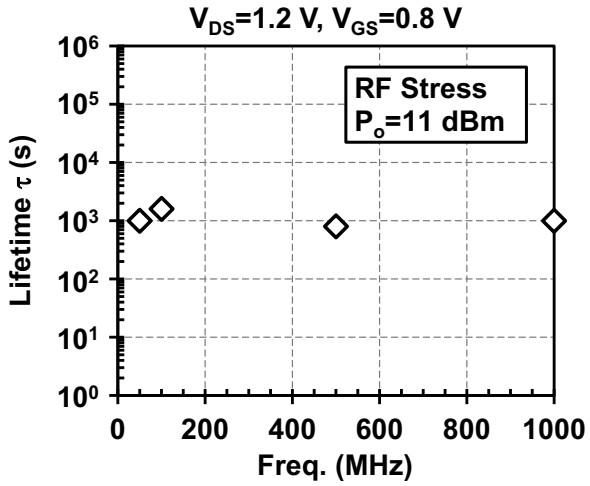


Figure 2.11: Measured lifetime of standard 65 nm NMOSFETs under RF stress condition of $P_o = 11$ dBm for different frequencies at $V_{DS} = 1.2$ V, $V_{GS} = 0.8$ V.

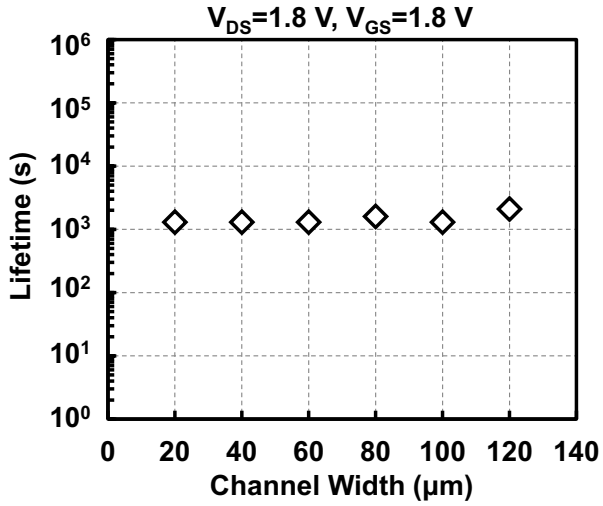


Figure 2.12: Measured lifetime of standard 65 nm NMOSFETs under DC stress condition of $V_{DS} = 1.8$ V, $V_{GS} = 1.8$ V for different channel width .

Fig. 2.7 shows the measured (diamond symbol) lifetime of standard 65 nm NMOSFETs under three different DC stress conditions. The recording bias voltages for the gate and drain terminal of the DUT are 0.8 V and 1.2 V , respectively. As shown in Fig. 2.7, the lifetime is only about 700 s for the stress condition of $V_{DS} = 2.0$ V, $V_{GS} = 0.8$ V. While the estimated lifetime (solid line) can be as long as 2×10^9 s for the stress condition of $V_{DS} = 1.2$ V, $V_{GS} = 0.8$ V. The lifetime estimation result is obtained by finding the best-fitting line for the measurement data using the equation in [43] ($\tau = K \cdot e^{b/V_{DS}}$). It seems that the HCI effects have a small influence on the lifetime of the transistors with

ordinary biases.

Nevertheless, the situation is changed when the RF signals are applied to the transistors. Fig. 2.8 shows the measurement result (diamond symbol) of I_{DSat} degradation when a 100-MHz RF signal is added to the gate of the NMOSFET. The output power at the drain terminal of the NMOSFET (P_{o}) is 11 dBm with the bias condition of $V_{\mathrm{DS}} = 1.2\,\mathrm{V}$, $V_{\mathrm{GS}} = 0.8\,\mathrm{V}$. The corresponding peak drain voltage ($V_{\mathrm{ds,peak}}$) is around 2.2V. The time for I_{DSat} degrading by 10% is vastly decreased to around 8×10^3 s (2.2 hours). The best-fitting line for the measurement data is also constructed to predict the degradation of I_{DSat} in accordance with the equation in [44] ($\Delta I_{DSat} = A \cdot t^n$).

The very short lifetime of the transistor operated with large RF voltage swing at drain terminal is also reported in other literatures [40, 45]. Fig. 2.9 shows the measured saturation drain current degradation of a 40-nm NMOSFET when a RF stress signal is applied to the drain terminal [45]. The stress condition is DC stress at the gate terminal ($V_{\mathrm{GS}} = 1.8\,\mathrm{V}$) and RF stress at the drain terminal ($V_{\mathrm{DS}} = 1\,\mathrm{V}$, $V_{\mathrm{ds,peak}} = 1.8$V, frequency=1 GHz). It is shown that the lifetime for 10% I_{DSat} degradation is about 50.9 hours. When the $V_{\mathrm{ds,peak}}$ value is increased a much worse lifetime performance is observed [40], as shown in Fig. 2.10. The measured transistor is fabricated in a 45-nm CMOS process. A RF stress signal is applied to the drain terminal with $V_{\mathrm{DS}} = 1\,\mathrm{V}$, $V_{\mathrm{ds,peak}} = 2$V. The frequency is 2.4 GHz. The gate terminal is connected to a DC bias voltage of 0.7 V. The I_{DSat} is measured under the condition of $V_{\mathrm{GS}} = V_{\mathrm{GS}} = 1.2\,\mathrm{V}$. The lifetime of the NMOSFET is only 1.4 hour under the stress condition described before. Even with a smaller $V_{\mathrm{ds,peak}}$ stress value, the 45-nm CMOS process shows worse lifetime performance as compared to the 65-nm counterpart, which indicates worse HCI performance for the scaled devices.

The low-frequency lifetime measurement results can be directly applied to the transistor with the stress signal having higher frequency and same amplitude [46], as demonstrated in Fig. 2.11. The lifetime of the transistors is about 10^3 s for different stress frequencies shown in Fig. 2.11. The extracted peak-to-peak drain voltage is around 2.2 V for all the measured frequencies.

Measurement results also show that the HCI issues are independent of the channel width as demonstrated in Fig. 2.12. The NMOSFETs with six different channel width are measured under DC stress condition of $V_{\mathrm{DS}} = 1.8\,\mathrm{V}$, $V_{\mathrm{GS}} = 1.8\,\mathrm{V}$. The measured lifetime are all around 10^3 s showing the independence of the channel width.

2.3 Aging Model of Hot-Carrier Degradation

According to recently published papers [39, 44], depending on the energy (voltage) and the flow of carriers (current), there are three main mechanisms which are responsible for

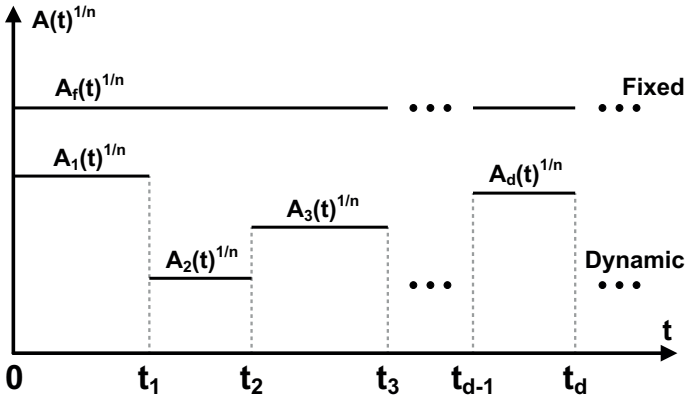


Figure 2.13: Diagrammatic sketch of $A^{\frac{1}{n}}(t)$ for fixed and dynamic operation.

the HCI damage: a) Single Vibrational Excitation (SVE) leads the high energetic carriers to break Si-H bond; b) For the mechanism of Electron Electron Scattering (EES), one carrier is promoted into higher energy by the other one and causes Si-H bond breaking; c) The mechanism of low energetic carriers accumulating enough energy to break Si-H bond is called Multiple Vibration Excitation (MVE).

Based on the three mechanisms described above (SVE, EES, and MVE), the quasi-static hot-carrier model for RF operation is well developed and verified in [44].

$$\Delta I_{\mathrm{DSat}}(t) = A(t) \cdot t^n = \left[\underbrace{\int_0^t A^{\frac{1}{n}}(\tau)\, d\tau}_{Age} \right]^n \tag{2.1}$$

$$\begin{aligned} A^{\frac{1}{n}}(t) &= K_{SVE} \left[\frac{I_{\mathrm{DS}}(t)}{W}\right]^{\alpha_1} \left[\frac{I_{\mathrm{BS}}(t)}{I_{\mathrm{DS}}(t)}\right]^{m} \\ &+ K_{EES} \left[\frac{I_{\mathrm{DS}}(t)}{W}\right]^{\alpha_2} \left[\frac{I_{\mathrm{BS}}(t)}{I_{\mathrm{DS}}(t)}\right]^{m} \\ &+ K_{MVE} V_{\mathrm{DS}}^{\frac{\alpha_3}{2}}(t) \left[\frac{I_{\mathrm{DS}}(t)}{W}\right]^{\alpha_3} \exp\left(\frac{-E_{\mathrm{emi}}}{kT}\right) \end{aligned} \tag{2.2}$$

where $I_{\mathrm{DS}}(t)$ and $I_{\mathrm{BS}}(t)$ are the time-varying drain and substrate current, respectively, which are functions of the time-varying drain-source voltage $V_{\mathrm{DS}}(t)$ and gate-source voltage $V_{\mathrm{GS}}(t)$. K and α are damage-mechanism-related constants. m and n are process-related constants. E_{emi} is the thermal activation barrier of hydrogen (H) emission. The parameters mentioned above can be extracted from DC stress measurements which covers a wide range of V_{DS} and V_{GS} combinations.

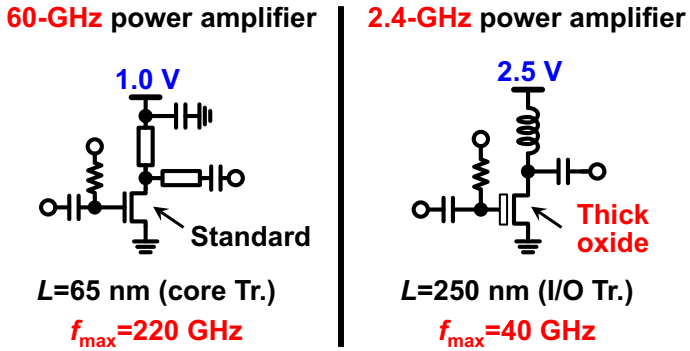


Figure 2.14: HCI issues for 60-GHz amplifiers.

The quasi-static model is demonstrated originally for the transistors operating at fixed biases and input/output power levels. However, it can be extended to dynamic operation situations under which the biases and input/output power change frequently. The basic idea is to reconstruct the age function introduced in Eq. (2.1) as the sum of various age functions corresponding to the dynamic operation conditions, as derived in Eq. (2.3).

$$\begin{aligned}\Delta I_{\mathrm{DSat}}(t) &= \left[\int_0^t A^{\frac{1}{n}}(\tau)\,d\tau\right]^n \\ &= \left[\int_0^{t_1} A_1^{\frac{1}{n}}(\tau)\,d\tau + \int_{t_1}^{t_2} A_2^{\frac{1}{n}}(\tau)\,d\tau \right. \\ &\quad \left. + \int_{t_2}^{t_3} A_3^{\frac{1}{n}}(\tau)\,d\tau + \cdots + \int_{t_{d-1}}^{t_d} A_d^{\frac{1}{n}}(\tau)\,d\tau + \cdots\right]^n \end{aligned} \tag{2.3}$$

where $A_d^{\frac{1}{n}}(t)$ is the degradation rate between t_{d-1} and t_d ($d = 1, 2, 3, \cdots$), which is determined by the specific bias conditions and input/output power levels during that time period. It is worthy of noticing that the integration of the degradation rate (age function) is proportional to the total degradation drift. Consequently, if the area below the time-domain waveform of the dynamic degradation rate is smaller than that of the fixed rate, the dynamic operation will result in a better lifetime, as illustrated in Fig. 2.13.

2.4 Hot-Carrier-Injection Issues at 60 GHz

As indicated in [44], hot-carrier-induced (HCI) effects are dominant for the reliability of the standard CMOS transistors in large-signal operation mode, which are generally used to realize the 60-GHz PAs. It is because the inherently large voltage swing at the output of the PA is the main source of the HCI damage. Unfortunately, a thick-oxide transistor, a

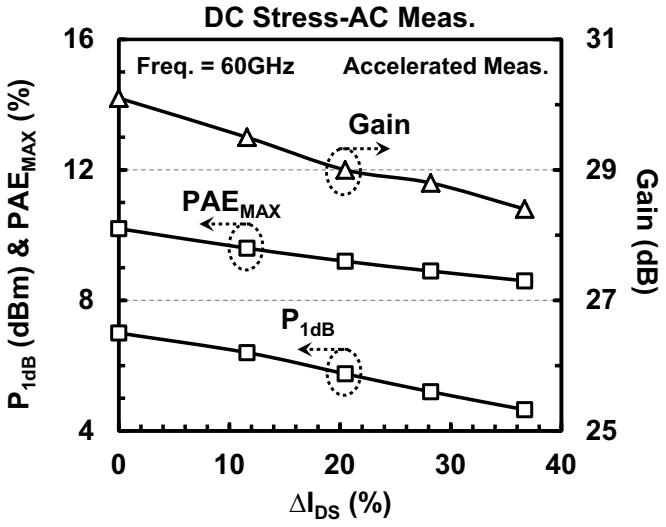


Figure 2.15: Measured HCI degraded ΔI_{DS} versus circuit performance of a 60-GHz CMOS power amplifier.

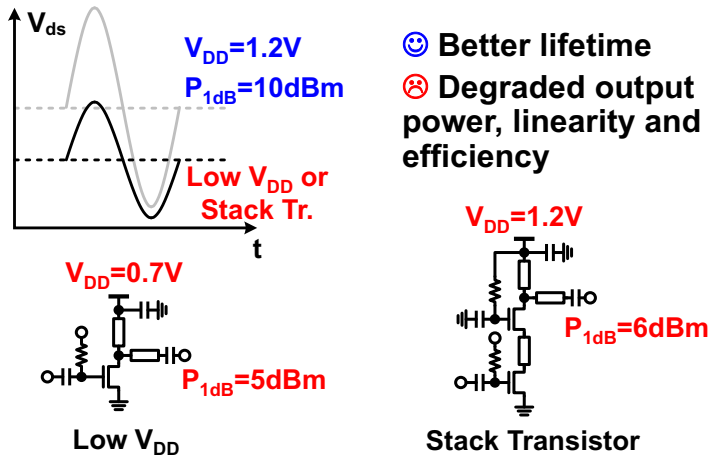
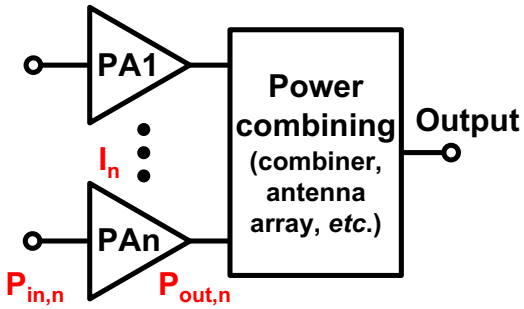


Figure 2.16: Conventional solutions of HCI issues for 60-GHz CMOS power amplifiers.

common solution for reliability issues at lower frequencies, can not be utilized for 60-GHz CMOS PA design due to its limited maximum oscillation frequency (f_{max}) as illustrated in Fig. 2.14. Fig. 2.15 demonstrates the performance degradation of the 60-GHz CMOS power amplifier with the HCI induced drain current decreasing. It can be observed that the P_{1dB} degradation is more than 2 dB when the drain current (measured with V_D=1.2V, V_G=0.7V) is decreased by 36%.

Much effort has been carried out to solve the HCI issues for the 60-GHz CMOS PAs. As shown in Fig. 2.16, reducing the operation supply voltage [47] and using cascode topology [48] for the PAs can greatly alleviate the HCI effects on the PAs but at the cost



$$\textbf{Individual: PAE} = \frac{P_{out,n} - P_{in,n}}{I_n V_{DD}} \approx \textbf{Combined: PAE} = \frac{n \times (P_{out,n} - P_{in,n})}{n \times I_n V_{DD}}$$

☺ **Compensate output power and linearity**

☹ **Deteriorated efficiency can not be improved**

Figure 2.17: Power combining techniques.

of the degraded output power, linearity, and efficiency.

Power combining techniques using on-chip combiner [49] and antenna array [15] depicted in Fig. 2.17 can be used to compensate the degraded output power and linearity. However, the deteriorated efficiency remains to be unimproved.

Chapter 3

Reliability-Enhanced 60-GHz CMOS PA using Variable Supply Voltage

3.1 Introduction

Wireless transceivers operating in the unlicensed 9-GHz band around 60 GHz in CMOS processes have been investigated and reported intensively in the past several years, due to their capability of achieving low-cost multi-gigabit-per-second short-range wireless communications [12,13,50]. It is known that a power amplifier (PA) is one of the key blocks of wireless transceivers, the properties of which are crucial for the system performance, such as linearity, efficiency, communication distance, *etc*. For practical uses of 60-GHz CMOS PAs, reliability, suffering from hot carrier, bias temperature instability, time dependent dielectric breakdown and so on, is one of the most significant issues [47]. Furthermore, as indicated in [44], hot-carrier-induced (HCI) effects are dominant for the reliability of the advanced CMOS transistors in large-signal operation mode, which are generally used to realize the 60-GHz PAs. It is because the main source of the HCI damage is the inherently large voltage swing at the output of the PA. However, a common solution for reliability issues at lower frequencies, thick-oxide transistors, can not be used for 60-GHz CMOS PA design due to the limited maximum oscillation frequency ($f_{\max}$).

Much work has been done to solve the HCI issues for the 60-GHz CMOS PAs. Reducing the operation supply voltage [47] and using cascode topology [48] for the PAs can greatly alleviate the HCI effects on the PAs but at the cost of the degraded output power, linearity, and efficiency. Power combining [49] and beamforming [15] techniques can be used to compensate the degraded output power and linearity. However, the deteriorated efficiency remains to be unimproved.

Meanwhile, compared with the counterpart of frequency division duplex (FDD), time

division duplex (TDD) is preferred for high-data-rate short-range communication systems, because the TDD operation can eliminate the stringent requirements of filtering and extend the available bandwidth for the transceivers. As for TDD operation of the 60-GHz transceivers, fast-recovery ability from sleep mode to awaking mode of the transmitters, especially the PAs, is necessary for multi-gigabit-per-second (multi-Gb/s) throughput (*e.g.* less than 3 μs for over 2 Gb/s throughput) [13, 51]. Unfortunately, not many papers have discussed this feature for the 60-GHz CMOS PAs before.

In this chapter, a 60-GHz digitally-assisted variable-supply-voltage PA is proposed and implemented to relieve the HCI influences on the circuit [52]. A fully-integrated mixed analog-digital low drop-out voltage regulator (LDO) is designed to dynamically adjust the supply voltage of the last stage of the PA (V_{PA}) between 0.7 V and 1.0 V. The adjustment of V_{PA} offers a possibility to meet different linearity, efficiency, output power, and lifetime requirements for the PA in actual applications. The PA is capable of outputting 13.2 dBm saturation power (P_{sat}), 10.2 dBm power at 1-dB compression point (P_{1dB}) and achieving 15.0% peak power-added efficiency (PAE). The PA fabricated in a standard 65-nm CMOS process is insensitive to the process variations thanks to the tunable supply voltage.

3.2 Proposed 60-GHz Variable-Supply-Voltage PA

3.2.1 System Block Diagram and Dynamic Control Scheme

Fig. 3.1 shows the entire block diagram of the proposed 60-GHz digitally-assisted variable-supply-voltage CMOS PA. The whole system is composed of a mixed analog-digital LDO, a 3-stage balanced PA and a digital control block with reference voltage generator. The mixed analog-digital LDO co-operating with the digital control block is used to dynamically tune the supply voltage V_{PA} for the last stage of the PA, which normally suffers the most from the HCI effects and dominates the lifetime of the PA. The dynamic control scheme under TDD operation depicted in Fig. 3.2 is described as follows:

a) When a wake-up signal is sent to the digital control block of the proposed PA, the mixed analog-digital LDO will turn on the supply voltage V_{PA} promptly.

b) After the PA is woken up, the digital control block will monitor the setting of the supply voltage and output power. If a control frame is received indicating the new supply voltage and output power settings, the LDO alters V_{PA} accordingly. Otherwise V_{PA} will be maintained in the same level. The key point of dynamic operation is when the transmitter does not require high output power and/or linearity, V_{PA} can be decreased to relieve the HCI stress. On the other hand, once the superior performance of the PA is demanded by

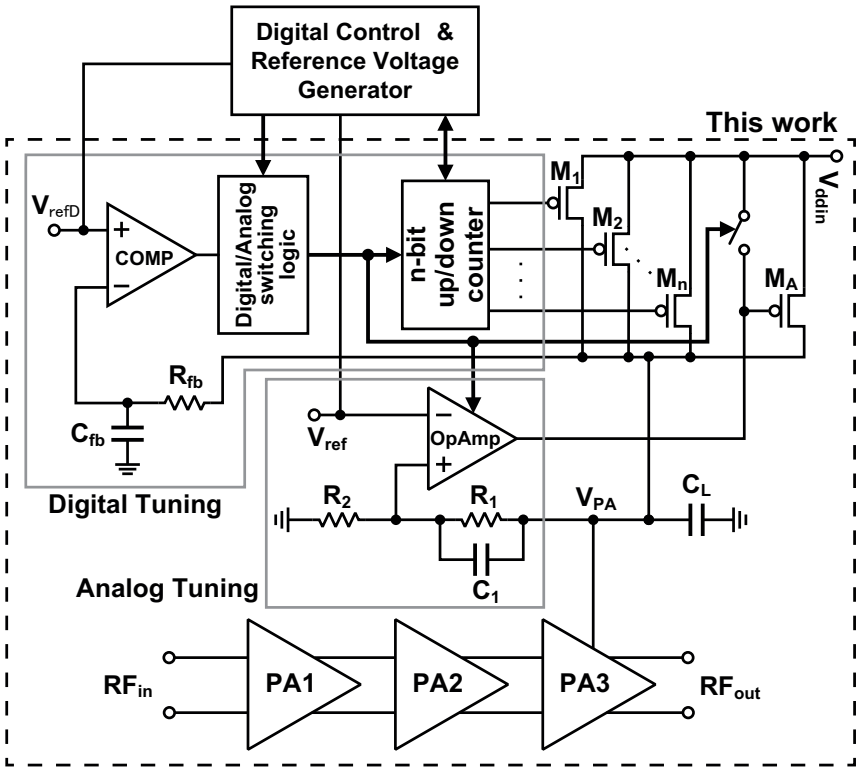


Figure 3.1: System block diagram of the proposed 60-GHz digitally-assisted variable-supply-voltage PA.

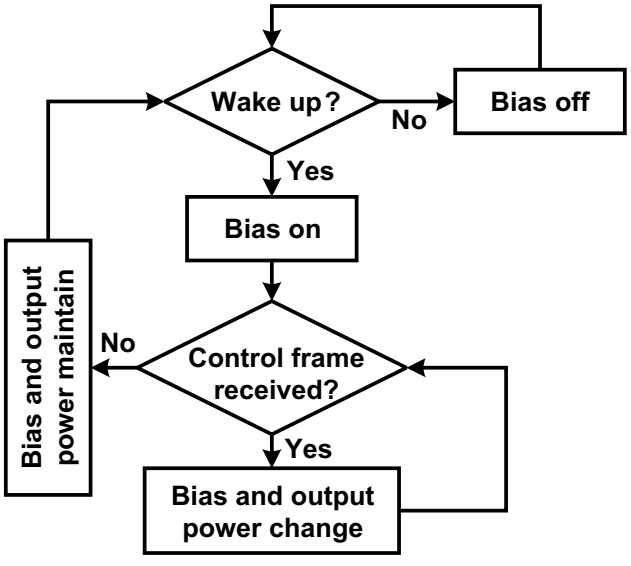


Figure 3.2: The flow chart of the dynamic control scheme for TDD operation.

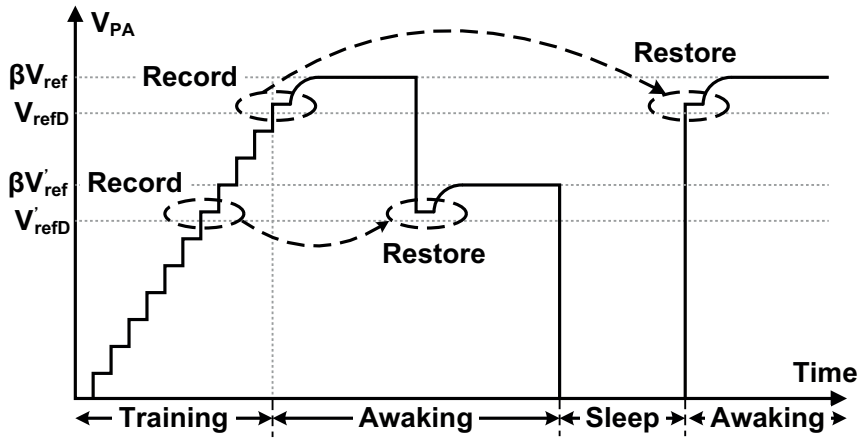


Figure 3.3: The conceptual transient operation of the mixed analog-digital LDO.

the transmitter, V_{PA} can be elevated to meet the requirements.

The digital control and reference voltage generator block is used to provide enable signals for the digital/analog switching logic and the n-bit up/down counter while generating reference voltages for the digital and analog tuning blocks. The control bits for M_1 to M_n can also be memorized in the digital control block.

3.2.2 Mixed Analog-Digital LDO

The mixed analog-digital LDO consists of a digital-tuning block, an analog-tuning block and an array of PMOSFETs, as can be seen in Fig. 3.1. The digital-tuning block [53, 54], including a dynamic comparator, an *n*-bit up/down counter and a digital/analog switching logic, is adopted and optimized in this work, because it consumes ultra-low power, can fully turn on the PMOSFETs which achieves low voltage drop-out, and easily accomplish fast recovery and tuning of the supply voltage V_{PA}. Where the fast recovery feature is necessary for multi-Gb/s wireless transmitters operating in time division duplex mode (*e.g.* less than $3\,\mu$s for over 2 Gb/s throughput) [13]. The analog-tuning block is utilized to avoid the inherently large ripple of the digital-tuning block when the 3-stage PA is working.

Fig. 3.3 illustrates the transient operation of the mixed analog-digital LDO with the assistance of the digital control block for fast tuning and recovery of the supply voltage V_{PA}. At the beginning of the LDO operation, the digital-tuning block goes through a training period while analog-tuning block is turned off by the switching logic. V_{PA} is swept from minimum to maximum value by adjusting the reference voltage of the digital-tuning block (V_{refD}). The digital control bits of the PMOSFETs (M_1 to M_n) for different values

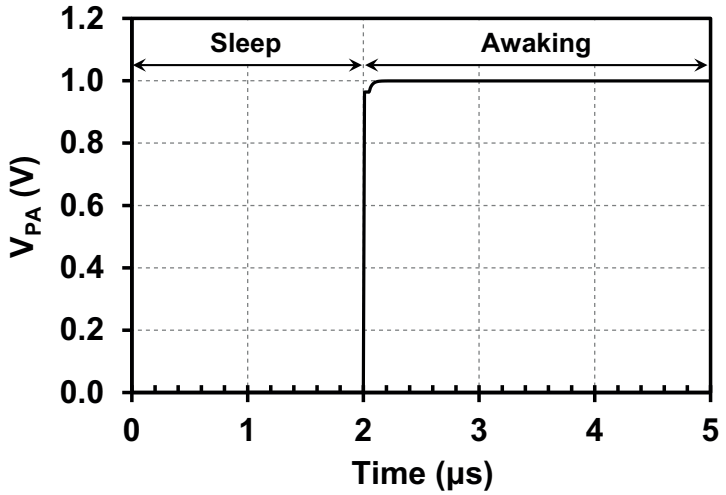


Figure 3.4: The simulation result of the wake-up time for the mixed analog-digital LDO.

of V_{refD} are recorded to the digital control block. Once the training period is finished, when the value of V_{PA} is larger than the setting value of V_{refD}, the LDO is switched from digital to analog mode by the switching logic. After a period of charging (or discharging), the LDO outputs a constant V_{PA} at the value of βV_{ref}, where $\beta = (R_1 + R_2)/R_2$ and V_{ref} is the reference voltage of the analog-tuning block, as depicted in Fig. 3.3. When the desired value of V_{PA} is changed or/and the circuit is awakened from sleep mode, the digital control block restores the control bits for M_1 to M_n to the up/down counter and generates reference voltages correspondingly. V_{PA} will be instantly charged (or discharged) to the value corresponding to the restored digital control bits, then tuned by the analog block of the LDO to the desired value in a short time. The simulation result shows that the recovery time of V_{PA} from sleep mode with a de-coupling capacitance C_L of 86 pF is less than 0.1 μs in this work, as demonstrated in Fig. 3.4.

3.2.3 60-GHz 3-stage Balanced PA

The schematic of the 3-stage balanced CMOS PA is shown in Fig. 3.5. The HCI effects on the PA are further alleviated owing to the adoption of the balanced topology. A transmission line (TL) with 1.4 dB/mm loss around 60 GHz is used for matching network, and an MIM transmission line (MIM TL) is realized for the de-coupling of the power supplies. The channel widths of the transistors used for the 3-stage balanced PA from input to output terminal are 2×20 μm, 2×30 μm, and 2×40 μm, respectively. The cross-coupled capacitors (C_{c1} and C_{c2}) connected between the gate and the drain of the opposite-side transistors are incorporated for the first and second stage of the PA to neutralize the para-

sitic gate-to-drain capacitances. The reverse isolation, stability, and power gain of the PA are improved by utilizing the capacitive cross-coupling technique [55, 56]. This 60-GHz PA can be connected directly to a differential antenna, and can also be connected to a single-ended antenna through an on-chip balun [57].

3.3 Experimental Results and Discussions

3.3.1 Measurement Results

To verify our design, the core blocks of the proposed 60-GHz PA including the mixed analog-digital LDO and the 3-stage balanced PA are fabricated in a standard 65 nm CMOS technology. The digital control and reference voltage generator block is not implemented in this work. The enable signals and reference voltages are provided by measurement

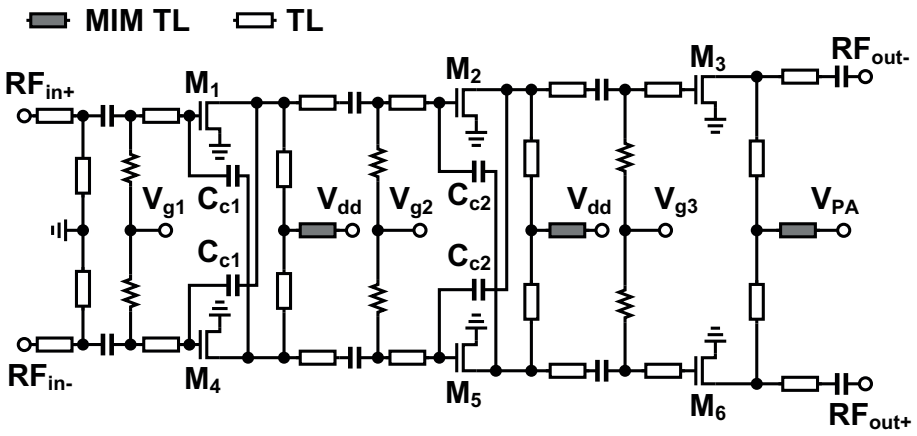


Figure 3.5: The 60-GHz 3-stage balanced PA core.

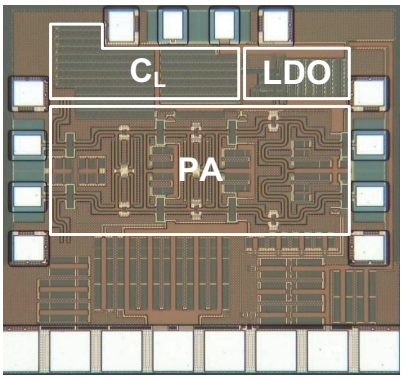


Figure 3.6: Die micro-photograph. Chip size: 0.70×0.80 mm^2 including pads.

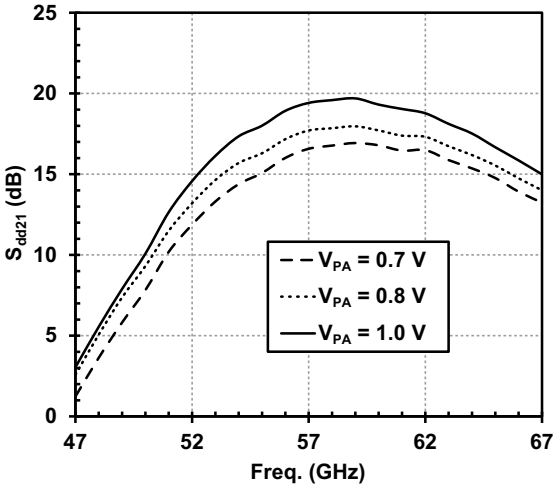


Figure 3.7: Measured S_{dd21} for various values of V_{PA}.

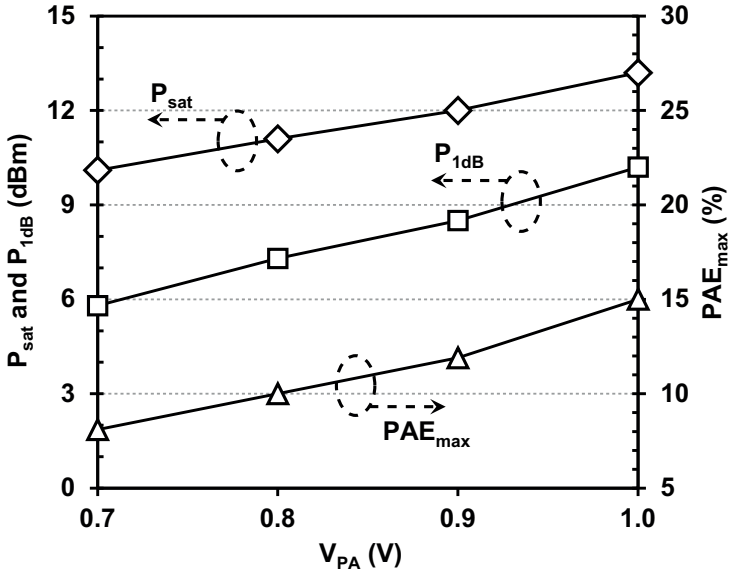


Figure 3.8: Measured P_{sat}, P_{1dB} and PAE_{max} versus V_{PA} at 60 GHz.

equipments. The fast tuning of the V_{PA} shown in Fig. 3.4 is not realized in this prototype. Fig. 3.6 shows the die micro-photograph of the circuit. The areas of the 3-stage balanced PA and the mixed analog-digital LDO are 0.132 mm^2 and 0.025 mm^2, respectively. The on-chip de-coupling capacitor (C_L) is 86 pF with a size of 0.051 mm^2. The supply voltage of the first and second stage of the PA (not tuned by the LDO) and the external input voltage of the LDO (V_{ddin}) are set to be 1.2 V for demonstration simplicity. The balun probes (GSSG) are used to measure the large-signal characteristics. The insertion loss of balun probes is de-embedded from the measurement results afterwards. Due to the limited

number of pads, V_{PA} cannot be measured directly, so V_{PA} is calculated by βV_{ref}.

As depicted in Fig. 3.7, the small-signal S-parameter of the PA is measured for different values of V_{PA}. The 3-dB bandwidth is about 13 GHz (from 53 GHz to 66 GHz) for all the measurement values of V_{PA}. The peak gain is 19.7 dB and 17.0 dB at 59 GHz for V_{PA} = 1.0 V and V_{PA} = 0.7 V, respectively. The measured P_{sat}, P_{1dB} and maximum PAE (PAE_{max}) are plotted versus V_{PA} at 60 GHz in Fig. 3.8. The P_{1dB} is reduced from 10.2 dBm to 5.8 dBm when V_{PA} is tuned from 1.0 V to 0.7 V as can be observed in Fig. 3.8. The HCI stress on the circuit is therefore lightened by decreasing the supply voltage and output power simultaneously, which leads to a better lifetime for the proposed PA. More detailed large-signal measurement results such as the input power (P_{in}) versus the output

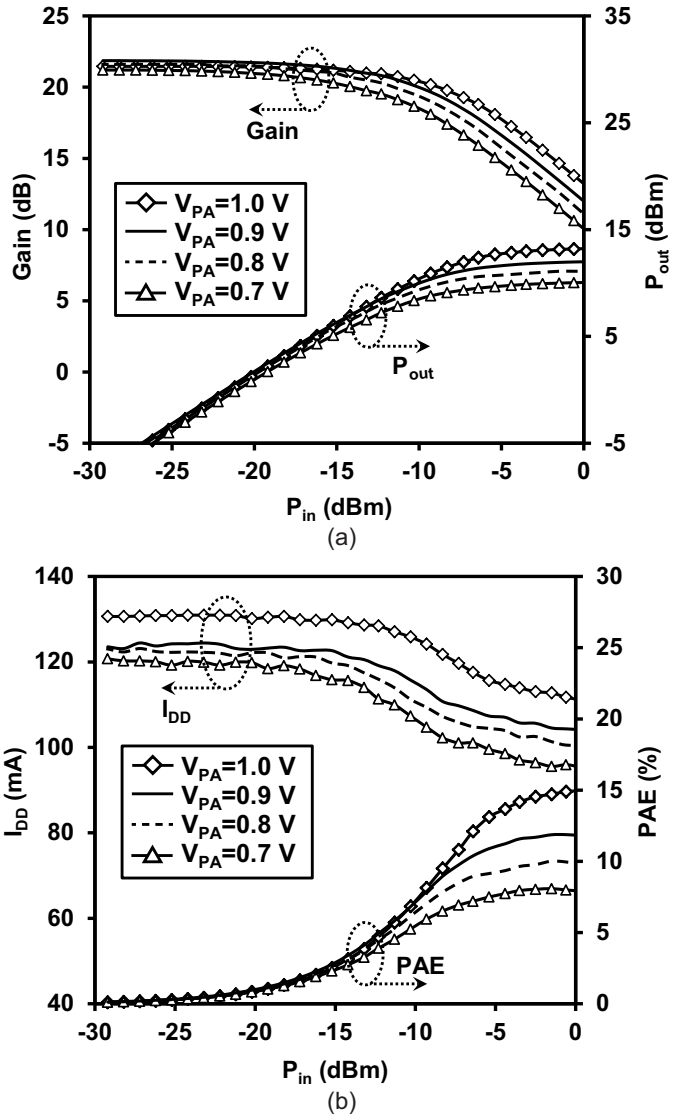


Figure 3.9: (a) Measured P_{in} versus P_{out} and Gain; (b) Measured P_{in} versus PAE and I_{DD} at 60 GHz.

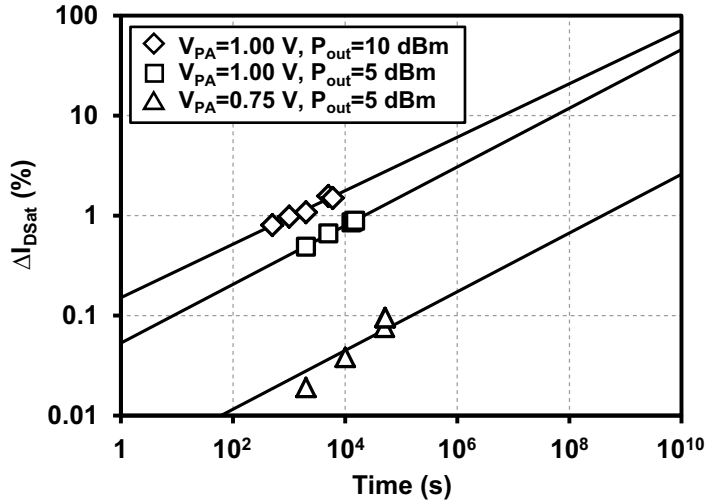


Figure 3.10: Measured (symbol) and estimated (solid line) ΔI_{DSat} of the NMOSFETs operating at 60 GHz for different values of V_{PA} and output power P_{out}.

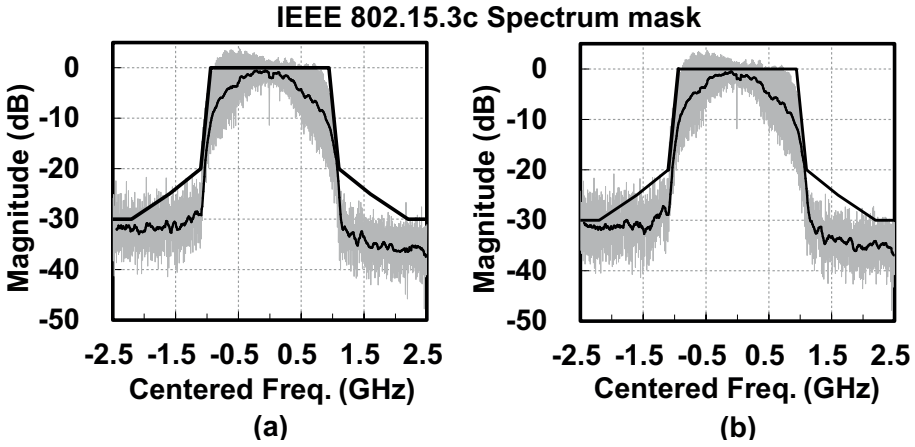


Figure 3.11: Measured output spectrum of the proposed PA centered at 62.64 GHz for QPSK modulation (a) $V_{\mathrm{PA}} = 1.0$ V, $P_{\mathrm{out}} = 4$ dBm; (b) $V_{\mathrm{PA}} = 0.7$ V, $P_{\mathrm{out}} = 3$ dBm.

power (P_{out}), gain, PAE, and the total DC current of all the on-chip building blocks (I_{DD}) are shown in Fig. 3.9. The power consumption of the PA is calculated from I_{DD} and the 1.2 V supply voltage, which is used for the PAE characterization. The static power consumption of the proposed PA varies from 145 mW (LDO: 26 mW including PMOS switches) to 157 mW (LDO: 12 mW including PMOS switches) when V_{PA} is changed from 0.7 V to 1.0 V.

In Fig. 3.10, the measured (symbol) and estimated (solid line) saturation drain current degradation of the NMOSFETs used in the last stage of the PA is illustrated under different

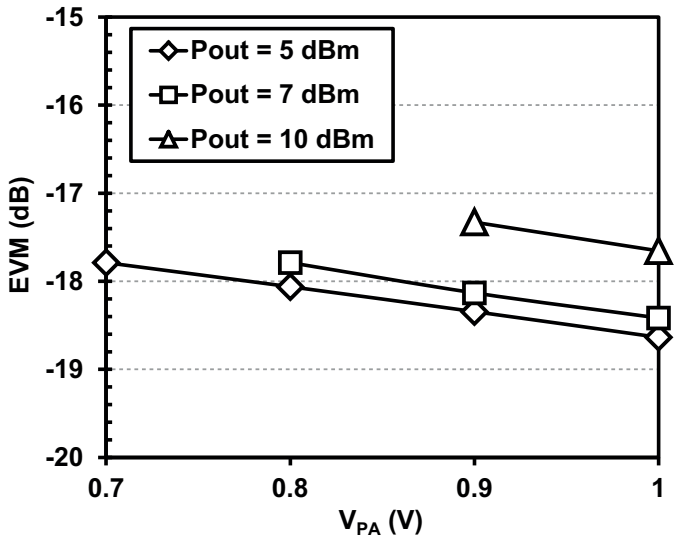


Figure 3.12: Measured EVM versus V_{PA} for QPSK modulation at different output power level.

Table 3.1: 60-GHz CMOS PA Performance Comparison.

Ref	CMOS Process	Freq. (GHz)	Supply (V)	P_{sat} (dBm)	P_{1dB} (dBm)	PAE_{max} (%)	Lifetime (year)	Area (mm^2)
[47]	90 nm	60	0.7	8.5	5.2	7.0	$> 10^{4*}$	0.18 (core)
			1.0	11.5	8.0	15.2	$> 10^{*}$	
[48]	65 nm SOI	60	1.2	10.5	7.1	22.3	N/A	0.573
			1.8	14.5	12.7	25.7		
			2.6	16.5	15.2	18.2		
[49]	65 nm	60	1.0	18.6	15.0	15.1	N/A	0.28
[56]	65 nm	60	1.0	11.5	8.0	15.2	$> 10^{*}$	0.696
This work	65 nm	60	$0.7^{\dagger}$	10.1	5.8	8.1	$> 3 \times 10^4$	0.56
			$1.0^{\dagger}$	13.2	10.2	15.0	> 0.2	

* Non-measured results † Only for the last stage V_{PA}

RF (60-GHz) stress conditions. When the output power of the PA (P_{out}) is 10 dBm and $V_{PA} = 1.00$ V, the lifetime of the NMOSFETs is only 0.2 year. While if $P_{out} = 5$ dBm and $V_{PA} = 0.75$ V, the lifetime is improved to far more than 10 years. It is worthy of knowing that the stress condition of $P_{out} = 5$ dBm and $V_{PA} = 0.75$ V induces very small

degradation in the saturation drain current at the beginning of the lifetime measurement. The time exponent of the recorded data fitting line is very different from other stress conditions, which theoretically should be same. Therefore, the average value of the time exponent for other stress conditions are used for the plotting of the estimated line.

Table 3.1 summarizes and compares the performance of the proposed power amplifier with that of the state-of-the-art PAs at 60 GHz in CMOS processes. It is shown in Table 3.1 that the proposed PA exhibits comparable output power and efficiency at high supply voltage (V_{PA} = 1.0 V) to the recently published PAs in the 60-GHz band for CMOS technologies. Meanwhile, at low supply voltage (V_{PA} = 0.7 V), the proposed PA with reasonable output power, efficiency and linearity still can be used for shorter distance communications or/and low-level modulation schemes (*e.g.* BPSK and QPSK).

As demonstrated in Fig. 3.11, the measured output spectrum of the proposed PA barely degrades when V_{PA} is reduced from 1.0 V to 0.7 V and output power is comparably small. The measurement is performed by applying a QPSK modulation signal to the input of the PA at channel 3 of IEEE 802.15.3c standard (61.56 GHz to 63.72 GHz) with a symbol rate of 1.76 Gs/s. The center frequency of this channel is 62.64 GHz. Both of the spectrums meet the IEEE 802.15.3c standard. Fig. 3.12 shows the measured EVM at various values of V_{PA} and P_{out}. The channel 3 of IEEE 802.15.3c standard and 3.52-Gb/s QPSK modulation signal are chosen again to evaluate the EVM performance of the proposed PA. All the measured EVM is lower than -17 dB and satisfies IEEE 802.15.3c standard. It can be observed that the measured EVM is changed from 11.7% (-18.6 dB) to 12.9% (-17.8 dB) for low output power (P_{out} = 5 dBm) if V_{PA} is tuned from 1.0 V to 0.7 V. The degradation of the EVM is less than 1 dB, which implies that the low supply voltage V_{PA} is preferred for low output power situation considering the HCI issues. While at high output power (P_{out} = 10 dBm), the measurement values of the EVM are 13.1% (-17.7 dB) and 13.6% (-17.3 dB) for V_{PA} = 1.0 V and V_{PA} = 0.9 V, respectively.

3.3.2 Application Scenario

It is known that for a fixed high communication data rate at 60-GHz band, large supply voltage and output power are needed for the PA to reach long communication distance. However, keeping the supply voltage and output power at high level will degrade the lifetime of the PA quickly. One solution is to sacrifice the communication distance or data rate for better lifetime, which causes bad user experiences. Therefore, the dynamic operation schemes [58], which are normally used for improving power efficiency and overcoming interference, can be adopted and extended to elevate the lifetime of the PA while providing high-data-rate and relatively long-range communication.

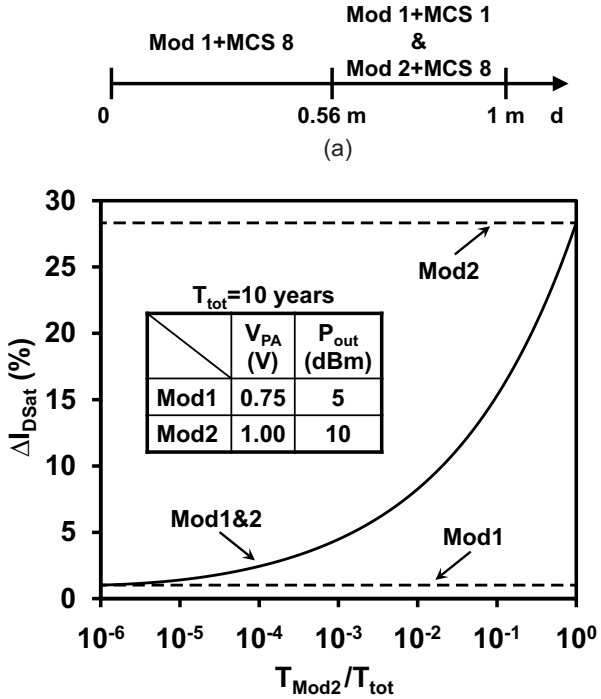


Figure 3.13: (a) One application scenario of the dynamically operated PA; (b) estimation of ΔI_{DSat} of the NMOSFETs for the application versus the percentage of the operation time of Mod 2.

Table 3.2: Single Carrier Mode of IEEE 802.15.3c Std.

MCS identifier	8		1
Data rate	2640 Mb/s		412 Mb/s
Receiver sensitivity	−56 dBm		−61 dBm
NF	8 dB		
Thermal noise	−73.5 dBm		
Required CNR	17.5 dB		12.5 dB
Tx antenna gain	2 dBi		
Distance	0.56 m	1 m	1 m
Frequency	60 GHz		
LOS loss	−63 dB	−68 dB	−68 dB
Rx antenna gain	2 dBi		
Implementation loss	−2 dB		
Required $P_{\mathrm{out,min}}$	5 dBm	10 dBm	5 dBm

The operation scheme is simply explained in this subsection by taking the single carrier mode of IEEE 802.15.3c standard as an example. As shown in Fig. 3.13 and Table 3.2, when the communication distance is more than 0.56 m and data rate is as high as 2640 Mb/s, the low output power mode (Mod1: $V_{PA} = 0.75\,V$ and $P_{out} = 5\,dBm$) can not satisfy the communication requirements.

The high output power mode (Mod2: $V_{PA} = 1.00\,V$ and $P_{out} = 10\,dBm$) is needed. In order to guarantee 10-year lifetime of the PA, the operation time period of high output power mode should be carefully arranged. Fig. 3.13 (b) shows the estimation results of ΔI_{DSat} of the NMOSFETs used in the last stage of the PA for the application mentioned in this subsection. Where T_{Mod2} and T_{tot} are the operation time of Mod2 and all of the modes, respectively. The results are calculated using Eq. (2.3) and the parameters extracted from the stress measurements. The lifetime of the PA is over 10 years, as long as the operation time of Mod2 is less than 2% of T_{tot}, as can be observed in Fig. 3.13 (b).

3.4 Conclusions

This chapter presents a 60-GHz variable-supply-voltage power amplifier using the digitally-assisted LDO, in a 65-nm CMOS process. The severe HCI issues for 60-GHz CMOS power amplifiers have been greatly alleviated through the dynamic operation. The lifetime of the proposed PA can be improved to over 10 years with the careful arrangement of various operation modes. On the other hand, the power amplifier is still able to provide 13.2 dBm saturation power, 10.2 dBm power at 1-dB compression point and 15.0% peak power-added efficiency at 60 GHz for high supply voltage ($V_{PA} = 1.0\,V$). The performance of the proposed PA at various V_{PA} conditions meets the requirements of short-range multi-gigabit-per-second communication standards (*e.g.* IEEE 802.15.3c).

Chapter 4

HCI-Healing 60-GHz CMOS Transceiver

4.1 Introduction

The research of 60-GHz CMOS transceivers has bloomed due to their capability of achieving low-cost multi-Gb/s short-range wireless communications [11]. Considering practical use of the 60-GHz CMOS transceivers, longer operation lifetime with high output power is preferred to provide reliable products. Unfortunately, as discussed before, the output power capability of the transmitter will gradually degrade due to the hot-carrier-injection (HCI) effects in the standard CMOS transistors at large-signal operation (*e.g.* power amplifiers). It is because the inherently large voltage swing at the output of the power amplifiers (PAs) is the main source of the HCI damage. Unfortunately, a thick-oxide transistor, a common solution for reliability issues at lower frequencies, cannot be utilized for 60-GHz CMOS PA design due to its limited maximum oscillation frequency ($f_{\max}$).

Conventional solutions are demonstrated to be very effective to solve the HCI issues for the 60-GHz CMOS PAs but at the cost of low output power, linearity, and efficiency. The proposed variable-supply-voltage PA can greatly alleviate the HCI issues while maintaining the capability of outputting large power and high linearity. However, in order to achieve normally required 10-year lifetime, the operation time of the high output power mode is limited to a short period. The solution for longer operation lifetime with high output power is still desired for providing reliable products.

This chapter presents a 60-GHz CMOS transceiver with HCI damage healing function, which can detect the HCI damage to the transistor used in the PA and heal it afterwards [59]. The proposed HCI-healing technique relieves the trade-off between the HCI reliability and the system performance, which guarantees longer operation lifetime

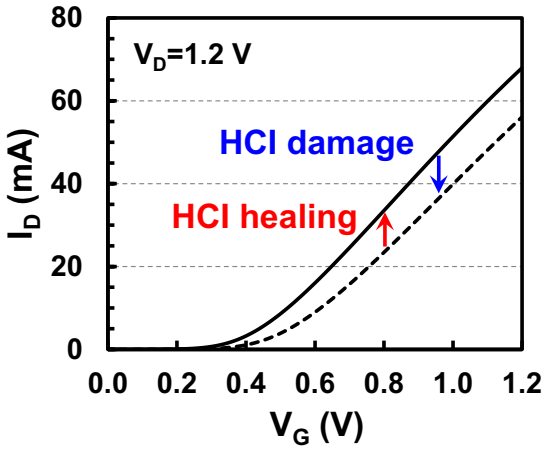


Figure 4.1: The conceptual illustration of HCI healing idea.

with high output power. The proposed transceiver demonstrates an EVM of -27.9 dB in 16 QAM and can transmit 7 Gb/s within 2.16-GHz bandwidth. The transmitter, receiver, and PLL consume 174 mW, 144 mW, and 44 mW from a 1.2-V supply, respectively. The core area of the TRX is 2.3 mm^2.

4.1.1 The Concept of HCI Healing

It is known that the HCI damage can severely deteriorate the current capability of the transistor and therefore the output power, linearity, and efficiency of the CMOS power amplifiers. The conventional solutions for the HCI issues mainly focus on the alleviation of the HCI damage on the CMOS transistors, which is accomplished by reducing the supply voltage and output power of the PAs. However, these solutions degrade the initial linearity and efficiency of the power amplifier with low output power capability and still can not prevent the damage to the transistor. Simply increasing the gate voltage of the transistor can temporarily compensate the degraded performance. Nevertheless, the increased gate voltage can accelerate the HCI damage causing a even worse lifetime of the transistor. Ultimately, the physical healing of the HCI damage is desired to maintain the initial system performance. With the proposed HCI healing technique, the HCI-damage induced current degradation is recovered once the degradation reaches a certain criteria, as illustrated in Fig. 4.1. Therefore, longer operation time with better system performance can be achieved.

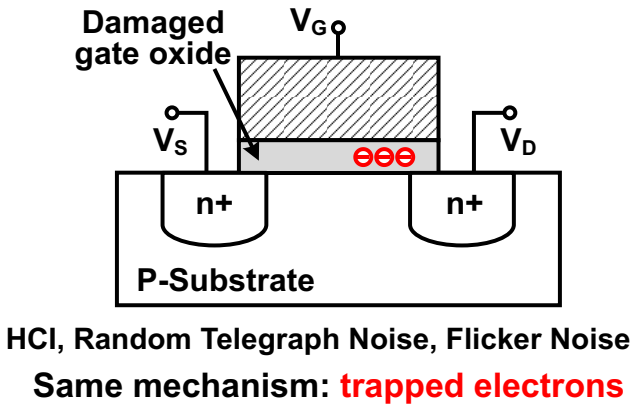


Figure 4.2: HCI damage mechanism.

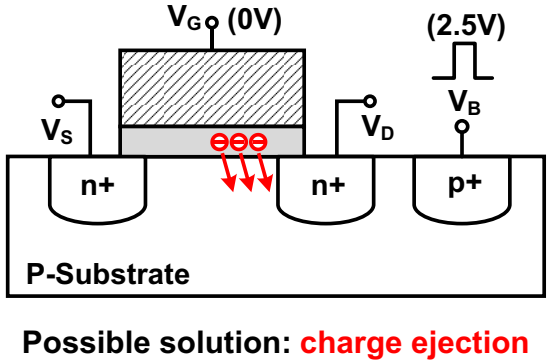


Figure 4.3: Possible solution for HCI damage healing.

Table 4.1: Bias Conditions of the HCI-Healing Transistor Module

Status	60-GHz operation	HCI damaging	HCI healing
V_{GT}	1.2 V	1.2V	0 V
V_S	0 V	0 V	High Z
V_G	Bias (*e.g.* 0.7 V)	Bias (*e.g.* 0.7 V)	0 V
V_H	0 V	0 V	High voltage
V_D	1.2 V (Small V_{od} swing)	1.2 V (Large V_{od} swing)	0 V

4.2 Proposed HCI-Healing Mechanism and Module

It is know that random telegraph noise (RTN) and flicker noise share the the same mechanism of randomly trapping and ejection of electrons in gate oxide [60]. The HCI damage

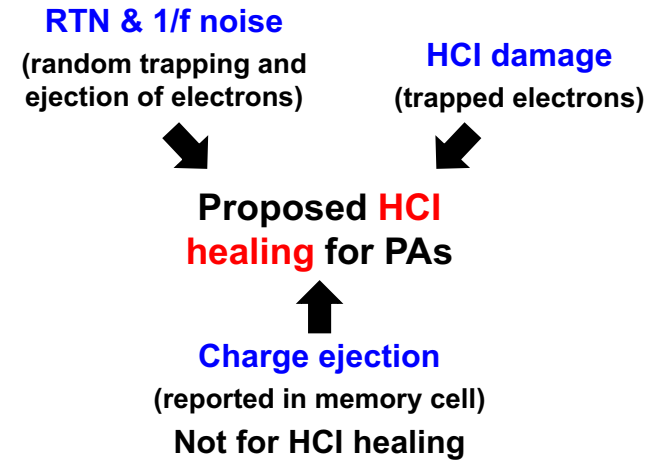


Figure 4.4: The relation between previous researches and the proposed healing technique.

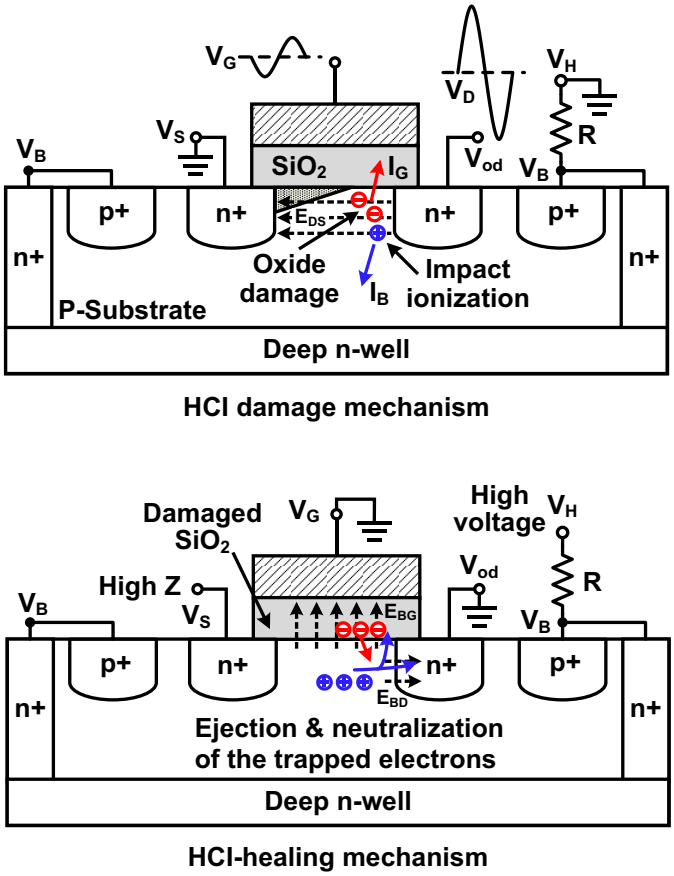


Figure 4.5: Transistor level HCI healing mechanism.

is also due to the trapped electrons in the gate oxide as depicted in Fig. 4.2. If we can find a solution to strengthen the ejection phenomenon of the trapped electrons in the damaged

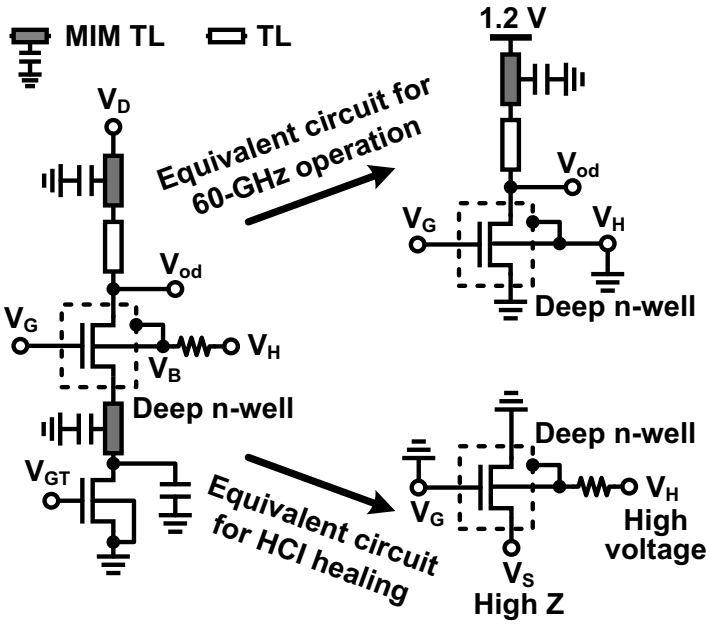


Figure 4.6: Proposed HCI-healing transistor module.

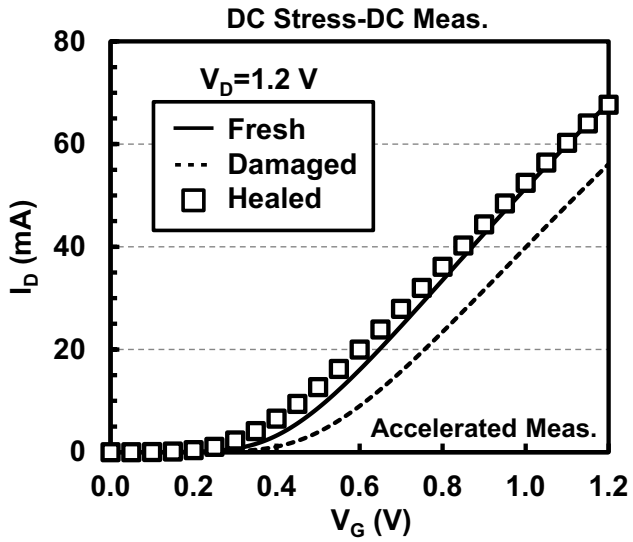


Figure 4.7: The measured I-V Curve of the stand-alone transistor TEGs.

gate oxide, the HCI damage can be physically healed. As shown in Fig. 4.3, it can be achieved by applying a short pulse of high voltage at the bulk terminal and low voltage at the gate terminal simultaneously. A non-volatile memory using a standard CMOS transistor has been reported with 100-times program/erase endurance [61], where the drain-side-assisted charge ejection technique in gate oxide is applied to control the threshold voltage (not for HCI healing). In this research, a charge ejection technique is applied to a

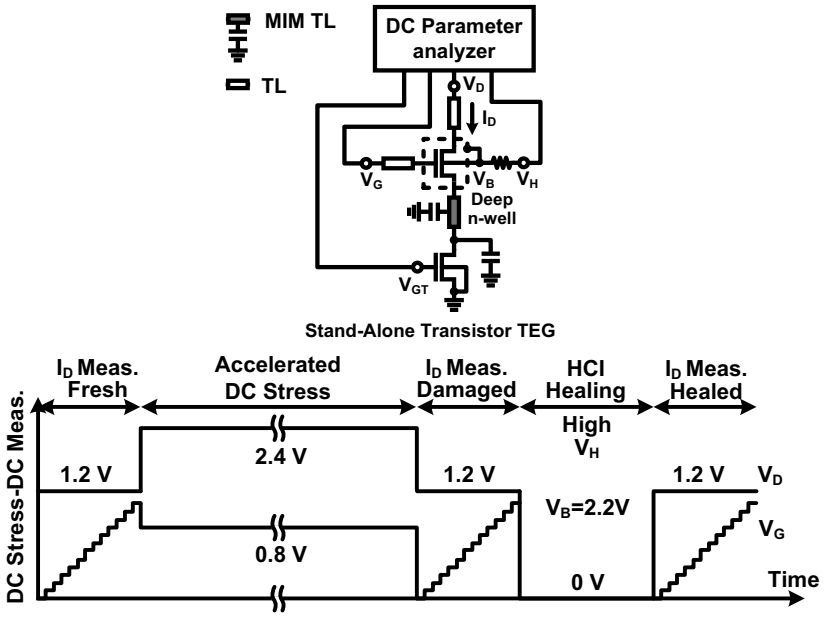


Figure 4.8: The setup and procedure for DC stress-DC measurement of the stand-alone transistor TEGs.

millimeter-wave power amplifier as shown in Fig. 4.5, which is the world's first reported HCI healing technique for the power amplifiers. The relationship between the researches of RTN, flicker noise, memory cell, and this work can be illustrated in Fig. 4.4. The corresponding proposed HCI-healing transistor module is depicted Fig. 4.6

The proposed HCI-healing transistor module is composed of a core NMOSFET with deep n-well, a tail switching transistor, a MIM transmission line (MIM TL) with a MIM capacitor array attached alongside, and a high-density decoupling capacitor. The body terminal of the core NMOSFET (V_B) is connected to the HCI-healing bias (V_H) through a current-limiting resistor. When the module is in HCI-healing status, the tail transistor is switched off, which creates a high impedance (high Z) terminal for the source of the core NMOSFET. The drain and gate terminals of the core NMOSFET are biased to ground. A high voltage is applied to V_H generating a strong vertical electric field between substrate and gate to eject and neutralize the trapped electron [61]. Meanwhile, the drain side is forward biased for assisting the HCI-healing procedure. In this work, an external 10-V voltage source is used for V_H. The measured peak current is 3.9 mA corresponding to a V_B of 2.2 V. On the other hand, in order to maintain the transistor performance for the 60-GHz operation, the MIM TL and high-density capacitor, together with the tail switch, are connected to the source of the core NMOSFET forming an RF ground. Table 4.1 summarizes the bias condition of each nodes for different operation statuses.

Fig. 4.7 demonstrates the HCI-healing capability of the proposed technique when ap-

plied to a transistor. The I_D-V_G curves of the stand-alone HCI-healing transistor TEG are measured at V_D =1.2 V. An accelerated DC stress of V_D=2.4 V is applied arising the HCI damage. Then the proposed HCI-healing technique is used to recover the drain current (I_D) as illustrated in Fig. 4.8. The HCI damage is mainly observed as V_{th} shift. Although adaptively increasing gate bias voltage (V_G) also can compensate I_D [62], the HCI effects are strengthen by the increased V_G shortening the lifetime of the transistor, as shown in Fig. 4.9.

4.3 60-GHz CMOS PA with HCI-Healing Function

Fig. 4.10 shows the 60-GHz CMOS PA with the proposed HCI-healing function. The PA has 6 stages with a common-source topology for the first 5 stages. The HCI-healing

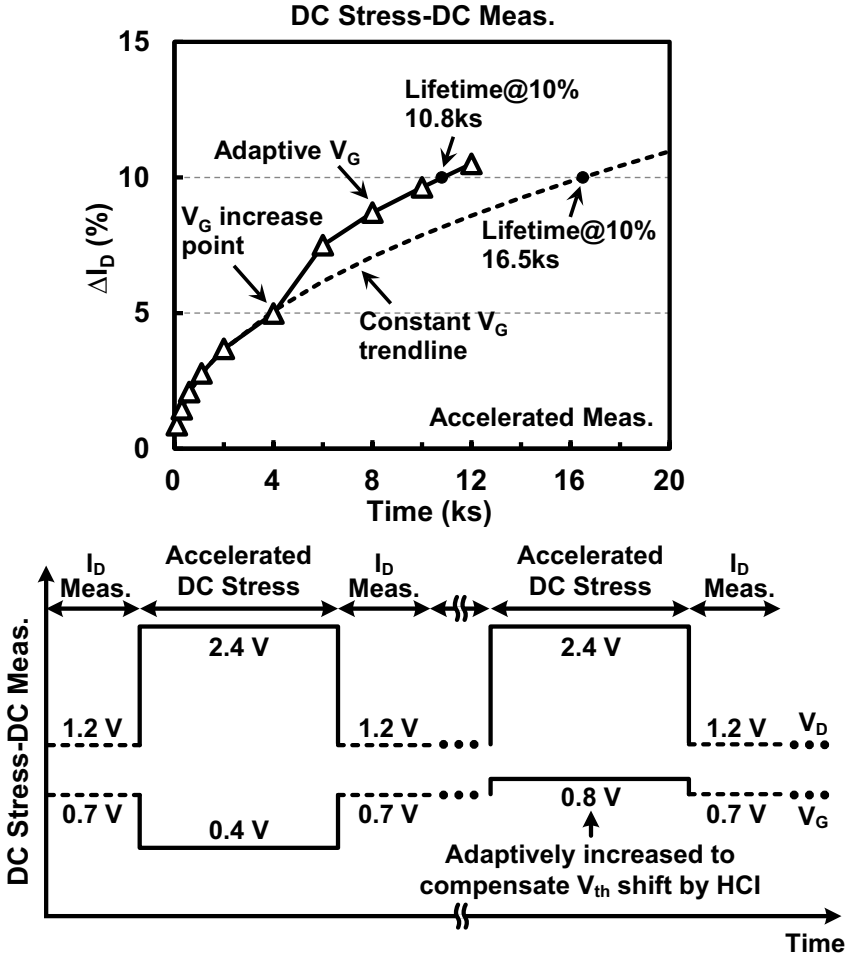


Figure 4.9: The measured lifetime of stand-alone transistor TEG.

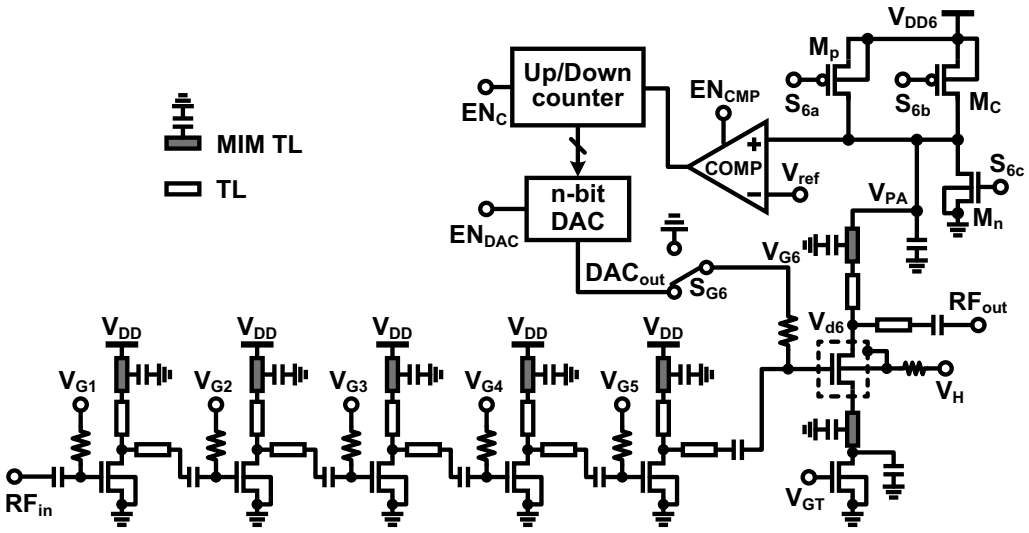


Figure 4.10: The topology of the 60-GHz CMOS PA with the proposed HCI-healing function.

Table 4.2: Status of the sub-blocks/switches at different operation modes

Status	S_{6a}	S_{6b}	S_{6c}	EN_{CMP}	EN_C	EN_{DAC}	V_{G6}
60 GHz operation	On	On	Off	Disable	Disable	Enable	DAC_{out}
HCI damage detection	Off	On	Off	Enable	Disable	Enable	DAC_{out}
HCI healing	Off	Off	On	Disable	Disable	Disable	GND

technique is utilized for the last stage which suffers the most from the HCI effects. At the very beginning, the PA goes through an initial gate bias setting phase. The supply switches M_p and M_n are turned off, M_c is on. The feedback loop (including the comparator, counter, and DAC) tunes the gate bias of the last stage (V_{G6}) to make V_{ref} equal to V_{PA}. When the PA is configured for the 60-GHz operation, all the PMOS supply switches (M_p and M_c) are turned on, and M_n is off. The gate-bias-adjusting feedback loop is disabled. The DAC is enabled to provide bias voltage. Due to the HCI effects, the drain current of the last stage of the PA is gradually decreased. If the PA is set to HCI damage detection mode when the PA is not amplifying RF signals. Part of the PMOS supply switches (M_p) is off. V_{PA} will be larger than V_{ref}. The comparator outputs " 1 " indicating that the core

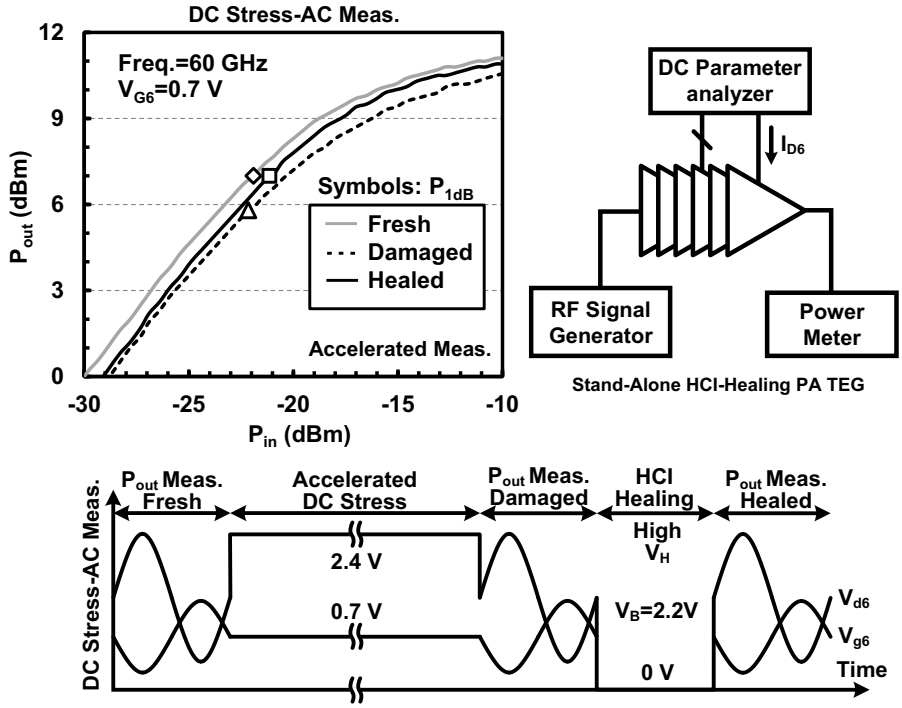


Figure 4.11: The measurement results and setup of P_{in}-P_{out} performance of the stand-alone PA TEG at 60 GHz

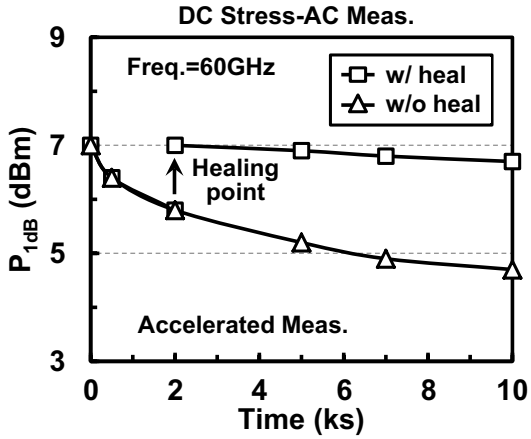


Figure 4.12: The measured $P_{1\text{dB}}$ of the PA (with and without HCI-healing) versus stress time at 60 GHz

transistor is damaged. When the PA is in HCI-healing status, V_{G6} and V_{PA} are connected to ground through S_{G6} and M_{n}, respectively. V_{GT} is off, and V_{H} is biased at a high voltage as introduced before. Table 4.2 summaries the statuses of the sub-blocks and switches at different operation modes of the PA.

The measured P_{in}-P_{out} performance of the stand-alone PA TEG at 60 GHz is shown in Fig. 4.11. The solid gray line is for undamaged fresh PA showing a 1-dB compression

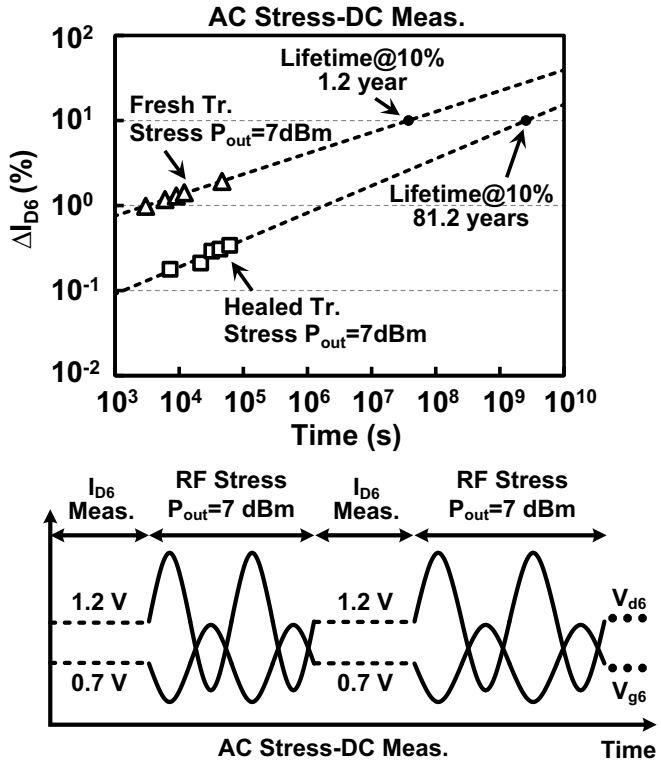


Figure 4.13: The measured I_{D6} degradation of the PA (before and after HCI-healing) versus stress time at 60 GHz

power (P_{1dB}) of 7 dBm. The accelerated DC stress (V_{DD6}=2.4 V) is applied to the last stage, which causes more than 1 dB degradation of P_{1dB}. After the HCI-healing function is enabled, a full recovery of the P_{1dB} can be observed. It also can be seen that the small-signal gain of the PA is not fully recovered because of small degradation in μC_{ox}.

The measured P_{1dB} of the PA (with and without HCI-healing) versus stress time is also depicted in Fig. 4.12. The accelerated DC stress (V_{DD6}) is used in the measurement. The measurement setup and procedure are illustrated in Fig. 4.11. It is shown that the P_{1dB} of the PA can be maintained near the undamaged value (7 dBm) when the HCI-healing technique is utilized.

The lifetime measurement results of the power amplifier are depicted in Fig. 4.13 with the drain current of the last stage (I_{D6}) measured under V_{G6}=0.7 V and V_{D6}=1.2 V. Two unstressed PA TEGs are used for the measurement. One is directly stressed using RF signal for lifetime measurement. The other one is firstly stressed using DC signal (V_{G6}=0.7 V and V_{D6}=2.4 V), which causes 20% reduction of saturation drain current. The RF stress lifetime measurement is conducted after the HCI healing is applied once. It can be observed that a lifetime of 81.2 years is achieved for the PA after the HCI-healing function

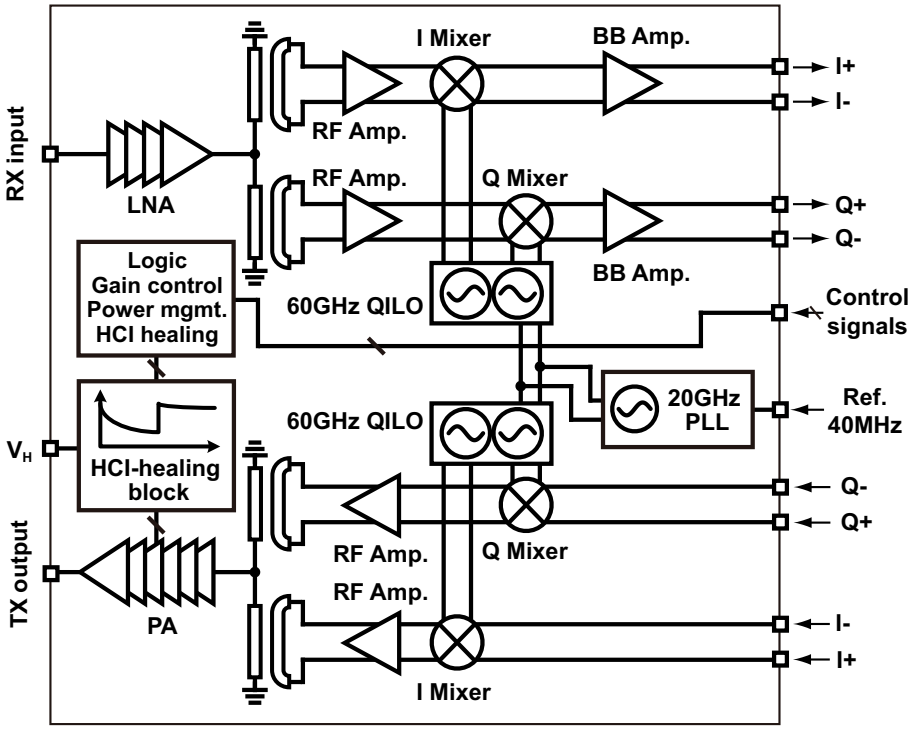


Figure 4.14: Block diagram of 60-GHz HCI-healing transceiver

is activated, which keeps outputting a 7-dBm continuous-wave signal. In a practical use, due to the large peak-to-average power ratio of the modulation signal, the HCI damage is smaller than that of the continuous-wave signal at 1-dB compression [48]. Therefore, one healing event is adequate during the lifetime of the device.

4.4 60-GHz HCI-Healing Transceiver

Fig. 4.14 shows the 60-GHz HCI-healing transceiver design using direct-conversion topology. The transmitter consists of the HCI-healing PA, RF amplifiers, I/Q passive mixers and a quadrature injection-locked oscillator (QILO). The receiver is composed of a 4-stage LNA, RF amplifiers, I/Q double-balanced mixers, baseband amplifiers, and a QILO. The carrier signal is generated through a 20-GHz PLL with a 40-MHz reference and the QILOs. The on-chip logic is integrated to achieve the gain control, power management, and HCI-healing function. The measured saturated output power (P_{sat}) of the transmitter is 11.3 dBm at the center frequency of 63.72 GHz excluding the PCB loss, and the $P_{1\text{dB}}$ is 6.3 dBm. The output power is measured by both a stand-alone PA and a transceiver chip integrated on a PCB. The PCB loss is estimated by calculating the difference between those saturated output powers.

Fig. 4.15 shows the measured EVM performance of the transmitter at different output

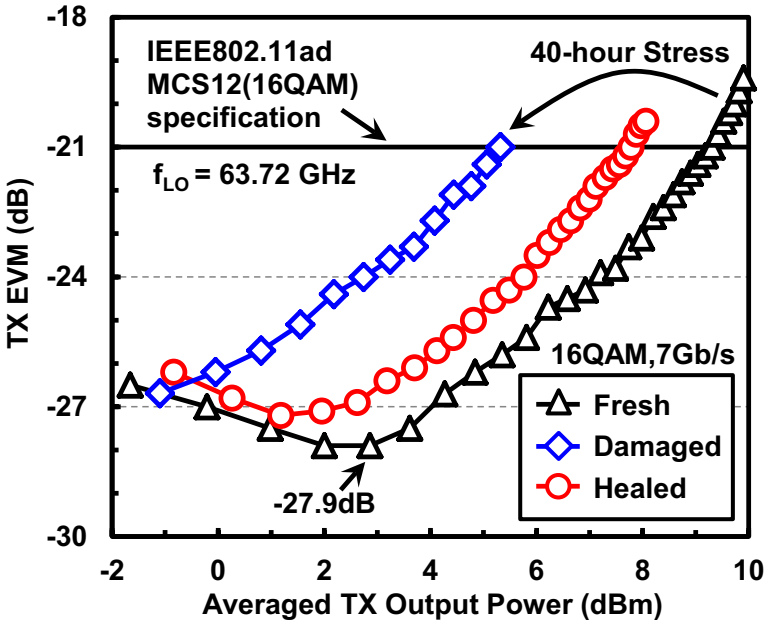


Figure 4.15: Measured TX EVM performance at different TX P_{out}

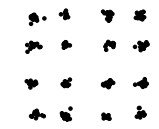
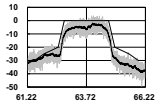
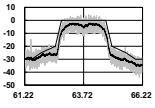
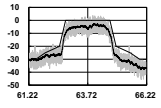
Modulation		16QAM		
Status		Fresh	HCI damaged	Healed
Data rate		7 Gb/s	7 Gb/s	7 Gb/s
Constellation				
Spectrum				
For same TX specification EVM=-21 dB	Tx P_{out}	9.3 dBm	5.3 dBm	7.8 dBm
	Tx-to-Rx EVM	-17.5 dB	-17.5 dB	-17.4 dB

Figure 4.16: The measured constellation and spectrum of the TX.

power. The carrier frequency of the modulated signal is 63.72 GHz. The symbol rate is 1.76 GS/s in 16QAM with a roll-off factor of 25%. The same PCB configured for TX mode is used in three different TX damaging statuses. The HCI damage is induced by using increased supply voltage of the board V_{DD} = 1.5V and saturated output power of P_{out}=12.5 dBm for 40 hours. It is shown that for the undamaged TX, the output power is 9.3 dBm when an TX EVM of -21 dB is achieved. After the HCI damage occurred, the

Table 4.3: Performance Comparison of 60-GHz CMOS transceivers.

Ref	Data rate (Modulation)	P_{out} (dBm) /each PA	TX efficiency P_{out}/P_{DC} (%)	CMOS (nm)	HCI healing	Core (mm^2)	Power consumption
[11]	28.16 Gb/s (16QAM)	8.5* @TX EVM=-21dB	2.8	65	NO	3.9	TX:251mW RX:220mW
[47]	2.6 Gb/s (QPSK)	6	3.0 w/o PLL	90	NO	3.4	TX:133mW RX:206mW
[10]	2.5 Gb/s (QPSK)	1.9 @TX EVM=-20dB	0.4	90	NO	5.7	TX:361mW RX:260mW
[15]	4.6 Gb/s (16QAM)	-4* @TX EVM=-23dB	0.5	40	NO	26.3†	TX:1190mW RX:960mW 16 × 16 array
[13]	2.6 Gb/s (QPSK)	N/A	N/A	65	NO	2.9	TX:160mW RX:233mW
[14]	2.5 Gb/s (QPSK)	2 @TX EVM=-22dB	0.5	90	NO	13.5†	TX:347mW RX:274mW
This work	7 Gb/s (16QAM)	9.3 @TX EVM=-21dB	3.9	65	**YES**	2.3	TX:218mW RX:188mW

* Estimated from literature † Chip area

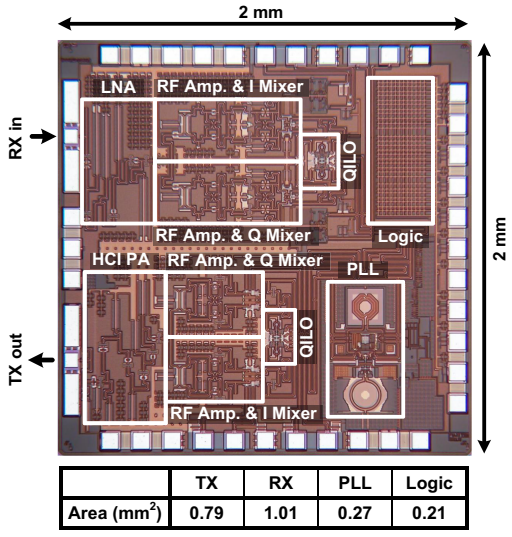


Figure 4.17: Die micrograph of the HCI-healing TRX.

output power of TX is reduced to 5.3 dBm for the same value of TX EVM. Finally the output power of TX are recovered to 7.8 dBm at TX EVM=-21 dB by activating the HCI-

healing function. The measured constellation and spectrum are also shown in Fig. 4.16.

Table 4.3 shows a comparison table for 60-GHz CMOS transceivers. This paper presents the first 60GHz transceiver with HCI-healing function, which guarantees over 81-year lifetime without sacrificing the output power and efficiency.

The proposed transceiver is fabricated in a 65 nm CMOS technology. The die micrograph is shown in Fig. 4.17. The core areas of the transmitter, receiver, PLL and control logic are 0.79 mm^2, 1.01 mm^2, 0.27 mm^2, and 0.21 mm^2, respectively.

4.5 Conclusions

This chapter presents a 60-GHz CMOS transceiver with hot-carrier-injection damage healing function by using charge ejection technique. The proposed transceiver achieves over 81-year lifetime without sacrificing the output power and efficiency. The transceiver demonstrates an EVM of -27.9 dB and can transmit 7 Gb/s in 16QAM within 2.16-GHz bandwidth. The front-end, fabricated in a 65 nm CMOS technology with a core area of 2.3 mm^2, consumes 214 mW and 184 mW from a 1.2-V supply in transmitting and receiving mode, respectively.

Chapter 5

60-GHz Wake-Up Receiver for Power Consumption Reduction

5.1 Introduction

60-GHz transceivers have been demonstrated to be one of the most promising candidates for short-range multi-gigabit-per-second wireless communications [12, 15]. However, even implemented in the low-power CMOS process, the power consumption of the 60-GHz transceiver front-end will be considerably large in order to overcome the large path loss at the 60-GHz band [63]. The power consumption of the baseband and digital-processing circuitry are not negligible due to the multi-Gb/s data rate and complex communication schemes such as orthogonal frequency division multiplexing (OFDM) and single-carrier frequency domain equalization (SC-FDE) [64]. Fig. 5.1 shows the power consumption breakdown for a typical 60-GHz CMOS transceiver with baseband circuitry from literature [65]. It can be observed that the total power consumption of the transceiver is over 900 mW, which means only this transceiver alone can drain a normal battery of a cell phone in several tens of hours, deteriorating the battery life and therefore user experience.

Obviously, for practical uses of the 60-GHz transceivers, a duty cycle control scheme as illustrated in Fig. 5.2 is necessary for systematic reduction of the power consumption over time. There are basically two types of schemes which can be used for the duty cycle control of the 60-GHz high-data-rate transceiver, as shown in Fig. 5.3.

One is called rendezvous scheme. The basic idea is to use a protocol-based built-in timer to turn on and off the 60-GHz high-data-rate transceiver periodically. Consequently, minimum extra components are required for the system, which also leads to low stand-by power consumption. Nevertheless, the rendezvous scheme generally has large latency

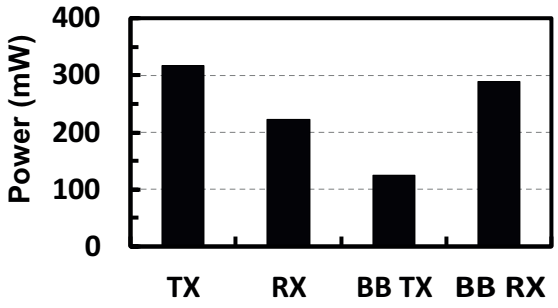


Figure 5.1: Power consumption breakdown of a a typical 60-GHz CMOS transceiver with baseband circuitry from literature.

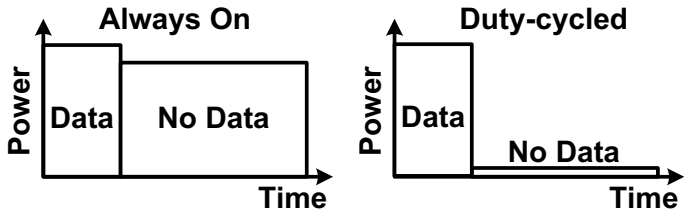


Figure 5.2: Conceptual illustration of the power consumption reduction by duty cycle control.

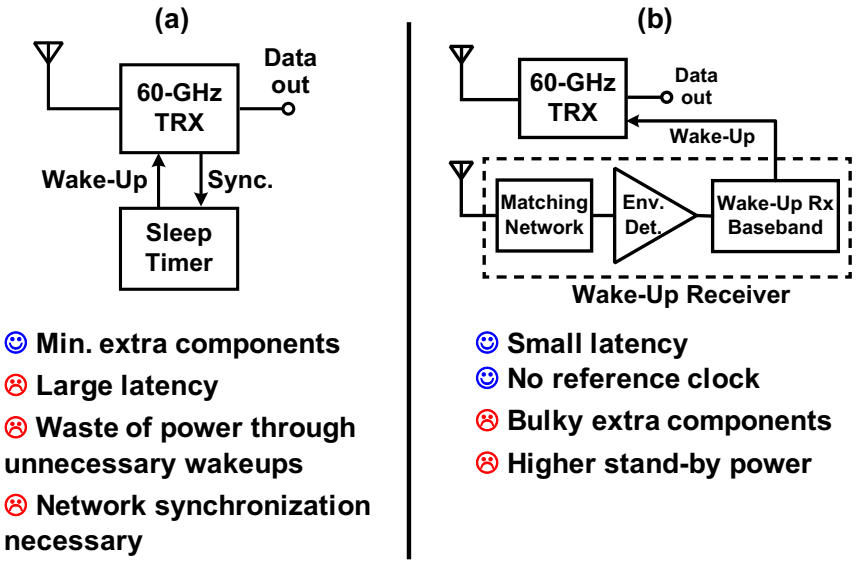


Figure 5.3: (a) Rendezvous scheme and (b) wake-up receiver for duty cycle control.

because of the protocol-based nature, which is not suitable for high-date-rate applications. Since the communication protocol can not guarantee the data transmitting and receiving

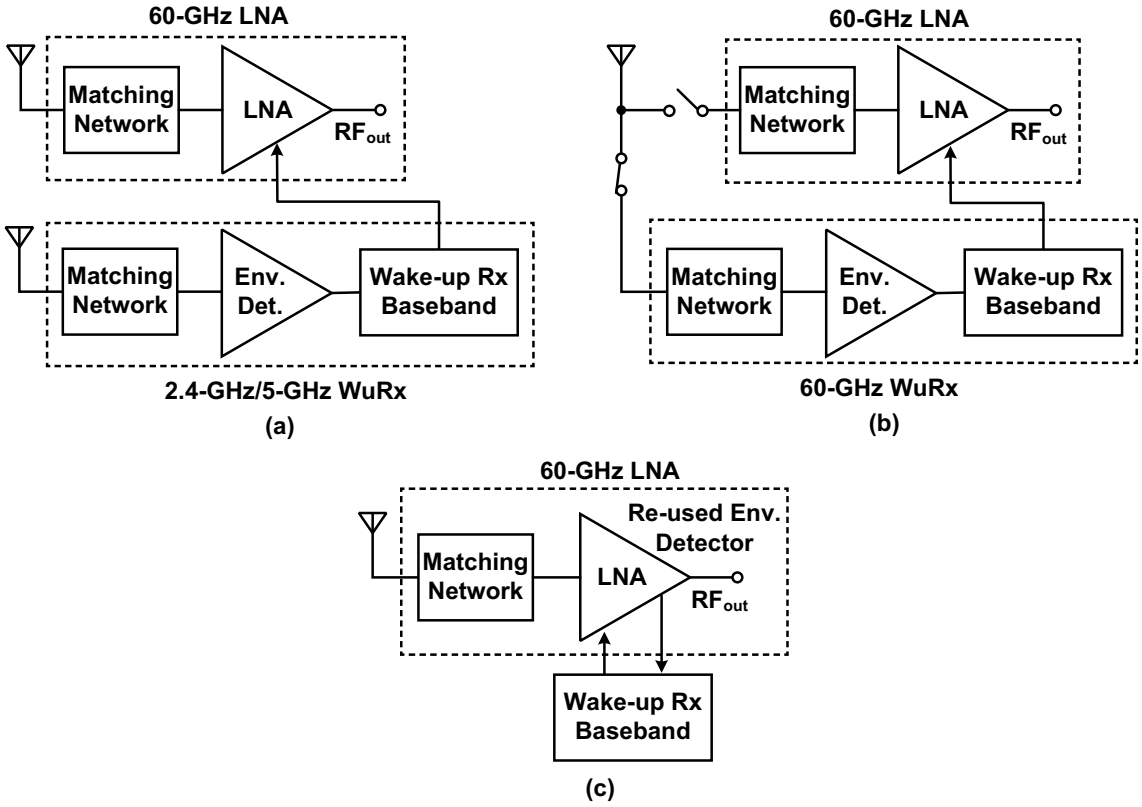


Figure 5.4: System block diagram of WuRxs for 60-GHz receivers (a) the general 2.4-GHz/5-GHz WuRx; (b) the general 60-GHz WuRx; (c) the proposed WuRx.

every time when the data transceiver is turned on, there is a large amount of waste power through unnecessary wake-ups. In addition, network synchronization is necessary for avoiding interference with other transceivers, which further increase the latency for data communication.

On the other hand, a wake-up receiver (WuRx), another solution for duty cycle control, has very small latency because of the radio-on-demand property. The wake-up receiver instead of the high-power transceiver is kept on monitoring the ”on” demand. Once the ”on” signal is received, the high-power transceiver will be turned on immediately, which is very suitable for high-data-rate applications. However, most of the reported WuRxs operate at low frequencies such as 2.4 GHz and 5 GHz [66–68]. Extra antennas and matching networks are required for adopting those WuRxs into the 60-GHz transceivers, which causes large area overhead, as shown in Fig. 5.4 (a). In addition, the low frequency bands (*e.g.* 2.4 GHz and 5 GHz) are becoming crowded as the use of various commercial wireless communication devices increases [67, 69]. It may need more power and area to overcome the interference in those frequency bands. Literature [70] indicates that the WuRx operating in 60-GHz band suffers less from the interference in the networks.

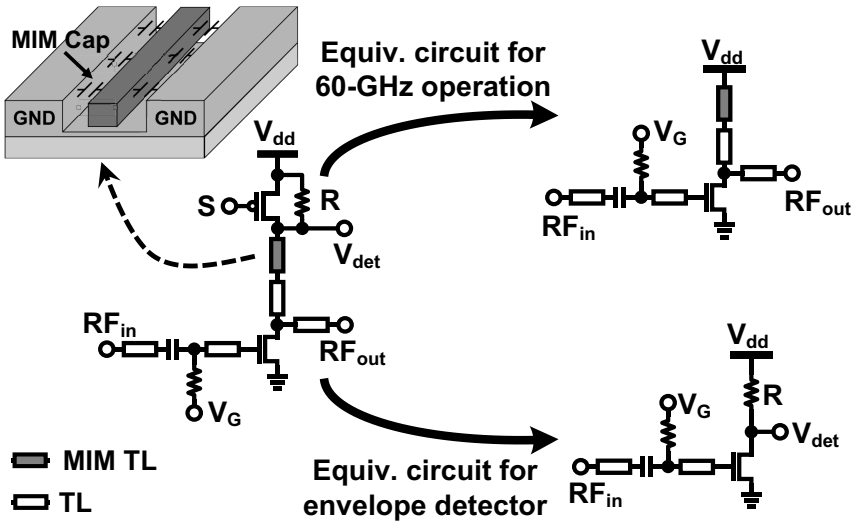


Figure 5.5: Schematic of the stage reused as the envelope detector

Unfortunately, the stand-alone envelop detector requires an extra input matching network if the WuRx is used for the 60-GHz high-speed transceivers. A bulky switch or matching network between the 60-GHz low-noise amplifier (LNA) and the WuRx is also required for achieving isolation of the two blocks shown in Fig. 5.4 (b).

In this chapter, a 60-GHz wake-up receiver with a reconfigurable 60-GHz LNA is presented as depicted in Fig. 5.4 (c) [71]. Because the gain stages of the 60-GHz LNA are reused as envelope detectors and pre-amplifiers, the bulky components mentioned above are eliminated in the circuit. Moreover, the sensitivity of the 60-GHz WuRx can be enhanced when several gain stages of the LNA are reconfigured as the pre-amplifier. The proposed WuRx fabricated in a 65-nm CMOS process occupies only $0.015\,\mathrm{mm}^2$ (excluding the LNA). The WuRx consumes $64\,\mu\mathrm{W}$ power from a 1-V supply achieving the sensitivity of $-46\,\mathrm{dBm}$. The sensitivity of the WuRx can be improved to $-60\,\mathrm{dBm}$ with the power consumption of $12.7\,\mathrm{mW}$ if several gain stages of the LNA are operated as the pre-amplifier.

5.2 Proposed 60-GHz Reconfigurable Wake-Up Receiver

5.2.1 The Reused Envelope Detector Stage

As mentioned above, the reusing of the LNA gain stages as the envelope detectors can greatly reduce the bulky components when the WuRx is integrated with the 60-GHz transceivers. However, the required circuit topology and bias of the envelope detector

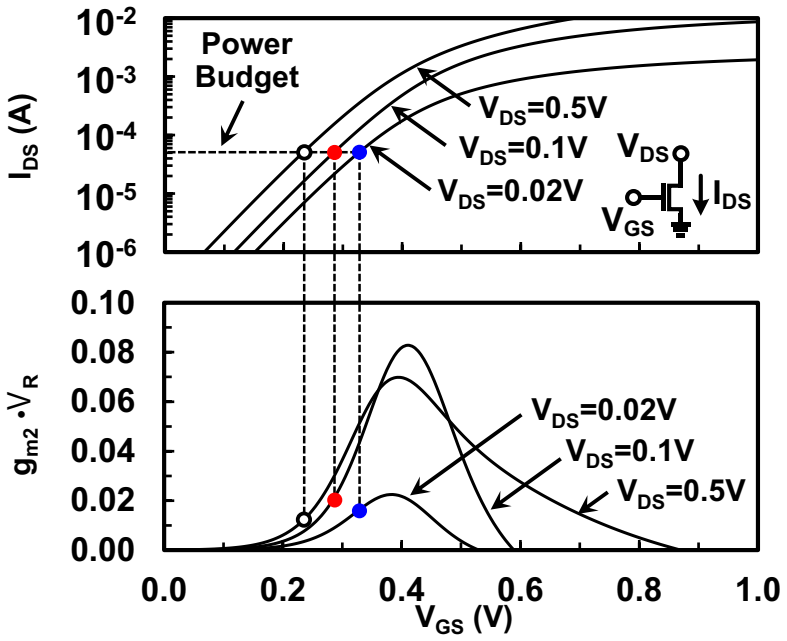


Figure 5.6: Illustration of the detector gain optimization

are different from those of the 60-GHz LNA. Therefore, some components are implemented to reconfigure the 60-GHz LNA stages. As shown in Fig. 5.5, a PMOS switch with a shunt resistor is inserted between the MIM transmission line and power supply port of the reused stage. When the reused stage is configured as a normal stage of the LNA, the switch is turned on. The switch with the shunt resistor exhibits low resistance, and will not affect the LNA performance. When the reused stage is reconfigured as the envelope detector, the switch is off showing a required high resistance for the sub-threshold envelope detector.

The gain of the sub-threshold amplitude detector is crucial to the sensitivity of the wake-up receiver. The optimization of the bias voltages and load resistance under a certain power budget is desired to achieve maximum gain. It is known that the voltage gain of detector (G_{det}) is proportional to the product of the load resistance (R_{det}) and the second-order nonlinearity coefficient of the transconductance (g_{m2}), as shown in Eq. 5.1.

$$\begin{aligned} G_{\mathrm{det}} &\propto g_{\mathrm{m2}} \cdot R_{\mathrm{det}} = g_{\mathrm{m2}} \cdot V_{\mathrm{R}}/I_{\mathrm{DS}} \\ &\propto g_{\mathrm{m2}} \cdot V_{\mathrm{R}} = g_{\mathrm{m2}} \cdot (V_{\mathrm{DD}} - V_{\mathrm{DS}}) \end{aligned} \tag{5.1}$$

where $V_{\mathrm{R}} = V_{\mathrm{DD}} - V_{\mathrm{DS}}$ is the voltage drop across the load resistor. I_{DS} is the bias current of the detector. It is shown that under a certain power budget (fixed I_{DS}), G_{det} is proportional to $g_{\mathrm{m2}} \cdot V_{\mathrm{R}}$. Therefore, the optimum values of bias voltages and load resistor for

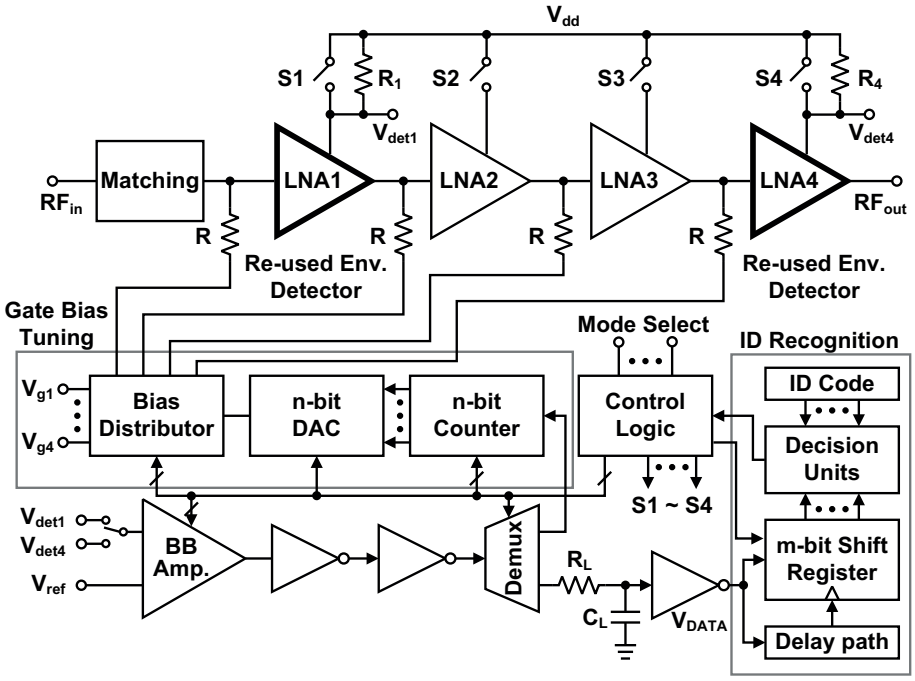


Figure 5.7: The detailed system block diagram of the proposed WuRx.

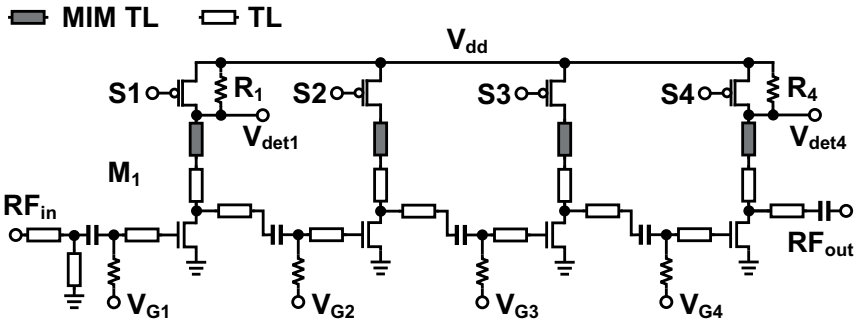


Figure 5.8: The detailed schematic of the 4-stage single-ended LNA.

maximization of G_{det} can be found out by plotting the I_{DS}–V_{GS} and $g_{\mathrm{m2}} \cdot V_{\mathrm{R}}$–$V_{\mathrm{GS}}$ curves at different values of V_{DS}, as depicted in Fig. 5.6.

5.2.2 The 60-GHz Wake-Up Receiver System

The system block diagram of the 60-GHz wake-up receiver with the reconfigurable 4-stage LNA is shown in Fig. 5.7. The whole system is composed of a 4-stage 60-GHz LNA (shown in Fig. 5.8), a gate bias tuning block, a baseband amplifier, an ID recognition block and a control logic block. The first and fourth stage of the 60-GHz LNA are reused

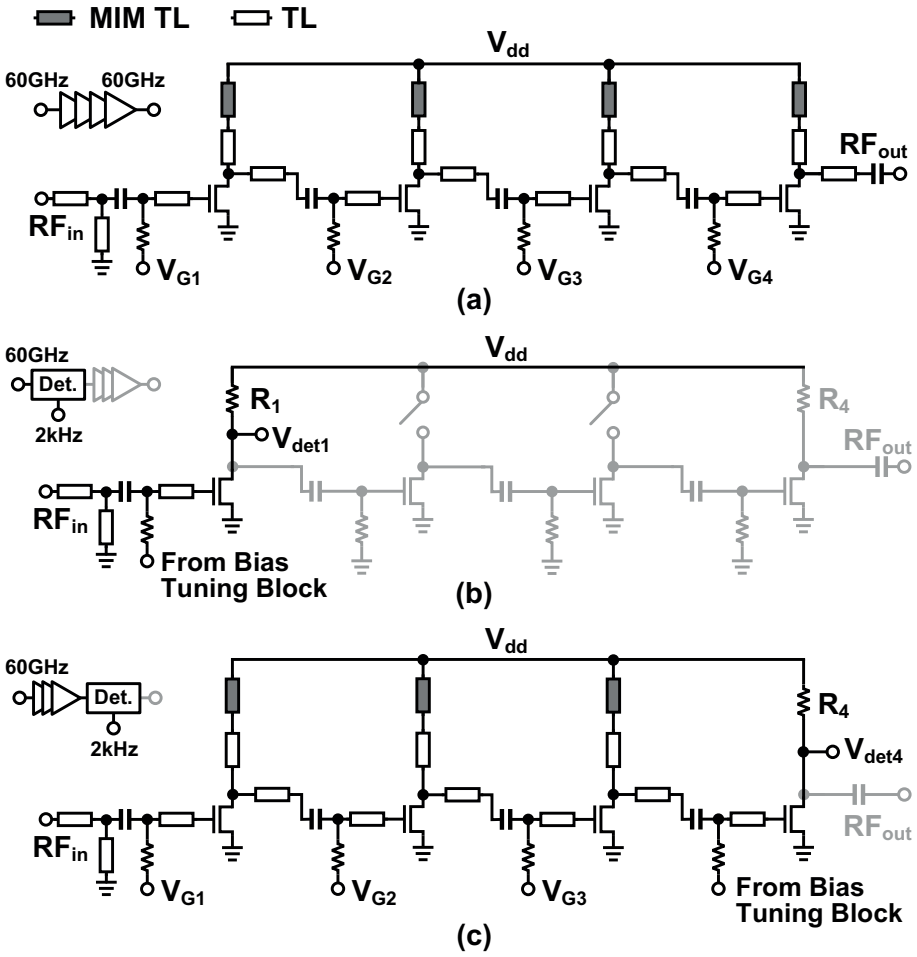


Figure 5.9: The equivalent circuit schematic of the 4-stage LNA in (a) normal operation mode; (b) low-power WuRx mode; (c) sensitivity-boosted WuRx mode.

as the envelope detectors for the WuRx. The gate bias tuning block is cooperating with the baseband amplifier to adjust the initial gate biases of the envelope detectors and provide proper gate bias voltages for other gain stages of the LNA. The ID recognition block is utilized to avoid false wake up. The control logic block is designed to switch on/off the circuit components according to the mode selection word.

When the reused stages are configured as a normal stage of the LNA, the switches are turned on. The equivalent circuit schematic of the 4-stage LNA in normal operation mode is shown in Fig. 5.9 (a). When the reused stages are reconfigured as the envelope detector, the switches are off showing a required high resistance for the envelope detector as depicted in Fig. 5.9 (b) and (c). Then the gate bias tuning block cooperating with baseband amplifier is turned on to automatically set the sub-threshold operation point for the envelope detector. Once the sub-threshold bias of the envelope detector is fixed, the

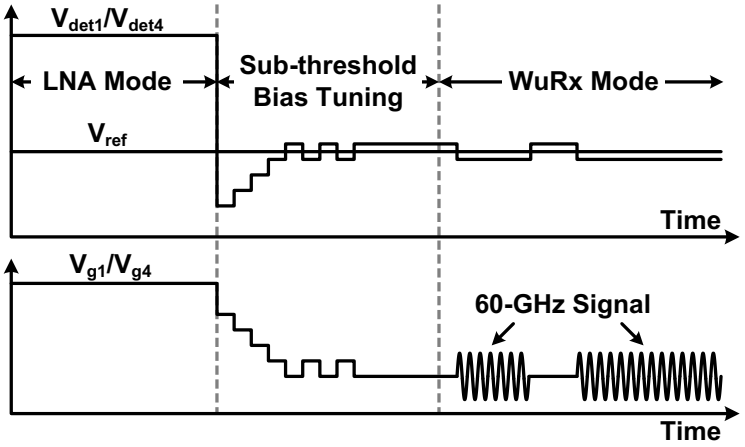


Figure 5.10: The conceptual transient voltage waveform of the WuRx.

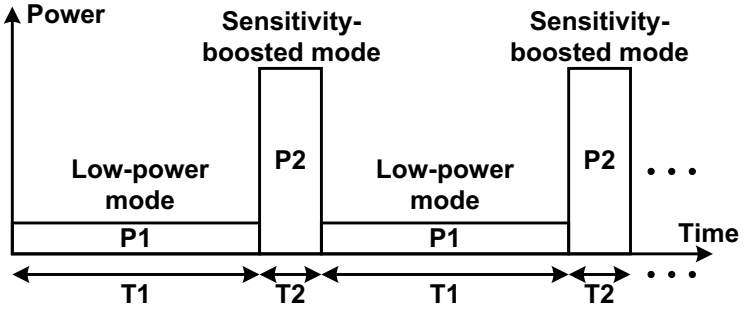


Figure 5.11: The simplified duty cycle scheme of the dual-mode WuRx.

baseband amplifier will be disconnected from the gate bias tuning loop by the demux. The WuRx is detecting the wake-up signal afterwards. The conceptual transient voltage waveform of the WuRx operation is illustrated in Fig. 5.10. To avoid false wake up, the ID recognition block.is implemented and connected to the output of the baseband amplifier during the detection period. If the received digital sequence is the same as the pre-stored ID code, the decision units will output ”1” configuring the LNA back to normal operation mode.

It is worthy of noticing that the WuRx has two operation modes. In the low-power mode, only the first stage of the LNA is reused as the sub-threshold envelop detector, other 3 stages are turned off as illustrated in Fig. 5.9 (b). In the sensitivity-boosted mode, the first 3 stages of the LNA are used as a pre-amplifier. The fourth stage is the envelope detector shown in Fig. 5.9 (c). It may be doubted that the improvement of the sensitivity is achieved at the cost of large power consumption. Fortunately, the power consumption of the WuRx can be easily controlled by arranging the duty cycle of the two operation

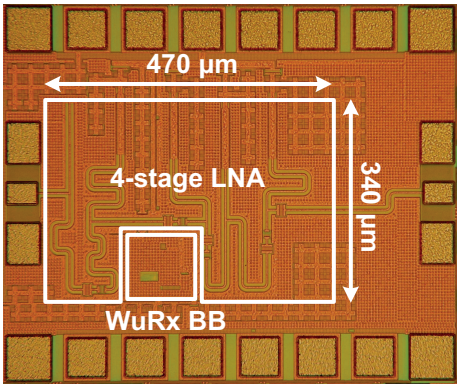


Figure 5.12: Die micro-photograph. WuRx: 0.015 mm^2 (excluding the LNA).

modes. Fig. 5.11 shows a simplified duty cycle scheme for the dual-mode operation. The average power consumption can be calculated by the following equation.

$$\text{Average Power} = \frac{\text{T1} \times \text{P1} + \text{T2} \times \text{P2}}{\text{T1} + \text{T2}} \tag{5.2}$$

For the 60-GHz LNA design, a transmission line (TL) with 1 dB/mm loss around 60 GHz is used for matching networks. An MIM transmission line (MIM TL) is employed for the de-coupling of the power supplies [57]. The schematic of the 4-stage single-ended LNA is shown in Fig. 5.9 (a). The channel widths of the transistors from input to output terminal are 1.5×24 μm, 1.5×24 μm, 2×20 μm, and 2×20 μm, respectively. The multi-stage gain peaking technique [57] is adopted for realizing wide and flat gain characteristics which is desired for 60-GHz high-speed wireless communications. The input and inter-stage matching networks are carefully designed for achieving reasonable reflection at the RF_{in} terminal for both LNA and WuRx operation modes.

5.3 Measurement Results

To verify our design, the proposed WuRx with the reconfigurable 4-stage LNA is fabricated in a 65 nm CMOS technology. Fig. 5.12 shows the die micro-photograph of the whole system. The area overhead of the proposed WuRx is only 0.015 mm^2 thanks to the reconfigurability of the LNA. The chip is measured on wafer using probe station. The measured input reflection coefficient (S11) of the WuRx at the terminal RF_{in} is depicted in Fig. 5.13. The S11 is around -10 dB at the frequency band of interest for both low-power mode and sensitivity-boosted mode.

Fig. 5.14 shows the measurement results of the S parameters when the system is op-

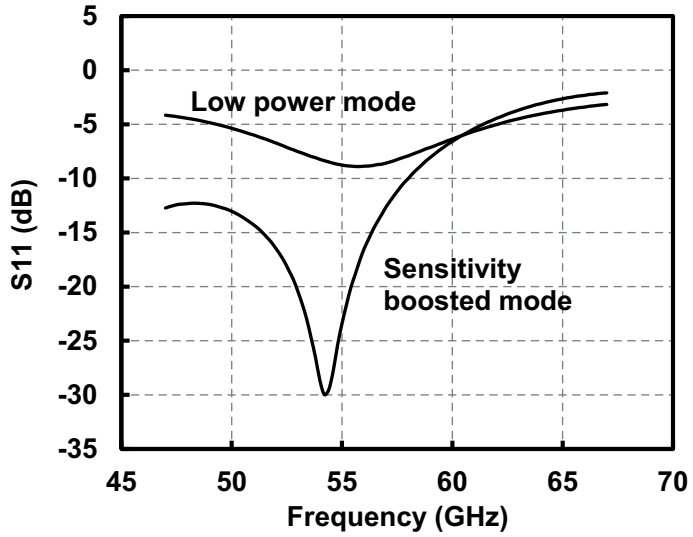


Figure 5.13: The measured input reflection coefficient of the WuRx at two different operation modes.

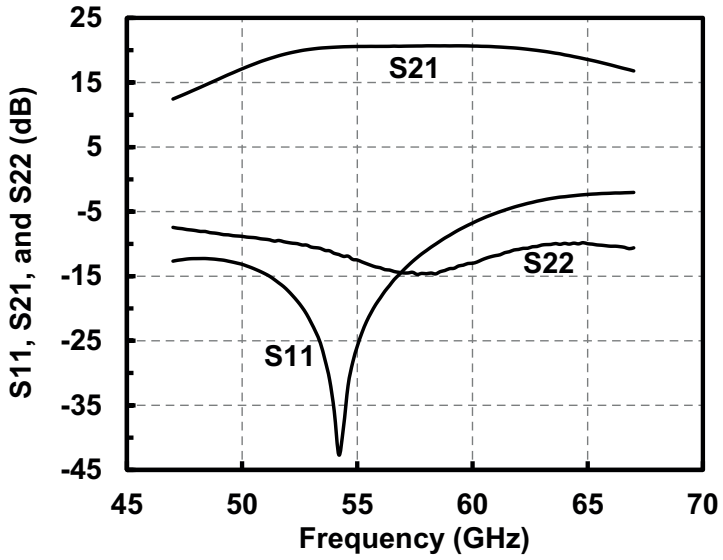


Figure 5.14: The measured S parameters of the 4-stage LNA.

erated as a 4-stage 60-GHz LNA. The peak gain is 20.7 dB at 59 GHz with a power consumption of 17.5 mW from 1-V supply. The -3 dB-bandwidth is from 50.5 GHz to 66 GHz.

The sensitivity of the WuRx is characterized using a signal generator and an oscilloscope. The amplitude modulated 57-GHz signal is produced by the signal generator, which is fed to the input terminal of the WuRx (RF_{in}). A 2-kHz envelope signal is used in the measurement. The output terminal of the WuRx (V_{DATA}) is connected to the os-

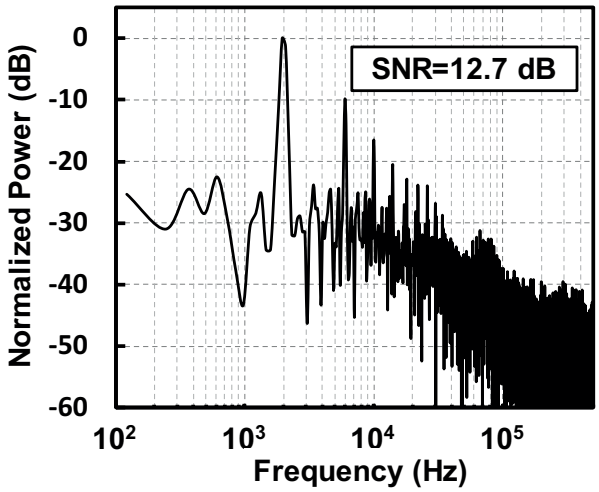


Figure 5.15: The measured spectrum of the received signal for P_{in}=−46 dBm (WuRx: low-power mode).

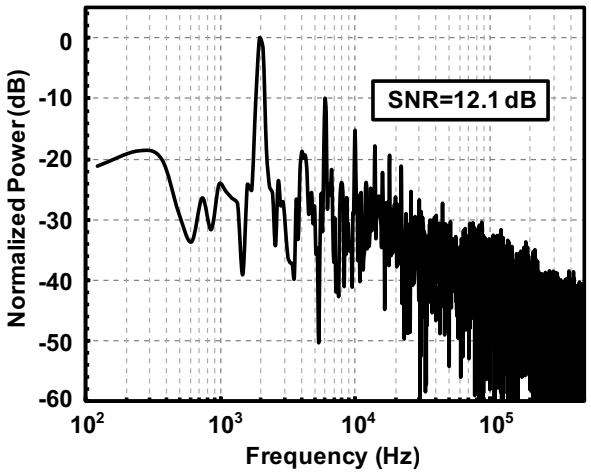


Figure 5.16: The measured spectrum of the received signal for P_{in}=−60 dBm (WuRx: sensitivity-boosted mode).

cilloscope through an external first-order band-pass filter (1 kHz-10 kHz). The received signal-to-noise ratio (SNR) is obtained from the data stored in the oscilloscope after Fast-Fourier Transform. The sensitivity of the WuRx is defined as the input power resulting a received SNR of 12 dB, which corresponds to the bit-error rate (BER) of 10^{-3} for amplitude-shift keying (ASK). The measured sensitivity of the WuRx is −46 dBm and −60 dBm with a power consumption of 64 μW and 12.7 mW, respectively. Fig. 5.15 and Fig. 5.16 demonstrate the measured spectrum of the received signal when the input power of the WuRx (P_{in}) is equal to −46 dBm and −60 dBm, respectively. As described in Section II-A, the average power consumption of the WuRx can be reduced to 77 μW if the

Table 5.1: Performance Comparison of the State-of-the-Art WuRxs in CMOS Processes.

Ref.	Frequency	Area Overhead	Extra Antenna/ Switch Required	False Detection	Sensitivity	Power
[66]	0.9 GHz	2.886 mm^2	Yes	Yes	−73 dBm	9 μW
[67]	5.8 GHz	0.114 mm^2*	Yes	Yes	−45 dBm	54 μW
[68]	0.915 GHz	0.36 mm^2	Yes	No	−80 dBm	51 μW
	2.4 GHz				−69 dBm	
[70]	60 GHz	1.09 mm^2	Yes	No	—†	9 μW
This work	60 GHz	**0.015 mm^2**	**No**	Yes	−46 dBm	64 μW
					−60 dBm	12.7 mW

* Estimated from literature † Only noise floor is shown

sensitivity-boosted mode is activated for 0.1% duty cycle.

Table 5.1 summarizes and compares the performance of the proposed WuRx with that of the state-of-the-art WuRxs in CMOS processes. The proposed WuRx shows the smallest area overhead and least requirement of extra bulky components with reasonable sensitivity and power consumption.

5.4 Conclusions

This chapter presents an area-efficient WuRx for 60-GHz high-speed wireless communication systems by reconfiguring the multi-stage LNA as envelope detectors. Due to the proposed reconfiguration technique, the WuRx requires an area overhead of only 0.015 mm^2 and does not need extra bulky components to be integrated with the 60-GHz transceivers. The WuRx also achieves the sensitivity of −46 dBm and −60 dBm with a power consumption of 64 μW and 12.7 mW, respectively. The average power consumption of the WuRx can be easily regulated by the duty cycle control technique.

Chapter 6

Ultra-Low-Power 60-GHz Transmitter with On-Chip Antenna

6.1 Introduction

With the continuous increase of the required number and bandwidth of internal I/Os in today's portable electronic systems, conventional electrical wireline interconnections among SoCs are limiting the design flexibility, integration level, system performance and reliability [72, 73]. Optical interconnections have been introduced to solve the issues of the electrical wireline interconnections, such as wideband matching, signal integrity, electro-magnetic interference, and frequency-dependent losses [74]. Nevertheless, it is difficult to realize the necessary optical-electrical and electrical-optical conversion devices in silicon processes, which degrades the connection flexibility and integration level, and increases implementation cost. Capacitive [75, 76] and inductive [77, 78] coupling interconnections have been reported to achieve high data rate, small chip size, and low power consumption. However, those techniques have very limited communication distance (less than 100 μm) with stringent requirement for the positioning of the couplers.

A millimeter-wave intra-connect using antennas as illustrated in Fig. 6.1 is one of the most promising candidates for the short-range internal communication (*e.g.* chip-to-chip) due to the potentials for flexible connection, high data rate, low power consumption, and integrated on-chip antennas. The possible electro-magnetic interference is also small because the propagation loss of the millimeter wave is inherently large. The transmitter in [73] shows a 10.7-Gb/s 60-GHz data link in CMOS technology, but this solution is power hungry due to the existence of the active modulator and buffers. Furthermore, an off-chip antenna is adopted for the system because of the intrinsic low gain of the CMOS on-chip antenna, which dramatically increases circuit size and introduces parasitic components.

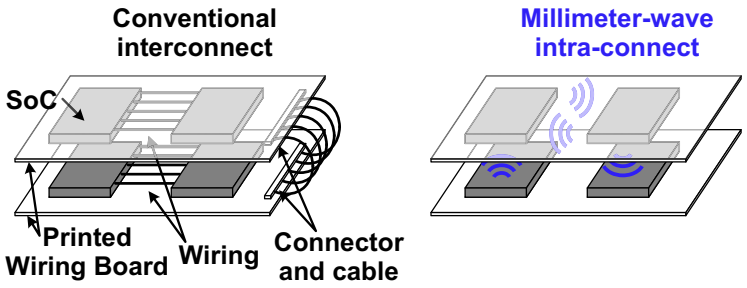


Figure 6.1: Millimeter-wave intra-connect using antennas.

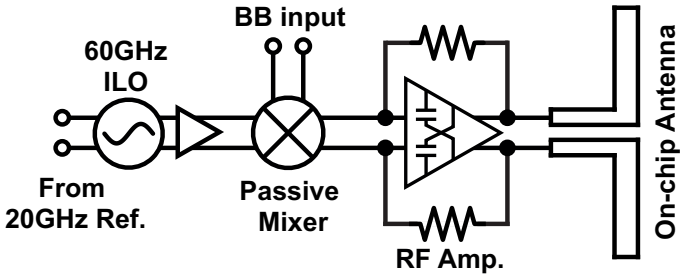


Figure 6.2: System block diagram of the proposed 60-GHz fully-integrated transmitter.

Literature [79] demonstrates a fully integrated 60-GHz transmitter with 2.2-Gb/s data rate. However the use of switched pulse-injected oscillator limits the communication data rate. A phased-array 60-GHz transmitter [80] is realized to overcome the intrinsic low gain of the CMOS on-chip antenna achieving over 10-Gb/s data rate.

This chapter presents a 60-GHz low power multi-Gb/s transmitter with a gain-enhanced on-chip antenna fabricated in a 65-nm CMOS technology [81]. An average radiation gain of -3 dBi for the on-chip antenna is achieved by using the helium-3 ion irradiation technique. The wideband and power-saving design of the transmitter core implements the high-data-rate communication with low power consumption. The proposed transmitter demonstrates a short-range communication (<2 mm) at a data rate of 5 Gb/s with a core area of 0.64 mm^2 (including the on-chip antenna) while consuming only 17 mW of power.

6.2 Transmitter Architecture and Link budget

The system block diagram of the proposed fully integrated 60-GHz transmitter is shown in Fig. 6.2. The whole transmitter is composed of an on-chip dipole antenna, a resistive-feedback RF amplifier, a double-balanced passive mixer, and an injection-locked oscillator (ILO). The ILO generates a 60-GHz local oscillator (LO) signal from a 20-GHz

Table 6.1: Link Budget for Short-Range High-Speed Communication

Carrier frequency	60 GHz	60 GHz
Distance	5 mm	2 mm
LOS loss	−22 dB	−14 dB
TX/RX antenna gain	−5 dBi	−5 dBi
Bandwidth	10 GHz	5 GHz
Thermal noise	−74 dBm	−77 dBm
NF	10 dB	10 dB
Required SNR	6.8 dB	6.8 dB
Implementation loss	−2 dB	−2 dB
Required $P_{\text{out,min}}$	−23.2 dBm	−34.2 dBm

reference. The LO signal is modulated by the baseband (BB) signal in the passive mixer. The modulated signal is amplified by the RF amplifier and radiated through the on-chip antenna. Because the topology of the resistive-feedback RF amplifier combined with the passive mixer is chosen for the transmitter, the wideband matching for both the baseband and RF port can be easily achieved with low power consumption. The gain of the CMOS on-chip antenna, which is inherently poor due to the low resistivity of the CMOS substrate, is improved by using the helium-3 ion implantation technique [81–83].

Table 6.1 shows an example link budget of the proposed transmitter with different communication distance and bandwidth. The line-of-sight (LOS) loss at 60-GHz is about −22 dB and −14 dB for 5-mm range and 2-mm range, respectively. The channel thermal noise is −74 dBm and −77 dBm with a signal bandwidth of 10 GHz and 5 GHz, respectively. The gain of the on-chip antenna is assumed to be −5 dBi for both the transmitter and receiver. A noise figure of 10 dB is also presumed for the receiver. The required signal-to-noise ration (SNR) is 6.8 dB for BPSK modulation achieving a bit error rate (BER) of 10^{-3}. An implementation loss of −2 dB is used to estimate the loss between the receiving on-chip antenna and the external receiver. Therefore, the required minimum output power of the transmitter is −23.2 dBm and −34.2 dBm, respectively.

6.3 60-GHz CMOS On-Chip Antenna

In 60-GHz band, the connections between RF circuits and off-chip antennas introduce parasitic components and radiation loss, which deteriorates the circuit performance and

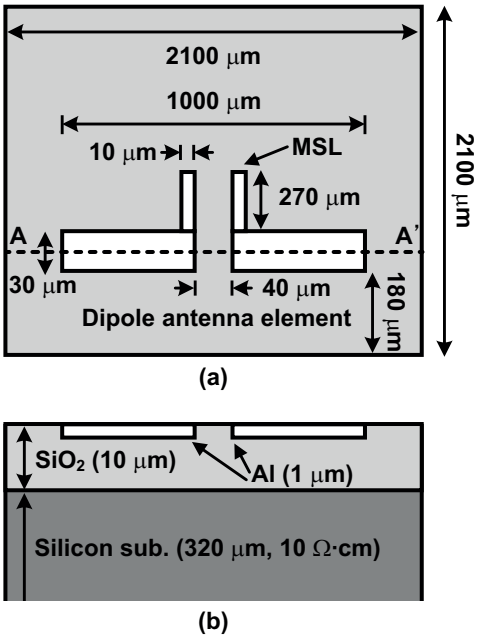


Figure 6.3: The analysis model of an on-chip dipole antenna (a) top view with antenna configuration; (b) A-A' cross-section view.

design flexibility [84]. Moreover, the off-chip antennas largely increase the device size and degrade monolithic integrity. Fortunately, on-chip antennas do not suffer from the issues mentioned above. However, the CMOS on-chip antenna normally has poor radiation gain and efficiency due to the low resistivity of the lossy silicon substrate used in CMOS technologies [85].

In order to gain a quantitative insight for the loss contribution, an analysis model of an on-chip dipole antenna is constructed in Ansys HFSS Ver.11 as depicted in Fig. 6.3. The dipole antenna instead of an end-fire type antenna is chosen in this work. Because the dipole antenna normally requires less chip area. Moreover, the dipole antenna has broader beamwidth, which is suitable for the communication with different chips (*e.g.* with the chips in vertical direction and in horizontal direction). The top metal layer (Al) with 1 μm thickness is used for the dipole elements which are fed by two micro-strip lines (MSLs). The silicon substrate (ε_r = 12) is modeled by a lossy layer with resistivity of 10 Ω·cm and 320-μm thickness. The detailed dimensions of the antenna are illustrated in Fig. 6.3. Fig. 6.4(a) shows the HFSS simulated radiation gain pattern of the dipole antenna at 60 GHz using the model described in Fig. 6.3. The radiation gain at X direction with $\varphi = 0^\circ$ is −8.2 dBi which corresponds to an efficiency of 26%. It is interesting to note that the silicon substrate contributes around 70% of losses. Therefore, reducing the substrate loss is an effective solution to improve on-chip antenna efficiency and power gain.

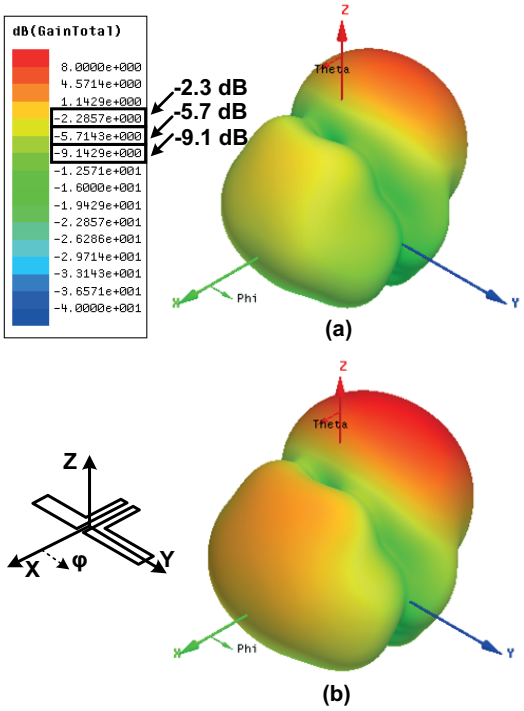


Figure 6.4: The simulated 3-D gain pattern of the on-chip antenna (a) with lossy substrate (10 Ω·cm); (b) with high resistivity substrate (1000 Ω·cm).

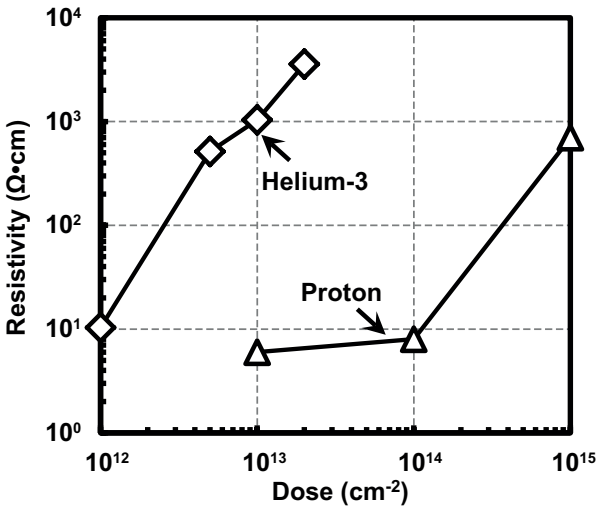


Figure 6.5: The measured resistivity of the n-type substrate versus the dose amount for helium-3 ion implantation and proton bombardment.

Much research has been conducted to improve the radiation gain and efficiency of the CMOS on-chip antennas. Literature [86] and [87] successfully reduce the substrate loss

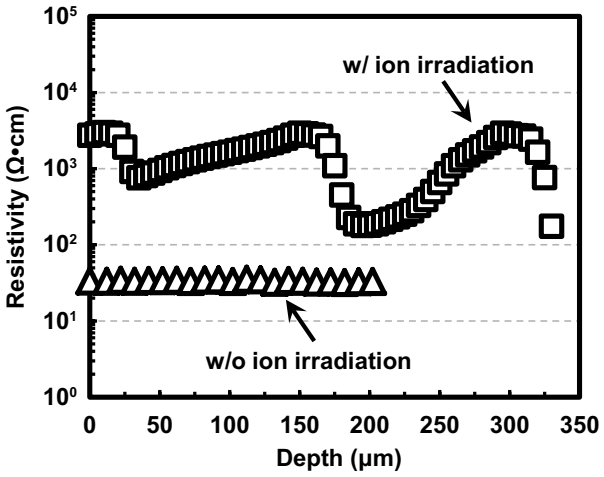


Figure 6.6: The measured resistivity of the CZ-P wafer substrate at different depth with and without helium-3 ion irradiation.

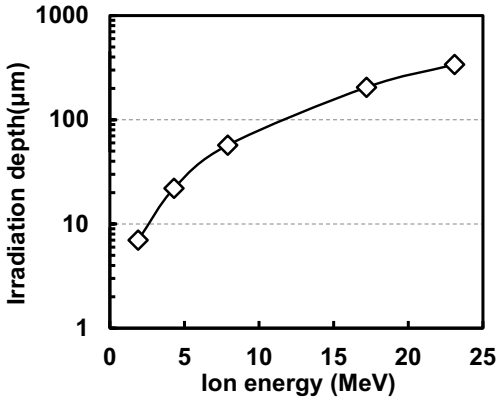


Figure 6.7: The calculated irradiation depth versus ion energy for helium-3 ion.

by using artificial magnetic conductor (AMC) at the cost of excessive chip area. Proton implantation techniques [88, 89] are very effective to increase the resistivity of the silicon substrate. Nevertheless, a high dose amount ($>10^{15}$ cm^{-2}) is usually required for the proton implantation, which results in less reliability and high process cost [90, 91].

In this chapter, a helium-3 ion implantation technique is used to enhance the on-chip antenna efficiency and power gain by effectively increasing the substrate resistivity. The helium-3 ions are implanted to the antenna chip using a cyclotron after the chip is fabricated. An aluminum mask plate with 0.5 mm thickness is used to protect the chip area outside of the ion-irradiated region. Due to charge trappings created by the irradiation and Coulomb scattering of the charged traps, the substrate resistivity increases with the

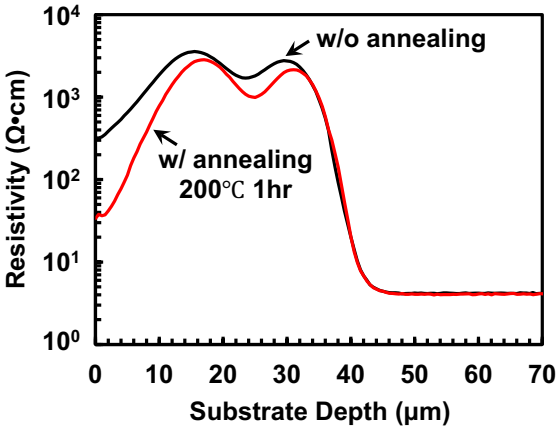


Figure 6.8: The measured resistivity of the CZ-P wafer substrate at different depth with and without annealing.

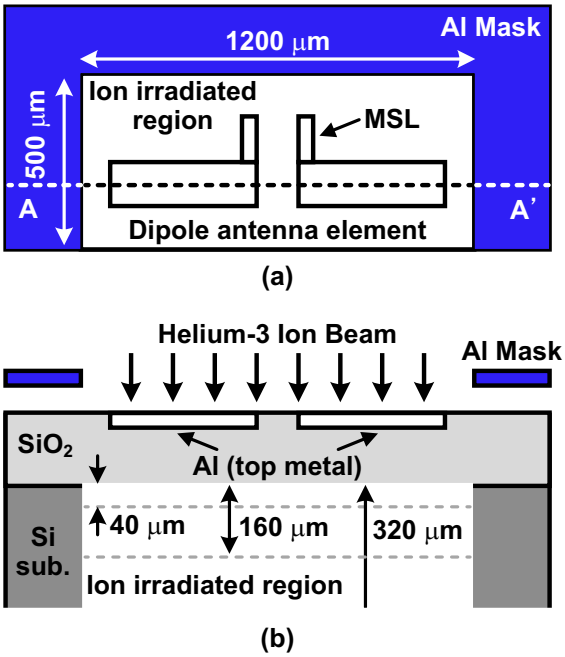


Figure 6.9: The proposed gain-enhanced on-chip dipole antenna (a) top view; (b) A–A' cross-section view.

increasing of the dose amount. Typically, the substrate resistivity at certain depth can be effectively increased from 4 Ω·cm to over 1000 Ω·cm with a small dose amount of 1×10^{13} cm^{-2} by utilizing the helium-3 ion implantation technique as demonstrated in Fig. 6.5 [83, 91].

To increase the resistivity of the whole substrate, the multiple-irradiation process is

normally required as illustrated in Fig. 6.6. A CZ-P bare wafer is used for the measurement. The helium-3 ions are bombarded to the depth of 13 μm, 160 μm, and 310 μm, respectively. The dose amount is 1×10^{13} cm^{-2} for each bombardment. It can be observed that an average resistivity of over 1000 Ω·cm is achieved within the 320-μm-depth substrate. The relationship between irradiation depth and ion energy for helium-3 ion calculated using ion-implantation simulator (SRIM) is also shown in Fig. 6.7 [92]. The influence of the annealing process on the resistivity of the ion irradiated substrate is shown in Fig. 6.8 [92]. The annealing condition is under the temperature of 200°C in 1 hour. There is no significant degradation of the substrate resistivity observed for the target depth.

Moreover, helium-3 ion has less lateral scattering compared with proton. The calculated beam spread range for helium-3 ion is about half of that for proton at 300-μm stopping range [83]. For the metal reliability with the helium-3 ion implantation technique, measurement results show that the resistance of the top metal in a 180 nm CMOS process only varies 0.5% after the implantation of the helium-3 ions, which is less than the process variation.

Therefore, a high-reliability low-process-cost ion implantation technique can be utilized to increase the substrate resistivity. Fig. 6.9 shows the proposed CMOS on-chip dipole antenna with helium-3 ion implantation technique. The antenna configuration is the same as in Fig. 6.3 except the 500 μm×1200 μm white area around the antenna indicates the ion irradiated region.

To further investigate the ion implantation technique, three different target depths of resistivity improvement (40 μm, 160 μm, and 320 μm) are applied to the on-chip antenna. HFSS simulation results demonstrate that the radiation efficiency is increased to 59% (gain = −4.5 dBi) when the target depth of 320 μm and the substrate resistivity of 1000 Ω·cm are applied as shown in Fig. 6.4(b).

6.4 Transmitter Front-End Design

The wideband characteristic and low power consumption are important for the design of 60-GHz wireless interconnect transmitter. However, a baseband input buffer, which achieves 50-Ω impedance matching, generally has a narrow-band characteristic with low power consumption.

In this work, the wideband input impedance matching is realized by using the double-balanced passive mixer and resistive-feedback RF amplifier as illustrated in Fig. 6.10. The wideband input impedance flatness of the RF amplifier is implemented by a resistive-feedback matching technique [50]. The input impedance of the RF amplifier (Z_{RF}) is down-converted to the baseband. The baseband input impedance (Z_{in}) is determined by

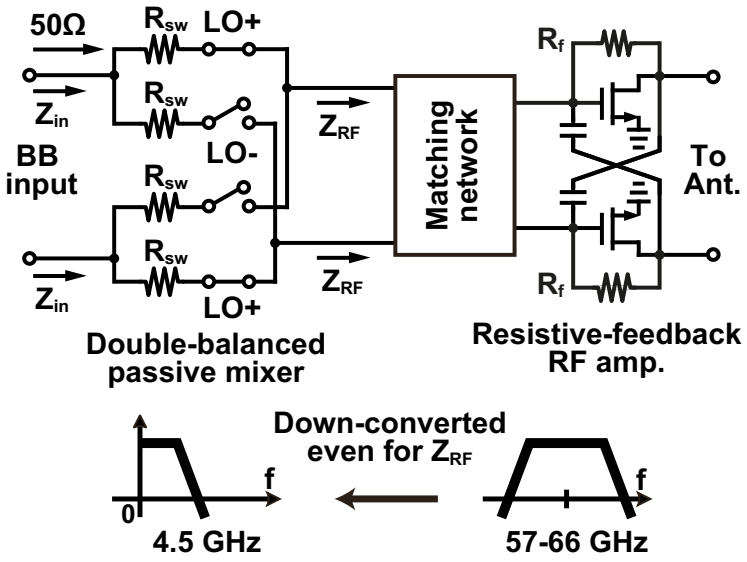


Figure 6.10: The topology of the double-balanced passive mixer and resistive-feedback RF amplifier.

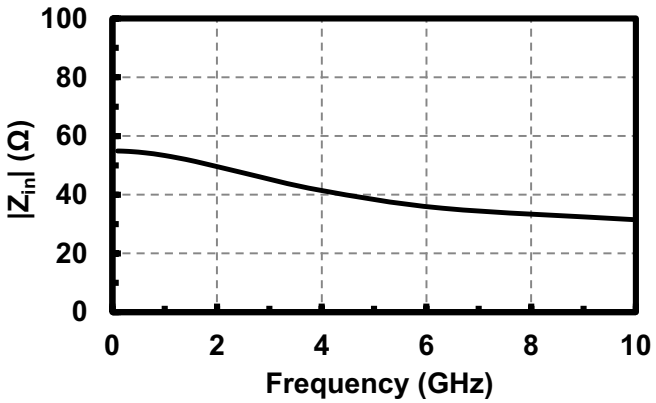


Figure 6.11: The simulated magnitude of the baseband input impedance ($|Z_{\text{in}}|$) versus frequency.

Z_{RF} and the on-resistance (R_{SW}) of the switches used for the passive mixer, which maintains the wideband matching for the baseband input.

$$Z_{\text{in}}(\omega) \approx R_{\text{SW}} + \frac{4}{\pi^2}\left[Z_{\text{RF}}(\omega_{\text{LO}} + \omega) + Z^*_{\text{RF}}(\omega_{\text{LO}} - \omega)\right] \tag{6.1}$$

Fig. 6.11 shows the simulated magnitude of the baseband input impedance ($|Z_{\text{in}}|$) at different frequencies. It is demonstrated that $|Z_{\text{in}}|$ remains around $50\,\Omega$ for about 5-GHz

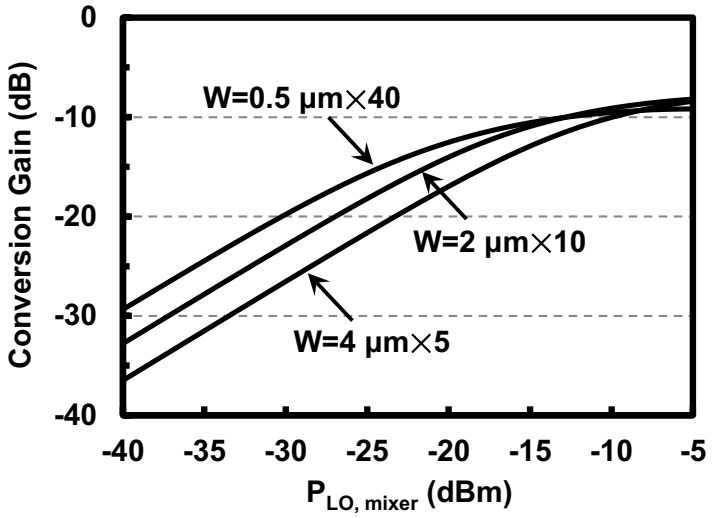


Figure 6.12: The simulated conversion gain of the mixer with f_{LO}=61.56 GHz and f_{BB}=0.1 GHz.

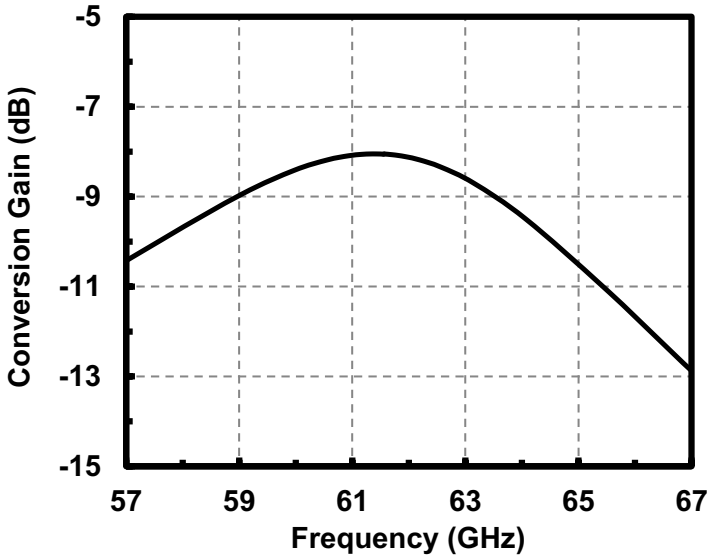


Figure 6.13: The simulated conversion gain of the passive mixer with RF amplifier at f_{LO}=61.56 GHz.

bandwidth.

The finger widths of the passive mixer switches are also optimized for reducing the required input power at the LO port of the mixer. It is known that the conversion gain of the passive mixer is proportional to the voltage amplitude at the gate terminal of the mixer switches [93]. Considering a sinusoidal waveform of the LO, the voltage amplitude (V_{LO})

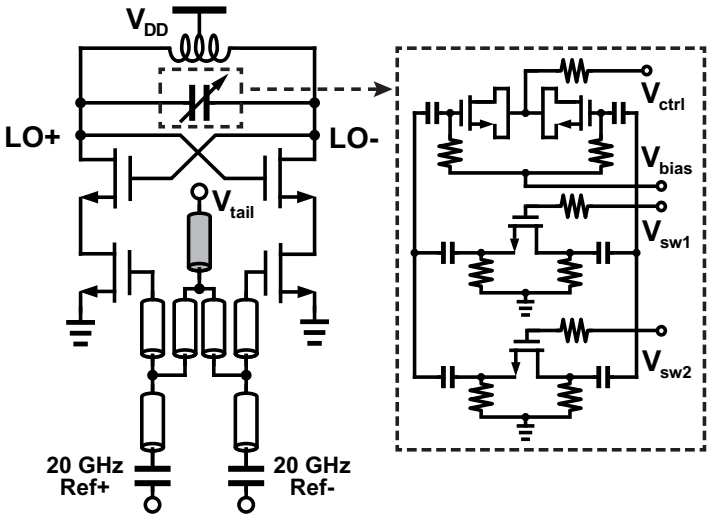


Figure 6.14: 60-GHz injection-locked oscillator topology.

can be expressed as

$$|V_{\mathrm{LO}}|^2 = P_{\mathrm{LO,\,mixer}} \times \frac{2|Z_{\mathrm{LO}}|^2}{Re\,[Z_{\mathrm{LO}}]} = P_{\mathrm{LO,\,mixer}} \times 2(R + \frac{X^2}{R}) \tag{6.2}$$

where $P_{\mathrm{LO,\,mixer}}$ is the input power at the LO port of the mixer. $Z_{\mathrm{LO}} = R + jX$ is the input impedance of the LO port. R is mainly contributed by the gate parasitic resistance of the switching transistor. While X is contributed by the gate parasitic capacitance of the transistor. Assume $R << |X|$, the second term of equation (6.2) increases with the decreasing of R. Therefore, the required $P_{\mathrm{LO,\,mixer}}$ for a certain conversion gain is reduced. Fortunately, the assumption of $R << |X|$ is normally satisfied with the typical transistor width of several tens of micrometers in the 60-GHz passive mixer. For example, the simulated result of the passive mixer with the transistor size of 4 μm×5 shows a $Z_{\mathrm{LO}} = 16 - j120\ \Omega$ at 61.56 GHz. Moreover, R is reduced with the decreasing of the finger width when the total transistor width is fixed. Theoretically, the smaller finger width is preferred with respect to reducing the required $P_{\mathrm{LO,\,mixer}}$.

Fig. 6.12 shows the simulated conversion gain (CG) of the passive mixer for different finger widths versus $P_{\mathrm{LO,\,mixer}}$. The LO frequency (f_{LO}) is 61.56 GHz, which is the center frequency of the 60-GHz band defined in IEEE 802.11ad standard. The baseband input frequency (f_{BB}) is 0.1 GHz. The total channel width is fixed to be 20 μm while the finger width is changed from 0.5 μm to 4 μm. It can be observed that the required $P_{\mathrm{LO,\,mixer}}$ for W=4 μm×5 is about 7 dB higher that for W=0.5 μm×40 at the conversion gain of −15 dB. In this design, a minimum finger width of 0.5 μm is chosen due to the transistor size

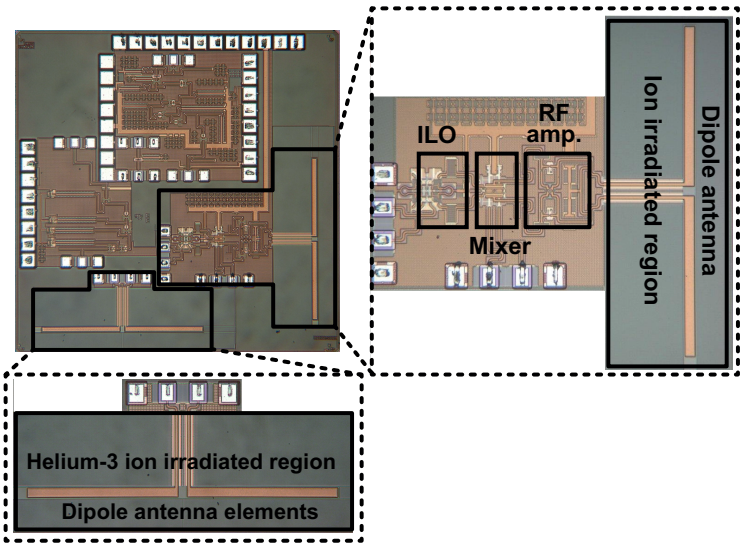


Figure 6.15: Die micro-photograph. Antenna area: 0.46 mm^2, TX core area: 0.18 mm^2.

limitation of the process design kit (PDK).

The simulated conversion gain of the passive mixer with the RF amplifier for both upper and lower sideband is shown in Fig. 6.13 with f_{LO}=61.56 GHz. The LO power is set to be −20 dBm. A conjugate matching is assumed between the LO and the passive mixer. The −3-dB bandwidth of the passive mixer with the RF amplifier is over 9 GHz as depicted in Fig. 6.13. The simulated power consumption of the resistive-feedback RF amplifier and the passive mixer are 8 mW and 0 mW, respectively. The local oscillator is realized by an injection-locked solution [12].

Fig. 6.14 shows the schematic of the 60-GHz injection-locked oscillator (ILO). A 2-bit capacitor array for coarse tuning and varactors for fine tuning are used to cover 58 GHz–65 GHz frequency range with a simulated power consumption of 10-mW.

6.5 Measurement Results

To verify our design, the proposed low power high speed 60-GHz transmitter with on-chip antenna is fabricated in a 65 nm CMOS technology. The stand-alone test chip for on-chip antenna characterization is also fabricated in the same die. Fig. 6.15 shows the die micro-photograph of the whole transmitter and the stand-alone antenna. The areas of the transmitter core and the on-chip antenna are 0.18 mm^2 and 0.46 mm^2, respectively.

There are two types of test chips. One type is post-processed by the helium-3 ion bombardment technique introduced in Section 3 over the region indicated in Fig. 6.15, while the other type has no ion-irradiated area. To investigate the influence of the resistivity-

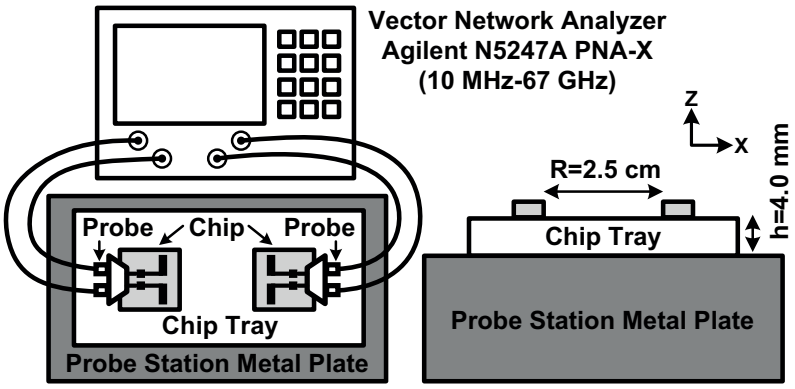


Figure 6.16: The illustration of the on-wafer measurement setup for the power gain of the on-chip antenna.

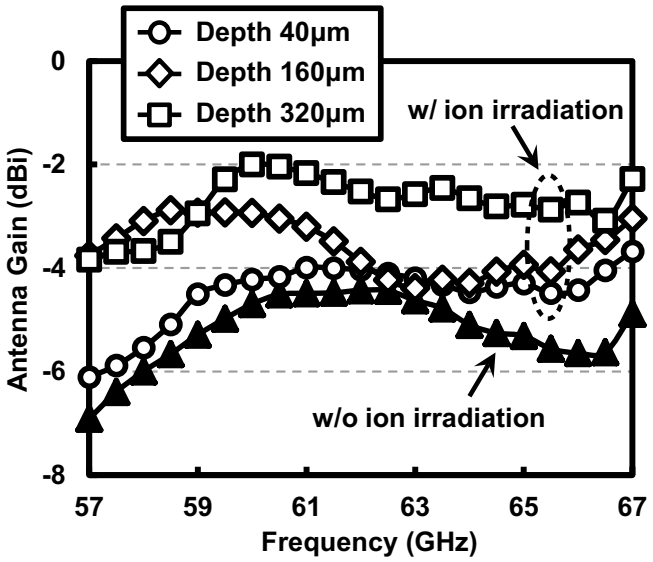


Figure 6.17: The measured antenna power gain with and without helium-3 ion irradiation.

improved substrate on the performance of the antenna, three different target depths (40 μm, 160 μm, and 320 μm) are applied to the on-chip antenna with helium-3 ion bombardment as illustrated in Fig. 6.9. The same dose amount of 3×10^{13} cm^{-2} is used in the three samples for fair comparison. As shown in Section 6.3, the substrate resistivity increases with the increasing of the dose amount. However, the process cost is also proportional to the dose amount. The dose amount used in this research is decided by considering the trade-off between the target substrate resistivity and process cost.

The power gain of the on-chip antenna is measured using the setup shown in Fig. 6.16. Two identical antennas located on the probe station are placed face-to-face with a distance R=2.5 cm. An air-filled plastic box (chip tray) with 4-mm height is used to lift the test

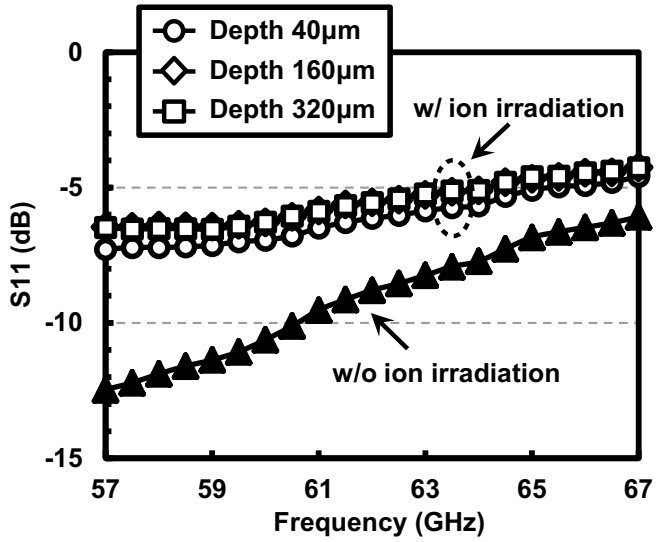


Figure 6.18: The measured S11 of the on-chip antenna with and without ion irradiation.

Table 6.2: Comparison with Previously Reported 60-GHz Band On-Chip Antennas.

Ref.	Process	Type of antenna	Frequency	Antenna gain	Core area
This work	65 nm CMOS	Dipole with helium-3 ion implantation	60 GHz	**−2.0 dBi**	**0.48 mm^2**
[80]	65 nm CMOS	Slot loop	60 GHz	−5.0 dBi†	0.64 mm^{2*}
[85]	180 nm CMOS	Yagi	60 GHz	−10.0 dBi	0.74 mm^{2*}
[86]	180 nm CMOS	Circularly polarized with AMC	65 GHz	−4.4 dBi	3.24 mm^2
[87]	90 nm CMOS	Yagi with AMC	60 GHz	−7.2 dBi	1.04 mm^2

* Estimated from literature † Not measured results

chip away from the metal plate, which alleviates the effects of the metal plate on the power gain of the on-chip antenna at X direction. The 4-mm height of the chip tray is determined by the spatial limitation of the probe positioner. The influence of the chip tray itself on the power gain of the on-chip antenna at X direction is negligible. The losses of the measurement equipments and cables are calibrated to the probe tips using standard impedance substrates. The power gain of one single antenna (G_{ante}) can be expressed as [85]

$$G_{\text{ante}}\,(\text{dB}) = \frac{1}{2}\,[\text{IL}\,(\text{dB}) - \text{PL}\,(\text{dB})] \tag{6.3}$$

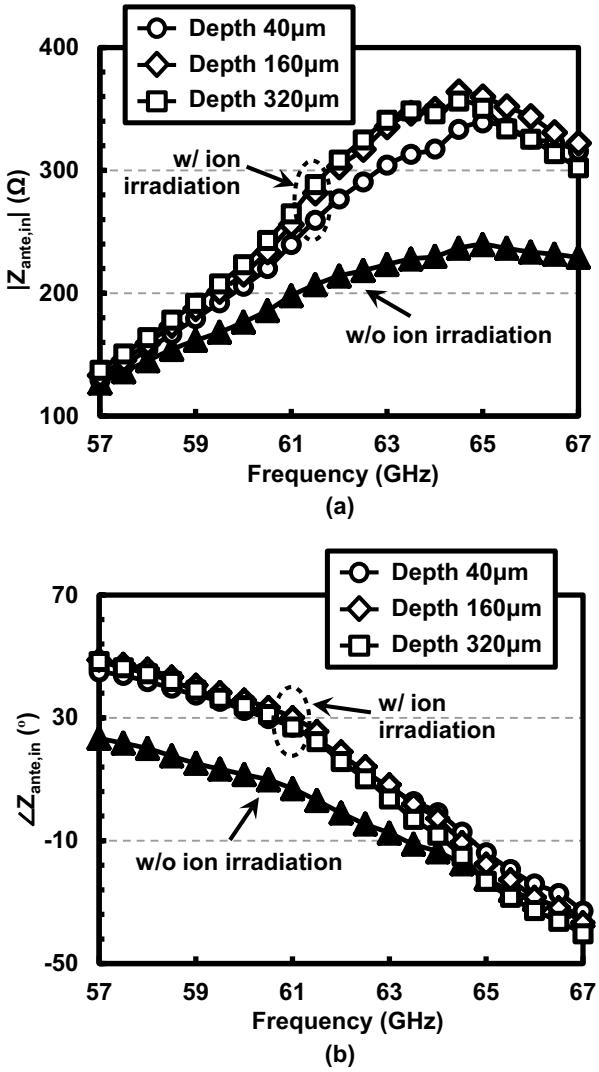


Figure 6.19: The measured differential mode (a) magnitude and (b) phase of the on-chip antenna input impedance.

$$\text{PL (dB)} = 10\log\left[\left(\frac{\lambda_0}{4\pi R}\right)^2 \times \left|1 - \frac{R}{\sqrt{R^2+4h^2}} e^{-ik_0\left(\sqrt{R^2+4h^2}-R\right)}\right|^2\right] \tag{6.4}$$

$$\text{IL (dB)} = 10\log\left(\frac{|S_{21}|^2}{1-|S_{11}|^2}\right) \tag{6.5}$$

where PL is the path loss considering the effect of the metal plate on the probe station. k_0 is equal to $2\pi/\lambda_0$. λ_0 is the wavelength in air. IL is the measured insertion loss between the two antennas from the vector network analyzer (VNA). The IL instead of S_{21} is used

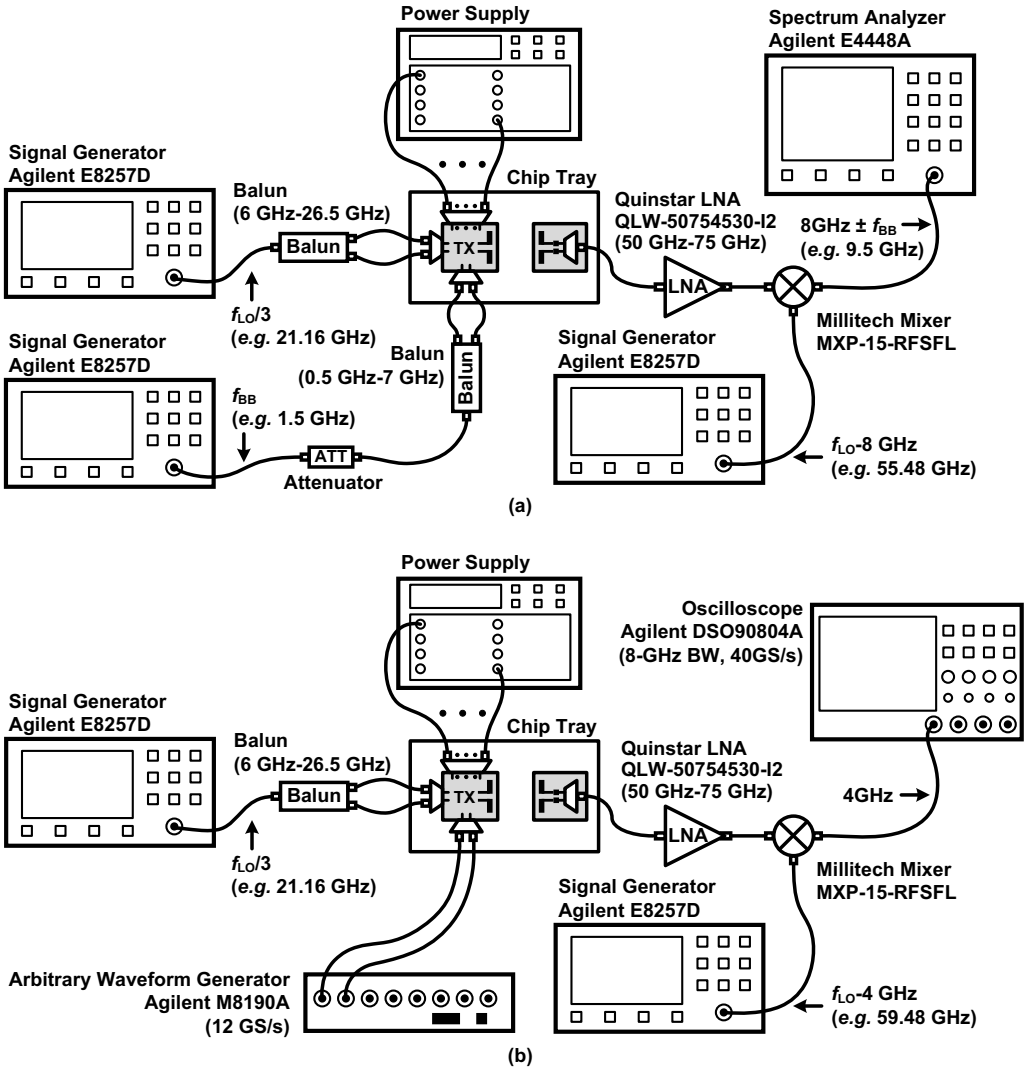


Figure 6.20: The illustration of the on-wafer measurement setup for (a) the conversion gain and output power of the transmitter; (b) digital modulation wireless transmission test.

for the characterization of the antenna gain. Because it is to de-embed the loss caused by the reflection at the input port of the antenna for the comparison of the antenna gain. In addition, the reflection loss can be improved by adjusting the input matching network.

Fig. 6.17 shows the measured power gain of the on-chip antenna with and without the ion implantation. When the ion irradiation is not applied, the radiation gain of over -7 dBi is achieved from 57 GHz to 67 GHz with the gain variation of less than 3 dB. It can be observed that with the increasing of the target depth, the antenna gain is gradually enhanced, which implies that the radiation efficiency of the on-chip antenna is also improved. When the target depth of 320 μm is applied, the radiation gain is improved to be

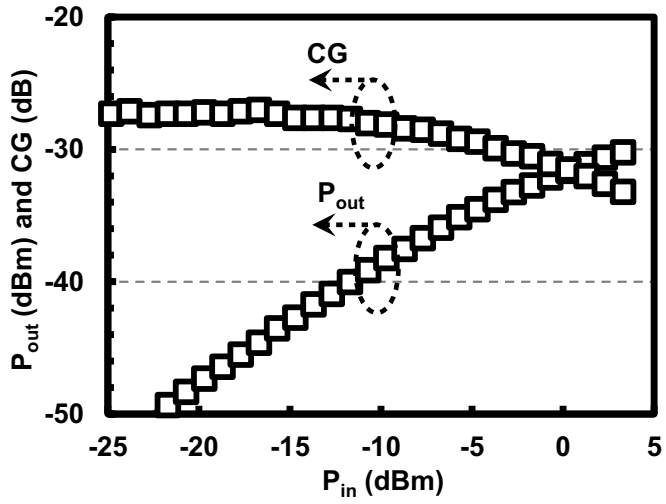


Figure 6.21: The measured P_{in}-P_{out} and CG curve of the transmitter (excluding the on-chip antenna) with f_{LO}=63.48 GHz and f_{BB}=1 GHz.

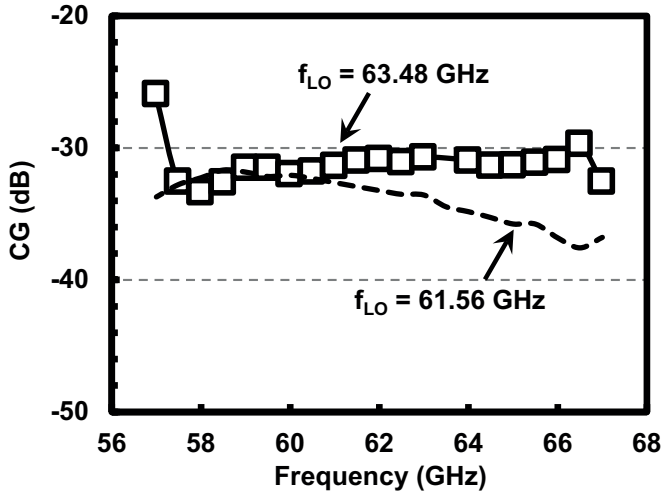


Figure 6.22: The measured transmitter conversion gain (excluding the on-chip antenna) versus frequency with different LO frequencies.

higher than −4 dBi. The average gain improvement is about 3 dB over the 10-GHz band of interest. The wide-and-flat gain characteristic of the on-chip antenna is maintained after the ion-irradiated process.

The S-parameter of the on-chip antennas is also measured for comparison of the on-chip antenna gain as illustrated in Fig. 6.18. Because the input impedance of the antenna is optimized in design under the condition of without ion implantation. The degradation of the input reflection coefficient (S_{11}) for the ion-irradiated antennas is caused by the change

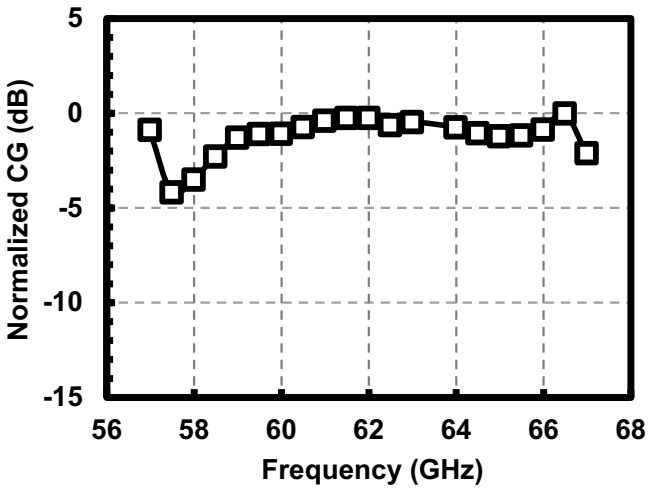


Figure 6.23: The measured transmitter conversion gain (including on-chip antenna) versus frequency with f_{LO}=63.48 GHz.

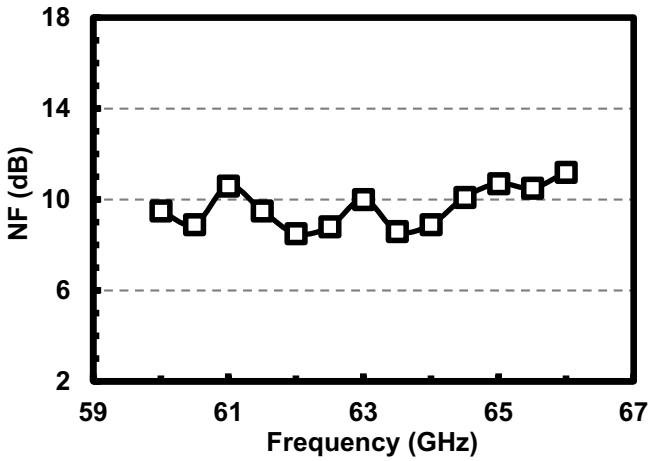


Figure 6.24: The measured NF of the external receiver versus frequency.

of the dipole antenna input impedance after ion implantation as depicted in Fig. 6.19. The loss due to the reflection is de-embedded for the gain measurement results.

Table 6.2 shows a performance comparison of the proposed CMOS on-chip dipole antenna and other state-of-the-art CMOS on-chip antennas at 60-GHz band. The proposed antenna achieves relatively high power gain (−2.0 dBi @ 60 GHz) with reasonable area occupation (0.48 mm^2). Therefore, the chips with the target ion-implantation depth of 320 μm are utilized in the following measurements of this section.

The measured baseband input power (P_{in}) versus output power (P_{out}) and CG of the transmitter excluding the on-chip antenna are shown in Fig. 6.21. The LO frequency (f_{LO}) is 63.48 GHz. The frequency of baseband signal is 1 GHz. The measurement setup is

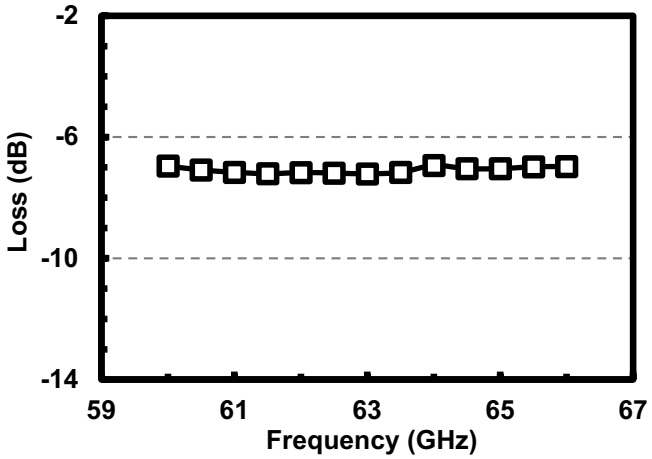
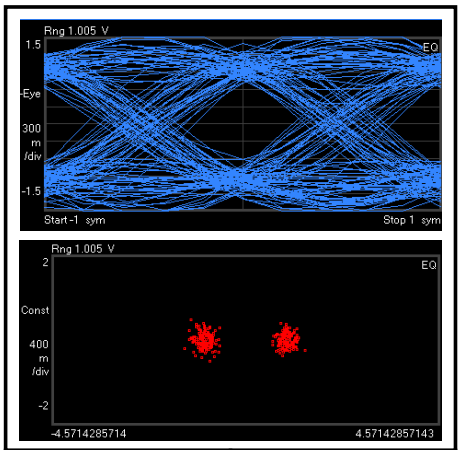


Figure 6.25: The measured connection loss from the RX antenna to the LNA versus frequency.



Modulation	BPSK
Data rate	5 Gb/s
EVM	-12 dB
TX EIRP	-36 dBm*

* For on-chip antenna gain = -3 dBi

Figure 6.26: The measured eye diagram and constellation at 5-Gb/s data rate for BPSK modulation and 1-mm distance.

illustrated in Fig. 6.20(a). The transmitter chip is located on the left side of the probe station. The receiver chip is placed at the right side of the probe station with the stand-alone on-chip antenna facing the transmitter. The received signal is amplified by an external low noise amplifier (LNA) and down-converted afterwards. It can be observed that the saturated output power is -30 dBm. The small-signal conversion gain is -27 dB at an input power of -25 dBm. The relatively low CG and output power of the transmitter compared

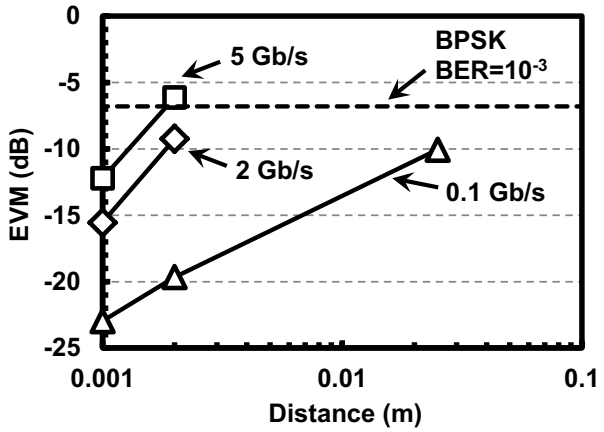


Figure 6.27: The measured EVM for BPSK modulation versus distance.

Table 6.3: 60-GHz Low-Power High-Data-Rate TX Performance Comparison.

Ref.	CMOS Process	Mod.	Data Rate	Power	Antenna	Integration Level	Core Area
This work	65 nm	BPSK	5.0 Gb/s†	17 mW	**On-chip**	60-GHz ILO, mixer, PA	0.64 mm²*
[72]	40 nm	ASK	11.0 Gb/s	29 mW	Off-chip	60-GHz VCO, mixer, PA	0.06 mm²
[73]	90 nm	OOK	10.7 Gb/s	31 mW	Off-chip	30-GHz VCO, doubler, modulator	0.15 mm²
[79]	65 nm SOI	OOK	2.2 Gb/s	28 mW	**On-chip**	60-GHz VCO, duty cycle ctrl., PA	0.82 mm²*
[80]	65 nm	QPSK	10.4 Gb/s	50 mW	**On-chip**	60-GHz VCO×4, PA×4, baseband	2.15 mm²*
[50]	40 nm LP	16QAM	7.0 Gb/s	167 mW	Off-chip	60-GHz QILO, mixer×2, PA	0.54 mm²*
[13]	65 nm	QPSK	2.6 Gb/s	160 mW	Off-chip	20-GHz PLL, PA doubler, mixer×3	0.95 mm²*

* Including on-chip antenna † Limited by the maximum sampling frequency of the AWG

with the simulation results shown in Section 6.4 are caused by the degraded input power at the LO port of the mixer ($P_{\mathrm{LO,\,mixer}}$), which is due to the unoptimized matching network between the 60GHz ILO and the passive mixer. The simulation, which uses the same matching network, shows that $P_{\mathrm{LO,\,mixer}}$ is dropped to -42 dBm from a typical ILO output

power of -22 dBm at 63.48 GHz. To demonstrate the transmitter performance, an LO frequency of 63.48 GHz is chosen for the transmitter measurement in this section. Because the measured CG at f_{LO}=63.48 GHz is higher than that at f_{LO}=61.56 GHz as depicted in Fig. 6.22.

The conversion gain of the transmitter with the gain-enhanced antenna is also measured when the LO is operating at 63.48 GHz. The measurement setup illustrated in Fig. 6.20(a) is used. Fig. 6.23 shows the measured conversion gain versus frequency. The conversion gain is normalized to the measured peak gain at 66.48 GHz. The −3 dB bandwidth is around 9 GHz (58 GHz–67 GHz). The gain variation of less than 4 dB is also achieved over the 9-GHz band of interest (57 GHz–66 GHz).

The data communication performance of the proposed transmitter is evaluated by applying a BPSK modulation signal to the baseband input. The measurement setup for the data communication shown in Fig. 6.20(b) is similar to that for the CG characterization except that the baseband signal is generated by the arbitrary waveform generator (AWG). The received signal is characterized by the oscilloscope. The LO frequency of the receiver mixer is set to 59.48 GHz. Fig. 6.24 shows the measured single-sideband noise figure (NF) of the external receiver, which includes the LNA, mixer, and oscilloscope. The measured connection loss from the output of the receiving antenna to the input of the LNA is illustrated in Fig. 6.25.

The frequency of the TX ILO is 63.48 GHz, which consumes 10 mW power from a 1.2-V supply. The eye diagram and constellation for 5 Gb/s data rate are demonstrated in Fig. 6.26 showing an EVM performance of −12 dB at 1-mm distance. The equivalent isotropically radiated power (EIRP) of the transmitter is −36 dBm for a −3-dBi gain of the on-chip antenna. The maximum data rate for 1-mm distance is mainly limited by the maximum sampling frequency of the AWG (*e.g.* 10-Gb/s data rate in BPSK requires 20 GS/s for AWG).

Fig. 6.27 shows the measured EVM at different distances between the transmitter chip and the receiving chip. A 5-Gb/s 60-GHz data link is achieved over a distance up to around 2 mm for BER$\leq 10^{-3}$ (EVM$\leq$ −6.8 dB) in BPSK modulation with the gain-enhanced on-chip antenna. The transmitter is operated at the output power of −33 dBm, which is the maximum achievable output power of the transmitter driven by the AWG. It is worthy of noticing that due to the low output power of the transmitter and high connection loss at the input side of the receiver, the implemented transmitter can barely meet the link budget for 2-mm distance and 5-Gb/s data rate elaborated in Section 6.2.

Table 6.3 summarizes and compares the performance of the proposed transmitter with that of the state-of-the-art low-power high-data-rate TXs at 60 GHz in CMOS processes. The proposed transmitter shows low power consumption, comparable data rate, and small

area with respect to the full on-chip solution. The power consumption reduction of this work is >40% lower than that of previously reported work in table 6.3. The lower data rate of 5 Gb/s is mainly because of the insufficient LO power and the measurement equipment, which is not limited by the potential of this topology. The relatively large TX core area of this work compared to that of the literature [72] is because of the not compact layout style.

6.6 Conclusion

This chapter presents a 60-GHz low-power high-data-rate transmitter with an gain-enhanced on-chip antenna in a 65-nm CMOS process. The radiation gain of the on-chip antenna is improved 3 dB by using the ion-irradiation techniques. The transmitter achieves 5-Gb/s data rate while consuming only 17 mW power with the area occupation of 0.64 mm^2, which is well-suited for the short-range wireless interconnection applications.

Chapter 7

Conclusions and Future Work

7.1 Conclusions

The 60-GHz CMOS transceivers are demonstrated to be one of the most promising low-power low-cost candidates for short-range multi-Gb/s wireless communications. To facilitate the commercialization of the 60-GHz CMOS transceivers, the techniques and solutions of the HCI-reliability enhancement and power consumption reduction are investigated in this dissertation.

For the HCI-reliability issues at 60-GHz band, it is shown that to meet the operation lifetime requirement of the transmitter, conventional solutions need to reduce the output power and supply voltage, which degrades the communication distance, linearity, efficiency, and therefore the user experiences. Although power combining and beamforming techniques can be used to compensate the degraded output power and linear-

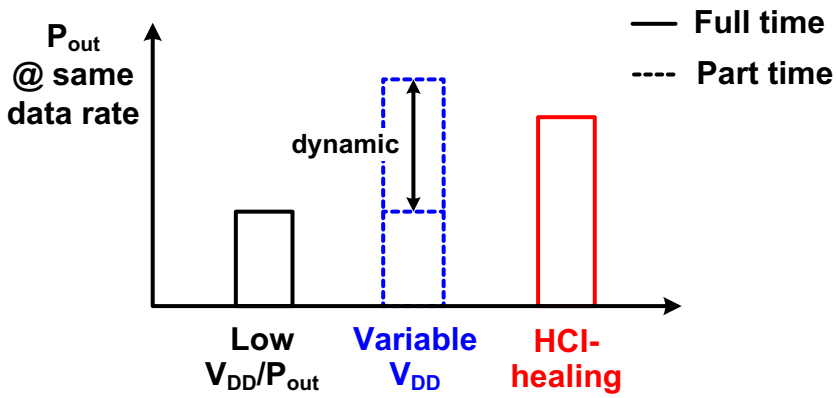


Figure 7.1: The conceptual illustration of the high-data-rate coverage radius for different HCI-issue solutions of the 60-GHz CMOS PA.

ity, the deteriorated efficiency remains to be unimproved. To address the HCI issues for 60-GHz applications, a transistor-level study of HCI physical mechanism and lifetime characterization methods under DC and RF stress have been conducted. Based on the acquired knowledge, the reliability model of transistors under AC-mode HCI stress is derived to provide a valuable solution of HCI damage alleviation by limiting the operation period of high output power condition. The proposed solution, which is realized by using variable-supply-voltage, provides a way to output superior power with high linearity and efficiency in a carefully restricted time period while satisfying the lifetime requirement. The lifetime of the implemented example PA can be improved to over 10 years with the careful arrangement of various operation supply voltages. On the other hand, the power amplifier is still able to provide 13.2 dBm saturation power, 10.2 dBm power at 1-dB compression point and 15.0% peak power-added efficiency at 60 GHz for high supply voltage (V_{PA} = 1.0 V). This solution is especially suitable for the applications with the burst requirement of high data rate at high output power. The HCI-healing technique introduced in this dissertation further relieves the trade-off between the HCI reliability and the system performance, which guarantees longer operation lifetime with high output power. The implemented transceiver using the proposed HCI-healing technique achieves over 81-year lifetime without sacrificing the output power and efficiency. The transceiver demonstrates an output power of 9.3 dBm at TX EVM = -21 dB and 3.9% TX efficiency. While for comparison, the conventional solutions normally have less than 1% TX effi-

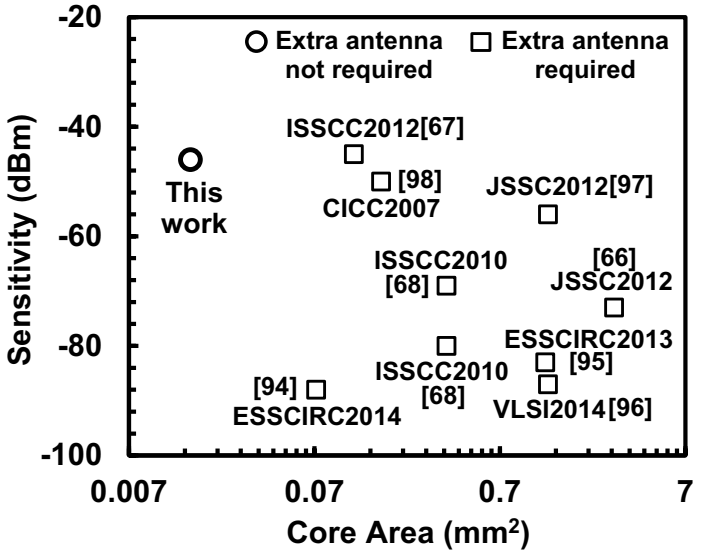


Figure 7.2: Core area versus sensitivity for the state-of-the-art low-power WuRxs and the work presented in this dissertation.

ciency and 2 dBm output power with comparable TX EVM performance considering the HCI reliability. The comparison of the different solutions for HCI issues of single-path 60-GHz PAs in standard CMOS processes is illustrated in Fig. 7.1.

For the power consumption reduction of the 60-GHz CMOS transceiver, it is known that the wake-up receiver is one of the most applicable choices to systematically reduce the power consumption over time. Conventional wake-up receivers using either the 60-GHz band or lower frequency bands share the same issue of needing bulky components, which increases the chip area and implementation cost. By reusing the 60-GHz LNA gain stages, the proposed 60-GHz wake-up receiver occupies an area overhead of only $0.015\,\mathrm{mm}^2$ and does not need extra antennas or switches to be integrated with the 60-GHz multi-Gb/s transceiver. The WuRx achieves the sensitivity of -46 dBm (low-power mode) and -60 dBm (sensitivity-boosted mode) with a power consumption of $64\,\mu\mathrm{W}$ and 12.7 mW, respectively. The average power consumption of the WuRx in sensitivity-boosted mode can be reduced by the duty cycle control technique. To highlight the compactness of the proposed WuRx, a summarization of core area versus sensitivity for the state-of-the-art low-power WuRxs ($3\,\mu$W-$65\,\mu$W) [66–68, 94–98] and the work presented in this dissertation is shown in Fig. 7.2.

Besides reducing the time-averaged power consumption of the 60-GHz transceiver by the duty cycle control scheme, the downscale of the operation power consumption of the transceiver can directly help to decrease the consumed power over time. Simple modulation schemes (such as BPSK and OOK) and low complexity of the transceiver topology are preferred in the context of energy efficiency (the ratio of power consumption to data rate). The energy efficiency potential of the 60-GHz high-data-rate transmitter is explored in this dissertation. The 60-GHz CMOS transmitter adopting the simple modulation schemes is designed and implemented using wideband and power-saving techniques, which guarantees the low-power and high-data-rate characteristic (high energy efficiency). An energy efficiency of 3.4 pJ/bit is achieved in BPSK with the 3-dB bandwidth of 9 GHz. The limited data rate (5 Gb/s) is mainly due to the limitation of the maximum sampling frequency of the AWG. The state-of-the-art researches [9–11, 13, 15, 72, 79, 80] and the works presented in this dissertation demonstrate that for ultra-short-range (several tens of centimeters) several-Gb/s wireless communications (*e.g.* chip-to-chip), the simple modulation schemes and low complexity system topologies have superior energy efficiency performance. Furthermore, the on-chip antenna with peak gain of -2 dBi at 60 GHz is integrated with the ultra-low-power transmitter core in a standard 65 nm CMOS process. The gain-enhanced antenna together with the wideband and power-saving design of the transmitter provides a low-power low-cost full on-chip solution for the short-range multi-Gb/s wireless communication.

7.2 Future Work

In terms of the future prospects for the proposed solutions of the HCI reliability issues, the variable-supply-voltage technique has the potential of achieving robustness system performance (not only HCI reliability) against process, voltage and temperature (PVT) variations with the help of other techniques such as auto-power-control (APC) feedback loop with integrated power detector, process and temperature self-sensing LDO, and variable-gain amplifiers (VGA) [10]. In addition, for the same low output power, low V_{DD} has the benefit of reducing the power consumption of the power amplifier. The effects of this phenomenon on the time-averaged power consumption of the 60-GHz transceiver need to be quantized according to the comprehensive study of output power distribution and propagation environment in certain applications. Moreover, the combination of the HCI-

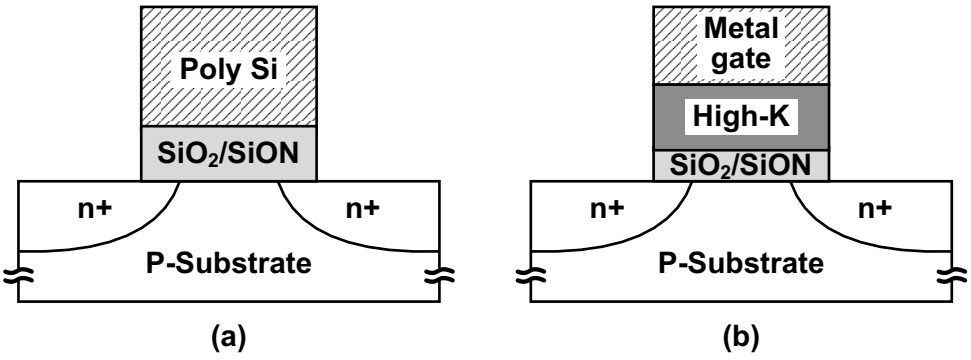


Figure 7.3: NMOS structure with (a)SiO_2/poly-Si; (b) high-k/metal gate.

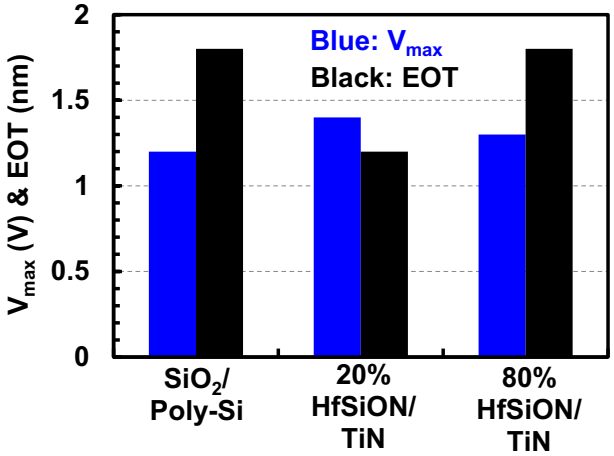


Figure 7.4: Measured $V_{\max}$ and EOT for SiO_2/poly-Si transistor and high-k/metal gate transistor with same gate length $L_g = 70nm$.

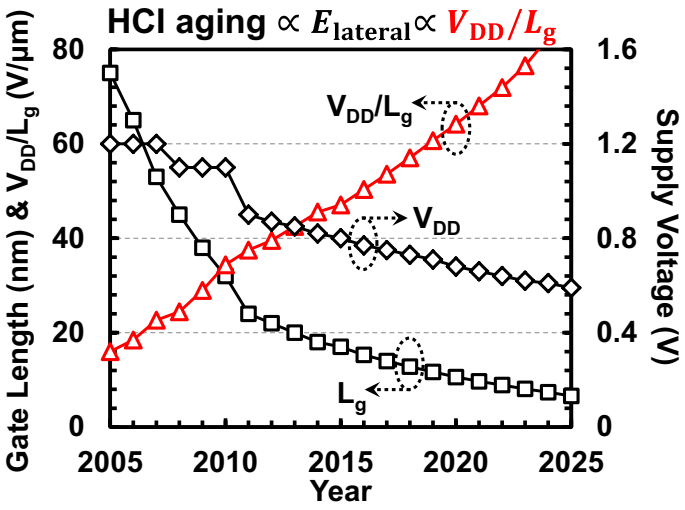


Figure 7.5: The channel lateral electric field trend in CMOS processes according to ITRS2013 and before.

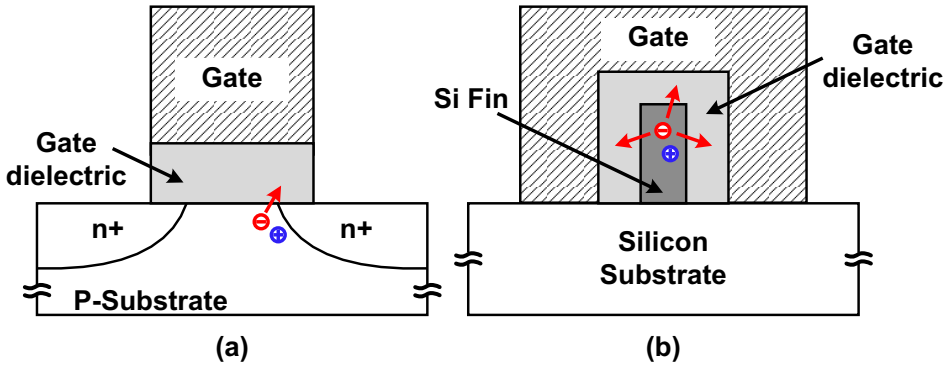


Figure 7.6: Hot carrier mechanism in (a) planar MOSFET; (b) tri-gate FinFET.

healing and variable-supply-voltage solutions, which is not difficult to realize because of the digital intensive nature of these techniques, may help to further narrow the gap between the optimum system performance and the device lifetime requirements.

SiO_2 has been the ”classical” dielectric material in CMOS devices due to its excellent insulating properties, low defect density, good mobility of carriers in the channel, and thermal stability. However, following the reduction of device dimensions fore-casted by Moore’s law, intolerable leakage currents appear when the SiO_2 thickness is scaled down. In order to reduce the leakage currents, the replacement of the SiO_2/poly-Si system by high-k/metal gates is introduced. The higher k-value allows for physically thicker dielectrics, with significant reduction of the gate leakage current, while the gate capacitance

is increased. In this regard, Hf-based high-k materials are considered good candidates to substitute SiO_2 in future CMOS generation. However, a thin SiO_2 or SiON interface layer has been maintained as shown in Fig. 7.3 Consequently, the substrate/dielectric interface does not change and HCI remains a issue in high-k technologies. Fig. 7.4 shows the measurement results from literature [99], which demonstrates the HCI performance of the high-k transistor is comparable or slightly better than that of the traditional SiO_2/SiON transistor with same gate length L_g=70 nm. V_{max} is the extrapolated operation voltage for ten-year lifetime after DC HCI stress at V_G=V_D=V_{max}. EOT is the effective oxide thickness. It is also worthy of noting that even with the high-k dielectric the HCI issues become more severe with the scaling down of the transistor size. Since the supply voltage scaling slow down because of the non-scalability of the sub-threshold slope, as depicted in Fig. 7.5. The issues also have been demonstrated in literature [100] with much worse measured HCI degradation of high-k metal-gate 28nm NMOSFET compared to reference transistor in 40nm CMOS node with SiON gate dielectric. The HCI reliability enhancement technique is necessary for the high-k metal-gate CMOS processes.

FinFETs with the excellent short channel control and switching characteristics are proved to be one of candidates to further extend the device scaling to the nano-scale regime. However, researches show that HCI degradation in FinFET is worse than planar devices because the confined geometry greatly raise the possibility of the HCI damge [101, 102], which can be explained in Fig. 7.6. The energetic carriers scattered in the channel of FinFET can intersect the gate walls all around the channel. A narrower fin is more likely to capture these scattered carriers. While the hot carriers in planar MOSFET only can intersect the gate in the vertical direction. It is interesting to know that for the FinFET, the hot carriers injected into the oxide bulk defects are the main degradation mechanism overwhelming the interface degradation by hot carriers and the cold carrier injection [103]. Therefore, the HCI-healing technique proposed in this thesis can be a valuable solution for reliability enhancement of the advanced CMOS processes such as FinFET.

For the proposed power-consumption-reduction techniques, new circuit technologies and operation schemes are desired to improve the sensitivity of the proposed 60-GHz WuRx without significantly increasing the consumed power of itself. Because the traditional ways of improving sensitivity at lower frequencies, such as amplifying the signal before the detector [98], double-sampling technique [68], and uncertain-IF structure [94], are not feasible for the low-power 60-GHz operation. Furthermore, as discussed in the previous section, the simple modulation schemes and low-complexity system topologies can be chosen for the purpose of reducing operation power consumption in the specific applications. Nevertheless, if more complexed modulation schemes and topologies are

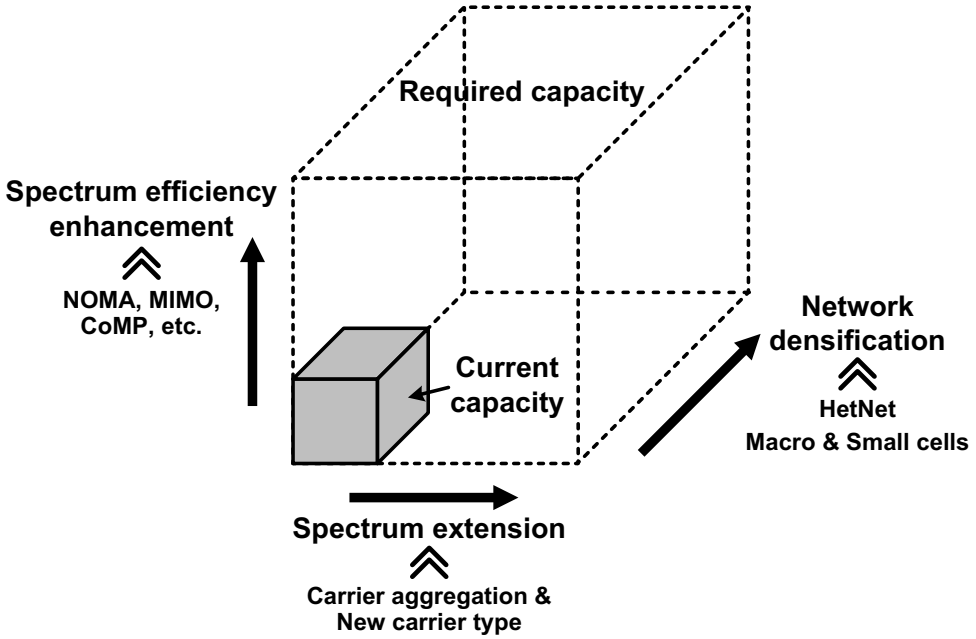


Figure 7.7: Directions of evolution for future radio access (5G).

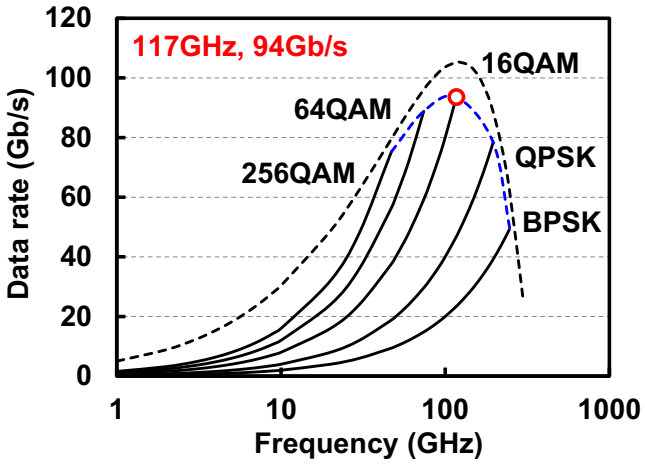


Figure 7.8: Calculated data rate versus carrier frequency at $P_{\text{eff}} = 20\,\text{dBm}$ and $\alpha = 0.2$.

required, how to reduce the operation power consumption will be a challenging topic.

In the end, I would like to emphasize the potential of the mmW techniques to enhance the mobile communications nowadays and in the future.

Firstly, for the currently used 3G/4G mobile communication, the exponentially increasing number of base stations in urban area causes deployment difficulties. Because the volume of the base station raises rapidly with the increasing number of neighborhood base stations when traditional backhaul connections using optical fibers are adopted. For-

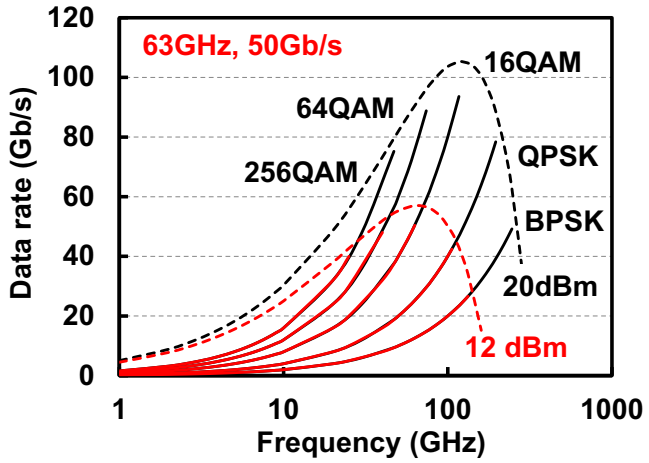


Figure 7.9: Calculated data rate versus carrier frequency at $P_{\text{eff}} = 12\,\text{dBm}$ and $\alpha = 0.2$.

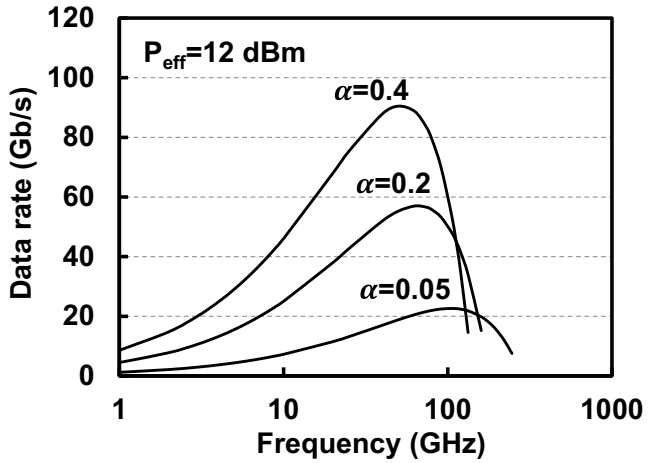


Figure 7.10: Calculated data rate versus carrier frequency at $P_{\text{eff}} = 12\,\text{dBm}$ and different α.

tunately, wireless backhaul equipments using mmW bands can be very compact (exhibiting a typical size of 40-80 mm^2) and easy to embed in urban appliances. Meanwhile, mmW backhaul solutions can provide superior data rate because of the ultra-wide available bandwidth (*e.g.* 9 GHz bandwidth around 60 GHz). Therefore, the mmW solution will be an attracting evolution of the backhaul connections among the base stations for 3G/4G and beyond.

Considering the evolution of the cellular networks for future radio access (5G), there is a prominent characteristic predicted by many network service providers, hardware manufacturers, and research institutes, which is the mobile communication capacity per square

kilometer (capacity/km^2) will become extremely high in 2020 and beyond (for instance, 1000 times higher than that of today's 3G networks). A set of radio access technologies is needed to satisfy the unprecedented capacity requirement as shown in Fig. 7.7. Basically, these technologies can be divided into three main directions which should be forwarded simultaneously. The discussion of the three directions and the role of mmW techniques in them are elaborated below.

Starting from the spectrum extension, the very crowded current cellular band needs to be extended for much higher data rate (for example, 10 times to 100 times). It would benefit from the utilization of mmW frequency band since the available bandwidth is ultra-wide as mentioned before (up to 9 GHz unlicensed bandwidth at 60-GHz band).

According to the Shannon-Hartley theorem, the channel capacity C (maximum achievable data rate) is the function of communication bandwidth (B) and signal to noise ratio (SNR), as shown in eq. (7.1).

$$C = B \cdot \log_2 (1 + SNR) \tag{7.1}$$

This equation can be approximated to the following form according to [104]

$$C_{\text{eff}} \approx B \cdot \left(\frac{10}{3} \log_{10}(SNR) - 1 \right) \tag{7.2}$$

Considering the receiver noise figure (NF) and implementation loss (IL), from Friis equation

$$\begin{aligned} C_{\text{eff}} \;\approx\; & B \cdot \left[\frac{1}{3} \left(P_{\text{t}}|\text{dBm} + G_{\text{t}}|\text{dBi} + G_{\text{r}}|\text{dBi} - IL|\text{dB} + 20 \log_{10}\left(\frac{c}{4\pi d f_{\text{c}}}\right) \right.\right. \\ + \;\; & \left.\left. 174 \; -10 \log_{10} B - NF|\text{dB} \right) - 1 \right] \end{aligned} \tag{7.3}$$

where P_{t} is the transmitting power. G_{r} and G_{t} are the antenna gain for receiver and transmitter, respectively. c is the speed of light (3×10^8 m/s). d is distance between the antennas in meter. f_{c} is the carrier frequency. The received signal power P_{r} can be written as.

$$P_{\text{r}}|\text{dBm} = P_{\text{t}}|\text{dBm} + G_{\text{t}}|\text{dBi} + G_{\text{r}}|\text{dBi} - IL|\text{dB} + 20 \log_{10}\left(\frac{c}{4\pi d f_{\text{c}}}\right) \tag{7.4}$$

and the receiver noise floor is

$$\text{Noise Floor} = -174 + 10 \log_{10} B + NF|\text{dB} \tag{7.5}$$

For simplification, define the effective received signal power P_{eff}

$$P_{\text{eff}}|\text{dBm} = P_{\text{t}}|\text{dBm} + G_{\text{t}}|\text{dBi} + G_{\text{r}}|\text{dBi} - IL|\text{dB} - NF|\text{dB} - 20\log_{10}(\frac{d}{1\text{m}}) \tag{7.6}$$

Solve the following differential equation

$$\frac{\text{d}C_{\text{eff}}}{\text{d}f_{\text{c}}} = 0 \tag{7.7}$$

Assume $B = \alpha f_{\text{c}}$, the maximum data rate $C_{\text{eff,max}}$ and corresponding carrier frequency $f_{\text{c,max}}$ can be expressed as [104]

$$C_{\text{eff,max}} = C_0 \left[\alpha^2 \frac{P_{\text{eff}}}{1\text{mW}}\right]^{\frac{1}{3}} \tag{7.8}$$

$$f_{\text{c,max}} = \frac{C_0}{10\log_{10}\text{e}} \left[\frac{1}{\alpha}\frac{P_{\text{eff}}}{1\text{mW}}\right]^{\frac{1}{3}} \tag{7.9}$$

where

$$C_0 = \frac{10\log_{10}\text{e}}{\text{e}} 10^{\frac{106.19}{10}} = 66.45 \text{ Gbit/s} \tag{7.10}$$

The maximum data rate and the corresponding carrier frequency are the function of P_{eff} and communication bandwidth ratio α. Fig. 7.8 shows the example of communication data rate versus carrier frequency under the condition of $P_{\text{eff}} = 20\,\text{dBm}$ (*e.g.* $P_{\text{t}} = 20\,\text{dBm}$, $G_{\text{t}} = G_{\text{r}} = 10\,\text{dBi}$, $NF = IL = 0\,\text{dB}$, $d = 10\,\text{m}$) and $\alpha = 0.2$. The black dash line is the estimated data rate through Shannon theorem. The blue dash line is the estimated maximum data rate for modulation scheme at BER<10^{-3}. The maximum data rate of 94 Gb/s for BER<10^{-3} is achieved with carrier frequency of 117 GHz in 16QAM. From the above equations, it also can be seen that for certain values of P_{eff} and α, the carrier frequency for maximum data rate will fall into the 60-GHz band, as demonstrated in Fig. 7.9. Where the black lines are results from Fig. 7.8. The red lines are calculated results for $P_{\text{eff}} = 12\,\text{dBm}$ (*e.g.* $P_{\text{t}} = 20\,\text{dBm}$, $G_{\text{t}} = G_{\text{r}} = 10\,\text{dBi}$, $NF = 8\,\text{dB}$,$IL = 0\,\text{dB}$, $d = 10\,\text{m}$) and $\alpha = 0.2$. The carrier frequency for maximum data rate of 50 Gb/s in 16QAM is 63 GHz. The influence of bandwidth ratio α on $C_{\text{eff,max}}$ and $f_{\text{c,max}}$ is also shown in Fig. 7.10. It is interesting to know that $C_{\text{eff,max}}$ can be simplified to

$$C_{\text{eff,max}} = 10\log_{10}(\text{e})\alpha f_{\text{c,max}} = 10\log_{10}(\text{e})B \approx 4.3B \tag{7.11}$$

The result is very close to the situation of 16QAM modulation, in which the $C/B = 4$. In other words, if P_{eff} and α are fixed for all the carrier frequencies, the communication using 16QAM modulation can achieve the maximum data rate, as depicted in Fig. 7.8.

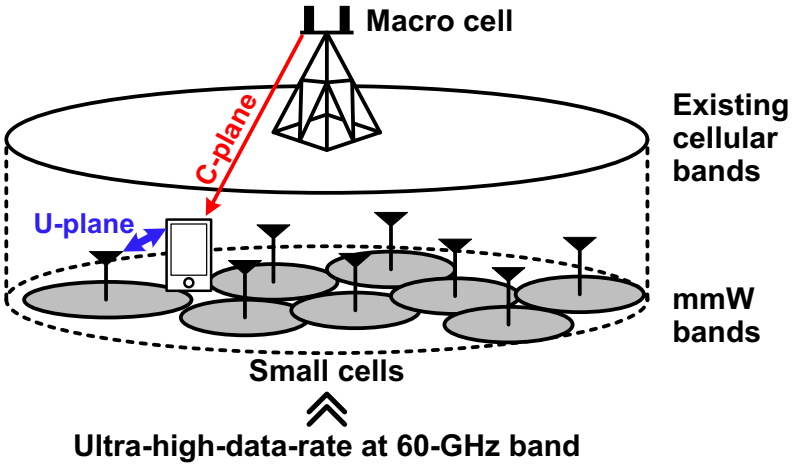


Figure 7.11: The concept of HetNet for future radio access (5G).

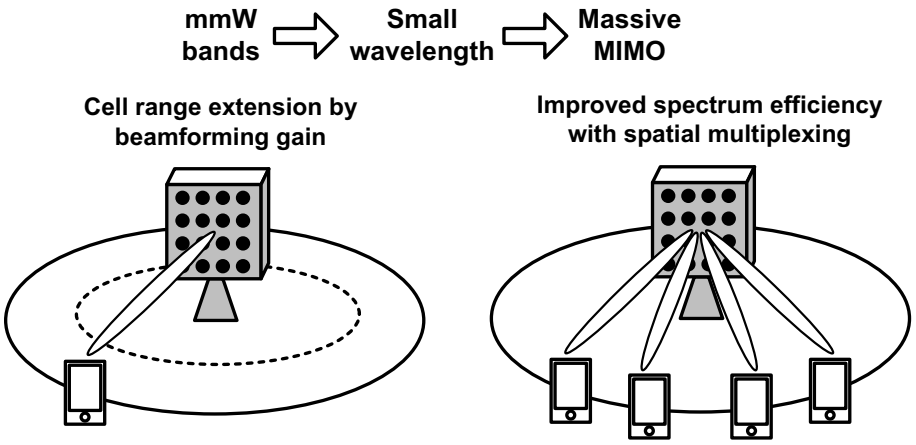


Figure 7.12: The examples of massive MIMO.

Therefore, some useful insights can be gained from the above equations: a) optimum carrier frequencies exist for maximum data rate; b) under certain P_{eff} constrain, for a fixed carrier frequency, bandwidth is not always the wider the better; c) increase of P_{eff} is welcome for all the carrier frequencies; d) 60-GHz band with medium transmitting power level (20dBm+) and wide bandwidth ($\alpha = 0.14$) are well suited for high-data-rate communication.

The exploitation of multiple bands can also greatly help to densifty the network by constructing a new type of network called ”multi-band heterogeneous network (HetNet)” [105]. The concept of the HetNet is illustrated in Fig. 7.11. The basic idea is to split control plane (C-plane) and user plane (U-plane) between macro and small (pico) cells in different frequency bands. Macro cells maintain good connectivity and mobility using existing cellular bands (C-plane). Small cells provides higher throughput and more

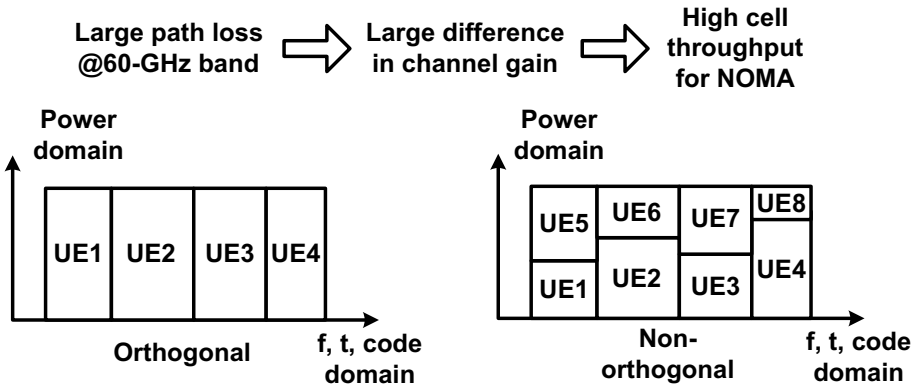


Figure 7.13: The orthogonal and non-orthogonal multiple access scheme.

flexible/cost-energy efficient operations using higher/wider frequency bands (U-plane). Therefore, more small cells can be added flexibly. To realize the multi-band HetNet, dynamic optimization of small cell parameters (TX output power, beam angle, cell range, *etc.*) is the challenging issue to maximize system rate. The interference from adjacent channels or even co-channels of the marco and small cells can severely degrade the communication quality [106]. Interference coordination and management techniques are desired to solve this issue.

Massive MIMO (multiple-input and multiple-output), beamforming using massive antenna elements, can improve spectrum efficiency with spatial multiplexing as illustrated in Fig. 7.12. This technique is especially attractive for the pico-cells using mmW frequencies because of the very small antenna size. The relatively large path loss at mmW bands can also be compensated by the massive MIMO technique extending the cell range. Non-orthogonal multiple access (NOMA) scheme [107] can further enhance the spectrum efficiency by using the path loss difference among users (power-domain) as shown in Fig. 7.13. The performance gain of the NOMA scheme increases when the path loss difference between user equipments are large. Interestingly, it is the nature of mmW frequency bands, especially of the 60-GHz band due to strong oxygen absorption, which motivates the utilization of the 60-GHz band for small-cell access and backhauling.

In the near future, a large number of wireless communication devices operating at 60-GHz band will appear in out daily life. The interference from adjacent channels or even co-channels can severely degrade the communication quality [106]. Regulations and techniques are desired to solve this issue.

With the increasing demand on wireless communication data rate, there may come a day that a very high spectrum usage efficiency (*e.g.* 256QAM) is required for the 60-GHz wireless systems as it is required in the lower frequencies nowadays. How to realize the

transceiver with very small I/Q mismatch and low phase noise local oscillators to meet the requirements remains to be a question. Especially, recent research [108] shows that off-state drain stress, which is normally happened in the voltage controlled oscillator, has significant effect on transistor flicker noise performance and degrades g_{rmm}. This degradation can cause prominent phase noise increase and start-up issue, which deteriorated the 60-GHz system performance. The effect of the HCI healing technique on the phase noise performance of the VCO would be a interesting topic.

In summary, the future mobile communication will have massive connected devices with diverse applications and unprecedented traffic volume. The requirements and challenges of the future radio access are widely spread, which includes support for data traffic explosion, massive device connectivity, quality of experience (QoE) for various applications, intelligent network with low power, low cost and high robustness, *etc*. The 60-GHz solution will have a important role in the future ”networked society”, hence facing the same chances and challenges associated with it. Researches all over the world including the works presented in this dissertation are paving the way for the evolution.

Bibliography

[1] M.S. Chen, Y.N. Shih, C.L. Lin, H.W. Hung, and J. Lee, “A fully-integrated 40-Gb/s transceiver in 65-nm CMOS technology,” IEEE J. Solid-State Circuits, vol.47, no.3, pp.627–640, Mar. 2012.

[2] M. Harwood, S. Nielsen, A. Szczepanek, R. Allred, S. Batty, M. Case, S. Forey, K. Gopalakrishnan, L. Kan, B. Killips, P. Mishra, R. Pande, H. Rategh, A. Ren, J. Sanders, A. Schoy, R. Ward, M. Wetterhorn, and N. Yeung, “A 225 mW 28 Gb/s SerDes in 40nm CMOS with 13 dB of analog equalization for 100 GBASE-LR4 and optical transport lane 4.4 applications,” IEEE ISSCC Dig. Tech. Papers, pp.326–327, 2012.

[3] R. Navid, E.H. Chen, M. Hossain, B. Leibowitz, J. Ren, C. huei Adam Chou, B. Daly, M. Aleksic, B. Su, S. Li, M. Shirasgaonkar, F. Heaton, J. Zerbe, and J. Eble, “A 40 Gb/s serial link transceiver in 28 nm CMOS technology,” IEEE J. Solid-State Circuits, vol.50, no.4, pp.1–14, Apr. 2014.

[4] P.C. Chiang, H.W. Hung, H.Y. Chu, G.S. Chen, and J. Lee, “60 Gb/s NRZ and PAM4 transmitters for 400 GbE in 65 nm CMOS,” IEEE ISSCC Dig. Tech. Papers, pp.42–43, 2014.

[5] “802.11n-2009–IEEE standard for information technology– local and metropolitan area networks–specific requirements– part 11: Wireless LAN medium access control (MAC)and physical layer (PHY) specifications amendment 5: Enhancements for higher throughput,” IEEE Std 802.11n-2009, Nov. 2009.

[6] Y. Zheng, K.W. Wong, M.A. Asaru, D. Shen, W.H. Zhao, Y.J. The, P. Andrew, F. Lin, W.G. Yeoh, and R. Singh, “A 0.18 μm CMOS dual-band UWB transceiver,” IEEE ISSCC Dig. Tech. Papers, pp.114–115, 2007.

[7] H. Hedayati and K. Entesari, “A 90-nm CMOS UWB impulse radio transmitter with 30-dB in-band notch at IEEE 802.11a system,” IEEE Trans. Microw. Theory Tech., vol.61, no.12, pp.4220–4232, Dec. 2013.

[8] S. Emami, R.F. Wiser, E. Ali, M.G. Forbes, M.Q. Gordon, X. Guan, S. Lo, P.T. McElwee, J. Parker, J.R. Tani, J.M. Gilbert, and C.H. Doan, "A 60GHz CMOS phased-array transceiver pair for multi-Gb/s wireless communications," IEEE ISSCC Dig. Tech. Papers, pp.164–165, 2011.

[9] K. Okada, K. Matsushita, K. Bunsen, R. Murakami, A. Musa, T. Sato, H. Asada, N. Takayama, N. Li, S. Ito, W. Chaivipas, R. Minami, and A. Matsuzawa, "A 60GHz 16QAM/8PSK/QPSK/BPSK direct-conversion transceiver for IEEE 802.15.3c," IEEE ISSCC Dig. Tech. Papers, pp.160–161, 2011.

[10] T. Tsukizawa, A. Yoshimoto, H. Komori, K. Miyanaga, R. Kitamura, Y. Morishita, M. Irie, Y. Nagaso, T. Watanabe, K. Takinami, and N. Saito, "A PVT-variation tolerant fully integrated 60 GHz transceiver for IEEE 802.11ad," Symp. VLSI Circuits Dig. Tech. Papers, pp.123–124, 2014.

[11] K. Okada, R. Minami, Y. Tsukui, S. Kawai, Y. Seo, S. Sato, S. Kondo, T. Ueno, Y. Takeuchi, T. Yamaguchi, A. Musa, R. Wu, M. Miyahara, and A. Matsuzawa, "A 64-QAM 60GHz CMOS transceiver with 4-channel bonding," IEEE ISSCC Dig. Tech. Papers, pp.346–347, 2014.

[12] K. Okada, K. Kondou, M. Miyahara, M. Shinagawa, H. Asada, R. Minami, T. Yamaguchi, A. Musa, Y. Tsukui, Y. Asakura, S. Tamonoki, H. Yamagishi, Y. Hino, T. Sato, H. Sakaguchi, N. Shimasaki, T. Ito, Y. Takeuchi, N. Li, Q. Bu, R. Murakami, K. Bunsen, K. Matsushita, M. Noda, and A. Matsuzawa, "A full 4-channel 6.3 Gb/s 60 GHz direct-conversion transceiver with low-power analog and digital baseband circuitry," IEEE ISSCC Dig. Tech. Papers, pp.218–219, 2012.

[13] T. Mitomo, Y. Tsutsumi, H. Hoshino, M. Hosoya, T. Wang, Y. Tsubouchi, R. Tachibana, A. Sai, Y. Kobayashi, D. Kurose, T. Ito, K. Ban, T. Tandai, and T. Tomizawa, "A 2 Gb/s-throughput CMOS transceiver chipset with in-package antenna for 60 GHz short-range wireless communication," IEEE ISSCC Dig. Tech. Papers, pp.266–267, 2012.

[14] T. Tsukizawa, N. Shirakata, T. Morita, K. Tanaka, J. Sato, Y. Morishita, M. Kanemaru, R. Kitamura, T. Shima, T. Nakatani, K. Miyanaga, T. Urushihara, H. Yoshikawa, T. Sakamoto, H. Motozuka, Y. Shirakawa, N. Yosoku, A. Yamamoto, R. Shiozaki, and N. Saito, "A fully integrated 60GHz CMOS transceiver chipset based on WiGig/IEEE802.11ad with built-in self calibration for mobile applications," IEEE ISSCC Dig. Tech. Papers, pp.230–231, 2013.

[15] M. Boers, I. Vassiliou, S. Sarkar, S. Nicolson, E. Adabi, B. Afshar, B. Perumana, T. Chalvatzis, S. Kavadias, P. Sen, W.L. Chan, A. Yu, A. Parsa, M. Nariman, S. Yoon, A.G. Besoli, C. Kyriazidou, G. Zochios, N. Kocaman, A. Garg, H. Eberhart, P. Yang, H. Xie, H.J. Kim, A. Tarighat, D. Garrett, A. Blanksby, M.K. Wong, D.P. Thirupathi, S. Mak, R. Srinivasan, A. Ibrahim, E. Sengul, V. Roussel, P.C. Huang, T. Yeh, M. Mese, J. Castaneda, B. Ibrahim, T. Sowlati, M. Rofougaran, and A. Rofougaran, "A 16TX/16RX 60GHz 802.11ad chipset with single coaxial interface and polarization diversity," IEEE ISSCC Dig. Tech. Papers, pp.344–345, 2014.

[16] M.J. Rosker and H.B. Wallace, "Imaging through the atmosphere at terahertz frequencies," Proc. IEEE IMS, pp.773–776, 2007.

[17] F. Giannetti, M. Luise, and R. Reggiannini, "Mobile and personal communications in the 60 GHz band: A survey," Wireless Personal Communications, vol.10, no.2, pp.207–243, 1999.

[18] C.R. Anderson and T.S. Rappaport, "In-building wideband partition loss measurements at 2.5 and 60 GHz," IEEE Transactions on Wireless Communications, vol.3, no.3, pp.922–928, May 2004.

[19] "50.2–71 GHz realignment," US Federal Register, vol.66, no.15, pp.7402–7409, January 2001. URL http://www.gpo.gov/fdsys/pkg/FR-2001-01-23/pdf/01-1038.pdf.

[20] S.K. Yong and C.C. Chong, "An overview of multigigabit wireless through millimeter wave technology: potentials and technical challenges," EURASIP Journal on Wireless Communications and Networking, vol.2007, pp.1–10, 2007.

[21] "Situations of actual use of spectrum in Japan (as of april 2014)," Ministry of Internal Affairs and Communications. URL http://www.tele.soumu.go.jp/resource/e/search/myuse/use0303/10g.pdf.

[22] "European commision decision of 13 may 2009 amending decision 2006/771/ec on harmonisation of the radio spectrum for use by short-range devices," Official Journal of the European Union, May 2009. URL http://ec.europa.eu/information_society/newsroom/image/13_may%202009%20expl%20doc_5867.pdf.

[23] "IEEE standard for information technology – telecommunications and information exchange between systems – local and metropolitan area networks – spe-

cific requirements. part 15.3: Wireless medium access control (MAC) and physical layer (PHY) specifications for high rate wireless personal area networks (WPANs) amendment 2: Millimeter-wavebased alternative physical layer extension," IEEE Std 802.15.3c-2009, Oct. 2009.

[24] "802.11ad-2012 - IEEE standard for information technology –telecommunications and information exchange between systems –local and metropolitan area networks–specific requirements -part 11: Wireless LAN medium access control (MAC) and physical layer (PHY) specifications amendment 3: Enhancements for very high throughput in the 60 GHz band," IEEE Std 802.11ad-2012, Dec. 2012.

[25] "WiGig and the future of seamless connectivity," Wi-Fi Alliance, Sep. 2013. URL http://www.wi-fi.org/download.php?file=/sites/default/files/private/WiGig_White_Paper_20130909.pdf.

[26] "WirelessHD next generation standard now available," WirelessHD press release, May 2010. URL http://www.wirelesshd.org/pdfs/WiHD%20Next%20Gen%20May%202010%20FINAL%20Web.pdf.

[27] "WirelessHD specification overview," WirelessHD Std. Overview, Aug. 2009. URL http://www.wirelesshd.org/pdfs/WirelessHDSpecification-Overview-v1%200%204%20Aug09.pdf.

[28] "High rate 60 GHz PHY, MAC and HDMI PALs," Standard ECMA-387 (2nd edition), Dec. 2010. URL http://www.ecma-international.org/publications/files/ECMA-ST/ECMA-387.pdf.

[29] T.S. Rappaport, J.N. Murdock, and F. Gutierrez, "State of the art in 60-GHz integrated circuits and systems for wireless communications," Proceedings of the IEEE, vol.99, no.8, pp.1390–1436, Aug. 2011.

[30] D. Stephens, T. Vanhoucke, and J.J.T.M. Donkers, "RF reliability of short channel NMOS devices," IEEE RFIC Symp. Dig. Papers, pp.343–346, 2009.

[31] K.K. Tokgoz, K. Lim, K. Okada, and A. Matsuzawa, "Shunt characterization technique of decoupling transmission line for millimeter-wave CMOS amplifier design," Proc. IEEE APMC, pp.274–276, 2014.

[32] K.K. Tokgoz, N. Fajri, Y. Seo, S. Kawai, K. Okada, and A. Matsuzawa, "A characterization method of on-chip Tee-junction for millimeter-wave CMOS circuit design," Proc. IEEE SSDM, 2014.

[33] N. Li, K. Matsushita, N. Takayama, S. Ito, K. Okada, and A. Matsuzawa, "Millimeter-wave amplifiers design by employing multi-line de-embedding technique," IEICE Trans. Electronics, vol.E93-A, no.2, pp.431–439, Feb. 2010.

[34] N. Li, K. Bunsen, N. Takayama, Q. Bu, T. Suzuki, M. Sato, Y. Kawano, T. Hirose, K. Okada, and A. Matsuzawa, "A 24 dB gain 51-68 GHz common source low noise amplifier using asymmetric-layout transistors," IEICE Trans. Electronics, vol.E95-A, no.2, pp.498–505, Feb. 2012.

[35] W. Wang, V. Reddy, A.T. Krishnan, R. Vattikonda, S. Krishnan, and Y. Cao, "Compact modeling and simulation of circuit reliability for 65-nm CMOS technology," IEEE Transactions on Device and Materials Reliability, vol.7, no.4, pp.509–517, Dec. 2007.

[36] S. Bhardwaj, W. Wang, R. Vattikonda, Y. Cao, and S. Vrudhula, "Predictive modeling of the nbti effect for reliable design," Proc. IEEE CICC, pp.189–192, 2006.

[37] M. Kimura, "Field and temperature acceleration model for time-dependent dielectric breakdown," IEEE Trans. Electron Devices, vol.46, no.1, pp.220–229, Jan. 1999.

[38] E. Takeda, N. Suzuki, and T. Hagiwara, "Device performance degradation due to hot-carrier injection at energies below the Si-SiO_2 energy barrier," IEEE EDM Tech. Dig., pp.396–399, 1983.

[39] C. Guerin, V. Huard, and A. Bravaix, "General framework about defect creation at the Si/SiO_2 interface," J. Appl. Phys., vol.105, no.11, pp.114513–1–114513–12, Jun. 2009.

[40] A.J. Scholten, D. Stephens, G.D.J. Smit, G.T. Sasse, and J. Bisschop, "The relation between degradation under DC and RF stress conditions," IEEE Trans. Electron Devices, vol.58, no.8, pp.2721–2728, Aug. 2011.

[41] K. Okada, "Millimeter-wave CMOS device modeling and issues," Proc. ESSCIRC, Sep. 2012. (Invited talk).

[42] N. Li, CMOS RF front-end amplifiers for integrated wireless transceivers, Ph.D. thesis, Tokyo Institute of Technology, 2010.

[43] E. Takeda and N. Suzuki, "An empirical model for device degradation due to hot-carrier injection," IEEE Electron Device Letters, vol.EDL-4, no.4, pp.111–113, Apr. 1983.

[44] L. Negre, D. Roy, F. Cacho, P. Scheer, S. Jan, S. Boret, D. Gloria, and G. Ghibaudo, "Reliability characterization and modeling solution to predict aging of 40-nm MOSFET DC and RF performances induced by RF stress," IEEE J. Solid-State Circuits, vol.47, no.5, pp.1075–1083, May 2012.

[45] L. Negre, D. Roy, S. Boret, P. Scheer, and D. Gloria, "Advanced 45nm MOSFET small-signal equivalent circuit aging under DC and RF hot carrier stress," IEEE International Reliability Physics Symposium, pp.811–814, 2011.

[46] G.T. Sasse, F.G. Kuper, and J. Schmitz, "MOSFET degradation under RF stress," IEEE Trans. Electron Devices, vol.55, no.11, pp.3167–3174, Nov. 2008.

[47] M. Tanomura, Y. Hamada, S. Kishimoto, M. Ito, N. Orihashi, K. Maruhashi, and H. Shimawaki, "TX and RX front-ends for 60 GHz band in 90 nm standard bulk CMOS," IEEE ISSCC Dig. Tech. Papers, pp.558–559, 2008.

[48] A. Siligaris, Y. Hamada, C. Mounet, C. Raynaud, B. Martineau, N. Deparis, N. Rolland, M. Fukaishi, and P. Vincent, "A 60 GHz power amplifier with 14.5 dBm saturation power and 25% peak PAE in CMOS 65 nm SOI," IEEE J. Solid-State Circuits, vol.45, no.7, pp.1286–1294, Jul. 2010.

[49] J. Chen and A.M. Niknejad, "A compact 1 V 18.6 dBm 60 GHz power amplifier in 65 nm CMOS," IEEE ISSCC Dig. Tech. Papers, pp.432–433, 2011.

[50] V. Vidojkovic, G. Mangraviti, K. Khalaf, V. Szortyka, K. Vaesen, W.V. Thillo, B. Parvais, M. Libois, S. Thijs, J.R. Long, C. Soens, and P. Wambacq, "A low-power 57-to-66GHz transceiver in 40nm LP CMOS with -17dB EVM at 7Gb/s," IEEE ISSCC Dig. Tech. Papers, pp.268–269, 2012.

[51] W. Deng, T. Siriburanon, A. Musa, K. Okada, and A. Matsuzawa, "A 58.1-to-65.0 GHz frequency synthesizer with background calibration for millimeter-wave TDD transceivers," Proc. ESSCIRC, pp.201–204, 2012.

[52] R. Wu, Y. Tsukui, R. Minami, K. Okada, and A. Matsuzawa, "A 0.7 V-to-1.0 V 10.1 dBm-to-13.2 dBm 60-GHz power amplifier using digitally-assisted LDO considering HCI issues," Proc. IEEE A-SSCC, pp.353–356, 2012.

[53] Y. Okuma, K. Ishida, Y. Ryu, X. Zhang, P.H. Chen, K. Watanabe, M. Takamiya, and T. Sakurai, "0.5-V input digital LDO with 98.7% current efficiency and 2.7-mA quiescent current in 65 nm CMOS," Proc. IEEE CICC, pp.323–326, 2010.

[54] K. Hirairi, Y. Okuma, H. Fuketa, T. Yasufuku, M. Takamiya, M. Nomura, H. Shinohara, and T. Sakurai, "13% power reduction in 16 b integer unit in 40 nm CMOS by adaptive power supply voltage control with parity-based error prediction and detection (PEPD) and fully integrated digital LDO," IEEE ISSCC Dig. Tech. Papers, pp.486–487, 2012.

[55] H. Asada, K. Bunsen, K. Matsushita, R. Murakami, Q. Bu, A. Musa, T. Sato, T. Yamaguchi, R. Minami, T. Ito, K. Okada, and A. Matsuzawa, "A 60 GHz 16 Gb/s 16QAM low-power direct-conversion transceiver using capacitive cross-coupling neutralization in 65 nm CMOS," Proc. IEEE A-SSCC, pp.373–376, 2011.

[56] W.L. Chan and J.R. Long, "A 58–65 GHz neutralized CMOS power amplifier with PAE above 10% at 1-V supply," IEEE J. Solid-State Circuits, vol.45, no.3, pp.554–564, Mar. 2010.

[57] K. Okada, N. Li, K. Matsushita, K. Bunsen, R. Murakami, A. Musa, T. Sato, H. Asada, N. Takayama, S. Ito, W. Chaivipas, R. Minami, T. Yamaguchi, Y. Takeuchi, H. Yamagishi, M. Noda, and A. Matsuzawa, "A 60-GHz 16QAM/8PSK/QPSK/BPSK direct-conversion transceiver for IEEE802.15.3c," IEEE J. Solid-State Circuits, vol.46, no.12, pp.2988–3004, Dec. 2011.

[58] M. Chiang, P. Hande, T. Lan, and C.W. Tan, "Power control in wireless cellular networks," Foundation and Trends in Networking, vol.2, no.4, pp.381–533, 2007.

[59] R. Wu, S. Kawai, Y. Seo, K. Kimura, S. Sato, S. Kondo, T. Ueno, N. Fajri, S. Maki, N. Nagashima, Y. Takeuchi, T. Yamaguchi, A. Musa, M. Miyahara, K. Okada, and A. Matsuzawa, "A HCI-healing 60GHz CMOS transceiver," IEEE ISSCC Dig. Tech. Papers, 2015. (To be presented).

[60] E. Simoen, B. Dierickx, C.L. Claeys, and G.J. Declerck, "Explaining the amplitude of RTS noise in submicrometer MOSFET's," IEEE Trans. Electron Devices, vol.39, no.2, pp.422–429, Feb. 1992.

[61] K. Miyaji, Y. Shinozuka, and K. Takeuchi, "Zero additional process, local charge trap, embedded flash memory with drain-side assisted erase scheme using minimum channel length/width standard CMOS single transistor cell," Japanese J. Appl. Phys., vol.51, pp.04DD02–1–04DD02–7, Apr. 2012.

[62] J.Y.C. Liu, A. Tang, N.Y. Wang, Q.J. Gu, R. Berenguer, H.H. Hsieh, P.Y. Wu, C. Jou, and M.C.F. Chang, "A V-band self-healing power amplifier with adaptive

feedback bias control in 65 nm CMOS," IEEE RFIC Symp. Dig. Papers, pp.1–4, 2011.

[63] V. Vidojkovic, V. Szortyka, K. Khalaf, G. Mangraviti, S. Brebels, W. van Thillo, K. Vaesen, B. Parvais, V. Issakov, M. Libois1, M. Matsuo, J. Long, C. Soens, and P. Wambacq, "A low-power radio chipset in 40nm LP CMOS with beamforming for 60GHz high-data-rate wireless communication," IEEE ISSCC Dig. Tech. Papers, pp.236–237, 2013.

[64] C. Thakkar, N. Narevsky, C.D. Hull, and E. Alon, "Design techniques for a mixed-signal I/Q 32-coefficient Rx-feedforward equalizer, 100-coefficient decision feedback equalizer in an 8 Gb/s 60 GHz 65 nm LP CMOS receiver," IEEE J. Solid-State Circuits, vol.49, no.11, pp.2588–2607, Nov. 2014.

[65] K. Okada, K. Kondou, M. Miyahara, M. Shinagawa, H. Asada, R. Minami, T. Yamaguchi, A. Musa, Y. Tsukui, Y. Asakura, S. Tamonoki, H. Yamagishi, Y. Hino, T. Sato, H. Sakaguchi, N. Shimasaki, T. Ito, Y. Takeuchi, N. Li, Q. Bu, R. Murakami, K. Bunsen, K. Matsushita, M. Noda, and A. Matsuzawa, "Full four-channel 6.3-Gb/s 60-GHz CMOS transceiver with low-power analog and digital baseband circuitry," IEEE J. Solid-State Circuits, vol.48, no.1, pp.46–65, Jan. 2013.

[66] D.Y. Yoon, C.J. Jeong, J. Cartwright, H.Y. Kang, S.K. Han, N.S. Kim, D.S. Ha, and S.G. Lee, "A new approach to low-power and low-latency wake-up receiver system for wireless sensor nodes," IEEE J. Solid-State Circuits, vol.47, no.10, pp.2405–2419, Oct. 2012.

[67] J. Choi, K. Lee, S.O. Yun, S.G. Lee, and J. Ko, "An interference-aware 5.8 GHz wake-up radio for ETCS," IEEE ISSCC Dig. Tech. Papers, pp.446–447, 2012.

[68] X. Huang, S. Rampu, X. Wang, G. Dolmans, and H. Groot, "A 2.4 GHz/915 MHz 51μW wake-up receiver with offset and noise suppression," IEEE ISSCC Dig. Tech. Papers, pp.222–223, 2010.

[69] S. Oh, N.E. Roberts, and D.D. Wentzloff, "A 116 nW multi-band wake-up receiver with 31-bit correlator and interference rejection," Proc. IEEE CICC, pp.1–4, 2013.

[70] T. Wada, M. Ikebe, and E. Sano, "60-GHz, 9-μW wake-up receiver for short-range wireless communications," Proc. ESSCIRC, pp.383–386, 2013.

[71] R. Wu, Q. Bu, W. Deng, K. Okada, and A. Matsuzawa, "A 0.015-mm^2 60-GHz reconfigurable wake-up receiver by reusing multi-stage LNAs," Proc. IEEE A-SSCC, pp.181–184, 2014.

[72] K. Kawasaki, Y. Akiyama, K. Komori, M. Uno, H. Takeuchi, T. Itagaki, Y. Hino, Y. Kawasaki, K. Ito, and A. Hajimiri, "A millimeter-wave intra-connect solution," IEEE ISSCC Dig. Tech. Papers, pp.414–415, 2010.

[73] C. Byeon, C.H. Yoon, and C.S. Park, "A 67-mW 10.7-Gb/s 60-GHz OOK CMOS transceiver for short-range wireless communications," IEEE Trans. Microw. Theory Tech., vol.61, no.9, pp.3391–3401, Sep. 2013.

[74] H. Morita, K. Uchino, E. Otani, H. Ohtorii, T. Ogura, K. Oniki, S. Oka, S. Yanagawa, and H. Suzuki, "A 12×5 two-dimensional optical I/O array for 600Gb/s chip-to-chip interconnect in 65nm CMOS," IEEE ISSCC Dig. Tech. Papers, pp.140–141, 2014.

[75] Q. Gu, Z. Xu, J. Ko, and M.C.F. Chang, "Two 10Gb/s/pin low-power interconnect methods for 3D ICs," IEEE ISSCC Dig. Tech. Papers, pp.448–449, 2007.

[76] A. Fazzi, R. Canegallo, L. Ciccarelli, L. Magagni, F. Natali, E. Jung, P. Rolandi, and R. Guerrieri, "3-D capacitive interconnections with mono- and bi-directional capabilities," IEEE J. Solid-State Circuits, vol.43, no.1, pp.275–284, Jan. 2008.

[77] N. Miura, T. Shidei, Y. Yuan, S. Kawai, K. Takatsu, Y. Kiyota, Y. Asano, and T. Kuroda, "A 0.55 V 10 fJ/bit inductive-coupling data link and 0.7 V 135 fJ/cycle clock link with dual-coil transmission scheme," IEEE J. Solid-State Circuits, vol.46, no.4, pp.965–973, Apr. 2011.

[78] N. Miura, Y. Kohama, H. Ishikuro, T. Sakurai, and T. Kuroda, "A high-speed inductive-coupling link with burst transmission," IEEE J. Solid-State Circuits, vol.44, no.3, pp.947–955, Mar. 2009.

[79] A. Siligaris, F. Chaix, M. Pelissier, V. Puyal, J. Zevallos, L. Dussopt, and P. Vincent, "A low power 60-GHz 2.2-Gbps UWB transceiver with integrated antennas for short range communications," IEEE RFIC Symp. Dig. Papers, pp.297–300, 2013.

[80] L. Kong, D. Seo, and E. Alon, "A 50mW-TX 65mW-RX 60GHz 4-element phased-array transceiver with integrated antennas in 65nm CMOS," IEEE ISSCC Dig. Tech. Papers, pp.234–235, 2013.

[81] R. Wu, W. Deng, S. Sato, T. Hirano, N. Li, T. Inoue, H. Sakane, K. Okada, and A. Matsuzawa, "A 17-mW 5-Gb/s 60-GHz CMOS transmitter with efficiency-enhanced on-chip antenna," IEEE RFIC Symp. Dig. Papers, pp.381–384, 2014.

[82] R. Wu, W. Deng, S. Sato, T. Hirano, N. Li, T. Inoue, H. Sakane, K. Okada, and A. Matsuzawa, "A 60-GHz efficiency-enhanced on-chip dipole antenna using helium-3 ion implantation process," Proc. IEEE EuMC, pp.108–111, 2014.

[83] N. Li, K. Okada, T. Inoue, T. Hirano, Q. Bu, A.T. Narayanan, T. Siriburanon, H. Sakane, and A. Matsuzawa, "High-Q inductors on locally semi-insulated Si substrate by helium-3 bombardment for RF CMOS integrated circuits," Symp. VLSI Technology Dig. Tech. Papers, pp.189–190, 2014.

[84] T. Hirano, T. Yamaguchi, N. Li, K. Okada, J. Hirokawa, and M. Ando, "60 GHz on-chip dipole antenna with differential feed," Proc. IEEE APMC, pp.304–306, 2012.

[85] H.R. Chuang, L.K. Yeh, P.C. Kuo, K.H. Tsai, and H.L. Yue, "A 60-GHz millimeter-wave CMOS integrated on-chip antenna and bandpass filter," IEEE Trans. Electron Devices, vol.58, no.7, pp.1837–1845, Jul. 2011.

[86] X.Y. Bao, Y.X. Guo, and Y.Z. Xiong, "60-GHz AMC-based circulary polarized on-chip antenna using standard 0.18-μm CMOS technology," IEEE Trans. Antennas Propag., vol.60, no.5, pp.2234–2241, May 2012.

[87] H.C. Kuo, H.L. Yue, Y.W. Ou, C.C. Lin, and H.R. Chuang, "A 60-GHz CMOS subharmonic RF receiver with integrated on-chip artificial-magnetic-conductor Yagi antenna and balun bandpass filter for very-short-range gigabit communications," IEEE Trans. Microw. Theory Tech., vol.61, no.4, pp.1681–1691, Apr. 2013.

[88] C. Liao, T.H. Huang, C.Y. Lee, D. Tang, S.M. Lan, T.N. Yang, and L.F. Lin, "Method of creating local semi-insulating regions on silicon wafers for device isolation and realization of High-Q inductors," IEEE Electron Device Letters, vol.19, no.12, pp.461–462, Dec. 1998.

[89] K.T. Chan, A. Chin, Y.B. Chen, Y.D. Lin, T.S. Duh, and W.J. Lin, "Integrated antennas on Si, proton-implanted Si and Si-on-quartz," IEEE EDM Tech. Dig., pp.40.6.1–40.6.4, 2001.

[90] K.T. Chan, A. Chin, Y.D. Lin, C.Y. Chang, C.X. Zhu, M.F. Li, D.L. Kwong, S. McAlister, D.S. Duh, and W.J. Lin, "Integrated antennas on Si with over 100 GHz performance, fabricated using an optimized proton implantation process," IEEE Microw. Wireless Compon. Lett., vol.13, no.11, pp.487–489, Nov. 2003.

[91] L.S. Lee, C. Liao, C.L. Lee, T.H. Huang, D.D.L. Tang, T.S. Duh, and T.T. Yang, "Isolation on Si wafers by MeV proton bombardment for RF integrated circuits," IEEE Trans. Electron Devices, vol.48, no.5, pp.928–934, May 2001.

[92] N. Li, K. Okada, T. Inoue, T. Hirano, Q. Bu, A.T. Narayanan, T. Siriburanon, H. Sakane, and A. Matsuzawa, "High-Q inductors on locally semi-insulated Si substrate by helium-3 bombardment for RF CMOS integrated circuits," IEEE Trans. Electron Devices, 2015.

[93] S. Zhou and M.C.F. Chang, "A cmos passive mixer with low flicker noise for low-power direct-conversion receiver," IEEE J. Solid-State Circuits, vol.40, no.5, pp.1084–1093, May 2005.

[94] C. Bryant and H. Sjöland, "A 2.45GHz, 50μW wake-up receiver front-end with -88dBm sensitivity and 250kbps data rate," Proc. ESSCIRC, pp.235–238, 2014.

[95] H. Milosiu, F. Oehler, M. Eppel, D. Fruhsorger, S. Lensing, G. Popken, and T. Thönes, "A 3-μw 868-MHz wake-up receiver with -83 dBm sensitivity and scalable data rate," Proc. ESSCIRC, pp.387–390, 2013.

[96] T. Abe, T. Morie, K. Satou, D. Nomasaki, S. Nakamura, Y. Horiuchi, and K. Imamura, "An ultra-low-power 2-step wake-up receiver for IEEE 802.15.4g wireless sensor networks," Symp. VLSI Circuits Dig. Tech. Papers, pp.1–2, 2014.

[97] X. Huang, A. Ba, P. Harpe, GuidoDolmans, H. de Groot, and J.R. Long, "A 915 MHz, ultra-low power 2-tone transceiver with enhanced interference resilience," IEEE J. Solid-State Circuits, vol.47, no.12, pp.3197–3207, Dec. 2012.

[98] N. Pletcher, S. Gambini, and J. Rabaey, "A 6μw, 1.9 GHz RF to digital baseband wakeup receiver for wireless sensor nodes," Proc. IEEE CICC, pp.539–542, 2007.

[99] E. Amat, T. Kauerauf, R. Degraeve, A.D. Keersgieter, R. Rodríguez, M. Nafría, X. Aymerich, and G. Groeseneken, "Channel hot-carrier degradation in short-channel transistors with high-k/metal gate stacks," IEEE Transactions on Device and Materials Reliability, vol.9, no.3, pp.425–430, Sep. 2009.

[100] A. Bravaix, Y.M. Randriamihaja, V. Huard, D. Angot, X. Federspiel, W. Arfaoui, P. Mora, F. Cacho, M. Saliva, C. Besset, S. Renard, D. Roy, and E. Vincent, "Impact of the gate-stack change from 40nm node SiON to 28nm high-k metal gate on the hot-carrier and bias temperature damage," IEEE International Reliability Physics Symposium, pp.2D.6.1–2D.6.9, 2013.

[101] S. Ramey, A. Ashutosh, C. Auth, J. Clifford, M. Hattendorf, J. Hicks, R. James, A. Rahman, V. Sharma, A.S. Amour, and C. Wiegand, "Intrinsic transistor reliability improvements from 22nm tri-gate technology," IEEE International Reliability Physics Symposium, pp.4C.5.1–4C.5.5, 2013.

[102] S. Liu, J. Wang, Y. Lu, D. Huang, C. Huang, W. Hsieh, J.H. Lee, Y. Tsai, J. Shih, Y.H. Lee, and K. Wu, "Self-heating effect in FinFETs and its impact on devices reliability characterization," IEEE International Reliability Physics Symposium, pp.4A.4.1–4A.4.4, 2014.

[103] M. Cho, P. Roussel, B. Kaczer, R. Degraeve, J. Franco, M. Aoulaiche, T. Chiarella, T. Kauerauf, N. Horiguchi, and G. Groeseneken, "Channel hot carrier degradation mechanism in long/short channel n-FinFETs," IEEE Trans. Electron Devices, vol.60, no.12, pp.4002–4007, Dec. 2013.

[104] K. Okada, "60GHz CMOS transceiver for 300Gb/s wireless communication," Microwave Workshops and Exhibition, 2013. (Workshop presentation).

[105] K. Yoshihisa, "Future radio access for 5G," International Workshop on Cloud Cooperated Heterogeneous Networks, 2013. (Workshop presentation).

[106] K. Takinami and N. Shirakata, "60GHz short-range wireless technologies for multi-gigabit systems," Microwave Workshops and Exhibition, 2014. (Workshop presentation).

[107] Y. Saito, Y. Kishiyama, A. Benjebbour, T. Nakamura, A. Li, and K. Higuchi, "Non-orthogonal multiple access (NOMA) for cellular future radio access," Vehicular Technology Conference, pp.1–5, 2013.

[108] V. Reddy, N. Barton, S. Martin, C.M. Hung, A. Krishnan, C. Chancellor, S. Sundar, A. Tsao, D. Corum, N. Yanduru, S. Madhavi, S. Akhtar, N. Pathak, P. Srinivasan, S. Shichijo, K. Benaissa, A. Roy, T. Chatterjee, R. Taylor, J. Krick, J. Brighton, J. Ondrusek, D. Barry, and S. Krishnan, "Impact of transistor reliability on rf oscillator phase noise degradation," IEEE EDM Tech. Dig., pp.401–402, 2009.

Appendix A

Publication List

A.1 Journal Papers

- **Rui Wu**, Yuuki Tsukui, Ryo Minami, Kenichi Okada, and Akira Matsuzawa, ”A Variable-Supply-Voltage 60-GHz PA with Consideration of HCI Issues for TDD Operation,” IEICE Transactions on Electronics, vol.E97-C, no.8, pp.803-812, Aug. 2014.
- **Rui Wu**, Wei Deng, Shinji Sato, Takuichi Hirano, Ning Li, Takeshi Inoue, Hitoshi Sakane, Kenichi Okada, and Akira Matsuzawa, ”A 60-GHz CMOS Transmitter with Gain-Enhanced On-Chip Antenna for Short-Range Wireless Interconnections,” IEICE Transactions on Electronics, vol.E98-C, no.04, Apr. 2015. (Accepted)

A.2 International Conferences and Workshops

- **Rui Wu**, Yuuki Tsukui, Ryo Minami, Kenichi Okada, and Akira Matsuzawa, ”A 0.7 V-to-1.0 V 10.1 dBm-to-13.2 dBm 60-GHz Power Amplifier Using Digitally-Assisted LDO Considering HCI Issues,” Proc. IEEE Asian Solid-State Circuits Conference (A-SSCC), Kobe, Japan, pp. 353-356, Nov. 2012.
- **Rui Wu**, Kenichi Okada, and Akira Matsuzawa, ”An AC-mode HCI Model and Output Power Management Scheme for Millimeter-wave PAs” IEEE/ACM Workshop on Variability Modeling and Characterization (VMC), San Jose, CA, Nov. 2013.
- **Rui Wu**, Wei Deng, Shinji Sato, Takuichi Hirano, Ning Li, Takeshi Inoue, Hitoshi Sakane, Kenichi Okada, and Akira Matsuzawa, ”A 17-mW 5-Gb/s 60-GHz CMOS

Transmitter with Efficiency-Enhanced On-Chip Antenna," in IEEE RFIC Symp. Dig. Papers, Tampa, FL, pp. 381-384, Jun. 2014.

- **Rui Wu**, Wei Deng, Shinji Sato, Takuichi Hirano, Ning Li, Takeshi Inoue, Hitoshi Sakane, Kenichi Okada, and Akira Matsuzawa, "A 60-GHz Efficiency-Enhanced On-Chip Dipole Antenna Using Helium-3 Ion Implantation Process," Proc. IEEE European Microwave Conference (EuMC), Roma, Italy, pp. 108-111, Oct. 2014.

- **Rui Wu**, Qinghong Bu, Wei Deng, Kenichi Okada, and Akira Matsuzawa, "A 0.015-mm^2 60-GHz Reconfigurable Wake-Up Receiver by Reusing Multi-Stage LNAs," Proc. IEEE Asian Solid-State Circuits Conference (A-SSCC), Kaohsiung, Taiwan, pp. 181-184, Nov. 2014.

- **Rui Wu**, Seitaro Kawai, Yuuki Seo, Kento Kimura, Shinji Sato, Satoshi Kondo, Tomohiro Ueno, Nurul Fajri, Shoutarou Maki, Noriaki Nagashima, Yasuaki Takeuchi, Tatsuya Yamaguchi, Ahmed Musa, Masaya Miyahara, Kenichi Okada, and Akira Matsuzawa, "A HCI-healing 60GHz CMOS transceiver," IEEE International Solid-State Circuits Conference (ISSCC), San Francisco, CA, Feb. 2015. (To be presented)

A.3 Domestic Conferences and Workshops

- **Rui Wu**, Ning Li, Kenichi Okada, and Akira Matsuzawa, "A 60-GHz digitally-controlled phase modulator with phase error calibration," IEICE Society Conference 2011, Sapporo, Japan, C-12-35, Sep. 2011.

- **Rui Wu**, Kenichi Okada, and Akira Matsuzawa, "A 0.5-V CMOS Power Amplifier with Adaptive Bias for Short-Rang Low-Power Applications," IEICE General Conference 2011, Tokyo, C-12-22, Mar. 2011.

- **Rui Wu**, Yuuki Tsukui, Ryo Minami, Kenichi Okada, and Akira Matsuzawa, "A 0.7 V-to-1.0V 10.1 dBm-to-13.2 dBm 60-GHz power amplifier using digitally-assisted LDO considering HCI issues," 電子情報通信学会 シリコンアナログ RF 研究会, Vol.RF2012-3, p.9, Dec. 2012.

- **Rui Wu**, *et al.*, "An ultra-compact 60-GHz wake-up receiver by reconfiguring multi-stage LNAs," 電子情報通信学会シリコンアナログ RF 研究会, Vol.RF2014-3, Mar. 2015. (To be presented)

- **Rui Wu**, *et al.*, ”An HCI-healing 60-GHz CMOS transceiver,” 電子情報通信学会シリコンアナログRF研究会, Vol.RF2014-3, Mar. 2015. (To be presented)

A.4 Co-Author

A.4.1 Conferences

- Kenichi Okada, Ryo Minami, Yuuki Tsukui, Seitaro Kawai, Yuuki Seo, Shinji Sato, Satoshi Kondo, Tomohiro Ueno, Yasuaki Takeuchi, Tatsuya Yamaguchi, Ahmed Musa, **Rui Wu**, Masaya Miyahara, and Akira Matsuzawa, ”A 64-QAM 60 GHz CMOS Transceiver with 4-Channel Bonding,” IEEE International Solid-State Circuits Conference (ISSCC), San Francisco, CA, pp. 346-347, Feb. 2014.

- Aravind Tharayil Narayanan, Wei Deng, Dongsheng Yang, **Rui Wu**, Kenichi Okada, and Akira Matsuzawa, ”A 0.011mm^2 PVT-Robust Fully-Synthesizable CDR with a Data Rate of 10.05 Gb/s in 28nm FD SOI,” Proc. IEEE Asian Solid-State Circuits Conference (A-SSCC), Kaohsiung, Taiwan, pp. 285-288, Nov. 2014.