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Article / Book Information

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論 文 要 旨

THESIS SUMMARY

専攻： Department of	Physical Electronics	専攻	申請学位（専攻分野）： Academic Degree Requested	博士 Doctor of	（Philosophy）
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要旨（英文 800 語程度）
Thesis Summary（approx.800 English Words）

This dissertation presents a study of reliability enhancement and power reduction solutions for 60-GHz high-data-rate transceivers in CMOS technologies.

Starting from the discussion for the key requirements of wireless transceivers in future radio access network, it shows that 60-GHz CMOS transceiver would be one of the most promising candidates with some significant challenges ahead such as hot-carrier-injection (HCI) reliability issues and low power consumption requirement.
To address the HCI issues for 60-GHz applications, a transistor-level study of HCI physical mechanism and lifetime characterization methods under DC and RF stress have been conducted. Based on the acquired knowledge, the reliability model of transistors under AC-mode HCI stress is derived to provide a valuable solution of HCI damage alleviation by limiting the operation period of high output power condition.

The proposed solution, which is realized by using variable-supply-voltage, provides a way to output superior power with high linearity and efficiency in a carefully restricted time period while satisfying the lifetime requirement. The lifetime of the implemented example PA can be improved to over 10 years with the careful arrangement of various operation supply voltages. On the other hand, the power amplifier is still able to provide 13.2dBm saturation power, 10.2dBm power at 1-dB compression point and 15.0% peak power-added efficiency at 60 GHz for high supply voltage (V_{PA}=1.0V).

Furthermore, based on the research of HCI damage mechanism, a 60-GHz CMOS transceiver with HCI damage healing function is realized by using charge ejection technique, which guarantees longer operation lifetime with high output power. The HCI-healing technique introduced in this dissertation further relieves the trade-off between the HCI reliability and the system performance. The implemented transceiver using the proposed HCI-healing technique achieves over 81-year lifetime without sacrificing the output power and efficiency. The transceiver demonstrates an output power of 9.3dBm at TX EVM = -21dB and 3.9% TX efficiency.

For the power consumption reduction of the 60-GHz CMOS transceiver, it is known that the wake-up receiver is one of the most applicable choices to systematically reduce the power consumption over time. Conventional wake-up receivers using either the 60-GHz band or lower frequency bands share the same issue of needing bulky components, which significantly increases the chip area and implementation cost. By reusing the 60-GHz LNA gain stages, the proposed 60-GHz wake-up receiver in this dissertation occupies an area overhead of only 0.015mm^2 and does not need extra antennas or switches to be integrated with the 60-GHz multi-Gb/s transceiver.

Besides reducing the time-averaged power consumption of the 60-GHz transceiver by the duty cycle control scheme, The energy efficiency potential of the 60-GHz high-data-rate transmitter is explored in this dissertation. The 60-GHz CMOS transmitter adopting the simple modulation schemes is designed and implemented using wideband and power-saving techniques, which guarantees the low-power and high-data-rate characteristic (high energy efficiency). An energy efficiency of 3.4pJ/bit is achieved in BPSK with the 3-dB bandwidth of 9GHz. The data rate (5Gb/s) is mainly limited by the maximum sampling frequency of the AWG and the insufficient local oscillator signal power.

At last, this dissertation is concluded with the insight that the combination of the proposed techniques and solutions in this research can help to achieve the reliable low-power high-data-rate 60-GHz transceivers in CMOS processes. Future researches are also discussed in the end of this dissertation.

備考 ： 論文要旨は、和文 2000 字と英文 300 語を 1 部ずつ提出するか、もしくは英文 800 語を 1 部提出してください。
Note : Thesis Summary should be submitted in either a copy of 2000 Japanese Characters and 300 Words (English) or 1copy of 800 Words (English).

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