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Thesis Outline

Charge-Domain Time-to-Digital Converter and Its Application to Fractional-N Frequency Synthesizer

（電荷領域時間デジタル変換器および分数周波数シンセサイザーへの応用）

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This doctoral dissertation is titled as “Charge-domain Time-to-Digital Converter and Its Application to Fractional-N Frequency Synthesizer”, composed of 7 chapters.

Chapter 1 introduces the background and the scope of this doctoral research on high-resolution TDC and low-noise fractional-N digital PLL. The resolution limitation of a delay chain TDC is analyzed, and the high-resolution capability of quantizing time in charge domain is explained. The proposal for the TDC is briefly described, followed by the definition of the term “charge domain TDC”. The basic issues in analog and digital PLLs are discussed. The introduced in-band phase noise of a digital PLL from the delay chain is calculated, while the design target requires the improvement by around 20 dB. The research target is clarified as: a wideband low noise fractional-N digital PLL with low power and small area, which necessities a breakthrough in the performance of the TDC.

Chapter 2 overviews recent TDC architectures, summarizes the main technique of each type, and discusses their advantages and disadvantages. Finally, the resolution, FoM, and area are benchmarked.

Chapter 3 overviews conventional analog TDCs and presents a SAR-ADC-based TDC. While other types of ADCs can be chosen, the conventional analog TDCs use counter-based ones or ΔΣ architectures, suffering from low resolution and narrow bandwidth. The reason for such compromise is discussed by overviewing ADC architectures. The overview reveals that the SAR-ADC is the best choice in terms of energy efficiency and area. A proposed solution is then presented using a G_m-C integrator to translate time difference into charge, and a SAR-ADC to quantize this

charge. With 90 nm CMOS, the presented TDC achieves 1 ps resolution without calibration, and the SAR-ADC overcomes the issues of speed, resolution, power, and area in conventional analog TDCs. However, the G_m-C integrator consumes high power and large area, which is unsuitable for a digital PLL.

Chapter 4 presents TDCs for the targeted PLL with high resolution, low power, and small area, using a pseudo-differential charge pump and a SAR-ADC. To satisfy with the in-band phase noise requirement of the PLL, the intrinsic noise of the proposed TDC is analyzed. The analysis can be regarded as a design guide for this type of TDCs in deciding the sampling capacitance and ADC's resolution. The simulation and measurement are consistent with the analysis. With 65 nm CMOS, the presented TDC achieves 0.8 ps resolution, with around 1 LSB intrinsic noise, 2.9 mW power consumption at 50 MS/s, and 0.018 mm^2 area. The TDC achieves the target as a building block for the proposed digital PLL. Moreover, comparing with the ones with same level of performance, the proposed TDC achieves best energy efficiency and area, as shown in Chapter 7.

Chapter 5 discusses the design considerations and estimated noise performance of a digital fractional-N PLL. Two types of TDC-based architectures are compared and the counter-based one is chosen. The phase noise of the ADPLL is analyzed. The analysis shows that with 3.6 GHz output and 50 MHz reference frequencies, around -107 dBc/Hz in-band phase noise is expected.

Chapter 6 presents a fractional-N digital PLL using the proposed TDC. To interface the TDC with the DCO in a counter-based architecture, a pulse gating circuit is proposed without using reference retiming to avoid the risk of metastability. To achieve high frequency resolution without introducing voltage-dependent and ΔΣ noises, a varacter-less and non-ΔΣ small area DCO is proposed, achieving 7 kHz frequency resolution. To suppress fractional spurs due to gain mismatch in time-to-phase conversion, a dual-loop LMS gain calibration is proposed, concerning with the current mismatch in the charge pump. With 65 nm CMOS, the measured in-band phase noise is -107.3 dBc/Hz in fractional-N mode. This result is consistent with the measured TDC performance in Chapter 4, and the phase noises estimation in Chapter 5. The power consumption is 8 mW, and the area is 0.38 mm^2. With 1 MHz loop bandwidth, the integrated jitter (1 – 10 MHz) is 0.425 ps. This translates to -238.4 dB FoM_j. This performance has outperformed most state-of-the-arts wideband fractional-N analog

PLLs, and is comparable with digital ones. Considering the same level of in-band phase noise, the proposed PLL achieves lowest power and smallest area owing to the proposed charge-domain TDC. This reveals that the performance can be further improved by revising the design of other building blocks.

Chapter 7 draws the conclusion and describes future works. This doctoral research is completed with a sub-picosecond resolution TDC with best energy efficiency and smallest area compared with state-of-the-arts, and a low-noise wideband digital fractional-N PLL with low power and small area, using the proposed TDC. Toward the technology scaling with lowered supply voltage and shortened channel length, possible solutions are discussed. Finally, future directions on the proposed TDC and PLL are considered, for further lowed noise, power consumption, and area.