論文 / 著書情報
Article / Book Information

Title	An All-Digital Reconfigurable Time-Domain ADC for Low-Voltage Sensor Interface in 65nm CMOS Technology
Authors	Yu Hou, Takamoto Watanabe, Masaya Miyahara, Akira Matsuzawa
Citation	IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences, Vol. E98-A, No. 2, pp. 466-475
Pub. date	2015, 2
URL	http://search.ieice.org/
Copyright	(c) 2015 Institute of Electronics, Information and Communication Engineers

IEICE TRANSACTIONS

on Fundamentals of Electronics, Communications and Computer Sciences

VOL. E98-A NO. 2
FEBRUARY 2015

A PUBLICATION OF THE ENGINEERING SCIENCES SOCIETY
The Institute of Electronics, Information and Communication Engineers
Kikai-Shinko-Kaikan Bldg., 5-8, Shibakoen 3 chome, Minato-ku, TOKYO, 105-0011 JAPAN

IEICE TRANS. FUNDAMENTALS, VOL.E98–A, NO.2 FEBRUARY 2015

PAPER Special Section on Analog Circuit Techniques and Related Topics

An All-Digital Reconfigurable Time-Domain ADC for Low-Voltage Sensor Interface in 65 nm CMOS Technology

Yu HOU[†a)], ***Nonmember***, **Takamoto WATANABE**[††], **Masaya MIYAHARA**[†], ***Members***, ***and*** **Akira MATSUZAWA**[†], ***Fellow***

SUMMARY An all-digital time-domain ADC, abbreviated as TAD, is presented in this paper. All-digital structure is intrinsically compatible with the scaling of CMOS technology, and can satisfy the great demand of miniaturized and low-voltage sensor interface. The proposed TAD uses an inverter-based Ring-Delay-Line (RDL) to transform the input signal from voltage domain to time domain. The voltage-modulated time information is then digitized by a composite architecture namely "4-Clock-Edge-Shift Construction" (4CKES). TAD features superior voltage sensitivity and 1st-order noise shaping, which can significantly simplify the power-hungry pre-conditioning circuits. Reconfigurable resolution can be easily achieved by applying different sampling rates. A TAD prototype is fabricated in 65 nm CMOS, and consumes a small area of 0.016 mm^2. It achieves a voltage resolution of 82.7 μV/LSB at 10 MS/s and 1.96 μV/LSB at 200 kS/s in a narrow input range of 0.1 Vpp, merely under 0.6 V supply. The highest SNR of TAD prototype is 61.36 dB in 20 kHz bandwidth at 10 MS/s. This paper also analyzes the nonideal effects of TAD and discusses the potential solutions. As the principal drawback, nonlinearity of TAD can be compensated by the differential-setup and digital calibration.

key words: *all-digital, reconfigurable resolution, TAD, low-voltage, sensor interface*

1. Introduction

Advanced sensor is a key technology to realize various electronic systems, such as automotive sub-systems, wearable devices, and health monitoring systems [1]–[3]. Generally speaking, a sensor consists of sensing element, interface circuit, and digital signal processor (DSP), as shown in Fig. 1(a). In particular, interface circuit is the bridge between physical world and digital realm.

While the scaling of CMOS technology meets the great demand of miniaturized and low-power sensors in recent years, it makes the design of conventional analog sensor interface more difficult. In order to overcome the ever-lowering supply voltage, there has been a great deal of research. For instance, Successive-Approximation-Register (SAR) ADC gains its popularity because of the superb power efficiency [4], especially under low supply voltage [5]. Despite SAR ADC is compatible with the scaling of CMOS technology, it usually requires a rail-to- rail input signal to guarantee a high SNR (Signal-to-Noise Ratio). LNA (Low-Noise Amplifier) and VGA (Variable-Gain Amplifier) are typically required as the pre-conditioning circuits. In addition, analog LPF (Low-Pass Filter) is necessary to suppress the noise occurring during the signal amplification. LNA, VGA and LPF inevitably consume expensive power and area overhead.

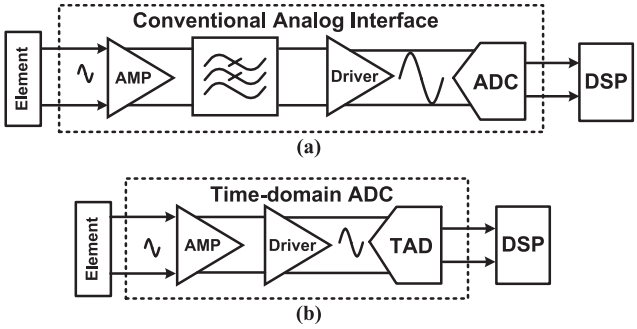


Fig. 1 (a) Conventional sensor interface; (b) Time-domain ADC.

Aforementioned, the conventional design paradigm is probably not suitable for energy-constrained sensors. New ADC topologies, which can maximally simplify the power-hungry analog conditioning circuits, are highly demanded. Among numerous candidates, the all-digital time-domain ADC (TAD) proposed in [6] is probably the primary choice, as shown in Fig. 1(b).

Different from the conventional ADCs, TAD requires a much narrower input range. An 11-bit, 100 kS/s TAD with 200 mV input range is reported in [6]. Narrow input range of TAD significantly relaxes the requirement of its VGA. Moreover, TAD can generate a low-pass filtering effect simultaneously with A/D conversion. Therefore, TAD can tolerate high-frequency noise in input signal. Analog pre-filter could be eliminated by the combination of TAD and digital post-filter [6]. And, the power-hungry low-impedance input buffer is not required to guarantee the input purity.

TAD is able to convert the weak output voltage of sensing element (V_{in}) into high-resolution digital data (DT) without the presence of high-gain amplifiers. In another word, TAD is highly sensitive to input voltage variation. Here, we define a parameter, namely voltage resolution, to represent the voltage sensitivity of TAD, which is expressed in Eq. (1).

$$voltage\ resolution = \frac{V_{in,\max} - V_{in,\min}}{DT_{\max} - DT_{\min}} \quad (1)$$

All-digital configuration is another advantage of TAD. It's easier to scale or port in other CMOS technologies. TAD

Manuscript received May 21, 2014.
Manuscript revised October 3, 2014.

[†]The authors are with the Department of Physical Electronics, TokyoInstitute of Technology, Tokyo, 152-8552 Japan.
[††]The author is with DENSO CORPORATION, Kariya-shi, 448-8661 Japan.
a) E-mail: houyu@ssc.pe.titech.ac.jp

DOI: 10.1587/transfun.E98.A.466

with similar architecture has been demonstrated in 0.8 μm, 0.65 μm, 0.35 μm, 0.18 μm, and 65 nm CMOS. The statistical data of voltage resolution, area and power consumption of these TADs are available in [7], which proves that CMOS scaling can improve TAD's voltage sensitivity. So far, the best voltage resolution of TAD is 15 μV/LSB, achieved at 1 MS/s in 65 nm CMOS process under 1.2 V supply voltage [7].

A novel architecture is firstly proposed in [8], namely "4-Clock-Edge-Shift Construction" (4CKES). It helps TAD break the fundamental limit set by technology. A 0.65 μm-CMOS TAD has been demonstrated to achieve the same voltage resolution as TAD in 0.25 μm CMOS.

The target of this work is to demonstrate the feasibility of 4CKES scheme in 65 nm CMOS. Especially, it aims to investigate the performance of TAD with narrow input range under ultra-low supply voltage. In addition, a simple but effective metastable prevention scheme is also proposed to refine the circuit design. Moreover, TAD's characteristics are theoretically analyzed and verified by simulation, which could help the system-level design.

The rest of this paper is organized as follows. Section 2 explains the operation principle of TAD. Section 3 briefly analyzes its characteristics. Section 4 describes the proposed architecture. Next, Sect. 5 presents the measurement results of TAD prototype. In the end, Sect. 6 concludes this paper.

2. Operation Principle

The operation principle of TAD involves a two-step conversion: (1) voltage-to-time conversion or voltage-to-delay conversion, (2) time-to-digital conversion.

2.1 Voltage-to-Time Conversion

Figure 2(a) shows an inverter-based delay line, wherein two adjacent inverters comprise a delay unit (DU). The delay of DU (T_d) can be modulated by its supply voltage (V_{in}), as expressed in [6]:

$$T_d(V_{in}) = \frac{bC_L V_{in}}{(V_{in} - V_{th})^a} : \quad a = 1.4\text{–}1.6 \tag{2}$$

where b and a are technology-dependent constants, C_L is the load capacitance, and V_{th} is the threshold voltage.

Figure 2(b) shows the delay-to-voltage characteristic of DU in 65 nm CMOS. It illustrates that T_d is inversely monotonic with V_{in}. T_d is however not sensitive to input variation (ΔV_{in}) in the high-voltage region, which reveals a tradeoff between DU's speed and its voltage sensitivity. Another tradeoff exists between the input range of DU and its linearity. As shown in Fig. 2(b), wide input range has to be sacrificed for achieving the acceptable linearity. While narrow input range is indeed undesired by the conventional ADCs, it guarantees TAD a better linearity.

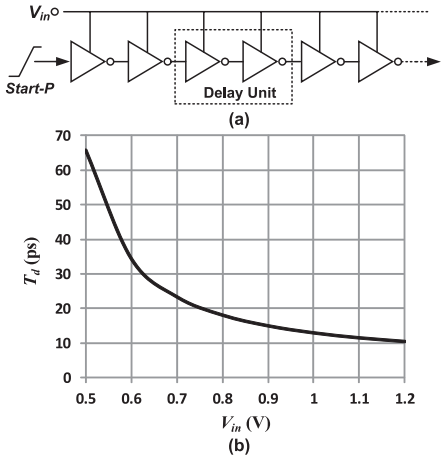


Fig. 2 (a) Schematic of inverter-based delay line; (b) Delay-voltage characteristic of delay unit in 65 nm CMOS, when it only loads next delay unit.

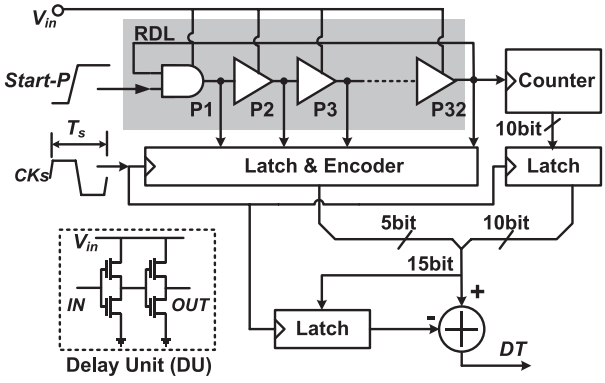


Fig. 3 Basic block diagram of TAD.

2.2 Time-to-Digital Conversion

Figure 3 illustrates the basic block diagram of TAD. A start pulse (*Start-P*) is responsible to activate the Ring-Delay-Line (RDL). The oscillation mechanism of even-stage RDL is explained in [9]. Simply speaking, *Start-P* passes a number of delay units (DUs) across RDL in a specific time (sampling period T_s). The stage number is then digitized by a frequency counter and other digital modules. In detail, counter digitizes the number of cycles that *Start-P* travels across RDL. "Latch and Encoder" digitizes the position of *Start-P* in RDL. Then, subtractor calculates the output difference in two sampling periods as the final output. When sensor is expected to power off the battery, TAD can be easily suspended by switching *Start-P* to the ground. This function is quite suitable for adaptive low-power sensor applications.

Once TAD is triggered by the start signal, it operates continuously without any dead time. No sample-and-hold circuit is required. It integrates the input voltage within the sampling period T_s. The digital output of TAD actually reflects the moving average of input voltage ($V_{in,average}$) during T_s. This intrinsic 1st-order LPF feature has been theoretically analyzed and verified in [10].

The 1st-order noise-shaping characteristic is invaluable to simplify TAD's input buffer. As shown in Fig. 3, inverter switching causes supply bounce, which imposes a high-frequency noise on input signal. Fortunately, the TAD combined with a digital post-filter could effectively remove this noise [6]. Consider that input bandwidth for sensor application is typically narrower than 100 kHz, a relatively high-impedance, narrow-bandwidth buffer is enough for TAD. In addition, the supply current of input buffer's output stage can be reused as supply currents for RDL [11]. In 65 nm CMOS process, supply current for RDL oscillating at several hundred megahertz (MHz) is only several tens of microampere (μA). Apparently, the power consumption of TAD's buffer is not an important problem. The output range of buffer can be controlled by conventional common-mode feedback (CMFB) method [11]. The common-mode (CM) output is stabilized at a reference voltage. The power consumption of reference generator is small since it only drives one input transistor of CMFB circuit.

Let's consider the design requirements of input buffer and reference buffer for high-resolution SAR ADC. The capacitive-DAC (CDAC) must be very large to meet the kT/C noise and element matching requirements. Either a small low-frequency output impedance buffer or a large reference decoupling capacitor is necessary. The power or area consumption would be expensive. In addition, the reference buffer must have enough driving ability to complete accurate CDAC settling in the short bit-cycling time. Aforementioned, TAD needs a less sophisticated input buffer and reference buffer than SAR ADC.

The digital output of TAD, namely DT, equals to:

$$DT = \left\lfloor T_s / T_d(V_{in,average}) \right\rfloor = \left\lfloor \frac{T_s (V_{in,average} - V_{th})^a}{bC_L V_{in,average}} \right\rfloor \quad (3)$$

In order to increase TAD's output resolution, a small $T_d(V_{in,average})$ is desirable. It's well known that CMOS scaling can shorten the gate delay of inverter. In the same condition of input range and sampling period, TAD in advanced technology will have a higher output resolution and voltage resolution as shown in Eq. (1). This explains why TAD's voltage resolution is improved as the CMOS scaling goes on.

Equation (3) also reveals the superb flexibility of TAD. Reconfigurable voltage resolution can be easily achieved by changing the sampling frequency ($1/T_s$). Thanks to this feature, TAD with no significant architectural change has been implemented in many sensor applications. For example, the high-resolution Magneto-Impedance (MI) sensor [12], rotational-gyro/accelerometer [13], and time measurement ASIC [14] have been implemented by TAD in low, intermediate, and high-speed clock, respectively.

3. Characteristics

3.1 Signal-to-Quantization-Noise Ratio

As analyzed in Sect. 2, the quantization noise of TAD is 1st-order shaped. The SQNR (Signal-to-Quantization- Noise Ratio) of TAD is similar to that of a conventional 1st-order delta-sigma ADCs [11]:

$$SQNR = 20\log_{10}\left(\frac{3}{\pi\sqrt{2}} \cdot \sqrt{\frac{f_s}{BW^3}} \cdot \frac{1}{V_{d,average}} \cdot \frac{\Delta f_{rms}}{f_o}\right) \quad (4)$$

where f_s is the sampling frequency of TAD, BW is the bandwidth, $\Delta f_{rms}/f_o$ is the oscillation frequency deviation of N-stage RDL due to the input voltage modulation.

A TAD in the architecture shown in Fig. 3 is simulated to verify the feasibility of Eq. (4). During the simulations, it is assumed that f_s is 40 MHz, as applied in the time-measurement ASIC [14]. The performances of TAD in different voltage regions are summarized in Table 1.

Table 1 Summary of simulation results in different voltage ranges where f_s = 40 MHz, BW = 10 MHz.

V_{in} range (V)	0.5-0.6	0.7-0.8	0.9-1.0
$VDDL$ (V)	0.6	0.8	1.0
$T_{d,average}$ (ps)	109.9	60.4	26.05
Δf_{rms} (MHz)	64.27	71.51	61.28
f_o (MHz)	298.6	763.3	1203.0
$SQNR_{calculation}$	48.44 dB	49.72 dB	48.43 dB
$SQNR_{simulation}$	47.32 dB	47.78 dB	48.10 dB
Power (μW)	37.88	150.47	394.04

Table 1 proves that Eq. (4) is feasible to estimate the SQNR of TAD. It's also interesting to note that although high voltage operation can accelerate the transition time of DU, it can't improve SQNR significantly. Take power into account, low voltage operation is more favorable.

In the real circumstances, non-ideal effects, such as sampling jitter, mismatch of RDL stages, phase noise of RDL, and metastability of digital circuits degrade the performance. These non-ideal effects will be analyzed in this section. Then, the system-level design considerations of TAD will be discussed.

3.2 Sampling Clock Jitter

In certain sense, TAD can be regarded as a TDC with reconfigurable time resolution (T_d). Sampling clock (T_s) serves not only for sampling the input signal but also as the time window to be quantized. Accordingly, jitter of sampling clock can be divided into two parts [15]: the sampling uncertainty and the error of input time window.

The effect of the former is apparently the same as that of those conventional ADCs. Let's analyze the latter here. In the sensor applications where quartz crystal oscillators can be utilized as reference clock, sampling jitter is far smaller than the time resolution of TAD. Sampling jitter is not an important problem in this case. As for the area-constrained applications, a built-in oscillator is typically needed. Jitter level is larger than the delay of DU. Given a certain jitter level, it's intuitive to think that a large T_d can reduce output variation. After all, it will result in less erroneous code. This conjecture is confirmed by [15]. As shown in Table 1, low-voltage operation can meet this very need. It's

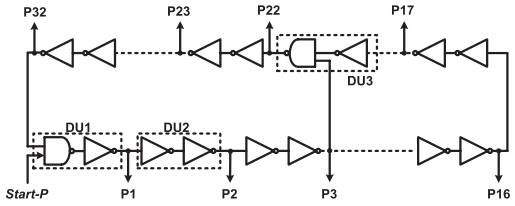


Fig. 4 Even-stage RDL comprising 3 types of delay units (DUs).

another proof that TAD is suitable for low-voltage application. Moreover, sensor applications usually use oversampling. The requirement of sampling jitter can be effectively relaxed by TAD's 1st-order noise-shaping feature combined with oversampling.

3.3 Mismatch of RDL Stages

Local temperature and process variation will introduce delay mismatch of RDL stages, denoted as $\Delta T_{d,mismatch}$. Delay mismatch yields deterministic and periodic error, which significantly degrades the linearity. Because each stage of RDL is independent from the other stages, delay mismatch will accumulate across the RDL. Thereby, a small number of RDL stages are desired for mismatch suppression. This conclusion has already been verified by Monte-Carlo simulation in [16].

Different from the conventional ring VCO, even-stage RDL of TAD has 3 types of delay units (DUs), as shown in Fig. 4. In this work, the feature size of these DUs has been cautiously chosen so as to minimize the delay mismatch of 3 different DUs. Nevertheless, it's difficult to ensure a satisfactory mismatch over wide input range. A narrow input range is better for suppressing mismatch.

3.4 Phase Noise of RDL

Flicker noise and white noise can randomly shorten or lengthen the delay of inverter. The resulted jitter or phase noise have been studied in previous works [17], [18].

Reference [17] and [18] proves that phase noise due to white noise is independent of the number of delay stages. It's the total gate capacitance and power consumption of RDL that determines phase noise. To suppress the phase noise due to white noise, a large power should be burnt.

In [18], a compact equation of phase noise due to flicker noise is derived, which reveals that the key to reduce the phase noise due to flicker noise is also to increase the total gate capacitance. The scaling of CMOS technology lowers gate capacitance and supply voltage. As a result, a longer RDL should be used for maintaining a satisfactory phase noise.

However, the bandwidth of sensor is typically narrow. A short RDL is actually more helpful to suppress in-band phase noise, since the free-running frequency of RDL is pushed far away from the interested low-frequency band. Furthermore, in-band phase noise is 1st-order shaped by TAD. Phase noise of RDL is therefore trivial to TAD's performance.

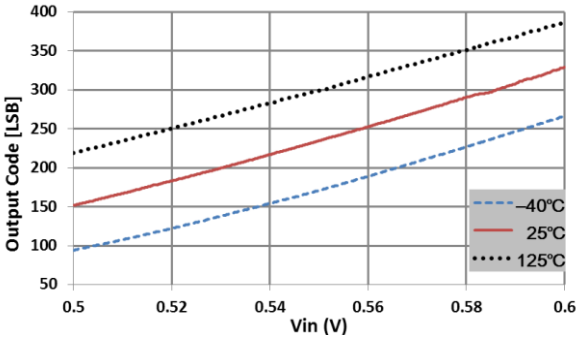


Fig. 5 Simulated characteristicin wide temperature range.

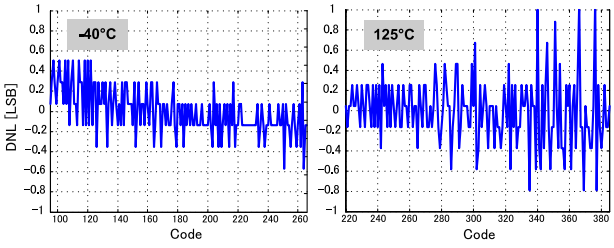


Fig. 6 DNL characteristic of TAD at −40°C and 125°C.

Table 2 Simulation results summary in wide temperature range.

Supply (V)	0.6		
V_{in} span (V)	0.5-0.6		
f_s (MS/s)	40		
Temperature	-40 ℃	25 ℃	125 ℃
Output code	94-267	152-329	219-386
Sensitivity	578.0 uV/LSB	565.0 uV/LSB	598.9 uV/LSB
DNL (LSB)	[-0.57, +0.50]	[-0.78, +1.20]	[-0.79, +1.09]

3.5 Effect of Temperature Variation

All-digital structure grants TAD superior environmental durability including even for strict automobile conditions. In [14], the characteristic of a 40 MS/s TAD has been experimentally confirmed in a wide range of temperature from −40°C to 125°C.

In order to verify the environmental durability of TAD under ultra-low supply voltage, TAD used in Sect. 3.1 is simulated at −40, 25, 125°C, respectively. Throughout the simulations, a ramp signal in range of 0.5–0.6 V is quantized by TAD at 40 MS/s. The simulation results are shown in Fig. 5. For all the simulations, we confirm the stable operation of TAD with monotonic characteristic. Figure 6 shows the DNL characteristic of TAD at −40 and 125°C, which reveals that there is no missing code. Table 2 summarizes the simulation results in the wide temperature range.

The resolution drift can be resolved by a conventional "dual-slope" digital correction method [6], [19]. TAD can alternatively quantize a reference signal V_{ref} and sensed signal V_{in}. The output data ratio $DT(\mathrm{V}_{in})/DT(\mathrm{V}_{ref})$ is then nor-

malized by a N-bit digital divider. The final output is calculated by Eq. (5). Normalization correction should be performed periodically due to temperature drift.

$$DOUT = \frac{DT(V_{in})}{DTV_{ref}} \times 2^N \tag{5}$$

3.6 System-Level Design Consideration

As TAD's core, RDL determines the overall performance. Sections 3.3 and 3.4 reveal that a short RDL is preferred to reduce performance degradation due to mismatch and phase noise. It however feeds counter a higher oscillation frequency, which necessitates a high-speed, high-power, high-resolution counter. This work uses ultra-low supply voltage to lower TAD's power. Unfortunately, it reduces the maximum input frequency of counter. To ensure an enough operation margin of counter, RDL shouldn't be too short. In [8], a 16-DU RDL is optimized for 0.65 μm-CMOS TAD. The time-resolution of proposed TAD is improved by 65 nm CMOS technology. A longer RDL is expected to guarantee the operation margin of counter, which makes DNL degradation due to mismatch become more severe. In addition, complex "latch and encoder" increases the overall power consumption.

Based on above considerations, the proposed TAD chooses a 32-stage RDL. The counter resolution depends on the specific applications. This work aims to exploit the achievable resolution of TAD in both high-speed and low-speed mode. Therefore, a 10-bit counter is used to meet the needs of low-speed mode.

4. Circuit Structure

Figure 7(a) illustrates the block diagram of proposed 17-bit 4CKES-TAD. It consists of two major blocks: (1) a 32-stage RDL driven by input voltage (V_{in}), (2) a time quantizer including a 10-bit frequency counter and four 5-bit encoders and other arithmetic circuits, which use a common supply (*VDDL*).

The basic idea of 4CKES-TAD is to sample the phase and frequency information of RDL by 4 different clocks (*CK1-CK4*) during one T_d. Figures 7(b) and 7(c) show the timing chart of clocks (*CK1-CK4*) and the schematic of clock buffer. This *CK1-4* shift timing is simply provided with modified switching-level inverters as a clock-buffer. Taking input voltage variation and the jitter induced by CKES generator into account, all the delay time from CKs to CK1-CK4, as shown in Fig. 7(c), are time-variant. In this work, CKES generator uses large-size transistors to lower jitter level [17]. The short delay lines are utilized to ensure the accumulated jitter much smaller than T_d, especially under ultra-low supply. The 1st-order noise shaping feature will further suppress jitter. With the help of transient-noise simulation, the moving average of Δt is designed to approximately equal to $T_d(V_{in,average})/4$ within the narrow input span (0.5–0.6 V).

One advantage of 4CKES-architecture is to suppress the metastability of encoder. Encoder is very vulnerable to the metastability problem if only one clock is imposed which results in one LSB mistake. In the case of 4CKES-TAD, only one encoder may suffer from metastability. The defective data is then averaged by the correct data from other encoders. The four sets of 15-bit data (*DT1, DT2, DT3,*

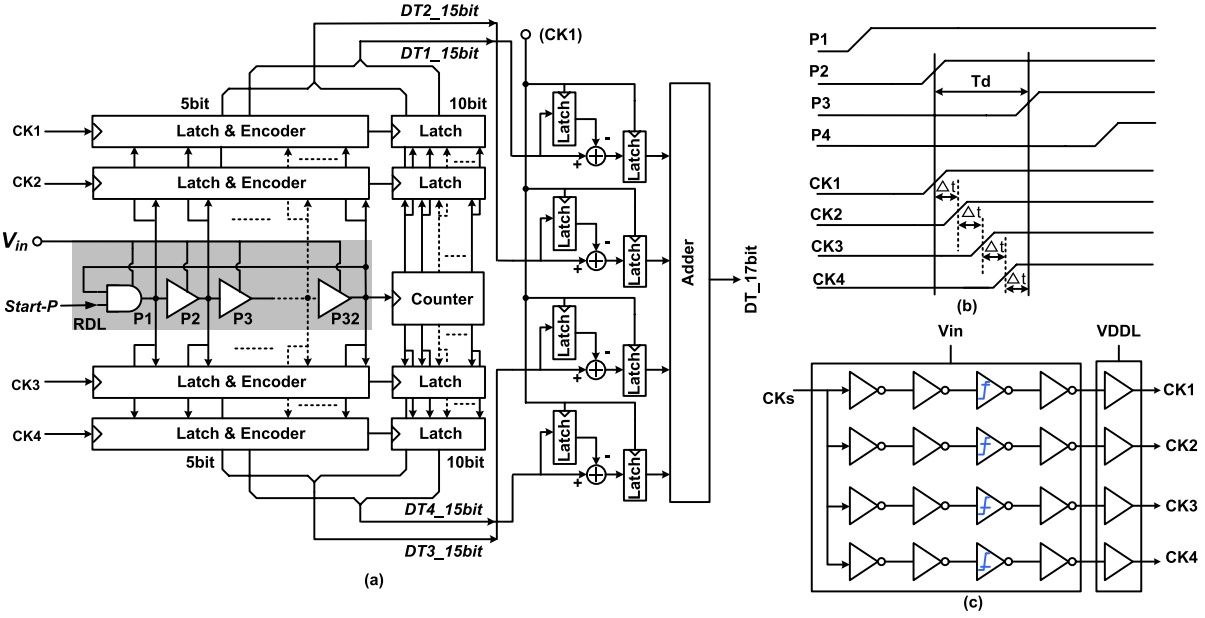


Fig. 7 (a) Block diagram of 4CKES-TAD; (b) Timing chart of sampling clocks CK1-CK4; (c) Schematic of clock generator.

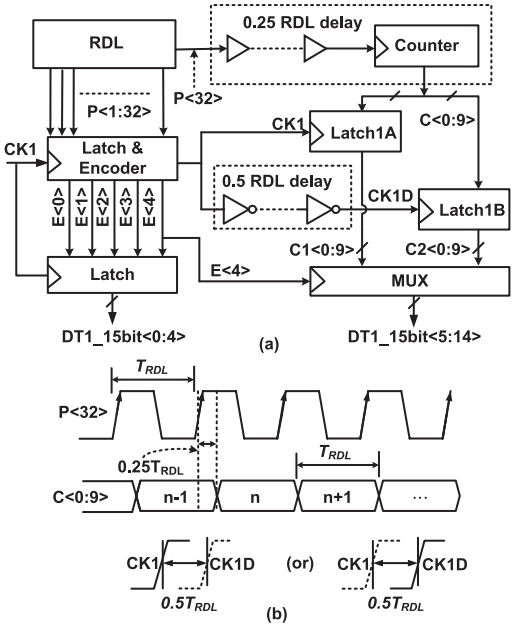


Fig. 8 (a) Metastability cancellation for the latch of counter; (b) timing chart.

DT4) are combined to generate 17-bit output. The extra 2-bit output resolution is another advantage of 4CKES-TAD over the conventional one.

Needless to say, metastability occurring in the latch of counter must also be precluded. The mechanism to avoid metastability is quite similar with the 4CKES method. As illustrated in Fig. 8 the output of counter is saved into 2 latches, which are synchronized by *CK1* and *CK1D*, respectively. Either *CK1* or *CK1D* may suffer from metastabiltity, as indicated by the dashed line. The metastable data can then be rejected by the mechanism introduced below.

In Fig. 8, MSB of the output of encoder ($E[4]$) equals to 0 if the start pulse (*Start-P*) is in the range of $[P1 - P16]$ when sampling clock (*CKs*) comes, otherwise $E[4] = 1$. If *CKs* arrives at the moment of *Start-P* in the vicinity of *P32 and P1*, the latch of counter may suffer from metastability. That is, metastbility error of counter's latch may happen when $E[4]$changes from 1 to 0.

In this work, we insert several buffers before counter to postpone the meta-stability window. These buffers and counter itself introduce 25% of oscillation period of RDL (T_{RDL}) approximately. As a result, metastability only happen when $E[4] = 0$. Accordingly, the correct output of counter can be sampled when $E[4] = 1$:

$$DT1\_15\,\text{bit}\langle 14:5\rangle = \begin{cases} C1\langle 9:0\rangle, & if \;\; E[4] = 1 \\ C2\langle 9:0\rangle, & if \;\; E[4] = 0 \end{cases} \tag{6}$$

5. Evaluation of TAD Prototype

The TAD prototype was fabricated in a 65 nm CMOS technology, and the die micrograph is shown in Fig. 9. TAD core occupies an area of 0.016 mm^2. In this section, the measured results will be presented. And, the potential methods for performance improvement will be discussed.

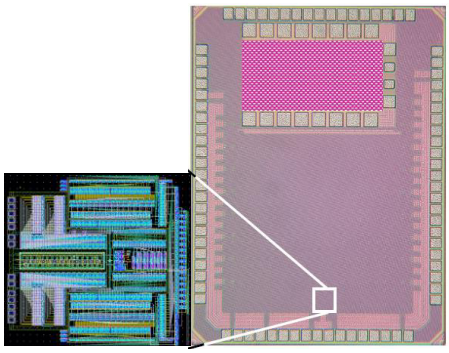


Fig. 9 Layout plot of TAD core (120 μm × 135 μm) and its test-chip micrograph (1.5 mm × 2.0 mm).

Table 3 Sensitivityof TAD prototype at different conversion rates.

Supply (V)	0.6		
V_{in} span (V)	0.5-0.6		
Area(mm^2)	0.016		
Conversion rate	200 kS/s	1 MS/s	10 MS/s
Resolution (bit)	15.7	13.5	10.2
Sensitivity(μV/LSB)	1.96	8.6	82.7

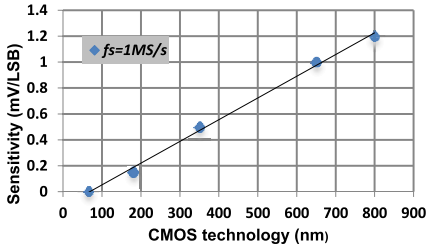


Fig. 10 Voltage resolution vs. CMOS technology at 1 MS/s.

5.1 Measurement Results

Table 3 shows the output resolution of TAD in different conversion rates. In the measurements, TAD quantizes a ramp signal ranging from 0.5–0.6 V under 0.6 V supply.

In Table 3, output resolution of TAD is defined as:

$$resolution = \log_2 (DT_{\max} - DT_{\min}) \tag{7}$$

Figure 10 shows TAD's voltage resolution in different CMOS technologies from 0.8 μm to 65 nm [7], including this TAD prototype. It proves that TAD is compatible with CMOS scaling, since voltage resolution is almost perfectly scalable with technology.

Table 4 summarizes the SNR performance at different conversion rates when V_{in} = [0.5 V, 0.6 V], $VDDL$ = 0.6 V. During the test, a digital LPF in software configures the bandwidth of interest as 20 kHz. TAD prototype aims to quantize a very narrow input range under ultralow supply. As shown in Table 4, a high oversampling ratio is helpful to improve SNR in this condition. If low-frequency clock is required by high-resolution application specification, a larger

Table 4 SNR of TAD prototype at different conversion rates when $VDDL$ = 0.6 V, V_{in} = 0.5–0.6 V, and BW = 20 kHz.

f_s (S/s)	f_{in} (kHz)	Resolution	SNR(dB)	Power(μW)
200k	9.99	15.7bit	50.64	63.1
1M	9.98	13.5bit	56.93	75.4
10M	8.54	10.2bit	61.36	93.2

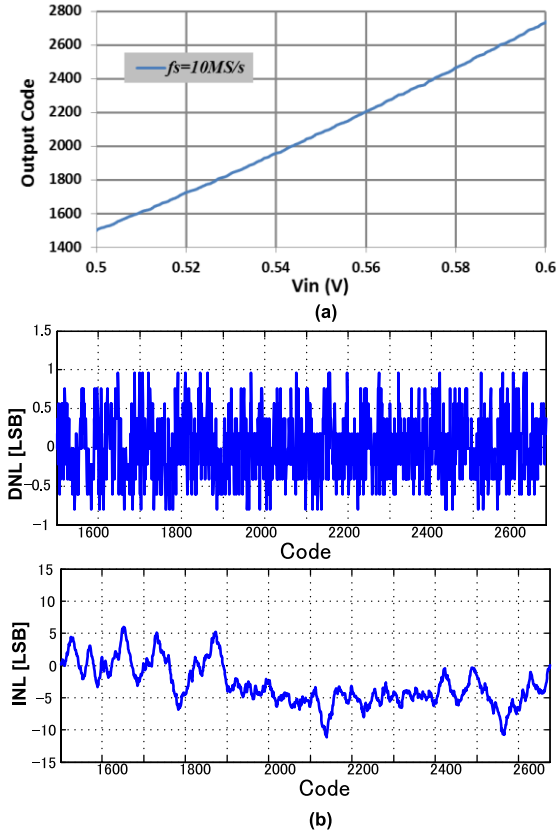


Fig. 11 (a) Static characteristic at 10 MS/s; (b) DNL and INL.

input range should be used. In that case, some linearity calibration techniques should be applied, which will be introduced in the next section.

Figure 11 presents the static characteristic and the DNL/INL of TAD prototype at 10 MS/s. The measured DNL is +0.96/−0.80 LSB, the INL is +5.95/−11.13 LSB. In several sensor applications where sensor is placed in a feedback system, INL requirement is not stringent. For example, TAD is responsible to keep an MEMS sensing element in the null position for the force-balance servo-system in [13], where TAD is used to detect the displacement from null position. TAD's relatively poor INL characteristic is not a problem to these applications.

5.2 Discussion: Nonlinearity Correction Methods

Several effective methods to correct TAD's nonlinearity have been studied in previous work, such as TAD consisting of linear delay element [20], K-locked loop [21], and digital background calibration using replica-VCO [22]. These

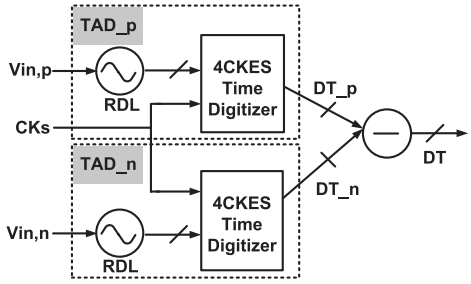


Fig. 12 Block diagram of differential-setupTAD.

methods have to rely on the additional analog components and burn abundant power.

Comparatively, the differential-setup method in [11] adds an identical TAD to quantize the differential inputs, and thus scales well with CMOS scaling. The testbench of differential-setup TAD is easy to build by using two identical TADs and a software subtractor. The block diagram of differential-setup TAD is shown in Fig. 12. The two RDLs are differential in the frequency domain. Ideally, two RDLs operate at nominally equal frequency for zero differential input, and quantize the frequency difference proportional to the differential input. However, free-running frequency offset and tuning gain mismatch between two RDLs typically degrade the performance.

The offset calibration can be conducted in the method as proposed in [19]. During the calibration, the inputs are shorted to the common-mode input voltage. The nonzero output due to offset can be stored in a digital register. Then, this data is subtracted from the output of TAD in normal operation. Tuning gain mismatch is severe neither, since input range of TAD is very narrow.

Figure 13(a) shows the output power-spectral-density (PSD) of single-end TAD at 200 kS/s and 100 kHz BW when V_{in} = 0.5–0.6 V and f_{in} = 9.9 kHz. Figure 13(b) shows the PSD of TAD after the differential-setup processing. The 2nd-order harmonic dominates the in-band distortion in single-end TAD. After the differential setup, the even-order harmonics are significantly suppressed. The 3rd-order harmonic determines SFDR. It is the nonlinear "V-to-T" characteristic of DU that dominates the SFDR and SNDR. Although this work only uses 100 mV input range to minimize this intrinsic linearity, the SFDR in Fig. 13(b) is only 56.11 dB. In order to achieve better linearity, the multi-straight-line approximation [8] or other calibration techniques [22] should be utilized.

In Fig. 14, the static characteristic of TAD at 200 kS/s and in a 0.4–0.6 V input range before and after the differential setup processing is shown. From this figure, it is also obvious that linearity performance is improved.

Table 5 shows the performance summary of TAD after the differential-setup processing and comparison with the state-of-art SAR ADCs and hybrid time-domain ADC. In this table, effective sensitivity of TAD is defined as:

$$\textit{effective sensitivity} = \textit{input range}/2^{ENOB} \tag{8}$$

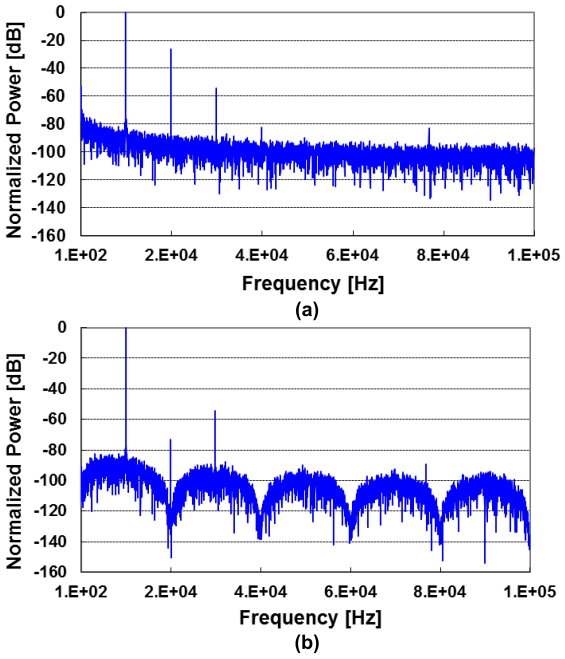


Fig. 13 Output PSD at 200 kS/s, BW = 100 kHz, V_{in} = 0.5–0.6 V, *VDDL* = 0.6 V before/after the differential-setup processing.

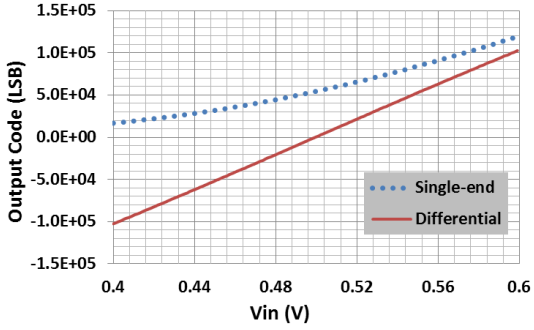


Fig. 14 Static characteristic of TAD at 200 kS/s before/after the differential-setup processing when V_{in} = 0.4–0.6 V.

We compare SAR ADC with TAD because SAR ADC also benefits from the scaling of CMOS technology. In order to make a fair comparison, no digital LPF is used to configure the effective bandwidth of TAD. Therefore, TAD's bandwidth now equals to the folding frequency of the sampling clock. Note that Table 5 only includes the power consumption of differential TADs. If necessary, the software digital subtractor can easily be implemented on chip. It won't contribute an enormous power addition.

Recently, the time-domain processing techniques have drawn a great attention from ADC designers. However, many time-domain ADCs are only hybrid-type ADC [25]–[27]. They quantize input signal in voltage domain and convert the residue voltage to time pulse at the 1st stage. Then, their 2nd-stage TDC conducts time-to-digital conversion. These reported time-domain ADCs relax the requirement of the inter-stage amplifier, but still need a sophisticated pre-conditioning circuit for their 1st-stage ADCs to ensure sampling and reference accuracy. This paper only compares TAD with [25], since Refs. [26] and [27] are not designed for sensor application. Table 5 shows that TAD, as an ADC working exclusively in time domain, has the best effective sensitivity.

Table 5 Performance summary and comparison table after the differential-setup processing.

	This work			[23]	[24]	[25]
Technology	65nm			65nm	90nm	90nm
Architectur	TAD			SAR	SAR	SAR+TDC
Supply (V)	0.6			0.55	1	0.5
V_{in} (V_{pp})	±0.1			±0.55	±1	±0.55
f_s(S/s)	200 k	1 M	10 M	20 k	10.24 M	1 M
BW(Hz)	100 k	500 k	5 M	10 k	5 M	500 k
SNDR(dB)	53.32	47.51	48.40	55	48.4	54.44
Effecive Sensitivity	0.52 mV/LSB	1.03 mV/LSB	0.93 mV/LSB	2.40 mV/LSB	11.44 mV/LSB	2.32 mV/LSB
Power(μW)	126.2	150.8	186.4	0.2	62	1.2
Area(mm^{2})	0.032			0.212	0.054	0.04

Table 5 shows that TAD can achieve a competitive SNDR even in a much narrower input range. It seems that TAD burns much more power than that of SAR ADCs. But, don't forget that TAD doesn't require any complicated pre-conditioning circuits. In terms of total power consumption of sensor interface, TAD is probably more efficient. Due to the same reason, it is probably unfair to use the Figure-of-Merit (FOM) of conventional ADCs to evaluate TAD. The performance of TAD should be assessed on system level.

6. Conclusion

The design paradigm of conventional analog-type sensor interface is facing severe challenges brought by the scaling of CMOS. As a competitive alternative, a time-domain sensor interface namely TAD, is presented in this paper. TAD has all-digital structure, and thereby benefits from CMOS scaling in terms of power, area, speed, and sensitivity. It can directly handle the weak input voltage because of not only the superb voltage resolution but also the intrinsic 1st-order noise shaping.

A 0.016 mm^2 TAD prototype in 4CKES architecture was fabricated in 65 nm CMOS process. It can quantize 0.1 Vpp input range with a reconfigurable resolution 82.7 μV/LSB at 10 MS/s and 1.96 μV/LSB at 200 kS/s, only under 0.6 V supply voltage in 20 kHz bandwidth. Nonlinearity of TAD can be effectively suppressed by the differential-setup processing. The differential-setup TAD achieves a 53.32 dB SNDR at 200 kS/s, in 100 kHz bandwidth. It also achieves competitive SNDR metric with that of conventional ADCs at 1 MS/s and 10 MS/s.

Acknowledgments

The authors would like to thank James Lin for helpful discussion and design support.

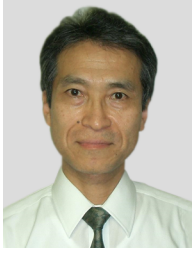
This work was supported by Huawei Technologies Co. Ltd., VLSI Design and Education Center (VDEC) in collaboration with Cadence Design Systems, Inc., and Berkeley

Design Automation for the use of the Analog FastSPICE (AFS).

References

[1] J. Marek, "MEMS for automotive and consumer electronics," IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers, pp.4–12, Feb. 2010.
[2] R.F. Yazicioglu, T. Torfs, J. Penders, I. Romero, H. Kim, P. Merken, B. Gyselinckx, H.J. Yoo, and C. Van Hoof, "Ultra-low-power wearable biopotential sensor nodes," Proc. Int. Conf. IEEE EMBS, pp.3205–3208, Sept. 2009.
[3] G.Y. Jeong and K.H. Yu, "Design of ambulatory ECG monitoring system to detect ST pattern change," Int. Joint Conf. SICE-ICASE, pp.5873–5877, Oct. 2006.
[4] M. Elzakker, E. Tuijl, P. Geraedts, D. Schinkel, E. Klumperink, and B. Nauta, "A 10-bit charge-redistribution ADC consuming 1.9 μW at 1 MS/s," IEEE J. Solid-State Circuits, vol.45, no.5, pp.1007–1015, May 2010.
[5] A. Shikata, R. Sekimoto, T. Kuroda, and H. Ishikuro, "A 0.5 V 1.1 MS/s 6.3 fJ/conversion-step SAR-ADC with tri-level comparator in 40 nm CMOS," Proc. IEEE Symp. VLSI Circutis, pp.262–263, June 2011.
[6] T. Watanabe, T. Mizuno, and Y. Makino, "An all-digital analog-to-digital converter with 12-μV/LSB using moving-average filtering," IEEE J. Solid-State Circuits, vol.38, no.1, pp.120–125, Jan. 2003.
[7] T. Watanabe and T. Terasawa, "A 0.0027 mm^2 9.5 bit 50 MS/s all-digital A/D converter TAD in 65 nm digital CMOS," Proc. 16th IEEE ICECS, pp.271–274, 2009.
[8] T. Watanabe and T. Terasawa, "An all-digital A/D converter TAD with 4-shift-clock construction for sensor interface in 0.65 μm CMOS," Proc. 36th IEEE European Solid-State Circuits Conf, pp.178–181, 2010.
[9] T. Watanabe and S. Yamaguchi, "An all-digital PLL for frequency Multiplication by 4-1022 with seven-cycle lock time," IEEE J. Solid-State Circuits, vol.38, no.2, pp.198–204, Feb. 2003.
[10] S. Masuda, T. Watanabe, S. Yamauchi, and T. Terasawa, "All-digital quadrature detection with TAD for radio-controlled clocks/watches," IEEE Trans. Circuits Syst. I, vol.56, no.2, pp.285–293, Feb. 2009.
[11] F. Opteynde, "A maximally-digital radio receiver front-end," IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers, pp.450–451, Feb. 2010.
[12] S. Tajima, Y. Okuda, T. Watanabe, H. Aoyama, M. Yamamot, and T. Uchiyama, "High resolution magneto-impedance sensor with TAD for low noise signal processing," IEEE Int. Magnetics Conf., pp.1173–1174, 2014.
[13] T. Terasawa and T. Watanabe, "Electrostatically levitated ring-shaped rotational-gyro/accelerometer using all-digital OFDM detection with TAD," Proc. IEEE SENSORS, pp.530–533, 2012.
[14] T. Watanabe and H. Isomura, "All-digital ADC/TDC using TAD architecture for highly-durable time-measurement ASIC," IEEE Int. Symp. Circuits and Systmes, pp.674–677, 2014.
[15] J. Kim, T.K. Jang, Y.G. Yoon, and S.H. Cho, "Analysis and design of voltage-controlled oscillator based analog-to-digital converter," IEEE Trans. Circuits Syst. I, vol.57, no.1, pp.18–30, Jan. 2010.
[16] G. Li, Y. Tousi, A. Hassibi, and E. Afshari, "Delay-line-based analog-to-digital converters," IEEE Trans. Circuits Syst. II, vol.56, no.6, pp.464–468, June 2009.
[17] A. Abidi, "Phase noise and jitter in CMOS ring oscillators," IEEE J. Solid-State Circuits, vol.41, no.8, pp.1803–1816, Aug. 2006.
[18] A. Homayoun and B. Razavi, "Relation between delay line phase noise and ring oscillator phase noise," IEEE J. Solid-State Circuits, vol.49, no.2, pp.384–391, Feb. 2014.
[19] A.K. Gupta, K. Nagaraj, and T.R. Viswanathan, "A Two-Stage ADC Architecture With VCO-Based Second Stage," IEEE Trans. Circuits Syst. II, vol.58, no.11, pp.734–738, Nov. 2011.
[20] H. Farkhani, M.M. Nejad, and M. Sachdev, "A fully digital ADC using a new delay element with enhanced linearity," IEEE Int. Symp. Circuits and Systmes, pp.2406–2409, 2008.
[21] H.C. Hor and L. Siek, "K-locked-loop and its application in Time Mode ADC," Proc. 12th ISIC, pp.101–104, 2009.
[22] S. Rao, K. Reddy, B. Young, and P.K. Hanumolu, "A 4.1 mW 12-bit ENOB, 5 MHz BW, VCO-based ADC with on-chip deterministic digital background calibration in 90 nm CMOS," Proc. IEEE Symp. VLSI Circutis, pp.C68–C69, June 2013.
[23] M. Yip and A.P. Chandrakasan, "A resolution-reconfigurable 5-to-10b 0.4 V-to-1 V power scalable SAR ADC for sensor applications," IEEE J. Solid-State Circuits, vol.48, no.6, pp.1453–1464, June 2013.
[24] P. Harpe, "A 30 fJ/conversion-step 8b 0-to-10MS/s asynchronous SAR ADC in 90 nm CMOS," IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers, pp.531–533, Feb. 2010.
[25] Y.J. Chen and C.C. Hsieh, "A 0.4 V 2.02 fJ/conversion-step 10-bit hybrid SAR ADC with time-domain quantizer in 90 nm CMOS," Proc. IEEE Symp. VLSI Circutis, pp.35–36, 2014.
[26] T. Oh, H. Venkatram, and U.K. Moon, "A time-based pipelined ADC using both voltage and time domain information," IEEE J. Solid-State Circuits, vol.49, no.4, pp.961–971, April 2014.
[27] M. Miyahara, I. Mano, M. Nakayama, K. Okada, and A. Matsuzawa, "A 2.2 GS/s 7b 27.4 mW time-based folding-flash ADC with resistively averaged voltage-to-time amplifiers," IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers, pp.542–544, 2014.

Yu Hou received the B.E. degree in electrical and information engineering from Dalian University of Technology, Dalian, China, in 2009, and M.E. degree in physical electronics from Tokyo Institute of Technol-ogy, Tokyo, Japan, in 2013. He is currently pursuing the PH.D. degree at Tokyo Institute of Technology. His research interest is mixed -signal circuits, especially data converters.



Takamoto Watanabe received the B.E. degree in electronic engineering from Mie University, Mie, Japan in 1979. He received the Ph.D. degree in electrical and computer engineering from Nagoya Institute of Techn-ology in 2003. He was formerly with Panas-onic Corporation, Osaka, Japan, developing digital ICs. In 1987, He joined DENSO CO-RPORATION, Aichi Japan. At Soken, Inc., he engaged in research on semiconductor sensor circuits. In 1989, he joined DENSO Research Laboratories, where he did research on semiconductor sensor circuits, ICs for automobiles, and ASIC functional circuits. In 2000, he was assigned to the Corporate R&D of DENSO, where he has been working on the research and development of digital-sensing circuits and devices, A/D converters, digital PLLs, RF circuits and their application devices. Dr. Watanabe is a member of The Institute of Elec-tronics, Information and Communication Engineers (IEICE) and the Society of Automotive Engineers (SAE) of Japan.

Masaya Miyahara received B.E. degree in mechanical & electrical engineering from Kisarazu National College of Technology, Kisarazu, Japan, in 2004, and M.E. and Ph.D. degree in physical electronics from Tokyo Institute of Technology, Tokyo, Japan, in 2006 and 2009 respectively. Since 2009, he is an assistant professor at Department of Physical Electronics, Tokyo Institute of Tec-hnology, Tokyo, Japan. His research interests are RF CMOS and mixed-signal circuits.

Akira Matsuzawa received B.S., M.S., and Ph.D. degrees in electronics engineering from Tohoku University, Sendai, Japan, in 1976, 1978, and 1997 respectively. In 1978, he joined Matsushita Electric Industrial Co. Ltd. Since then, he has been working on research and development of analog and mixed-signal LSI technologies, ultra-high speed ADCs, intelligent CMOS sensors, RF CMOS circuits, and digital read-channel technologies for DVD systems. From 1997 to 2003, he was a general manager in advanced LSI technology development center. On April 2003, he joined Tokyo Institute of Technology and he is a professor on physical electronics. Currently, his research interests are CMOS wireless transceiver, RF CMOS circuit design for SDR and high-speed data converters. He served the guest editor in chief for special issue on analog LSI technology of IEICE transactions on electronics in 1992, 1997, and 2003, committee member for analog technology in ISSCC, IEEE SSCS elected Adcom from 2005 to 2008, and IEEE SSCS Distinguished lecturer. He received the IR100 award in 1983, the R&D100 award and the remarkable invention award in 1994, and the ISSCC evening panel award in 2003 and 2005. He is an IEEE Fellow since 2002 and an IEICE Fellow since 2010.