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Doctoral Thesis

A study on AlGaN/GaN HEMT gate stacks for

threshold voltage control and leakage current suppression

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Abstract

AlGaN/GaN high-electron-mobility-transistor (HEMT) has been receiving much attention for high efficient power converter devices owing to its high electron mobility of over 1000 cm^2/Vs and high breakdown field. Recent epitaxial growth of nitride based layers has enabled AlGaN/GaN growth on Si substrates with appropriate stress relaxation buffer layers, which enables mass production on a large size wafer over 12 inches, so that high performance devices can be realized at relatively low cost. However, there are still some issues to overcome both in substrate quality and device process and reliability. One of the issues is that the devices operate with normally on characteristics, which is due to the piezoelectric and spontaneous polarization of the AlGaN/GaN devices, and should be avoided in terms of fail-safe operation. On the other hand, large gate leakage current due to Schottky gate configuration limits the overdrive voltage of the devices, limiting the on-current. The thesis experimentally demonstrates the advantages of poly-Si gate electrodes and La_2O_3 gate dielectrics for shifting the threshold voltage to positive direction and for suppressing the gate leakage current.

B doped poly-Si was obtained with BF_2 ion implantation into an intrinsic poly-Si layer for gate electrode material. As there were less reaction between poly-Si and the AlGaN surface, the devices revealed high process temperature endurance with suppressed gate leakage current. By tuning the BF_2 ion implantation conditions, the threshold voltage was found to be controlled depending on the distribution of F atoms in AlGaN layer. Excess F ions near the AlGaN/GaN interface showed degraded mobility due to enhanced diffusion of F atoms at the interface, which suggests the distribution of F atom profile in the AlGaN layer should be tailored. The poly-Si gated AlGaN/GaN HEMTs revealed high reliability against stress voltage application test over conventional Schottky gate ones.

For La_2O_3 gate dielectrics, the threshold voltage was found to shift to positive direction with higher temperature annealing. The phenomena were attributed the presence of negative fixed charges at the interface layer, reactively created between the La_2O_3 and AlGaN layers during the thermal processes. Moreover, an increase in capacitance with annealing was observed owing to the crystallization of the La_2O_3 film, which exhibit a dielectric constant of 27 when annealed over 500 ^oC. With this high k-value and the negative charges, La_2O_3 gate dielectrics have attractive physical properties to relax the trade-off performance between capacitance density and threshold voltage for AlGaN/GaN HEMT.

Finally, we investigate the prospects of poly-Si gate with La_2O_3 gate dielectrics base on the obtained experimental results. Device structures including thickness and annealing conditions for normally-off operation based on F ion distributions in the AlGaN layer with negative charges at the interface of lanthanum oxide and AlGaN layer are proposed.

Contents

Chapter 1: Introduction

Power devices based on wide bandpgap semiconductors such as SiC and GaN are promising as candidates for small size and low loss electronic converters with high power conversion efficiency. In particular, AlGaN/GaN high-electron-mobility-transistor (HEMT) devices are being in the development of high power and high-frequency applications due to high electron carrier concentration at the hetero-interface. However, there are still some issues that need to be addressed before the technology will replace existing Si technologies. In this chapter, the introduction of power devices and its trend to high conversion efficiency has been described and the status of GaN based device developments is reviewed. Moreover, the advantages of AlGaN/GaN HEMT, both electrical as well as process point of views are summarized. Also, the current issues for the devices are stated. Based on the backgrounds, the purpose and the structure of the thesis are stated.

1.1 Power devices for high power conversion efficiency

At present, lots of attention is paid toward renewable energy and maximize the usage of the energy efficiency for the next few decades because of the world's urgent requirements in the energy saving and the environment protection. Energy consumption can be categorized in mainly four aspects; residential, commercial, transportation, and industrial in today's modern society. All the activities consume various kinds of energy in our daily life like as heat generation, light and so on. In terms of primary energy consumption, about 40% of primary energy is used for electricity generation. Therefore,

energy saving is increasingly dependent upon the efficient and reliable electrical power management for generation, storage, transportation and conversion.

Power electronic converters are used to convert and control electrical energy in power systems, which plays an important role in the development of modern industry. Figure 1.1 shows the power consumption of FY2005 in Japan. About 29% of the electric power is consumed as home power supply, and 57% of the electrical power are consumed as motor drive system, most of which are used in fan and pumping. If the variable frequency drivers operated by high efficient power converters are implemented, 20%~30% of the energy consumption can be saved.

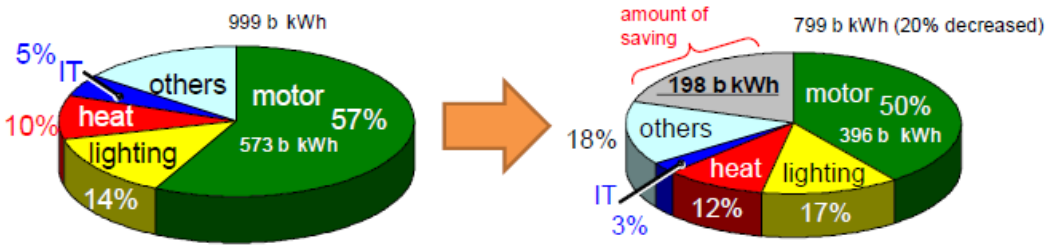


Figure 1.1 Power consumption in Japan can be reduced with high efficient converters.

Power electronic technology is widely used in electric power conversion. In most automation and process control systems, required to convert electrical energy from one form into another by power conversion, such as voltage, current, frequency and phase. These power conversions are called converters or inverters.

Inverters are able to control various types of electric motors by converting the frequency of the AC power supply. The power consumption such as home appliances vary by time to time, inverters should be controlled depending on the required power to be supplied. An essential feature of an ideal power conversion is that it should not produce

any energy loss. Therefore, more high efficiency energy conversion is expected in most electrical power systems.

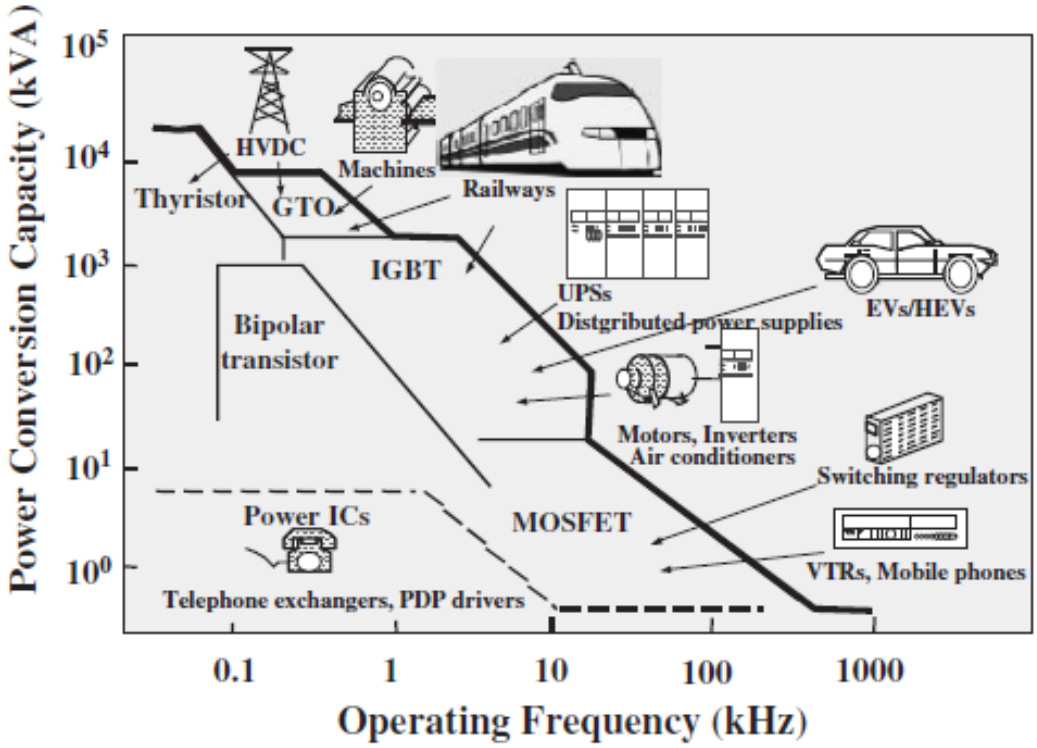


Figure 1.2 Various application areas of power electronics, where high-efficiency switching devices are used [1.1]

Figure 1.2 shows various application areas of power electronics, where high-efficiency switching devices are used in power systems and power conversion [1.1]. Power electronics are being used over a wide power range, with ratings from milliwatts up to gigawatts. As shown in the above figure, depending on the required power capacity and operating frequency, different types of power semiconductor devices are being used for different power electronics application field. At the low power fields (less than 1kW), MOSFET power devices are commonly used to convert electrical energy as a switching

power supply element for portable communication devices, electronic systems (audio, video, and controllers) and personal computer systems. The trend of this application field is toward higher switching frequencies and lower operating voltage. Low cost and can be mass produced are the main factors for the development and commercialization of technological innovation. In the 1kW-1MW power field, IGBTs-based power converters are being used for household appliances, electric vehicles (EVs)/hybrid electric vehicles (HEVs), motors and power supply transforms. Most power converters in the high power field (greater than 1MW power range) are used (GTO) turn-off thyristor type devices to convert electrical energy such as HVDC transmission systems, machines and railways [1.1].

The requirements for these power electronics are low power loss under high-switching-frequency operation. Therefore, the requirements for power switching devices are lower resistance in the on state (conducting) and higher blocking voltage in the off state (forward or reverse blocking). Passive component such as transformers, inductors and capacitors, which temporarily store energy within the converters system [1.2]. Higher frequency operation enables smaller passive component.

1.2 Status of GaN based device development

Semiconductor material properties strongly affect the device performances. Table 1.1 shows a summary of some physical properties of semiconductor substrates. High electron mobility and high electron velocity are desired for higher frequency operation. The high breakdown field is suitable for devices operate at higher voltage with low leakage current as they improve the power efficiency of devices in the power supply system. Most of the

power loss is wasted as heat generation. To retain the efficiency for the converters, heat dissipation systems have to be implemented to the devices with high thermal conductivity [1.3]. In addition, wide bandgap materials with high thermal conductivity are important parameters for improved device's cooling ability and small size.

Table 1.1 Semiconductor material property and features [1.4]

Material property	Device property	Improved performance	System advantages
High breakdown field	High voltage	Power density, gain, efficiency and output impedance	Larger bandwidth, smaller number of dies and less energy usage
	High doping		
High thermal conductivity	High temperature	Small die size and more output power/die	Easier system cooling
Wideband gap			
High electron velocity	High frequency	High f_t	High system frequency
		High f_{max}	

Si device is the main semiconductor material of high power switching devices for a long time such as the metal-oxide-semiconductor field effect transistor (MOSFET), gate turn-off thyristor (GTO) and insulated gate bipolar transistor (IGBT). However, the physical properties silicon material limit the device operations. In recent years, the development of wide bandgap semiconductor device has increased in small size and high efficiency power device, owing to their superior material properties.

Table 1.2 Physical properties of various semiconductor materials [1.5-1.8]

	Si	SiC(4H)	GaN
Band gap (eV)	1.12	3.2	3.4
Electron Mobility (cm^2/Vs)	1500	900	2100
Saturated Velocity (cm/s)	1×10^7	2.2×10^7	2.7×10^7
Breakdown Field (V/cm)	3×10^5	2.5×10^6	3×10^6
Thermal Conductivity (W/cmK)	1.5	4.9	2.3

GaN and SiC wide band gap semiconductors are attractive for next generation power electronics. Compared to Si, GaN and SiC have advantages in breakdown field and thermal conductivity, especially GaN has high electron mobility, which are expected to replace Si technology in high power and high frequency applications. SiC is a compound semiconductors by combining silicon and carbon. It has a high bonding energy, which is a stable crystalline structure compared to silicon. In addition, SiC has a high breakdown filed, which about 10 times than that of silicon. Therefore, SiC devices are widely used for high power applications than 1200 volts. On the other hand, although breakdown voltage of GaN devices lower than that of SiC devices, GaN devices are suited for high frequency applications. Recently, a technology of hetero-epitaxial growth of GaN on silicon (111) substrate has been accomplished, so that the wafer diameters up to 8 or 12 inches can be utilized, which helps to reduce the production cost. GaN devices will dominate in the 600 volt- 1200 volt range application with high power conversion high frequency applications, such as in switching power supply.

As given in Table 1.2, the material properties of SiC and GaN have desirable device features for high power application. Specifically, GaN has high electron mobility 2100 cm^2/Vs and high saturation electron velocity about $2.7\times10^7 cm/s$, which contributes to higher current density for high frequency switching devices. GaN exhibits about 10 times higher breakdown field than silicon, which leads to low on resistance. Moreover, GaN has a wide bandgap of 3.4eV and high thermal conductivity, high thermal conductivity material can greatly help to dissipate heat during high power operation, increase the power output.

As a result, these material properties are suitable for power electronics applications [1.9]. GaN device can be operated at high speed switching with low lost, small size and high efficiency compared to silicon device.

1.3 Advantages of AlGaN/GaN HEMT

The main advantage of GaN over SiC channel is the ability to form heterostructures with other group III-V compounds. The most prevalent HEMT structure is the AlGaN/GaN HEMT. AlGaN/GaN HEMT structures have lots of advantages over other wide bandgap semiconductors, owing to high mobility over 1000 cm^2/Vs. This high mobility can be achieved by using two dimensional electron gas (2DEG) by strains at AlGaN and GaN interface. In addition, AlGaN and GaN both have high breakdown voltage about 10 times higher than that of silicon, so that AlGaN/GaN HEMT is emerging as a promising candidate for future high power and high frequency applications.

In this thesis, HEMTs were fabricated on wafers with an undoped $Al_{0.25}Ga_{0.75}N$ layer on GaN layers epitaxially grown on Si (111) wafers.

1.4 Challenges of AlGaN/GaN HEMT

AlGaN/GaN HEMT structures have been strong candidates for high power appliances with low power consumption [1.10-1.11]. High-density-2DEG are accumulated at the interface between AlGaN layer and GaN layer by spontaneous and piezoelectric polarization effects, which makes it possible to realize a low on-state resistance and faster switching speed for the transistor characteristics [1.12]. However, there are still some issues that need to be addressed before this technology will replace existing Si technologies. There are some limitations associated with AlGaN/GaN structures as shown in Figure1.3.

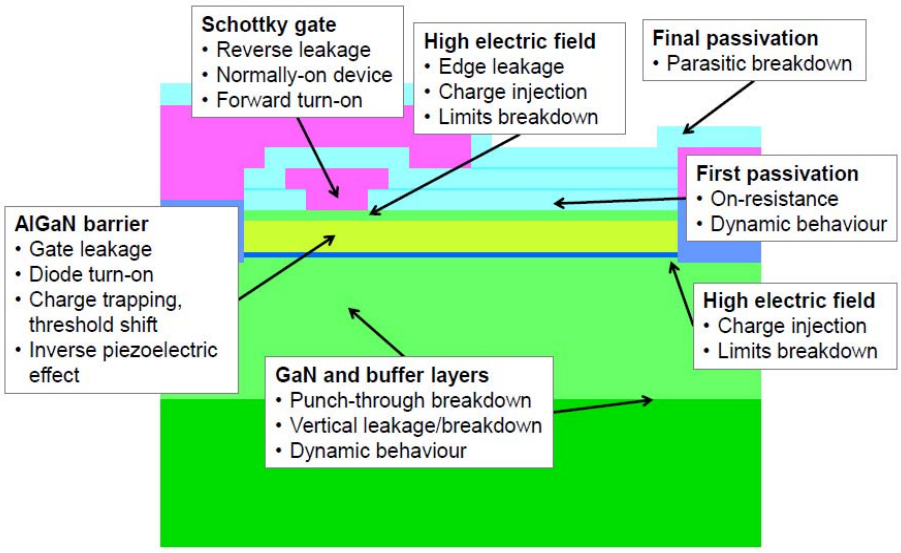


Figure 1.3 Issues of AlGaN/GaN HEMT [1.13]

In power electronics applications, AlGaN/GaN HEMT is considered as an electronic

component, which usually requires normally-off characteristics for a switch-mode power device. However, AlGaN/GaN HEMTs usually exhibit normally-on operation with a negative threshold voltage typically around -4 V, resulting in increased circuit complexity and standby power consumption [1.14]. Normally-off AlGaN/GaN HEMT in which no current flows at no gate bias is strongly required for fail-safe operation [1.15]. The threshold voltage can be modified through the device fabrication, which depend on the Schottky barrier height, carrier concentration and the thickness of AlGaN layer.

Gate recess technique is a common fabrication technique to obtain normally-off characteristics. This technique is used to reduce the AlGaN barrier layer thickness under the gate region by using etching methods. The reduction in the AlGaN thickness by gate recess process can decrease the 2DEG density, so that with a deep enough gate-recess etching, the threshold voltage can be shifted to a positive value and normally-off characteristics can be obtained. The schematic diagram as shown in Figure 1.4.

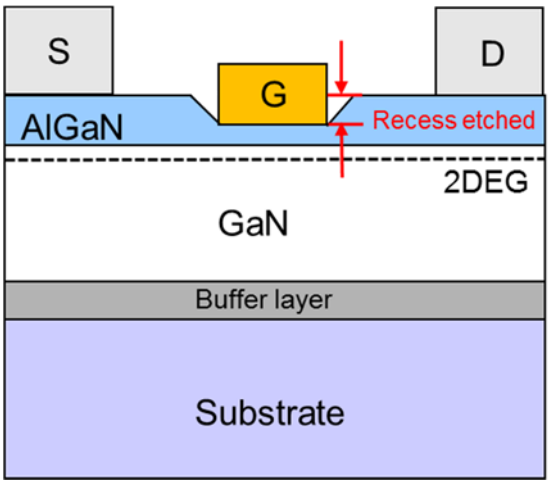
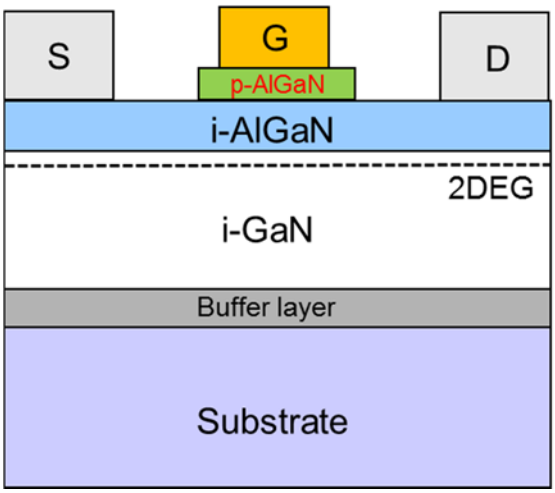
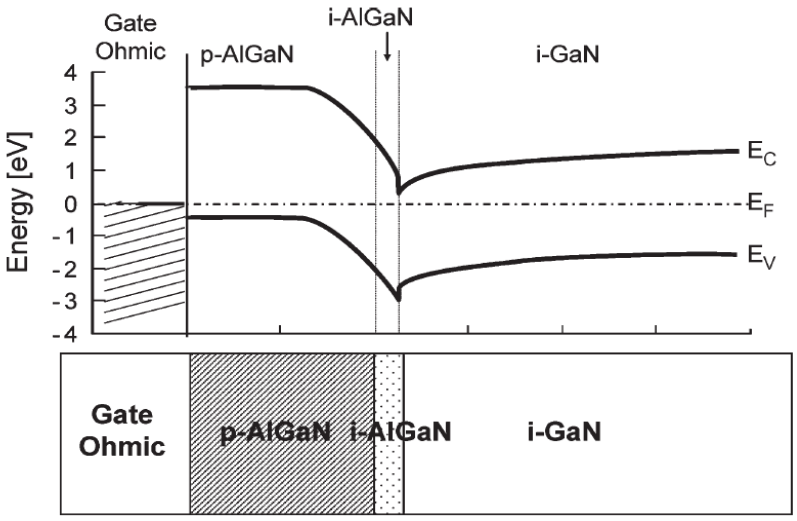


Figure 1.4 Recess-gate structure of AlGaN/GaN HEMT

Wet etching has some advantages of low cost and low damage to the wafer. However, wet etching techniques for AlGaN/GaN HEMT structure are still lacking. Therefore, dry etching has been used for the recess gate process in the fabrication process of AlGaN/GaN HEMTs [1.16-1.22]. However, dry etching will introduce damages and associated defects to the AlGaN layer, which will affect the device performance. In addition, the uniformity in the recess etching depth and consequently the uniformity in the threshold voltage, which will result in large leakage current. Therefore, insertion of the gate insulator to recover the leakage current for recess gate structure is necessary.



(a) p-type AlGaN layer on the AlGaN/GaN structure



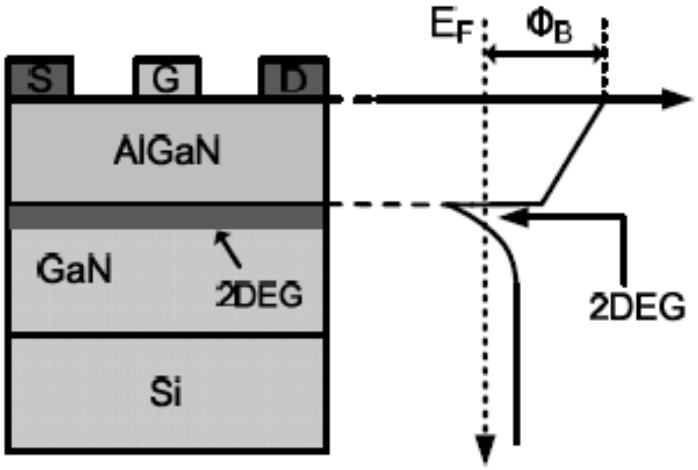
(b) Band diagram of the GIT under a gate bias of 0V [1.24]

Figure 1.5 P-type cap structure and band diagram

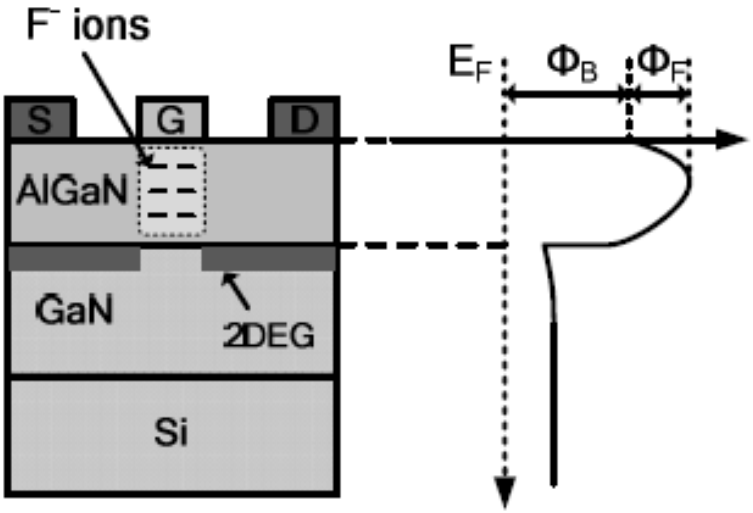
Another method to modify the threshold voltage of AlGaN/GaN HEMT technique is using p-type GaN layer capping on the AlGaN/GaN structure to lift up the potential of the channel [1.23-1.24]. The structure and band diagram are shown in Figure 1.5(a) and (b). The structure is called gate injection transistor (GIT). The structure utilizes hole injection from p-type gate to the interface of AlGaN/GaN compensate 2DEG electrons and thereby obtain normally-off characteristics. However, this structure increases the forward gate voltage [1.25-1.26].

Fluoride implantation treatment is a method to obtain positive threshold voltage through modifies the energy bandgap [1.27-1.31]. The potential in the AlGaN barrier can

be effectively raised due to the fluorine ions have a strong electronegativity and which are negative charge [1.27-21.28]. The band diagrams are shown in Figure 1.6.



(a) Conventional AlGaN/GaN HEMT



(b) E-mode HEMT with CF_4 plasma treatment

Figure 1.6 Conduction band schematic diagrams [1.31]

The fluorine ions are incorporated into the AlGaN barrier by CF_4 plasma treatment, these negatively charged fluorine ions will cause an upward bending of the conduction band in the AlGaN layer [1.29-1.30]. Unfortunately, some fluorine ions as impurities into the channel result in mobility degradation.

Another issue for AlGaN/GaN is gate leakage current, which increases losses in the devices and limits the performance of the devices. Defect states play an integral role in gate leakage through a trap-based tunneling mechanism [1.32], the current leakage through the buffer layer above the substrate deteriorates the pinch-off characteristics [1.1]. As a solution for gate leakage, an insulating layer with wide bandgap and high dielectric constant is promising for the AlGaN/GaN structure. Prevalent gate dielectrics have been investigated, such as SiO_2 [1.33-1.36], SiN [1.37-1.38], HfO_2 [1.39-1.40] and Al_2O_3 [1.41-1.43]. The results show that an insulated gate structure is extremely effective for leakage current suppression. High dielectric constant materials show a low interface state density as an insulating layer for AlGaN/GaN MISHFET. Also, it is reported that reliability can be improved with the use of gate dielectrics owing to the suppression of nitrogen vacancies. On the contrary, the introduction of an insulating layer results in the shift in the threshold voltage and increase in interface trap density, which impact the stability of voltage that turn on AlGaN/GaN HEMT. Therefore, further examination such as materials and the fabrication process selection is necessary to relax the trade-off performance for AlGaN/GaN HEMT.

1.5 Purpose and structure of this thesis

The purpose of this study is to implement new materials which can shift the threshold voltage and reduce the gate leakage current. For this purpose, poly-Si is selected as gate electrode materials, which has endurance against high process temperature. The material also has high compatibility with CMOS process. Moreover, La_2O_3 is selected as a new gate dielectric material for AlGaN/GaN HEMTs, as it possesses a high dielectric constant. The interface reaction upon annealing temperature is characterized.

In the next chapter, the fundamental physics that lie in the AlGaN/GaN HEMT are summarized. The basic structure of the devices, the effect of polarization by heteroepitaxial growth and the formation of two dimensional gas (2DEG) are explained.

In chapter 3, the AlGaN/GaN substrates used in this study are described. Also, detailed processes for HEMT fabrication including cleaning, isolation, metallization and gate dielectric formations are summarized. Also, the characterization methods of the fabricated HEMT devices are stated.

In chapter 4, boron doped poly-Si gate electrodes are introduced for AlGaN/GaN HEMT and its process compatibility is discussed. The BF2+ ion implantation energy dependent threshold voltage tuning was confirmed, suggesting the feasibility to achieve normally-off HEMT devices. A large suppression in the gate leakage current as well as high reliability against stress test was performed. The issues related to the doping including mobility degradation accompanied by enhanced diffusion of F ions, the sheet resistivity of poly-Si gate electrodes are discussed.

In chapter 5, introduction of lanthanum oxide gate dielectrics and its device performances are described. The threshold voltage was reported to shift to positive direction with thermal treatment, due to interface reaction between the lanthanum oxide and the AlGaN layer. The interface was found to contain negative fixed charges and the density increases with temperature. The gate leakage current was reported to be suppressed by orders of magnitudes at both off and of states, indicating larger overdrive can be applied.

In chapter 6, the prospects for normally-off AlGaN/GaN HEMT devices with reduced gate leakage currents are described. Device structures, including thickness and annealing conditions for normally-off operation based on F ion distributions in the AlGaN layer with negative charges at the interface of lanthanum oxide and AlGaN layer are proposed.

Finally, chapter 7 concludes the thesis and future remarks are stated.

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Chapter 2: Fundamentals of AlGaN/GaN HEMT

In this chapter, the fundamental physics that lie in the AlGaN/GaN HEMT are summarized. The basic structure of the devices, the effect of polarization by heteroepitaxial growth and the formation of two dimensional gas (2DEG) are explained.

2.1 Properties of AlGaN/GaN HEMT

2.1.1 HEMT

HEMT exhibits high carrier mobility on a hetero structure with different band gap materials as like AlGaAs/GaAs structure and AlGaN/GaN structure.

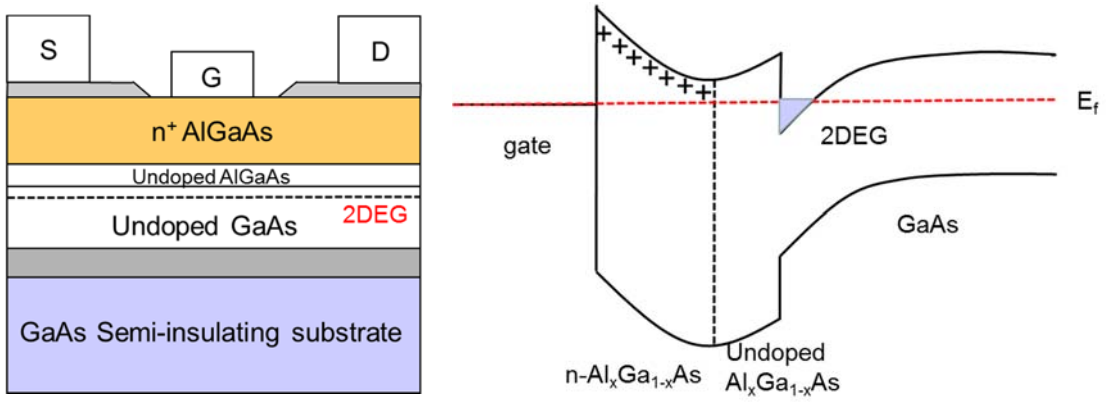

Figure 2.1 (a) An example of a nAlGaAs/GaAs HEMT structure and (b) its energy band profile

The first HEMT that a kind of field effect transistor using the heterojunction of a highly doped n-type AlGaAs thin layer and the undoped GaAs layer was invented by Takashi Mimura in 1979 [2.1, 2.2]. The formation of a quasi-triangular potential well at the hetero-interface between AlGaAs and GaAs due to two different band gap materials. The electrons supplied by donors in the n-type AlGaAs can from the higher band gap of AlGaAs layer move into the GaAs potential well, formed two dimensional electron gas (2DEG) [2.3]. The schematic structure of AlGaAs/GaAs HEMT and the band diagram as shown in Figure 2.1 (a) and (b). A thin intrinsic AlGaAs layer known as spacer layer is introduced between n-type AlGaAs layer and undoped GaAs layer, it makes electrons are spatially separated from ionized donors, the ionized impurity scattering is considerably reduced and leads to an increase in the mobility [2.4]. The HEMT is originally used for high speed and low noise applications because of high mobility and less electron collisions.

2.1.2 AlGaN/GaN structure

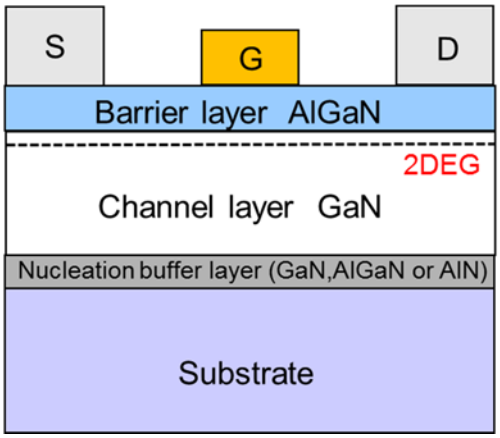

Figure 2.2 Basic structure of an AlGaN/GaN HEMT structure

AlGaN/GaN HEMT is a heterostructure field effect transistor for high voltage and high frequency operation since the first report in 1991 [2.5, 2.6]. The schematic cross-section of a general AlGaN/GaN HEMT structure is shown in Figure 2.2. Two different bandgap materials AlGaN/GaN layer is grown on substrate through buffer layer. While an AlGaN layer grown on a GaN layer polarization effect occurs due to internal spontaneous polarization and external piezoelectric polarization. Polarization field induced positive charge is present at the bottom of AlGaN layer, these positive charges can cause an accumulation of 2DEG electrons at the interface of AlGaN/GaN heterostructure. High 2DEG density up to 10^{13} cm^{-2} can be obtained in the AlGaN/GaN heterostructure without any doping [2.7-2.11], which is more than five times larger as compared to AlGaAs/GaAs structure. Therefore, high mobility about two thousand was realized in AlGaN/GaN HEMT, which a strong advantage for high frequency operation.

AlGaN has a higher bandgap than that of GaN, a potential well formation at the heterostructure of AlGaN/GaN and electrons will accumulate underneath the hetero interface to form a sharper quantum well due to polarization effect, as shown in Figure 2.3. AlGaN layer is used as a barrier layer for AlGaN/GaN HEMT. This barrier layer is mostly intrinsic layer, which means impurity scattering is non-existent, results in high mobility. The AlGaN layer thickness or Al content of AlGaN may affect 2DEG density at the interface. That will discuss in detail in a subsequent section.

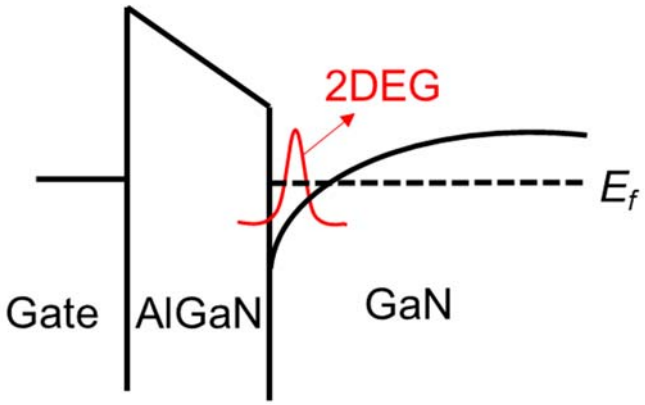

Figure 2.3. Band gap profile of AlGaN/GaN HEMT

GaN growth techniques need to fulfill the requirements of low defect density and smooth morphology, which will affect device performance [2.12]. Defects are responsible for the mobility reduction due to defect scattering. Moreover, high defect density will affect piezoelectric polarization effects and then decrease 2DEG carrier concentration. Dislocations is the path for leakage current [2.13] and impact on performance reliability in the AlGaN/GaN HEMT devices [2.14]. Therefore, reduce defect density in growing GaN films is a non-negligible factor. The crystallinity and properties of GaN strongly depend on the growth techniques. Recently, GaN growth techniques have been developed, including MOVPE (metal organic vapor phase epitaxy), MBE (molecular beam epitaxy) and HVPE (hydride vapor phase epitaxy).

Growth of high quality and freestanding GaN substrate technology is a challenge due to high melt temperature and immature growth technique. GaN epitaxially grown on foreign substrates need consider lattice mismatch and thermal mismatch between GaN and substrate materials. Different lattice constant will induce tensile strain or compressive

strain when a film is grown on foreign substrate. Thermal mismatch is usually expressed by thermal expansion coefficient and it describes the size change of films with a change in temperature after growth. Difference in CTE (coefficient of thermal expansion) between film and substrate also can cause strain. Strain in the film not only influence the surface morphology, band gap energy and phonon frequency, but also induce defects such as dislocation [2.15]. There is a high defect density in the range of 10^{7}-10^{10} cm^{-2} for GaN based device and then influence the device on the optical and electrical properties. In general, there are three main types of substrate used for the growth AlGaN/GaN HEMT structure such as silicon carbide [2.16, 2.17], sapphire [2.18, 2.19, 2.20] and silicon [2.21]. The lattice constant of SiC is very close to that of GaN, which is about 3%. In addition, SiC substrate has a high thermal conductivity about 5 W/cm-K and that is highly beneficial for heat dissipation in the device. However, SiC substrate is very expensive and has large crystallographic defect density. Although sapphire substrate exhibits a large lattice mismatch of 15% with GaN and a small thermal conductivity 0.42 W/cm-K at 300K. It is still the most commonly used substrate for GaN growth because of low cost and high quality. Si is a potential substrate due to excellent availability of large diameters at low lost and acceptable thermal conductivity [2.22]. However, large lattice mismatch and large CTE between GaN and Si leads to the formation of cracks in the films. To compensate large mismatch between GaN and the substrate, nucleation buffer layers are introduced between channel layer GaN and substrate [2.23]. This intermediate layer AIN (on SiC and sapphire), AlGaN (on SiC and sapphire) and GaN (on sapphire) layer have been suggested.

2.2 Polarization effects

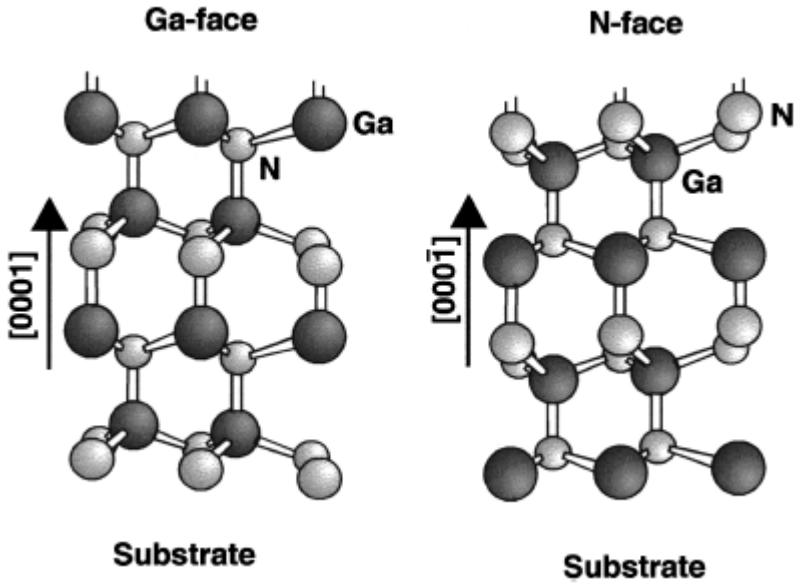

Figure 2.4 GaN crystal structure of wurtzite Ga-face and N-face [2.24]

GaN is a III-V compound material with wurtzite crystal structure. GaN is composed of Ga atoms with a large ionic radius and N atoms with a small ionic radius with mixed covalent ionic bonds. There are two distinct faces, Ga-face and N-face, which are respectively corresponding to the (0001) and (000$\bar{1}$) crystalline faces. Crystal structure of wurtzite Ga-face and N-face GaN as shows as Figure 2.4 [2.24].

Unlike AlGaAs/GaAs HEMT, AlGaN/GaN HEMT does not require doped top layer due to AlGaN and GaN are polar materials. 2DEG are induced in the AlGaN/GaN HEMT by nature polarization effect including spontaneous polarization and piezoelectric polarization. Due to an intrinsic asymmetry of the bonding in the equilibrium wurtzite crystal structure, it exhibits a spontaneous polarization field along the hexagonal c-axis

in the wurtzite lattice. The spontaneous polarization can cause electric filed up to 3MV/cm in the AlGaN and GaN crystals. The spontaneous polarization is directed from the nitrogen atomic layer to the gallium atomic layer [2.25]. Piezoelectric polarization by strain induced due to the lattice mismatch between different composition materials. Piezoelectric polarization in the direction of the *c*-axis can be given by

$$P_{PE} = 2\frac{a - a_0}{a_0}(e_{31} - e_{33}\frac{C_{13}}{C_{33}}), \qquad \text{Eq. (2.2.1)}$$

a and a_0 is the lattice constant of different materials at equilibrium. Furthermore, e_{31}, e_{33} are the piezoelectric coefficients and C_{13}, C_{33} are the elastic constants of the material [2.26]. The piezoelectric polarization can cause an additional electric fields about 2MV/cm in the AlGaN/GaN HEMT. Therefore, strong electric fields about 5MV/cm caused by polarization effect in the AlGaN/GaN crystals structure, which produce high sheet charge density about $6\times10^{12} \sim 2\times10^{13}\text{cm}^{-2}$ at the interface between AlGaN layer and GaN layer [2.24] .

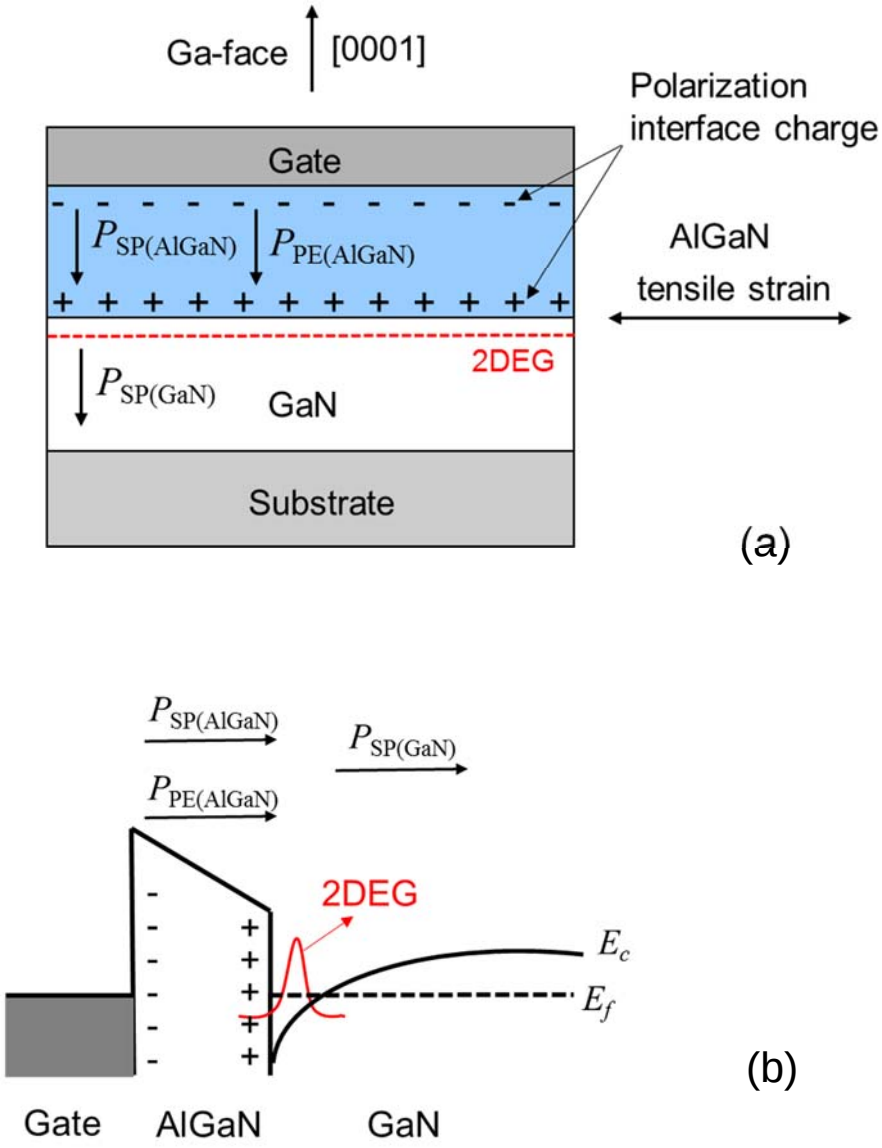

Figure 2.5 (a) Polarization induced charge and direction of the spontaneous and piezoelectric polarization in Ga-face and strain between AlGaN and GaN (b) band diagram of AlGaN/GaN heterostructure and formation of 2DEG at the interface between AlGaN and GaN

When AlGaN is grown on top of GaN heterostructure and the AlGaN layer under tensile strain, piezoelectric polarization will increase and the spontaneous and piezoelectric polarization have the same direction. The polarization induced sheet charge is positive, which is present at the bottom of AlGaN layer. Polarization sheet charge density can be defined by

$$\begin{aligned}\sigma &= P(top) - P(bottom) \\ &= P_{SP}(top) + P_{PE}(top)\} - \{P_{SP}(bottom) + P_{PE}(bottom)\}\end{aligned} \quad , \qquad \text{Eq. (2.2.2)}$$

Positive charges will be largely compensated by electrons, these electrons will form a high concentration of 2DEG at the interface of AlGaN/GaN heterostructure [2.24, 2.26], as shown in Figure 2.5 (a) and (b).

2.3 Formation of 2DEG

Unlike AlGaAs/GaAs HEMT, electrons forming 2DEG are supplied from the modulation-doped n-type AlGaAs layer. The 2DEG is formed in AlGaN/GaN HEMT even if AlGaN layer without intentional doping, it has been suggested that the source of 2DEG electrons come from the donor-like surface states. A surface donor model was proposed by J. P. Ibbetson in 2000, it assumes surface donors as the origin of 2DEG electrons and explains mechanism of 2DEG formation. He pointed out that space charge in the AlGaN/GaN HEMT structure include five types, negative charges in the 2DEG, polarization charges ($+\sigma_{PZ}$ and $-\sigma_{PZ}$), charges in the AlGaN layer due to doping ($+\sigma_{AlGaN}$), charge due to ionized surface states ($\sigma_{Surface}$) and buffer charge (σ_{buffer}) [2.27]. For an undoped AlGaN layer, $\sigma_{AlGaN} = 0$. Polarization charge is exactly zero due to polarization dipole formation. Furthermore, it assumes that the Fermi level lies close to

the GaN conduction band edge and setting $\sigma_{buffer} = 0$ [2.27]. Thus, the source of 2DEG electrons are surface states, as shown in Figure 2.6.

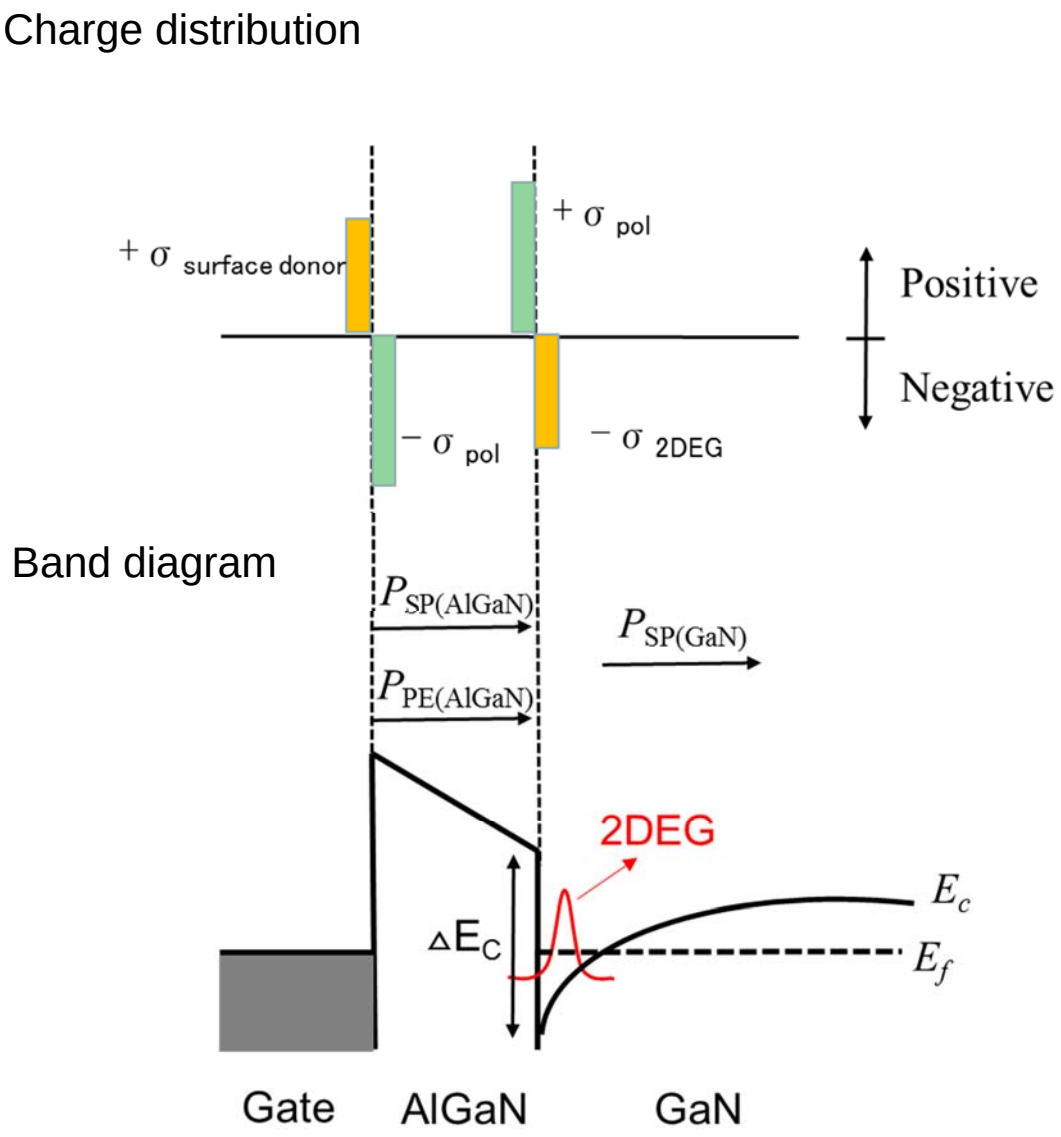

Figure 2.6 Schematic conduction band diagram and charge distribution for an AlGaN/GaN HEMT

It assume that the surface states below the conduction band edge of AlGaN layer is donor-like at energy E_D, which is neutral when occupied and positive when emptied. If the surface state below the Fermi level and this distance is sufficiently deep, no 2DEG electrons generated at the interface. With the increase of the barrier layer thickness until the donor energy reach the Fermi level, called critical thickness, electrons can transfer to the conduction band states due to strong polarization induced electrical field, more and more donor states to be emptied, leaving behind positive charge and thereby forming a high 2DEG density [2.27], as shown in Figure 2.7.

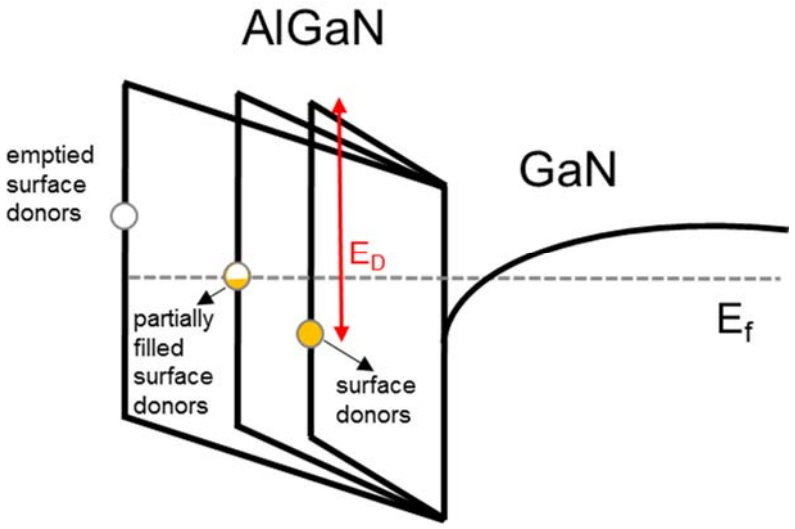

Figure 2.7 Schematic band diagram illustrating the surface donor model

The Al mole fraction of AlGaN layer can also affect 2DEG density, 2DEG density can increase with increasing the Al mole fraction due to larger bandgap, larger conduction band discontinuity and enhanced polarization effect [2.28]. Further increase in the AlGaN thickness and the Al mole fraction will cause decrease in 2DEG carrier density and deterioration of mobility, it is reasonable that strain relaxation in the AlGaN layer [2.26], as shown in Figure 2.8 [2.27].

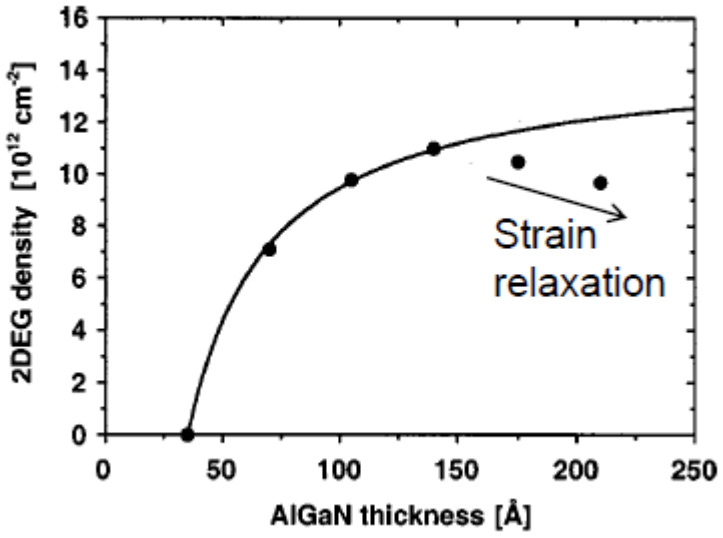

Figure 2.7 Room temperature 2DEG density measured as a function of $Al_{0.34}Ga_{0.64}N$ barrier thickness [2.27]

Donors-like surface states are the source of 2DEG electrons, these positive charge are compensated by polarization induced negative charges at the top of AlGaN layer. It has been suggested that native donors-like defects might be nitrogen vacancies or oxygen impurities [2.29-2.33]. SiN passivation layer can increase 2DEG density in AlGaN/GaN

HEMT due to reduced surface barrier after passivation [2.29]. SiN passivation induced positive charges are neutralized by polarization induced negative charges at the interface between SiN layer and AlGaN barrier layer. Therefore, the surface barrier height decreases [2.34].

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Chapter 3: Fabrication process and Characterization Methods

In this chapter, the AlGaN/GaN substrates used in this study is described. Also, detailed processes for HEMT fabrication including cleaning, isolation, metallization and gate dielectric formations are summarized. Also, the characterization methods of the fabricated HEMT devices are stated.

3.1 AlGaN/GaN HEMT substrate

AlGaN/GaN wafers components affect the characteristic property of AlGaN/GaN HEMT device. GaN growth technique and conditions decide the defect density, buffer layer and substrate materials influence lattice mismatch and crack in AlGaN/GaN substrate. Furthermore, the thickness of AlGaN barrier layer and Al mole fraction are effect on the 2DEG density at the interface between AlGaN and GaN. Therefore, AlGaN/GaN substrate growth technique still greater improvement is expected. The substrate structure in this work is shown in Figure 3.1. AlGaN/GaN HEMT transistors were fabricated on undoped $Al_{0.25}Ga_{0.75}N$ (30nm) with GaN layers epitaxially grown on Si (111) wafers utilizing buffer layer.

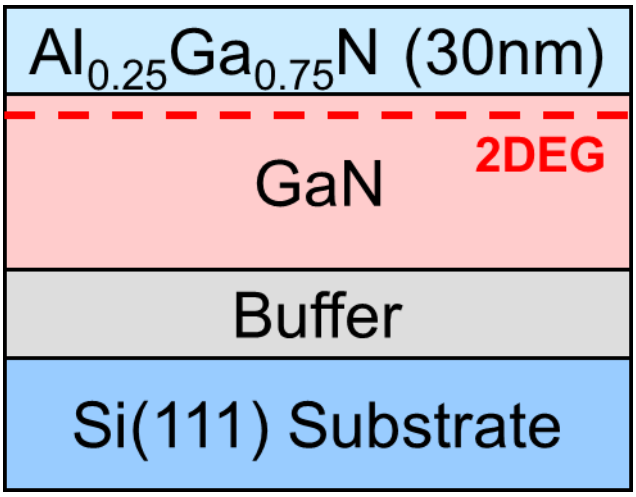

Figure 3.1 AlGaN/GaN HEMT substrate

3.2 Fabrication process

Because experiment is to select the suitable process and materials for achieving the goals of this work, the fabrication process have been changed along with the experimental results at different experimental stage. A brief description of the fabrication process is given as follow: after chemical cleaning of the substrate, mesa isolation was formed by inductively coupled plasma (ICP) etching with Cl_2-based gas. Source and drain contacts were formed by Ti-based metal and subsequently annealed in N_2 ambient for obtaining ohmic contact. Afterwards, a 100nm-thick SiO_2 film deposition was achieved. After channeal opening process, high-k gate dielectric material and gate metal are respectively deposited. Finally, electrical characterization of the devices are analyzed using leakage current density-voltage (J-V) and capacitance-voltage (C-V) measurement methods. The

detailed fabrication procedure is described separately in subsequent chapters.

3.2.1 Surface cleaning

During the device fabrication, the surface treatment and cleaning conditions are important. In the early stage of experiment, the wafers were treated by sulfuric-peroxide mixture (SPM) as same as Si wafers. SPM involves H_2O_2: H_2SO_4 mixture typically in 1:4 for 10 min at a hot plate temperature of 180 ºC. Subsequently, the wafers were treated by 1%HF for 1min. But then it was found that SPM treatment impinges an unfavorable influence on the AlGaN/GaN substrate which is the pit formation at the dislocations and the size of the pits became larger with longer time for the SPM treatment. Therefore, AlGaN/GaN wafers were simply cleaned by acetone and ethanol for 5 minutes separately in ultrasonic cleaning machine.

3.2.2 Device isolation

In order to separate each adjacent device, isolation process have been suggested. Either mesa etching or ion implantation is usually used to achieve device isolation of AlGaN/GaN HEMT. Low damage and highly controllable mesa etching process for AlGaN/GaN device are expected [3.1]. Ion implantation process for device isolation can offer planar device to improve the fabrication process yield and reduce mesa-sidewall gate leakage current compared to mesa etching [3.2]. An effective method of N_2 plasma for device isolation and effect of plasma gas on mesa etching of AlGaN/GaN device will be discussed in Appendix A. In this work, inductively coupled plasma reactive ion etching

(ICP-RIE) process with Cl_2-based gas is commonly used to form mesa isolation of AlGaN/GaN device. Typical advantage of inductively coupled plasma (ICP) etching is possible to independently control ICP power and bias RF power, which provide separate control over ion energy and ion density to adjust etching rate. In this work, SAMCO's RIE-101iPH was used to perform mesa etching process. The AlGaN/GaN samples were etched by ICP-RIE with ICP power 80 W and bias power 20W in a mixture gas of Cl_2 and Ar. AlGaN/GaN etch rate is 50 nm/min with a flow of Cl_2/Ar = 20/10 sccm.

3.2.3 Metallization

Parasitic contact resistances limited the performance of AlGaN/GaN HEMT device, minimization of the contact resistance is necessary. Therefore, metallization process for achieving low-resistance and thereby obtaining optimum device performance is quite important, includes two types, S/D ohmic contacts and Schottky contact.

Ti/Al-based metallization is commonly used for ohmic contacts of AlGaN/GaN HEMT with low resistance [3.3]. Nitrogen can be extracted from AlGaN to react with Ti at high temperature annealing, forming TiN islands and shows rough surface [3.4]. Reaction create a large amount of N vacancies as donors at the interface at the interface of metal/AlGaN [3.5].

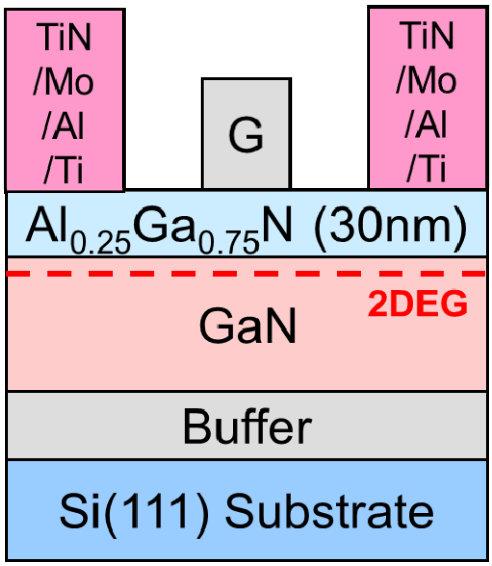

Figure 3.2 Ti (15nm)/Al (60nm)/Mo (35nm)/TiN (10nm) metallization as contact metal materials for AlGaN/GaN HEMT transistors

After device isolation was formed by inductively coupled plasma (ICP) etching with Cl_2-based gas, the next process of device fabrication was S/D ohmic contacts formation. Contact metals were deposited by RF sputtering. In RF magnetron sputtering, a thin film is grown on a substrate that is placed in a vacuum chamber. Once the substrate is placed into the vacuum chamber, the air is removed and argon gas is introduced to the chamber, particles of the target material are ionized and the ions collide with the argon gas atoms at high pressure. The negatively charged target material lines up on the substrate to form a thin film. Thin films can range in thickness from a few to a few hundred atoms or molecules [3.6]. Ti (15nm)/Al (60nm)/Mo (35nm)/TiN (10nm) metallization as contact metal materials are used for AlGaN/GaN HEMT transistors, as shown as Figure 3.2. TiN was deposited by RF sputtering in an argon and nitrogen gas mixture ambient, the ratio is Ar/ N_2 = 8:2. After metal deposition, rapid thermal annealing (RTA) was carried out for

forming ohmic contacts at 950ºC in N_2 ambient for 1min. The ohmic contacts are patterned by lift-off.

Schottky contacts on AlGaN/GaN structure is an important element for device operation. The characteristics of Schottky diodes depend on the properties of metal and AlGaN and surface state on the AlGaN layer. Large leakage current through Schottky contacts degrade gate controllability and increase the power consumption. Therefore, Schottky contacts have been developed for the applications of AlGaN/GaN HEMT.

3.2.4 Gate dielectrics

In order to suppressed the gate leakage current of AlGaN/GaN HEMT structure, High-k gate dielectrics were deposited in ultra-high vacuum by electron-beam evaporation method.

In this work La_2O_3 thin film was deposited by e-beam evaporation at room temperature. The pressure in the chamber during depositions was 10^{-7}~10^{-5} Pa. Electron beam, which is accelerated by a 5 kV electric field, is emitted and bombarded to the La_2O_3 source under the control of a magnetic sweep controller. A film thickness counter is used for monitoring the physical film thickness in real time. The growth rate of the thin film is controlled at 0.003 A/s to 0.005 A/s to ensure the quality of the film.

3.3 Electrical characterization method

The fabricated HEMTs were electrically measured by on-wafer probe station. This study mainly focuses on the characterization of current measurements and capacitance measurements.

3.3.1 Leakage current density-voltage (J-V) measurement

J-V measurement was performed using HP4156C semiconductor parameter analyzer. In order to tracing the switching behaviors, a sweep voltage started from –10 V and swept towards +5 V, with a step of 0.05 V.

3.3.2 Capacitance-voltage (C-V) measurement

C-V characteristic measurements were performed with various frequencies (1 kHz~1 MHz) by precision LCR Meter (E4980A, Agilent).

The intrinsic energy level E_i or potential, ϕ, in the neutral part of device is taken as the zero reference potential. The surface potential, ϕ_s, is measured from this reference level. The capacitance is defined as

$$C = \frac{dQ}{dV}, \qquad \text{Eq. (3.3.1)}$$

where Q is the charges and V is the applied gate voltage. It is the change of charge due to a change of voltage and is most commonly given in units of farad/unit area [3.7].

Reference

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Chapter 4: Poly-Si gate electrode for V_{th} control and leakage current suppression

In this chapter, boron doped poly-Si gate electrodes are introduced for AlGaN/GaN HEMT and its process compatibility is discussed. The BF_2^+ ion implantation energy dependent threshold voltage tuning was confirmed, suggesting the feasibility to achieve normally-off HEMT devices. A large suppression in the gate leakage current as well as high reliability against stress test were performed. The issues related to the doping including mobility degradation accompanied by enhanced diffusion of F ions, sheet resistivity of poly-Si gate electrodes are discussed.

4.1 Introduction

The V_{th} of a typical AlGaN/GaN HEMT is around -4 V. V_{th} is dependent on the Schottky barrier height (ϕ_B), the carrier concentration (N_d) and the thickness of the AlGaN layer (d). Analytically, V_{th} is expressed as:

$$V_{th} = \phi_B - \frac{qN_d d^2}{2\varepsilon_0 \varepsilon_S} - \frac{\Delta E_c}{q} + \frac{E_F}{q}, \qquad \text{Eq. (4.1.1)}$$

where N_d is the carrier concentration, which depends on the design of the epitaxial structure such as the Al mole fraction and doping concentration. Large ϕ_B or low N_d, thinner d are the strait forward way to obtain a normally-off operation.

The Schottky gate on AlGaN/GaN is an issue for HEMT as it gives large leakage

current. Also, the interface at the gate metal and the AlGaN layer induces defects which worsens the reliability of the devices. Various Schottky electrode materials for AlGaN/GaN HEMT have been reported so far, including Ni, Pt/Au, and W. Unfortunately, general metal gates have poor thermal stability, which affect performance of AlGaN/GaN HEMT. For instance, Ni is react easily with AlGaN layer to form oxides at the metal/AlGaN interface, which may change the electrical properties and then influence device failure [4.7]. High fields lead to defect formation under gate electrode region after stressing step. These defects present under the gate are associated with gate sinking, which increased gate leakage current [4.8]. On the contrary, Pt electrodes show sharp interface between metal and AlGaN layer, however, crack formation during electrical stress applications are reported due to piezoelectric strain induction. Therefore, much more stable gate metal material has been required to improve reliability of AlGaN/GaN HEMTs.

In this thesis, p^+-polycrystalline silicon was selected as a gate electrode material, as the material has high thermal stability against agglomeration and is robust against oxidation by residual oxygen atoms in the annealing ambient [4.9]. Moreover, the process is compatible with conventional process and can be easily patterned by plasma etching equipment. In addition, F ion incorporation, which is commonly utilized to shift the V_{th}, can also be implemented by using BF_2 ion implantation for realizing p^+-type poly-Si.

4.2 Poly-Si gate electrode for AlGaN/GaN HEMT

Poly-Si has high melting point and adjustable work function dependent on different doping concentration. When deposited on the AlGaN layer with subsequent annealing at

1075 ºC for 1 min, a thin interface layer formation between poly-Si and AlGaN layer as in Figure 4.1 have been confirmed. The layer was found to be SiON, which was confirmed by electron energy loss spectroscopy (EELS) of the layer. Therefore, it can be concluded that poly-Si reacts with the AlGaN surface but is limited to the very surface. Note that there were no enhanced reaction at the dislocations of the AlGaN layer. Moreover, the formation of SiON layer might eliminate the issue of Fermi-level pining.

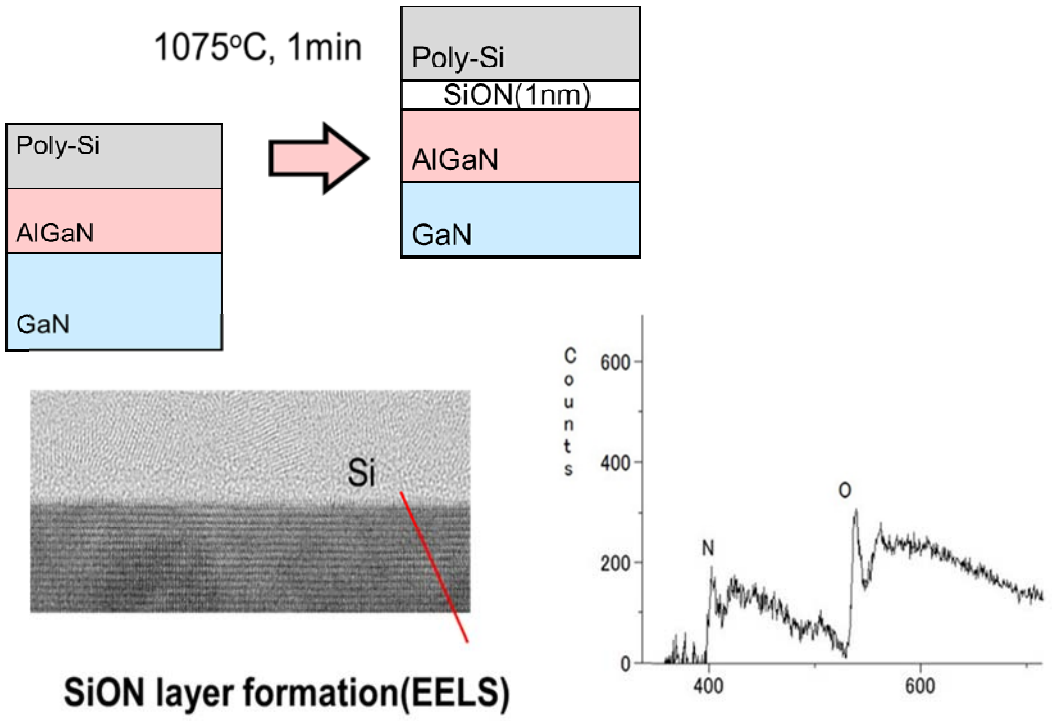

Figure 4.1 Interface SiON formation after annealing process and SiON formation have been confirmed by EELS

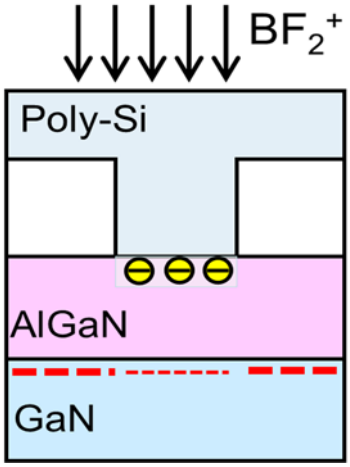

Figure 4.2 Poly-Si gate and BF_2 ion implantation approach toward normally off operation

BF_2 ion implantation process was used for threshold voltage control of AlGaN/GaN HEMT. BF_2 ion implant down to the middle of AlGaN layer, which can reduce polarization effect, and thereby deplete the two-dimensional electron gas (2DEG) in the channel as show as Figure 4.2.

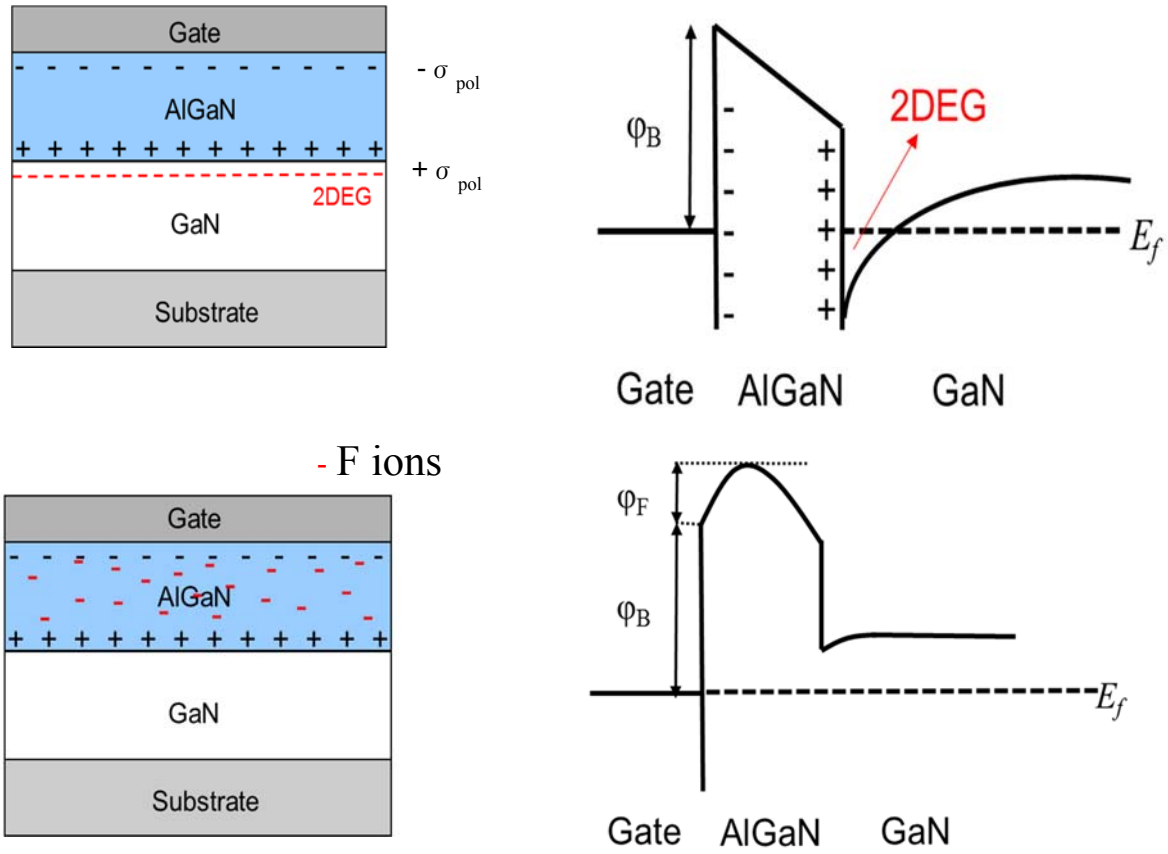

Figure 4.3 Negative fixed charges for threshold voltage control

F ions incorporated in AlGaN layer, capture a free electron and become a negative fixed charge, these negative fixed charges bend the conduction band upwards and deplete the 2DEG to control V_{th}, as shown in Figure 4.3 [4.6].

4.2.1 Experimental Procedure

Poly-Si electrode formation process was carried out through BF_2 ion implantation as Figure 4.4 shows. 400 nanometers SiO_2 grown on *n*-Si (100) substrates were fabricated for poly-Si electrode formation process. After performing sulfuric peroxide mixture cleaning followed by HF dip cleanings, Si films with thickness of 30nm were deposited

by e-beam evaporation at a substrate temperature of 500 ^{o}C in ultra-high vacuum. BF_2 ions implant to the samples with different ion implantation conditions. Then, activation annealing was carried out immediately for poly-Si formation. Activation annealing process compatibility with ohmic contacts process at any typical range of annealing temperature. Resistivity of poly-Si measured by 4 point probe, the results with different BF_2 ion implantation conditions, annealing temperature and annealing time are shown as Figure 4.5.

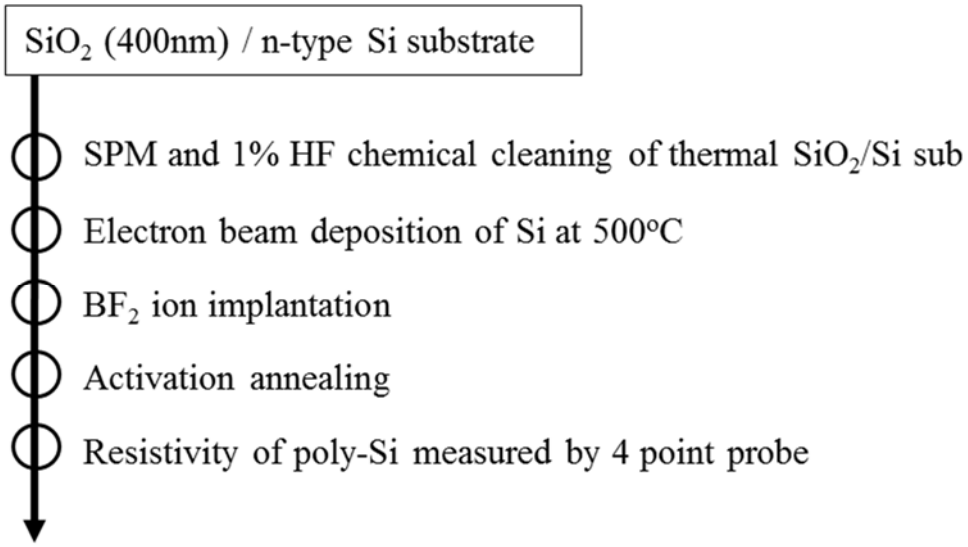

Figure 4.4 Poly-Si formation process

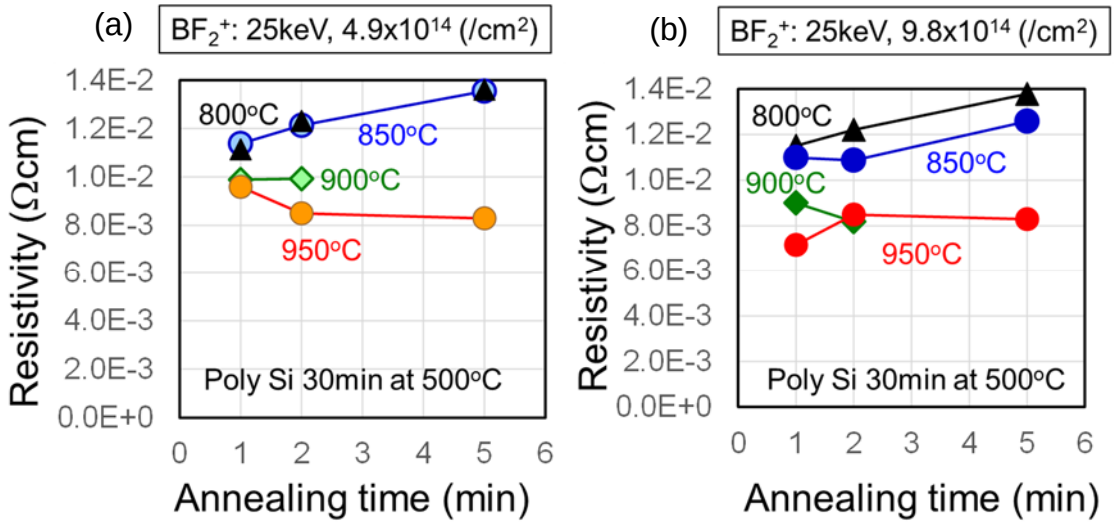

Figure 4.5 Poly-Si resistivity dependent on annealing time

Annealing temperature is one of the most important parameters for poly-Si formation. In this poly-Si formation process, annealing temperature are range from 800°C to 950°C, BF_2 ion implantation energy is 25keV, dose concentration is $4.9\times10^{14}/cm^2$ and $9.8\times10^{14}/cm^2$, respectively. Figure 4.5 (a) shows BF_2 ion implantation energy and dose concentration are 25keV, $4.9\times10^{14}/cm^2$. Resistivity increased with annealing time increase at 800°C and 850°C. It could not be seen change with annealing time increase at 900°C. At 950°C, reduction in resistivity with longer annealing time. The relation of resistivity and annealing time at more higher dose concentration $9.8\times10^{14}/cm^2$ are shown as Figure 4.5 (b). Resistivity is increased with longer annealing time at 800°C. Slight decrease in annealing time of 2min at 850°C, with longer annealing time, resistivity is gradually increased. At higher annealing temperature of 900°C, resistivity reduced obviously. Increased in resistivity with longer annealing time at 950°C. Form the results in Figure 4.5 (a) and (b), stable increased in resistivity with longer annealing time under

900°C. The resistivity of poly-Si is around $1 \times 10^{-2}\Omega$cm. Poly-Si formation can be confirmed.

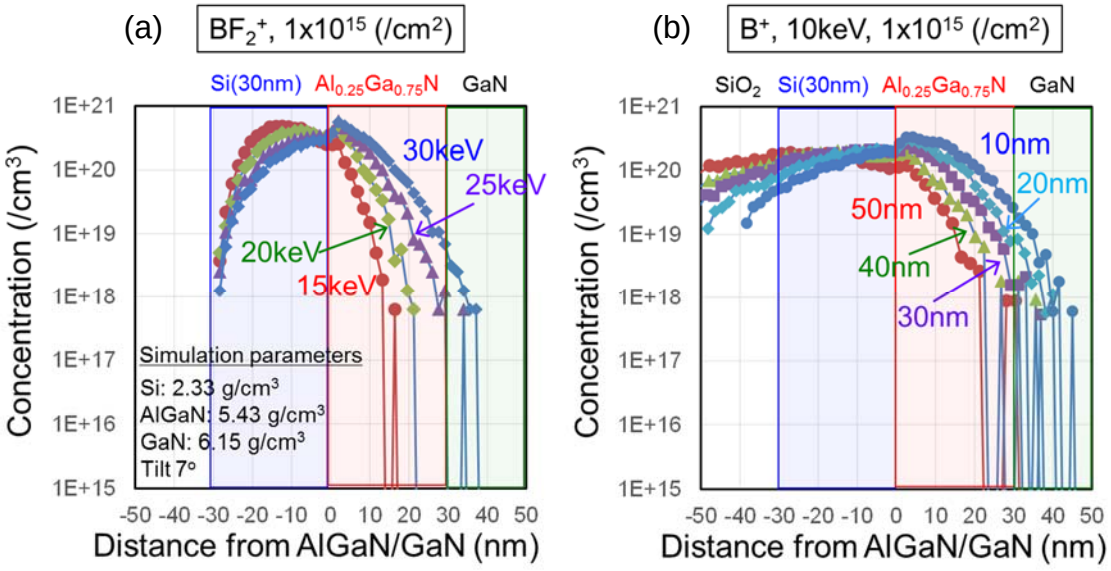

Figure 4.6 TRIM profiles of BF_2^+ (a) and B^+ (b) implants into Si/AlGaN/GaN substrate

BF_2^+ and B^+ implants into Si/AlGaN/GaN substrate are simulated in TRIM, which is shown as Figure. 4.6. Introduction BF_2^+ into Si/AlGaN/GaN substrate by variable ion implantation energy at 7° wafer tilt and a dose of $4.9 \times 10^{14}/cm^2$, ion implantation depth in substrate can be seen as Figure 4.6 (a). BF_2 should be implanted close to 5nm of 2DEG. which can obtain normally off characteristics. B is most common p-type dopant for Si. The lowest B ion implantation energy is 10keV in our tools, SiO_2 layer need to be used for closing to 5nm due to ^{11}B lighter than BF_2. The relation of required SiO_2 film thickness and depth to the substrate is simulated as Figure 4.6 (b) shows. In our case, BF_2 ion implantation are selected for transistors because of fluorine can trap interstitial silicon.

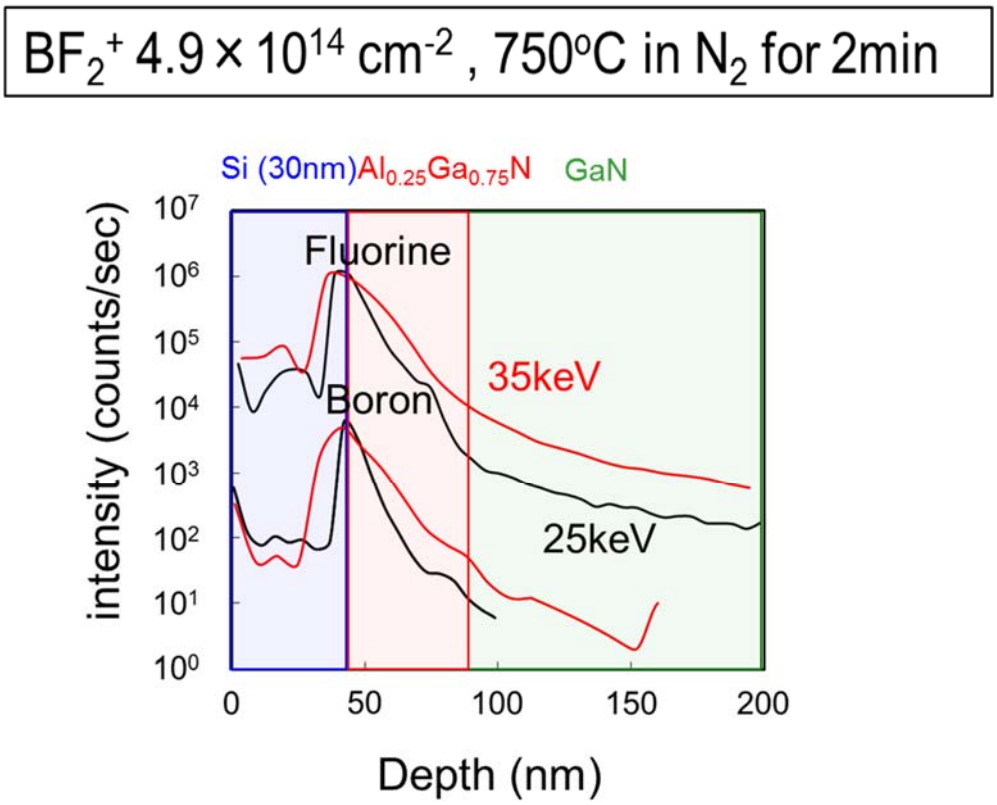

Figure 4.7 SIMS profiles of BF_2^+ implants into Si/AlGaN/GaN substrate

SIMS (secondary ion mass spectrometry) is usually used for measuring dopant with depth in compound semiconductors. 25keV and 35keV BF_2^+ were implanted in Si (30nm)/AlGaN (30nm)/GaN substrate with dose concentration of $4.9 \times 10^{14}/cm^2$, respectively. For the electrical activation, the implanted samples were annealed at 750°C in nitrogen ambient for 2 minutes. The implanted profiles were measured by using secondary ion mass spectrometry. The measurement results were characterized as Figure. 4.7 shows. A larger amount B and F ions implanted into the substrate with higher ion implantation energy.

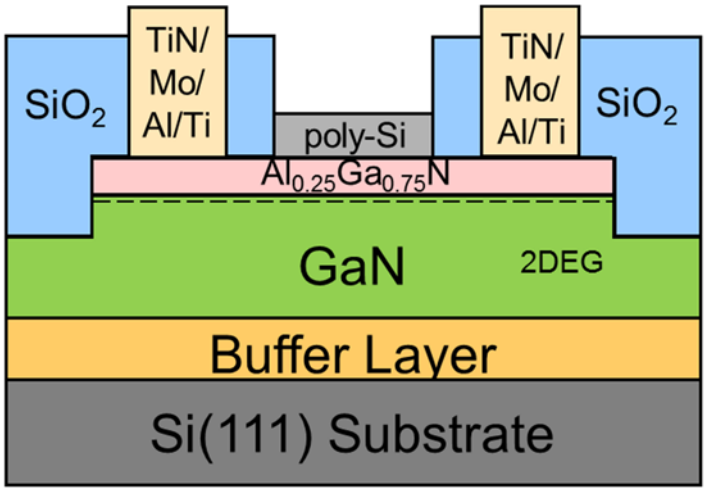

Figure 4.8 Device structure of AlGaN/GaN HEMT with poly-Si gate

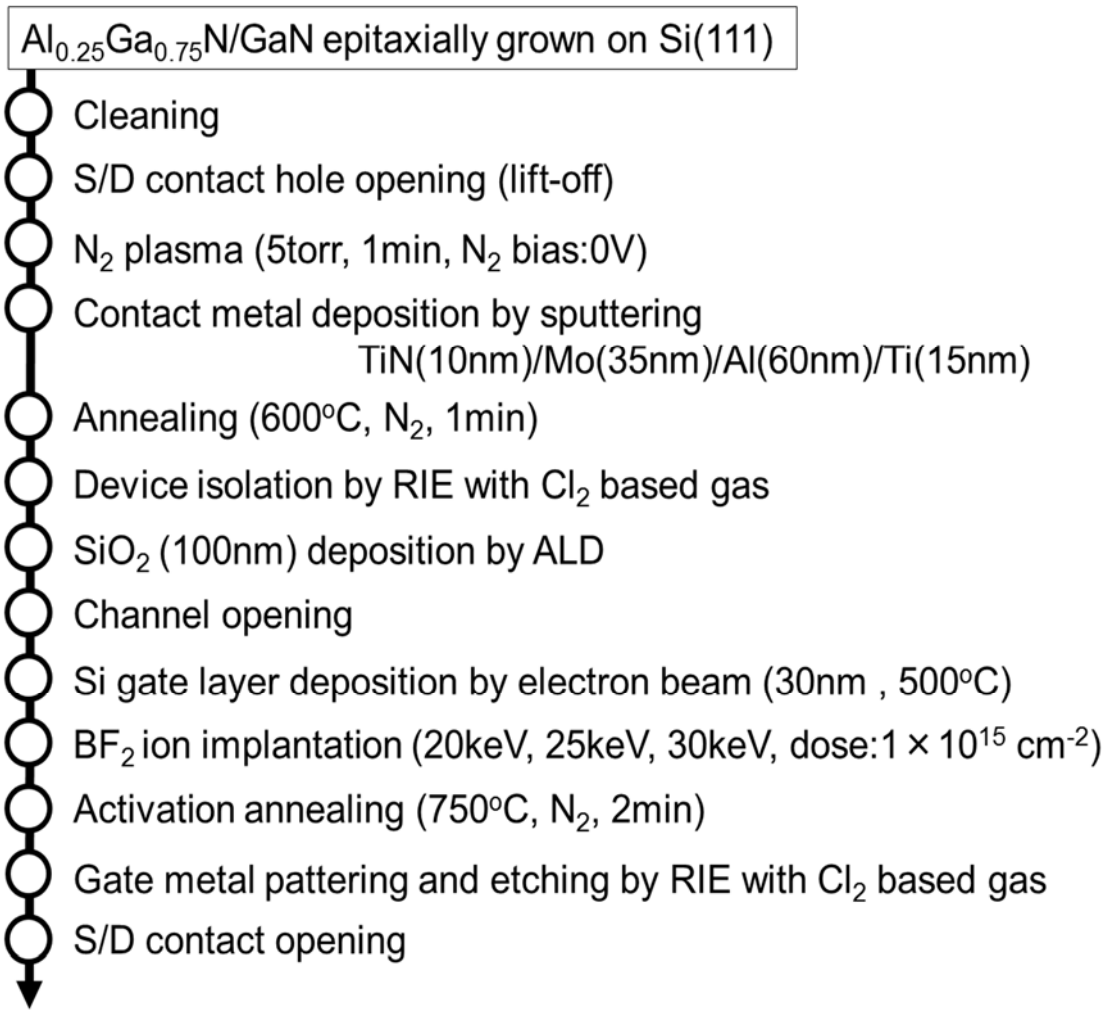

Figure 4.9 Fabrication process of AlGaN/GaN HEMT with poly-Si gate

Transistors were fabricated on $Al_{0.25}GaN_{0.75}$/GaN epitaxial grown on Si (111) substrate. The device structure and fabrication process is shown in Figure 4.8 and Figure 4.9, respectively. After the mesa isolation formation by reactive ion etching (RIE) with Cl_2-based plasma, ohmic contacts were formed by TiN/Mo/Al/Ti for 1min at 600°C in N_2 ambient. Prior to the TiN/Mo/Al/Ti deposition, N_2 plasma treatment at 5 torr for 1min were carried out in S/D regions. 100nm SiO_2 was deposited by ALD. 30nm Si Schottky gate was deposited by E-beam evaporation at a substrate temperature of 500 °C. Then, BF_2 ions implant to the device, ion implantation energy is 20 keV, 25 keV and 30 keV,

respectively. Dose concentration is 4.9×10^{14} (/cm^2). Activation annealing was carried out immediately for poly-Si formation at 750^{o}C in N_2 for 2min. In order to investigate the contributions of poly-Si gate for AlGaN/GaN HEMT, TiN gate with a thickness of 50nm was fabricated as reference electrode. TiN was deposited in an argon (Ar) and nitrogen (N_2) gas mixture ambient and flow ration for Ar: N_2=8:2 by RF sputtering. The electrodes were patterned by RIE with Cl_2-based chemistry. Gate length (25 μm) and width (100 μm) of the gate electrode area are used for the measurements.

After the measurements of the initial characteristics, the sample of poly-Si gate with 20keV BF_2 ion implantation and TiN gate electrode were measured. The electrical stress at the OFF–state below threshold voltage (V_{th}) was applied to AlGaN/GaN HEMT. The stress at the gate (V_{GS}) and drain (V_{DS}) was ranged from -8 V to -14V and 0 V to 30 V, respectively. The bias stress step and the stress time during the OFF–state was 0.5V and 20 sec, respectively.

4.2.2 Results and discussion

The threshold voltage of AlGaN/GaN HEMT with poly-Si gate electrodes dependent on various BF_2 ion implantation energy are shown in Figure 4.10. The threshold voltage shifts to the positive direction with increased BF_2 ion implantation energy. It has been known that more F and B ions implanted to the substrate with higher energy. Fluorine has a strong electronegativity and large amount fluorine implanted to the AlGaN barrier layer that caught electron to become negative fixed charge. These negative fixed charge modulate the potential and deplete 2DEG in the channel [4.6]. When it reach a certain value, there is no 2DEG in the channel and the threshold voltage value presents positive.

In this case, positive threshold voltage is obtained with BF_2 ion implantation energy over 25 keV. Normally-off characteristics of AlGaN/GaN HEMT has been confirmed.

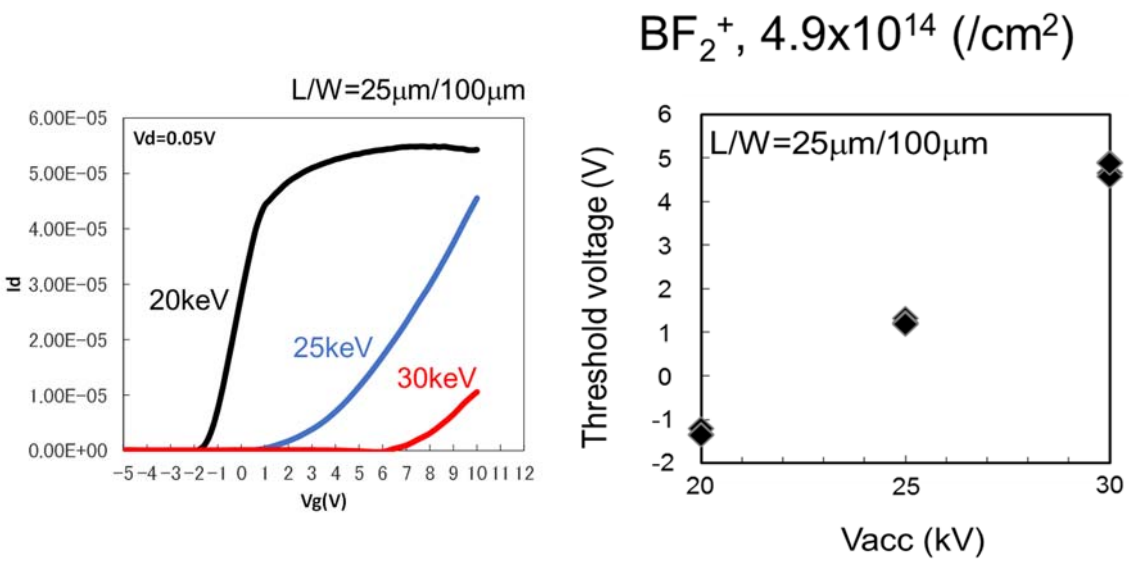

Figure 4.10 I_d-V_g characteristics and threshold voltage dependent on the BF_2 ion implantation energy

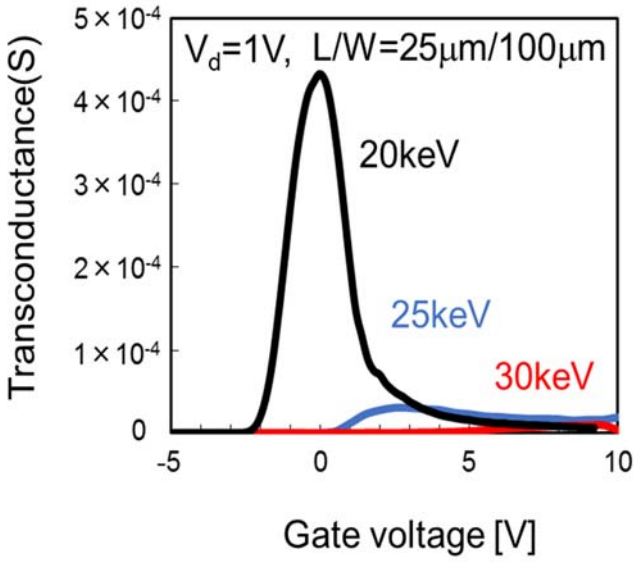

Figure 4.11 g_m characteristics of AlGaN/GaN HEMT with poly-Si gate electrodes

Figure 4.11 shows transconductance (g_m) characteristics of AlGaN/GaN HEMT with poly-Si gate electrodes. Drain current decrease with larger ion implantation energy, the reason is considered that some ions through AlGaN layer into the GaN layer, generated trapes leads to reduce drain current. Moblility decrease with increasing doping concentration due to increase scattering from high concentrations of ionized impurities.

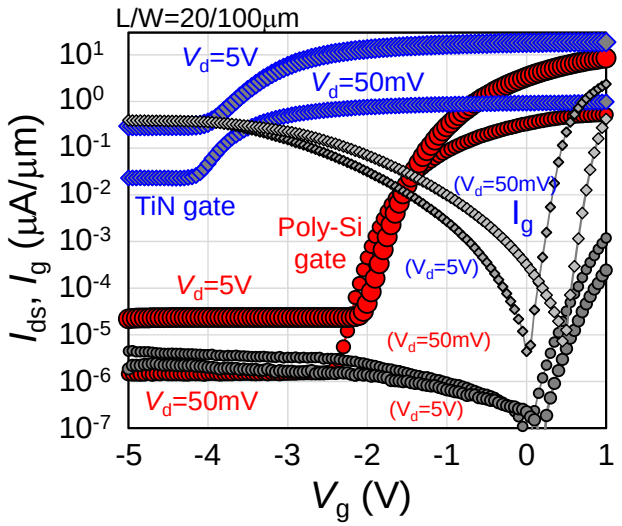

Figure 4.12 Transfer characteristics of HEMT devices with poly-Si and TiN gate electrodes. A large reduction in J_g can be achieved with the poly-Si gate electrode.

Transfer characteristics of HEMTs with poly-Si and TiN gate electrodes are shown in Figure 4.12, where gate leakage currents are also plotted. A positive V_{th} shift was observed with the poly-Si gated device, which is in good agreement with F-ion-treated HEMTs. The off-characteristics of the TiN-gated device is mainly determined by the gate leakage current (J_g), where a high gate leakage current by 4 orders of magnitude is measured

compared to that of poly-Si electrodes. Generally, the J_g depends on the properties of the AlGaN layer and surface, nitrogen vacancies and pits and/or dislocations in the crystal [4.10, 4.11], however, as the same epitaxial wafers are used, the difference might be due to the damage creation during reactive sputtering plasma process. The J_g at on-state (V_g=1) also showed reduction by 2 orders of magnitude with the poly-Si gate electrode. Therefore, poly-Si gate electrodes are effective in reducing the gate leakage current in both on and off-states.

Effective mobility for electrons (μ_{eff}) on 2DEG density (N_s), shown in Figure 4.13, revealed reduction in lower carrier density range, suggesting the presence of Coulomb scattering near the interface of AlGaN and GaN layers [4.12]. Secondary ion mass spectroscopy (SIMS) measurement of a sample with the same structure after annealing, shown in Figure 4.14 revealed the presence of F ions distributing in the AlGaN layer and some of them exist in the GaN layer. The distribution of B atoms showed fairly nice agreement with as-implanted simulation profile, therefore, the F atoms seems to be diffused during the annealing process. Indeed, diffusion of F atoms is reported for AlGaN/GaN structure when annealed over a temperature of 350 ^{o}C [4.13], and also degradation is observed in μ_{eff} [4.14]. Based on the above consideration, the origin of the additional scattering source can be considered to be F ions as they are negatively charged in the AlGaN layers. Therefore, one need to consider the effect of F ion diffusion with thermal treatment to compromise the V_{th} shift and μ_{eff} degradation.

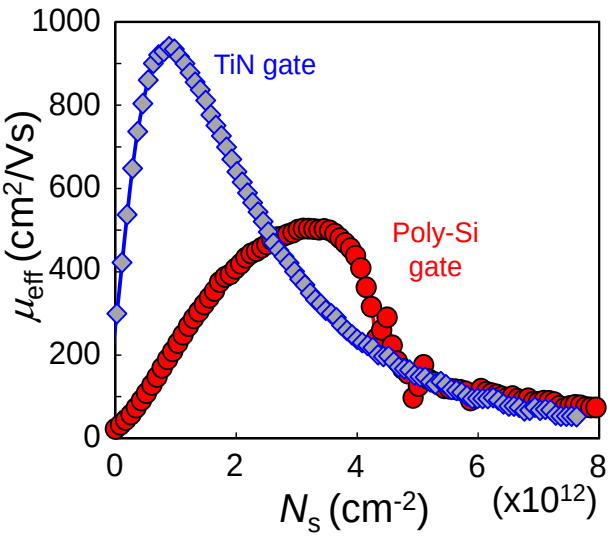

Figure 4.13 Extracted effective electron mobility of both devices, showing large degradation with BF_2 implantation.

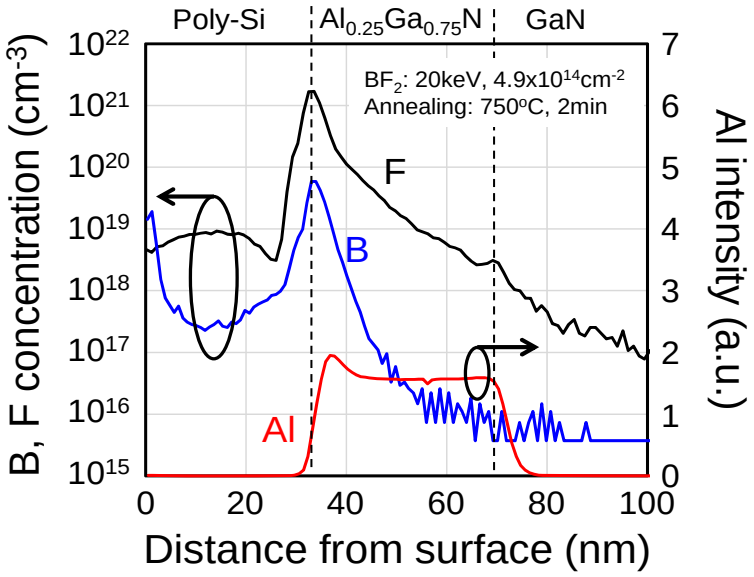

Figure 4.14 SIMS depth profiles of F, B and Al atoms. Distribution of F atoms into AlGaN/GaN interface and also into GaN layer is confirmed.

A stress voltage to the gate electrodes, ranging from -8 to -16 V, was applied to the devices for 20 sec, while applying 20 V to the drain electrode. Under this condition, a high electric field at the drain side edge of the gate electrodes is applied and electron injections from gate to AlGaN layer occurs. Figure 4.15 shows the change in the J_g after each stress applications, where an increase in J_g can be seen with higher stress. When a voltage lower than -11 V was applied, a change in the leakage conduction can be seen in the V_g range of -2 to 0.5 V. As the increase is observed in both negative and positive bias regions, suggesting a creation of novel conduction path in the leakage current. Recent analysis of Pt gate electrodes on AlGaN/GaN structure showed the presence of an interfacial layer at metal/AlGaN interface, suggesting the presence interface reaction [4.15]. A pit-like defect creation at the interface layer and also in the AlGaN layer is reported after reverse bias stress application, near the drain edge of the electrode, which is explained by the inverse piezoelectric stress, where additional tensile strain is applied to the AlGaN layer. In addition to the defect creation, diffusion of Pt atoms into the pit is clearly observed. Defect creation after reverse bias stress application is also confirmed by electroluminescence (EL) study, where a strong correlation is reported between EL intensity and gate leakage current [4.16]. Although, the gate material is different from the reference, creation of pits in the AlGaN layer with electromigration of Ti atoms into the defects might be the source for the increase in leakage current.

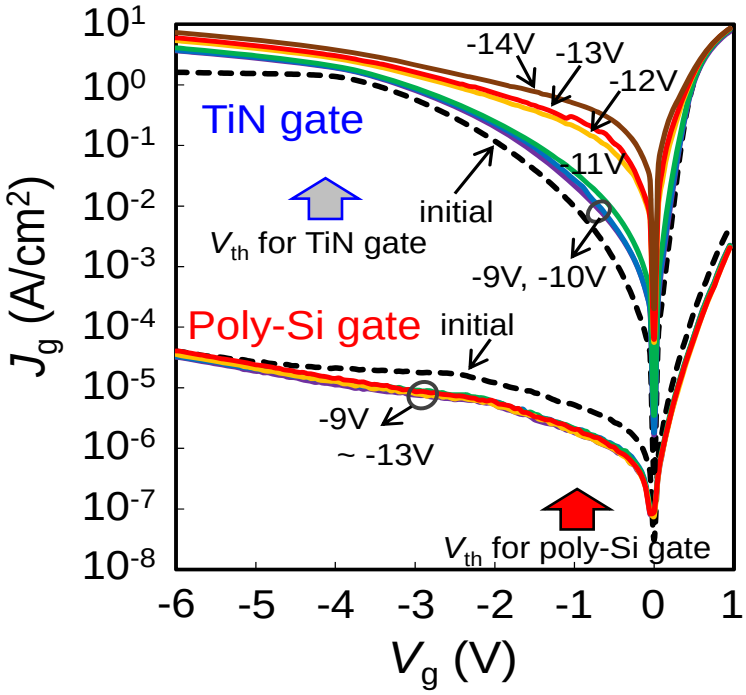

Figure 4.15 Leakage current characteristics of both devices after each stress voltage applications.

On the other hand, a slight decrease in the J_g was observed with the devices with poly-Si gate electrodes, and the value showed little change after further stress application. The fact suggests initial electron filling into trap sites in the AlGaN layer occurs and no further trap sites are generated by stress application. The difference against TiN electrode might be the presence of band bending in the poly-Si layer to reduce the electric filed in the AlGaN layer. Moreover, a formation of SiON layer with low dielectric constant at the poly-Si and AlGaN interface, which is clearly observed at elevated annealing temperature, may also help reduce the field. Poly-Si gate may also suffer from pit formations by the

inverse piezoelectric. However, in terms of the diffusion, Si atoms are expected to diffuse in the form of insulator (oxide or nitride), therefore, the leakage path may not contribute to the gate leakage current.

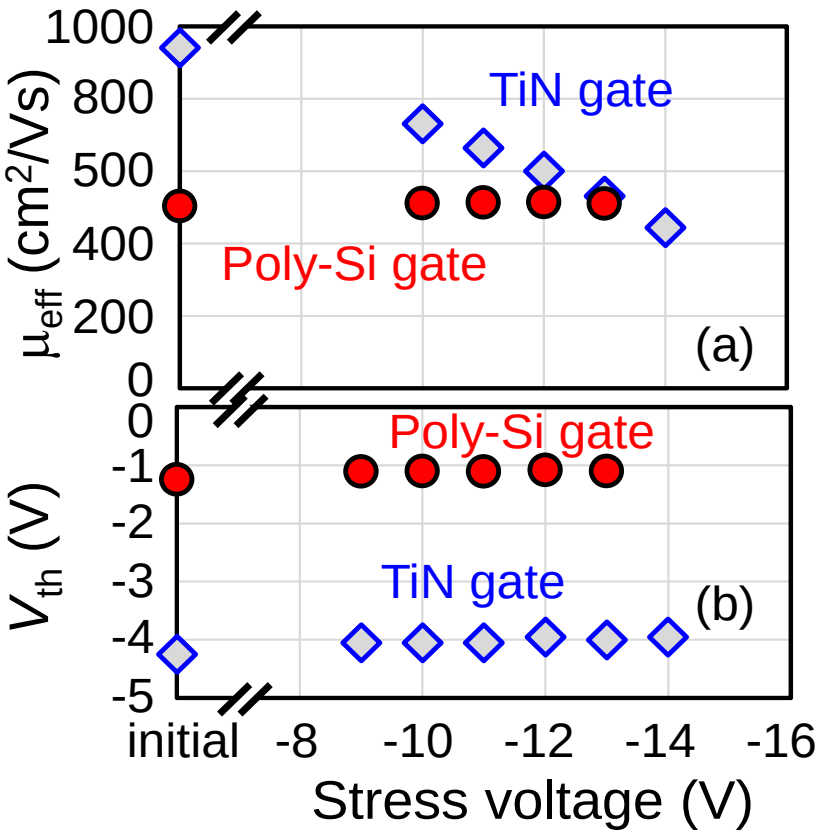

Figure 4.16 (a) Maximum effective mobility and (b) V_{th} change after each reverse-bias stress voltage applications.

The μ_{eff} of the samples at the peak value and the the V_{th} of the device after stress application are shown in Figure 4.16 (a) and (b). To examine time dependent characteristics, the devices are stressed under V_g = -12V and V_d = 20V up to 1000 sec at room temperature, as shown in Figure 4.17 (a) and (b).

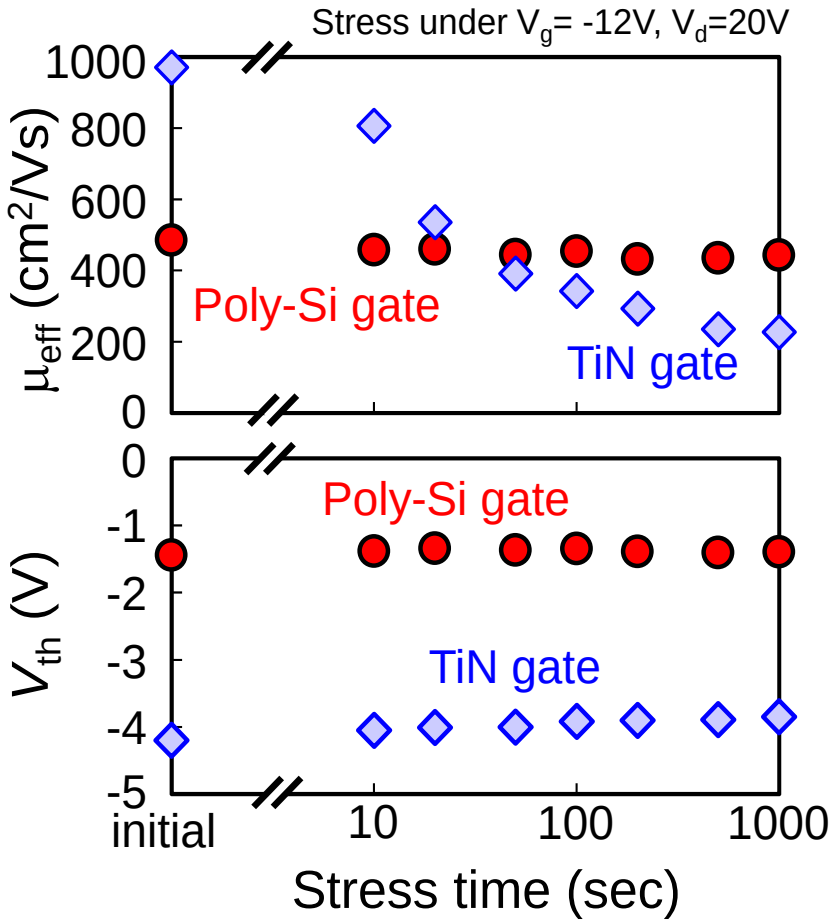

Figure 4.17 (a) Maximum μ_{eff} and (b) V_{th} change with increasing the stress time

A monotonic decrease in the μ_{eff} was observed with the TiN-gated device, suggesting an additional scattering source is presented with the stress application. Indeed, the V_{th} of

the device showed a slight positive shift after stress application, indicating trapping of injected electrons in the AlGaN layer or at the interface of AlGaN and GaN layers. In contrast, the μ_{eff} of the poly-Si device showed no change after stress application. A higher reliability with poly-Si gated devices may be attributed to suppressed electron injections by reduced gate leakage current. As a result, the TiN gated device showed degraded μ_{eff} comparable or even reduced values that of the poly-Si gated device after the stress application. Therefore, poly-Si gate electrodes have advantages over the TiN Schottky gate in terms of reliability.

4.3 Conclusion

Electrical characterization of poly-Si gate electrodes with BF_2 implantation for GaN HEMT has been performed. Normally-off characteristics can be obtained over 25keV with BF_2 ion implantation. Compared to TiN gate electrodes, poly-Si gate electrodes showed positive V_{th} shift by F ion incorporation and revealed reduced gate leakage current. The electron mobility was found to be degraded due to F ion penetration into AlGaN/GaN interface and GaN layer. However, stable V_{th} with low J_g against reverse-bias stressing was obtained with poly-Si gate electrodes.

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Chapter 5: La_2O_3 gate dielectrics for AlGaN/GaN HEMT

We attempt to use La_2O_3 as a gate dielectric for AlGaN/GaN HEMT owing to its wide bandgap of 5.5eV, high dielectric constant of 23.4 and nice interface properties with substrate. In this chapter, electrical characteristics of AlGaN/GaN HEMT with La_2O_3 gate dielectrics have been investigated. After annealing process, an interface layer formation have been confirmed. Capacitance increase and positive threshold voltage shift are obtained with increasing annealing temperature.

5.1 Introduction

AlGaN/GaN high electron mobility transistor (HEMT) structures have been strong candidates for power devices with low power consumption. The major factor that limit the performance and reliability of AlGaN/GaN high-electron mobility transistors (HEMTs) is high gate leakage current [5.1], which increases losses in the devices. To reduce the gate leakage current, introduction of gate dielectrics, especially high-k materials, to form MOSHFET has been shown to be effective [5.2]. Some of drawbacks of the MOS structure is that the gate capacitance decreases due to series connection of gate dielectrics to AlGaN layer, which reduces the drain current as well as transconductance. Also, due to increased gate-to-channel distance by gate dielectrics

insertion, the V_{th} shifts to negative direction, which poses difficulty in designing driver circuits [5.3]. Thinner gate dielectric layer can suppress those side effects to some degree, however, there is a trade-off between the gate leakage current. Therefore, the use of a gate dielectric material with a high permittivity, a high k-value, is mandatory to relax the trade-off relation. As for V_{th} shift, a negatively charged interface at the dielectric and the AlGaN layer is preferable as the charges shift the V_{th} to positive direction [5.4]

We propose to use lanthanum oxide (La_2O_3) as gate dielectrics. La_2O_3 is one of the rare earth oxides has been tried as gate dielectric, because it has a wide bandgap of 5.5 eV and a k-value of 23.4. This material is known to react with substrates, including Si, Ge and InGaAs. One of the features of this material is that reactively formed interface layers show fairly nice interface properties, so that interface state density of 10^{10}can be achieved for Si and 10^{11} can be achieved for both Ge and InGaAs.

5.2 Experimental procedure

AlGaN/GaN HEMTs with La_2O_3 gate dielectrics were fabricated on an undoped 24-nm-thick $Al_{0.25}Ga_{0.75}N$ layer on GaN layers epitaxially grown on a Si (111) substrate. Figure 5.1 shows the fabrication flow of AlGaN/GaN transistors. After chemical cleaning of the substrate, a 100nm-thick SiO_2 layer was deposited using plasma-enhanced chemical vapor deposition (PECVD). Mesa isolation was formed by inductively coupled plasma (ICP) etching with Cl_2-based gas. Source and drain contacts were formed by titanium-based metal and subsequently annealed in N_2 ambient at 750 ^oC for 1min.

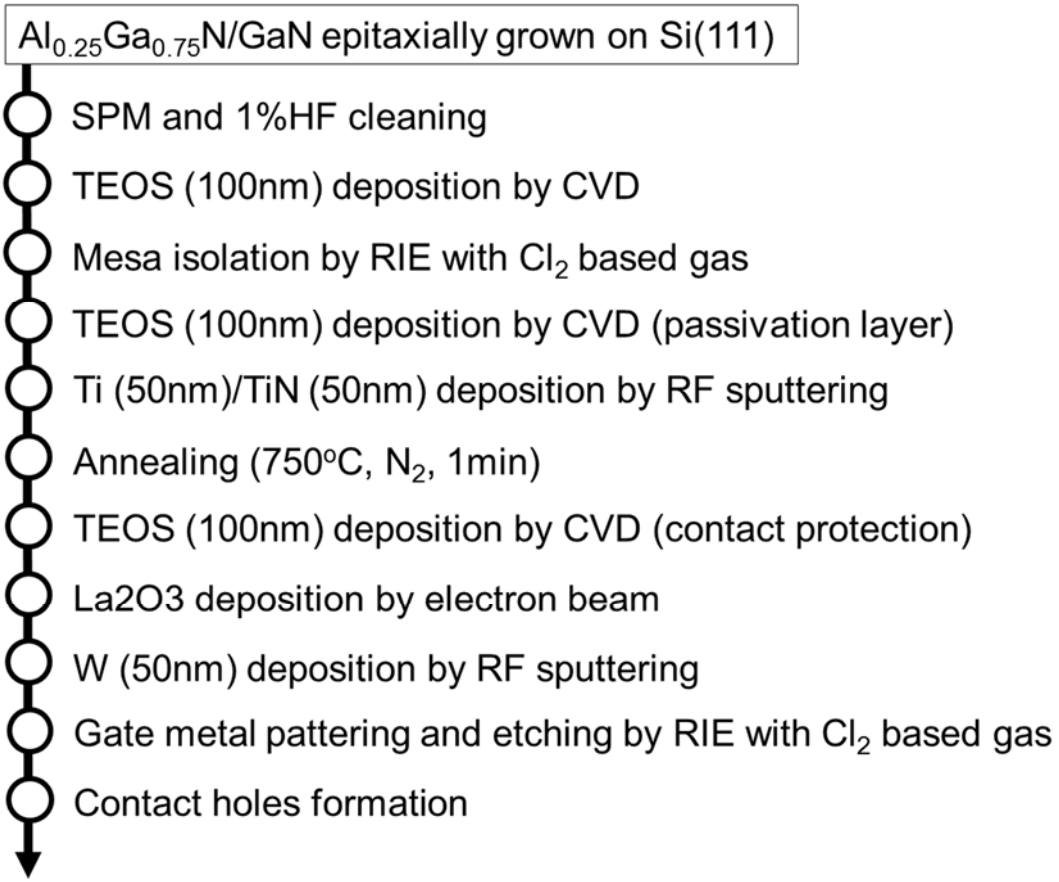

Figure 5.1 Fabrication process of AlGaN/GaN HEMT with La_2O_3 gate dielectrics

Afterwards, La_2O_3 gate materials were deposited by electron-beam evaporation in an ultra-high vacuum at a pressure of 10^{-6} Pa and at room temperature. After La_2O_3 deposition, a 50nm-thick tungsten (W) layer was *in-situ* deposited using RF magnetron sputtering without exposing the wafers to air to minimize high-k layer moisture absorption or contamination. The W layer was patterned by web etching using H_2O_2 solution to form gate electrodes. Then contact holes to source and drain regions were formed. An FET using W Schottky gate without high-k materials was also fabricated as a reference. Finally, devices were post-metallization annealed (PMA) using a rapid thermal annealing (RTA) furnace in forming gas (F.G) (N_2:H_2=97%:3%) ambient at various

temperatures. Electrical characteristics of AlGaN/GaN HEMT with La_2O_3 gate dielectrics have been investigated. After intimal measurement, annealing process with different temperature were carried out. Annealing process effects on AlGaN/GaN HEMT with La_2O_3 gate dielectrics were summarized.

5.3 Results and discussion

Figure 5.2(a) shows gate voltage (V_g) dependent channel current (I_{ds}), I_{ds}-V_g, characteristics of W gated Schottky AlGaN/GaN HEMT and those with La_2O_3 gate dielectrics with drain voltage (V_d) of 50 mV, annealed at 300 ^oC and 500 ^oC. HEMTs with Schottky gate show large leakage current at off-state of V_g=-5V, and do not show large improvement with 500 ^oC annealing. The threshold voltage (V_{th}) stays almost constant around -3.5 V, which is expected from modeling with spontaneous and piezoelectric polarizations. On the other hand, insertion of La_2O_3 reduces the off-state leakage current by two orders of magnitude, and eventually an on/off ratio of 10^5, measured at V_g of 0 and -5 V, is achieved. The sample annealed at 300 ^oC firstly showed negatively shifted I_{ds}-V_g curve, however after annealing at 500 ^oC, the I_{ds}-V_g curve shifted to positive direction, which is higher than that of Schottky samples. This strongly suggesting either reaction between the La_2O_3 and AlGaN layers or creation of negative charges at the interface. The summary of the V_{th} on annealing temperature, shown in Figure 5.2(b), also shows a further monotonic positive shift in V_{th} for the HEMTs with La_2O_3 dielectrics, and the overall positive V_{th} shift by 0.7 V was obtained from 300 ^oC annealed sample to 725 ^oC annealed one. In contrast, the V_{th} of W gated Schottky HEMT stayed around -3.5 V, and when annealed over 550 ^oC a shift toward negative direction was observed. The shift can be understood from generation of positively charged nitrogen vacancies due to

reaction between W layer and AlGaN surface.

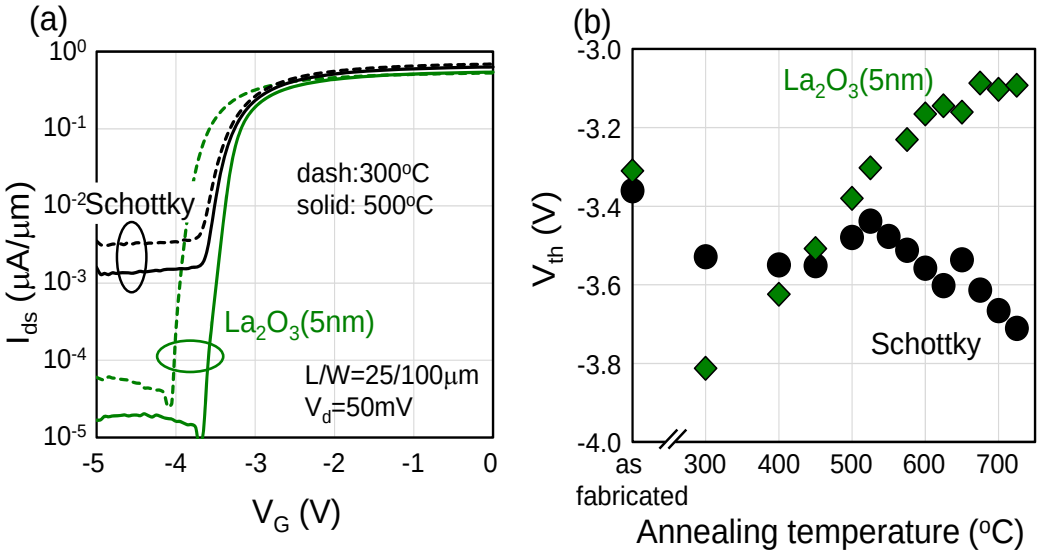

Figure 5.2 (a) I_{ds}-V_g characteristics of Schottky gated AlGaN/GaN HEMT and that with 5-nm-thick La_2O_3 gate dielectrics annealed at 300°C and 500 °C. (b) V_{th} on annealing temperature shows positive shift with La_2O_3 gate dielectrics.

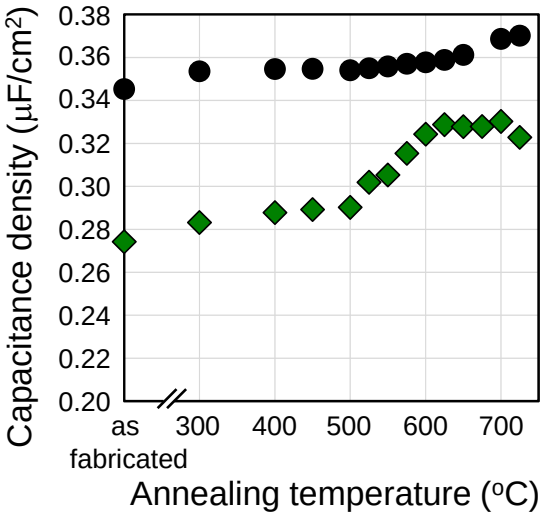

Figure 5.3 Capacitance density of W Schottky gate HEMT and W gated HEMT with La_2O_3 gate dielectrics

Gate-to-channel capacitance (C_{gc}) measurements at a frequency of 100 kHz, shown in Figure 5.3, revealed a constant capacitance density of 0.35 μF/cm^2 with Schottky HEMT up to 500 ºC. On the other hand, W gated HEMT with La_2O_3 gate dielectrics showed a capacitance density of 0.28 μF/cm^2. From calculation of the deposited thickness of La_2O_3 layer, a dielectric constant of 10, which is quite small, can be extracted. After gradual increase in the capacitance, a further steep increase is observed starting from an annealing temperature of 525 ºC, and reached to a maximum value of 0.33 μF/cm^2 at 625 ºC annealing. As the temperature for the La_2O_3 film to crystalize is reported to be 500 ºC, the change in the capacitance might be the increase in the dielectric constant of La_2O_3 film, where a k-value of 27 can be estimated which is quite reasonable for a pure La_2O_3 film [5.5]. From capacitance density measurements, the effective electron mobility can be extracted and its peak values are summarized in Figure 5.4. A higher peak mobility can be obtained with insertion of La_2O_3 gate dielectrics even at as fabricated device, which might be protection of the AlGaN surface from damage induction during sputter deposition of W layer. A higher mobility can be preserved even after annealing, where a severe degradation can be seen with Schottky devices, suggesting creation of charged defects in the AlGaN layer.

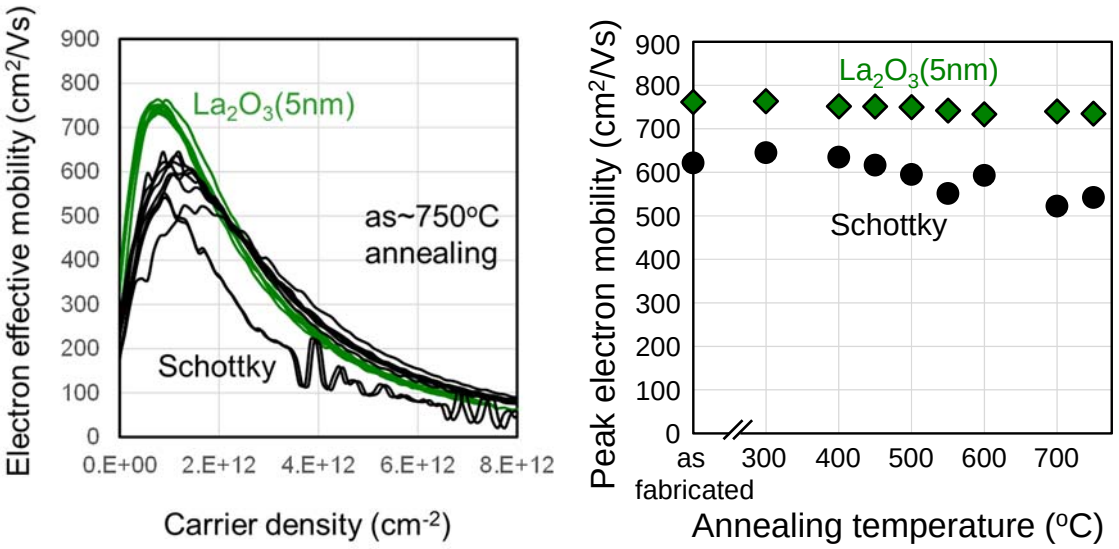

Figure 5.4 Extracted peak electron mobility of the devices.

Gate leakage current density (J_g) on annealing temperature is show in Figure 5.5 (a) and leakage current at forward (V_g=1V) and reverse bias (V_g =-5V) are summarized in Figure 5.5 (b), respectively. Increase in the J_g with higher annealing temperature was observed in both samples, however, with insertion of La_2O_3 gate dielectrics, the J_g was suppressed by one and two orders of magnitudes at forward and reverse bias, respectively. The suppression can allow larger overdrive voltage application to gate electrodes. Note that the conduction of within the leakage current changes with insertion of La_2O_3 layer over annealing 700 °C. As symmetrical current characteristics at low bias region can be seen, the leakage path might be the edge of the gate electrode, rather than the conduction through La_2O_3 films, namely the peripheral or sidewall of the mesa-regions, where La_2O_3 films are in contact with GaN substrates.

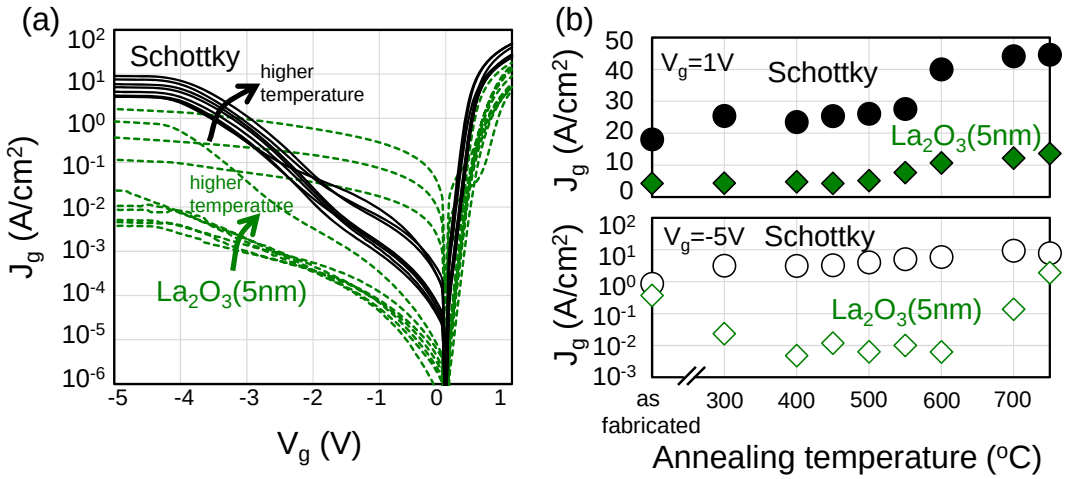

Figure 5.5 (a) J_g characteristics of W Schottky gated HEMT and W/La_2O_3 HEMT on different annealing conditions. (b) Leakage current at forward (V_g=1V) and reverse gate (V_g=-5V) voltage application.

Figure 5.6 shows a positive shift in threshold voltage with different La_2O_3 dielectric thicknesses dependent on annealing temperature. With the increase in La_2O_3 dielectric thickness, the positive shift in V_{th} increases. The bigger shift of the threshold voltage suggests there are reaction between at La_2O_3 and AlGaN layer and create more negative charges at the interface. Figure 5.7 shows capacitance increase along with annealing temperature. Insertion of thicker La_2O_3 dielectric, a greater increase in the capacitance can be observed.

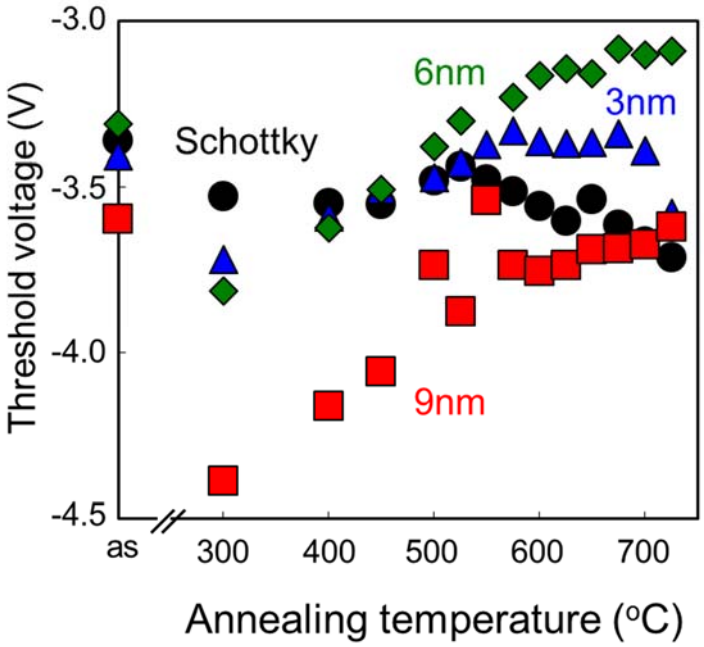

Figure 5.6 Threshold voltage on annealing temperature shows positive shift with different La_2O_3 gate dielectrics

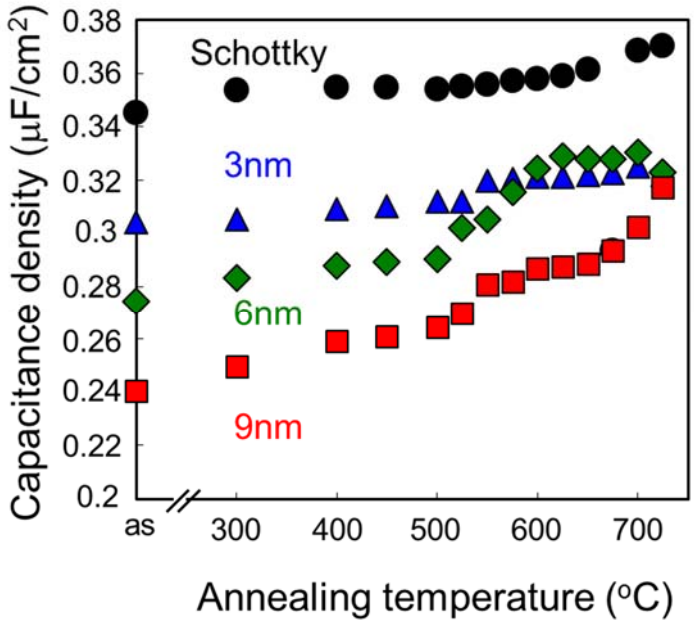

Figure 5.7 Capacitance increase along with annealing temperature

A cross-sectional transmission electron micrograph (TEM), shown in Figure 5.8 (a), shows the presence of a layer with a clear bright contrast between the La_2O_3 and AlGaN layers. The thickness of the interfacial layer is found to be 2 nm. One can also observe lattice image in the La_2O_3 layer with random orientations, suggesting the formation of polycrystalline phase. The samples before and after annealing were analyzed by HX-PES measurements. Al 1*s* spectra and its deconvoluted spectra are shown in Figure 5.5 (b). Here, the components of Al-N bonding states in AlGaN layer are extracted by modeling the depth dependent binding energy shift which reflect the presence of electric filed in the AlGaN layer. As a results, the voltage drop in AlGaN layer (V_{AlGaN}) before and after annealing were extracted to be 1.15 and 0.91 eV, respectively [5.6]. The difference of 0.24 V is consistent with the measured V_{th} difference, shown in Figure 5.2(b). An oxidized state was found even in the sample without annealing, and the intensity increased by 2.5 times after annealing. Therefore, the interface layer with a bright contrast should contain oxidized Al atoms, which was formed by interface reaction between La_2O_3 and AlGaN layers.

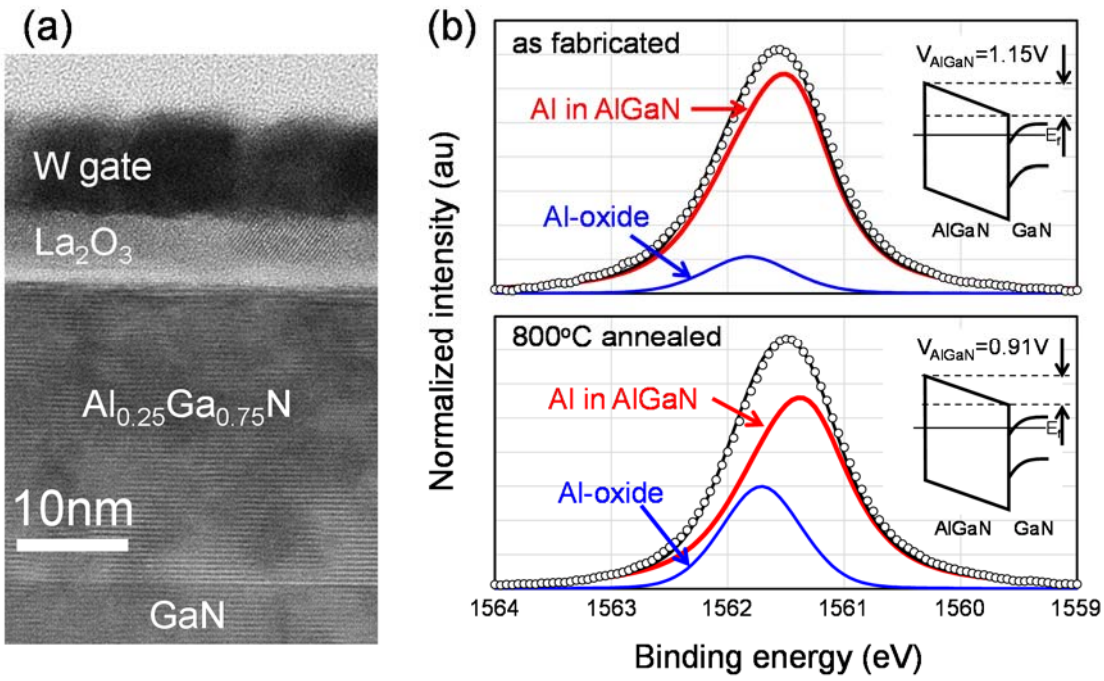

Figure 5.8 (a) Cross-sectional TEM image of the sample with La_2O_3 gate dielectrics, annealed at 800 °C. A clear bright contrast indicates the formation of interface layer between the La_2O_3 layer and AlGaN layer. (b) Al 1s spectra before and after annealing in 800 °C. An increase in oxidized Al component was confirmed.

Considering the capacitance density obtained with the device annealed at 600 °C, the V_{th} value of -3.2 V is far from the theoretical value of -3.8 V. Therefore, it can be considered that a negative charge with an amount of 1.5×10^{13} cm^{-2} can be estimated to present at the interface between the La_2O_3 and the AlGaN layers. The presence of negatively charged interface is a prominent feature of La_2O_3 gate dielectrics on AlGaN layer, where most of the gate dielectrics show positively charged interface. The physical origin of the negative charges is still not clear, however, the formation of interface layer, which is shown later, may be the source of the charges. If one can control and increase

the amount of the negative charges more than 9×10^{13} cm^{-2}, a device with a normally-off characteristic can be obtained, shows in Figure 5.9.

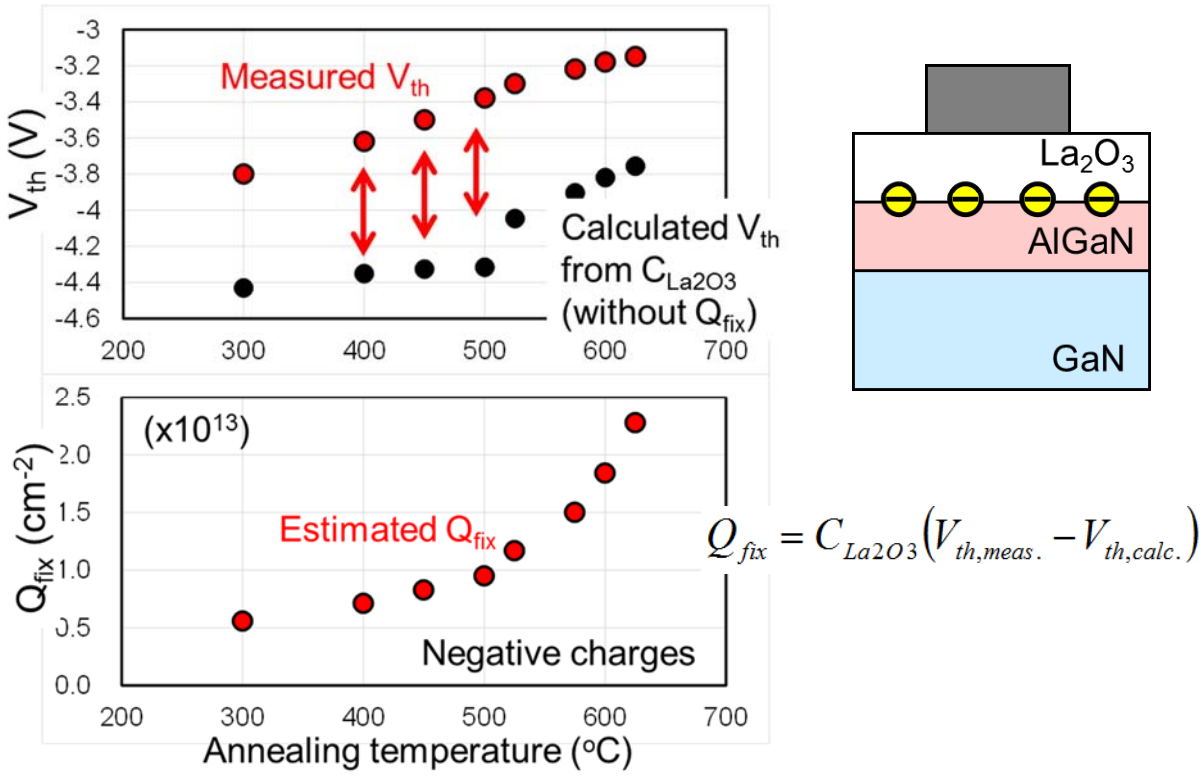

Figure 5.9 Fixed charge estimation at La_2O_3 /AlGaN interface

5.4 Conclusion

The annealing temperature dependent electrical characteristics of La_2O_3 gate dielectrics for W gated AlGaN/GaN HEMT have been characterized. The V_{th} was found to shift to positive direction with higher temperature annealing and exceed the values for W gated Schottky HEMT. The shift can be modeled by the presence of negative charges at the Al oxide-based interface layer between La_2O_3 and AlGaN layers. Moreover, an increase in capacitance with annealing can be the crystallization of the La_2O_3 films and a

k-value of 27 is estimated. With this high k-value and the negative charges, La_2O_3 gate dielectrics have attractive physical properties to relax the trade-off performance in capacitance density and V_{th} for AlGaN/GaN HEMT.

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Chapter 6: Prospect of poly-Si gate with La_2O_3 gate dielectrics

In this chapter, electrical characteristics of p^+-poly-Si gate and SiO_2 gate dielectrics have been investigated. Based on this results, the prospect of poly-Si gate with La_2O_3 gate dielectrics is given. Process design for poly-Si gate with La_2O_3 gate dielectrics is performed.

6.1 Integration of p^+-poly-Si gate and SiO_2 gate dielectrics for AlGaN/GaN HEMT

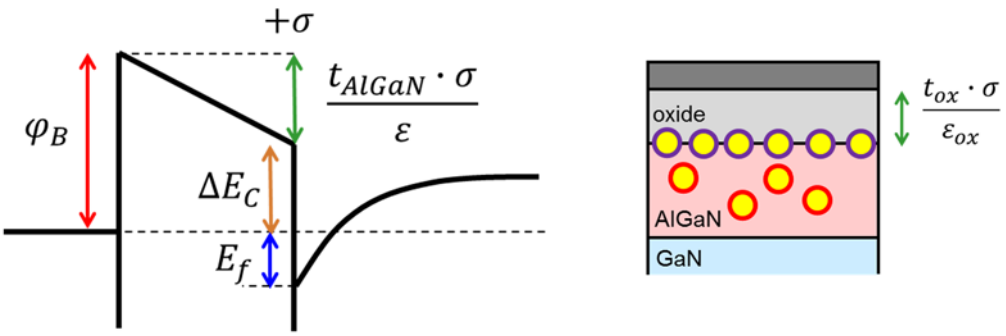
The threshold voltage model in the fluorinated devices for a standard MOSHEMT needed consider oxide thickness, different charge and fluorine effect on device. The threshold voltage for fluorinated MOSHEMT can be expressed as

$$V_{th} = \frac{\phi_B}{q} - \frac{\Delta E_c}{q} + \frac{E_F}{q} - \frac{t_{AlGaN} \cdot \sigma}{\varepsilon_{AlGaN}} - \frac{t_{ox} \cdot \sigma}{\varepsilon_{ox}} - q\int_0^{t_{AlGaN}+t_{ox}} N_F(x)\left(\frac{t_{ox}}{\varepsilon_{ox}} + \frac{x}{\varepsilon_{AlGaN}}\right)dx - \frac{qt_{ox}N_{ox}}{\varepsilon}$$

Eq. (6.1)

where Φ_b is the metal barrier height, ΔE_c is conduction band offset between AlGaN and GaN as shown in Figure 6.1. E_F is Fermi lever at GaN. t is the thickness, ε is the permittivity, and the subscripts ox and AlGaN refer to the oxide and barrier AlGaN layer,

respectively. N_F is fixed charge density in AlGaN layer and Nox is the fixed charge at AlGaN surface. $q\int_0^{t_{AlGaN}+t_{ox}} N_F(x)(\frac{t_{ox}}{\varepsilon_{ox}}+\frac{x}{\varepsilon_{AlGaN}})dx$ is the threshold voltage shift induced by fluorine plasma treatment. It has been reported that the negative fixed charges is the main factor to the threshold voltage shift due to fluorine ions inside AlGaN/GaN structure.



6.1 band gap diagram and fixed charges in AlGaN/GaN MOSHEMT

6.1.1 Introduction

Electrical characteristics of AlGaN/GaN HEMT with poly-Si gate electrode have been investigated. Positive threshold voltage shifts and leakage current suppression are obtained by using poly-Si gate electrode. SiO_2 is the first gate dielectrics used for AlGaN/GaN HEMT. Next, we attempt to insert SiO_2 gate dielectrics to poly-Si gate structure and compare the electrical characteristics of poly-Si gate with and without SiO_2 gate dielectrics.

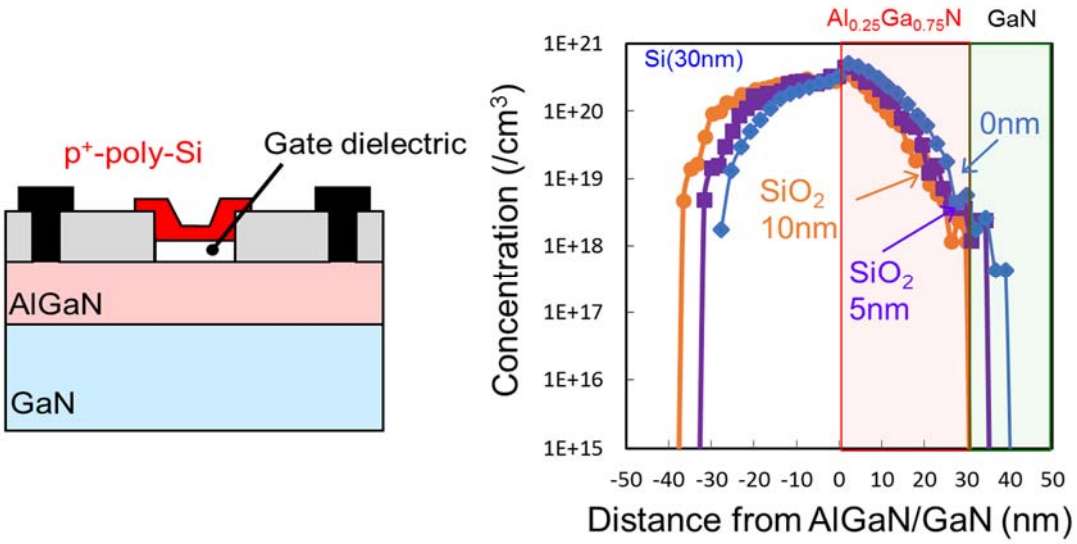


Figure 6.2 Integration of p^+-poly-Si gate and SiO_2 gate dielectrics and depth profile by TRIM simulation

The acceleration voltage for BF_2 ions needs to be redesigned due to ion distribution differs with gate dielectric insertion, shows in Figure 6.2.

6.1.2 Experimental Procedure

Fabrication of Poly-p^+Si gate HEMT with SiO_2 gate dielectric as shows in Figure 6.3, 6.4.

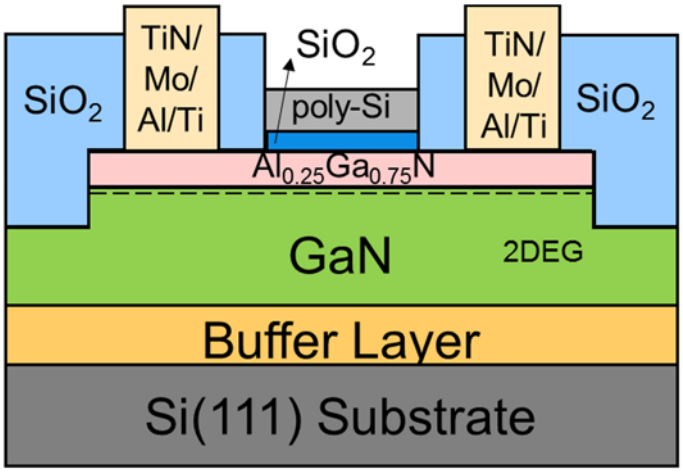


Figure 6.3 Device structure of AlGaN/GaN HEMT with SiO_2 gate dielectrics

$Al_{0.25}GaN_{0.75}$/GaN epitaxially grown on Si (111) wafers were used for fabrication of AlGaN/GaN HEMT. Figure 5.1 and Figure 5.2 shows the device structure and fabrication process, respectively. After cleaning, mesa isolation of the devices formed by reactive ion etching (RIE) with Cl_2-based gas. TiN/Mo/Al/Ti metal deposition for S/D contacts were carried out by RF-sputtering. Ohmic contacts were formed by rapid thermal annealing at 600ºC in N_2 ambient for 1munite. Prior to the TiN/Mo/Al/Ti deposition, N_2 plasma treatment at 5 Torr for 1min were carried out in S/D regions. Then, SiO_2 was deposited with a thickness of 100nm by ALD. After the channel regions were opened, the thickness of 5nm and 10nm SiO_2 films were deposited by ALD as gate dielectrics for AlGaN/GaN HEMT. 30nm Si Schottky gate was deposited by E-beam evaporation at a substrate temperature of 500ºC. Then, BF_2 ions implant to the device, ion implantation energy and dose concentration is 30keV and 4.9×10^{14} (/cm^2), respectively. Activation annealing was carried out immediately for poly-Si formation at 750ºC in N_2 for 2min. Finally, the electrodes were patterned by RIE with Cl_2-based chemistry. Gate length (25 μm) and width (100 μm) of the gate electrode area are used for the measurements.

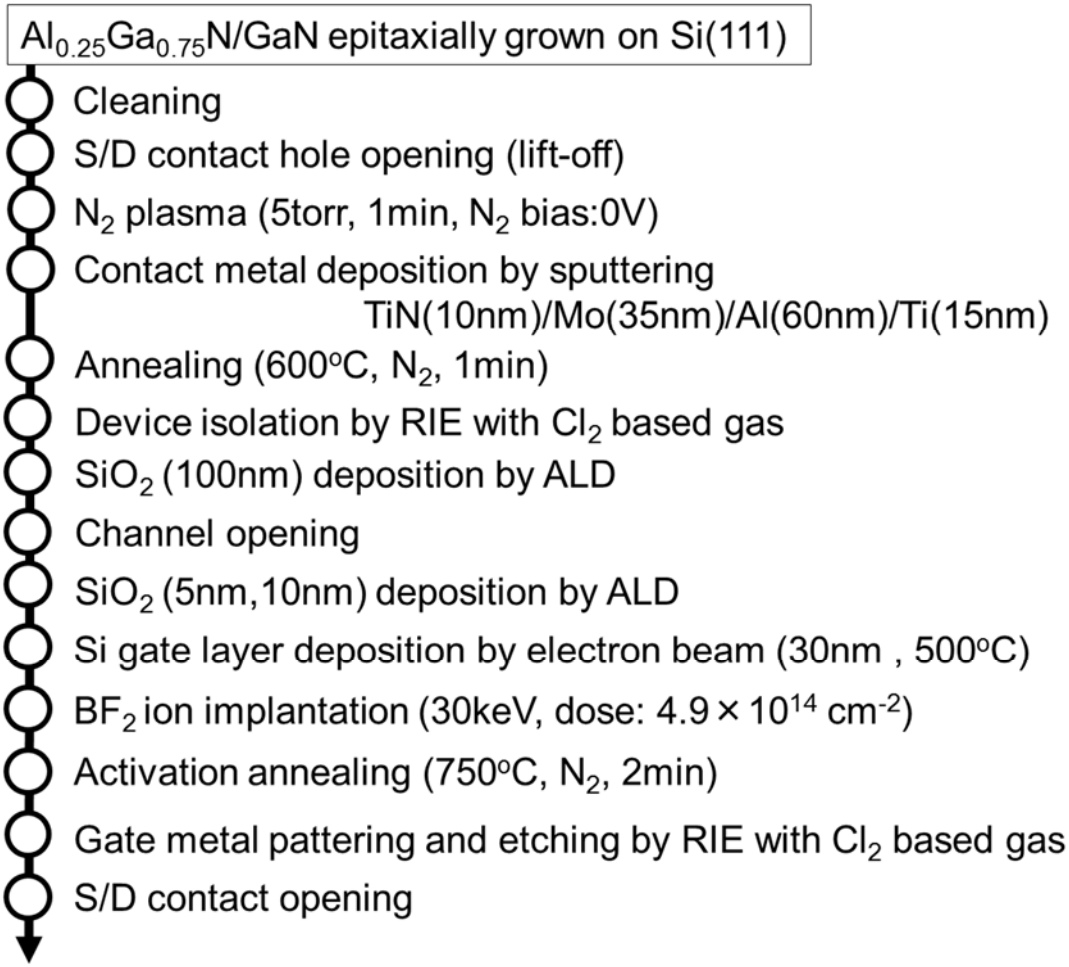


Figure 6.4 Fabrication process of AlGaN/GaN HEMT with SiO_2 gate dielectrics

6.1.3 Results and discussion

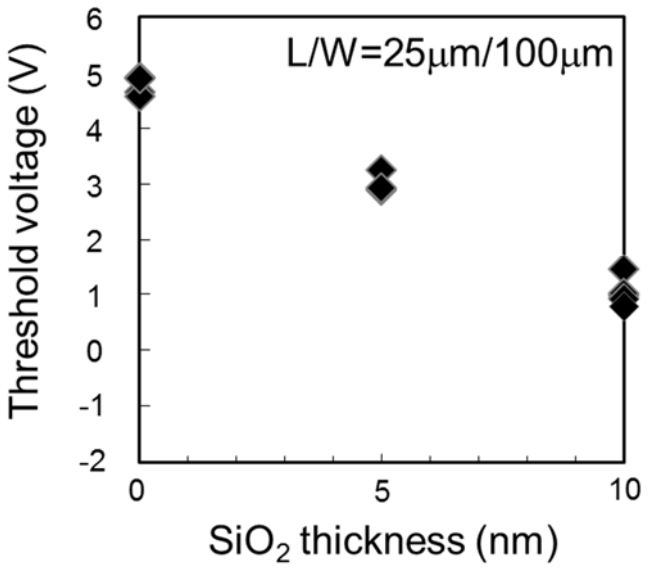


Figure 6.5 Threshold voltage characteristics with variable SiO_2 thickness

The relation of threshold voltage and SiO_2 thickness is shown as Figure 6.5. The threshold voltage shifts to the negative direction with thicker SiO_2 thickness. The negative shifts in threshold voltage suggest that reduced the diffusion depth into the AlGaN layer. The depletion 2DEG reduced in the channel with thicker SiO_2 thickness. The other reason may be fixed charge increased in thicker SiO_2 thickness after annealing process.

Figure 6.6 shows leakage current characteristics of AlGaN/GaN HEMT with SiO_2 gate dielectrics at gate voltage of 1V. The result presents leakage current was suppressed to be about $10^{-6}A/cm^{-2}$ with using SiO_2 gate dielectrics. With increased the thickness of SiO_2 gate dielectrics, Slight reduction in gate leakage current was observed. This might be due to small change in the thickness of SiO_2 gate dielectrics.

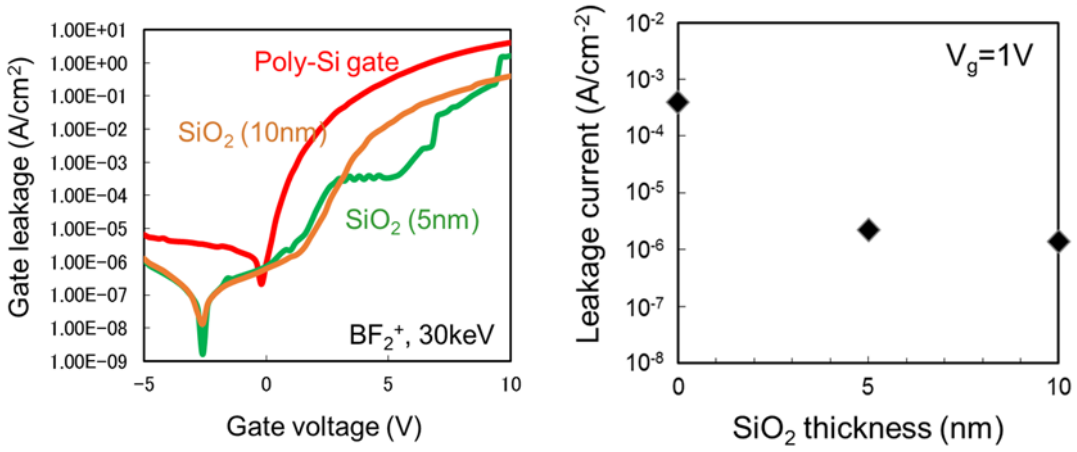


Figure 6.6 Leakage current characteristics with variable SiO_2 thickness

6.2 Redesign of acceleration voltage for p^+-poly-Si/La_2O_3 structure

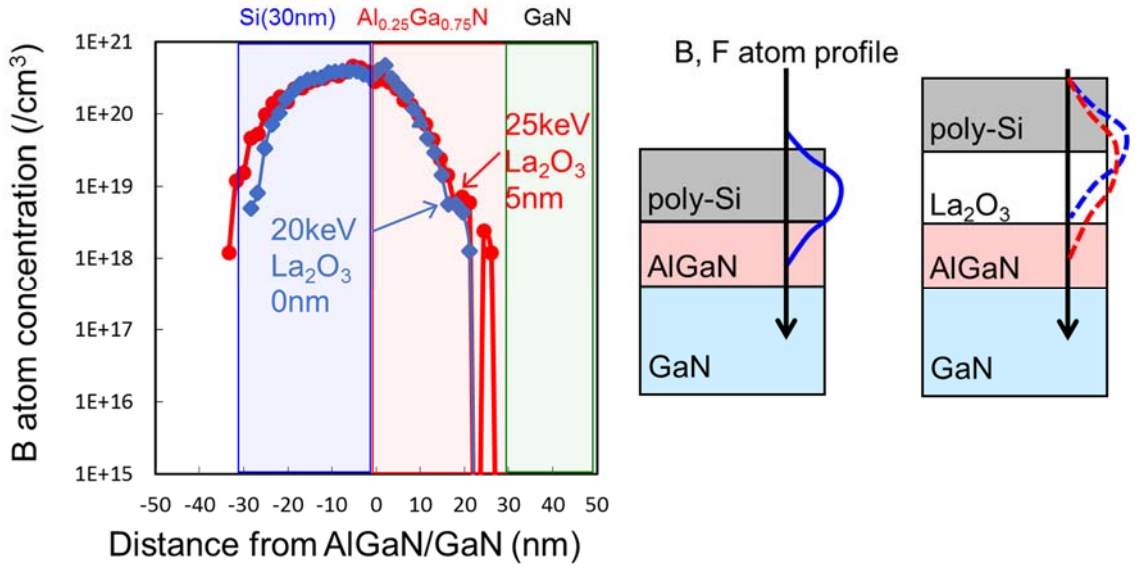


Figure 6.7 Redesign of acceleration voltage (V_{acc})

Insertion of La_2O_3 gate dielectrics between poly-Si and AlGaN layer, in order to obtained same B and F atom profile in the AlGaN layer, acceleration voltage for BF_2 ions needs to be added, as shown in Figure 6.7. Same atom profile in AlGaN can be obtained by adding 5keV in V_{acc} with insertion of 5 nm La_2O_3 gate dielectrics.

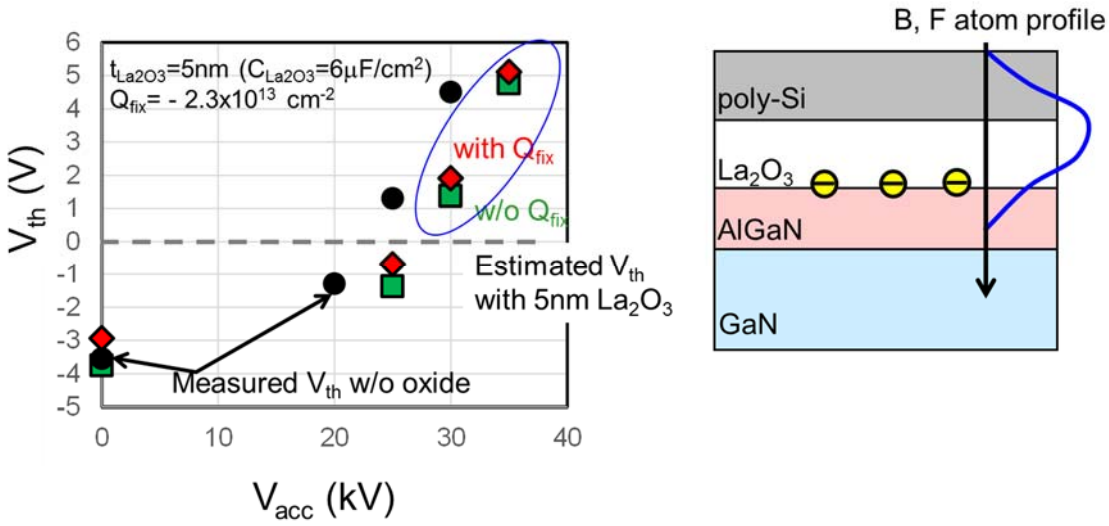


Figure 6.8 V_{th} estimation with p^+-poly-Si/La_2O_3 structure

When insertion of La_2O_3 gate dielectrics, V_{th} shifts to the negative direction. After high annealing process, V_{th} shift to the positive direction due to the present of negative fixed charge at the interface. Integration of p^+-poly-Si gate and La_2O_3 gate dielectrics, normally off characteristics can be expected by adding acceleration voltage of BF_2 ion implantation. It assume negative fixed charge at La_2O_3/AlGaN interface is $2.3\times10^{13}cm^{-2}$, based on experimental value of C_{La2O3} and V_{th} w/o oxide, $V_{th}>0$ (normally off) characteristics with 5-nm-thick La_2O_3 gate dielectrics can be achieve when V_{acc} is over 28keV, as shown in Figure 6.8.

Chapter 7: Conclusion

In this work, we proposed to use poly-Si gate and La_2O_3 gate dielectric to achieve normally-off operation and suppress gate leakage current. The different parts of this study are descried as follows.

A) Poly-Si gate electrode for AlGaN/GaNHEMT

Poly-Si gate electrode formation is achieved by using BF_2 ion implantation process and activation annealing. BF_2 ion implantation to the AlGaN layer can delete 2DEG at the interface of AlGaN layer and GaN layer, which control threshold voltage shift. AlGaN/GaN HEMT transistors with poly-Si gate by different BF_2 ion implantation energies are fabricated. It is found ① Positive threshold voltage has confirmed over 25keV. Normally-off operation have been demonstrated. ② Leakage current was suppressed to be 10^{-4} A/cm^2 at gate voltage of 1V. ③ Stability electrical characteristics were obtained after stress.

B) La_2O_3 gate dielectric for AlGaN/GaN HEMT

Electrical properties with La_2O_3 gate dielectric have been studied. Gate leakage current can be suppress with La_2O_3 gate dielectrics, a k-value of 27 can be estimated. Positive V_{th} shift with high temperature annealing can be explained by the presence of negative charges at the Al oxide-based interface layer between La_2O_3 and AlGaN. Prospect of poly-Si gate with La_2O_3 gate dielectrics

C) Prospect of poly-Si gate with La_2O_3 gate dielectrics.

Electrical characteristics of SiO_2 gate dielectrics with poly-Si gate for AlGaN/GaN

HEMT have been investigated. About 10^{-6} A/cm^2 leakage current at gate voltage of 1V was obtained with SiO_2 gate dielectrics. Based on this results, the prospect of poly-Si gate with La_2O_3 gate dielectrics is given. Process design for poly-Si gate with La_2O_3 gate dielectrics is performed. When insertion of La_2O_3 gate dielectrics, V_{th} shifts to the negative direction. After high annealing process, V_{th} shift to the positive direction due to the present of negative fixed charge at the interface. Integration of p^+-poly-Si gate and La_2O_3 gate dielectrics, normally off characteristics can be expected by adding acceleration voltage of BF_2 ion implantation. It assume negative fixed charge at La_2O_3/AlGaN interface is 2.3×10^{13}cm^{-2}, based on experimental value of C_{La2O3} and V_{th} w/o oxide, $V_{th}>0$ (normally off) characteristics with 5-nm-thick La_2O_3 gate dielectrics can be achieve when V_{acc} is over 28keV.

Appendix A: Ion implantation isolation

Device isolation is an important process for transistor, usually there are two methods for isolation process as shown in Figure A1: mesa etching and ion implantation. Mesa process, isolated insufficiency caused gate leakage in edge region. Planar device process can avoid this problem because of ion implantation process allow isolation and planar area selective doping. Therefore, ion implantation process is proposed.

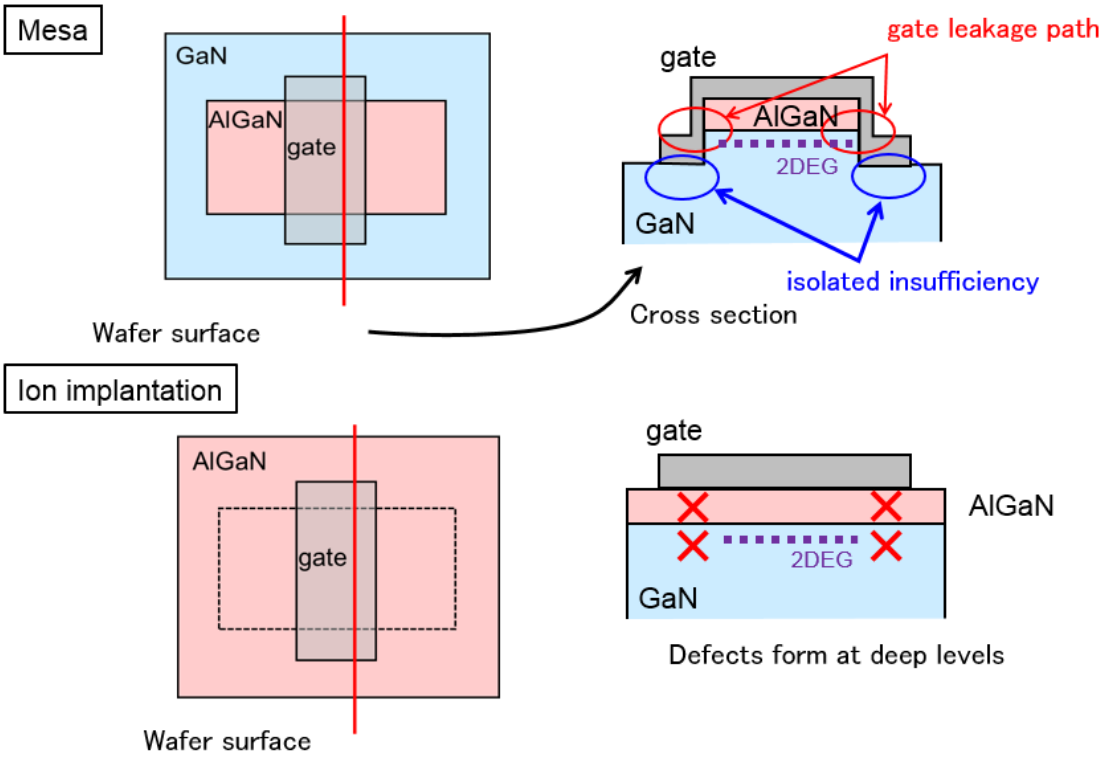


Figure A1 Advantage of ion implantation isolation

Panasonic reported about Fe ion implantation is effective for device isolation. It present detailed analysis and mechanism of thermally stable isolation of GaN device by Fe ion

implantation. Fe forms deep level, resistivity of Fe ion implanted region remains over 1010 W/sq even after annealing at 1200°C.

A simple and reliable process is needed. We attempt to use N_2 plasma treatment for device isolation. The fabrication flow is given as follow:

- Cleaning
- Plasma-TEOS(100nm) deposition
- SiO_2wet etching
- Depletion 2DEG process
- SiO_2 hole opening
- Contact formation: Mo(35nm)/Al(60nm)/Ti(15nm)
- 950°C, 1min in N_2 (Ohmic formation)
- Measurement

Depletion 2DEG process are used in four type processes as follow:

1. Common (control)
2. Oxidation process (800°C, 30min)
3. N_2 plasma (CCP, 300W, 5min)
4. N_2 plasma (CCP, 300W, 5min) +Oxidation process (800°C, 30min)

Results were analyzed by 4 point measurement as shown in Figure 3.5. We respectively obtained 3.8×10^2 Ohm/ sq sheet resistivity on a common device, 1.4×10^5 Ohm/ sq on 800°C oxidation process, 1.6×10^9 Ohm/ sq on N_2 plasma process and 2.3×10^{11} Ohm/ sq on N_2 plasma/oxidation process.

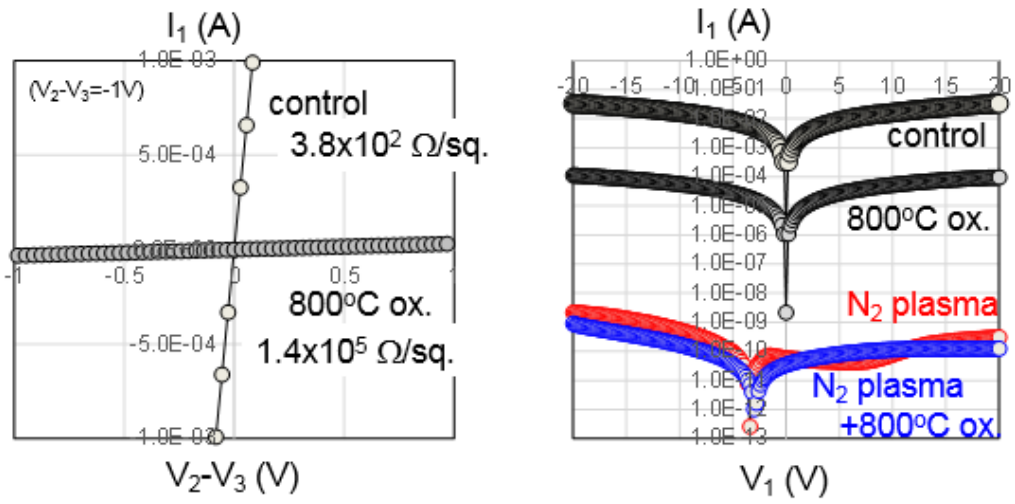


Figure A2 N_2 plasma isolation

Publication and Presentation List

Journals

1. J. Chen, T. Kawanago, H. Wakabayashi, K. Tsutsui, H. Iwai, D. Nohata, H. Nohira, K. Kakushima, "La_2O_3 gate dielectrics for AlGaN/GaN HEMT", Microelectronics Reliability, vol. 60, pp. 16-19 (2016).
2. J. Chen, H. Wakabayashi, K. Tsutsui, H. Iwai, K. Kakushima, "Poly-Si gate electrodes for AlGaN/GaN HEMT with high reliability and low gate leakage current", Microelectronics Reliability, doi:10.1016/j.microrel.2016.05.014 (2016).

Conference publications

1. J. Chen, K. Tsuneishi, K. Kakushima, P. Ahmet, Y. Kataoka, A. Nishiyama, N. Sugii, K. Tsutsui, K. Natori, T. Hattori, H. Iwai, "Thickness Dependent Electrical Characteristics of AlGaN/GaN MOSHEMT with La_2O_3 Gate Dielectrics", ECS Transactions, Vol. 50(3), pp. 353-357 (2012).
2. K. Tsuneishi, J. Chen, K. Kakushima, P. Ahmet, Y. Kataoka, A. Nishiyama, N. Sugii, K. Tsutsui, K. Natori, T. Hattori, H. Iwai, "Ti silicide electrodes low contact resistance for undoped AlGaN/GaN structure", ECS Transactions, Vol. 50(3), pp. 447-450 (2012).

International Conferences

1. J. Chen, K. Tsuneishi, K. Kakushima, P. Ahmet, Y. Kataoka, A. Nishiyama, N. Sugii, K. Tsutsui, K. Natori, T. Hattori, and H. Iwai, "Thickness Dependent Electrical Characteristics of AlGaN/GaN MOSHEMT with La_2O_3 Gate Dielectrics", 222nd Meeting of ECS, Progr#2558, Oct. 10th, 2012, Hawaii, USA.
2. J. Chen, G. Lu, K. Kakushima, P. Ahmet, Y. Kataoka, A. Nishiyama, N. Sugii, K. Tsutsui, K. Natori, T. Hattori, and H. Iwai, "Electrical characteristics of AlGaN/GaN-

HEMT with La-oxide gate dielectrics", IEEE EDS WIMNACT-37, Progr#p31, Feb. 10th, 2013, Tokyo.

3. J. Chen, K. Kakushima, Y. Kataoka, A. Nishiyama, N. Sugii, H. Wakabayashi, K. Tsutsui, K. Natori, H. Iwai, and W. Saito, "Process dependent electrical characteristics of La_2O_3 gate dielectrics on AlGaN/GaN device", IEEE EDS WIMNACT-39, Progr#8, Feb. 7th, 2014, Tokyo.
4. J. Chen, K. Kakushima, T. Kawanago, Y. Kataoka, A. Nishiyama, N. Sugii, H. Wakabayashi, K. Tsutsui, K. Natori and H. Iwai, "Electrical characteristics of AlGaN/GaN devices with poly-Si gate electrode and BF_2 ion implantation", IEEE EDS WIMNACT-45, Progr#4, Feb. 19th, 2015, Tokyo.
5. K. Tsuneishi, J. Chen, K. Kakushima, P. Ahmet, Y. Kataoka, A. Nishiyama, N. Sugii, K. Tsutsui, K. Natori, T. Hatorri, and H. Iwai, "Ti Silicide Electrodes Low Contact Resistance for Undoped AlGaN/GaN Structure", 222nd Meeting of ECS, Progr#2569, Oct. 11th, 2012, Hawaii, USA.
6. K. Tsuneishi, J. Chen, K. Kakushima, P. Ahmet, Y. Kataoka, A. Nishiyama, N. Sugii, K. Tsutsui, K. Natori, T. Hattori, and H. Iwai, "A Robust Ohmic Contact Process for AlGaN/GaN using Ti-silicide electrodes", IEEE EDS WIMNACT-37, Progr#p32, Feb. 10th, 2013, Tokyo.

Domestic Conferences

1. J. Chen, K. Tsuneishi, K. Kakushima, P. Ahmet, Y. Kataoka, A. Nishiyama, N. Sugii, K. Tsutsui, K. Natori, T. Hattori, and H. Iwai, "Electrical characteristics of AlGaN/GaN-HEMT using HfO_2 and La_2O_3 as gate dielectrics", The 59th JSAP Spring Meeting, the Japan Society of Applied Physics, Waseda University, March 18, 2012.No. 18a-GP7-1.

2. J. Chen, K. Tsuneishi, K. Kakushima, P. Ahmet, Y. Kataoka, A. Nishiyama, N. Sugii, K. Tsutsui, K. Natori, T. Hattori, and H. Iwai, "Thickness dependent electrical characteristics of AlGaN/GaN-HEMT with La_2O_3 as gate dielectrics", The 73th JSAP Autumn Meeting, the Japan society of Applied Physics, Ehime University/ Matsuyama University, September 12, 2012. No. 11a-PA5-14
3. J. Chen, K. Kakushima, Y. Kataoka, A. Nishiyama, N. Sugii, H. Wakabayashi, K. Tsutsui, K. Natori, H. Iwai, and W. Saito, "Process dependent electrical characteristics of La_2O_3 gate dielectrics on AlGaN/GaN device", The 61th JSAP Spring Meeting, the Japan society of Applied Physics, Aoyama Gakuin University, March 17, 2014. No.18p-PG3-9.
4. K. Tsuneishi, J. Chen, K. Kakushima, P. Ahmet, Y. Kataoka, A. Nishiyama, N. Sugii, K. Tsutsui, K. Natori, T. Hattori, and H. Iwai, "Current-voltage characteristics of stacked $NiSi_2$ on AlGaN/GaN and the effect of impurity incorporation", The 59th JSAP Spring Meeting, the Japan society of Applied Physics, Waseda University, March 18, 2012.No. 18a-GP7-2.
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6. G. Lu, J. Chen, T. Kawanago, K. Kakushima, P. Ahmet, Y. Kataoka, A. Nishiyama, N. Sugii, K. Tsutsui, K. Natori, T. Hattori, and H. Iwai, "Electrical characteristics of AlGaN/GaN devices with La_2O_3 gate dielectrics on annealing temperature", The 60th JSAP Spring Meeting, the Japan society of Applied Physics, Kanagawa Institute of

Technology University, March 28, 2013.No. 28p-GP11-7.

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