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Title(English)	Study of VCO-Based Analog-to-Digital Converters in Advanced CMOS Technology
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THESIS OUTLINE

専攻： Department of	Physical Electronics	専攻	申請学位（専攻分野）： Academic Degree Requested	博士 Doctor of	（Philosophy）
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Thesis Outline

The research subject of this thesis is VCO-based ADC. VCO-based ADC performs the A/D conversion in time domain by employing almost all digital circuits. Therefore, it is also referred to as the time-domain ADC. It gains popularity recently because of the excellent compatibility with CMOS technology scaling. On the other hand, it is well-known that SAR ADC is the most scalable conventional ADC. The research objectives of this thesis are: (1) finding the applications where VCO-based ADC may beat SAR ADC and (2) proposing circuit techniques to help VCO-based ADC beat SAR ADC in some aspects, such as SNDR, voltage sensitivity, and etc.

Chapter 1 introduces the research background of this thesis. Different from most conventional ADCs, SAR ADC benefits from CMOS scaling, thanks to its highly digitalized architecture. It has become the mainstream ADC in the few years. Recently, time-domain ADC emerges as another option in advanced CMOS. It quantizes the input time signal with the voltage-controlled inverter-based delay line or VCO. The time resolution, area and power consumption could be improved as CMOS scaling. Superior to the delay-line time-domain ADC, VCO-based ADC can achieve much large input range with 1st-order noise shaping. That's why it is chosen as the research subject of this thesis. So far, no previous work has systematically compared the pros and cons of these two scalable ADCs. That becomes the motivation of this thesis.

In Chapter 2, the state-of-art SAR ADCs are firstly overviewed. It shows that SAR ADCs are difficult to achieve high SNDR (>70 dB). Next, the reasons are analyzed. Also, several popular SNDR improvement techniques are introduced. A 12-bit, 50 MS/s SAR ADC prototype with 4 SNDR improvement techniques is fabricated in a 65 nm CMOS process. The measurement results reveal that SAR ADC cannot achieve high SNDR without the high-quality conditioning circuits (e.g. the low-impedance reference generator). Chapter 2 points the possible research direction for VCO-based ADCs. The higher SNDR could be the major advantage of VCO-based ADCs.

VCO-based ADCs have their own limitations to achieve high SNDR, which must be overcome to surpass SAR ADCs. These limitations are analyzed in Chapter 3. Firstly, the quantization noise is analyzed. After that, the other non-ideal effects are investigated. In detail, the phase noise of VCO dominates the in-band noise floor. The nonlinear voltage-to-frequency (V-to-F) tuning gain of VCO (K_{vco}) brings the severe distortion, which results in a poor dynamic range. Finally, a typical design example of VCO-based ADC is simulated. The simulation results are used to verify the theoretical

analysis. It proves that the K_{vco} nonlinearity must be suppressed or calibrated to achieve high SNDR.

In Chapter 4, the K_{vco} linearization techniques are firstly overviewed. It shows that no previous work achieves low power (<1 mW) and high SNDR (>70 dB) simultaneously. Motivated by this status quo, a SAR-VCO 1-1 MASH ADC is proposed to achieve high SNDR by 2nd-order noise shaping. A noise-shaping SAR ADC eliminates the power-hungry Op-amp in the first stage. A dynamic amplifier increases the SNR with superior power efficiency. The second-stage VCO-based ADC only quantize the small-amplitude and input-independent residue, which relaxes the VCO linearity requirement significantly. Moreover, a foreground calibration is proposed to suppress the inter-stage gain error. A prototype ADC is designed in a 65 nm CMOS to verify the proposed ADC architecture. The transistor-level simulation results show that 75.7 dB SNDR is achieved over 5 MHz bandwidth at 60 MS/s. The power consumption is 748.9 μW under 1.0 V supply, which results in a FoM of 14.9 fJ/conversion-step. These results prove that VCO-based ADCs have potential to beat SAR ADCs in terms of SNDR.

As introduced in Chapter 5, some sensors require very high voltage sensitivity and excellent DNL, rather than high ADC linearity. Intuitively, the nonlinear VCO-based ADCs are perfectly suitable to these applications, as long as it can achieve high voltage sensitivity. A time-interpolation technique, 4-Clock-edge-Shifter (4CKES), is proposed to realize the sub-gate time resolution and thus satisfy this very need. In order to verify the proposed technique, a prototype has been developed in a 65 nm CMOS. The ADC prototype consumes a small area of 0.016 mm^2, and achieves a voltage resolution of 82.7 μV/LSB at 10 MS/s or 1.96 μV/LSB at 200 kS/s within a narrow input range of 0.1 V merely under 0.6 V supply. What's more, the 1st-order noise shaping characteristic of VCO-based ADC significantly simplifies the sensor pre-conditioning circuits. Aforementioned, VCO-based ADCs are capable to beat SAR ADCs in terms of voltage sensitivity for the low-voltage sensor application.

In Chapter 6, the conclusion of this research is drawn. SAR ADCs have advantages in those low-power applications. VCO-based ADCs are better in terms of SNDR and voltage sensitivity. The development prospects of VCO-based ADC and the future works related to this research are also discussed. The high-order CT delta-sigma ADC with VCO quantizer and open-loop amplifier-based integrator is a promising research direction.