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著者(和文)	SASONGKO FIRMAN
Author(English)	Firman Sasongko
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Study of Modular Multilevel Double-Star Chopper-Cells Converters for High-Power Front-to-Front Applications

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Supervisor : Prof. Hirofumi Akagi

By
Firman Sasongko

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Chapter 1

Introduction

1.1 Background

Wind energy is one of the most promising candidates for future decentralized renewable-energy-based power generation [1]–[5]. In particular, offshore wind reserves an enormous potential for future large-scale sustainable energy resources [6]–[11]. Fig. 1.1 shows the total installed capacity of offshore wind farms worldwide. The installed capacity has been increasing since the last decade, and has reached to more than 10 GW in 2015. Furthermore, many ongoing offshore wind farm projects are expected to increase the total installation to more than 52 GW, while annual installations are expected to rise to more than 7 GW by 2022 [13].

Fig. 1.2 shows the installed capacity of offshore wind farms by country, in which the United Kingdom is currently on the lead in this sector. Although most of the offshore wind farms today are located in European seas, many countries worldwide have planned to install more offshore wind farms within the next decades. Currently, as the largest contributor in Asian countries, China has installed large offshore wind farms, and has planned to install many more in the near future. Meanwhile, most of the offshore wind farm activities in Japan are still in early concepts [7], or demonstration projects, such as the *Fukushima Floating Offshore Wind Farm Demonstration Project* (FORWARD) [14].

Offshore wind has several favorable characteristics compared to onshore wind, for instance, higher wind speed, less turbulence, and large areas availability, thus leading to higher energy yield and capacity factor. Concurrently, wind turbine sizes have been increasingly developed and optimized for offshore environment in the last decade [15]–

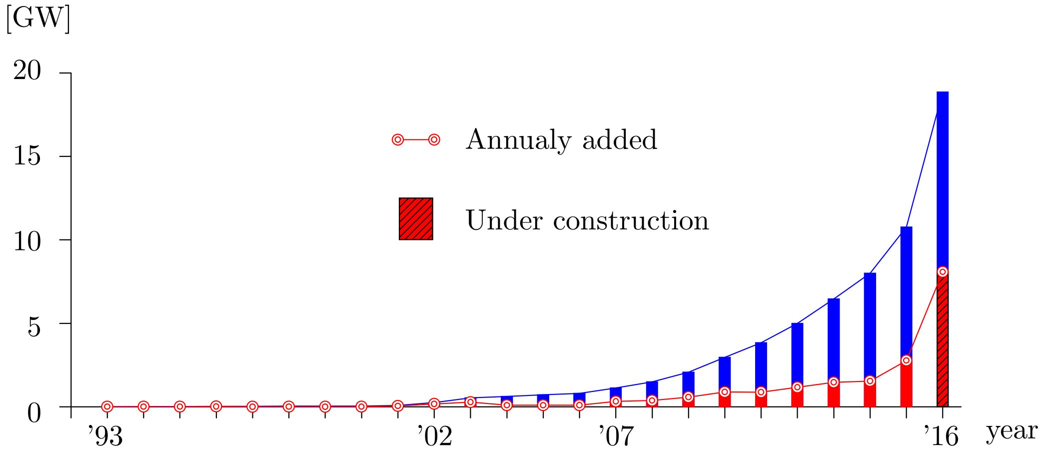


Fig. 1.1: Global total installed capacity of offshore wind farms in 2016 [12].

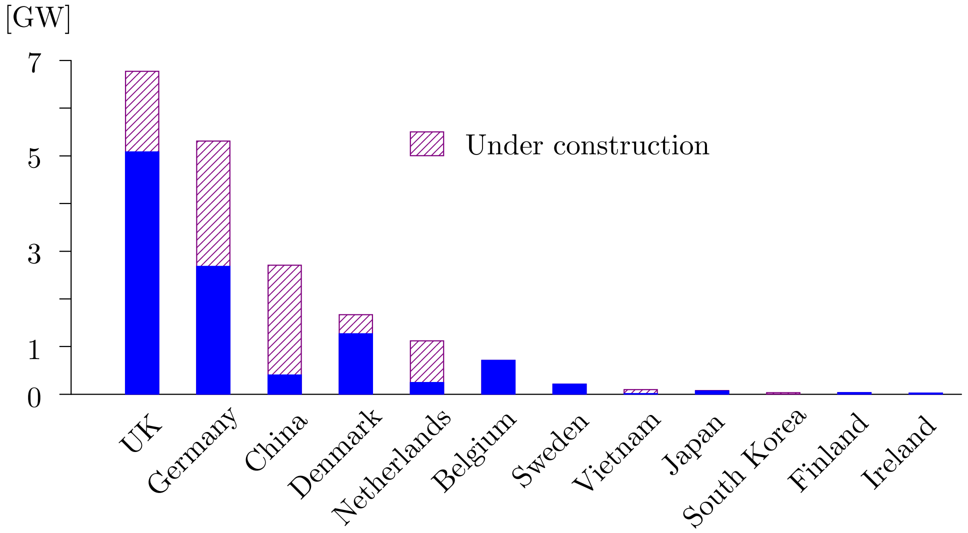


Fig. 1.2: Total installed capacity of offshore wind farms in 2016 by country [12].

[21]. Moreover, many problems associated with installation of onshore wind farms, such as acoustic noises, visual impacts, and land conflicts, are less relevant to offshore wind farm projects.

Recently, a substantial shift towards more large offshore wind farms has been made [15],[16]. Future offshore wind farms are likely to be farther away from shore to increase the size and to reduce visual impacts. A large offshore wind farm can be located more than 100 km away from shore, which requires long transmission cables from the inland grid network. Moreover, the technical requirements including the wind turbines and their foundations, the transmission distance and its capacity, and also the collection layout and grid interconnection should be designed to suit far offshore conditions [21]–[28].

One of the obstacles in far offshore locations is the water depth that can be more than 50 m, rendering the currently used foundations inapplicable. The deep water issue is not always associated with offshore locations that are far from coastlines. For example, nearly all of Japan's offshore wind resources are in deep water, whereas 61% of the US offshore wind resources are in water depths of more than 100 m [8], [9]. This challenge can be overcome by using a foundation that can float on water surface. There are several prototypes of floating wind turbines that have been developed by many countries. Japan has introduced a floating wind turbine with the rated power of 7 MW [14], which is currently the largest of its kind. Floating wind turbines can unlock the promising deep offshore potential [11], and enable remote wind farms far from coastline.

1.1.1 Existing Offshore Wind Farms

Most of existing offshore wind farms to date are less than 600 MW in capacity, and located less than 50 km from shore with the average water depth less than 50 m. Fig. 1.3 shows general configuration of an offshore wind farm. Depending on its size, an offshore wind farm may contain a large number of wind turbines spread over an area of tens of square kilometers. The wind turbines are usually connected in a ring or a radial/star configuration as shown in Fig. 1.3. The commonly used offshore wind turbine foundations are monopile, gravity-based, tripod, and jacket types [10], [11], [15], [16]. The power from the wind turbines are collected at the substation on an offshore platform by using medium-voltage ac interconnection before sending it to an inland grid through a high-voltage alternating current (HVAC) transmission system. The platform may contain compensation reactors, standby diesel generator (DG) sets, and grounding transformers to support the operation of the wind farm.

Fig.1.4 shows the most commonly used offshore wind turbine-generator systems in multi-megawatt class: the doubly-fed induction generator (DFIG) with partial-scale converters, the squirrel-cage induction generator (SCIG), synchronous generator (SG), or the direct-drive permanent magnet synchronous generator (PMSG) with full-scale converters

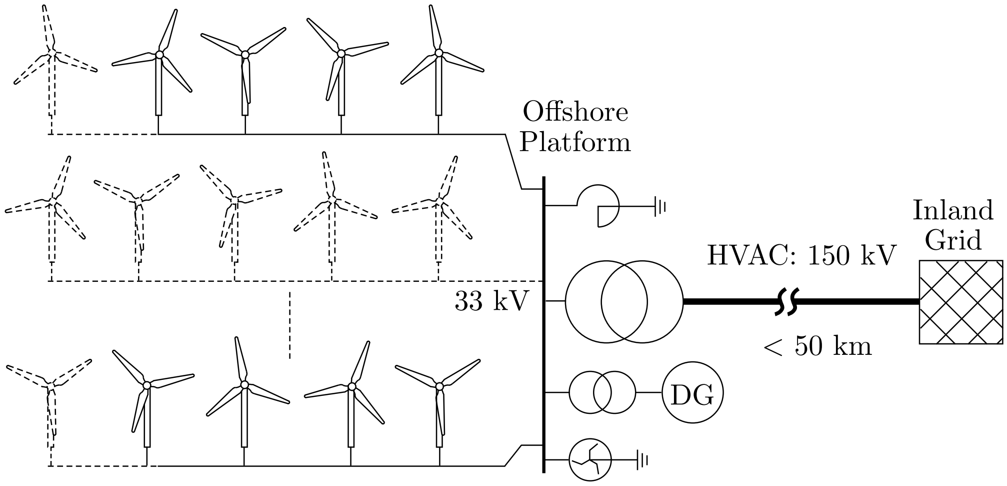
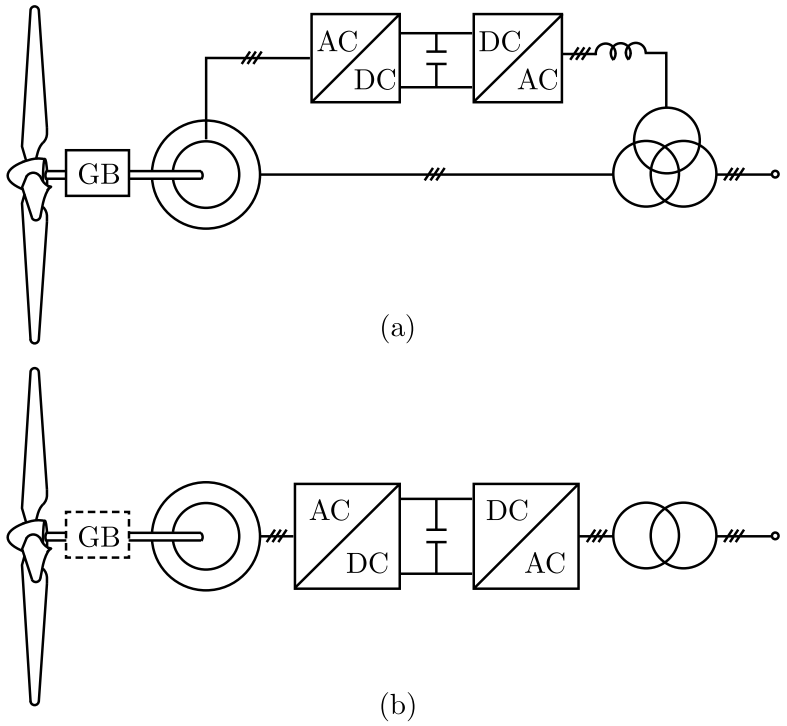


Fig. 1.3: Existing offshore wind farm configuration in general.

(FSCs) [16]–[21]. Currently, the DFIG system has a large market share for wind farm power generation. However, it may not be suitable for future high-power offshore application because of the necessity to perform regular maintenances on the gearbox (GB), slip rings and brushes. On the other hand, the direct-drive multi-pole PMSG offers better reliability and noise reduction since no slip rings and gearbox are used [29], thus is believed to be suitable for future multi-megawatt offshore generators [18]–[21]. However, although the multi-pole PMSG produces less losses and has ride-through capability, it has larger size and weight compared to the DFIG system. A good compromise between size and reliability may be achieved by using a single-stage gearbox with PMSG that enables the generator to operate at medium-speed operation [19], [21].

In multi-megawatt applications, the neutral point clamped (NPC) converter is the most adopted topology used in the full-scale converters because of its good performance to extract maximum power from wind, and to comply with stringent grid requirements [19]–[21]. For offshore applications, in which the power converters should be highly reliable and require less maintenance, the PMSG system equipped with a multi-pulse diode rectifier may become another better alternative [30]–[34]. However, the diode rectifier produces a higher harmonic distortion on the generator side leading to increased generator losses and torque pulsations. Nevertheless, multi-pulse diode rectifiers have higher efficiency and reliability, and lower cost compared to voltage-source converter



(a)

(b)

Fig. 1.4: Offshore wind turbine-generator systems. (a) DFIG with partial-scale converters. (b) SCIG, SG, or direct-drive PMSG with full-scale converters.

(VSC)-based rectifiers.

1.1.2 Offshore Wind Farm Transmission System

In the near future, offshore wind farms are most likely larger in size and farther from coastline. Fig. 1.5 shows offshore wind farm projects in the North Sea. The current largest offshore wind farm in the world is the London Array that has a capacity of 630 MW (175 × 3.6-MW wind turbines). The wind farm is located more than 20 km from the coastline, and it has been operating since 2013. As a comparison, the Teesside A wind farm (Dogger Bank project), which has been through the planning process, will be having a capacity of 1200 MW using 120–200 × 6–10-MW wind turbines. This offshore wind farm will be located at approximately 200 km away from the coastline, which is about ten times than the location of the London Array. Moreover, the Dogger Bank project consists of four offshore wind farms with the total capacity of 4800 MW.

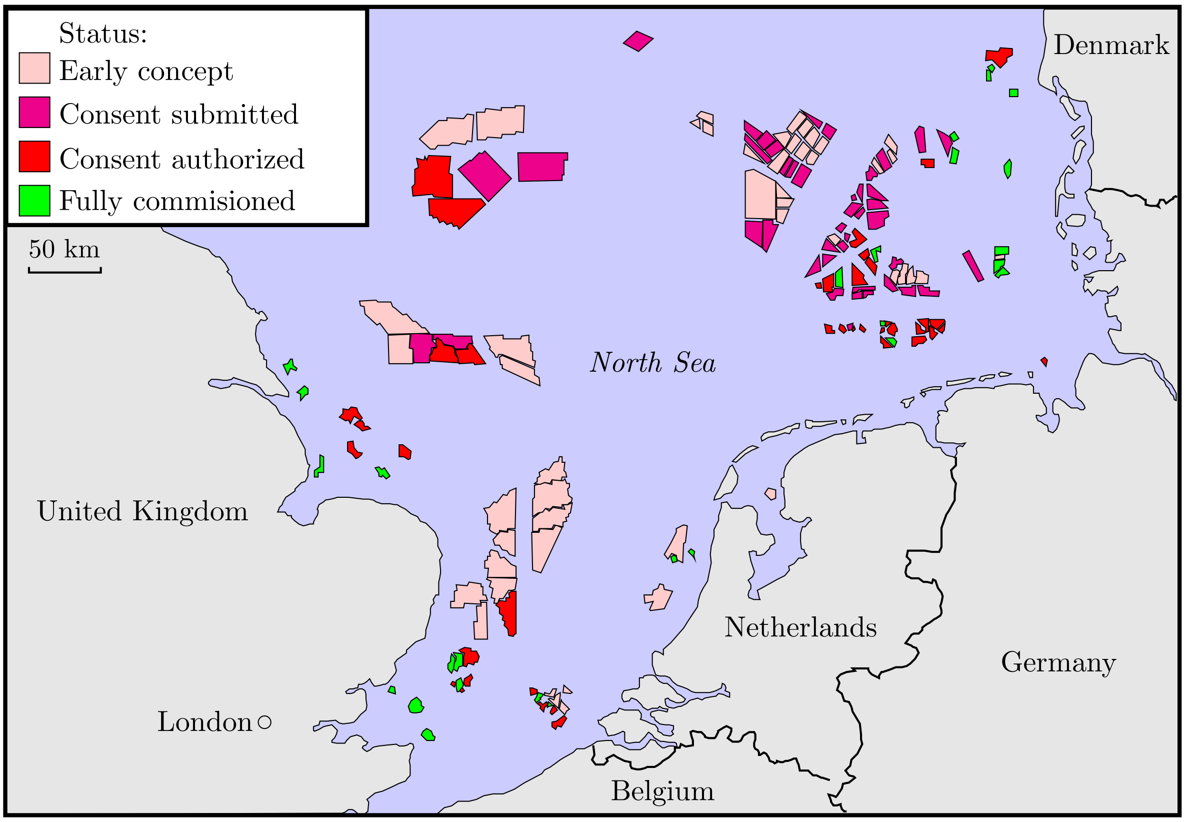


Fig. 1.5: Offshore wind farms in the North Sea [12].

The existing wind farm transmission systems to date are dominated by HVAC systems. However, the upper limits of transmission voltage and distance are restricted because of the large charging current associated with submarine ac cables. Therefore, to get the electric power onshore without major losses, the high-voltage direct current (HVDC) transmission system is likely to be employed for future large-scale offshore wind farms that are relatively far away from the coastlines [22]–[28]. Many research opportunities are wide open to obtain a reliable, effective, and efficient mean to collect and transmit the power from large offshore wind farms to the main grids in the future.

1.2 Research Objectives

The main objective of the research contained in this dissertation is on the investigation of practical feasibility of a high-power front-to-front (FTF) system based on modular multilevel double-star chopper-cells (DSCC) converters for dc power collection and transmission systems. The research methods include conceptual design, mathematical and numerical analyses, as well as experimental and simulated implementations. Three distinctive objectives can be divided as follows:

■ **Performance and practicability verification of the FTF system through experimental implementation.** The aim of the research is to obtain experimentally the operating performance of the FTF system under several conditions. The research also aims at the determination on the appropriate power flow control and the frequency on the ac-link terminals of the FTF system.

■ **Performance and reliability verification of a dc power collection based on the FTF system using multiple DSCC converters.** The FTF system is intended for a medium-/high-voltage, high-power, bidirectional, isolated dc power collection and transmission system. Verification of the system performance and reliability for dc power collection under dynamic and fault conditions will be the aim of the research. It also aims at determining the fault current and the appropriate protection control.

■ **Investigation of a high-power DSCC converter using the phase-shifted-carrier pulsewidth modulation at low-switching-frequency operation.** The research focuses on the determination of constraints in the phase-shifted-carrier pulsewidth modulation (PSC-PWM) method used in the DSCC converter at low carrier-frequency ratios with respect to the ac grid frequency. From the obtained results, the research aims at proposing a modification to the PSC-PWM method to enable low-switching-frequency operation of the DSCC converter.

1.3 Dissertation Outline

This dissertation contains seven chapters, and it is organized as follows:

■ **Chapter 1** is the current chapter that provides an introduction and background on the increasing trend of the offshore wind farms. The necessity of using more efficient and effective power collection and transmission system is hinted as the motivation in this research. This chapter also clarifies the research objectives, and explains the content of each chapter in this dissertation.

■ **Chapter 2** reviews several options on power collection layouts of large offshore wind farms. Particular high-power dc-dc converter topologies for future dc power collections of offshore wind farms are discussed. Finally, a brief review on the current trend of modular multilevel converters is also provided along with their modulation methods.

■ **Chapter 3** discusses the circuit configuration and operating principles of the DSCC converter. Analytical discussion on the switching function of a chopper-cell voltage and the harmonic spectrum of the capacitor voltage is discussed in this chapter. This chapter also discusses the power-flow and the capacitor balancing controls.

■ **Chapter 4** discusses an experimental verification of an FTF system consisting of two DSCC converters. A downscaled FTF system rated at 10 kW and 400 Vdc is designed, constructed, and tested to verify its operation and control under steady and transient conditions with medium frequency operation. It consists of two three-phase DSCC converters with 16 cells per leg. A control strategy for controlling the power flow between the two converters is presented as well in this chapter.

■ **Chapter 5** discusses a dc power collection application based on the FTF system. The flexibility and scalability of the FTF system for dc power collection are explained. A simulation system of an FTF-based dc power collection rated at 10 MW and 13.2 kVdc is designed and utilized to verify its performance and reliability. Later in this chapter, the fault-handling capability, the fault current determination, and the protection strategy are presented. Simulated results for transient and fault operations are provided to verify the performance of the proposed dc power collection.

■ **Chapter 6** presents a new carrier-based PWM method based on a modified PSC-PWM. Analytical and numerical approaches are used to determine the constraints in the PSC-PWM associated with low carrier-frequency ratios with respect to the ac grid frequency. Basic principles of the new phase-shifted rotating-carrier pulsewidth modulation (PSRC-PWM) are explained, and rigorous mathematical analyses are performed to obtain the voltage harmonic spectra of the arm-side terminals and the capacitor in a chopper cell. This chapter also discusses the optimal carrier frequency of the PSRC-PWM when the carrier frequency goes below double the ac grid frequency. A simulation system of a three-phase grid-connected DSCC converter rated at 200 MW, 100 kV, and 50 Hz with 64 cells per leg is designed to verify the effectiveness of the proposed modulation method.

■ **Chapter 7** provides the conclusions, and points out the contributions of this dissertation. Future research to improve the FTF system based on DSCC converters are also provided in this chapter.

Chapter 2

Literature Review

2.1 Introduction

This chapter reviews several literatures related to high-power dc-dc converters for dc power collection and transmission. High voltage dc transmission (HVDC) becomes necessary when a long cable transmission is used to interconnect a large power generation to the main grid, such as the interconnection of large offshore wind farms to inland grids. This chapter provides several configuration of power collection for offshore wind farms. Several high-power converter topologies are also provided. Finally, this chapter gives an overview of the modulation methods used for the modular multilevel double-star chopper-cells (DSCC) converter in high-power applications.

2.2 DC Power Collection and Transmission for Large Offshore Wind Farms

Power collection and transmission system based on dc grids could be an alternative solution for future sustainable power generations [22]–[24], [35]–[41]. DC power system offers higher reliability and flexibility than the conventional ac power system. The transmissible power of dc system is not limited by the transmission length as in ac power system. Some of the electrical energy transmitted would be lost in the form of reactive power when a long distance alternating current cable is used. On the contrary, the high-voltage direct current (HVDC) transmission technology significantly reduces transmission losses, and may be the only viable solution for economical and low-loss power

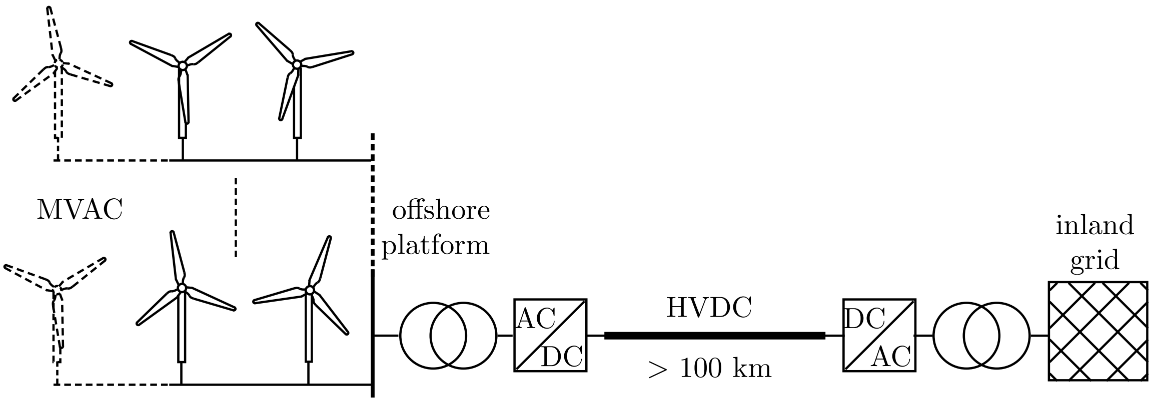


Fig. 2.1: Offshore wind farm power collection: an ac-dc layout.

transmission through cable over distances of more than 80 km.

Fig. 2.1 shows an interconnection of an offshore wind farm to an inland grid using HVDC converters. This configuration uses an ac-dc layout, in which the power from the wind turbines are collected through a medium voltage ac network, and then converted to dc at the wind-farm-end HVDC converter before sending it trough HVDC transmission system over long distance. The wind turbines can use the current trend of generator-converter sets, such as the DFIG or the direct-drive PMSG with full-scale converters as discussed in Chapter 1. Note that all the voltage, phase, and frequency of the wind turbine array should be synchronized to the medium ac network to transfer the power properly.

In order to realize dc power transmissions, medium- and high-voltage dc-dc converters are required. Several technical configurations have been used in many HVDC projects: the classical line-commutated-converter (LCC), two-level voltage-source converters (VSCs), and the modular multilevel converter (MMC) [42]–[49]. Since the space requirement is critical in an offshore installation, the LCC-based HVDC is unfavorable because it requires heavy and bulky auxiliary filters. On the other hand, the VSC-based HVDC requires fewer auxiliary filters, and offers attractive advantages such as fast independent control of active and reactive power, black-start capability, and reactive power support during grid faults. Although the current VSC-HVDC system might suffer from a higher converter cost and losses, the VSC-HVDC may be the preferred solution as the

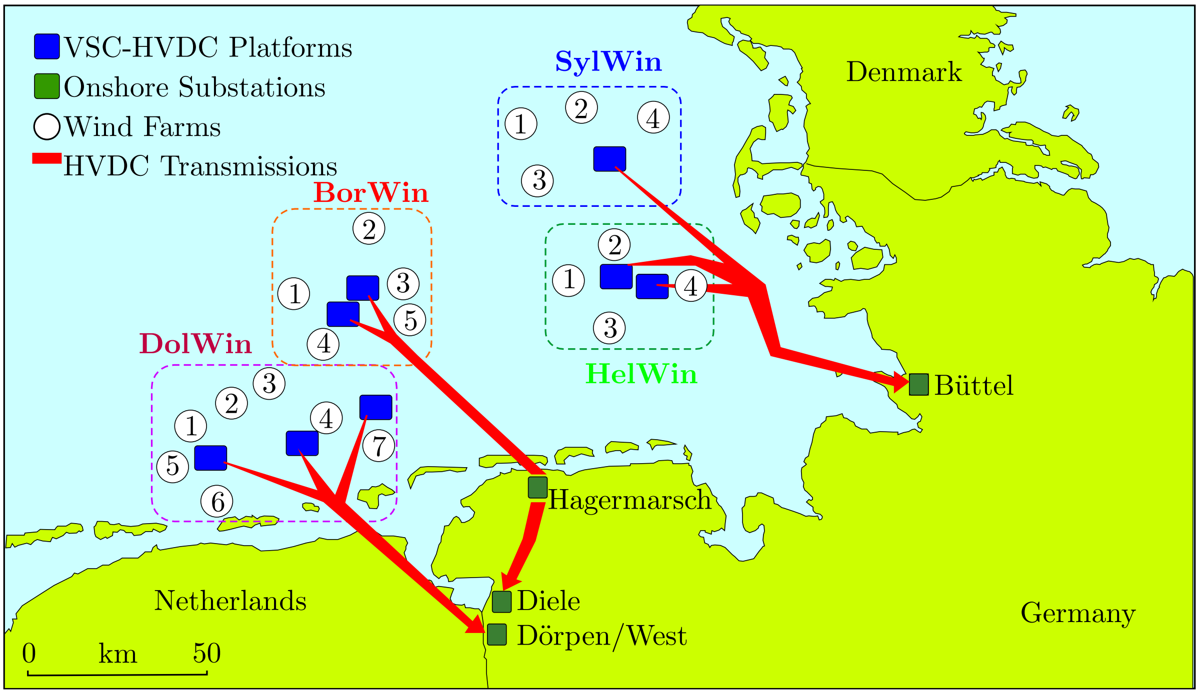
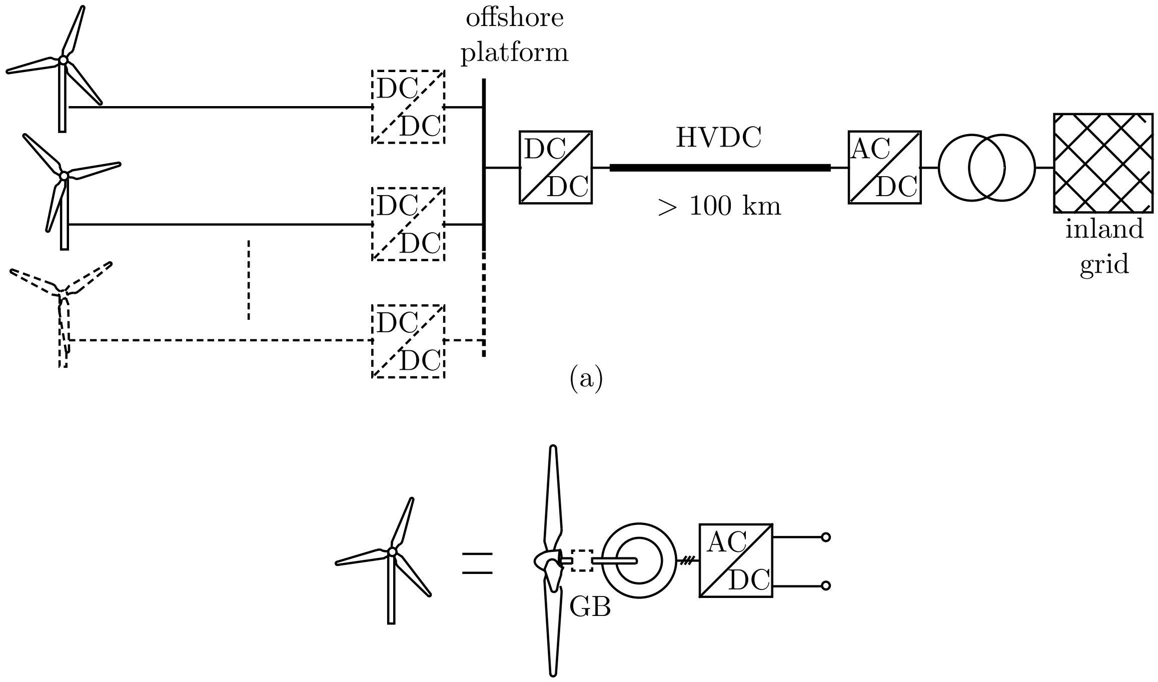


Fig. 2.2: HVDC interconnection for offshore wind farms in Germany [50].

converters for offshore power transmissions to comply with grid requirements imposed to the integration of wind farms to grid networks [16], [22], [26]–[28], [42]–[49].

Fig. 2.2 shows interconnections of several wind farms to the inland grid using ac-dc layout that employs VSC-HVDC in Germany. Each wind farm cluster, that is, HelWin, SylWin, BorWin, and DolWin, consists of several wind farms that are interconnected to an VSC-HVDC in an offshore platform using medium-voltage ac network. The VSC-HVDC converter collects the power from the wind farms before transmit the power to the inland grid through HVDC transmission. As an example, the HelWin1 uses a ±250-kV HVDC transmission system to transmit 576 MW of power to the inland grid for a total length of 85 km. The HelWin2 converts 155-kVac to ±320-kV HVDC transmission, and transmits 690 MW of power via a submarine high-voltage cable from the feed-in point on the platform to the grid connection point in Büttel, northwest of the city of Hamburg, for over 130 kilometers away. Afterward, the converter substation at the grid connection point converts the power back into alternating current for inland transmission and distribution. It is reported that the HVDC transmission losses are less than 4% [50].

Another alternative for power collection is based on a dc-dc layout that has been pro-



(a)

(b)

Fig. 2.3: Alternative power collection for offshore wind farms. (a) A dc-dc layout. (b) Wind turbine generator-converter set.

posed for large offshore wind farms [35]–[41]. A dc-dc power collection layout can be more easily controlled in a distributed manner. Fig. 2.3 shows an offshore wind farm configuration based on a dc-dc layout. Each power generation unit can be a single connection of a wind turbine (WT) or multiple series-parallel connections of wind turbines (WTs). The wind turbine may use a PMSG with a rectifier. Intermediary converters, as shown in dashed boxes in Fig. 2.3(a), are required to match the dc output voltages from the wind turbines on the power collection point. Otherwise, the dc output voltage on each wind turbine should be controlled directly from the converter set inside the nacelle. The generator-converter set, as shown in Fig. 2.3(b), requires less components because the converter needs only to generate a dc output voltage. Therefore, this configuration has higher reliability and flexibility than the ac-dc layout. Moreover, the dc-dc layout requires less footprint on the nacelle of each wind turbine, which is very suitable for far offshore applications.

An interconnection of several dc power generations using a multi-terminal dc network

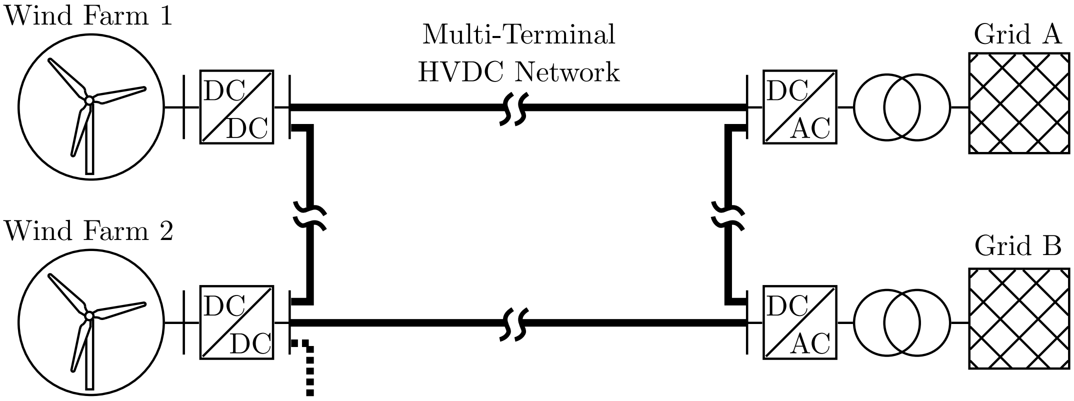


Fig. 2.4: Multi-terminal dc power transmission.

may become common in the near future, owing to the fact that VSC-HVDC technology has many advanced capabilities. Fig. 2.4 shows an interconnection of several offshore wind farms and inland grids using a multi-terminal HVDC network. The multi-terminal HVDC network is an extension of the well-established point-to-point HVDC interconnection, and it can improve the transmission system reliability and stability [51]–[54]. The development of the multi-terminal HVDC requires medium-/high-voltage and high-power dc-dc converters. They should be able to change one voltage level to another voltage level that may have a high voltage ratio.

The multi-terminal HVDC network also requires a robust protection system to deal with dc faults. However, the current technology of dc circuit breaker is still being developed [55]–[57], and hence may not be economically feasible at the moment [58]–[60]. Therefore, instead of using costly dc breakers, other alternatives have to be found [45], [61], [62].

2.2.1 High-Power DC Transformer

Similar to an ac power network that requires ac power transformers, a dc power network requires dc power transformers to adjust different voltage levels. Several topologies have been proposed for medium-voltage dc transformers [63]–[67]. Resonant converters can be applied for high-ratio dc-dc converters to reduce switching power loss [63]–[65]. However, they lack galvanic isolation and scalability for high-power applications.

Recently, several publications have proposed a front-to-front (FTF) configuration based on modular multilevel converters (MMCs) for high-power dc transformers [62]– [74]. The basic form of the MMC is incapable to handle dc faults in such that when a dc-side short circuit occurs, the fault current continues to flow through the anti-parallel diodes across the switching devices. However, the anti-parallel diodes can not withstand the large surge current, and should be equipped with press-pack thyristors in parallel with the diodes. Fast interruption of the fault current is essential for dc grid reliability. By interconnecting two MMCs in an FTF connection, with a transformer for galvanic isolation and voltage matching, a high-power dc-dc power conversion system can be achieved, while at the same time gaining an inherent dc-fault blocking capability.

Luth et al. have discussed the advantage of using medium frequency operation on the ac-link of an FTF system that can achieve significant volume saving due to reduced cell-capacitance requirement [74]. The authors have provided a simulation system based on an FTF system with three-phase 350-Hz ac-link operation. It is concluded that although significant volume saving can be achieved by using medium frequency operation on the ac link of the FTF system, a trade-off should be made between volume saving and switching power loss due to the increased switching frequency.

Kenzelmann et al. have proposed the use of an FTF system as a discrete tap-changer by using a two-level modulation instead of a multilevel modulation [62]–[69]. The authors provided experimental results of the FTF system using two single-phase 1-kW MMCs with four cells per leg and 1-kHz ac-link frequency. The power control of the system is done by using phase shift control between two MMCs. However, the proposed system requires several ac-link periods, which depends on the number of cells per leg, to balance the capacitors equally.

Gowaid et al. have proposed a medium-frequency FTF system based on a quasi two-level modulation [70], [71]. The ac-link voltage waveform is similar to a two-level modulation with a controllable slope. The advantages of using this modulation method include dv/dt stress alleviation, and cell-capacitances and footprint reduction. Moreover, no common-mode dc current is present in the arm of the MMCs. To control the power, the authors use both phase-shift and voltage-magnitude control. However, since the ac output voltage is almost similar to a two-level modulation method, it is necessary to modify

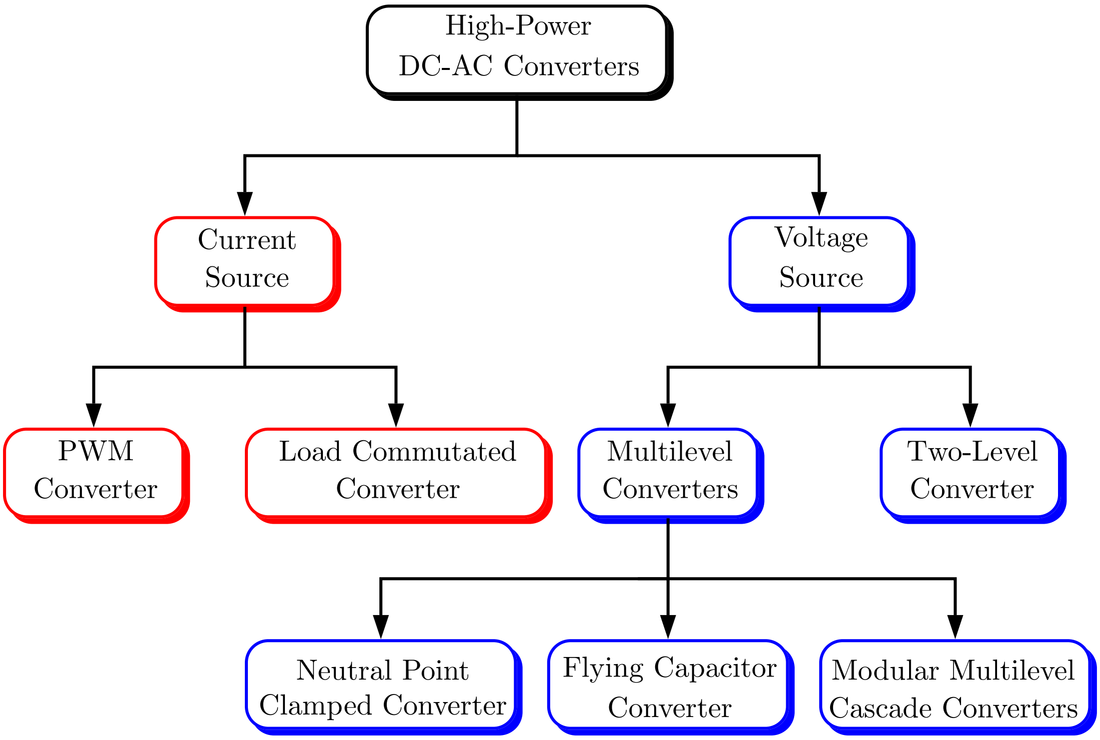


Fig. 2.5: High-power dc-ac converter classification.

the power transformer core to allow several harmonic frequencies in power transfer. Furthermore, the FTF system requires a discrete dc-link capacitor, which may impede the system in high-voltage applications.

2.3 High-Power Converter Topologies

Various high-power converter topologies exist and have found many industrial applications [75]–[81]. Fig. 2.5 shows a classification of high-power dc-ac conversion system. In high-power and high-voltage applications, multilevel converters are more attractive compared to two-level converters because they produce lower harmonic voltages and its resultant harmonic currents, which comply with the power quality standard. Moreover, multilevel converters solve the problem regarding the uneven voltage sharing that is present in two-level converters using series-connected power devices.

Before massive research and implementation of the MMC, the three-level neutral-point clamped (NPC) converter, which was introduced in late 1970s, is considered the first real

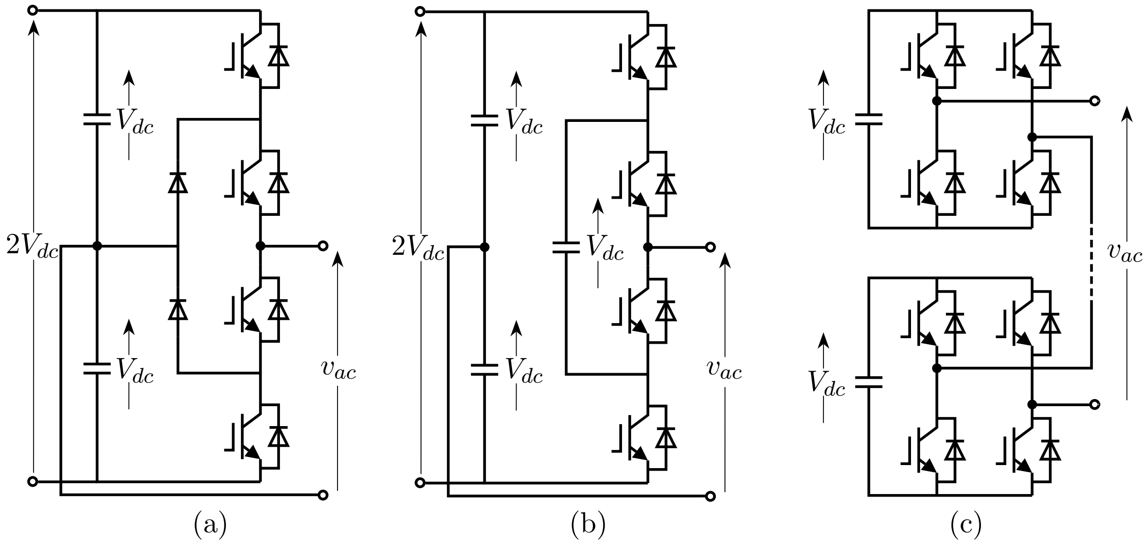


Fig. 2.6: One phase leg of multilevel converter topologies. (a) Neutral-point clamped (NPC) converter. (b) Flying-capacitor (FC) converter. (c) Cascaded H-bridge (CHB) converter.

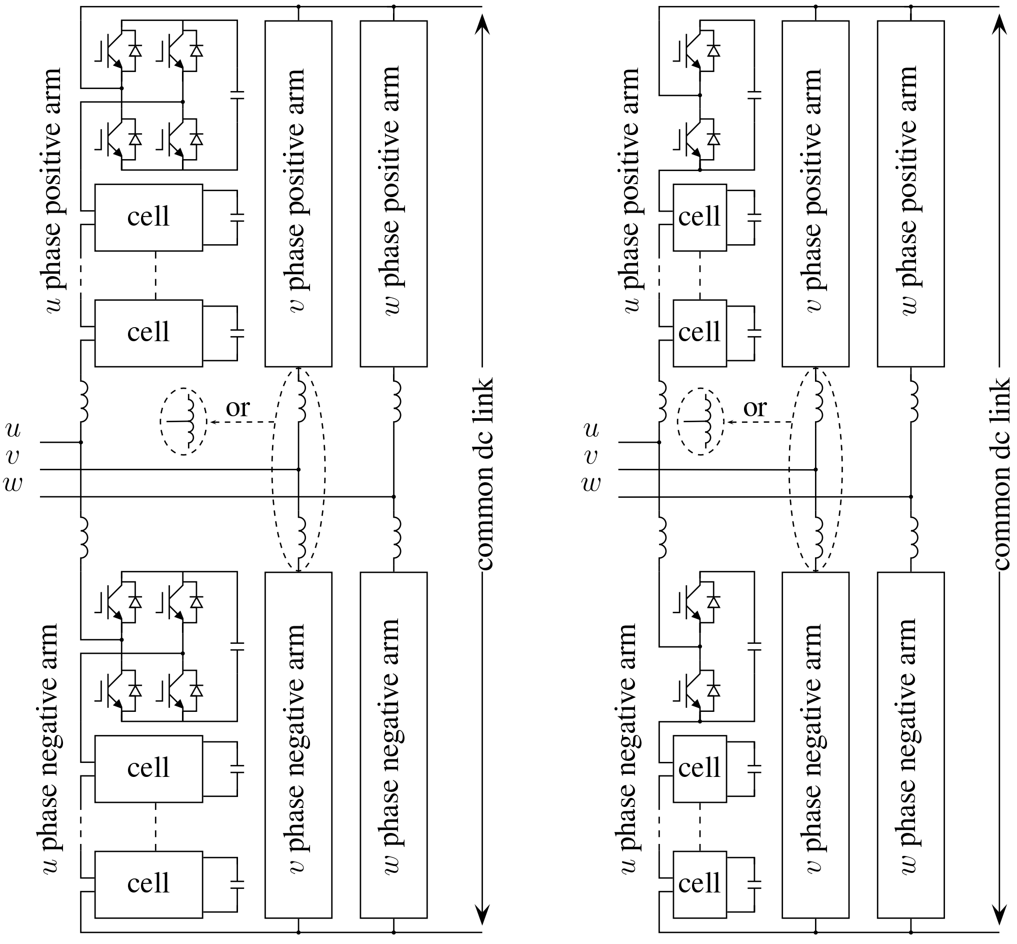
multilevel converter for medium voltage application [82]–[84]. Fig. 2.6(a) shows the three-level NPC converter, which is one of the most popular multilevel topologies used in the industry with the rated power within several ten of megawatts. The applications of NPC converter includes high-power ac motor drives (conveyors, pumps, fans, and mills, etc), and regenerative applications in back-to-back configuration, as in the full-scale converters for grid-connected wind turbines. However, it becomes less attractive at higher number of voltage level because of higher and uneven distribution of losses in the outer and inner devices, and unbalance dc-link capacitor voltage when conventional modulation strategies are used [78].

Another multilevel converter topology that has found particular applications, such as medium-voltage traction drives, is the flying-capacitor (FC) converter, as shown in Fig. 2.6(b) [75]. To produce an additional voltage level, a floating capacitor should be put between the middle switches of a phase leg of the converter. Although the FC converter has a modular structure, it has found less industrial penetration mainly because of higher switching frequencies that is necessary to keep the capacitors properly balanced. Hence, this topology may not be feasible for high-power applications, and may be limited to high-bandwidth high-switching frequency applications.

Fig. 2.6(c) shows the cascaded H-bridge (CHB) converter that has been successfully commercialized for very high-power applications because of its series expansion capability using cascaded configuration. It features no voltage balancing problem due to the use of an isolated dc source in each H-bridges cell. For ac-ac power conversion, a phase-shifting transformer with many secondaries is necessary to feed all of the H-bridge cells. Because of the bulky and expensive multiwinding transformer, this topology has a smaller market penetration. Nevertheless, the CHB converter is suitable for applications that use many dc sources like photovoltaic power generation [85], active filters, static var compensators (SVC) [86],[87], and battery energy storage system (BESS) [88].

The modular multilevel converter (MMC) has gained more attention recently for high power applications [43]–[45], [78]–[81], [89]–[96]. Because of modularity and redundancy of the cells or submodules used in the MMC, the number of series-connected cells can be adjusted easily to meet the desired voltage rating of the converter. This topology is highly modular, redundant, scalable, and flexible in terms of the number and type of cells, control methods, and other configurations. Thus, the MMC possesses a vast possibilities of converter topologies that may create confusion among researchers. Because of this reason, a classification and terminology that provides each of the converter topologies a distinguishable name has been proposed [96]. The converter topologies share a common family name, that is, the modular multilevel cascade converter (MMCC). However, each topology has a different individual name, which depends on the circuit configuration. For example, the aforementioned CHB converter can be classified as an MMCC based on single-star bridge-cells (MMCC-SSBC), or single-delta bridge-cells (MMCC-SDBC). For the sake of simplicity, the name can be termed as simply SSBC and SDBC converters, respectively.

Two other configurations of the MMCC that are applicable to medium-voltage motor drives, HVDC transmission, back-to-back (BTB) and front-to-front (FTF) systems, and renewable power conditioning system are the MMCC based on double-star chopper cells (MMCC-DSCC) [97]–[109], and the MMCC based on double-star bridge cells (MMCC-DSBC) [110], [111]. Fig. 2.7 shows the circuit configuration of the MMCC-DSBC and the MMCC-DSCC. While the MMCC-DSCC cannot produce a higher ac voltage from the dc-link voltage, the MMCC-DSBC has a buck-boost function of the dc-link for rectification



(a) (b)

Fig. 2.7: Two modular multilevel cascade converter topologies. (a) The DSBC converter. (b) The DSCC converter.

and inversion. Therefore, this converter can tolerate a broad range of dc-link voltage variations, which occurs in renewable energy sources such as wind and solar power. The MMCC-DSBC can also act as a three-to-single-phase direct frequency changer that is similar to cycloconverter [96], [111]. Moreover, it can tolerate dc fault inherently without causing any fault current [109]. From here on throughout this dissertation, the MMCC-DSCC and its applications will be discussed extensively, and the name will only be written as DSCC converter. The DSCC converter is originally developed for HVDC transmission systems, and is named as the MMC [89], [90]. It but can also be applied in many other applications such as motor drives.

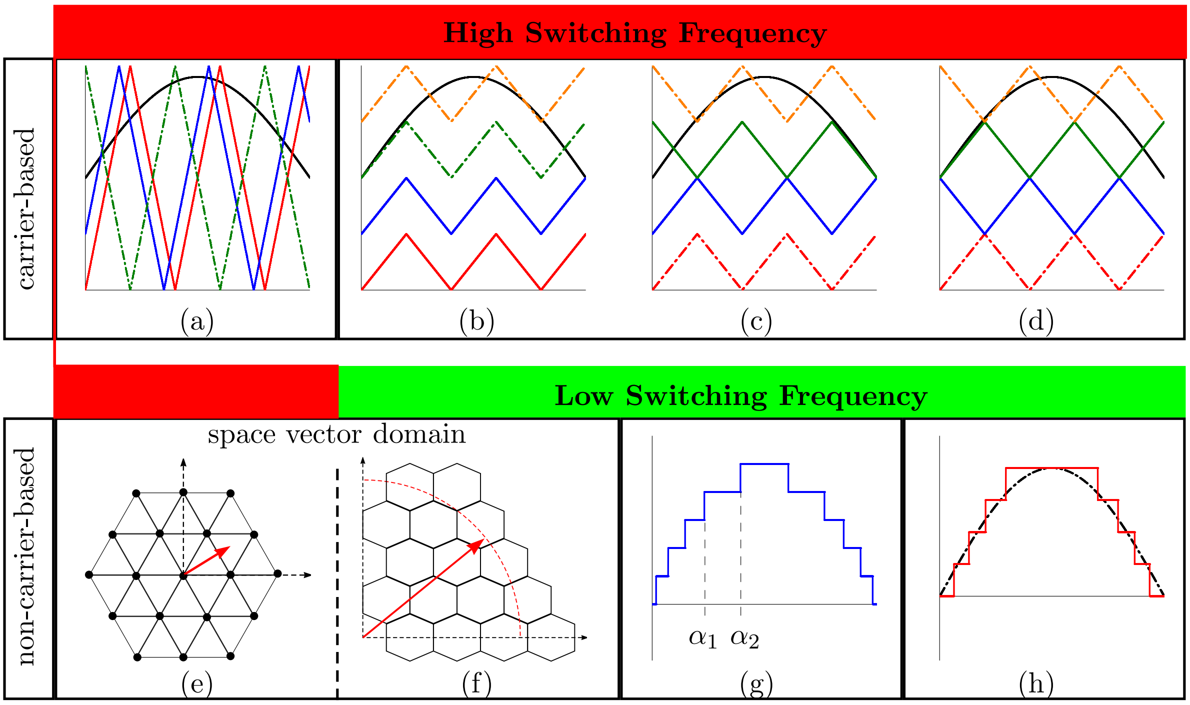


Fig. 2.8: Modulation methods for multilevel converters. (a) PSC-PWM. (b) PD-PWM. (c) POD-PWM. (d) APOD-PWM. (e) SVM. (f) SVC. (g) SHE. (h) NLC.

2.4 Modulation Methods for the DSCC Converter

In high-power and high-voltage applications, any converter should be designed to have high efficiency. Therefore, the switching frequency of the converter should be set as low as possible to reduce switching power loss. On of the advantages of multilevel converters over two-level or three-level converters is that the equivalent switching frequency of the ac-terminal voltage can be much higher than the actual switching frequency of the cells used in the multilevel converters. Thus, only a very small or even no filtering circuit is required at the grid side because of much better voltage quality [78]–[81].

Modulation methods for multilevel converters can be categorized into two groups, that is, carrier-based pulsewidth modulations (PWM) and non-carrier-based modulations or programmed PWM [78]–[81], [112]–[140]. Fig. 2.8 shows various modulation methods for multilevel converters that are also applicable to the DSCC converter. The carrier-based modulation techniques are mostly using either the phase-shifted-carrier PWM (PSC-

PWM) [112]–[116], or the level-shifted-carrier PWM (LSC-PWM) [117]–[120].

The carrier-based PWM method assigns a triangular carrier signal for each cell in the DSCC converter. In the PSC-PWM method, the triangular carriers for all cells within a phase leg have the same peak-to-peak amplitude, frequency, and voltage level (offset), but they have different phase shifts, as shown in Fig. 2.8(a). On the other hand, the LSC-PWM uses a triangular carrier with different voltage level for each cell. Depending on the phase shift of each cell, the LSC-PWM can be categorized into phase-disposition (PD-PWM), phase-opposition disposition (POD-PWM), or alternative phase-opposition disposition (APOD-PWM) as shown in Fig. 2.8(b)–(d), respectively.

Compared to the LSC-PWM, the PSC-PWM technique features inherent equal power distribution and lower capacitor-voltage fluctuation [122]–[124]. Furthermore, to achieve the same ac-terminal voltage quality as the PSC-PWM, the carrier frequency of the LSC-PWM technique need to be increased so as to produce equal number of pulses every ac-terminal period. The carrier signals of the LSC-PWM have to be rotated periodically to produce equal power distribution, and to balance the energy of all the floating capacitors in the DSCC converter. However, both modulation techniques are usually used with a high switching frequency which leads to a high switching power loss.

Non-carrier-based modulation techniques can produce a staircase voltage waveform using several algorithm, such as space vector modulation (SVM) [75], [78], [80], space vector control (SVC) [75], selective harmonic elimination (SHE) technique [120], [129], [130], nearest level control (NLC) modulation technique [131]–[136], and averaging or submodule unified PWM (SUPWM) [126]–[127], and other modulation methods [128], [137]–[140].

The SVM is a technique in which the reference voltage is represented as a reference vector. Each discrete switching state of the converter lead to a discrete output voltage, and it can be also represented as the possible voltage vector (state vector), as shown in Fig. 2.8(e). The SVM technique generates the voltage reference vector as a linear combination of the state vectors. The average output voltage of the state vectors equal to the reference over one switching period. The SVM technique requires trigonometric function calculations, look-up tables, or coordinated system transformations, which increase the computational load. The SVM method may not be suitable for the DSCC converter when the number of cells is too high because it requires complex vector calculation and selection. Moreover, the computational cost and the algorithm complexity are increased with the number of levels.

The SVC technique produces the ac output voltage by approximating the reference voltage to the closest vector that can be generated by the converter, as shown in Fig. 2.8(f). The SVC requires a numerical algorithm capable of finding the closest vector to the reference voltage. Since the operating principle is based on an approximation and not a time average of the reference as in the SVM, it is suitable for multilevel converter with a high number of levels. Therefore, the SVC can produce a fundamental switching frequency, and it can be easily implemented in closed-loop and high-bandwidth systems. However, due to the low and variable switching frequency, they present higher total harmonic distortion for converters with a lower number of levels and also for low modulation indexes.

The SHE technique produces the ac-terminal voltage according to the switching angles, as shown in Fig. 2.8(g), by performing an offline computation to solve the harmonic equations with associated modulation index and harmonic elimination requirement so that arbitrary harmonics (usually of low order) are eliminated. The computation is based on the Fourier series and the assumption of steady-state sinusoidal voltages. The computation results are stored in lookup tables, and the switching angles can be interpolated according to the operating conditions. The SHE technique controls directly the harmonic spectrum of the ac-terminal voltage, and it can reduce the switching frequency even to as low as the fundamental frequency. However, it is limited in practice to open-loop or low-bandwidth applications because the switching angles are computed offline, and stored in tables. The complexity of the computation process to solve nonlinear equations increases as the number of level increases. Moreover, both of the number and scale of the tables will be too large when it comes to hundreds of voltage levels and a wide range of modulation indexes.

The NLC modulation technique directly provides the number of cells to be inserted for each arm according to the nearest integer value of the reference voltage, as shown in Fig. 2.8(h). The harmonic contents of the ac-terminal voltage are highly related to the number of available cells in each arm. To obtain the switching patterns, the voltage reference is multiplied by the number of positive voltage levels, and then a round function is applied to find the required output voltage level nearest to the desired voltage waveform. The NLC technique is basically the time-domain version of the SVC, which in essence is the same principle but considering the closest voltage level that can be generated by the converter instead of the closest vector. The NLC determines only the switching instants, and thus a cell selection method is required to conduct the capacitor voltage balancing. The NLC technique is based on fundamental-frequency switching, and it might be much simpler to facilitate the modulation process, and requires less computational efforts, while achieving a comparable performance compared to the SVC or SHE techniques. The advantage of the NLC technique emerges along with the increase of cell numbers in the DSCC converter. However, because of the approximation nature of round function used in the NLC, the voltage level selection at each sampling period always contains error.

Several recent publications have addressed various non-carrier-based modulation techniques for the DSCC converter that generate low switching frequencies [128], [132]–[134], [140]. The switching frequencies can be as low as the ac-terminal frequency by using the “nearest voltage-level control” modulation method [132]–[134]. A new modulation technique proposed by Ilves et al. can also produce a fundamental switching frequency [140]. Hassanpoor et al. proposed another modulation technique based on a “tolerance band” that can produce low switching frequency close to fundamental frequency [128]. However, the switching frequency is not constant depending on operating conditions. Although the programmed PWM may produce low switching frequencies, the complexity of the algorithms increases as the number of cells increases. Many manufacturers favor the proven technology and simplicity of the matured carrier-based PWM techniques over new modulation techniques that have low-switching-frequency advantage but usually at the expense of more complex implementation [78].

A few attempts had discussed carrier-based PWM to operate in low switching frequency [112], [114], [115]. However, no literature has discussed the use of carrier-based PWM with low carrier frequency that is comparable to the aforementioned programmed-based PWM methods. It is even stated that carrier-based PWM cannot be used with carrier frequency lower than 100 Hz, where the fundamental frequency is 50 Hz [128].

Table 2.1: Low-switching-frequency operation for the DSCC converter

Modulation Method	Switching Frequency	Reference
Selective Harmonic Elimination (SHE)	f_{ac}	[140]
Nearest Voltage Level Control (NLC)	f_{ac}	[132], [134]
Tolerance Band Modulation	$1.4f_{\mathrm{ac}} \sim 2.2f_{\mathrm{ac}}$	[128]
NLC	$2.2f_{\mathrm{ac}} \sim 3.2f_{\mathrm{ac}}$	[133]
Phase-Shifted-Carrier PWM (PSC-PWM)	$2.2f_{\mathrm{ac}}$	[112]
PSC-PWM	$2.5f_{\mathrm{ac}}$	[114]
Modified PSC-PWM	$\sim 3f_{\mathrm{ac}}$	[115]

Nevertheless, low-switching-frequency operation tends to make the floating capacitor voltages in the DSCC converter fluctuate higher compare to that of the higher switching frequency used in carrier-based PWM methods. Therefore, a tradeoff between low switching frequency and low capacitor voltage ripple should be made regardless of the modulation method [122], [133].

Table 2.1 shows a summary of the aforementioned modulation methods that produce low switching frequencies. The switching frequencies are normalized to the ac-terminal frequency f_{ac}. Some of the modulation methods produce non-fixed switching frequencies that depend on the operating condition.

2.5 Summary

This chapter has provided an overview on several options of power collection and transmission for large offshore wind farms. The imminent properties of multilevel converters for medium-/high-voltage and high-power applications have also been described, including the applications of each converter topology. It can be concluded that the modular multilevel cascade converter family is very suitable for high-power applications. This chapter has also reviewed various modulation methods that have been developed recently with the aim of reducing the switching power loss.

Chapter 3

The Modular Multilevel Double-Star Chopper-Cells Converter

3.1 Introduction

This chapter discusses theoretical reviews on circuit operation and control method of the modular multilevel double-star chopper-cells (DSCC) converter. The operation of the DSCC converter discussed in this dissertation is based on the phase-shifted-carrier pulsewitdh modulation (PSC-PWM) method. The circulating current and power flow within one leg of the DSCC converter will be discussed in detail. This chapter also discusses voltage fluctuation across the capacitor of a chopper cell, which is caused by a PWM operation, to give an insight on the harmonic contents of the capacitor voltage. Finally, a power control and a capacitor balancing control used for the DSCC converter are also presented.

3.2 Circuit Configuration

Fig. 3.1 shows the circuit configuration of a three-phase DSCC converter consisting of N series-connected chopper cells for each phase leg. The circuit configuration of the DSCC converter is similar to the MMC [90]–[94]. The DSCC converter uses a center-tapped inductor L_Z instead of two single inductors between upper and lower arms of each phase leg [96]. The ac-terminal voltage contains $N+1$ and $2N+1$ levels in maximum at the line-to-neutral and line-to-line voltage, respectively. In a grid-connected scheme, an

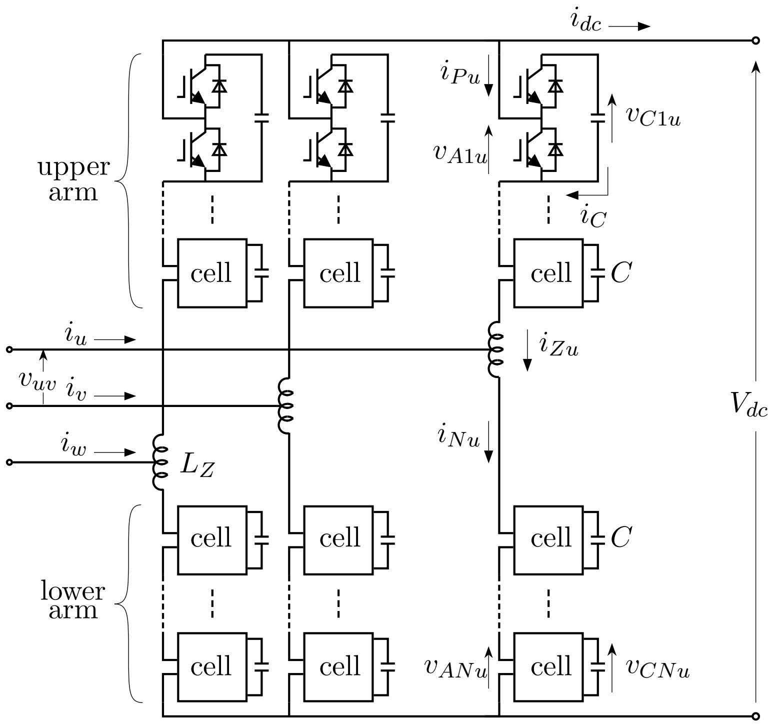


Fig. 3.1: Circuit configuration of a three-phase DSCC converter with N chopper cells per leg.

ac-link inductor in each phase should be connected between the ac mains terminal and the center terminal of the center-tapped inductor L_Z to support the voltage difference between the two terminals.

To analyze the circuit, it is helpful to consider only a single phase-leg circuit of the DSCC converter. In the discussion of the circuit analysis to follow, without loss of generality, only the u-phase leg will be mentioned because the analysis is the same for the other two phase legs.

Fig. 3.2 shows a single phase representation of the DSCC converter in which v_u is the ac-terminal voltage of the u-phase leg, and is measured with respect to the middle point of the dc terminals or the ground node in Fig. 3.2. The dc-link terminals are connected to two dc voltage sources, each of which has half the voltage of V_{dc}. The series-connected chopper cells in each arm can be represented by an ideal sinusoidal voltage source, v_{Pu} and v_{Nu}, respectively, for upper/positive and lower/negative arm. Note that v_{Pu} and v_{Nu} are out of phase by 180° each other. The phase voltage v_u can then be represented

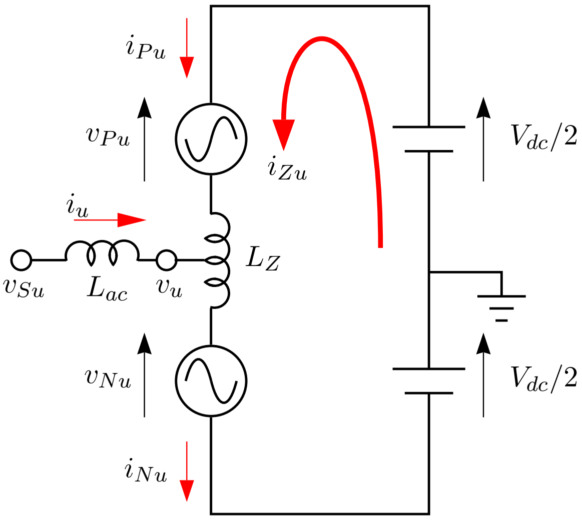


Fig. 3.2: Ideal representation of a single phase leg DSCC.

as

$$v_u = \frac{1}{2}(v_{Nu} - v_{Pu}). \tag{3.1}$$

The phase voltage v_u can also be represented in terms of the dc voltage V_{dc} with the assumption of zero voltage drop across the center-tapped inductor L_Z as follows:

$$v_u = -v_{Pu} + \frac{V_{dc}}{2}, \tag{3.2}$$

$$v_u = v_{Nu} - \frac{V_{dc}}{2}. \tag{3.3}$$

There are two independent currents in the phase leg, that is, the dc circulating current i_{Zu} and the ac supply or line current i_u. The upper and lower arm currents can be regarded as dependent currents, and they can be expressed as follows:

$$i_{Pu} = -\frac{i_u}{2} + i_{Zu}, \tag{3.4}$$

$$i_{Nu} = \frac{i_u}{2} + i_{Zu}. \tag{3.5}$$

Equations (3.4) and (3.5) show that the upper and lower arms contain ac and dc current components because the circuit is connected to a dc voltage and an ac voltage at the same time. The equations also show that the line current component on the upper and lower arms are out of phase by 180° each other. As a result, the magnetic fluxes produced

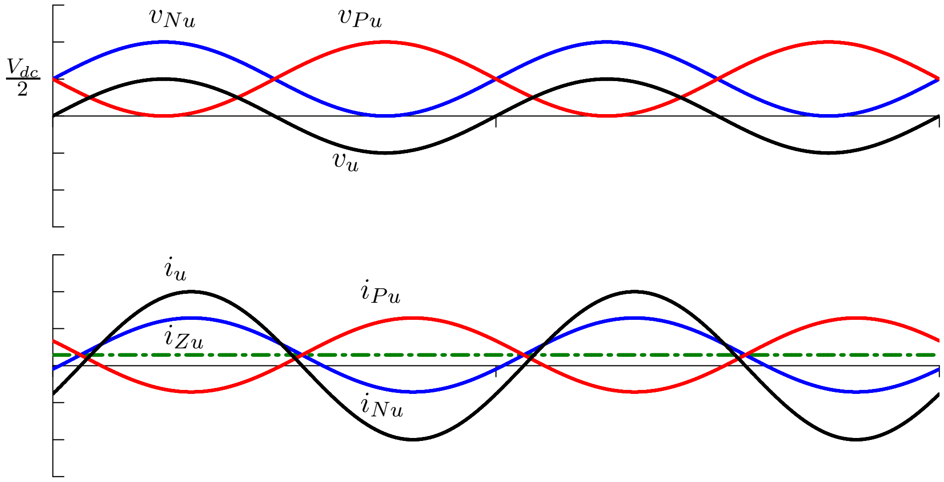


Fig. 3.3: Ideal signal waveforms of one leg of the DSCC converter.

by the line current cancel out each other inside the magnetic core of the center-tapped inductor. Therefore, the inductor presents no inductance to the line current i_u, whereas it renders the inductance L_Z to the circulating current i_{Zu} that is flowing through all the chopper cells in the u-phase leg.

Fig. 3.3 shows the ideal signal waveforms of the voltages and currents in the single phase DSCC converter. The circulating current i_{Zu} plays an important role in power transfer between the dc side and ac side of the DSCC converter. The dc-capacitor average voltage in each chopper cell can be regulated by controlling the circulating current i_{Zu}.

In an ideal three-phase DSCC converter, the ac-terminal voltages and line currents can be represented follows:

$$v_u = \sqrt{\frac{2}{3}}V\sin\omega t, \tag{3.6}$$

$$v_v = \sqrt{\frac{2}{3}}V\sin(\omega t - \frac{2\pi}{3}), \tag{3.7}$$

$$v_w = \sqrt{\frac{2}{3}}V\sin(\omega t + \frac{2\pi}{3}), \tag{3.8}$$

$$i_u = \sqrt{2}I\sin(\omega t - \theta), \tag{3.9}$$

$$i_v = \sqrt{2}I\sin(\omega t - \frac{2\pi}{3} - \theta), \tag{3.10}$$

$$i_w = \sqrt{2}I\sin(\omega t + \frac{2\pi}{3} - \theta), \tag{3.11}$$

where V and I are the root mean square (rms) values of the line-to-line voltages and the line currents, respectively, ω is the operating frequency at the ac link of the DSCC converter, and θ is the phase difference between the voltage and current in the same phase leg. In a DSCC converter with a dc voltage of V_{dc}, the maximum amplitude of the peak voltage that can be achieved at the ac terminal without going into over-modulation is

$$\begin{aligned}\hat{V}_u &= \sqrt{\frac{2}{3}}V \\ &= \frac{V_{dc}}{2}.\end{aligned} \tag{3.12}$$

Thus, the attainable line-to-line rms voltage of the DSCC converter with a dc voltage V_{dc} and a modulation index M $(0 \leq M \leq 1)$ is as follows:

$$V = \frac{\sqrt{3}}{2} M V_{dc}. \tag{3.13}$$

For an example, when the dc-side voltage V_{dc} is 400 V, then the maximum achievable line-to-line voltage is 245 V.

The three-phase power on the ac side of the DSCC converter can be represented as follows:

$$P_{ac} = \sqrt{3} V I. \tag{3.14}$$

Equation (3.14) applies for a balanced and ideal three-phase DSCC converter system. In an actual system, the ac-terminal voltage of the DSCC converter may contain some harmonic-frequency components because of the staircase or PWM modulation. Thus, the actual power equation also includes the harmonic components.

The dc power flowing in the circuit can be represented as

$$P_{dc} = V_{dc} I_{dc}, \tag{3.15}$$

where I_{dc} is the dc current of the DSCC converter. In a balanced three-phase DSCC converter, it can be assumed that the dc current amplitude is three times the circulating current in each phase leg I_Z as follows:

$$I_{dc} = 3 I_Z. \tag{3.16}$$

By assuming $P_{ac} = P_{dc}$ and substituting (3.15) and (3.16) to (3.14), the rms value of the line current can be represented as follows:

$$I = \frac{\sqrt{3} V_{dc} I_Z}{V}. \tag{3.17}$$

By using (3.13) and (3.17), the circulating current I_Z can be related to the line current as follows:

$$I_Z = \frac{MI}{2\sqrt{2}}. \tag{3.18}$$

Equation (3.18) shows that to achieve a balance power transfer for a modulation index M, the circulating current I_Z should be controlled based on the rms line current I.

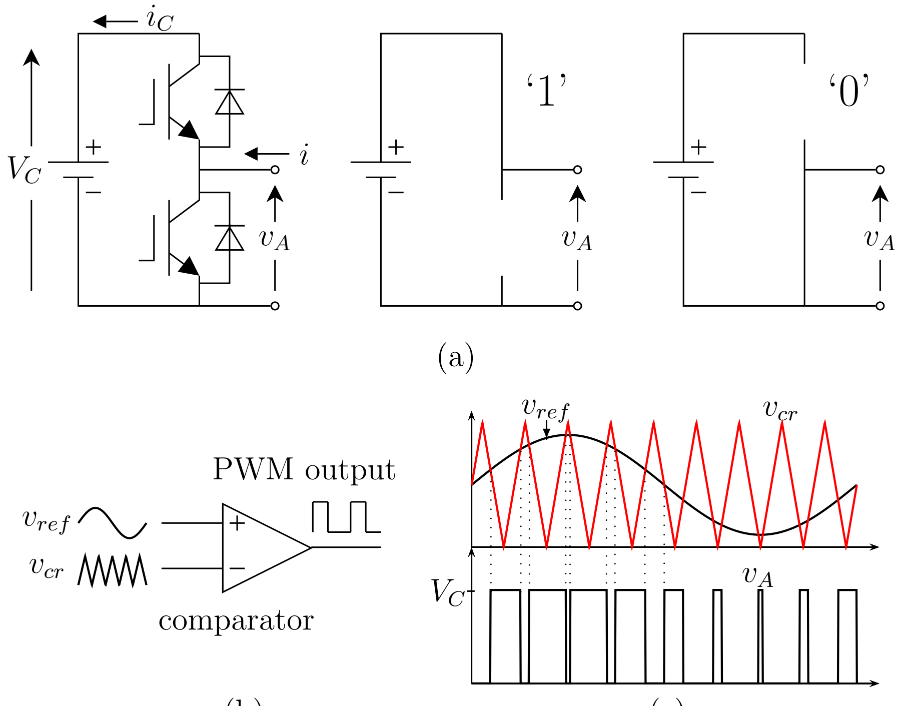
3.3 Pulsewidth Modulation for Chopper Cells

3.3.1 Switching Function

Fig. 3.4 shows basic operation of a half-bridge cell or a chopper cell that consists of two power switches that switch alternately to produce ‘1’ and ‘0’ states. The dc-side of the chopper cell is connected to a dc voltage source or an energy storage such as a capacitor. The chopper cell is in ‘1’ state if the upper switch is turned on while the lower switch is turned off. Otherwise, the chopper cell has a ‘0’ state. In a pulsewidth modulation (PWM) method, the arm-side voltage of the chopper cell is produced by modulating a reference signal with a carrier signal, as depicted in Fig. 3.4(b). The output of the modulator is used as a signal to drive the switches to produce the desired arm-side voltage v_A.

Fig. 3.4(c) shows voltage waveforms in the PWM method applied to the chopper cell and its respective arm-side voltage. The upper switch is turned on when the reference signal v_{ref} is higher than the carrier signal v_{cr}. Likewise, the lower switch is turned on when the reference signal v_{ref} is lower than the carrier signal v_{cr}. When the chopper cell is in ‘1’ state, the arm-side voltage v_A is connected to the dc-side of the chopper cell, thus having the same voltage of V_C. On the contrary, when the chopper cell is in ‘0’ state, the arm-side voltage v_A has a zero voltage. With this strategy, it is possible to produce an ac signal by manipulating the reference signal v_{ref}. However, the actual arm-side voltage has not only the desired reference signal v_{ref} but also the switching harmonics caused by the PWM method. Nevertheless, a dc-to-ac power conversion can be achieved easily with this strategy.

Basically, the chopper cell is used for a dc-to-ac power conversion by modulating a



(a)

(b)

(c)

Fig. 3.4: A chopper cell circuit employing PWM. (a) Basic operation. (b) PWM generator. (c) Chopper-cell voltage waveforms.

sinusoidal signal over a triangle or sawtooth signal to produced a PWM voltage. It is possible to explain the arm-side voltage v_A as a function of the dc-side voltage V_C and a switching function S in time domain:

$$v_A = SV_C, \tag{3.19}$$

$$S = v_{ref} + \sum_{m=1}^{\infty} \frac{2}{m\pi} \sin(m\pi v_{ref}) \cos\big(m(\omega_{cr}t + \theta_{cr})\big), \tag{3.20}$$

where v_{ref} is the reference signal, ω_{cr} is the angular frequency of the triangular carrier, and θ_{cr} is the phase shift of the carrier to an arbitrary point in time. Note that (3.19) holds with the assumption of zero dead time, that is, the upper and lower switches of the chopper cell commutate instantaneously. The switching function S is basically a mathematical expression of the PWM signal based on Fourier series expansion for any positive integer m.

The reference signal v_{ref} can be assumed as a sinusoidal signal that has an angular frequency of ω_{ac} and a dc offset, as shown in Fig. 3.4(c), and can be written as

$$v_{ref} = \frac{1}{2} + \frac{M}{2}\cos(\omega_{ac}t + \theta_{ac}), \tag{3.21}$$

where M is the modulation index, and θ_{ac} is the phase shift of the reference signal to an arbitrary point in time. It is assumed for now that the maximum peak-to-peak voltage of the reference is one volt with the dc offset of 1/2. From (3.20) and (3.21), the switching function S can then be expressed as

$$S = \frac{1}{2} + \frac{M}{2}\cos(\omega_{ac}t + \theta_{ac}) + \sum_{m=1}^{\propto} \frac{2}{m\pi}\sin\left(\frac{m\pi}{2} + \frac{m\pi M}{2}\cos(\omega_{ac}t + \theta_{ac})\right)\cos\big(m(\omega_{cr}t + \theta_{cr})\big). \tag{3.22}$$

The first and second terms on the right-hand side of (3.22) are essentially the dc and fundamental ac components from the reference signal v_{ref}, whereas the last term of the equation indicates the switching harmonics H which can be expanded as follows:

$$H = \begin{cases} \displaystyle\sum_{m=1}^{\propto} \frac{2}{m\pi}\cos\left(\frac{m\pi}{2}\right)\sin\left(\frac{m\pi M}{2}\cos(\omega_{ac}t + \theta_{ac})\right)\cos\big(m(\omega_{cr}t + \theta_{cr})\big) & \text{if } m \text{ is even} \\ \displaystyle\sum_{m=1}^{\propto} \frac{2}{m\pi}\sin\left(\frac{m\pi}{2}\right)\cos\left(\frac{m\pi M}{2}\cos(\omega_{ac}t + \theta_{ac})\right)\cos\big(m(\omega_{cr}t + \theta_{cr})\big) & \text{if } m \text{ is odd.} \end{cases} \tag{3.23}$$

One way to solve (3.23) is by using the Jacobi-Anger expansion of the Bessel function to simplify the equation further:

$$H = \sum_{m=1}^{\propto}\sum_{n=-\propto}^{\propto} \frac{2}{m\pi}J_n\left(\frac{m\pi M}{2}\right)\sin\left(\frac{\pi}{2}(m+n)\right)\cos\left((m\omega_{cr} + n\omega_{ac})t + m\theta_{cr} + n\theta_{ac}\right), \tag{3.24}$$

where J_n is the n-th Bessel function of the first kind, and n is any integer number. By inserting the switching harmonics H in (3.24) back into the switching function S in (3.22), the switching function S finally becomes

$$\begin{aligned} S = \frac{1}{2} + \frac{M}{2}\cos(\omega_{ac}t + \theta_{ac}) + \sum_{m=1}^{\propto}\sum_{n=-\propto}^{\propto} \frac{2}{m\pi}J_n\left(\frac{m\pi M}{2}\right)\sin\left(\frac{\pi}{2}(m+n)\right) \\ \times\cos\left((m\omega_{cr} + n\omega_{ac})t + m\theta_{cr} + n\theta_{ac}\right). \end{aligned} \tag{3.25}$$

A deeper insight of (3.25) shows that the switching function S contains the following components:

1. DC and fundamental ac frequency (ω_{ac}) that resemble the reference signal,

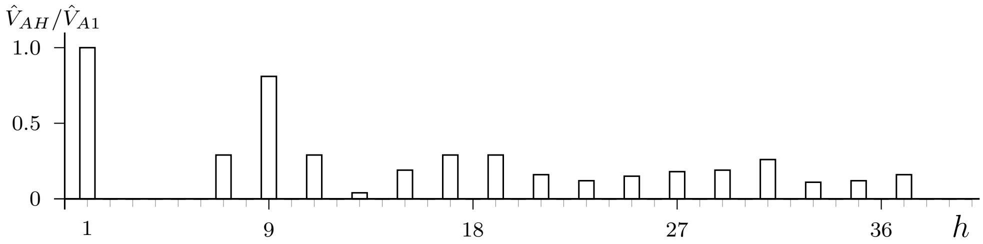


Fig. 3.5: Normalized harmonic spectrum of the switching function with modulation index $M = 0.9$ and carrier frequency $\omega_{cr} = 9\omega_{ac}$.

2. Odd integer multiples of carrier frequency $\big((2m'-1)\omega_{cr}\big)$,
3. Even sideband harmonics at the central of odd integer multiples of carrier frequency $\big((2m'-1)\omega_{cr} \pm 2n'\omega_{ac}\big)$,
4. Odd sideband harmonics at the central of even integer multiples of carrier frequency $\big(2m'\omega_{cr} \pm (2n'-1)\omega_{ac}\big)$.

Note that $2m'-1$ and $2n'-1$ represent odd numbers of m and n, respectively. Likewise, $2m'$ and $2n'$ represent even numbers of m and n, respectively. It is interesting to note that even integer multiples of carrier frequency $(2n'\omega_{cr})$ are not present in the switching function.

Fig. 3.5 shows the harmonic spectrum of the switching function from Fig. 3.4 for several harmonic orders h. Note that if the carrier frequency is set to an odd integer multiple of the fundamental frequency, then the arm-side voltage v_A contains no even harmonics. The switching harmonics will move further from the fundamental frequency as the carrier frequency gets higher. On the other hand, as the carrier frequency gets lower, low order harmonics will appear and may heavily influence the desired output voltage.

3.3.2 Capacitor Current

It is important to know the dc-side current of the chopper cell as the current determines the dc-side voltage of the chopper cell, especially when a capacitor is being used instead of a dc voltage source. The dc-side current of the chopper cell is basically the arm-side

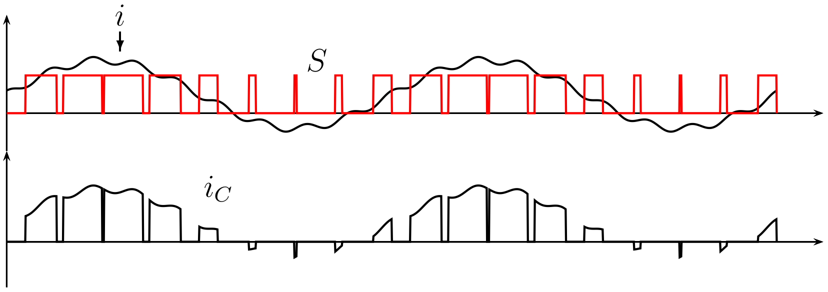


Fig. 3.6: Capacitor current in the chopper cell circuit from Fig. 3.4.

current when the upper switch is turned on, and equal to zero when the lower switch is turned on.

Fig. 3.6 shows the capacitor current i_C as a function of the arm-side current i and the switching function S. The capacitor current can be described simply as

$$i_C = Si. \tag{3.26}$$

The arm-side current i is any current containing dc component, ac fundamental and its harmonics components, and can be written as

$$i = I_{dc} + \sum_{l=1}^{\propto} \hat{I}_l \cos\left(l\omega_{ac}t + \theta_{il}\right), \tag{3.27}$$

where l indicates the frequency components of the arm-side current, and θ_{il} represents the phase shift of each frequency component. Note that the arm-side current has the same fundamental frequency ω_{ac} as the reference voltage v_{ref}. From (3.25) – (3.27), the capacitor current can be expressed as

$$\begin{aligned} i_C = {} & \frac{I_{dc}}{2} + \frac{MI_{dc}}{2}\cos(\omega_{ac}t + \theta_{ac}) + \sum_{l=1}^{\propto} \frac{\hat{I}_l}{2}\cos\left(l\omega_{ac}t + \theta_{il}\right) \\ & + \sum_{l=1}^{\propto} \frac{M\hat{I}_l}{2}\cos\left(l\omega_{ac}t + \theta_{il}\right)\cos(\omega_{ac}t + \theta_{ac}) \\ & + \sum_{m=1}^{\propto}\sum_{n=-\propto}^{\propto} \frac{2I_{dc}}{m\pi} J_n\left(\frac{m\pi M}{2}\right)\sin\left(\frac{\pi}{2}(m+n)\right)\cos\left((m\omega_{cr} + n\omega_{ac})t + m\theta_{cr} + n\theta_{ac}\right) \\ & + \sum_{m=1}^{\propto}\sum_{n=-\propto}^{\propto}\sum_{l=1}^{\propto} \frac{2\hat{I}_l}{m\pi} J_n\left(\frac{m\pi M}{2}\right)\sin\left(\frac{\pi}{2}(m+n)\right) \\ & \times \cos\left((m\omega_{cr} + n\omega_{ac})t + m\theta_{cr} + n\theta_{ac}\right)\cos\left(l\omega_{ac}t + \theta_{il}\right). \end{aligned} \tag{3.28}$$

Equation (3.28) can be regarded as a general solution for the capacitor current when the arm current contains all the frequency components including a dc component. If we can assume that the arm current contains only dc and fundamental ac components, then the equation can be simplified as follows:

$$i_C = \frac{I_{dc}}{2} + \frac{M\hat{I}_1}{4}\cos(\theta_{ac} - \theta_{i1}) + \hat{I}_{C1}\cos(\omega_{ac}t + \theta_{C1}) + \frac{M\hat{I}_1}{4}\cos(2\omega_{ac}t + \theta_{i1} + \theta_{ac}) + i_{CH}, \tag{3.29}$$

where $\hat{I}_{C1}$ and θ_{C1} are the magnitude and phase of the fundamental ac component of the capacitor current, respectively; i_{CH} is the switching harmonic components of the capacitor current, and can be calculated as follows:

$$\hat{I}_{C1} = \frac{1}{2}\sqrt{(MI_{dc})^2 + \left(\hat{I}_1\right)^2 + 2MI_{dc}\hat{I}_1\cos(\theta_{ac} - \theta_{i1})}, \tag{3.30}$$

$$\theta_{C1} = \tan^{-1}\left(\frac{MI_{dc}\sin(\theta_{ac}) + \hat{I}_1\sin(\theta_{i1})}{MI_{dc}\cos(\theta_{ac}) + \hat{I}_1\cos(\theta_{i1})}\right), \tag{3.31}$$

$$\begin{aligned} i_{CH} = & \sum_{m=1}^{\propto}\sum_{n=-\propto}^{\propto}\frac{2I_{dc}}{m\pi}J_n\left(\frac{m\pi M}{2}\right)\sin\left(\frac{\pi}{2}(m+n)\right)\cos\left((m\omega_{cr} + n\omega_{ac})t + m\theta_{cr} + n\theta_{ac}\right) \\ & + \sum_{m=1}^{\propto}\sum_{n=-\propto}^{\propto}\frac{\hat{I}_1}{m\pi}J_n\left(\frac{m\pi M}{2}\right)\sin\left(\frac{\pi}{2}(m+n)\right) \\ & \times\cos\Big(\big(m\omega_{cr} + (n-1)\omega_{ac}\big)t + m\theta_{cr} + n\theta_{ac} - \theta_{i1}\Big) \\ & + \sum_{m=1}^{\propto}\sum_{n=-\propto}^{\propto}\frac{\hat{I}_1}{m\pi}J_n\left(\frac{m\pi M}{2}\right)\sin\left(\frac{\pi}{2}(m+n)\right) \\ & \times\cos\Big(\big(m\omega_{cr} + (n+1)\omega_{ac}\big)t + m\theta_{cr} + n\theta_{ac} + \theta_{i1}\Big). \end{aligned} \tag{3.32}$$

From (3.29) – (3.32), it can be seen that the capacitor current contains dc, fundamental ac frequency, second harmonic, and also switching harmonic components when the flowing arm current consists of dc and fundamental ac components. The magnitude of the capacitor current depends on the dc and fundamental ac components of the arm current (I_{dc} & $\hat{I}_1$), the modulation index M, as well as the phase shift between the fundamental ac components of the arm voltage and current in the chopper cell ($\theta_{ac} - \theta_{i1}$). The carrier frequency used in the chopper cell utilizing a PWM method influences considerably the profile of the switching harmonic components in the capacitor current i_{CH}. If the switching harmonic components of the capacitor current can be omitted, then

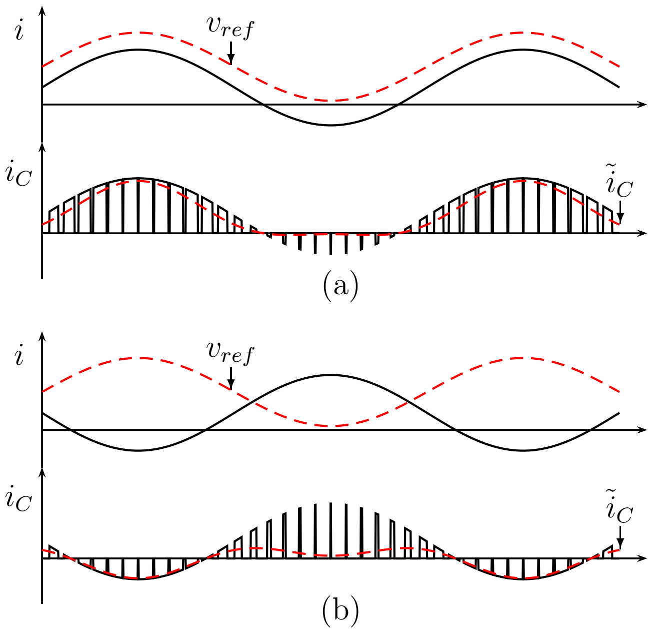


Fig. 3.7: Arm current i, capacitor current i_C and its analytical approximation $\tilde{i}_C$, in a chopper cell with modulation index $M = 0.9$ and carrier frequency $\omega_{cr} = 25\omega_{ac}$. (a) For $\theta_{ac} - \theta_{i1} = 0$. (b) For $\theta_{ac} - \theta_{i1} = \pi$.

the capacitor current can be seen as a current containing only dc, fundamental ac, and second harmonic components. The approximated value of the capacitor current $\tilde{i}_C$ can be written as

$$i_C \approx \tilde{i}_C = \frac{I_{dc}}{2} + \frac{M\hat{I}_1}{4}\cos(\theta_{ac} - \theta_{i1}) + \hat{I}_{C1}\cos(\omega_{ac}t + \theta_{C1}) + \frac{M\hat{I}_1}{4}\cos(2\omega_{ac}t + \theta_{i1} + \theta_{ac}). \quad (3.33)$$

Fig. 3.7(a) shows the arm current i, the capacitor current i_C and its approximated value $\tilde{i}_C$ using only dc, fundamental ac, and second harmonic components (shown by the red dashed line), when the arm current has the same phase shift as the arm voltage. Fig. 3.8(a) shows the respective normalized harmonic spectrum of Figs. 3.7(a). Fig. 3.7(b) shows another case when the arm current is 180^o out of phase from the arm voltage. It is obvious that the average value of the capacitor current may contain a dc component as the phase shift of the arm current varies and may cause a problem for the capacitor average voltage. The dc component of the capacitor current is not only defined by the first two terms of the right-hand side of (3.29), but may also come from the combination

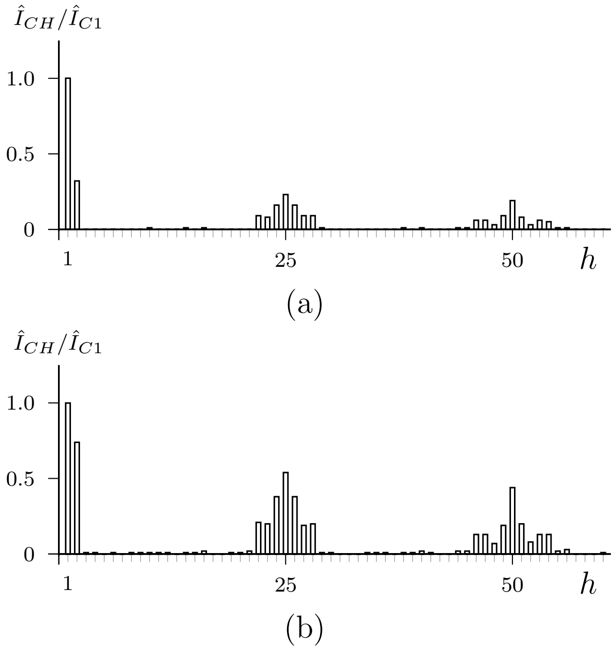


Fig. 3.8: Normalized harmonic spectrum of the capacitor current from Fig. 3.7. (a) For $\theta_{ac} - \theta_{i1} = 0$. (b) For $\theta_{ac} - \theta_{i1} = \pi$.

of the ratio of the carrier frequency to the ac frequency of the reference (ω_{cr}/ω_{ac}), and the harmonic indexes m, n, and l in (3.28).

3.3.3 Capacitor Voltage Fluctuation on a Chopper Cell

The dc-side voltage of the chopper cell should be maintained constant around the rated voltage throughout the operation of the chopper cell. Ideally, the dc-side voltage of the chopper cell should not contain any ripple voltage as in the case of using a dc voltage source. However, in applications where a capacitor is used instead of a dc voltage source, fluctuation of the voltage may happen and should be limited to some degree. A small voltage ripple on the capacitor voltage means that the life expectancy of the capacitor can be longer as compared to the capacitor voltage with a higher voltage ripple. It can also mean that for the same life expectancy, the capacitance of the capacitor can be made smaller thus saving cost and space. For that reason, it is important that the capacitor voltage fluctuation be known analytically before designing an actual converter system that contains many chopper cells.

The capacitor voltage in Fig. 3.4 can be described simply as

$$v_C = v_{C0} + \frac{1}{C}\int i_C \, dt, \tag{3.34}$$

where v_{C0} and C are the initial voltage and the capacitance of the capacitor, respectively. From (3.28) and (3.34), the capacitor voltage can be written as

$$\begin{aligned}
v_C = {} & v_{C0} + \frac{I_{dc}}{2C}t + \frac{MI_{dc}}{2C\omega_{ac}}\sin(\omega_{ac}t + \theta_{ac}) + \sum_{l=1}^{\propto}\frac{\hat{I}_l}{2lC\omega_{ac}}\sin\left(l\omega_{ac}t + \theta_{il}\right) \\
& + \sum_{l=1}^{\propto}\frac{M\hat{I}_l}{4(l-1)C\omega_{ac}}\sin\big((l-1)\omega_{ac}t + \theta_{il} - \theta_{ac}\big) \\
& + \sum_{l=1}^{\propto}\frac{M\hat{I}_l}{4(l+1)C\omega_{ac}}\sin\big((l+1)\omega_{ac}t + \theta_{il} + \theta_{ac}\big) \\
& + \frac{2I_{dc}}{\pi C}\sum_{m=1}^{\propto}\sum_{n=-\propto}^{\propto}\frac{J_n\left(\frac{m\pi M}{2}\right)\sin\left(\frac{\pi}{2}(m+n)\right)}{m^2\omega_{cr} + mn\omega_{ac}}\sin\left((m\omega_{cr} + n\omega_{ac})t + m\theta_{cr} + n\theta_{ac}\right) \\
& + \frac{1}{\pi C}\sum_{m=1}^{\propto}\sum_{n=-\propto}^{\propto}\sum_{l=1}^{\propto}\frac{\hat{I}_l J_n\left(\frac{m\pi M}{2}\right)\sin\left(\frac{\pi}{2}(m+n)\right)}{m^2\omega_{cr} + m(n-l)\omega_{ac}} \\
& \times \sin\Big(\big(m\omega_{cr} + (n-l)\omega_{ac}\big)t + m\theta_{cr} + n\theta_{ac} - \theta_{il}\Big) \\
& + \frac{1}{\pi C}\sum_{m=1}^{\propto}\sum_{n=-\propto}^{\propto}\sum_{l=1}^{\propto}\frac{\hat{I}_l J_n\left(\frac{m\pi M}{2}\right)\sin\left(\frac{\pi}{2}(m+n)\right)}{m^2\omega_{cr} + m(n+l)\omega_{ac}} \\
& \times \sin\Big(\big(m\omega_{cr} + (n+l)\omega_{ac}\big)t + m\theta_{cr} + n\theta_{ac} + \theta_{il}\Big).
\end{aligned} \tag{3.35}$$

Equation (3.35) shows a very complex mathematical expression when the arm current is assumed to be containing all of the frequency components and a dc component. When only the dc and fundamental ac components are considered in the arm current, the equation can be simplified as follows:

$$\begin{aligned}
v_C = {} & v_{C0} + \frac{1}{2C}\left(I_{dc} + \frac{M\hat{I}_1}{2}\sin(\theta_{ac} - \theta_{i1})\right)t + \hat{V}_{C1}\sin(\omega_{ac}t + \theta_{C1}) \\
& + \frac{M\hat{I}_1}{8C\omega_{ac}}\sin(2\omega_{ac}t + \theta_{i1} + \theta_{ac}) + v_{CH}.
\end{aligned} \tag{3.36}$$

where $\hat{V}_{C1}$ is the magnitude of the fundamental ac component of the capacitor voltage, and v_{CH} is the switching harmonic components of the capacitor voltage, and can be written as follows:

$$\hat{V}_{C1} = \frac{\hat{I}_{C1}}{C\omega_{ac}} = \frac{1}{2C\omega_{ac}}\sqrt{(MI_{dc})^2 + \left(\hat{I}_1\right)^2 + 2MI_{dc}\hat{I}_1\cos(\theta_{ac} - \theta_{i1})}, \tag{3.37}$$

$$
\begin{aligned}
v_{CH} = {} & \frac{2I_{dc}}{\pi C} \sum_{m=1}^{\propto} \sum_{n=-\propto}^{\propto} \frac{J_n\left(\frac{m\pi M}{2}\right) \sin\left(\frac{\pi}{2}(m+n)\right)}{m^2\omega_{cr} + mn\omega_{ac}} \sin\left((m\omega_{cr} + n\omega_{ac})t + m\theta_{cr} + n\theta_{ac}\right) \\
& + \frac{\hat{I}_1}{\pi C} \sum_{m=1}^{\propto} \sum_{n=-\propto}^{\propto} \frac{J_n\left(\frac{m\pi M}{2}\right) \sin\left(\frac{\pi}{2}(m+n)\right)}{m^2\omega_{cr} + m(n-1)\omega_{ac}} \\
& \times \sin\Big(\big(m\omega_{cr} + (n-1)\omega_{ac}\big)t + m\theta_{cr} + n\theta_{ac} - \theta_{i1}\Big) \\
& + \frac{\hat{I}_1}{\pi C} \sum_{m=1}^{\propto} \sum_{n=-\propto}^{\propto} \frac{J_n\left(\frac{m\pi M}{2}\right) \sin\left(\frac{\pi}{2}(m+n)\right)}{m^2\omega_{cr} + m(n+1)\omega_{ac}} \\
& \times \sin\Big(\big(m\omega_{cr} + (n+1)\omega_{ac}\big)t + m\theta_{cr} + n\theta_{ac} + \theta_{i1}\Big) . \qquad (3.38)
\end{aligned}
$$

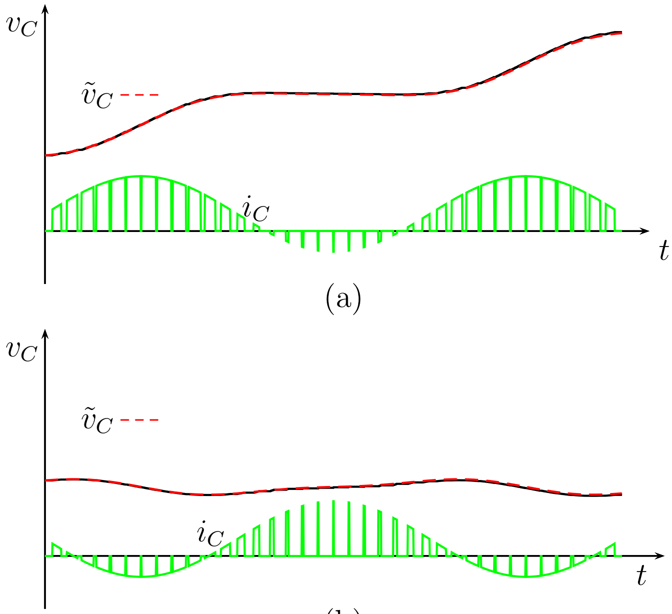
From (3.36) and (3.37), it can be seen that the dc and fundamental ac components of the capacitor voltage depend on the modulation index M, the phase shift between the arm-side voltage and current $\theta_{ac} - \theta_{i1}$, and the dc component I_{dc} and fundamental ac component $\hat{I}_1$ in the arm current. The second term of the right-hand side of (3.29) and (3.33) determine the stability of the capacitor average voltage since it may cause a gradual deviation from the desired capacitor voltage. Therefore, these two terms should be equal to zero as to maintaining a stable capacitor voltage:

$$
I_{dc} = -\frac{M\hat{I}_1}{2} \cos(\theta_{ac} - \theta_{i1}). \qquad (3.39)
$$

Applying (3.39) to (3.33), the second term of the right-hand side of (3.36) disappears, and the capacitor average voltage then becomes

$$
\bar{v}_C = v_{C0}. \qquad (3.40)
$$

Fig. 3.9 shows the capacitor voltage waveforms when different capacitor currents, as in Fig. 3.7, are applied to the capacitor. It can be easily noticed that the capacitor voltage may get unstable, either rising up or falling down, and depends heavily on the capacitor current. When the capacitor current contains no dc component, as shown in Fig. 3.9(b), the average value of the capacitor voltage can be maintained naturally assuming that there is no disturbances in the capacitor. However, for practical reason, the capacitor voltage may drift gradually although only ac components exist in the capacitor current. This issue should be considered when designing the control system.



(a)

(b)

Fig. 3.9: Capacitor voltage waveforms corresponding to the respective capacitor currents from Fig. 3.7. (a) For $\theta_{ac} - \theta_{i1} = 0$. (b) For $\theta_{ac} - \theta_{i1} = \pi$.

The approximated value of the capacitor voltage $\tilde{v}_C$, shown by the red dashed lines, are derived from the approximated capacitor current $\tilde{i}_C$ from Fig. 3.7 as follows:

$$\begin{aligned} v_C \approx \tilde{v}_C = v_{C0} + \frac{1}{2C}\left(I_{dc} + \frac{M\hat{I}_1}{2}\sin(\theta_{ac} - \theta_{i1})\right) t + \hat{V}_{C1}\sin(\omega_{ac}t + \theta_{C1}) \\ + \frac{M\hat{I}_1}{8C\omega_{ac}}\sin(2\omega_{ac}t + \theta_{i1} + \theta_{ac}). \end{aligned} \tag{3.41}$$

It can be seen from Fig. 3.9 that the approximated capacitor voltages are well matched with the actual capacitor voltages although the harmonic components are excluded from the equation. It is, however, not the general case, especially when the carrier frequency is set to be lower and close to the fundamental frequency.

Fig. 3.10(a) shows the harmonic spectrum of the capacitor voltage in Fig. 3.9(b), whereas Fig. 3.10(b) shows the harmonic spectrum of the capacitor voltage when the carrier frequency is decreased to $\omega_{cr} = 5\omega_{ac}$. As the carrier frequency gets closer to the fundamental frequency, the sideband harmonics of the capacitor current and voltage will eventually coincide with the fundamental frequency, and may even produce dc and sub-

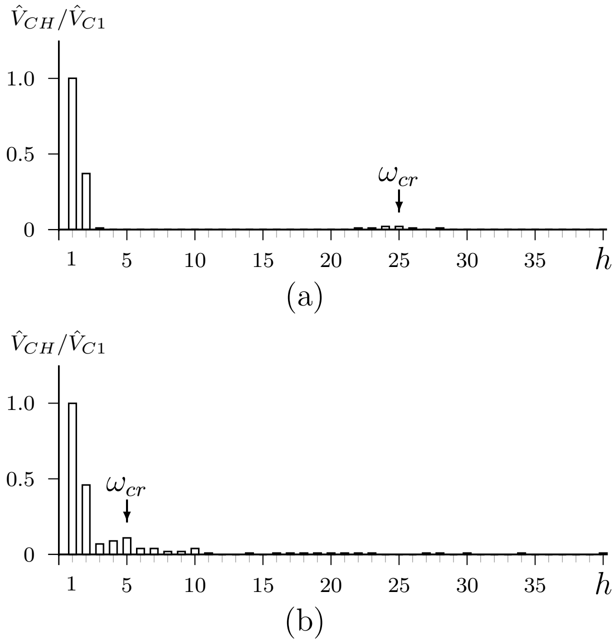


Fig. 3.10: Normalized harmonic spectrum of the capacitor voltage. (a) For $\omega_{cr} = 25\omega_{ac}$. (b) For $\omega_{cr} = 5\omega_{ac}$.

harmonic components. The fundamental frequency component of the capacitor voltage is not only influenced by the dc and fundamental ac components of the capacitor current but also by the sideband harmonics of the capacitor current.

3.3.4 Phase-Shifted-Carrier PWM

The PSC-PWM method assigns a triangular carrier signal for each chopper cell in the DSCC converter. Let $F_{tri}(t)$ be a triangular function that has unity amplitude, and f_{cr} be the frequency of the carrier signal. The mathematical description of the carrier signal v_{cr} can be described as follows:

$$v_{cr} = F_{tri}(\omega_{cr}t + \theta_{cr}), \tag{3.42}$$

where θ_{cr} represent the phase shift of the carrier signal to an arbitrary point in time.

Fig. 3.11 illustrates the carrier waveforms in a PSC-PWM-based DSCC converter consisting of 16 cells per leg. The carrier signals in each arm of the DSCC are phase-shifted each other by $4\pi/N$. For instance, if (3.42) is assigned to a chopper cell in an arm of the DSCC, the two adjacent chopper cells in series have carrier phase shifts of

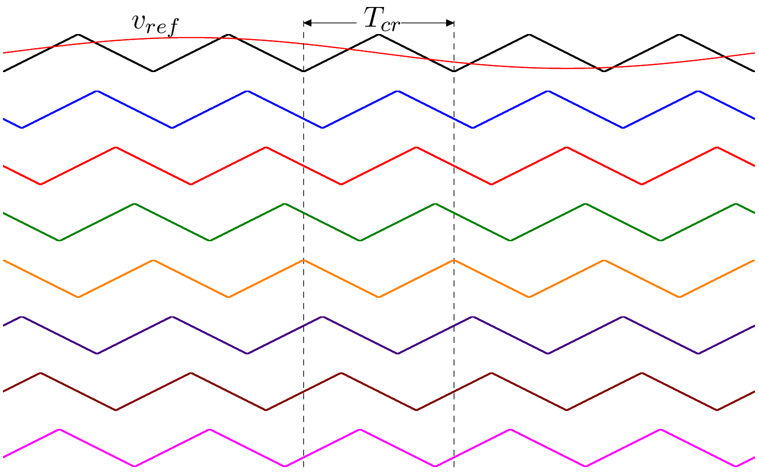


Fig. 3.11: Eight triangular carrier waveforms in the PSC-PWM for chopper cells within an arm of a 16-cell DSCC converter.

$\theta_{cr} + 4\pi/N$ and $\theta_{cr} - 4\pi/N$. The carrier phase shift between the upper and lower arms in each phase leg is $2\pi/N$ to achieve voltage harmonic cancellation. The arm voltage of a DSCC converter that has N chopper cells per leg can be expressed as

$$\begin{aligned} v_{arm} = &\frac{NV_C}{4} + \frac{NV_C}{4} M \cos(\omega_{ac}t + \theta_{ac}) \\ &+ \frac{NV_C}{\pi} \sum_{m=\frac{Ni}{2}}^{\infty} \sum_{n=-\infty}^{\infty} \frac{1}{m} J_n \left(m\frac{\pi}{2} M \right) \sin\left((m+n)\frac{\pi}{2} \right) \\ &\times \cos\left(m\omega_{cr}t + n\omega_{ac}t + n\theta_{ac} \right), \end{aligned} \tag{3.43}$$

where V_C is the nominal capacitor voltage in each chopper cell, i is an integer number. Equation (3.43) shows that the carrier harmonic components are exist only for odd multiples of m $(= Ni/2)$, while the sideband harmonics are exist only for even number of n when m is an odd number; and odd number of n when m is an even number. When the number of chopper cells per arm $N/2$ is set to an even number, the harmonics in the arm voltage v_{arm} contains only odd sideband harmonic components around even multiples of $\omega_{cr} \times N/2$ without carrier harmonic components.

A major advantage of the PSC-PWM combined with a closed-loop control is that the actual switching frequency of each chopper cell is equal to the carrier frequency regardless of operating conditions, circuit parameters, or control gains [98]. Note that the equivalent switching frequency for each leg is equal to $N \times f_{cr}$. Moreover, the circuit behavior can be easily determined and analyzed because the circuit configuration can be modeled as a *linear* and *continuous* system [112]–[114].

3.4 Control Method

3.4.1 Power Flow Control

The DSCC converter can be seen as a voltage source or a current source that can deliver/absorb the power to/from the ac grid, as shown in Fig. 3.2 for a single phase representation. The ac terminal of the DSCC converter v_u is connected to the ac-grid terminal v_{Su} through an inductance L. The inductance L has a role to support voltage difference between the DSCC converter and the ac grid. In a three-phase representation, the ac grid can be regarded as an ideal three-phase ac-voltage source that has phase voltages as follows:

$$v_{Su} = \sqrt{\frac{2}{3}} V_S \sin(\omega t + \theta_S), \tag{3.44}$$

$$v_{Sv} = \sqrt{\frac{2}{3}} V_S \sin(\omega t - \frac{2\pi}{3} + \theta_S), \tag{3.45}$$

$$v_{Sw} = \sqrt{\frac{2}{3}} V_S \sin(\omega t + \frac{2\pi}{3} + \theta_S), \tag{3.46}$$

where V_S is the rms value of the grid line-to-line voltage, $\omega = 2\pi f$ is the angular frequency of the grid, and θ_S is the initial voltage angle of the grid. From (3.6)–(3.8) and (3.44)–(3.46), the power flow between the ac grid and DSCC converter is given as follows:

$$P = \frac{V_S V}{\omega L} \sin(\theta_S), \tag{3.47}$$

$$Q = \frac{V_S V}{\omega L} \cos(\theta_S) - \frac{V_S^2}{\omega L}, \tag{3.48}$$

where P is the active power, Q is the reactive power, and θ_S is the voltage angle between the grid and the converter. Equations (3.47) and (3.48) applies only for a steady condition with the assumption of a very small line resistance ($R << X$).

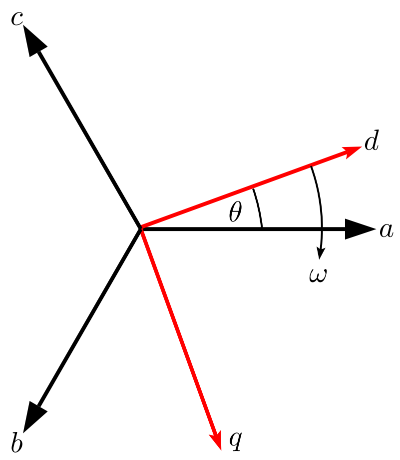


Fig. 3.12: The stationary abc-reference frame and the rotating dq-reference frame.

3.4.1.1 Rotating Reference Frame

From (3.6)–(3.8), (3.44)–(3.46), and Fig. 3.2, the voltage equations of the grid-connected converter system in a matrix form with the assumption of zero line resistance is given as follows:

$$\begin{bmatrix} v_{Su} \\ v_{Sv} \\ v_{Sw} \end{bmatrix} - \begin{bmatrix} v_u \\ v_v \\ v_w \end{bmatrix} = L\frac{d}{dt}\begin{bmatrix} i_u \\ i_v \\ i_w \end{bmatrix} \tag{3.49}$$

A three-phase ac system with three ac variables can be transformed into a dc system with two variables by using a direct-quadrature (dq) transformation. The transformation rotates the stationary reference frame of the three-phase ac system resulting in a rotating reference frame, or a dq-reference frame [141]. In other words, the ac voltages and currents in the three phase system can be changed into d-axis voltage and current, and q-axis voltage and current that have dc quantities.

Fig. 3.12 illustrates the rotating dq-reference frame with respect to the stationary abc-reference frame for the three-phase ac system. Note that each vector variable in the abc-reference frame represents the instantaneous value of a sinusoidal signal with an angular frequency of ω. The q-axis is lagging the d-axis by 90^o, as shown in Fig. 3.12. Because the dq-reference frame is rotating at the angular frequency of ω, the variables in the d-axis and q-axis become dc variables.

By using a transformation matrix C, the three phase voltages in (3.44)–(3.46) can be transformed into the rotating dq-reference frame as follows:

$$\begin{bmatrix} v_{Sd} \\ v_{Sq} \end{bmatrix} = [C] \begin{bmatrix} v_{Su} \\ v_{Sv} \\ v_{Sw} \end{bmatrix} \tag{3.50}$$

where $[C]$ is defined as follows

$$[C] = \sqrt{\frac{2}{3}} \begin{bmatrix} \sin(\theta) & \sin(\theta - \frac{2\pi}{3}) & \sin(\theta + \frac{2\pi}{3}) \\ \cos(\theta) & \cos(\theta - \frac{2\pi}{3}) & \cos(\theta + \frac{2\pi}{3}) \end{bmatrix} \tag{3.51}$$

By using a similar transformation as in (3.50), (3.49) can be transformed into the dq-reference frame as follows:

$$\begin{bmatrix} v_{Sd} - v_d \\ v_{Sq} - v_q \end{bmatrix} = L\frac{d}{dt} \begin{bmatrix} i_d \\ i_q \end{bmatrix} + \begin{bmatrix} 0 & -\omega L \\ \omega L & 0 \end{bmatrix} \begin{bmatrix} i_d \\ i_q \end{bmatrix} \tag{3.52}$$

The instantaneous active and reactive power at the ac grid terminals can be represented in the dq-reference frame as follows:

$$\begin{bmatrix} p \\ q \end{bmatrix} = \begin{bmatrix} v_{Sd} & v_{Sq} \\ v_{Sq} & -v_{Sd} \end{bmatrix} \begin{bmatrix} i_d \\ i_q \end{bmatrix} \tag{3.53}$$

where p and q are the instantaneous active and reactive power, respectively. If the ac-grid terminal voltages are set as the reference voltages for the dq-reference frame, the q-axis voltage component of the ac grid terminal always has a zero value. The power equations become as follows:

$$p = v_{Sd} i_d, \tag{3.54}$$

$$q = -v_{Sd} i_q. \tag{3.55}$$

3.4.1.2 Decoupled Current Control

Equations (3.54) and (3.55) reveal that the instantaneous active power control of the converter to (or from) the grid can be achieved by controlling the d-axis current component i_d. Likewise, the instantaneous reactive power q can be regulated by controlling the q-axis current component i_q. However, equation (3.52) shows that the grid-connected converter system contains a cross coupling component ωL between d-axis and q-axis. That is to say, the d-axis voltage is affected by the q-axis current, and the q-axis voltage is affected by the d-axis current. As a result, i_d (or i_q) cannot be controlled simply by adjusting the d-axis (or $q - axis$) voltage component of the converter. For instance, to produce i_d, v_d will also be affected by the d-axis voltage component of the ac grid, v_{Sd}, and the cross coupling from the q-axis current component, $\omega L i_q$. Therefore, the active (or reactive) power cannot be controlled independently if the power-flow controller uses a voltage control scheme.

To regulate the instantaneous active and reactive power independently, a current control equipped with a feedforward control can be used. This feedforward control is commonly known as the decoupled current control. It cancels out the cross coupling between d and q axes. Thus, the decoupled current control can regulate the instantaneous active power p by simply controlling the d-axis current component, i_d. Likewise, to regulate the instantaneous reactive power q, only the q-axis current component, i_q, need to be controlled.

Fig. 3.13 shows the decoupled current control that can be implemented into the DSCC converter to achieve power flow control. Since the decoupled control method needs a voltage reference for synchronization, the phase voltages (or line-to-line voltages) of the ac-grid terminals should be measured for feedback purpose. Because the current components in d-axis and q-axis are dc variables, the decoupled current control can use a proportional-integral (PI) controller for each of the current components. To produce the ac-voltage commands for the DSCC converter (v_u^*, v_v^*, and v_w^*), the decoupled current control requires dq-current commands (i_d^* and i_q^*), a feedforward control from the ac-grid voltages (v_{Su}, v_{Sv}, and v_{Sw}), and a feedback from the ac-link currents (i_u, i_v, i_w). The d-axis current command corresponds to the active-power command p^* plus the overall capacitor-voltage control command Δi_d^*, which is discussed in the next section. The q-axis current command corresponds to the reactive-power command q^*.

3.4.2 Capacitor Voltage Balancing Control

Controlling the voltages of the floating dc capacitors in the DSCC converter is one of the common issues to be solved. The capacitor voltage in each chopper cell may deviate from the desired nominal value because of the disturbances such as parasitic resistances, transients, and harmonics. An appropriate control method should be applied to regulate

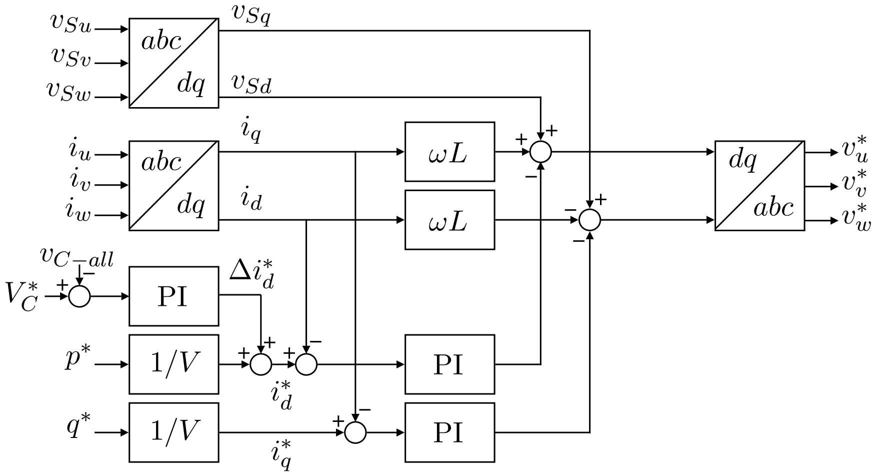


Fig. 3.13: Control block diagram of the decoupled current control including the overall capacitor-voltage control.

the capacitor voltages so as to make the DSCC converter stable. The PSC-PWM-based DSCC converter discussed in this dissertation utilizes a three-layer hierarchical control to balance the capacitor voltages:

- Overall capacitor-voltage control.
- Circulating current control.
- Individual balancing control.

3.4.2.1 Overall capacitor-voltage control

The overall capacitor-voltage control in the top layer takes the responsibility to regulate the mean voltage of all the capacitors to its reference v_C^*. Adjusting a small amount of active power supplied from the ac mains makes it possible to regulate the arithmetical average voltage of all the capacitors, which is given by

$$v_C = \frac{1}{3N}\sum_{j=1}^{N}\sum_{x=u,v,w} v_{Cjx}, \tag{3.56}$$

where N is the number of chopper cells per leg. The adjusted active power corresponds to the whole power loss of the DSCC converter. In other words, the overall capacitor-voltage control compensates a slight power difference between the ac side and dc side.

The active current produced by the control, Δi_d^*, is then incorporated in the decoupled current control as shown in Fig. 3.13.

3.4.2.2 Circulating Current Control

The circulating current control in the middle layer plays an important role in balancing the energy in the three legs. It consists of two distinct balancing controls, that is, the leg-balancing control and arm-balancing control. The leg-balancing control uses the dc component of the circulating current in each leg to exchange a small amount of active power among the three legs. The arm-balancing control the fundamental (50 Hz) ac component of the circulating current to adjust the active-power difference between the upper and lower arms in each leg. It is responsible for balancing six mean voltages, each of which is the mean voltage of $N/2$ capacitors per arm.

The leg- and arm-balancing controls can be described from the power flow in the DSCC circuit. Since the upper- and lower-arm voltages have dc and ac components, by assuming that the circulating current i_{Zu} also contains ac components, then the upper- and lower-arm average power also have dc and ac part as follows:

$$\begin{aligned} P_{Pu} &= \int_{t_0}^{t_0+T} v_{Pu} i_{Pu}\, dt \\ &= \frac{VI\cos\theta}{2\sqrt{3}} + \frac{V_{dc}I_{Z0}}{2} - \frac{VI_{Z1}}{\sqrt{3}}, \qquad (3.57) \\ P_{Nu} &= \int_{t_0}^{t_0+T} v_{Nu} i_{Nu}\, dt \\ &= \frac{VI\cos\theta}{2\sqrt{3}} + \frac{V_{dc}I_{Z0}}{2} + \frac{VI_{Z1}}{\sqrt{3}}, \qquad (3.58) \end{aligned}$$

where V, I, and θ are the line-to-line rms voltage, the line rms current and the power factor angle respectively, while I_{Z0} and I_{Z1} are dc and fundamental ac component of the circulating current respectively. The first term of each equation above is related to ac power, the second term is related to dc power and the third term is related to the circulating power in each arm. Note that the dc power within one leg is directly related to the dc component of the circulating current. The total dc power is equal to the summation of dc powers in all legs. By controlling the dc term of the circulating

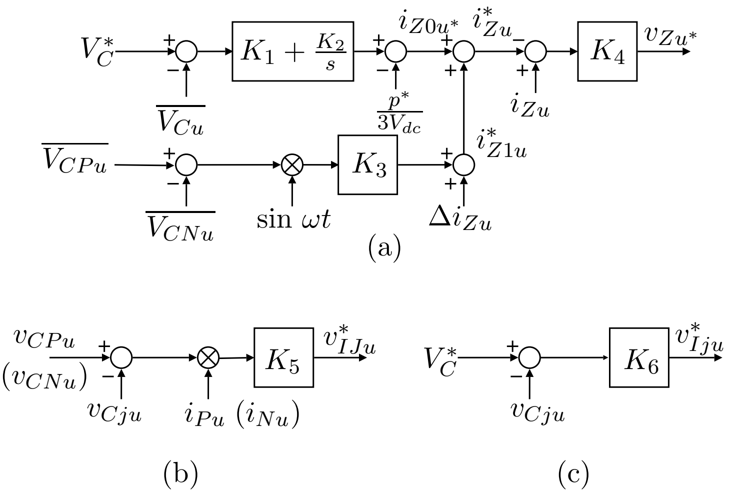


Fig. 3.14: Control block diagram for balancing the capacitor voltages.

current, we can regulate the average capacitor voltage in each leg [101].

Because of the circuit topology nature, the ac power fluctuates between the upper and lower arms and can cause imbalance in each arm capacitor voltage. This problem can be solved by controlling the third term of (3.57) and (3.58), that is, by controlling the fundamental ac component of the circulating current which has the same phase as the ac-terminal voltage.

Fig. 3.14(a) shows the control block diagram of the circulating current control. The leg-balancing control uses the dc component of the arithmetical average voltage of the capacitors in each leg (for instance, $\overline{V_{Cu}}$ for u phase) as a feedback. It can be obtained by using a filter, such as a moving-average filter (MAF). Likewise, the arm-balancing control uses the dc component of the arithmetical average voltage of the capacitors in the two arms within each leg, $\overline{V_{CPu}}$ and $\overline{V_{CNu}}$. Because the arm-balancing control adjust the fundamental ac component of the circulating current, the voltage difference between $\overline{V_{CPu}}$ and $\overline{V_{CNu}}$ should be multiplied with a sinusoidal signal that has the same phase as the ac-terminal voltage.

In a balanced three-phase system, the amplitude of the fundamental ac component of the circulating current that is flowing in each phase leg is equal to each other ($I_{Z1u} = I_{Z1v} = I_{Z1w}$), resulting in the following equation:

$$\hat{i}_{Z1u} + \hat{i}_{Z1v} + \hat{i}_{Z1w} = 0, \tag{3.59}$$

note that $\hat{i}_{Z1u}$ represents the current command from the voltage difference between $\overline{V_{CPu}}$ and $\overline{V_{CNu}}$. The fundamental ac component of the circulating current in a phase leg is likely to be unequal to the other phase legs due to imperfections and dynamic of the DSCC converter system. The fundamental ac component of the circulating current in u phase depends on the energy imbalance between the upper arm and lower arm of u phase. Likewise, the fundamental current component of the circulating current in v phase depends on the energy imbalance between the upper arm and lower arm of v phase. Therefore, (3.59) may not apply in actual operation of the DSCC converter. This imbalanced condition results in producing an fundamental ac component on the circulating current that flows trough the dc side, which is undesirable.

Therefore, other fundamental ac component should be added in addition to the current command $\hat{i}_{Z1u}$. Equation (3.59) can be modified to prevent an ac current component flowing through the dc side as follows:

$$\hat{i}_{Z1u} + \hat{i}_{Z1v} + \hat{i}_{Z1w} + \Delta i_{Z1u} + \Delta i_{Z1v} + \Delta i_{Z1w} = 0. \tag{3.60}$$

The new terms (Δi_{Z1u}, Δi_{Z1v}, and Δi_{Z1w}) represent cross-coupling components of the circulating current. To obtain the cross-coupling component for the u phase, Δi_{Z1u}, the fundamental ac currents from the other two phases can be used. However, the currents should not interfere with the active power exchange between the upper and lower arms in their respective phases. Therefore, they should be in the form of reactive currents that have 90^o phase shift from the fundamental ac current components ($\hat{i}_{Z1v}$ and $\hat{i}_{Z1w}$). The cross-coupling components for v and w phases can be obtained similarly.

Fig. 3.15 explains how to generate the cross-coupling components of the circulating current. The fundamental ac component of the u-phase circulating current that has 180^o phase shift from $\hat{i}_{Z1u}$ produces the cross-coupling components to the other two phases, as shown in Fig. 3.15(a). On the other hand, the cross-coupling component to the u phase can be obtained from the summation of the fundamental ac components of the v- and w-phase circulating currents that have 180^o phase shift from $\hat{i}_{Z1v}$ and $\hat{i}_{Z1w}$, respectively, as shown in Fig. 3.15(b).

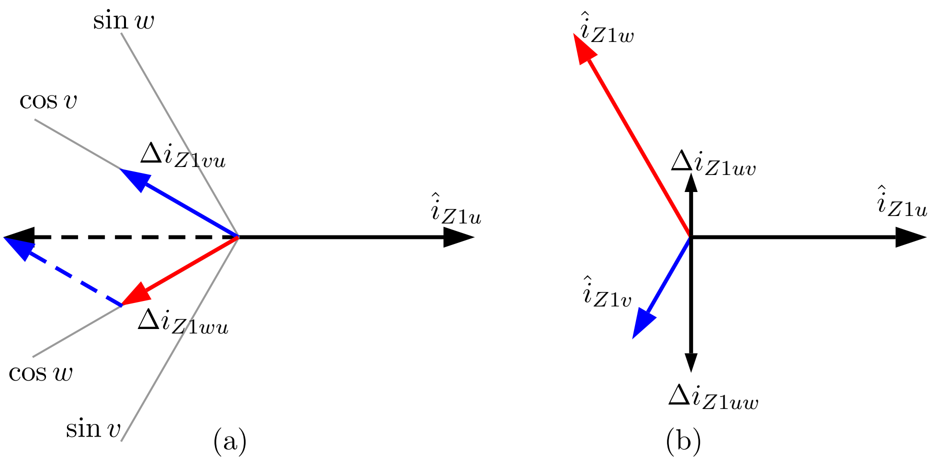


Fig. 3.15: Vector diagram of the cross-coupling component. (a) The cross-coupling components from the u phase to v and w phases. (b) The cross-coupling component to the u phase generated from v and w phases.

3.4.2.3 Individual Balancing Control

The individual balancing control residing in the bottom layer takes charge of regulating each capacitor voltage to the mean voltage of $N/2$ capacitors per arm. This straightforward control adjusts the active power formed by the arm-side voltage of each chopper cell and the arm current. A digital low-pass filter, such as the MAF, is necessary for the individual balancing control in order to extract the dc component from each capacitor voltage that contains ac frequency components. The interaction of the arm-side voltage of each chopper cell and the arm current may produce a small dc current component on the capacitor resulting in dc voltage deviation on the capacitor. The individual balancing control has the ability to cancel out such a small dc current, thus making the DSCC converter stable. However, the individual balancing control cannot be made too large to prevent overmodulation on the chopper cells.

To ensure each capacitor voltage within one arm is equal to the average value, the individual capacitor control has to be applied. When the arm current flows into the cell, the capacitor will be charged if the cell is activated. Likewise, when the arm current flows out from the cell, the capacitor will be discharged if the cell is activated. The arm current will not flow into or out from the capacitor if the cell is turned off, thus no charging/discharging condition occurs. By using these condition states as a rule, the capacitor voltage in each cell can be maintained at the desired value. Fig. 3.14(b) shows the individual-balancing-control block diagram when the converter is controlling the current on the power transfer. Fig. 3.14(c) shows individual-balancing-control block diagram when the converter is not controlling the power flow on the circuit, that is, it acts as only a voltage source.

The arm-side voltage command for each cell in the upper arm of u-phase (for $j : 1 \sim \frac{n}{2}$) is given by

$$v_{ju}^{*} = v_{FF} - \frac{2v_{u}^{*}}{n} + v_{Zu}^{*} + v_{Iju}^{*}. \tag{3.61}$$

With similar derivation, the voltage command for each cell in the lower arm of u-phase (for $j : \frac{n}{2} + 1 \sim n$) is given by

$$v_{ju}^{*} = v_{FF} + \frac{2v_{u}^{*}}{n} + v_{Zu}^{*} + v_{Iju}^{*}, \tag{3.62}$$

where v_{FF} is the feedforward control to maintain the voltage at the dc side which is equal to V_{dc}/n; v_{u}^{*} is the power control output; v_{Zu}^{*} is the circulating-current-control output; and v_{Iju}^{*} is the individual balancing control output. Each cell voltage command should then be normalized to the capacitor voltage for generating the chopper cell modulation index M.

3.5 Summary

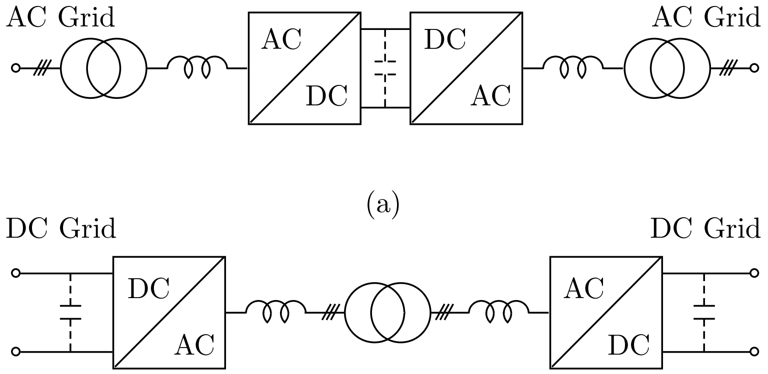
This chapter has discussed the operating principles of the DSCC converter based on PSC-PWM and a hierarchical control method for capacitor balancing. The circuit operation explained in this chapter gives an overview to the circulating current and power flow in one leg of the converter. The harmonic contents of the capacitor voltage can be derived based on the arm current and the arm-side PWM voltage of a chopper cell in a leg of DSCC converter. The capacitor balancing control method is obtained linearly based on the circuit equation, and hence a simple PI controller can be used to regulate the capacitor fluctuation.

Chapter 4

A Front-To-Front System Based on DSCC Converters

4.1 Introduction

This chapter discusses a high-power front-to-front (FTF) system application consisting of a couple of three-phase modular multilevel double-star chopper-cells (DSCC) converters and a single three-phase ac-link transformer. The circuit configuration and the control strategy of the FTF system are described. This chapter designs, constructs, and tests a three-phase downscaled DSCC-based FTF system rated at 400 Vdc and 10 kW using a low frequency ratio of 5/2, where the carrier frequency is 450 Hz, and the ac-link frequency is 180 Hz. Moreover, experiments are carried out with the same carrier frequency as 450 Hz but at different ac-link frequency of 112.5 Hz, where the carrier frequency is exactly an integer multiple of the ac-link frequency. This chapter also includes simulated waveforms under the same circuit parameters and control gains as the experimental ones to enhance the reliability and validity of both experiment and simulation system. Later in this chapter, reactive power compensation methods are presented to prevent overvoltage issue in the FTF system.



(a)

(b)

Fig. 4.1: Basic configurations. (a) A back-to-back (BTB) system between two ac grids. (b) A front-to-front (FTF) system between two dc grids.

4.2 FTF Configuration

4.2.1 BTB and FTF Systems

One of typical applications of DSCC converters to grid connections is a back-to-back (BTB) system, [104],[106],[107],[117] as shown in Fig. 4.1(a). The BTB system can be used as an interface between two ac grids. It can act practically as a frequency changer, an asynchronous power-flow controller, or a bidirectional ac-to-dc or dc-to-ac power converter in a long-distance high-voltage dc current (HVDC) system. Fig. 4.1(b) shows a front-to-front (FTF) system that is characterized by the combination of two bidirectional power converters with a single ac-link transformer, as opposed to the BTB system. Modern DSCC converters as well as conventional two-level or three-level voltage-source converters are applicable to the FTF system. The dc-link capacitors indicated by the broken lines in Fig. 4.1 are indispensable when the conventional voltage-source converters are used. However, it can be eliminated from both BTB and FTF systems when a pair of DSCC converters are used, thus resulting in reducing the size and weight, as well as in improving system reliability.

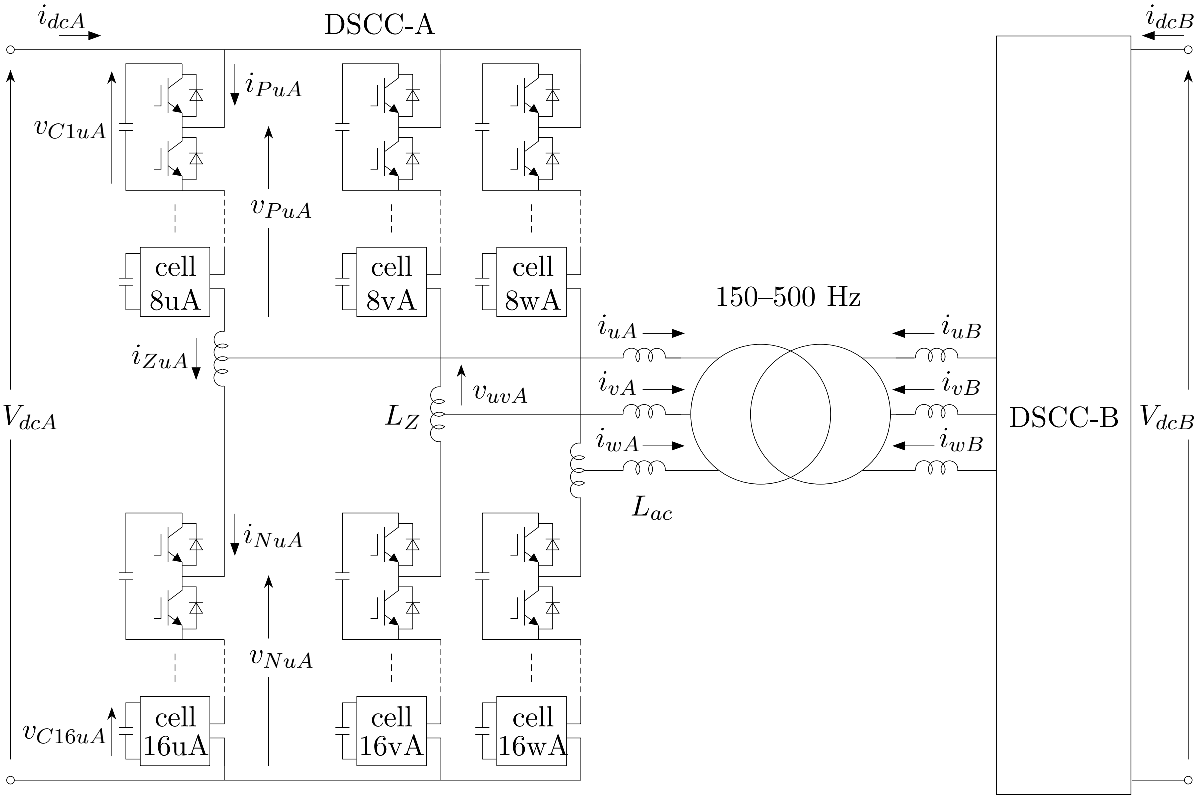


Fig. 4.2: Circuit diagram of an FTF system consisting of two 16-cell DSCC converters and an ac-link transformer.

4.2.2 DSCC-Based FTF System

Fig. 4.2 shows the basic circuit diagram of an FTF system using two DSCCs with 16 chopper-cells per phase leg. Two three-phase DSCCs are connected together at their ac sides via a single three-phase transformer for galvanic isolation and voltage matching. Each phase leg consists of series-connected chopper-cell circuits and a center-tapped inductor. The number of chopper cells in each DSCC converter can be adjusted to withstand the respective system voltage at their dc sides. In this case, the high-voltage-side DSCC converter requires more chopper cells than the low-voltage-side DSCC converter to withstand high-voltage dc grid.

Power converters used for grid connections usually share their respective ac or dc terminals with other converters to create a common ac or dc link. When an FTF system is applied to two dc grids, the coupling of one dc grid with the other is done through an intermediary ac-link transformer for galvanic isolation and voltage matching. This configuration can be expanded to use multiple converters connected to the same ac link, creating the so-called “multiterminal dc-grid interconnection.” Since the dc voltages are not directly coupled, a dc fault on one feeder does not propagate directly to the others. Fast switching operation of the converters used in the FTF system can isolate the faulty feeder from the other healthy feeders. The operation of the FTF system on the power collection and under fault condition will be discussed in Chapter 5.

For dc-power collection and transmission applications such as distributed dc-power generators, an FTF system has collecting-side converters and a transmission-side converter. For multiple collecting-side DSCCs operation, the number of chopper cells in each converter may differ, depending on the power rating of each converter. Thus, the transmission-side DSCC converter should be equal to the total rated power of the collecting-side DSCCs. Considering that the ac-link voltages nearly resemble sinusoidal waveforms for a large number of chopper cells, the interface inductors can be made smaller, thus reducing the size and cost. Since the dc voltage of each collecting-side feeder is independent, the FTF system offers a flexible dc-power collection. This feature enables the use of apparatus with different voltage ratings. Moreover, the ac-link voltage and frequency in the system can be adjusted freely as desired. Medium frequency operation at the ac link makes the size and weight of the transformers, inductors, and capacitors more compact and lighter as compared to the 50-Hz frequency operation, thus saving the available space and also the cost. This scheme can be advantageous when a cost-effective uncontrolled rectifier is used with an ac generator to produce a dc voltage in a wind turbine generator of an offshore wind farm.

4.3 Control Strategy

Similar to other voltage-source converters, a DSCC converter can act as an inverter, or a rectifier, to release or absorb power to, or from, the ac link, respectively. Regulating a mean dc voltage of many floating dc capacitors in the DSCC converter is one of the common issues to be solved. The mean dc voltage in each individual chopper cell may deviate from the desired value because of disturbances such as parasitic resistances, transients, and harmonics. The aim of the control strategy for the FTF system is to control

Table 4.1: Master and slave control modes

Role	Control	Function	AC-Link Frequency
Master	Open-loop	Voltage source	Controllable
Slave	Closed-loop	Current source	Uncontrollable

the power flow while keeping individual mean dc voltages of all the capacitors within an allowable value. The hierarchical control method for capacitor voltage balancing, which has been discussed in detail in Chapter 3, will be used in the following experiments.

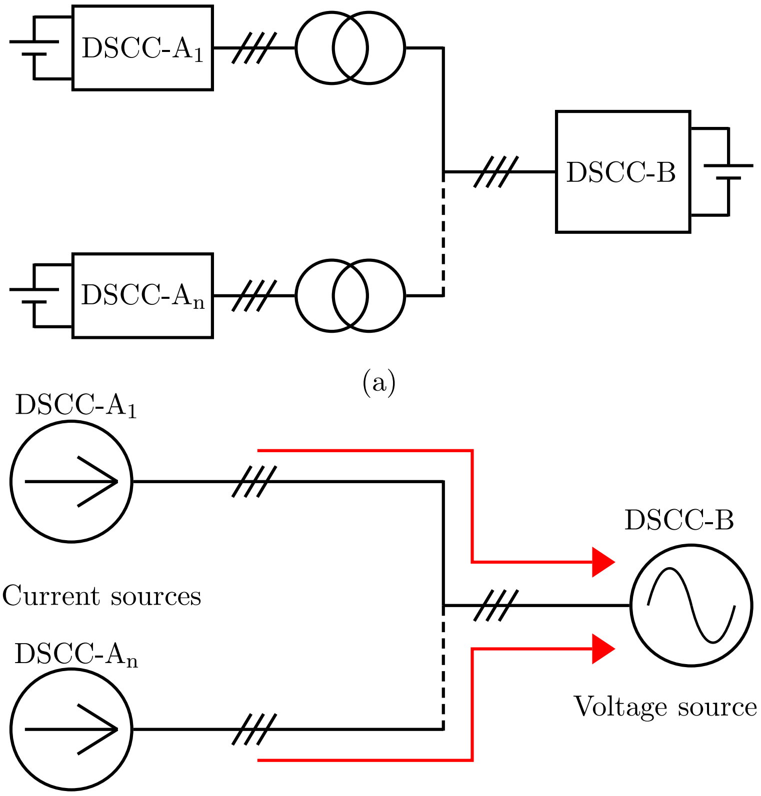
4.3.1 Master and Slave Control Modes

DSCC converters employed in an FTF system can be separated into a master converter and a slave converter. To work properly, the master converter should maintain the voltage and frequency of the ac link while the slave converter should control the power flow. This role assignment makes the master converter act as a voltage source, whereas the slave converter is assigned as a current source. Table 4.1 summarizes the differences in control mode between the master and slave converter. This strategy makes it easy to expand the FTF system to a multi-terminal interconnection, where several slave converters are connected to a single master converter.

Fig. 4.3 illustrates a multi-terminal FTF system and its equivalent circuit. This scheme is similar to a power system, where large power stations control the grid voltage and frequency, while smaller power generators should be synchronized to the grid when sending their respective power.

4.3.2 Power Flow Control

A decoupled current control as depicted in Fig. 3.13 can achieve a fast power flow control on a three-phase ac system. Since this control method needs a voltage reference for synchronization, the DSCC converter that uses the master mode should produce a voltage reference for the slave converter that controls the power flow. The ac-link voltage and frequency can be determined by feeding voltage references into the master converter.



(a)

(b)

Fig. 4.3: Power control in a multiterminal FTF system. (a) Circuit diagram. (b) Equivalent circuit.

The three-phase line-to-neutral voltage references in the master converter can be written as

$$v_u^* = \sqrt{\frac{2}{3}} V_{ac} \sin \omega t, \tag{4.1}$$

$$v_v^* = \sqrt{\frac{2}{3}} V_{ac} \sin(\omega t - \frac{2\pi}{3}), \tag{4.2}$$

$$v_w^* = \sqrt{\frac{2}{3}} V_{ac} \sin(\omega t + \frac{2\pi}{3}), \tag{4.3}$$

where V_{ac} is the line-to-line rms voltage at the ac side of the master converter, and ω is a desired angular frequency of the ac link. For the DSCC converter configuration, the maximum of the ac-link peak voltage depends on the dc link voltage, which is equal to $V_{dc}/2$. The frequency can be selected freely, depending on a compromise between the system size and the switching loss. For medium-/high-voltage high-power converters, the actual switching frequency or the carrier frequency should be set as low as possible to reduce the switching loss. On the other hand, using a low switching frequency may make the response time of the controller slow. The derived optimal carrier frequency discussed in [114] can be regarded as a compromise between the switching loss and the response time of the controller. This chapter discusses the power flow control of the FTF system using the derived optimal frequency ratios, where the carrier frequency is 450 Hz, and the ac-link frequencies are 180 Hz and 112.5 Hz.

While the master converter has the function of controlling the ac-link voltage and frequency, the slave converter plays an important role in adjusting power flow at the voltage and frequency. The power flow can be adjusted indirectly by controlling two independent currents on the rotating dq reference frames; the d-axis current for active power and the q-axis current for reactive power, respectively as shown in Fig. 3.13. Since ac voltage commands in (4.1)–(4.3) at the master converter are used as a feedforward input for the decoupled current control, only the three-phase ac-link currents of the slave converter should be detected to form a current feedback loop. Hence, neither phase-locked loop (PLL) circuit nor ac voltage sensor is required for the control system.

4.4 Experimental Setup

Fig. 4.4 illustrates the circuit configuration of the DSCC-based FTF system used in the following experiments. It uses an adjustable dc power supply for both dc sides, and the ac-link line-to-line rms voltage is set at 200 V. DSCC-A uses a slave-mode operation whereas DSCC-B uses a master-mode operation in the following discussions. Table 4.2 summarizes the parameters used in the circuit. Each converter circuit consists of 16 chopper cells per leg. A phase-shifted pulsewidth modulation (PWM) technique is applied to 16 triangular-carrier signals at a constant frequency of $f_{cr} = 450$ Hz, which are phase-shifted each other by 22.5°. With this technique, all chopper-cells will have equal switching and conduction power losses. Note that the equivalent switching frequency for each leg is 7.2 kHz ($= 16 \times f_{cr}$). The ac-link frequency f_{ac} is selected based on the optimum ratio derived in [114] to achieve switching-power-loss reduction.

The overall control system consists of single Texas Instruments TMS320C6713 digital signal processor (DSP), two Altera Cyclone II field-programmable gate array (FPGA)

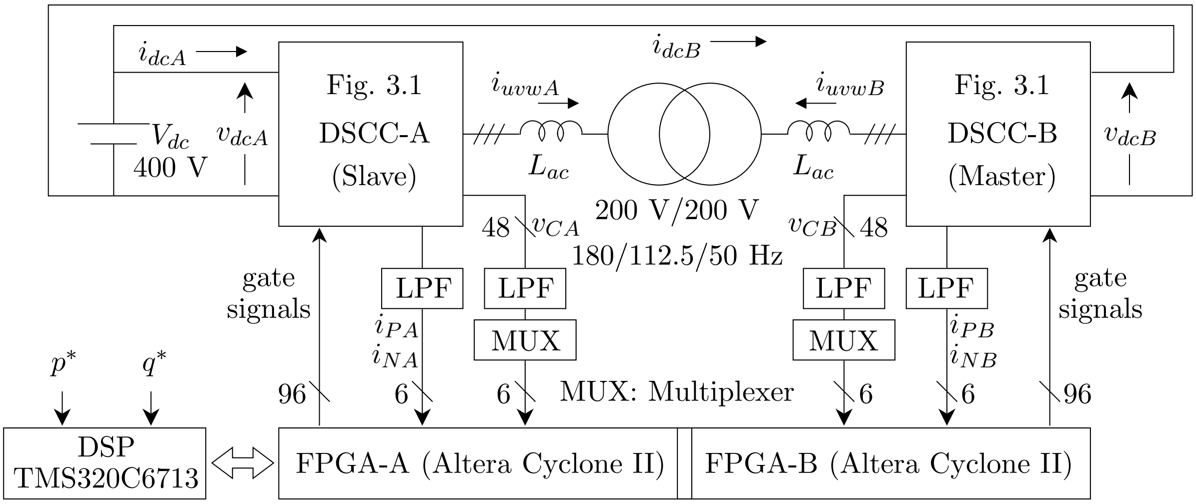


Fig. 4.4: Experimental circuit configuration for the 400-Vdc, 10-kW DSCC-based FTF system with a constant carrier frequency of 450 Hz.

units, and some interface circuits for signal filtering units and multiplexer (MUX) units. Each FPGA unit detects the 48-to-6 multiplexed dc-capacitor voltages, and the positive and negative arm currents. Note that no ac-link voltage is detected, so that only 14 analog signals are sent to each FPGA unit. Each FPGA unit produces 96 (=2×48) gate signals in total to drive all the chopper cells, each of which consists of four parallel RENESAS RJK1529 MOSFETs per chopper arm. Two PC-based data acquisition (DAQ) systems (Yokogawa WE7000) are simultaneously used for capturing experimental waveforms. The sampling frequency of the DAQ system was set to 100 kHz for all operations.

Fig. 4.5 shows a photograph of the downscaled DSCC-based FTF system used for this experiment. Fig. 4.6 shows the transformer used in the ac-link connection between the slave and master converters. Note that the transformer and dc capacitors used in this experiment are optimized for 50-Hz operation. Further reductions in size and weight should be made, according to the ac-link frequencies used in the system. An optimum ac-link frequency can be decided by a good compromise among transformer size and weight, switching losses, and ac-link harmonic contents. However, the optimization on the ac-link frequency is not discussed in this dissertation and should be considered for

Table 4.2: Circuit parameters for experiment

Rated power	P	10 kW
Nominal dc voltage	V_{dc}	400 V
AC-link line-to-line voltage	V_{ac}	200 V
AC-link frequency	f_{ac}	180/112.5/50 Hz
Transformer voltage ratio		1 : 1
Chopper-cell number per leg	N	16
Capacitor	C	6.6 mF
Capacitor mean voltage	V_C	50 V
Unit capacitance constant	H [142]	40 ms
AC-link inductor	L_{ac}	0.4 mH (11.3%*)
Center-tapped inductor	L_Z	3 mH (84.8%*)
PWM carrier frequency	f_{cr}	450 Hz
Equivalent switching frequency	Nf_{cr}	7.2 kHz
Dead time		8 μs

Values in ( ) are on a three-phase, 200-V, 10-kW, 180-Hz base.

future research.

In the following discussions, the 180-Hz ($f_{cr}/f_{ac} = 5/2$ [114]) ac-link frequency is used for the FTF system under several conditions, that is, start-up procedure, steady operation, transient operation, and power-reversal operation. Moreover, the experimental waveforms are compared to the simulated ones to enhance the reliability and validity of both experiment and simulation. The circuit simulation is conducted by using "PSCAD/EMTDC" software package under the same conditions as those in the experiment, including circuit parameters, control gains, sampling frequency, dead time, and delay time of the controller, to improve the accuracy of the simulated system. An ac-link frequency of 112.5 Hz ($f_{cr}/f_{ac} = 4$) is also experimented with the same carrier frequency as 450 Hz ($f_{cr}/f_{ac} = 4$). However, only the transient operation is presented in this section since the other conditions yield similar results to those at the ac-link frequency of 180 Hz. The ac-link frequencies of 50 Hz and 100 Hz were also conducted at the beginning of

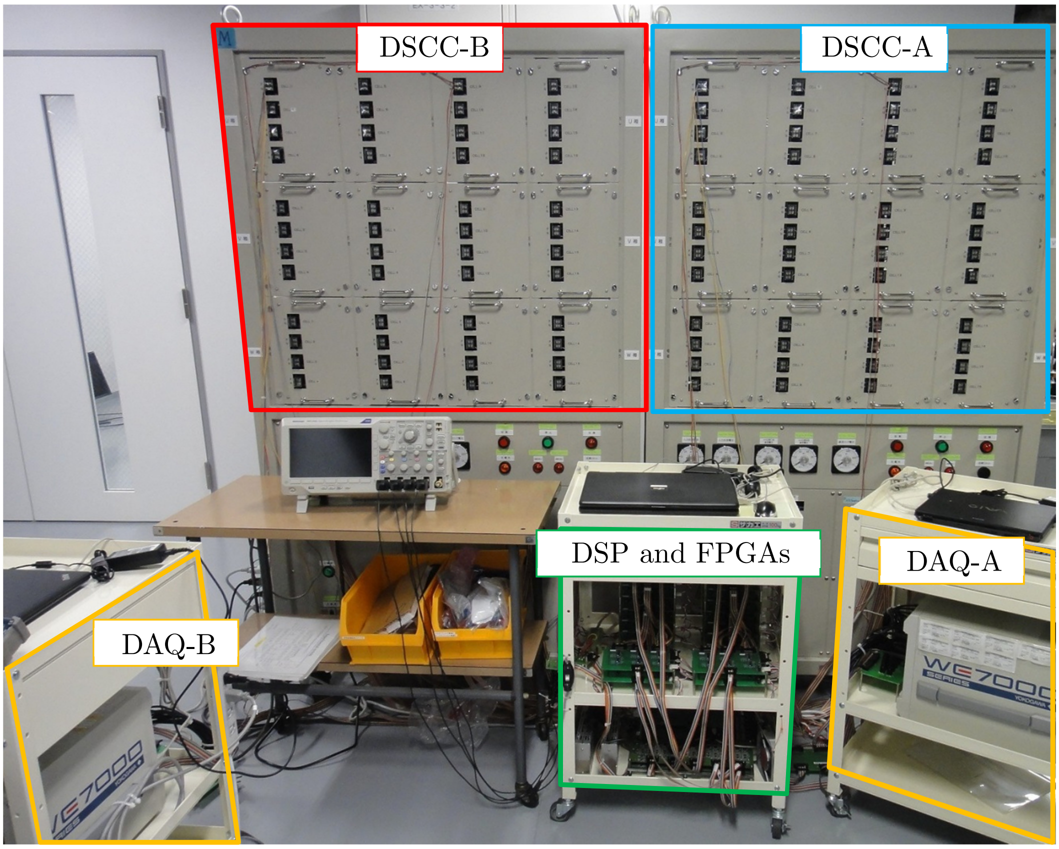


Fig. 4.5: Photo of the 400-Vdc, 10-kW DSCC-based FTF system, the digital controller, and data acquisition systems used for experiments.

this research and are used in this dissertation for a comparison on the capacitor voltage fluctuation and experiments on reactive power compensation.

4.5 Experimental and Simulated Waveforms

4.5.1 Start-up Procedure

Before the system starts transferring any power, all the floating dc capacitors should be charged up to a pre-determined value of 50 V without any auxiliary charging equipment. Fig. 4.7 shows the experimental waveforms at the start-up process for DSCC-A and DSCC-B. Before t_0, all the floating dc capacitors will be initially charged up to a dc voltage of 25 V ($= 400V/16$) when the dc side of the DSCC converters are connected

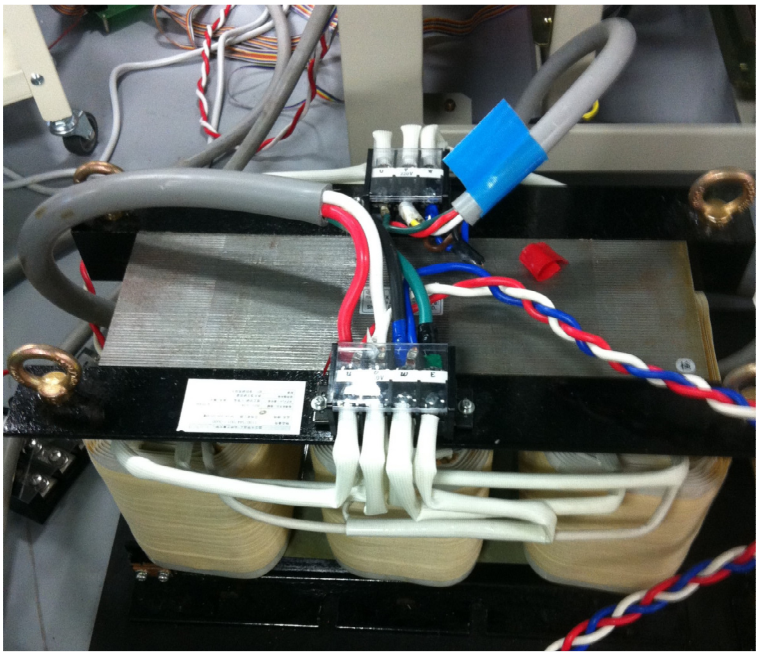


Fig. 4.6: Photo of the three-phase, 15-kVA, 220/220-V, and 50-Hz transformer used for experiments.

to a nominal dc voltage. In this experiment, the initial charging was carried out using an adjustable dc voltage power source shown in Fig. 4.4. The output dc voltage was being adjusted from 0 to 400 V gradually to avoid inrush current. All the floating dc capacitors was charged up to 25 V equally when the dc voltage reaches the nominal value of 400 V. Since no switching operation occurs during the initial charging, the charging current flows in each leg trough the upper diode of each chopper cell.

The switching operation starts after t_0, where the appropriate switching operation was charging all the floating capacitors from 25 V to the predetermined value of $V_C^* =$ 50 V during an interval of T_1 =500 ms. For this reason, the charging process should be completed before raising the ac-link voltages of both converters. The pre-charging operation is controlled by using the capacitor balancing control in the master mode. Only the capacitor voltages of cell numbers 1 and 9 in the u-phase are shown in Fig. 4.7. Note that a small dc current flows as the charging process occurs. After the capacitors are charged up to the reference value, the ac-link voltage is building up until it reaches 200 V within T_2 =500 ms. The time interval for capacitor charging and the voltage-raising, T_1

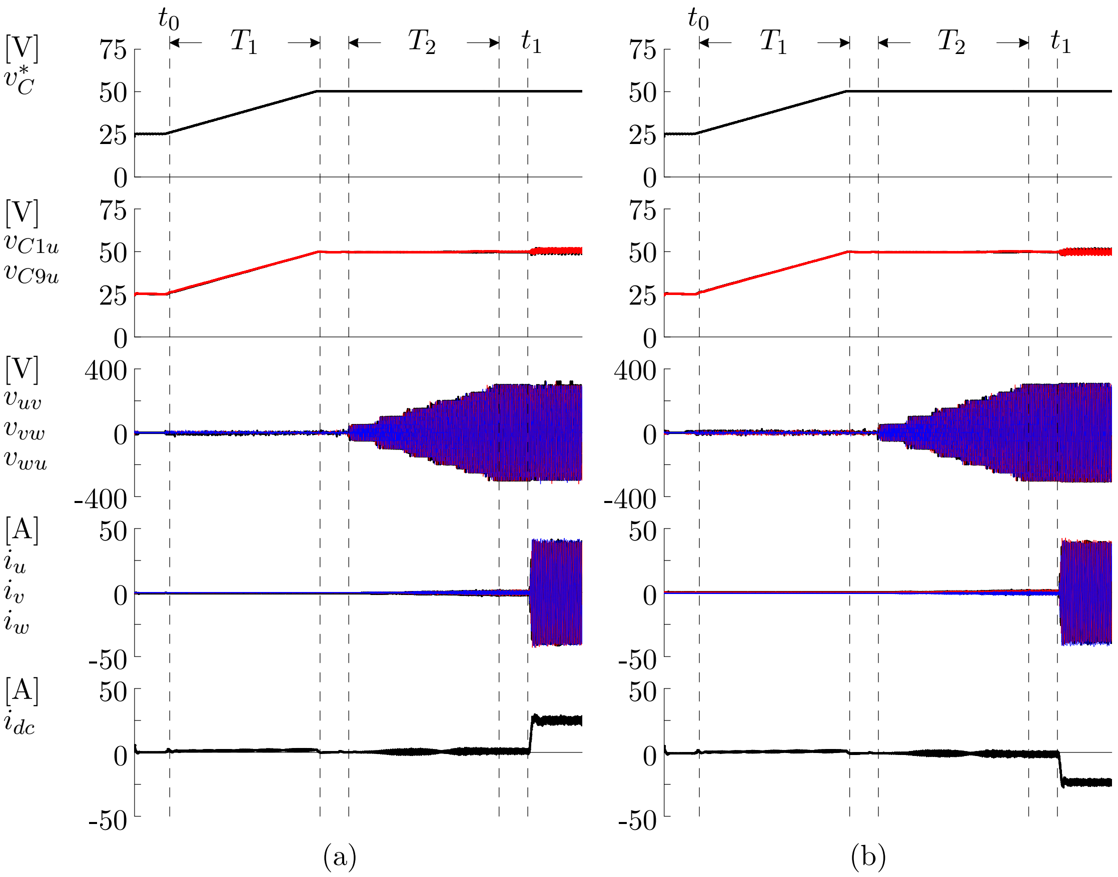


Fig. 4.7: Experimental waveforms of the FTF system during start-up process. (a) DSCC-A. (b) DSCC-B.

and T_2, can be adjusted by the controller. Both DSCC-A and DSCC-B use the master mode for charging and ac-link voltage-raising processes. Afterward, the power reference can be generated to the desired value at t_1. It can be seen that the capacitor voltages start fluctuating after a power transfer occurs. Note that the operation of DSCC-A is changed to the slave mode at t_1 and the power command can be regulated as desired using the decoupled current control.

A real FTF system may use the auxiliary starting circuit as shown in Fig. 4.8. It should be installed between the dc voltage source and the DSCC converters. This auxiliary starting circuit consists of a circuit breaker (CB), a current-limiting resistor, and a magnetic contactor (MC). The initial charging is done by firstly turning on the CB, and all the floating dc capacitors will be charge up through the current-limiting resistor. Afterward, the MC is turned on, and the initial charging is completed, which brings the

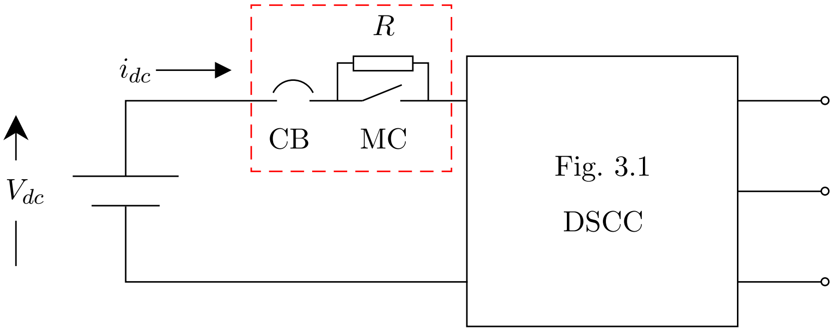


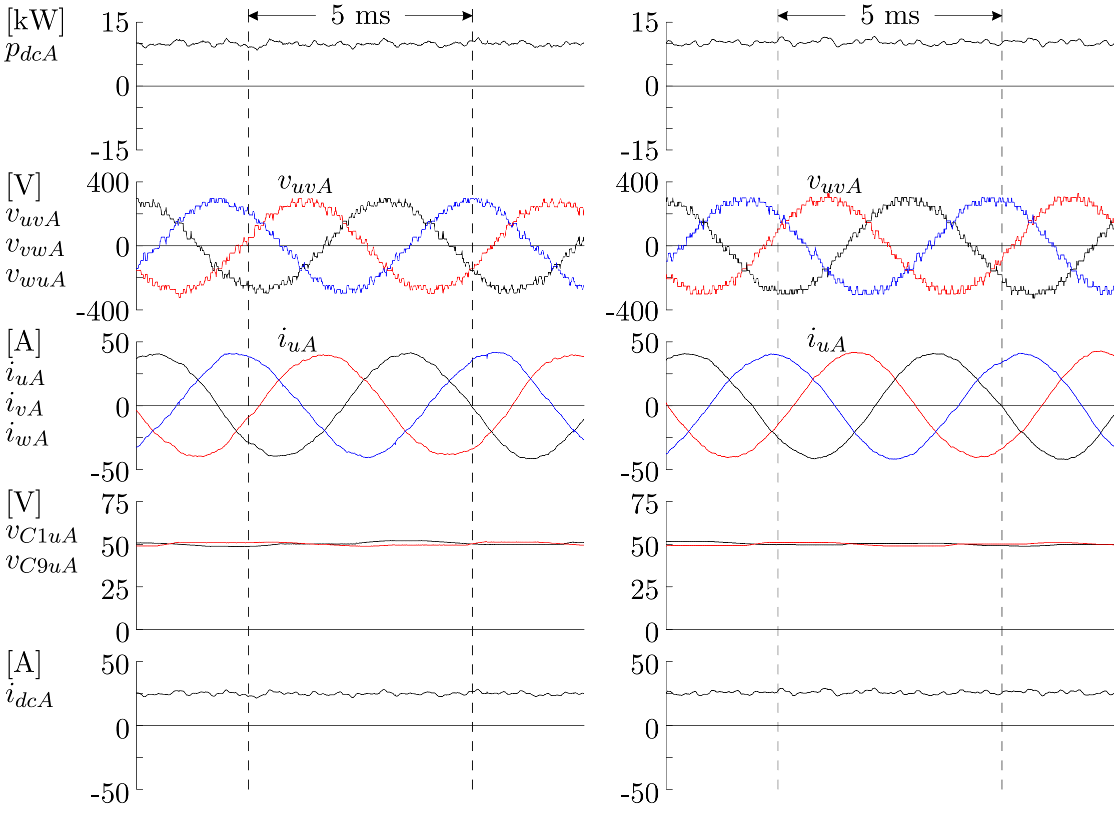
Fig. 4.8: Configuration of an auxiliary circuit for the pre-charging process of a DSCC converter.

all capacitor voltages at the nominal voltage of the capacitor.

4.5.2 Steady-State Performance

Fig. 4.9 shows the experimental and simulated waveforms in a steady-state condition for DSCC-A using $f_{cr}/f_{ac} = 5/2$ when it is sending a power of 10 kW to DSCC-B. Fig. 4.10 shows the respective experimental and simulated waveforms for DSCC-B. This experiment was done by setting DSCC-B in master mode and DSCC-A in slave mode. This arrangement means that DSCC-B should act as a voltage source, while DSCC-A acts as a current source. It can be seen that the ac link has three-phase multilevel voltages and sinusoidal currents. The total harmonic distortion (THD) of the ac-link voltage and current are as low as 8.8% and 2.8%, respectively, although a frequency ratio of 5/2 is utilized. Moreover, the waveforms from the simulated results are very look alike from those of the experimental results.

Note that neither arm currents nor capacitor voltages in the v-phase and w-phase legs is shown in Figs. 4.9 and 4.10, because the waveforms differ only in phase from those in the u-phase leg. The voltage references used for generating the ac-link voltages in DSCC-B are used as feedforward voltages in the decoupled current control for DSCC-A. Note that DSCC-B was operating at unity power factor because DSCC-A did set the reactive power reference to zero ($q^* = 0$) at the ac-side of DSCC-B. The peak-to-peak voltage of the capacitor is as low as 3.2 V (6.4%). This result is understandable because



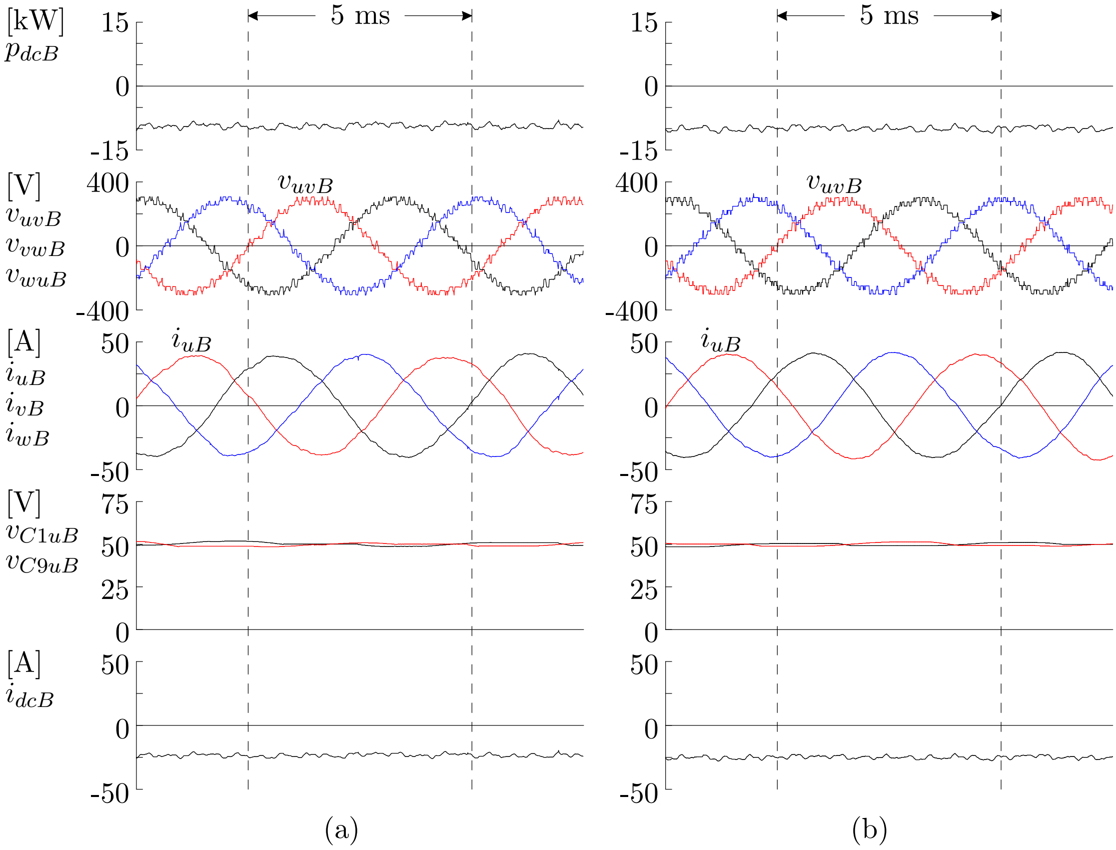
(a) (b)

Fig. 4.9: Experimental and simulated waveforms of DSCC-A with $f_{cr}/f_{ac} = 5/2$, operating in the slave mode under the rated inversion. ($p^* =$ 10 kW, $q^* =$ 0). (a) Experimental waveforms. (b) Simulated waveforms.

of the unit capacitance constant H of the capacitor was at 40 ms. This value was actually designed for the 50 Hz operation. As the frequency goes higher, the unit capacitance constant can be made smaller thus reducing the size and cost of the capacitors.

4.5.3 Transient Operation

Fig. 4.11 shows the experimental and simulated waveforms for DSCC-A using $f_{cr}/f_{ac} = 5/2$ with the slave mode under several power reference changes. Fig. 4.12 shows the respective waveforms for DSCC-B with the master mode operation. The power reference p_A^* was changed in the slave converter (DSCC-A) from 10 kW to 8 kW, and then changed



(a) (b)

Fig. 4.10: Experimental and simulated waveforms of DSCC-B with $f_{cr}/f_{ac} = 5/2$, operating in the master mode under the rated rectification. ($p^* =$ 10 kW, $q^* =$ 0). (a) Experimental waveforms. (b) Simulated waveforms.

back to 10 kW for 20 ms with step changes. Afterward, a ramp change from 10 kW to 0 W within 10 ms occurs before another ramp change that brings back the output power from 0 W to 10 kW. The waveforms from DSCC-B operating as the master converter are similar to those from DSCC-A with the opposite power direction. Note that the power reference p_B^* is not controlling the power on the master converter, but is shown only for a comparison with the power on DSCC-B.

The waveforms show that the system remains stable although the power reference p^* was changed instantaneously. At the instant moment when the power is changed from 8 kW to 10 kW, the ac voltages and currents remain balanced and have only very small spikes. Notice that the capacitor voltages remain stable without any alteration although

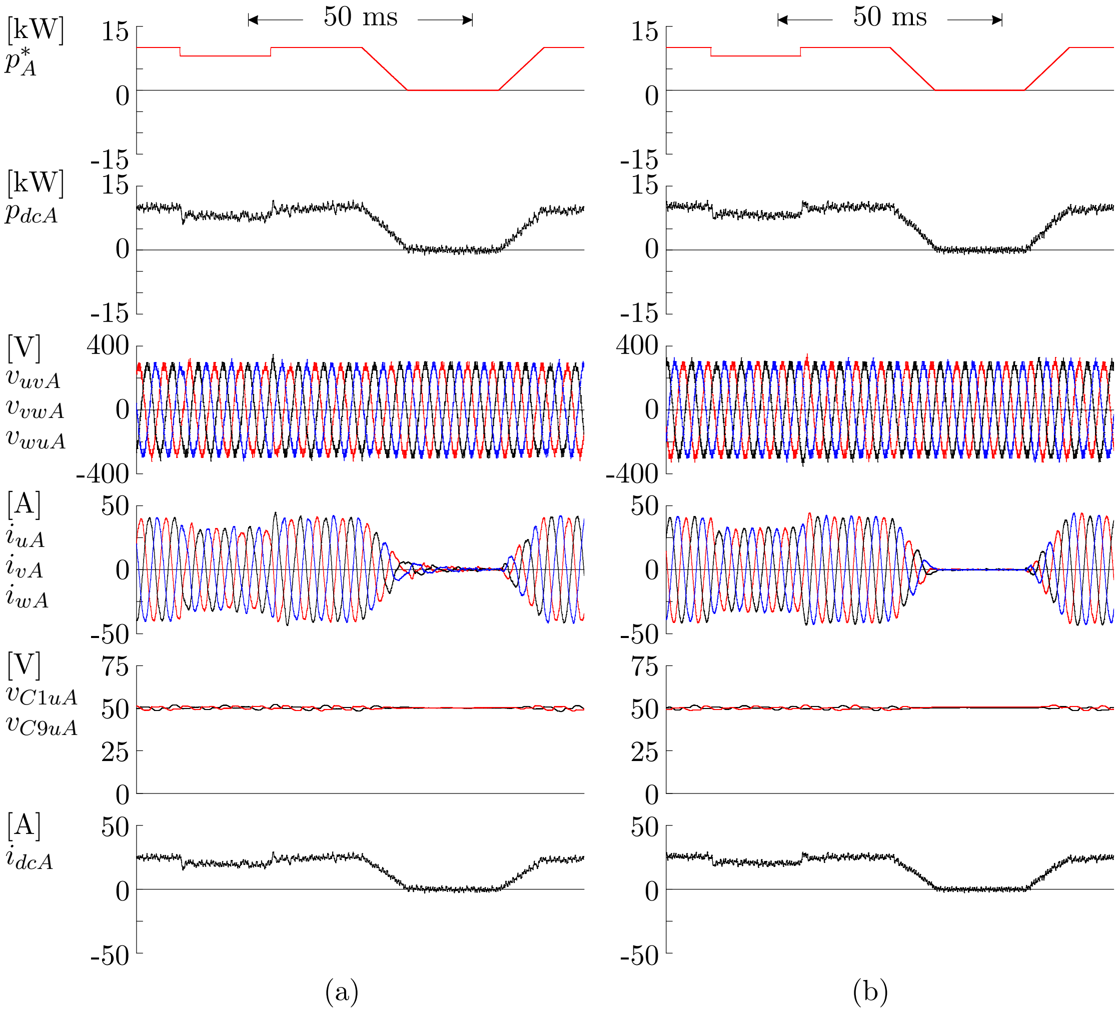
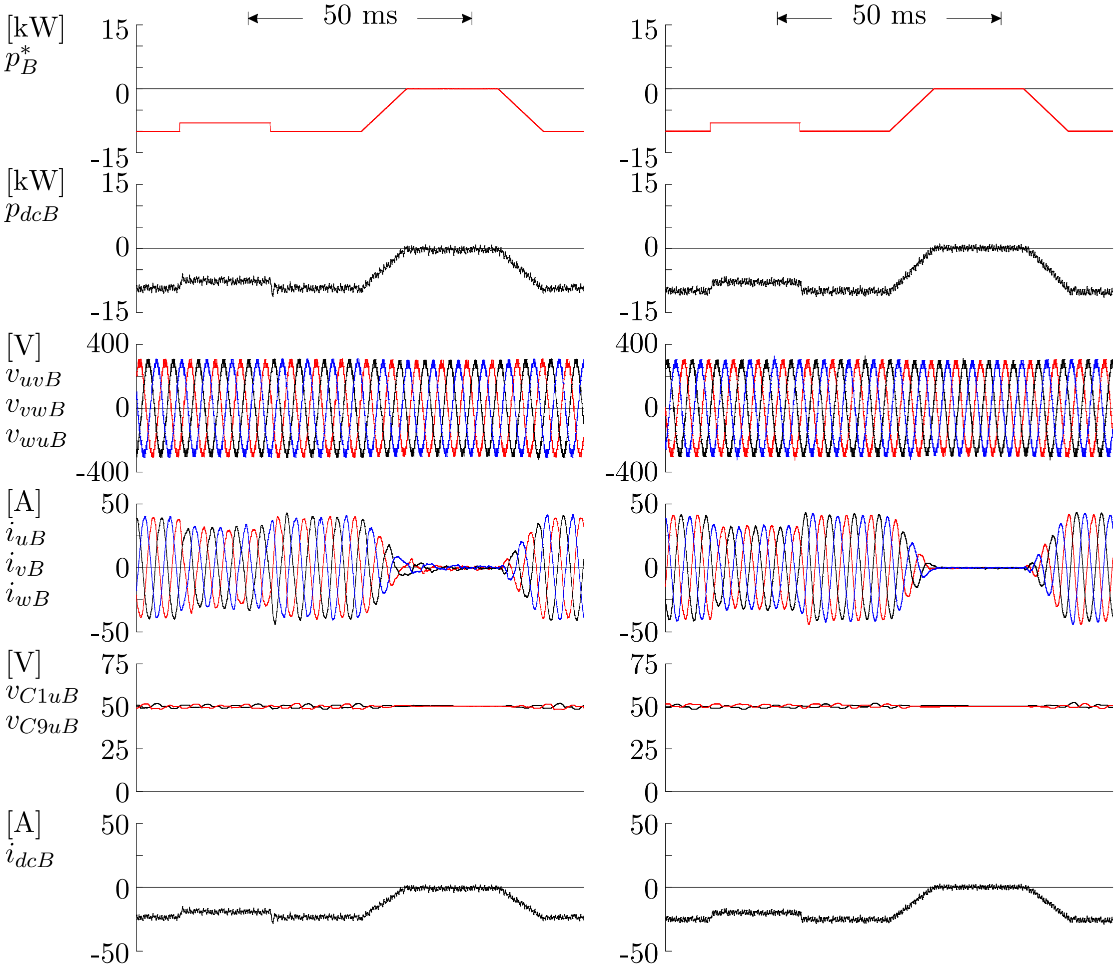


Fig. 4.11: Experimental and simulated waveforms of DSCC-A with $f_{cr}/f_{ac} = 5/2$, operating in the slave mode under a step change of power reference p^*. (a) Experimental waveforms. (b) Simulated waveforms.

step and ramp power changes are performed. Comparing the results from the simulated waveforms to those of the experimental waveforms, it can be seen that the two systems yield very similar waveforms although step and ramp changes on the power reference are carried out.



(a) (b)

Fig. 4.12: Experimental and simulated waveforms of DSCC-B with $f_{cr}/f_{ac} = 5/2$, operating in the master mode under a step change of power reference p^*. (a) Experimental waveforms. (b) Simulated waveforms.

4.5.4 Power Reversal Operation

It is necessary for high-power dc-to-dc converters connected to a dc grid to allow a bidirectional power flow to/from the grid without changing the polarity of both voltages. The power control of the FTF system utilizing decoupled current control on the slave converter can change the power direction very easily by changing the magnitude of the active current reference i_d^* without altering the polarity or amplitude of dc-link voltages. The power reversal operation can be done very fast in the order of milliseconds.

Figs. 4.13 and 4.14 show the experimental and simulated waveforms in the FTF system using $f_{cr}/f_{ac} = 5/2$ under the rated-power reversal operation. The power reference was changed linearly from 10 kW to -10 kW during an interval of 20 ms. The results on both DSCC-A and DSCC-B show a stable and very-fast power-reversal operation. These results conclude that the power reversal can be achieved without any problem on the capacitor-voltage balancing as shown in the figures.

Fig. 4.15 shows the experimental waveforms of DSCC-A and DSCC-B using $f_{cr}/f_{ac} = 4/1$ under the rated-power reversal operation at another ac-link frequency of 112.5 Hz. The power reference is adjusted with a ramp change of 10 kW to -10 kW during 20 ms as before. The result demonstrates that although the carrier frequency f_{cr} is an integer multiple of the ac-link frequency f_{ac} with a ratio of four, the FTF system can run in stable operation under both steady-state and transient conditions. It can be concluded that the individual balancing control plays a very important role to cancel out small dc current components on the capacitor voltages [114].

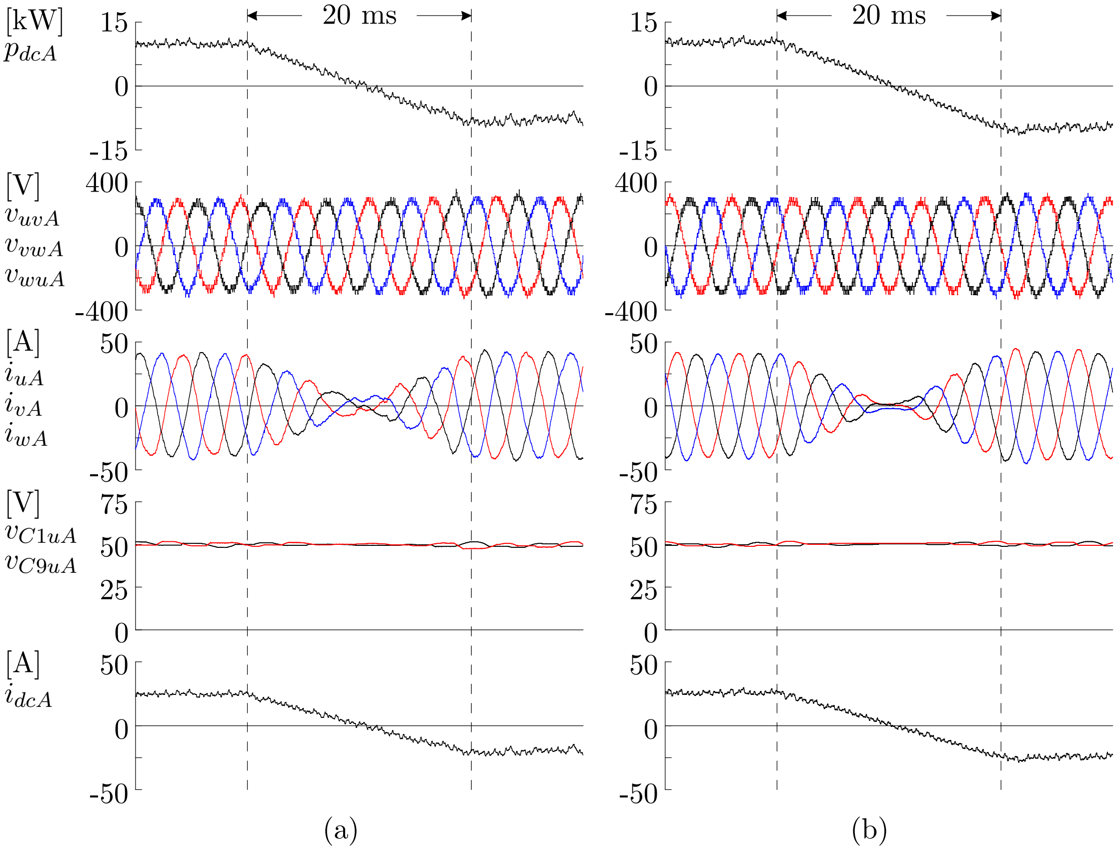
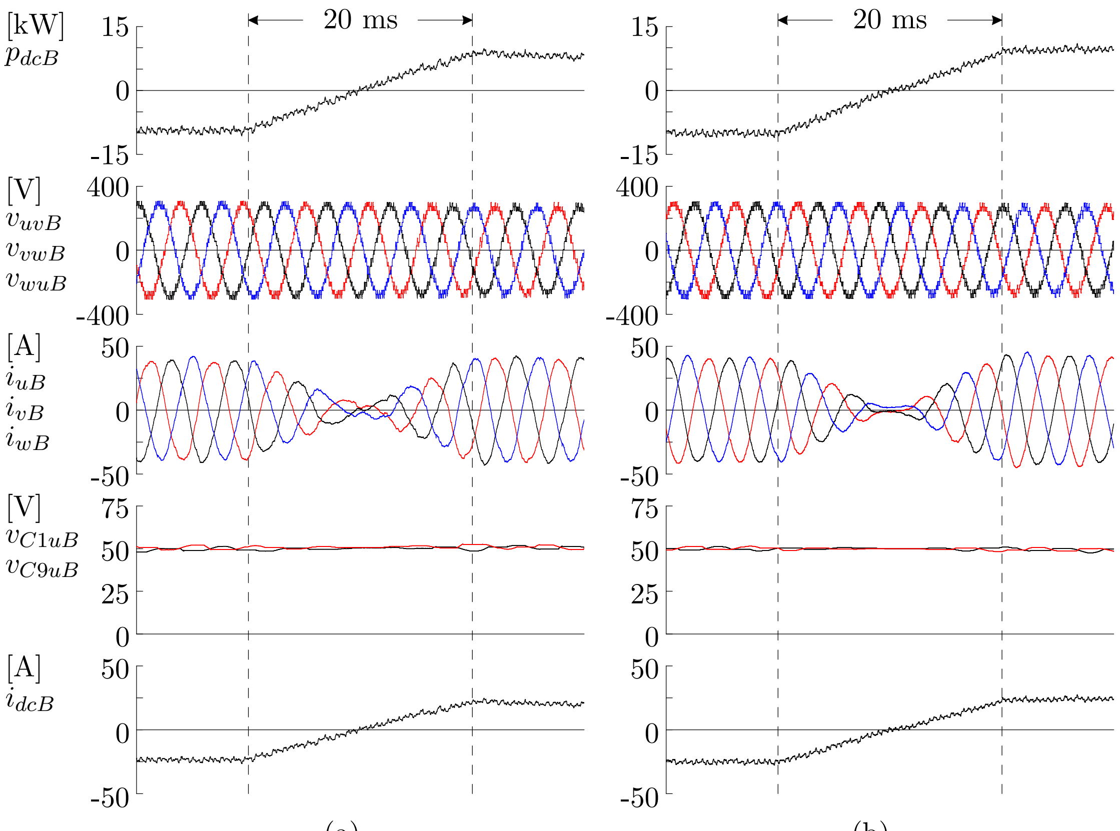


Fig. 4.13: Experimental and simulated waveforms of DSCC-A with $f_{cr}/f_{ac} = 5/2$, operating in the slave mode under the rated-power reversal from inversion to rectification during an interval of 20 ms. (a) Experimental waveforms. (b) Simulated waveforms.



(a) (b)

Fig. 4.14: Experimental and simulated waveforms of DSCC-B with $f_{cr}/f_{ac} = 5/2$, operating in the master mode under the rated-power reversal from rectification to inversion during an interval of 20 ms. (a) Experimental waveforms. (b) Simulated waveforms.

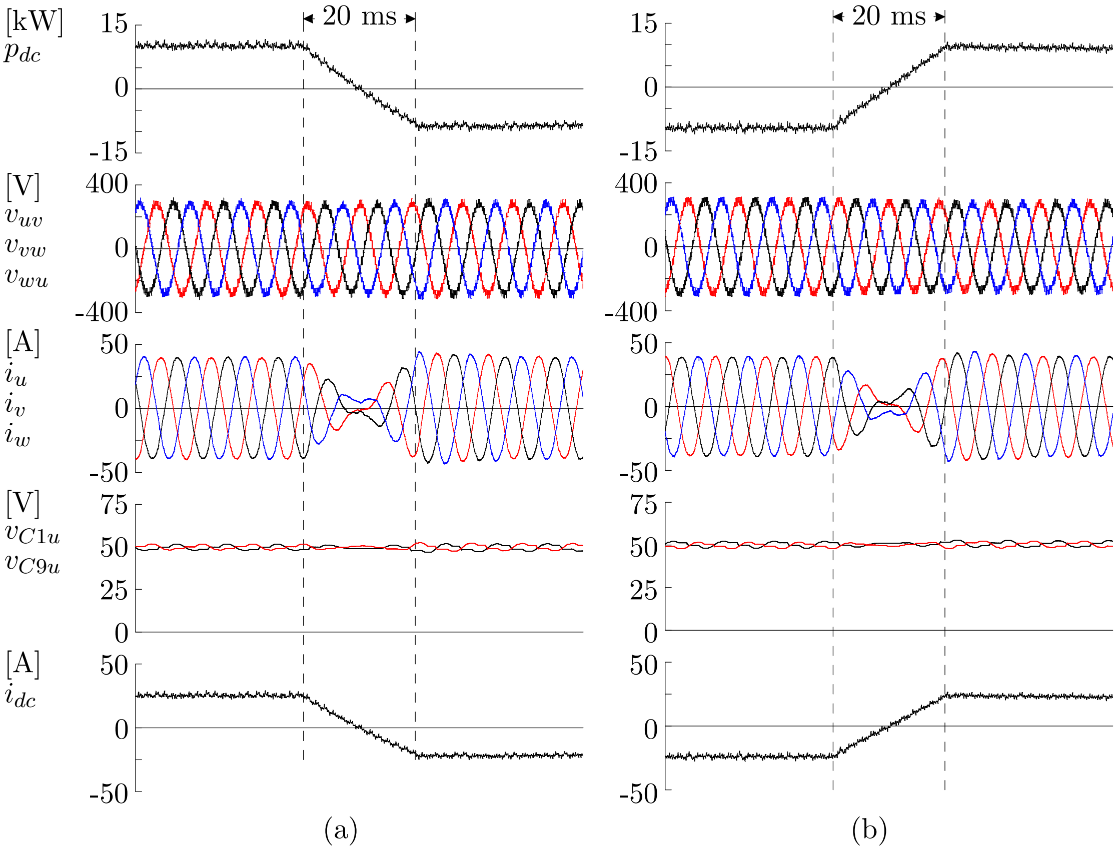


Fig. 4.15: Experimental waveforms of the FTF system with $f_{cr}/f_{ac} = 4/1$ under the rated-power reversal operation. (a) DSCC-A. (b) DSCC-B.

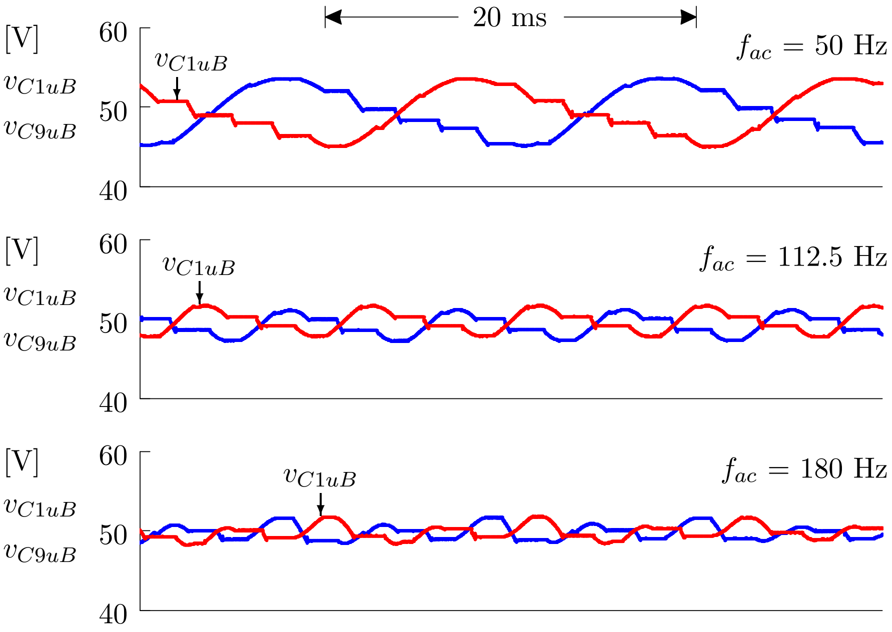


Fig. 4.16: Experimental comparison in capacitor voltage fluctuation among three ac-link frequencies, f_{ac} = 50, 112.5, and 180 Hz at the same carrier frequency as f_{cr} = 450 Hz.

4.5.5 Capacitor Voltage Fluctuation and Harmonic Frequency Spectra of Capacitor Voltage

Fig. 4.16 shows the experimental waveforms of the capacitor voltage fluctuation under the following three ac-link frequencies: f_{ac} = 50, 112.5, and 180 Hz, where the carrier frequency f_{cr} was kept constant at 450 Hz. The ac-link inductor L_{ac} for the 50-Hz case is 2 mH instead of 0.4 mH. The peak-to-peak ripple voltage Δv_{Cju} for all the cases are 8.6 V, 3.8 V, and 3.5 V at 50 Hz, 112.5 Hz, and 180 Hz, respectively. For the 180-Hz ac-link frequency case, the peak-to-peak ripple voltage Δv_{Cju} corresponds to 7% of the rated dc capacitor voltage. It is obvious that the peak-to-peak ripple voltage of the capacitors gets higher as the ac-link frequency gets lower, as long as the same capacitance value is used.

Figs. 4.17 and 4.18 show the normalized values of analytical, experimental, numerical, and simulated harmonic frequency spectrum of v_{C1u} on the slave converter at f_{ac} = 180 Hz and 112.5 Hz, respectively, under the rated power inversion [114]. The figures show that all harmonic spectrum agree well with each other. Note that the harmonic

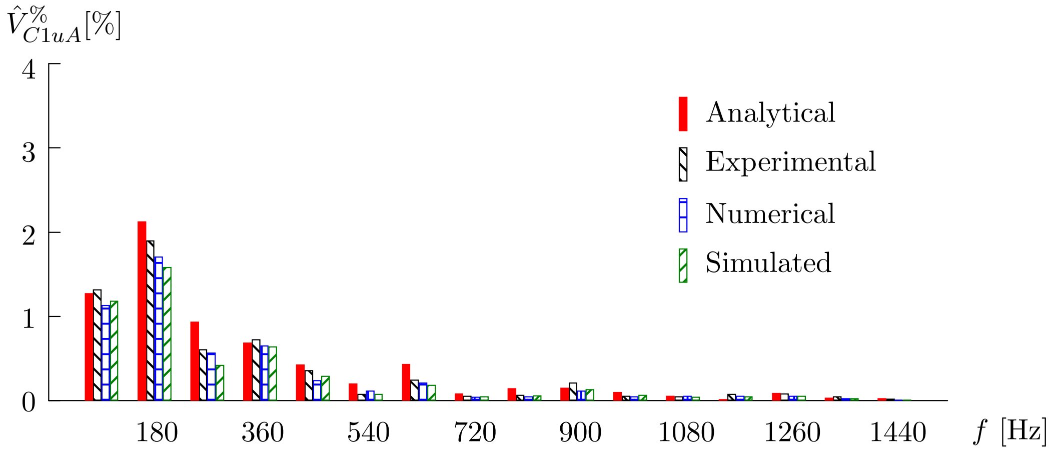


Fig. 4.17: Frequency spectrum of the ac components contained in v_{C1u} of DSCC-A at f_{ac} = 180 Hz and f_{cr} = 450 Hz.

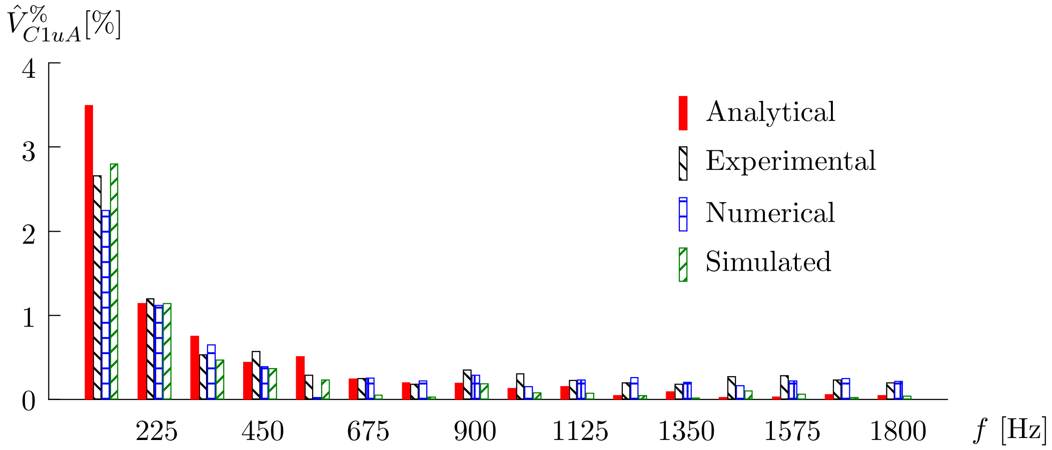


Fig. 4.18: Frequency spectrum of the ac components contained in v_{C1u} of DSCC-A at f_{ac} = 112.5 Hz and f_{cr} = 450 Hz.

components caused by switching action influence the capacitor voltage fluctuation when the ratio of the carrier frequency with respect to the ac-link frequency gets lower.

The harmonic components caused by switching action include not only the second-order and carrier-frequency components but also the sideband frequencies around the integer multiples of the carrier frequency. When f_{ac} = 180 Hz and f_{cr} = 450 Hz, the lowest harmonic frequency f_L is 90 Hz ($= f_{cr} - 2f_{ac}$) on the capacitor voltage fluctuation. Correspondingly, the moving window time of the moving-average filter, which is used for the voltage-balancing control of all the dc capacitors, is set on the basis of the lowest

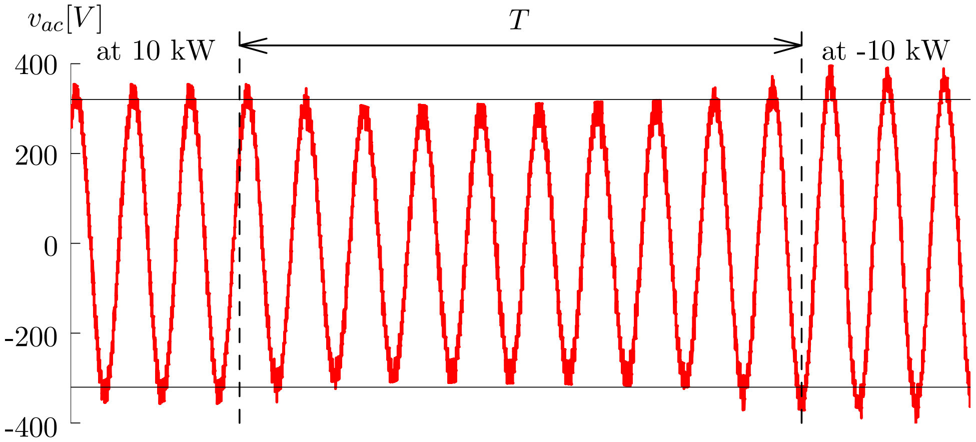


Fig. 4.19: Experimental waveform of ac-link voltage on the slave converter during power-reversal operation.

harmonic frequency, that is, $1/f_L$. On the other hand, for the ac-link frequency of 112.5 Hz, the lowest harmonic frequency f_L is the same as 112.5 Hz, so that the moving window time can be set as $1/f_{ac}$. Although the capacitor voltages are fluctuating at 112.5 Hz and its integer multiples, the average capacitor voltages can be kept at 50 V by using an appropriate moving-average filter incorporated in the voltage-balancing control.

4.6 Reactive Power Compensation

The slave converter in the FTF system uses the decoupled current control to deliver/absorb the power to/from the master converter. The slave converter uses a feed-forward voltage reference instead of using a PLL circuit as has been mentioned in Section 4.3. To deliver maximum power to the master converter, the set point for a unity power factor is at the ac terminals of the master converter. However, overvoltage at the ac terminals of the slave converter might occur because of the uncontrolled nature of the voltage on the slave mode. Moreover, when the ac-link inductance L_{ac} is relatively large to reduce the harmonic current on the ac link, the over voltage is likely to occur at high power transfer. Overmodulation on the cells of the slave converter may occur because of the voltage command from the decoupled current control to produce a unity power-factor operation on the master converter. Therefore, the ac-terminal voltage of the slave converter should be regulated to avoid overmodulation and overvoltage issues.

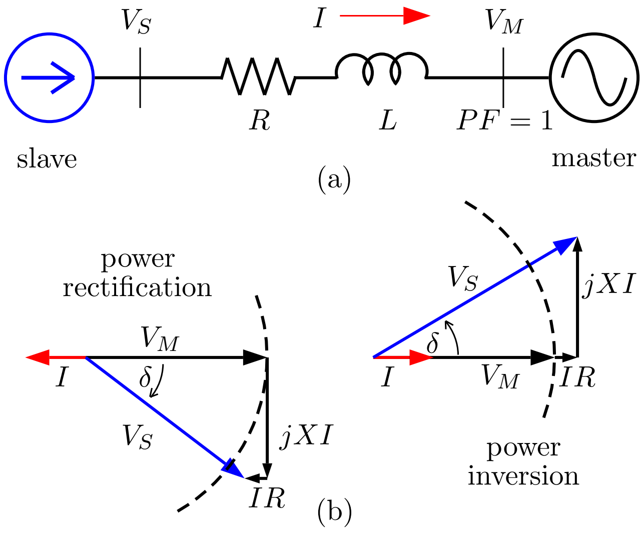


Fig. 4.20: Power transfer in an FTF system with unity power factor at the ac terminal of the master converter. (a) Single-phase equivalent circuit. (b) Phasor diagram.

Fig. 4.19 shows the experimental waveform of the slave voltage when the power direction is changed from the rated inversion to the rated rectification. It can be seen that the slave ac-terminal voltage is higher than the nominal value whenever a large power transfer occurs. This phenomenon can be explain by looking at the equivalent circuit and the phasor diagram of the FTF system as shown in Fig. 4.20. The FTF system using two DSCC converters can be modeled as a connection of a current source to a voltage source through an ac-link impedance. The current source represents the slave converter while the voltage source represents the master converter. The impedance shown in the figure represents a total equivalent value that includes the ac-link inductors L_{ac}, the transformer, and stray resistances and inductances. The ac-terminal voltage of the slave converter is considered larger than the nominal voltage (or the voltage on the ac terminals of the master converter) when the voltage vector is outside the voltage boundary (shown by the dashed arc line). The phasor diagram shows that the larger the total inductance on the ac link, the higher the voltage angle δ of the slave converter with respect to the master converter resulting in an over voltage on the ac-terminal voltage of the slave converter.

One way to resolve this issue is by absorbing a reactive current component to bring a

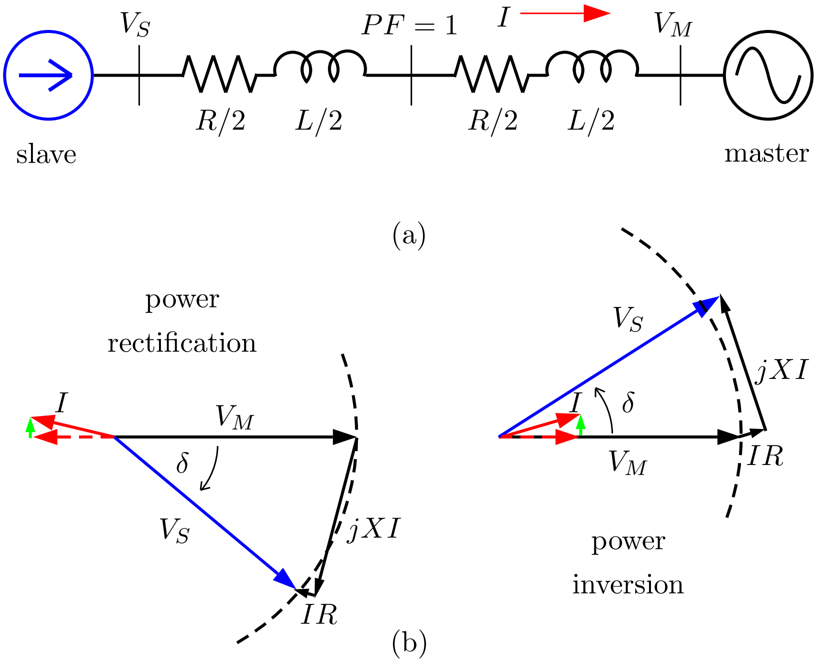


Fig. 4.21: Power transfer in the FTF system when a reactive power compensation is applied. (a) Single-phase equivalent circuit. (b) Phasor diagram.

unity power factor at the middle node of the ac-link impedance, that is, at the transformer point. Fig. 4.21 shows the equivalent circuit and the phasor diagram when a reactive power compensation is introduced. The amplitude of the slave voltage can be reduced at the expense of reactive power absorption by the slave converter. The current is now leading with respect to the ac terminals of the master converter resulting in a non-unity power factor operation at the master converter. Note that the master converter does not alter the current because it operates as a voltage source. Therefore, the reactive power compensation should be done by the slave converter. In this section, there are two proposed control method that will be discussed: a feedback compensation, and a feedforward compensation. Both control methods adjust the reactive power (or q-axis current) command to reduce the overvoltage on the slave converter.

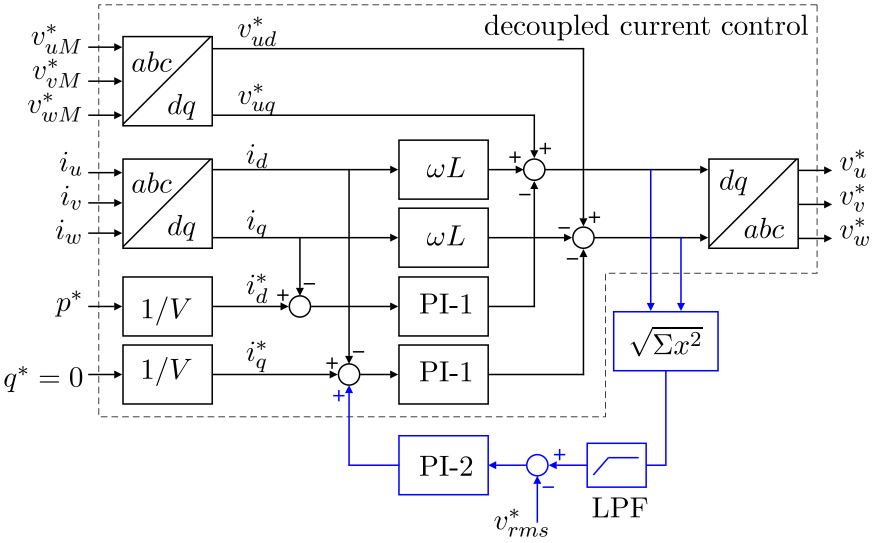


Fig. 4.22: Control block diagram of a feedback control for reactive power compensation.

4.6.1 Feedback Control

A feedback control for reactive power compensation can be realized by using the available information on the circuit or the control signals. Since the control target is the ac-terminal voltage of the slave converter, the rms voltage on the ac terminals of the slave converter should be used as a feedback signal to be compared with the desired voltage reference v_{rms}^*. Fig. 4.22 shows the proposed feedback control block diagram to compensate the reactive power and reduce the overvoltage on the slave ac terminals. Note that the feedback control uses the information from the decoupled current control because no PLL circuit is used to detect the ac-terminal voltage of the slave converter. Therefore, the proposed control method is easy to implement without any additional circuit. The rms value of the ac-terminal voltage of the slave converter can be obtained from the previous voltage command of the decoupled current control v_d^{*-1} and v_q^{*-1} as follows:

$$v_{rms} = \sqrt{(v_d^{*-1})^2 + (v_q^{*-1})^2}. \tag{4.4}$$

A simple PI controller is used to control the reactive power by using the voltage command information from the decoupled current control. A low-pass filter can be used to filter out any high-frequency component before comparing the previous voltage

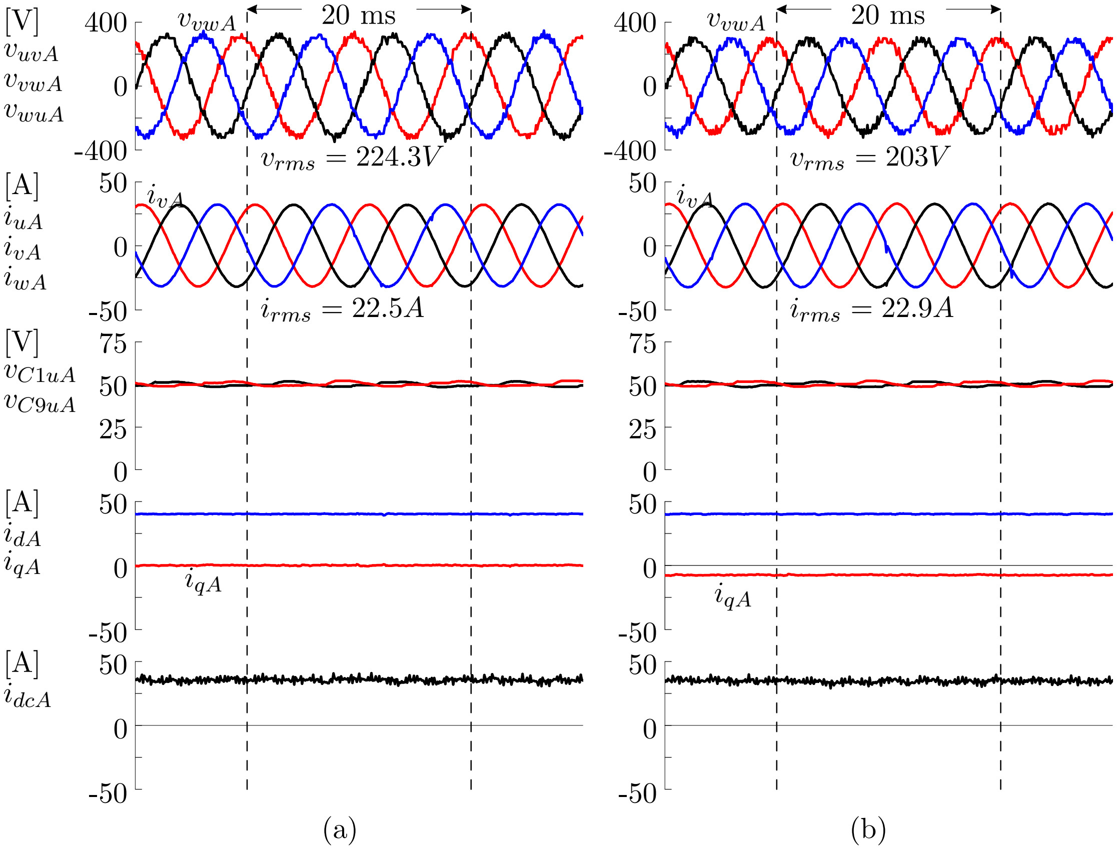


Fig. 4.23: Comparison of the experimental waveforms on DSCC-A with $f_{cr}/f_{ac} = 9/2$ at 8-kW power operation. (a) Without feedback compensation. (b) With feedback compensation.

command with the voltage reference v^*_{rms}. Fig. 4.23 shows an experimental comparison between the waveforms of the slave converter without any compensation (Fig. 4.23(a)) and the waveforms with a feedback compensation on the reactive power (Fig. 4.23(b)). The results are obtained from the same FTF system circuit as the previous discussion with the ac-link frequency f_{ac} and inductor L_{ac} of 100 Hz and 2 mH (31.4%), respectively. The waveforms show that the rms voltage of the slave ac terminals can be reduced from 224.3 V to 203 V by using the feedback control compensation, which is very close to the nominal voltage of 200 V. Note that the ac-link currents are slightly increased due to the additional q-axis current component.

4.6.2 Feedforward Control

The aforementioned feedback control method contains a control delay caused by the use of previous voltage command. Another way of achieving a reactive power compensation without a control delay is by using a feedforward control. If the master converter ac-terminal voltage V_M is assumed to have zero phase angle; and the slave converter is assumed to have voltage phase angle of δ, and the inductance is assumed to be much higher than the resistance ($j\omega L >> R$), the apparent power on the ac terminals of the master converter S_M can be written as follows:

$$\begin{aligned} S_M &= V_M\angle 0 \times I^* \\ &= V_M\angle 0 \left(\frac{V_S\angle\delta - V_M\angle 0}{j\omega L}\right)^* \\ &= \frac{V_M V_S \cos\delta - V_M^2 - jV_M V_S \sin\delta}{-j\omega L}. \end{aligned} \tag{4.5}$$

The active and reactive power components on (4.5) can be separated to form the following:

$$P_M + jQ_M = \frac{V_M V_S \sin\delta}{\omega L} + j\frac{V_M V_S \cos\delta - V_M^2}{\omega L}. \tag{4.6}$$

The first term of (4.6) is the active power component that leads to the following relations:

$$\sin\delta = \frac{P_M \omega L}{V_M V_S}, \tag{4.7}$$

$$\cos\delta = \frac{\sqrt{(V_M V_S)^2 - (P_M \omega L)^2}}{V_M V_S}. \tag{4.8}$$

The second term of (4.6) represents the reactive power component. The cosine component on the second term of (4.6) can be substituted with (4.8) to obtain the relation of reactive power Q_M with the active power P_M as follows:

$$Q_M = \sqrt{\left(\frac{V_M V_S}{\omega L}\right)^2 - P_M^2} - \frac{V_M^2}{\omega L}. \tag{4.9}$$

Equation (4.9) shows that the reactive power on the ac terminals of the master converter can be represented by using the power P_M, the rms voltage on the master and slave converter, and the inductance on the ac link. Since the voltage on the master converter is determined as in (4.1)–(4.3), and the active power P_M is determined by the power command on the slave converter, (4.9) can be rewritten as follows:

$$Q_M = \sqrt{\left(\frac{V_M^* V_S}{\omega L}\right)^2 - (P^*)^2} - \frac{(V_M^*)^2}{\omega L}. \tag{4.10}$$

Equation (4.10) shows that the reactive power Q_M depends only on the ac-link impedance and the ac-terminal voltage of the slave converter. When the reactive power is set to zero at the ac terminals of the master converter, the ac-terminal voltage of the slave converter can be obtained from (4.10) as

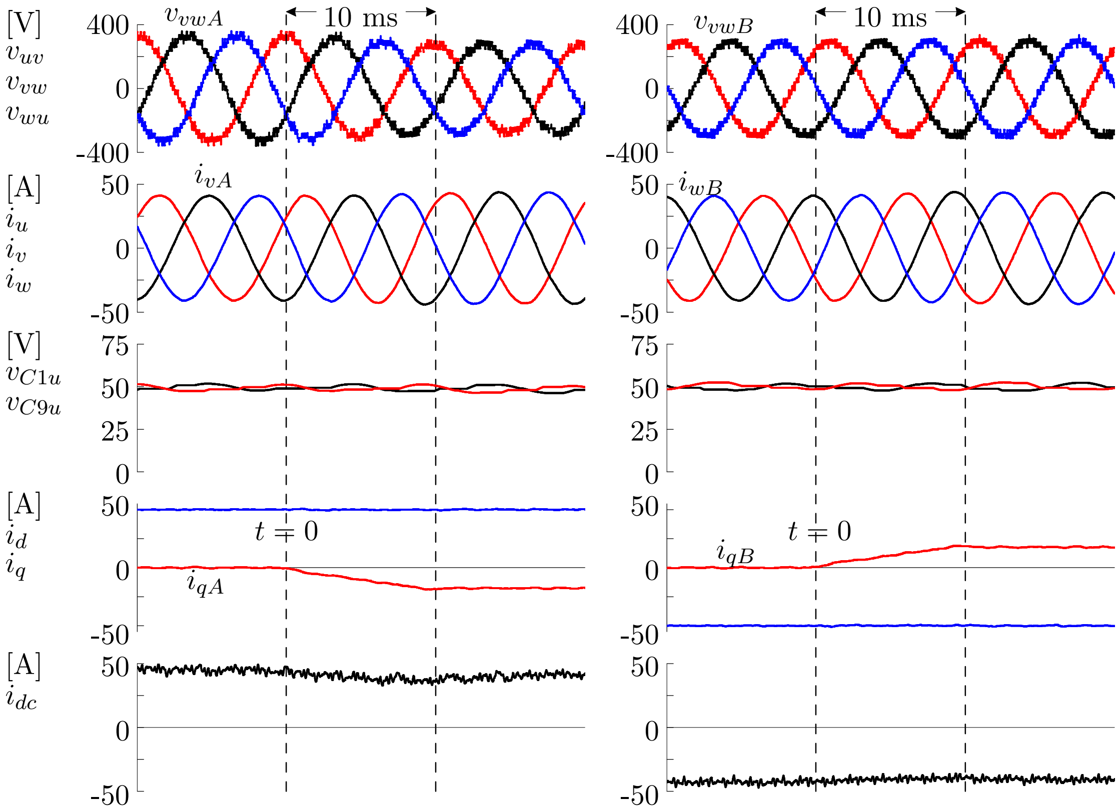
$$\begin{aligned} V_S &= \sqrt{(V_M^*)^2 + \left(\frac{P^* \omega L}{V_M^*}\right)^2} \\ &= \sqrt{(V_M^*)^2 + (I_d^* \omega L)^2}, \end{aligned} \tag{4.11}$$

where I_d^* is the active current command on the decoupled current control. Equation (4.11) shows that the ac-terminal voltage of the slave converter tends to be higher than the nominal voltage V_M^* when sending/receiving the power to/from the master converter while keeping a unity power factor at the master converter. Thus, to avoid overvoltage on the slave converter, an amount of reactive power should be received.

The ac-terminal voltage of the slave converter can be set equal to the nominal voltage V_M^* by substituting $V_S = V_M^*$ in (4.10) to obtain the reactive power command as follows:

$$\begin{aligned} I_q^* &= \frac{Q^*}{V_M^*} \\ &= \sqrt{\left(\frac{V_M^*}{\omega L}\right)^2 - (I_d^*)^2} - \frac{V_M^*}{\omega L}. \end{aligned} \tag{4.12}$$

This reactive power command I_q^* can be used as a feedforward control command to the decoupled current controller in the slave converter. Therefore, this method can achieve reactive power compensation faster since there is no control delay time as in the feedback controller. However, accurate parameter determination of the transformer and other impedances on the ac link are necessary. Note that the unity power-factor operation is shifted to the middle point of the ac-link impedance, that is, at the transformer, when $V_S = V_M^*$ is utilized. The slave converter can be set slightly higher if desired by using $V_S \kappa = V_M^*$, where κ is a scale factor in a real number that is slightly higher than one.



(a) (b)

Fig. 4.24: Simulated waveforms of the FTF system with $f_{cr}/f_{ac} = 9/2$ at rated-power operation when the feedforward compensation is activated at $t = 0$. (a) DSCC-A. (b) DSCC-B.

To verify the proposed feedforward control, a simulation system is constructed using the same circuit parameters as those in Table 4.2 except for the ac-link frequency f_{ac} and inductor L_{ac} value that are set at 100 Hz and 2 mH (31.4%) respectively. Note that the simulation system has achieved a very-good agreement of signal waveforms with the experimental results as shown in Section 4.5. Fig. 4.24 shows the simulated results when the feedforward compensation method is activated at $t = 0$. The ac-link voltage of the slave converter before the activation of the compensator was 231.4 Vrms. The ac-terminal voltage of the slave converter after the activation can be significantly reduced to 198 Vrms, which is a reduction of 14.4% from before.

The compensation was done by a ramp command to prevent overshoot on the control circuit. A reduction of 1 A (3.6%) on the dc current of the slave converter was also observed. However, the ac currents of the slave converter get slightly higher with an increment of 6.6% from 28.8 A to 30.7 A. This increment happens because of the increase on the q-axis current component as can be seen in the figure. Note that the capacitor balancing control can still operate normally without any disturbance although the reactive power compensation is introduced. Fig. 4.24 (b) also shows that the feedforward reactive power compensation on the slave converter does not alter the operation of the master converter. Nevertheless, the master converter is no longer operating in a unity power factor as before.

4.7 Summary

This chapter has discussed experimental evaluation on an FTF system consisting of a pair of DSCC converters and a three-phase transformer for voltage matching and galvanic isolation. The system configuration is applicable to a medium-/high-voltage high-power bidirectional isolated dc-to-dc converter. The voltage and frequency of the ac link can be controlled directly by the master converter. As a result, neither phase-locked loop (PLL) circuit nor ac voltage sensor is required. To reduce overvoltage on the slave converter that operates using a current controller, a reactive power compensator based on feedback or feedforward control can be used. The viability and validity of the system have been verified by a simulation system and a downscaled 10-kW, 400-Vdc, 200-Vac experimental system. The FTF system based on phase-shifted-carrier PWM with optimal carrier frequency ratios of $f_{cr}/f_{ac} = 5/2$ and 4/1 yields stable operation and provides good transient performance. Moreover, the simulated waveforms agree well with the experimental waveforms not only in steady states but also in transient states, thus resulting in enhancing the reliability and validity of both experiment and simulation.

Chapter 5

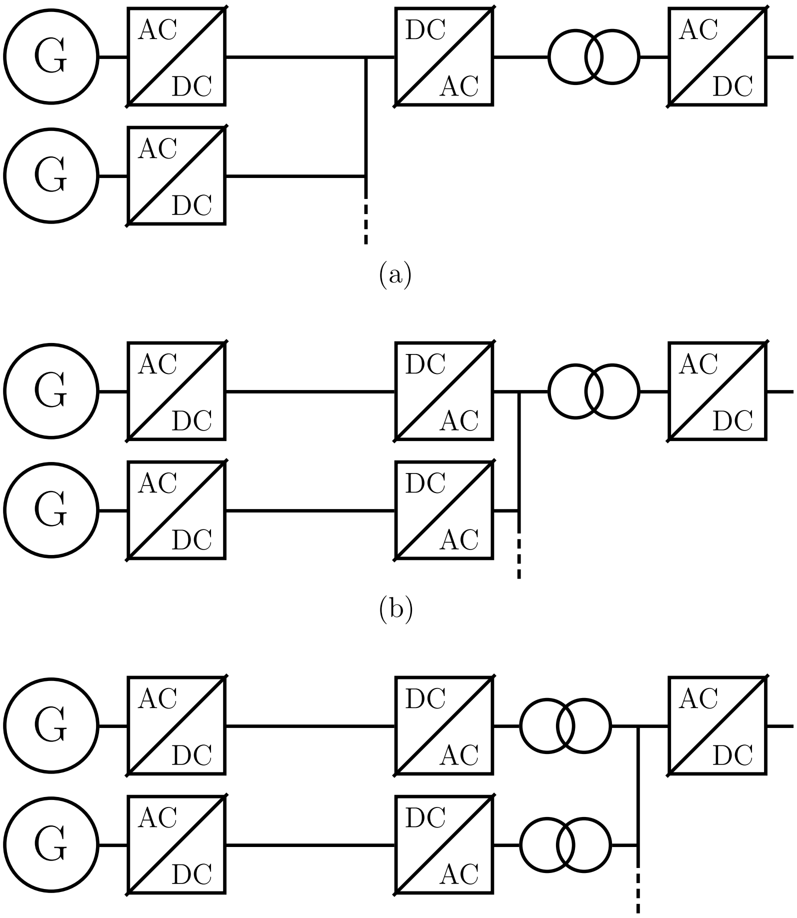
A DC Power Collection Based on the FTF System

5.1 Introduction

This chapter presents a flexible and scalable dc power collection based on a medium-/high-voltage, high-power FTF system utilizing multiple DSCC converters. The system configuration is applicable to multi-terminal dc power networks such as off-shore wind farms. The system is an extension of the system configuration described in Chapter 4. The focus of the discussion is the performance of the dc power collection system under transient and dc fault conditions. Simulated results on the performance of a 10-MW dc power collection is presented in this chapter with two DSCC converters at the power-collecting side. Later in this chapter, the dc faults handling capability of the system is discussed. It includes fault current determination and a fault protection scheme. Finally, simulated results on the short-circuit protection of the dc power collection system are presented to verify the effectiveness of the fault-handling capability of the DSCC-based FTF system.

5.2 DC Power Collection for Offshore Wind Farms

A dc-dc layout for power collection along with multi-terminal dc transmission is a promising candidate for future offshore wind farms [22]–[24], [35]–[41], [52]–[54]. A high-power dc-dc transformer aimed for large dc grids should provide three main functions,



(a)

(b)

(c)

Fig. 5.1: Several configurations of dc power collection using the FTF system.

that is, voltage stepping, voltage or power regulation, and fault isolation [39]. In particular, a vulnerability to dc faults that may hinder the development of a multi-terminal dc grid should be overcome by the dc-dc transformer or other alternatives instead of using costly dc breakers [45], [51], [61], [62]. An FTF system configuration based on DSCC converters can provide an isolated power-collection capability in addition to the three main functions of dc-dc transformer.

Fig. 5.1 shows three possible configurations using the FTF system for dc power collection. The first configuration, shown in Fig. 5.1(a), uses two high-power converters for power collection and transmission. Both converters of the FTF system uses the same power rating but with different voltage rating. All the distributed dc power generations are connected to the medium-voltage dc grid on the low-voltage side of the FTF system, hence the dc output voltages from the power generation units should be controlled to match the dc grid voltage. The second configuration, shown in Fig. 5.1(b), uses one low-voltage-side converter of the FTF system for each dc power generation unit. The power collection is done trough the ac coupling of the ac link terminals of the low-voltage-side converters on the FTF system. This configuration allows the interconnection of uncontrolled dc output voltages from the power generation units. Moreover, dc circuit breakers are not needed and fault protection can be handled by the converter operation, whereas the first configuration requires medium voltage dc circuit breakers for fault protection. However, the second configuration uses more converters than the first one. The last configuration, shown in Fig. 5.1(c), is an alternative to the second configuration, where instead of using one big transformer for ac coupling and galvanic isolation, it uses one transformer for each low-voltage-side converter on the FTF system. This configuration interconnects the power generation units at the ac terminals of the high-voltage-side of the FTF system. Note that each transformer used in this configuration has smaller rated power and higher allowable voltage ratio.

Fig. 5.2 shows the proposed a dc power collection based on an FTF system applicable for the interconnection of offshore wind-farms to inland grids. A DSCC converter (as shown in Fig. 3.1) can be regarded as a building block for the interconnection of several dc power generation based on the FTF system. The dc power collection in one cluster of power generation is achieved by interconnecting several converters at their ac terminals, forming front-to-front configuration consisting of many DSCC converters. The power from the wind turbines are collected by the power-collecting side DSCC converters. A large DSCC at the power-transmitting side convert the ac power at the ac-link to dc power before transmit the power to the inland grid.

A medium frequency transformer steps up the voltage from the power-collecting side voltage level to a higher voltage. The frequency of the transformer used here can be 50/60 Hz or higher to reduce the size of the transformer and passive components. The reduction on the size of the passive components is very important in an offshore applications. Moreover, the galvanic isolation can be achieved by using one transformer for each power-collecting converter (or a multi-winding transformer) or a single large transformer with

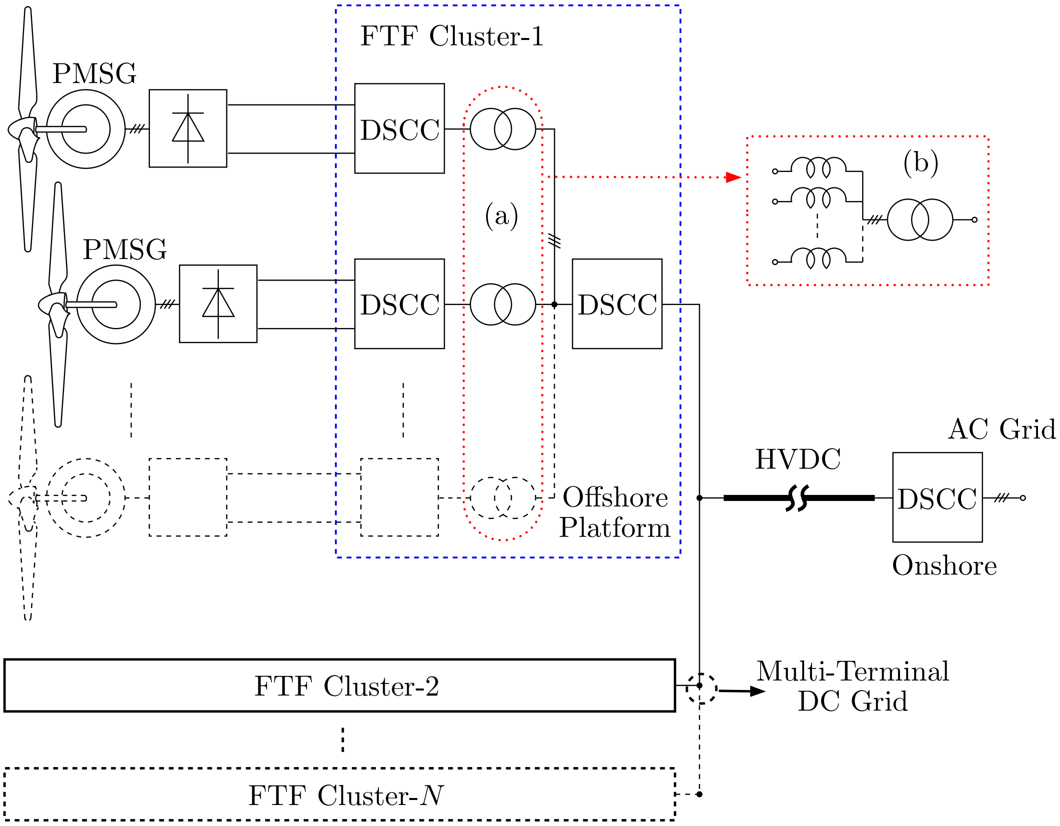


Fig. 5.2: The proposed system configuration of a dc power collection for offshore wind farms based on the FTF system. (a) Using one transformer for each slave converter. (b) Using one big transformer with ac-link inductances for all converters.

line inductances. This interconnection adopts the configurations on Figs. 5.1(c) and 5.1(b), respectively.

Offshore medium-voltage dc-dc power converters are not needed in the proposed dc power collection since the dc output voltage from each turbine is directly connected to a large power collection and transmission system. This power collection and transmission design could be advantageous since a two-voltage-level system is employed [24]. The idea of using series connection of wind turbines may improve efficiency and remove completely the offshore platforms [35], [36]. However, the insulation level of the equipment represents a major practical issue for the proposed configuration.

A combination of a multi-pole permanent magnet synchronous generator (PMSG) with a three-phase six-pulse diode rectifier for dc power generation shows a promising candidate for offshore wind farm applications [30]–[34], [110]. The multi-pole permanent magnet generator enables the variable-speed power generation to operate at its maximum power coefficient over a wide range of wind speed, while at the same time achieving reliability improvement and reducing maintenance expenses since the gearbox and slip-ring parts can be eliminated. It is reported that generator bearings, rotor cables for the slip ring unit, and gearbox failures are the most common causes of low availability of wind turbines [15]. Moreover, although a variable uncontrolled dc voltage will be produced by the three-phase six-pulse diode rectifier, the FTF system can still extract maximum power from wind by varying the input power based on the speed signal from the generator [38], [31].

The proposed system consists of a transmission-side converter and power-collecting-side converters. For offshore wind farm applications, the system could be located in the offshore platform several kilometers away from the wind farm location. The proposed system collects the distributed dc power from wind turbines and transmits the power to the inland grid directly through the HVDC transmission without intermediate converters for medium-voltage elevation. Furthermore, the system offers bi-directional power flow which can provide the wind towers with emergency power from inland grid instead of using diesel generators when on-site maintenance works are needed [16]. The DSBC and DSCC are applicable to the front-to-front application since they have five-terminal circuits to interconnect the dc terminals to the three-phase ac circuit [96]. The DSBC configuration has the advantage on producing a constant ac voltage [110]. It is particularly useful for the power-collecting side converters when the dc-link voltages from wind turbines vary widely depending on wind conditions. Either the DSCC or DSBC configuration can be used for the transmission-side converter. Note that when DSCC converter configuration is utilized, ac circuit breakers should be put at the ac-link of the converter for protective measure. On the contrary, the DSBC can be utilized without the need of ac breakers[109]. Nevertheless, the DSCC configuration offers less switching devices, compared to the DSBC configuration.

The system can be expanded into several subsystems and clusters which may be located in different areas or platforms. Each cluster can have any number of branches of the power-collecting (low-voltage side) converters with independent dc voltage level, which

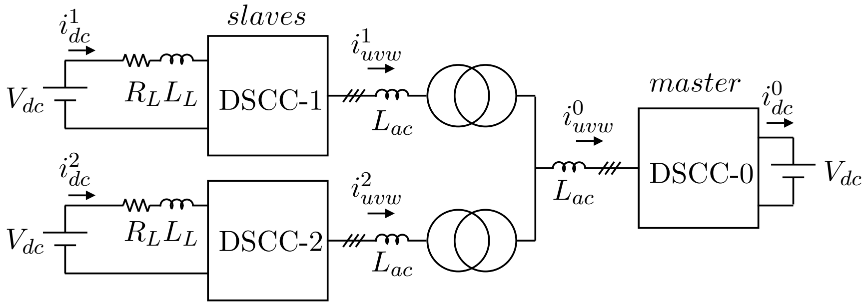


Fig. 5.3: Circuit configuration of a dc power collection based on the FTF system for simulation.

are connected at the ac link of the transmission-side converter. Each power-collecting converter may have a different power rating depending on the generated power at its feeder. Each power-collecting converter may also have a different number of cells per leg. With this configuration, the transmission-side converter will have a power rating equal to the total power rating in the collecting side. The flexibility and scalability of the proposed configuration is very favorable for interconnecting large offshore wind farms or other distributed power generations using renewable energy sources such as photovoltaic.

5.2.1 DC Power Collection System Performance

This section uses only three DSCC converters to form an FTF system as shown in Fig. 5.3 for simulation circuit configuration. The power-collection side uses two slave-mode DSCCs while the transmission-side has a master-mode DSCC with the total rated power of 10 MW. This assumption is made based on 5-MW wind turbines at the power-generating units that are connected to the slave converters. All converters use 16-cell per leg with the dc-side and ac-link voltages of 13.2 kV and 6.6 kV/300 Hz, respectively. For an actual system, the high-voltage IGBT modules with the rated voltage of 3.3 kV [143]–[145] can be used for the power switches in each chopper cell. The rated power and voltage of the master converter should be higher when many slave converters are connected. Table 5.1 summarizes the circuit parameters used for simulation.

The phase-shifted-carrier PWM technique is applied and 16 triangular-carrier signals with the frequency f_C of 1350 Hz are phase-shifted each other by 22.5^o. With this

Table 5.1: Circuit parameters for simulation

Parameter	Symbol	Value
Rated power	P	10 MW
Nominal dc voltage	V_{dc}	13.2 kV
Ac-link voltage	V_{ac}	6.6 kV
Ac-link frequency	f_{ac}	300 Hz
Transformer voltage ratio		1 : 1
Cell count per leg	N	16
DC capacitor	C	1.5 mF
DC capacitor nominal voltage	V_C	1.65 kV
Unit capacitance constant	H	20 ms at 1.65 kV
Ac-link inductor	L_{ac}	0.183 mH (8%)
Center-tapped inductor	L_Z	0.55 mH (23.8%)
DC-line inductance	L_L	1 mH
DC-line resistance	R_L	0.1 Ω
Modulation method		PSC-PWM
Carrier frequency	f_{cr}	1350 Hz
Equivalent switching frequency	Nf_{cr}	21.6 kHz
Dead time		4 μs

( ) on a three-phase 6.6-kV, 10-MW, 300-Hz base

technique, all chopper-cells will have equal switching and conduction power losses. Note that the equivalent switching frequency for each leg is 21.6 kHz for 1350-Hz carrier frequency and 16 carrier-signals operation. The carrier frequency could be decided based on a good compromise between switching losses and ac-link harmonic contents. The higher carrier frequency will produce the higher switching losses but also less harmonic contents. The simulation is conducted by using "PSCAD/EMTDC" software package and a fully digital control method is implemented with a dead time of 4 μs.

Figs. 5.4–5.6 show simulated waveforms for the three converters in the FTF system. DSCC-2 is delivering power of 5 MW while a power transient occurs in DSCC-1 from

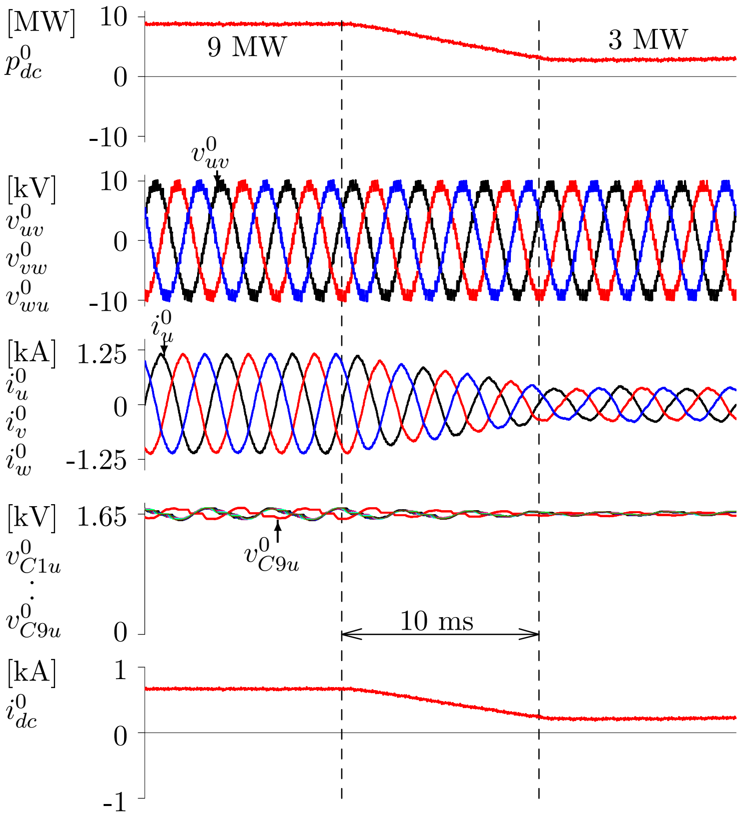


Fig. 5.4: Signal waveforms on DSCC-0 at power reversal on DSCC-1.

4 MW to -2 MW within 10 ms as shown in Figs. 5.5 and 5.6, respectively. Although the power flow is usually from the power-generating unit to the transmitting unit, this case shows that the system is a bi-directional power converter and capable of reversing the power very fast. A reverse power flow is useful when the power generating unit requires an emergency power supply such as when a maintenance is needed in a far offshore location [16]. Fig. 5.4 shows the corresponding power transient in the master converter without altering the operation of DSCC-2. Note that the power flow in DSCC-0 is positive from the ac to dc-link direction, whereas the power direction is positive from dc to ac-links terminals for the slave converters.

The results show that the master-slave combination results in an easy power transfer when many slave converters are to be connected. The use of a decoupled current control on each slave converter enables a fast power command. In actual system of an offshore wind farm, power-command alterations for slave converters are needed to extract the maximum power from the varying wind speed. The power command should follow the

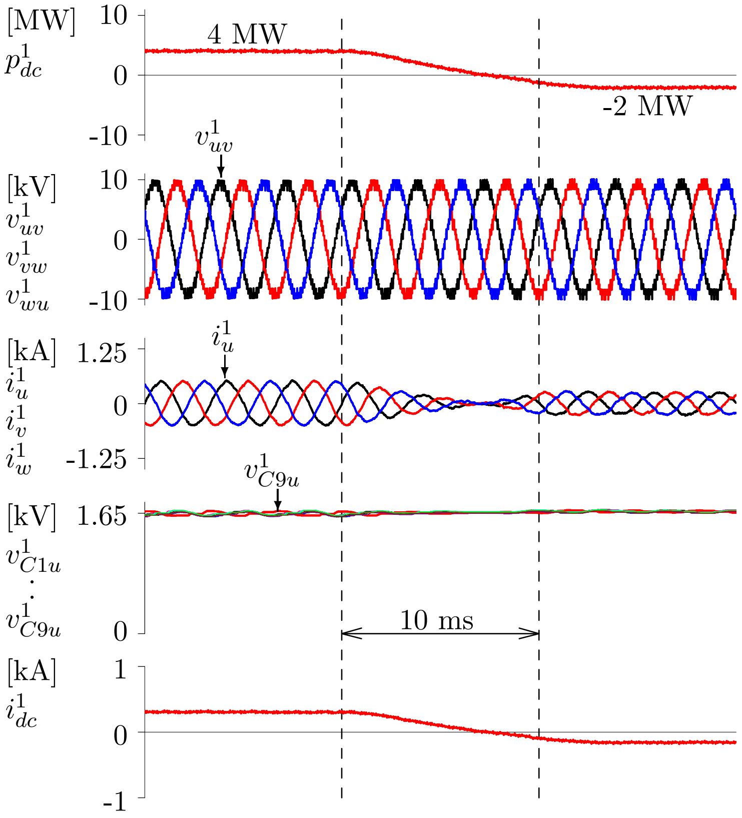


Fig. 5.5: Signal waveforms on DSCC-1 when a power reversal occurs.

maximum-power curve based on the corresponding wind speed. Therefore, a communication signal is required between each wind turbine and the corresponding slave converter to match the power-command on the slave converter to the maximum power from the wind turbine.

Notice that the capacitor voltages on the chopper cells of u-phase leg are balanced although a power transient happens. The capacitor voltage ripple in each converter has different magnitude due to the power distribution difference. Although not shown in the figures, the other capacitor voltages on lower arm of u-phase, upper and lower arms of v-phase and w-phase legs have similar results. From these results, it is obvious that the capacitor balancing control is very effective to maintain the capacitor voltages within acceptable values under steady-state and transient conditions.

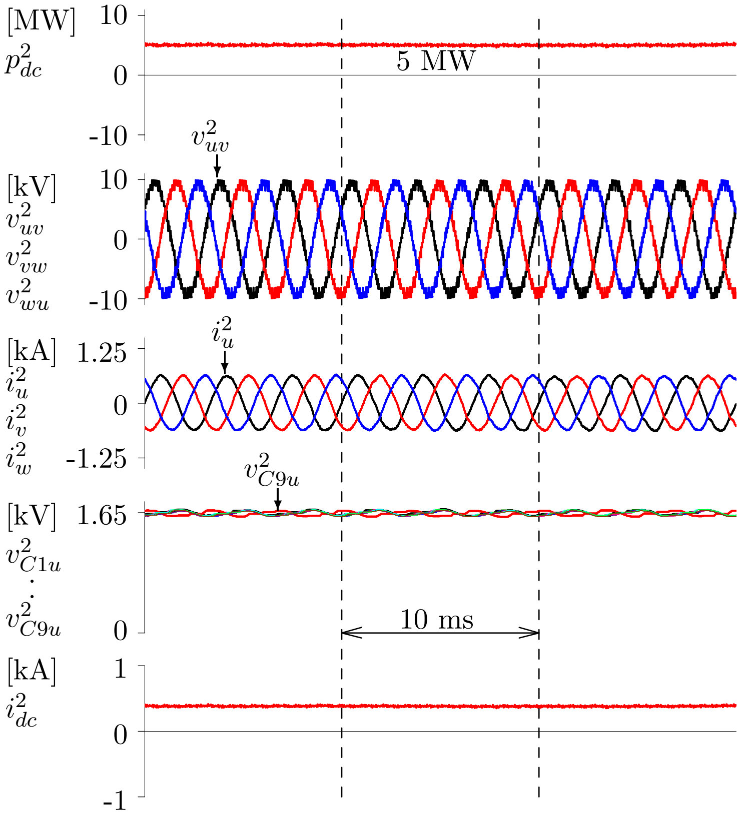


Fig. 5.6: Signal waveforms on DSCC-2 at power reversal on DSCC-1.

5.3 DC Fault-Blocking Capability on the FTF System

DC short circuits may occur on both the transmission side or the power-collecting feeders. For handling dc faults, the proposed system can use the safety-procedure operation of the FTF system with the help of common ac breakers. When a dc fault on the dc transmission side (or dc grid) occurs, all converters in each end of the FTF system should be turned off, avoiding short-circuit current to flow into the converters. Since the fault is handled directly by the converter operation, the rating of the ac circuit breaker may be lower than the nominal load current. When a dc fault occurs in one of the power-collecting feeders, the FTF system should also be turned off to avoid the fault propagation into the larger dc-grid system. The other healthy feeders can operate normally sending power to dc grid after isolating the faulty feeder from the rest of the system. This feature improves the reliability of the dc power-collecting system.

5.3.1 Short-Circuit Protection Scheme

All of the dc and ac currents in the system will fall to zero instantaneously when the system is shut down except for a dc fault current on the faulty feeder caused by the remaining energy in the feeder. Fig. 5.7 shows the current flow after all of the connected DSCCs are turned off by the fault protection control. All of the dc circulating current on each leg of the faulty converter will flow to the fault point trough the lower diode in each chopper cell. Note that the other converters are turned off so that the ac-link voltage becomes zero and no current will flow in the ac-link terminals. The fault current i_{sc} can be determined by the dc circulating current i_Z, dc-line/cable impedance, and converter-arm impedances. Prior to a dc fault, the circuit equation on each leg can be written as follows:

$$v_{dc-leg} = V_{dc} - L_Z \frac{di_Z}{dt} - i_Z R_{leg} - v_L. \tag{5.1}$$

where v_{dc-leg} represents the equivalent dc voltage across a leg in a DSCC; R_{leg} is the equivalent leg resistance; and v_L represents the voltage drop on the dc line impedance from the generating point to the converter. The circulating current depends on the power

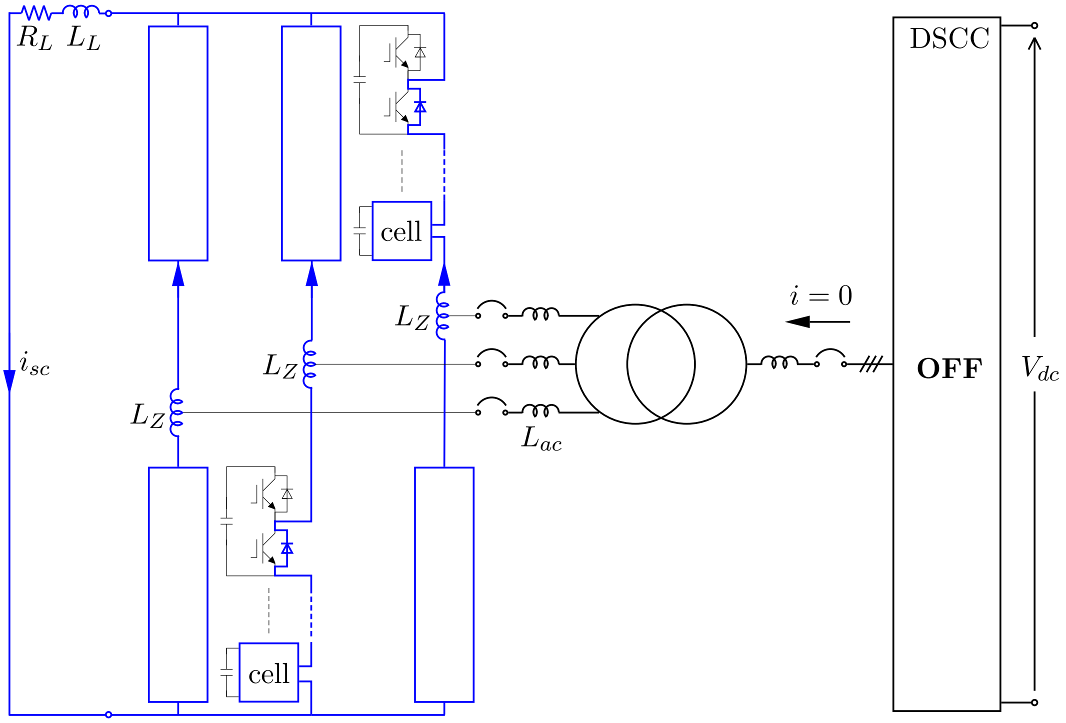


Fig. 5.7: Current path of a dc short-circuit in a DSCC-based FTF system.

prior to the fault. At the fault instant, (5.1) becomes

$$v_{dc-leg} = -L_Z \frac{di_Z}{dt} - i_Z R_{leg} - \alpha v_L. \tag{5.2}$$

where α represents the length factor from the fault point to the converter with respect to the whole distance from the power generating point to the converter.

Equation (5.2) shows that the equivalent dc voltage v_{dc-leg} on each leg is still connected to the short-circuit line until turned off by the fault-current detection control. The fault current will flow due to the moment when the leg voltages are connected to the fault line. Since the switching operation of the converter is very fast, the fault current can be suppressed effectively. The amplitude of the equivalent dc voltage v_{dc-leg} prior to the fault will affect the amplitude of the fault current. Assuming each leg of a three-phase DSCC converter shares equal circulating i_Z prior to a fault, the short-circuit current i_{sc} can be determined as follows:

$$i_{sc} = -3i_Z. \tag{5.3}$$

The peak value of the fault current depends on the impedances of the dc-line/cable and converter arms as well as the power prior to the fault. A very high current may flow

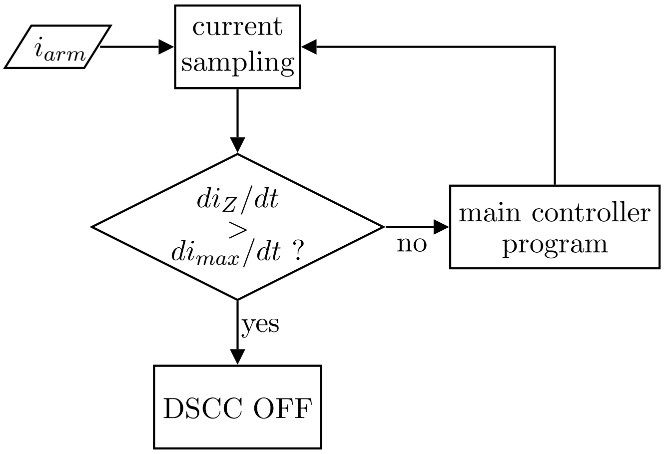


Fig. 5.8: Fault protection flowchart inside the main controller of a DSCC in the FTF system.

and cause damaging the chopper cells in the converter if the DSCC is still connected to the short circuit. Therefore, a fast fault protection control is necessary.

The fault protection control can be a simple di/dt protection limit. It can be put in the same main controller of each DSCC converter. Fig. 5.8 shows a flowchart of the fault protection scheme used for the FTF system. When the fault protection in the controller detects a high di/dt that is passing a certain limit, the converter will be turned off. Thus, the equivalent leg dc voltage on (5.2) becomes zero immediately and the equation becomes a simple first-order circuit. The detection limit should be set low enough to detect a fault occurrence faster, but should be high enough so that a sudden power change will not interrupt the operation of the FTF system. Moreover, the faster the sampling rate of the controller, the faster the fault current can be detected. However, the stored energy on the coupled inductors and dc line inductance is still exist causing the fault current to discharge. The discharging time constant of the short circuit current can be calculated as follows:

$$\tau_{sc} = \frac{\alpha L_L + L_Z}{\alpha R_L + R_{leg}}. \tag{5.4}$$

Equation (5.4) shows that the time constant of the fault current depends on the dc-line/cable and converter-arm impedances. Since the arm resistance should be zero ideally, only the coupled inductor L_Z can be adjusted to limit the fault current. If the L_Z is

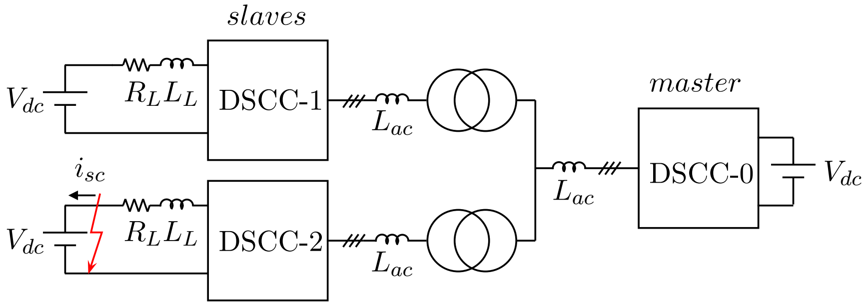


Fig. 5.9: A dc short-circuit occurrence at the feeder of DSCC-2 converter in the FTF-based dc power collection system.

made smaller, then the time constant will be faster but the peak of the fault current will be higher. On the other hand, if the L_Z is made bigger, then the peak of the fault current will be smaller but time constant will be longer. While we cannot change the dc-line impedance, the arm inductance can be adjusted and depends on the ac-link frequency operation. Therefore, although the use of a higher switching frequency enables the use of smaller coupled inductors, the fault-current amplitude might be compromised. Thus, a trade-off should be made between a lower peak current or a faster time constant.

5.3.2 System Performance Under DC Fault

In this section, the dc power collection using three DSCC converters is simulated under a dc fault on one of the power-collecting feeders as shown in Fig. 5.9. The fault position is assumed to be in the same point as the dc voltage source in the faulty feeder. The circuit parameters are the same as those in Section 5.2.1. The aforementioned protection scheme is employed in the controller with the di_{max}/dt limit of 5400 kA/s.

Figs. 5.10–5.12 show simulated waveforms of the converters in the FTF system under a dc fault occurrence. Prior to the fault, DSCC-1 and DSCC-2 are sending the power of 4 and 5 MW, respectively, to DSCC-0 as a master converter. The fault occurs at the dc feeder of DSCC-2 at $t = 0$. As soon as the protection limit di_{max}/dt is violated, the system turns off the switching operation of the whole FTF system resulting the ac-link voltages to fall down to zero instantaneously. Consequently, the power flow is halted and no current is flowing on the ac-link terminals.

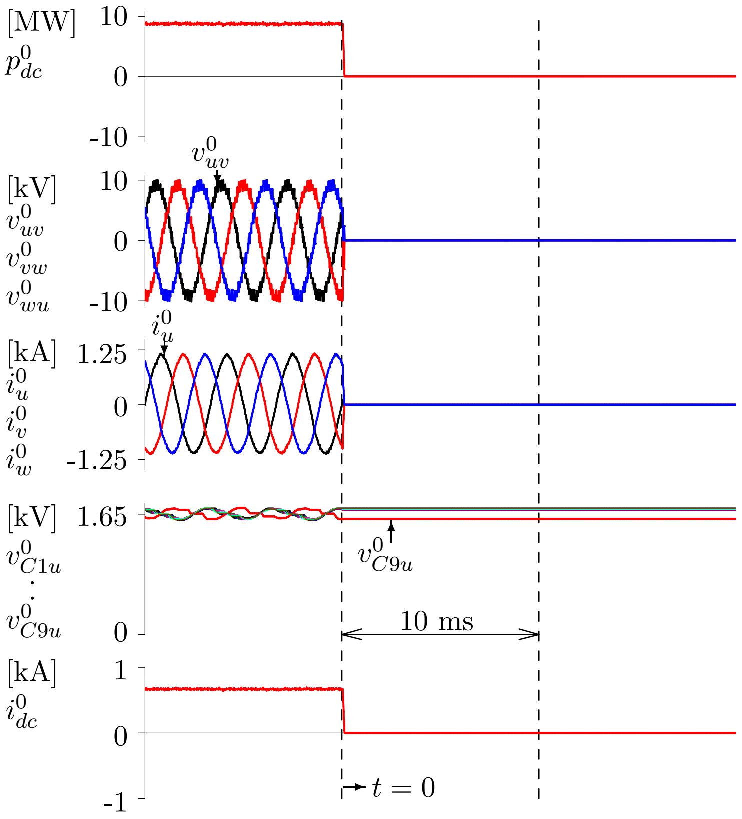


Fig. 5.10: Signal waveforms of DSCC-0 on fault occurrence of the feeder of DSCC-2 at $t = 0$.

The simulated waveforms show that when a dc fault occurs on the feeder of DSCC-2 at $t = 0$, the FTF system can act very fast to block the fault current. Since DSCC-2 operates in inversion mode, the dc current starts to reverse its amplitude when the fault occurs as shown in Fig. 5.12. The stored energy on the coupled inductors within the converter L_Z and the dc-line inductance L_L will cause a discharging process of the short-circuit current. Note that the dc currents on the other converters are blocked almost instantaneously without overshoot as shown in Figs. 5.10 and 5.11. Note also that the dc capacitor voltages on the chopper cells are only slightly different from the nominal value after the fault.

The fault current amplitude depends on the impedances within the converter legs and the dc-line/cable impedance from the converter to the fault location. Fig. 5.13 shows the short-circuit current under several different values of coupled inductor L_Z. The discharging time and current-overshoot amplitude will need to be compromised by

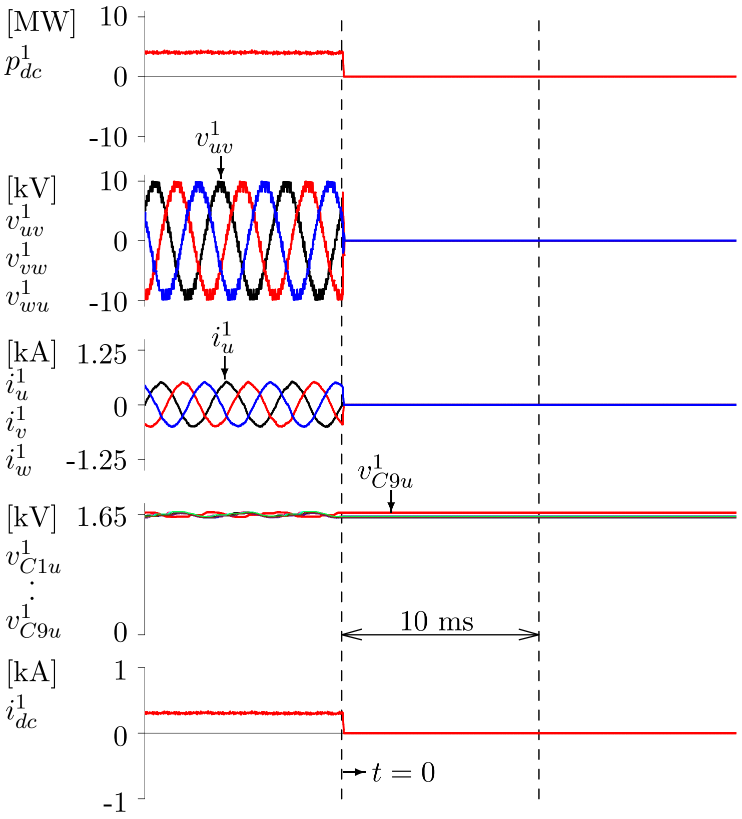


Fig. 5.11: Signal waveforms of DSCC-1 on fault occurrence of the feeder of DSCC-2 at $t = 0$.

adjusting the values of the coupled inductors L_Z to get the permissible peak amplitude of the fault current.

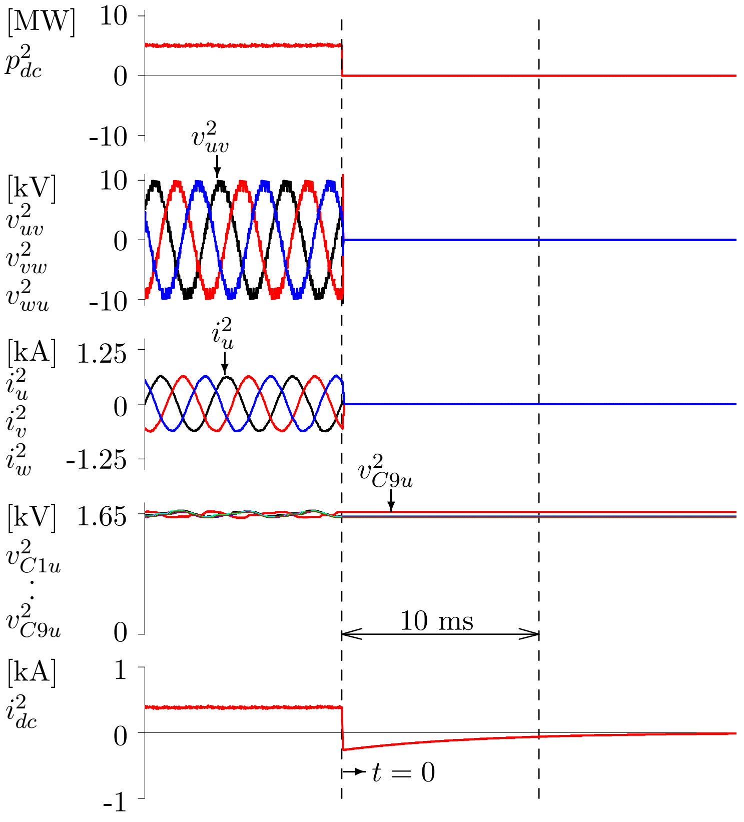


Fig. 5.12: Signal waveforms of DSCC-2 on fault occurrence of the feeder at $t = 0$.

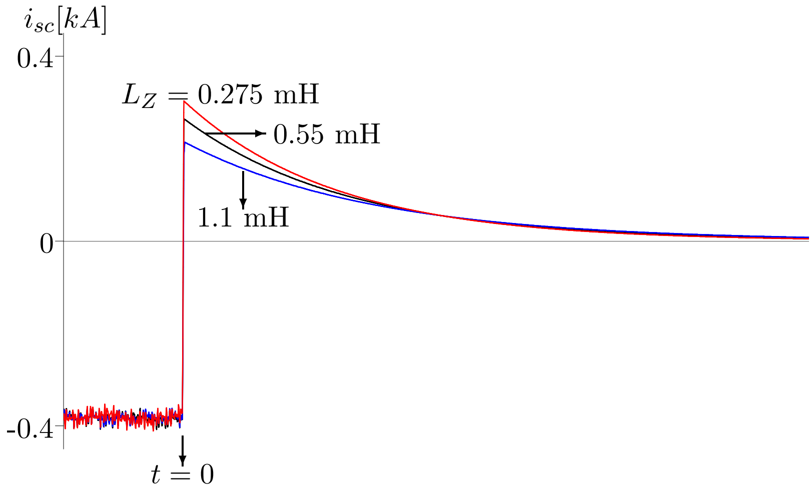


Fig. 5.13: Comparison of short-circuit current i_{sc} for several values of center-tapped inductors L_Z.

5.4 Summary

A dc power collection based on the FTF system utilizing many DSCC converters has been proposed in this chapter. The proposed dc power collection offers a flexibility in terms of the number and rating of slave converters connected to the system. Moreover the FTF system is scalable allowing the connection of several clusters of FTF systems to form a larger dc power collection system. The power-flow control in the FTF system can be performed by implementing a slave-mode operation on each of the collecting-side DSCCs while the transmission-side DSCC acts as a master converter. The decoupled current control used in each slave converter enables an easy power transfer to the master converter without interfering the operation of other slave converters that are connected to the same ac-link. Since, the ac-link voltage and frequency is determined and controlled by the master converter, no voltage sensor nor PLL circuit is required at the ac-link terminals. Furthermore, the fast fault-blocking capability of the FTF system has also been discussed in this chapter. The system handles dc faults effectively by turning off the operation of all converters connected to the same ac-link without the need of dc circuit breakers. The maximum amplitude and the discharging time constant of the fault current on the faulty feeder is highly dependent on the leg impedances, dc-line impedance between the fault point and the converter, the di/dt protection limit, as well as the current sampling rate. The simulated results have verified the performance of the proposed dc power collection based on the FTF system under steady and transient conditions as well as the fault-handling operation.

Chapter 7

Conclusion and Future Research

7.1 Conclusion

This dissertation covers a comprehensive discussion on a high-power front-to-front (FTF) system configuration based on modular multilevel double-star chopper-cells (DSCC) converters and its application on dc power collections. Reviews on the various topologies of power collection and transmission system for future large offshore wind farms discussed in Chapter 2 lead to an indication that a dc-dc layout is a promising candidate. The dc-dc layout requires less power converters on the nacelle of wind turbines and has higher reliability and flexibility than the ac-dc layout. Many proposals are published in search for a suitable high-power dc-dc converter that can replace a traditional ac transformer. The proposed FTF system based on DSCC converters has the function of both as a dc transformer and a dc-power collector and transmitter. This dissertation contributes mainly in the following three topics:

■ **Experimental Verification of a DSCC-Based FTF System** This dissertation has provided an intensive discussion on the performance of the FTF system using two DSCC converters based on simulations and experiments. The complete analysis of circuit and control of a DSCC converter provided in Chapter 3 facilitates the preamble to the FTF system operation. The proposed master-slave configuration controls the power flow easily between the two DSCC converters. The ac-link voltage and frequency is determined and controlled by the master converter, which eliminates the need for ac voltage sensors or PLL circuit. A feedback and a feedforward controllers for a reactive power compensation have been proposed for the FTF system. The reactive power compensation enables a unity power factor to be put at the middle point of the FTF system, avoids overvoltages, and maintains the ac terminals of the slave converter at its nominal value. The simulated and experimental results provided in Chapter 4 verify the effectiveness of the FTF system and its control strategy as a high-power, bidirectional, and isolated dc-dc converter. Both the simulated and the experimental waveforms agree very well with each other not only in steady states but also in transient states, which enhances the reliability and validity of both the simulations and the experiments conducted in this research.

■ **Performance Verification of the FTF System for a DC Power Collection** This dissertation has discussed and verified the performance of a dc power collection based on the FTF system utilizing multiple DSCC converters. The proposed system provides flexibility and scalability as a dc power collection. The master-slave configuration proposed in Chapter 4 enables an easy power transfer between each slave converter to the master converter without interfering the operation of other slave converters that are connected to the same ac-link. This dissertation has also discussed the fast fault-blocking capability of the FTF system without the need of dc circuit breakers. The determination of the fault current amplitude and the discharging time constant has been provided, and an easy protection control scheme has been proposed. The simulated results provided in Chapter 5 have verified the performance of the proposed dc power collection based on the FTF system under steady and transient conditions as well as the fault-handling operation.

■ **Low-Switching-Frequency Operation With a Rotating-Carrier PWM** This dissertation has proposed a new modulation method based on a phase-shifted rotating-carrier PWM (PSRC-PWM) for a DSCC converter intended for high-power applications. A thorough discussion on a PWM method at a low carrier-frequency ratio with respect to the ac-grid frequency (CFR) has specified several constraints of using a phase-shifted-carrier PWM method. The PSRC-PWM method opens possibility of using a low CFR because of the inherent balancing capability on the capacitor voltages and the arm-side voltages of all cells. The harmonic equation of the arm-side voltage of a chopper cell with

PSRC-PWM has been derived analytically, and compared to the numerical result. The PSRC-PWM method has been verified by simulations using a 100-MW, 66-kV, and 50-Hz DSCC system resulting in a stable operation of the DSCC converter, and a balanced condition on the capacitor voltages although the carrier frequencies are in the range of 20–100 Hz. Based on several performance criteria, this dissertation has concluded that the optimal CFR is 3/2 for carrier frequencies that are lower than double the ac-grid frequency. The FTF system discussed in Chapters 4 and 5 can gain benefits from the PSRC-PWM by implementing a medium ac-link frequency in a kilohertz-frequency range without the need of using a much higher switching frequency. As a result, the weight and volume of the ac-link transformer and the passive components on the chopper cells can be reduced significantly, while high switching power loss can be avoided at the same time.

7.2 Future Research

■ **Efficiency Estimation** This dissertation did not cover efficiency estimation of the FTF system based on DSCC converters. The aim of this system configuration is for a dc power collection that has been discussed in Chapter 5. The FTF system can also be categorized as a solid-state transformer (or a dc transformer) that transform a dc voltage level to another voltage level. Therefore, the efficiency of the system should match or at least close to the traditional ac transformers. Further work is needed to estimate the efficiency of the DSCC-based FTF system. A trade-off between the switching losses and size-reduction gain on the passive components when using a higher medium-frequency ac-link operation should also be considered to obtain the applicable ac-link frequency range against the power rating of the FTF system.

■ **Experimental Verification of the Proposed PSRC-PWM** The experimental and simulated results presented in Chapter 4 are agree very well with each other. Therefore, although only simulated results are presented in Chapters 5 and 6, the author of this dissertation believes that the the simulation system and its results are reliable. Nevertheless, an experimental verification of a DSCC converter using the PSRC-PWM is also important to have more solid proof and to reconfirm the simulated results. Furthermore, the simulated results of the downscaled system using the PSRC-PWM presented in Section 6.7 represents a drawback regarding the use of low number of cell in a DSCC converter with PSRC-PWM. Therefore, a compensation method to remove or reduce the voltage spike is necessary in a DSCC converter with low number of cells such as the downscaled system presented in Chapter 3.

■ **Operation Under Chopper-Cell Failures** A fault-tolerant capability is a very important feature for a power converter. Since a DSCC converter has many series-connected chopper cells, failures on several cells might compromised the normal operation of the system. The fault-tolerant capability enables the DSCC converter to maintain continuous operation although several chopper cells fail to operate normally or are at fault. One of the advantages of the DSCC topology is a redundant chopper-cells connection where several chopper cells can be put in each arm as reserved cells and operate in a stand-by mode. Therefore, the fault-tolerant capability and redundant connection of chopper cells can improve the reliability of the DSCC converter especially when the converter is to be located in a location that has limited access such as an offshore platform.

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List of Publications

Journals

[1] F. Sasongko, K. Sekiguchi, K. Oguma, M. Hagiwara, and H. Akagi, "Theory and experiment on an optimal carrier frequency of a modular multilevel cascade converter with phase-shifted PWM," *IEEE Transactions on Power Electronics*, vol. 31, no. 5, pp. 3456–3471, May 2016.

[2] F. Sasongko and H. Akagi, "Low-switching-frequency operation of a modular multilevel DSCC converter with phase-shifted rotating-carrier PWM," *IEEE Transactions on Power Electronics* (*conditionally accepted with mandatory revision*)

International Conferences

[1] F. Sasongko, M. Hagiwara, and H. Akagi, "A front-to-front (FTF) system consisting of two modular multilevel cascade converters based on double-star chopper-cells," in *Proc. IEEE International Future Energy Electronics Conference (IFEEC '13)*, Tainan, Taiwan, Nov. 3–6, 2013, pp. 488–493.

[2] F. Sasongko, M. Hagiwara, and H. Akagi, "A front-to-front (FTF) system consisting of multiple modular multilevel cascade converters for offshore wind farms," in *Proc. International Power Electronics Conference (IPEC/ECCE-ASIA'14)*, Hiroshima, Japan, May 18–21, 2014, pp. 1761–1768.