論文 / 著書情報
Article / Book Information

題目(和文)	CMOS集積回路による分周器を用いない低ジッタクロック発生器の研究
Title(English)	A Study of Low-Jitter Divider-Less CMOS Clock Generators
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出典(和文)	学位:博士(学術), 学位授与機関:東京工業大学, 報告番号:甲第10564号, 授与年月日:2017年3月26日, 学位の種別:課程博士, 審査員:岡田 健一,松澤 昭,益 一哉,髙木 茂孝,伊藤 浩之,滝波 浩二
Citation(English)	Degree:Doctor (Academic), Conferring organization: Tokyo Institute of Technology, Report number:甲第10564号, Conferred date:2017/3/26, Degree Type:Course doctor, Examiner:,,,,,
学位種別(和文)	博士論文
Category(English)	Doctoral Thesis
種別(和文)	要約
Type(English)	Outline

Thesis Outline

This dissertation presents a study of low-jitter clock generation techniques using divider-less phase locked loops. Clock generator is one of the most important component in modern electronic communication and are used for various applications. This thesis deals with two of the main roles of clock generators in electronic communication; carrier signal generation and clock and data recovery. The importance of clock generators in modern electronic communication systems is briefly discussed in chapter 1 of this thesis.

A phase locked loop (PLL) based clock generator is selected as the base architecture due to its versatility. The jitter (or phase noise) present in the PLL affects the quality of communication in various ways, which sets maximum limits on the performance of the communication system such as the maximum achievable speed, maximum communication distance etc.. In order to improve the quality of communication, the jitter in the clock generator needs to be reduced. Analysis of the PLL is carried out in chapter 2 to determine major factors affecting the noise generation in PLL based clock generators. Based on the observations from the phase noise analysis of the PLLs, jitter reduction techniques can be broadly classified into two categories (i) inband phase noise reduction techniques and (ii) outband phase noise reduction techniques. It is recognized from the analysis that in a PLL, the voltage controlled oscillator (VCO) is the major contributor to the outband noise whereas the loop components of the PLL are the major sources of noise affecting the inband phase noise.

Chapter 3 of this thesis explores outband phase noise reduction by improving the noise performance of the voltage controlled oscillator (VCO). Since VCO is also one of the major power consuming component in a PLL based clock generator, special care is taken to ensure that the VCO techniques proposed in this thesis achieves phase noise reduction without significantly increasing the power consumption. The thesis presents three VCO architectures, namely, (i) adaptive tail-feedback VCO, (ii) pulse-VCO, and (iii) pulse-tail-feedback VCO for reducing the oscillator phase noise without compromising the power consumption. The VCOs proposed in this thesis are implemented in 180nm CMOS technology and the effectiveness of the implemented techniques are verified in cleanroom measurements.

The analysis carried out in chapter 2 shows that removing the divider from the PLL helps in the reduction of the jitter by lowering the inband phase noise. Two divider-less PLL techniques namely, (i) sub-sampling technique and (ii) injection-locking technique are discussed. The unique set of characteristics possessed by each of these techniques makes them ideal candidates for use in different clock generation applications; for example, sub-sampling PLL based clock generators are suitable for frequency synthesis applications whereas injection-locking PLL based clock generators are more

suitable in clock data recovery applications.

A fractional-*N* frequency synthesizer is presented in chapter 3, which utilizes sub-sampling technique for bypassing the use of a divider. The fractional-*N* sub-sampling PLL (F*N*-SSPLL) presented in this thesis utilizes techniques such as pipelined phase interpolation, fast-frequency acquisition and highly-efficient VCO design for achieving low-jitter performance with low-power consumption. The F*N*-SSPLL proposed in this thesis is fabricated using 65nm CMOS technology. The fabricated prototype achieves 116fs rms jitter in integer-*N* mode with a power consumption of 2.82mW and an rms jitter of 133fs in fractional-*N* mode with a power consumption of 6.2mW. The figure of merit of the prototype is calculated at 250dB, which is the highest reported to this day for a fractional-*N* PLL based clock generator.

Injection-locking; another divider-less PLL technique, is used for designing the clock data recovery (CDR) system presented in chapter 4. Thanks to the wide bandwidth of the injection-locking technique, the CDR achieves fast locking and larger suppression of the voltage controlled oscillator noise, which are essential for enabling high data-rates. The architecture presented in this thesis is implemented in all-digital domain using only digital design flow. This reduces the time-to-market and the cost of production. This clock data recovery system presented in this thesis also employs several techniques such as phase-filtering, edge-injection and coupled oscillator for reducing the jitter and improving the reliability in an all-digital implementation framework. A prototype of the proposed CDR is implemented in 28nm FD-SOI process. While operating with a 10.06Gbps 2^7-1 PRBS data, the prototype achieves 0.7ps rms-jitter in the recovered clock with a power consumption of 16.1mW. This corresponds to a state-of-the art energy efficiency of 1.6pj/bit.

Finally the conclusions of the thesis is presented in chapter 5 along with some of the possible future directions of the research work.