# 論文 / 著書情報
# Article / Book Information

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| 題目(和文) | CMOS集積回路による分周器を用いない低ジッタクロック発生器の研究 |
| Title(English) | A Study of Low-Jitter Divider-Less CMOS Clock Generators |
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（博士課程）
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# 論文要旨

THESIS SUMMARY

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| 専攻：<br>Department of | Physical Electronics 専攻 | 申請学位（専攻分野）：<br>Academic Degree Requested | 博士 (Philosophy)<br>Doctor of |
| 学生氏名：<br>Student's Name | Tharayil Narayanan Aravind | 指導教員（主）：<br>Academic Advisor(main) | Kenichi Okada |
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要旨（英文 800 語程度）
Thesis Summary（approx.800 English Words ）


This dissertation presents a study of low-jitter clock generation techniques using divider-less phase locked loops. Clock generators are an important part of the electronic communication and are used for various applications. This thesis deals with two of the main roles of clock generators in electronic communication; carrier signal generation and clock and data recovery.

A phase locked loop (PLL) based architecture is selected as the base architecture for clock generator due to its versatility. Analysis of the phase locked loops is carried out to determine major factors affecting the noise generation. Based on the observations from the phase noise analysis of phase locked loops, jitter reduction techniques are broadly classified into two categories (i) inband noise reduction techniques and (ii) outband noise reduction techniques.

Divider-less PLLs are capable of providing very low inband phase noise performance. Two divider-less PLL techniques namely, (i) sub-sampling technique and (ii) injection locking technique are discussed. Each of these techniques possess a unique set of characteristics that makes them ideal candidates for use in different clock generation application; sub-sampling is identified as a suitable candidate for frequency synthesis applications whereas injection locking clock generation is more suitable in clock data recovery applications.

A fractional-N frequency synthesizer is designed using sub-sampling technique. The fractional-N sub-sampling PLL (FN-SSPLL) presented in this thesis utilizes techniques such as pipelined phase interpolation, fast-frequency acquisition and highly-efficient VCOs for achieving low-jitter performance with low-power consumption. The FN-SSPLL proposed in this thesis is fabricated using 65nm CMOS technology. The fabricated prototype achieves 116fs rms jitter in integer-$N$ mode with a power consumption of 2.82mW and an rms jitter of 133fs in fractional-$N$ mode with a power consumption of 6.2mW. The figure of merit of the prototype is calculated at 250dB, which is the highest reported to this day for a fractional-$N$ PLL based clock generator.

Injection-locking; another divider-less PLL technique, is used for designing a clock data recovery (CDR) system. Thanks to the wide bandwidth of the injection-locking technique, the CDR achieves fast locking and larger suppression of the voltage controlled oscillator noise. This enables implementation of the system in all-digital domain which is fully-synthesizable, which reduces the time-to-market and thus the cost of production. This work also employs several techniques such as phase-filtering, edge-injection and coupled oscillator for reducing the jitter and improving the reliability in an all-digital implementation framework. A prototype of the proposed CDR is implemented in 28nm FD-SOI process. While operating with a 10.06Gbps $2^7$-1 PRBS data, the prototype achieves 0.7ps rms-jitter in the recovered clock with a power consumption of 16.1mW. This corresponds to a state-of-the art energy efficiency of 1.6pj/bit.

Apart from the systems mentioned above, the thesis also explores outband phase noise reduction by improving the noise performance of the voltage controlled oscillator (VCO), which is also one of the major power consuming component in a PLL based clock generator. The thesis presents three architectures, namely, (i) adaptive tail-feedback VCO, (ii) pulse-VCO, and (iii) pulse-tail-feedback VCO for reducing the oscillator phase noise without compromising the power consumption. The VCOs are implemented in 180nm CMOS technology and the effectiveness of the implemented techniques were verified in cleanroom measurements.


備考 ： 論文要旨は、和文 2000 字と英文 300 語を 1 部ずつ提出するか、もしくは英文 800 語を 1 部提出してください。
Note : Thesis Summary should be submitted in either a copy of 2000 Japanese Characters and 300 Words (English) or 1copy of800 Words (English).

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