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Title of thesis:

A Study of Synthesizable Phase-Locked Loop for Clock Generation

Outline of thesis:

This dissertation presents a study of synthesizable phase-locked loop (PLL) for clock generation in CMOS technology. By using injection locking technique, a low-power, low-cost and high performance synthesizable PLL can be implemented using digital standard cells without any modification, and automatically place-and-routed by a digital design flow without any manual placement. It achieves a FoM of -236.5dB with the layout area of 0.0066mm^2. To further improve the phase noise performance, a low-jitter mostly synthesized phase-locked loop based on injection-locking technique, with LC-based digitally controlled oscillator (DCO), is proposed. Different from ring-based DCO used in the conventional synthesizable injection locked PLL with a high reference, LC-based DCO is firstly proposed based on 3-input NAND for a low-reference IL-PLL. It achieves a FoM of -250.3dB, the best one among synthesizable PLLs. The synthesizable PLLs can achieve comparable performance with low power and small area. In order to satisfy the frequency resolution requirement, a Fractional-N IL-PLL is investigated and implemented. In order to relax the deteriorate spur level due to hard switching using injection locking; a soft injection technique is employed to improve the spur performance. A 28 phase coupled ring oscillator is utilized to generate multi-phase, while the gating controller is used to control logic which determine the phase of the injection signal. The typical FoM is -224.6dB at the output frequency of 1.5222GHz. The fully synthesizable two-stage Fractional-N PLL consumes little area and provide low jitter clock generator.