論文 / 著書情報
Article / Book Information

題目(和文)	
Title(English)	Millimeter-Wave CMOS Transceiver Toward 100Gb/s Communication Systems
著者(和文)	TokgozKorkutKaan
Author(English)	Korkut Kaan Tokgoz
出典(和文)	学位:博士(学術), 学位授与機関:東京工業大学, 報告番号:甲第10891号, 授与年月日:2018年3月26日, 学位の種別:課程博士, 審査員:岡田 健一,松澤 昭,益 一哉,髙木 茂孝,伊藤 浩之,川野 陽一
Citation(English)	Degree:Doctor (Academic), Conferring organization: Tokyo Institute of Technology, Report number:甲第10891号, Conferred date:2018/3/26, Degree Type:Course doctor, Examiner:,,,,,
学位種別(和文)	博士論文
Type(English)	Doctoral Thesis

Millimeter-Wave CMOS Transceiver Toward 100Gb/s Communication Systems

by

Korkut Kaan Tokgoz

A Ph. D. dissertation submitted in partial satisfaction of the requirements for the degree of

Department of Physical Electronics

in the

Graduate School of Science and Engineering

of

Tokyo Institute of Technology

Supervised by

Prof. Kenichi Okada and Prof. Akira Matsuzawa

Winter 2017

To my family,

Acknowledgment

First of all, I would like to thank Prof. Kenichi Okada, and Prof. Akira Matsuzawa for giving me this wonderful opportunity to be a part of Matsuzawa&Okada Laboratory, and Tokyo Institute of Technology.

I would like to express my sincere thanks to Prof. Kenichi Okada, for his valuable guidance till now starting from the day of enrollment. Even with his very busy schedule, he always spent his valuable time on not only technical issues, but also on writing, presentation skills, and daily life talks. I am thankful for his advices, comments, and suggestions on every issue. For sure, without his guidance this work could not be done. In short, I appreciate his trust in me.

I am very grateful to Prof. Akira Matsuzawa for his help and support from the day I arrived in Japan. His advices on every issue is very valuable and I always tried to follow them.

I would like to thank Yoshino Kasuga and Makiko Tsunashima for their valuable helps and time on applications, documents, registrations and monthly reports for several different topics. Their advices and explanations on these issues are always very helpful.

I am also grateful to Prof. Kazuya Masu, Prof. Shigetaka Takagi, Prof. Hiroyuki Ito, from Tokyo Institute of Technology, Tokyo, Japan; and Dr. Yoichi Kawano from Fujitsu Lab., Atsugi, Japan for their valuable time for examining my thesis.

I, also, would like to thank Shotaro Maki, Jian Pang, Noriaki Nagashima, Seitarou Kawai, Ibrahim Abdo, Takuya Fujimura, Yuuki Seo, Nurul Fajri, and Kimsrun Lim for their contributions on the works that we have conducted. I am thankful to all of the past and present members of our laboratory for daily conversations and talks.

I am grateful to my parents, Hatice&Serdar Tokgoz, for their endless love, support, prayers and encouragement. I thank my sister Emel (Tokgoz) Yildiz and my brother-in-law Alparslan Yildiz for making Japan homelike being together in Tokyo, and sharing great moments. I thank my little brother Baybars Baturalp Tokgoz for being the joy of our family.

Abstract

In this thesis, millimeter-wave CMOS wireless transceivers are proposed to achieve data-rates of more than 100Gb/s. An ultra-wideband 70-to-105GHz wireless transceiver is implemented on 65nm CMOS technology based on frequency-interleaving architecture. This work achieves the world fastest data-rate of 120Gb/s. Additionally, a 60GHz low-loss transmit/receive switch circuitry is proposed based on re-using LNA and PA transistors as switching elements with matching block design for TDD transceivers. Switch architecture has no area consumption with 1.1dB minimum loss in RX mode and 2.3dB minimum loss in TX mode. Accurate methods on device layout optimization, de-embedding, characterization and modeling are done for both active and passive devices to achieve robust and accurate wireless transceivers. The characterization of devices is done up to 320GHz. A 16-stage 273-to-301GHz amplifier is designed in 65nm CMOS achieving a peak gain of 21dB with a power consumption of 35mW from a 1.2V DC supply.

Contents

List of Figures

List of Tables

Chapter 1

Introduction

1.1 Expectations from Wireless Technology

People, from the beginning of the history, have the desire to reach others who are physically far from themselves. Thus, humanity invented several ways for long-range communications such as the smoke signals, which are just a few bits per hours or so. In time the method, media, and tools are evolved to communication with visible light, telegraph, telephone, radio and television, and so on. After the invention of cellular phones, radio frequency and wireless communication systems have been growing tremendously [1].

Wireless technology in general, has been being developed and has been evolving for several decades and it is continuing to be so. The reasons behind this is the desires and requirements from the society itself. Furthermore, these desires and requirements change in time. For example, the demand by the users for smart-phone usage increased in several ways; such as, higher mobility, quality, and higher data rates of mobile communications.

However, for nowadays wireless technology, the demand on the user end is not the only driving factor. There are several other technologies require the wireless technology to be evolved. A few examples of these driving forces are IoT, IoE, new computational technologies, ultra-high resolution entertainment technologies; such as 3D-TV, 4K, 8K TV, virtual reality, augmented reality and so on. All of these driving forces require higher and higher data to be processed at a given time. Such that, one of the most powerful upstream in wireless technologies is to achieve more and more data rates, as the demand from the users and number of devices connected to wireless networks increase. Some short-range application examples of ultra-high data-rate wireless communications along with required data-rates, range, and application scenarios are listed in [2] and given below in Table 1.1. The user end applications range from high-resolution media entertainment

Table 1.1: Ultra-High Data-Rate Short Range Wireless Communication Applications.

Application	Data-Rate (Gb/s)	Range (m)	Scenario
Internet Access	100	5	NLOS
Ultra HDTV	72	5	NLOS
3D-TV	400	5	NLOS
Kiosk Download	2.5-256	1	LOS
Docking	2.5-256	1	LOS
Peripheral Interconnect	2.5-256	5	NLOS
Clustering of Computers	4-300	5	NLOS
Circuit Board Interconnect	2.5-256	1	LOS
Chip-to-Chip Interconnect	2.5-410	0.5	LOS

to fast indoor internet access. Moreover, chip-to-chip, PCB-to-PCB and clustering of computers are some other emerging applications require high-data-rate. One can observe from the table that the required data-rates may go up to hundreds of Gb/s in the near future. Some of them, are already in demand. Unfortunately, there is no low-cost solution is provided till now to achieve such kind of ultra-high data-rate systems.

The cellular technology keeps growing and, nowadays, 5G systems has been increasingly studied day by day to achieve user end data-rates of 1Gbps to eventually 10Gbps. The increase in this data capacity per user, one has to consider the overall network infrastructure since the overall data transfer from one data-center to another data-center or to a base station increases tremendously. Generally, fiber-optic cables are the first choice for high-speed backhaul networking. Nevertheless, there are two disadvantages of a fiber-optic system over a wireless backhaul system. One is the latency of fiber-optic system is almost two times than that of a wireless system. The other disadvantage of a fiber-optic system on the new 5G cellular system is caused of the required number of base stations in an urban area; such as Tokyo. With the new system, there will be hundreds or thousands of pico or fempto base stations in a metropolitan area. Considering the required data-rate for each user, to place a fiber-optic cable between these thousands of base stations would cause tons of infrastructure works causing time consumption for deployment, cost of the systems and etc. However, an ultra-high speed wireless backhaul point-to-point system can easily solve these infrastructure issues. Fiber systems have been used for decades and it is well-known and well-developed technology. Nevertheless, going below sea, river, or a lake still an issue for a fiber-optic system. Hence, in rural areas, the need for point-point wireless backhaul networks are clear [3]. These kind of backhaul networks do also require hundreds of Gbps in number. Moreover, long range is required for these systems.

Table 1.2: Modulation schemes and their required transmitter to receiver SNDR (EVM) requirements for a bit-error-rate (BER) of 10^{-3}, and the required data bandwidth for a 100Gbps wireless communication data-rate.

BPSK	QPSK	8PSK	16QAM	32QAM	64QAM	128QAM	256QAM
6.8dB	9.8dB	12.8dB	16.5dB	19.5dB	22.5dB	25.5dB	28.5dB
100GHz	50GHz	33.3GHz	25GHz	20GHz	16.7GHz	14.3GHz	12.5GHz

1.2 Methods and Approaches to Increase Wireless Data-Rate

In order to realize higher data rates, there are several methods can be implemented. Mainly there are two general ways to increase the data-rate. One is to increase the spectral efficiency for an predefined bandwidth. The other is to increase the bandwidth for the same spectral efficiency. Table 1.2 represents the required wireless communication quality for different modulation schemes. Moreover, the required bandwidth to achieve a 100Gbps wireless communication for each modulation scheme is included in the figure. For example for the same bandwidth the modulation schemes may become more complex and hence, the spectral efficiency increases. For instance, for the same bandwidth if one upgrade the modulation schemes from BPSK to QPSK, or QPSK to 16QAM, or 16QAM to 256QAM, data-rate doubles. However, every doubling of data-rate by using more complex modulation schemes requires additional 3dB, 6.7dB, 12dB of improvement, respectively, on transmitter to receiver signal to noise and distortion ration (SNDR) or error vector magnitude (EVM). Considering the characteristics of millimeter-wave systems and the difficulty to design high performance millimeter-wave transceivers, increasing the modulation complexity may not always be the best way to achieve ultra-high data-rates. Hence, the modulation scheme should be considered throughout along with several other requirements and capabilities of a system. In the next chapter these considerations are done based on theoretical and calculation based methodology.

Fig. 1.1 and 1.2 represents the data-rate for the IEEE802.11.xx standards. Fig. 1.1 represents the standards of IEEE802.11, IEEE802.11a, IEEE802.11b, IEEE802.11g, IEEE802.11n, and IEEE802.11ac from 1997 to 2014 for frequencies of 2.4GHz and 5GHz. One can observe that the data-rate increases from IEEE802.11b to IEEE802.11a because of increasing bit per symbol (i.e. increasing the modulation complexity). Fig. 1.2 represents the standards of IEEE802.11ad from 2013 to 2024 (expected) for unlicensed 60GHz frequency region. Similar effect of increasing the data-rate can be observed for increasing the modulation complexity from QPSK to 16QAM and to

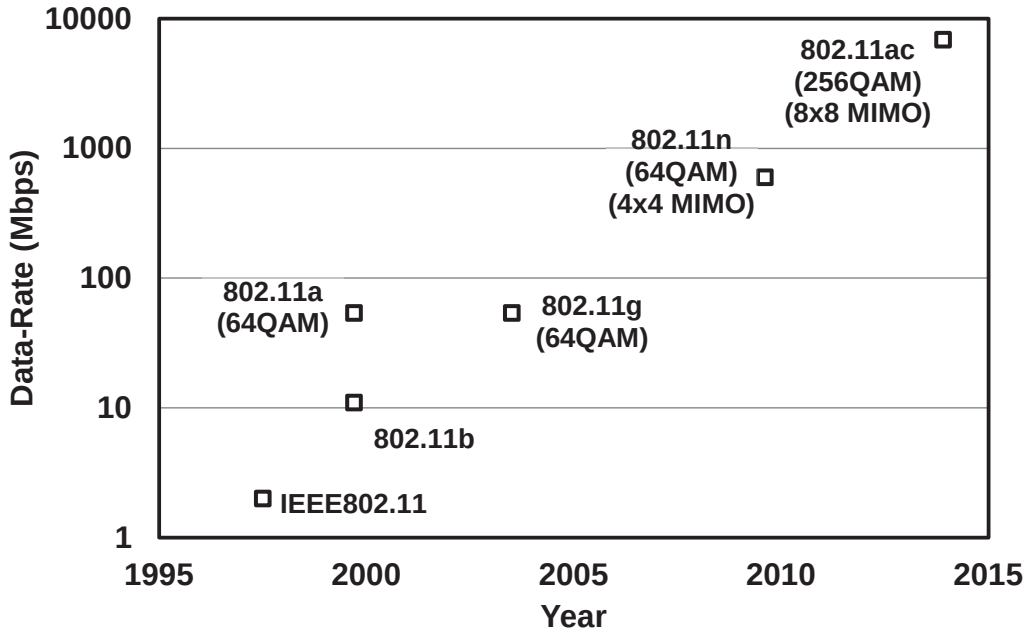


Figure 1.1: Wireless communication standard IEEE802.11, 11a, 11b, 11g, 11n, and 11ac data-rates.

64QAM for 1-channel usage in 60GHz standards. However, as mentioned above, increasing the modulation complexity cannot always solve the problem for higher data-rate demand. A more straightforward way to increase the data-rate is to increase the data bandwidth. Such applications can be observed in Fig. 1.2 between 1-channel 64QAM (2.16GHz data bandwidth) which can achieve 10.56Gbps wireless communications and 4-channel bonding 64QAM (8.64GHz bandwidth) which can achieve a data rate of 42.24Gbps wireless communications. The data-rate and the bandwidth are linearly dependent. However, the transmitter and receiver have to be reconsidered since the bandwidth is multiplied by 4, the noise contribution would increase by 6dB which affects the transmitter to receiver SNDR performance. Hence, the capabilities for the system have to be considered. As mentioned, above an analytical approach is made in next chapter which investigates the way to achieve 100Gbps with ultra-wideband transceivers and optimum modulation complexity.

Another way to increase the data-rate is again based on the spectral efficiency. This way is multi-input multi-output (MIMO) systems. Fig. 1.2 shows that data-rate can be doubled by using 2-by-2 MIMO for 4-channel 64QAM systems as a result 84.48Gbps data-rate can be possible. Moreover, data-rates can go up to 337.92Gbps by

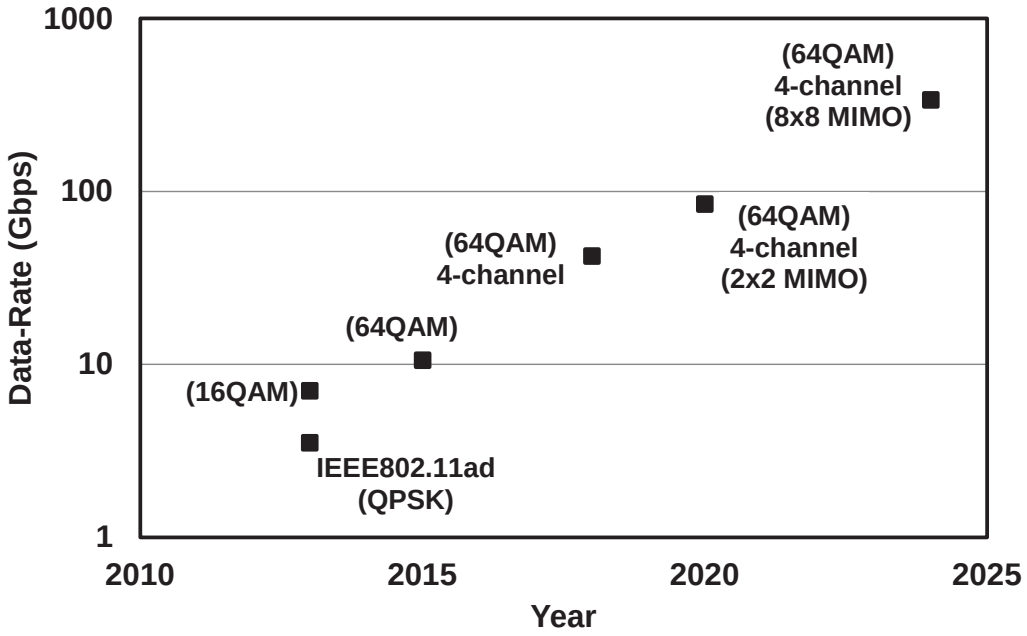


Figure 1.2: Wireless communication standard IEEE802.11ad data-rates.

implementing 8-by-8 MIMO. For this case, 8 transmitters and 8 receivers have to be used. If every transmitter and receiver use one antenna, the overall physical volume, and overall cost of the system increase considerably. Moreover, silicon area consumption has to be considered. In chapter 6, a transmitter-receiver antenna switch architecture is introduced to decrease the overall cost of the system without consuming extra silicon area and having less loss than the conventional approaches at 60GHz.

As it is mentioned above increasing the bandwidth is one solution to increase the data rate of the system. However, for low frequency applications this cannot be the case. This is mainly because; frequency assignments and allocations are very limited for each application in all around the world [4]. Nevertheless, as the frequency increases to millimetre-wave (mm-wave) region larger bandwidths are available. For this reason, mm-wave frequency region attracts attention from both academia and industry, hence; very high speed and high-data-rate wireless transceivers (TRX) become available. For instance, researchers around the world trying to achieve 100Gbps or more data rate using hybrid optical fiber-wireless communications [5, 6] due to the standardization of 100 G Ethernet [5]. These systems are a combination of several different manufacturing technologies; such as, electronics, opto-electronics, fibre, and etc. To provide an example [6], the modulation is done in optical domain. Because air is too lossy for

optical applications, the modulated optical signal is down converted to mm-wave frequency region from 75 to 110GHz using a photo detector. The transmission and reception of signal is done via antennas using W-band (75 to 110GHz). The received signal is first amplified and fed into another optical modulator. Down conversion is done in optical domain. The integration of these systems all together has different challenges, consumes high volumes and power, and the cost of the implementation is increased considerable. Moreover, eventually analog and digital baseband circuitry is needed for data processing at the receiver end. Hence, considering the requirements of the future for wireless technologies a full electronic solution is demanded, such as; implementing the chip with standard bulk CMOS manufacturing technology.

1.3 Millimeter-Wave Research and CMOS

Interest in millimeter-wave (mm-wave) frequency region keeps its importance owing to several characteristics and applications. To name a few of them; larger available bandwidths for high-speed high-data-rate wireless communication applications [7–12], imaging and biomedical applications owing to the characteristics of electromagnetic (EM) waves to pass through nonconducting materials [13–15], availability to use smaller on-chip antennas with increased frequency and single chip RFID applications [16], and so on.

In the past, high-frequency research was mainly based on compound semiconductors, since the transistors in these manufacturing technologies could work on very high frequencies with good performances. Together with the continuous advancements in CMOS fabrication processes the highest working frequencies of transistors are increased year by year and above mentioned systems are became possible to be implemented in CMOS [7–16]. It is worth noting that CMOS processes will continue to evolve and advance in the future as it can be observed from Fig. 1.3 which are pointed out in [17]. According to Fig. 1.3, transistors will work in much higher frequencies which will open up new applications and possibilities for CMOS. The reasons for this shift to CMOS is the several important advantages of CMOS processes. First and most important advantage of CMOS is its much lower cost compared to compound semiconductor counterparts. Monolithic implementation of mm-wave circuits with analog and digital baseband circuitry is another important advantage of CMOS. Moreover, CMOS is a well-known technology studied for several decades.

As mentioned in the above section, optical systems are bulky and more expensive than full electronic implementation solutions. Hence, to decrease the cost and achieve practical usage, semi-conductor base solutions are required. III-V semiconductors have

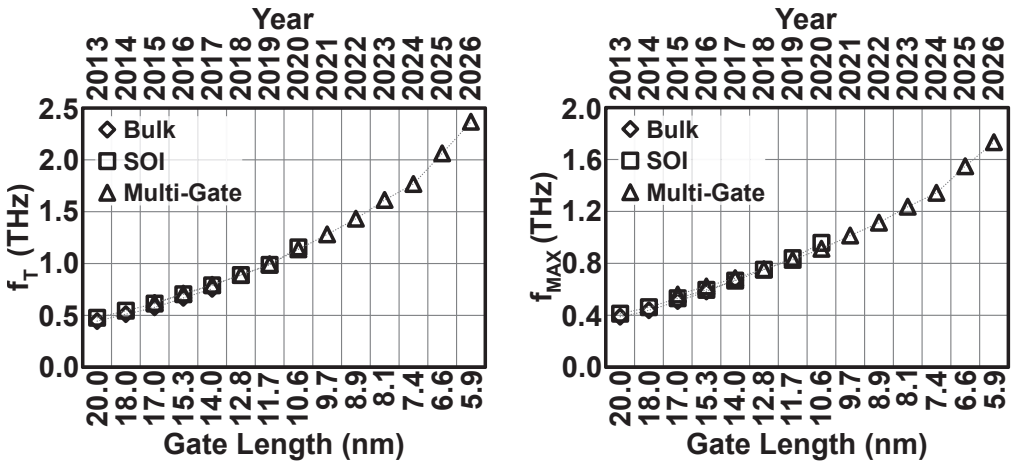


Figure 1.3: Transistors expected performances in terms of (a) Cut-off frequency (THz) vs. gate length (nm) and years, and (b) maximum oscillation frequency (THz) vs. gate length (nm) and years based on ITRS Roadmap of 2013.

been extensively used for millimeter-wave (mm-wave) IC design with advantages of low parasitics, high output power with higher operating frequencies [18–22]. The disadvantage, on the other hand, of these systems is the monolithic integration with baseband circuitry, and the cost of silicon area. CMOS, on the other hand, can be a more viable solution with less cost for mm-wave wireless. Hence, in all of the focus for manufacturing technology in this thesis is CMOS.

1.4 Organization of Thesis

The aim of this thesis is to investigate and achieve millimeter-wave CMOS transceivers toward more than 100Gbps data-rate. The thesis is organized as follows;

In chapter 2, some fundamentals are provided for millimeter-wave wireless transceiver design, such as; optimum carrier frequency and bandwidth along with optimum modulation scheme are investigated based on theoretical approach.

Chapter 3 presents the modeling and characterization of active and passive devices. First, the conventional device characterization approaches are provided. Following to that, improvement of the active and passive device models are provided since the accuracy of the current models are questionable especially after around 70GHz. Differential device characterization approaches and differential de-embedding method for virtual-thru are investigated and presented. Moreover, multi-port device characterization methodologies are provided based on two-port VNA measurements.

Chapter 4 introduces amplifier designs. Amplifiers are a must for a transceiver system, and especially at millimeter-wave frequencies amplifier design is an important concern especially on CMOS. A W-Band LNA design is provided based on positive feedback common-source topology. A 300GHz amplifier design along with measurement results are given on a 65nm standard bulk CMOS process. A bi-directional LNA/PA is introduced for 60GHz frequency region.

Chapter 5 provides all the phases of the design and implementation of an ultra-wideband W-Band frequency-interleave transceiver which achieves world fastest 120Gbps wireless communications.

In chapter 6, a transmitter-receiver switch architecture with no area penalty, unlike the conventional approaches, is introduced with its design methodology. Finally, chapter 7 concludes the thesis.

Chapter 2

Millimeter-Wave Transceiver Design

2.1 Device Characterization and Tile-Based Design

The design of mm-wave circuits starts from the device characterization [7, 12, 23–25]. This is, mainly, because foundaries generally provide models of devices up to around 20 GHz, and these models cannot accurately reflects performances at mm-wave frequency region. Moreover, generally for mm-wave circuits some custom components might be needed, for example transmission lines, corners, tee-junctions, baluns, and etc. Moreover, transistors can be customized according to the needs of the required circuits [26, 27]. For these reasons, mm-wave research has to start to obtain accurate device models working in high-frequency region. In [26], transistors, transmission lines, capacitors and inductors performances tried to be predicted using CAD tools before manufacturing. Transistors are modeled with the combination of PDK model and layout parasitic extracted parasitics. Although, the performances of simulations and measurements of transistors matched well for certain frequency region and related parasitics, some of the parasitic components and performances could not accurately obtained. The authors noted that some of the mismatch are due to the parasitic inductances which are not included in layout parasitic extraction. It is better to note that layout parasitic extraction worked well for this case because the used process is SOI and transistor manufacturing is done in an isolated layer, for which the parasitics are not strongly frequency dependent, rather than in silicon-substrate. The passive components are EM simulated. Using these models the authors designed three different low-noise-amplifiers (LNAs) for Q-, V-, and W-band with state-of-the-art noise performances. Unfortunately, the small-signal measurment results and simulation data are off-balance, for all three. In [27], transistor models are extracted with a combination of PDK model and EM simulating the interconnects up to the connection metallization. This method counts for all possible parasitics as accurate as the EM simulations are.

This modeling approach can be a good start for circuit design. However, considering all of the interconnects and parasitics, even for a transistor, the EM simulation consumes considerable amount of time. The required time for a complete system level design is considerably large considering all different components and inter-stage connections.

As mentioned before, the accuracy of the circuits are strongly related with the accuracy of the device models. To ensure the accuracy of the device models, for mm-wave designers, a manufacturing and measurement cycle has to be done beforehand of the actual design. One of the most appropriate design methodology for mm-wave circuits and systems is called "tile-based" design [7, 9, 12, 25]. In this design methodology, every device are customized for direct connection to transmission lines. Transmission lines are the back-bone for this methodology because for such high frequencies transmission line based design is easier and predictable since transmission lines are easily scalable with length as long as its characteristic impedance, propagation constant and loss factor are known. Since every device is designed to connect to transmission line their characterization also involves transmission line, hence every parasitics are included in characterization cycle. All of the basic components can be characterized; e.g. transmission line corners, tee-junctions, transistors, capacitors, metal-insulator-metal transmission lines, probing pads, baluns, differential devices, and so on. However, it is better to note that every device needs a priori understanding and hence their characterization method might change.

2.2 Optimum Carrier Frequency and Moduation

Selection of carrier frequency, bandwidth and modulation determine the overall system considerations. Eq. (2.1) represents the Shannon's channel capacity. It is reasonable to assume as the frequency increases, bandwidth (BW) also increases. Hence, we can assume that the BW is a fraction of center frequency (f_c) as in Eq. (2.2). Moreover, Eq. (2.2) shows that noise (N) is directly proportional with BW.

$$\mathrm{C} = \mathrm{BW}\log_2(1 + \mathrm{S/N}) \tag{2.1}$$

$$\mathrm{BW} = \alpha \mathrm{f_c} \tag{2.2}$$

$$N = kT\mathrm{BW} \tag{2.3}$$

Using the above three equations and assuming a 30% BW with respect to f_c, and

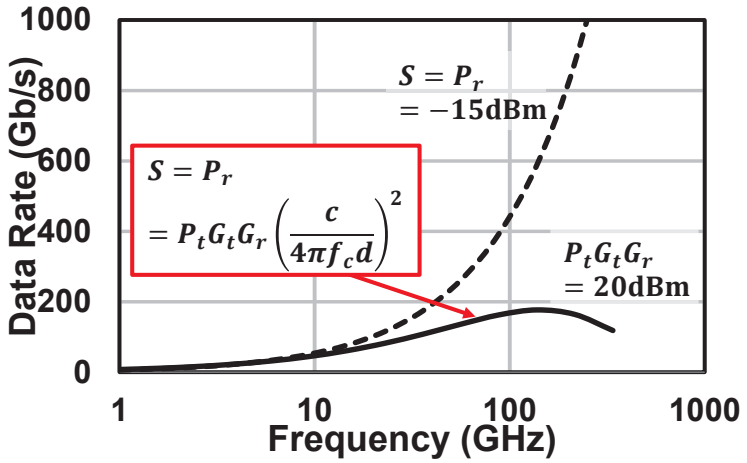


Figure 2.1: Channel capacity vs. f_c when the bandwidth is 30% of f_c, the dashed line represents the data rate when received power is assumed to be constant at -15dBm, and the solid line represents the data rate as the received power is changing as center frequency changes ($S = P_{\text{eff}} = 20\text{dBm}$).

constant received power ($S = P_r$) of -15dBm; the channel capacity (data-rate) vs. f_c can be illustrated as in Fig. 2.1 (the dashed line). It is observed that the data-rate can be increase as f_c increases and after some point, it saturates. Unfortunately, this is not the case from a practical point of view, because as f_c increases the propagation loss increases considerably, and output power from a CMOS device is limited as the operating frequencies lay in mm-wave or sub-terahertz regions. To have a more practical approach, Friis transmission equation should be accounted for the received signal power as shown in the following equation.

$$S = P_r = P_t G_t G_r \left(\frac{c}{4\pi f_c d}\right)^2 \tag{2.4}$$

G_t and G_r represent the TX and RX antenna gain, whereas P_t is the TX output power. In here, these three parameters are mentioned as effective power ($P_{\text{eff}} = P_t G_t G_r$). d is the distance between TX and RX, and c is the speed of light. Assuming and effective power of 20dBm (e.g. $P_t = 20\text{dBm}$, $G_t G_r = 0\text{dBi}$) with a TX to RX distance of 1m, 30% fractional BW, data-rate results as in Fig. 2.1 and Fig. 2.2 (solid black line). The data-rate is not always increasing, there is a peak and it starts to decrease because received signal power (square marked line in Fig. 2.2) is inversely proportional to the square of f_c and always increasing noise power (triangular marked line in Fig. 2.2), even though the BW is proportional to f_c. The channel capacity is drawn up to S/N ratio of 1,

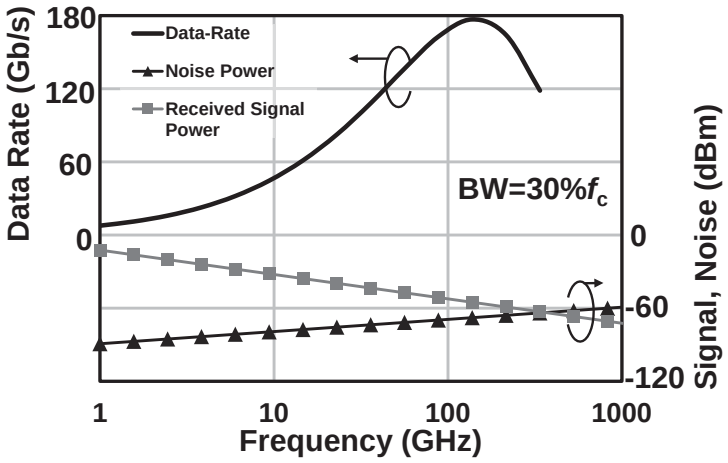


Figure 2.2: Channel capacity vs. f_c (solid black line) when P_{eff} = 20dBm, and d = 1m. Signal power (square marked line) and noise power (triangle marked line) plotted on the secondary vertical axis.

although theoretically continuously decreasing. Nevertheless, the calculation does not include practical modulation schemes. Fig. 2.3 represents the achievable data-rates in consideration with modulation schemes for BW=30%. Theoretical SNR (dB) limits for BER = 10^{-3} are used to calculate the data-rates for modulations of 256QAM (8-bit, 28.5dB), 64QAM (6-bit, 22.5dB), 16QAM (4-bit, 16.5dB), QPSK (2-bit, 9.8dB), and BPSK (1-bit, 6.8dB). Although theoretical calculations achieve around 180Gb/s, it cannot be achieved in considerations with modulation schemes. A 100Gb/s can be achieved with 64QAM modulation at f_c =56GHz (BW=17GHz) which is close to the required SNR limit or with 16QAM modulation at f_c =85GHz (BW=25GHz, 72 to 97GHz) which still has some margin in terms of required SNR. For this reason, while designing the ultra-wideband transceiver, 16QAM modulation is aimed at W-Band.

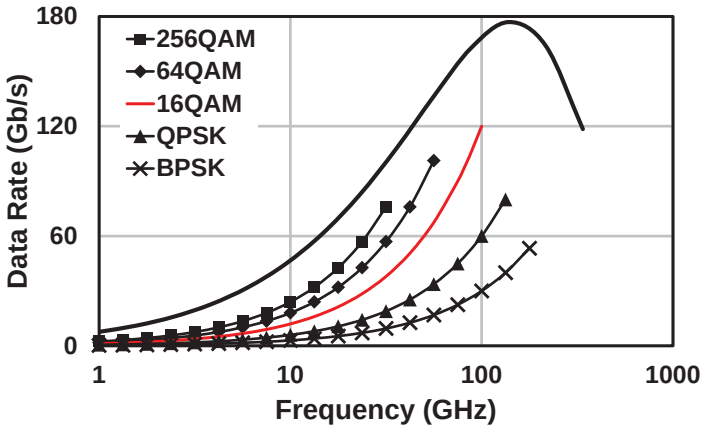


Figure 2.3: Channel capacity vs. f_c for different modulation schemes when $P_{\text{eff}} = 20$dBm, and BW=30%.

2.3 Transistor Gain Definitions

Three gain definitions are revised in this section; starts with the well-known maximum available gain, and then unilateral gain. Finally maximum achievable gain is briefly provided.

2.3.1 Maximum Available Gain

Maximum available gain (MAG) can be achieved when both input and output port of the transistor is matched to components before and after the transistor as illustrated in Fig. 2.4(a). Note that "MC" is used as an abbreviation for matching circuit (or block). A theoretical definition for MAG can be given as;

$$MAG = \left(k - \sqrt{k^2 - 1}\right)\frac{|Y_{21}|}{|Y_{12}|} \tag{2.5}$$

where k is the stability factor of the transistor, which can be calculated as;

$$k = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{21}S_{12}|} \tag{2.6}$$

$$\Delta = S_{11}S_{22} - S_{12}S_{21} \tag{2.7}$$

Several transistors MAG response is given in Fig. 2.5 from the modeled versions using Eqs. (2.5)-(2.7). Transistor modeling is explained in the next chapter. From the figure, only transistor with a width of 36μm (1.5μm × 24) does not trip to maximum available

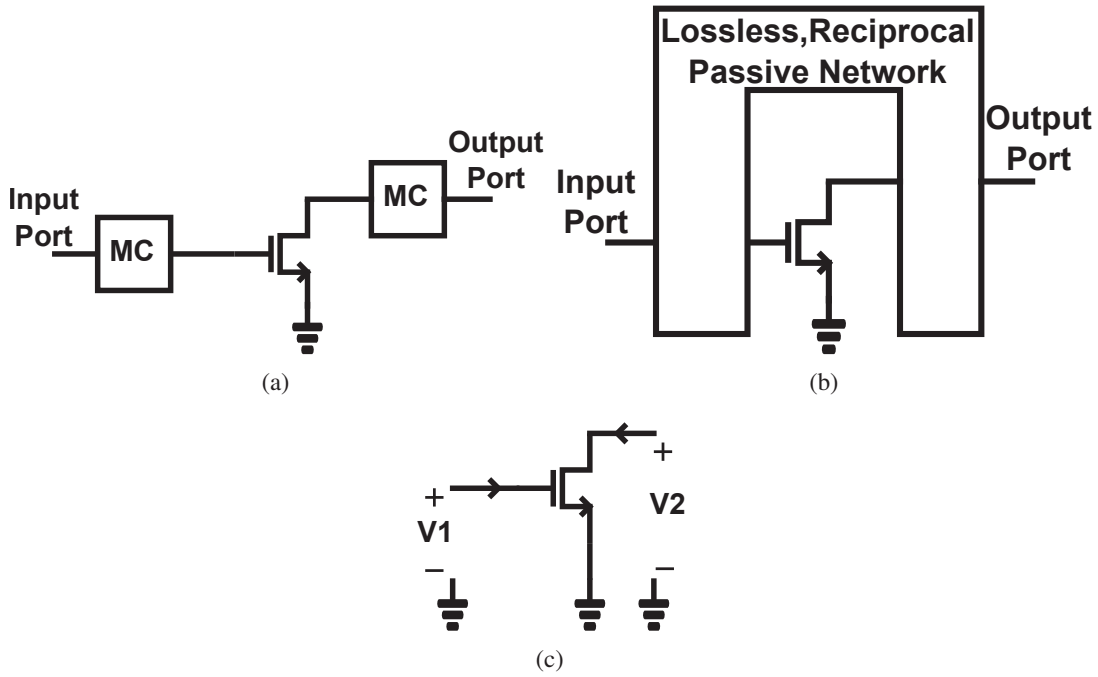


Figure 2.4: Gain definitions (a) maximum available gain, (b) unilateral gain, and (c) additional conditions for maximum achievable gain.

gain region (the corner points on the MSG/MAG responses of other transistors). Before the corner point the stability factor of the transistors are below 1 that is why it is called the maximum stable gain (MSG) region, and after the corner point the stability factor of the transistors are more than 1, that is why it is called the maximum available gain (MAG) region.

2.3.2 Unilateral Gain

In Fig. 2.4(b) a lossless, reciprocal and passive network is embedded between transistor's gate and drain to cancel out transistor's gate-to-drain parasitics which would result in infinite isolation in theory between gate and drain. This is called unilateralization (sometimes neutralization, e.g. in capacitive cross coupling differential amplifiers). That is $|Y_{12}|$ became 0 using this embedded lossless, reciprocal and passive network. Another condition for unilateralization is the same condition with MAG which is input and output ports are simultaneously matched to the networks before and after transistor. Unilateral gain is directly related with transistor's internal parameters. It is not directly dependent on embedded network. The only duty of the embedded network is to cancel out the gate to drain capacitance and resistance. The unilateral gain can be

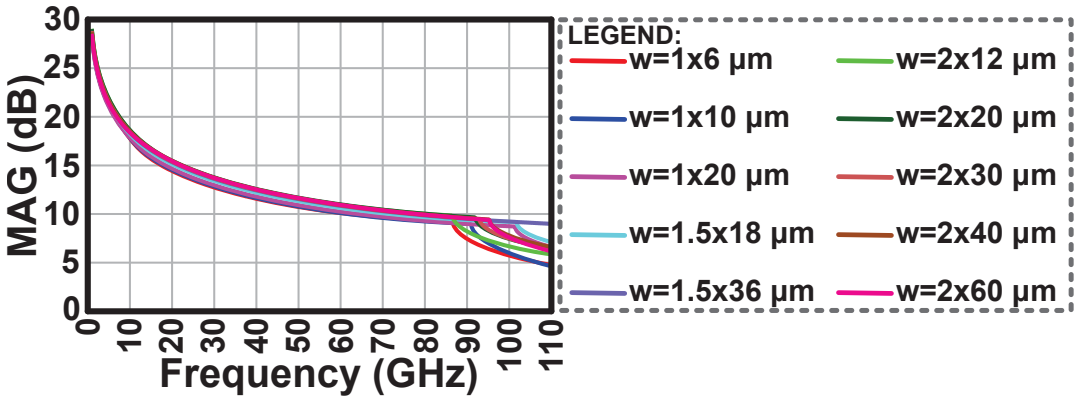


Figure 2.5: Maximum available gain comparisons for different transistor sizes (AxBµm means that A is one finger width, and B is the total width).

calculated as;

$$UG = \frac{|Y_{21}|^2}{4(G_{11}G_{22} - G_{12}G_{21})} \tag{2.8}$$

where UG is the abbreviation for unilateral gain, $|Y_{21}|$ is transistors Y-parameter, G_{ij} is the real part of related Y-parameter. Using this definition unilateral gain of transistors are calculated. Same transistors as in Fig. 2.5 are used. In the following figure unilateral gain comparisons for different size transistors are provided. It can be observed that, again, 36µm (1.5µm×24) have the highest gain considering whole W-band. It is better to remind that the embedding network has no effect on the calculation of unilateral gain, since it is assumed to be lossless, reciprocal and passive. However, in reality it is not the case. Embedding network cannot be lossless in reality. This fact actually affects the available performance of the transistor, and degrades from the theoretical values. Using this kind of embedding network transistor can be forced to have more gain which is called maximum achievable gain. This topic is described in the next sub-section.

2.3.3 Maximum Achiavable Gain

As it is mentioned, transistors can be forced to have more gain than MAG or UG. Similar to UG, transistor again is surrounded by an embedding network (Fig. 2.4(b)). By introducing another condition on unilateral gain maximum achievable gain (MACG) can be obtained based on the definition of unilateral gain as in the following equation;

$$MACG = (2UG - 1) + 2\sqrt{UG(UG - 1)} \tag{2.9}$$

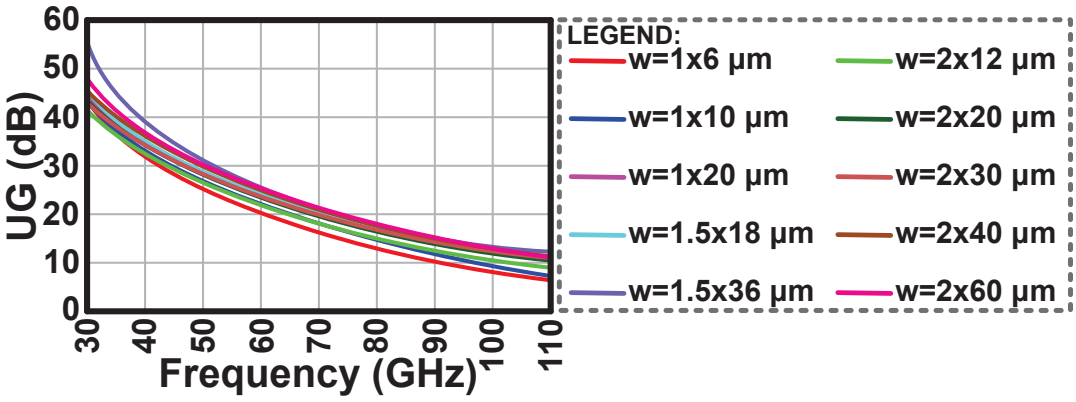


Figure 2.6: Unilateral gain comparisons for different transistor sizes (AxBµm means that A is one finger width, and B is the total width).

Please refer to Fig. 2.6, as the frequency decreases UG value of the transistors increase. For that reason Eq. (2.9) can be approximated when UG value is too high (i.e. frequency is low) as;

$$MACG \approx 4UG \tag{2.10}$$

This means MACG is around 6 dB higher than UG. However, in order to get MACG out of a transistor some additional conditions are required. Fig. 2.4(c) illustrates the voltage and current relations on the gate and drain of a transistor. As it is described in [28], the real output power from this transistor can be given as;

$$P_{\mathrm{R}} = -Re\{V_1^* I_1 + V_2^* I_2\} \tag{2.11}$$

where * is the complex conjugate of the related parameter, and voltage and currents are defined in Fig. 2.4(c). By using the properties of Y-parameters on voltages and currents the above equation can be modified to achieve the following equation;

$$\frac{P_{\mathrm{R}}}{|V_1|^2} = -(G_{11} + A^2 G_{22}) - A|Y_{12} + Y_{21}^*|cos(\angle(Y_{12} + Y_{21}^*) + \phi) \tag{2.12}$$

in which A and ϕ are defined as;

$$A = \frac{|V_2|}{|V_1|} \tag{2.13}$$

$$\phi = \frac{\angle V_2}{\angle V_1} \tag{2.14}$$

Using Eq. (2.12) one can find the point to get maximum power output from transistor

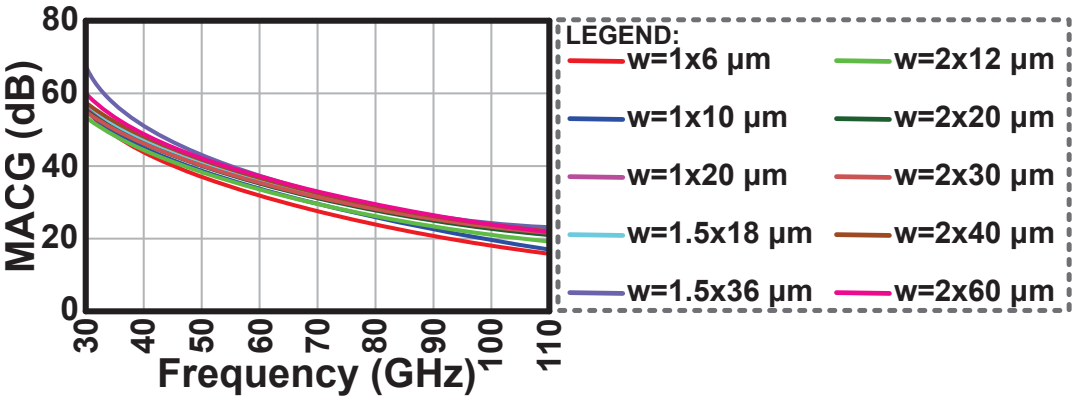


Figure 2.7: Maximum achievable gain comparisons for different transistor sizes (AxBµm means that A is one finger width, and B is the total width).

with the same input voltage (or power) with the following optimum conditions [28] on A and ϕ;

$$A_{\text{opt}} = \frac{|Y_{12} + Y_{21}^*|}{2G_{22}} \tag{2.15}$$

$$\phi_{\text{opt}} = (2k+1)\pi - \angle(Y_{12} + Y_{21}^*) \tag{2.16}$$

In order to provide a quantitative results for MACG, same transistors gain results used in the two previous gain definitions are calculated according to the above equations. Found values are presented in Fig. 2.7. As expected, transistor with a width of 36µm (1.5µm $\times$ 24) have the highest MACG.

Chapter 3

Modeling and Characterization of Devices

3.1 Introduction

This chapter first addresses the already in use, in-house, device models along with the de-embedding and methods to obtain these models in Section 3.2. De-embedding is the first important step for accurate device models and characterization approaches. Conventional de-embedding and transmission line (TL) characterization are introduced in Section 3.2.1. After this, transistor modeling is provided in Section 3.2.2. Furthermore, passive device modeling methods are given in Section 3.2.3 for transmission line corners (bends), tee-junctions, metal-insulator-metal transmission lines (MIM-TLs), DC-cut capacitors and etc. Section 3.2.4 presents design and implementation of a V-Band one-stage common-source amplifier with the current models. In this section, results show well matched agreement between simulation and measured S-parameters. However, when the models are used for a W-Band one-stage common-source amplifier, the simulation and measured S-parameters differ very much and these are presented in Section 3.2.5. For this reason, Section 3.3 introduces improved de-embedding, device modeling and characterization approaches working up to 110GHz.

Section 3.4 introduces differential virtual-thru de-embedding and cross-line characterization based on differential VNA measurements for differential capacitive cross-coupled amplifiers.

Before conclusion, in Section 3.5 multi-port passive device characterization approaches for two-port measurements are presented.

3.2 Conventional Device Models

3.2.1 Pad Parasitic De-Embedding and Transmission Line Models

As mentioned above, de-embedding is the first and most important step for device characterizations. A small error occured in the de-embedding phase would reflect to all of the device characterizations and models, since for every device characterization structures pads and transmission lines are used. Before obtaining device models one has to de-embed pad parasitics and additional transmission lines. In [29], a de-embedding method is introduced based on L-2L method. L-2L method is also referred as virtual-thru de-embedding method, because using two measured transmission line responses with lengths "L" and "2L" one can obtain direct back-to-back connected responses of left and right pads. The method is superior to physical thru de-embedding procedure considering high-frequencies where coupling is a problem. This method is proved to be useful compared to other de-embedding methods; e.g. open-short, open-short-thru, physical thru, while taking into account the transmission line models applied on a 4-stage power amplifier (PA), as provided in [30]. L-2L method is briefly introduced in here for two different 65 nm CMOS processes. Two processes and related de-embedding results are discussed to observe the effects of different processes on the calculation of pad parasitics de-embedding. It is proved that conventional methods for pad parasitic calculation may not work for different processes. De-embedding results regarding to the second process using conventional methods are not very accurate especially after 50 GHz. For this reason a mathematical calculation approach for pad parasitics are introduced in [31] and explained in here. Here, the investigation start from the first process for which de-embedding results are accurate. In the first process, used transmission lines are Coplanar-Waveguide (CPW) based and top metal used for signal line with metal width of 6μm and thickness of 1.2μm.

One can observe illustrations of two different length transmission line structures with lengths "L" in Fig. 3.1(a) and "2L" in Fig. 3.1(b). The two measured results can be converted from S-parameters to transfer parameters (T-parameters) and they can be divided into cascaded sub-networks as [32];

$$[T_{\mathrm{M,L}}] = [T_{\mathrm{lpad}}][T_{\mathrm{L}}][T_{\mathrm{rpad}}] \tag{3.1}$$

$$[T_{\mathrm{M,2L}}] = [T_{\mathrm{lpad}}][T_{\mathrm{2L}}][T_{\mathrm{rpad}}] \tag{3.2}$$

By taking the inverse of Eq. (3.2) and multiplying from both left and right side with Eq. (3.1) virtual-thru response can be obtained in terms of T-parameters as in the follwoing equation. This can also be observed in Fig. 3.2.

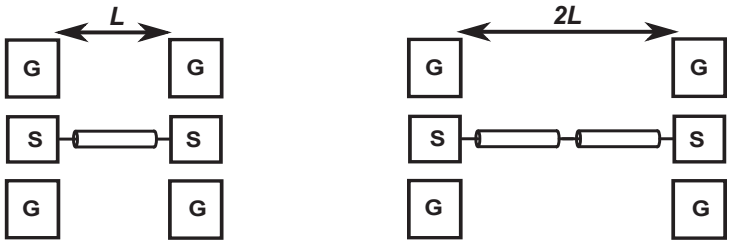


Figure 3.1: Transmission line structures used for de-embedding (a) with length "L", and (b) with length "2L" (Note that two transmission line structures are connected in series for illustration purposes regarding lengths).

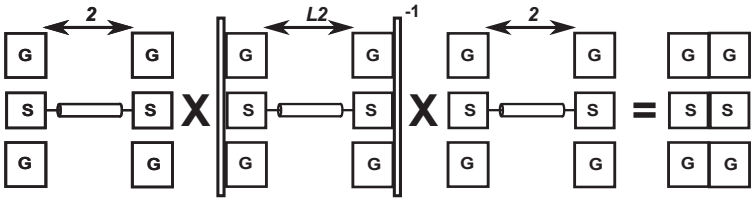


Figure 3.2: Illustration of calculation to obtain virtual-thru response of pads.

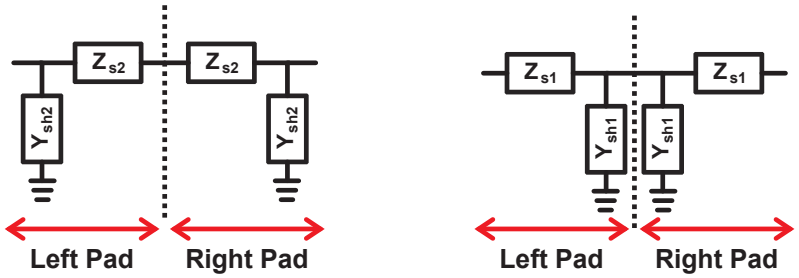
$$[T_{\text{thru}}] = [T_{\text{lpad}}][T_{\text{rpad}}] = [T_{\text{M,L}}][T_{\text{M,2L}}]^{-1}[T_{\text{M,L}}] \tag{3.3}$$

It is better to mention the virtual-thru response calculated in Eq. (3.3) can be solved for two unknowns. Moreover, actual pad parasitics have reciprocal response but not symmetrical. For full representation of pad parasitics three parameters are needed in terms of S-parameters (or three lumped constant parameters however this is also an approximation of the previous state). For this reason, one has to make assumptions for further calculation. In [29], pad parasitics are assumed to have Π-model when left and right pads are connected back-to-back as also illustrated in Fig. 3.3(a). This lumped network can be represented in terms of Y-parameters and two lumped constants (Y_{sh2} and Z_{s2}) can be solved as in the following set of equations;

$$[Y_{\text{thru}}] = ttoy([T_{\text{thru}}]) \tag{3.4}$$

$$[Y_{\text{thru}}] = \begin{bmatrix} Y_{11} & Y_{21} \\ Y_{21} & Y_{11} \end{bmatrix} = \begin{bmatrix} Y_{\text{sh2}} + 1/2Z_{\text{s2}} & -1/2Z_{\text{s2}} \\ -1/2Z_{\text{s2}} & Y_{\text{sh2}} + 1/2Z_{\text{s2}} \end{bmatrix} \tag{3.5}$$

$$Y_{\text{sh2}} = Y_{11} + Y_{21} \tag{3.6}$$



(a) (b)

Figure 3.3: Representation of pad parasitics in terms of lumped models (a) Π-model and (b) T-model when the pads are assumed to be connected back-to-back.

$$Z_{s2} = \frac{-1}{2Y_{21}} \tag{3.7}$$

Note that Y-parameters have symmetrical response as mentioned above. Similarly, T-model parameters (Y_{sh1} and Z_{s1}) (illustrated in Fig. 3.3(b)) of back-to-back connection of left and right pads can be calculated by converting the T-parameters to Z-parameters as in the following set of equations;

$$[Z_{thru}] = ttoz([T_{thru}]) \tag{3.8}$$

$$[Z_{thru}] = \begin{bmatrix} Z_{11} & Z_{21} \\ Z_{21} & Z_{11} \end{bmatrix} = \begin{bmatrix} Z_{s1} + 1/2Y_{sh1} & 1/2Y_{sh1} \\ 1/2Y_{sh1} & Z_{s1} + 1/2Y_{sh1} \end{bmatrix} \tag{3.9}$$

$$Z_{s1} = Z_{11} - Z_{21} \tag{3.10}$$

$$Y_{sh1} = \frac{1}{2Z_{21}} \tag{3.11}$$

In order to calculate the pad parasitics and achieve transmission line characteristics, 200μm and 400μm length transmission lines are measured. After converting the measured S-parameters to T-parameters above mentioned equations are gone through. The parasitics for two different models are calculated and presented in Fig. 3.4. Red lines in these graphs represent the calculated parameters from T-model and blue lines represent the calculated parameters from Π-Model. It can be observed real parts of series and shunt components and imaginary part of series components are very close to each other. On the other hand, imaginary part of shunt components deviate from each other after around 30GHz. Using these two models the pad parasitics are de-embedded from 200μm transmission line structure again using T-parameters [29], and de-embedded

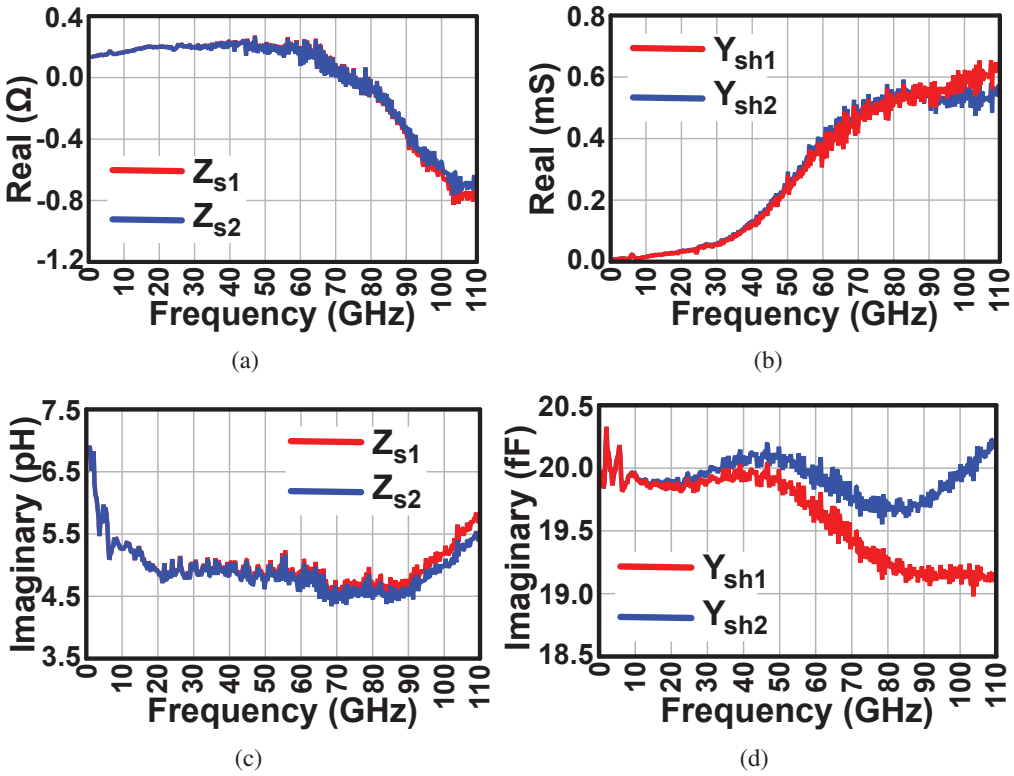


Figure 3.4: Calculated pad parasitic parameters (red lines represent parasitic components calculated from T-Model and blue lines represent parasitic components calculated from Π-Model) for two different calculation method (a) real part of series parasitic components (Ω), (b) real part of shunt components (mS), (c) imaginary part of series components (pH), and (d) imaginary part of shunt components (fF).

T-parameter response converted back to S-parameters (Eq. (3.12)) in order to calculate transmission line characteristics as introduced in [33]. The calculations are also given in here for characteristic impedance, loss term, propagation constant and quality-factor.

$$[T_{\text{de,200µm}}] = [T_{\text{lpad}}]^{-1}[T_{\text{200µm}}][T_{\text{rpad}}]^{-1} \tag{3.12}$$

$$Z_{\text{ch}} = \sqrt{Z_{\text{o}}\frac{(1+S_{11})^2 - S_{21}^2}{(1-S_{11})^2 - S_{21}^2}} \tag{3.13}$$

Note that S_{11} and S_{21} are the de-embedded transmission line S-parameters. Using these as in Eq. (3.13) Z_{ch} can be calculated which is the characteristic impedance of transmission line. Moreover, Z_{o} is the system impedance, in general 50Ω.

$$e^{-\gamma l} = \left(\frac{1 - S_{11}^2 + S_{21}^2}{2S_{21}} \pm K \right)^{-1} \tag{3.14}$$

where γ is the complex propagation constant of transmission line and can be divided as $\alpha + j\beta$. α is the loss term and β is the propagation constant of transmission line, and l is the length of corresponding transmission line. To calculate γ natural logarithm has to be applied on Eq. (3.14). After dividing the result to length of transmission line γ can be divided into real and imaginary parts to obtain α and β, respectively. Moreover, K can be calculated again using S-parameters as in the following equation;

$$K = \left(\frac{(1 + S_{11}^2 - S_{21}^2) - (2S_{11})^2}{(2S_{21})^2} \right)^{0.5} \tag{3.15}$$

Please note that, because of the square-root operation in K calculation sudden changes on the phase has to be observed and corrected ($\pm$ term in Eq. (3.14)). Additional to these equations, one more parameter has to be introduced about the performance of a transmission line which is quality-factor, an important parameter when mm-wave circuits are concerned. Q-factor of transmission line is equal to $\beta/(2\alpha)$. Eq. (3.13)-(3.15) are used to calculate the de-embedded (Eq. (3.12) converted to S-parameters) transmission line characteristics for 200µm, using the mentioned Π-, and T-model for pad parasitics, and found results are presented in Fig. 3.5. Note that α, β, and hence Q-factor for two different pad de-embedding are exactly the same and presented as red lines in these graphs. On the other hand, found characteristic impedance for two-different pad models differ from each other after around 30 GHz. The main reason of this difference is because of pad parasitic capacitance as mentioned above. Another observation is that Π-model has better de-embedding results (black line in Fig. 3.5(a)) compared to T-Model (blue line in Fig. 3.5(a)) considering that characteristic impedance has to be flat (gray dashed line in Fig. 3.5(a)) when frequency increases. This can be proved from the theory while considering *RLCG* (per unit length characteristics of transmission line) representation of characteristic impedance;

$$Z_{\text{ch}} = \sqrt{\frac{(R + j\omega L)}{(G + j\omega C)}} \tag{3.16}$$

As frequency increases $(R + j\omega L) \approxeq j\omega L$, and $(G + j\omega C) \approxeq j\omega C$ so that $Z_{\text{ch}} \approxeq \sqrt{L/C}$ which is constant. For this reason, one can conclude that Π-model for pad is much more reasonable than T-model upto around 70GHz, even so, after 70GHz Π-model, also, deviates from theory.

Another de-embedding approach is the symmetrical pad response [34]. Before going

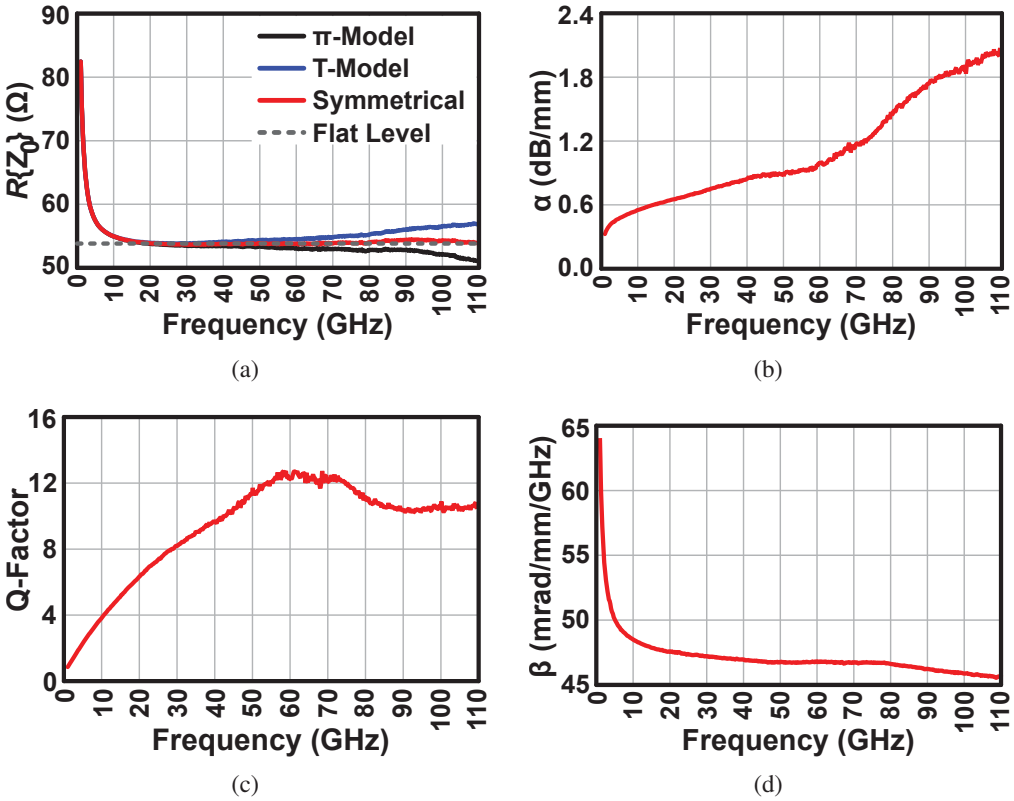


Figure 3.5: Obtained transmission line characteristics using above equations (a) real part of characteristic impedance (Ω)(black line is from Π-model, blue line is from T-model, red line is from symmetry assumption, dashed gray line is for flat leveling), (b) loss term α (dB/mm), (c) quality-factor, and (d) propagation constant β (mrad/mm/GHz).

into this approach, a more general representation of pad parasitics is illustrated in Fig. 3.6. As mentioned above one can only obtain two parameters whether they are S-parameters, Z-parameters or Y-paramaters. Reciprocal pad response of left pad (Eq. (3.17)) and right pad (Eq. (3.18)) responses in terms of S-parameters are given as;

$$[S_{\text{pleft}}] = \begin{bmatrix} S_{\text{p11}} & S_{\text{p21}} \\ S_{\text{p21}} & S_{\text{p22}} \end{bmatrix} \tag{3.17}$$

$$[S_{\text{pright}}] = \begin{bmatrix} S_{\text{p22}} & S_{\text{p21}} \\ S_{\text{p21}} & S_{\text{p11}} \end{bmatrix} \tag{3.18}$$

Since one cannot solve for these three parameters an assumption must be done. Let us assume that Z_{s1} is equal to Z_{s2}, two series parasitics in Fig. 3.6. By assuming such pad S-parameters are assumed to be reciprocal and symmetrical as;

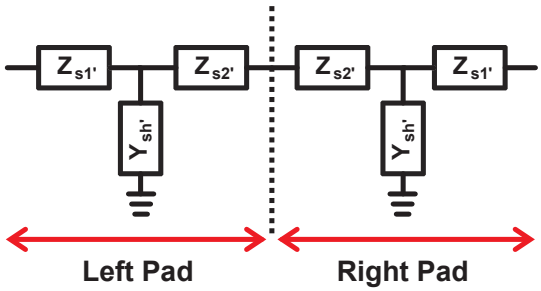


Figure 3.6: Illustration of a more general pad model (Double-T type).

$$[S_{\text{pleft}}] = [S_{\text{pright}}] = \begin{bmatrix} S_{\text{p11}} & S_{\text{p21}} \\ S_{\text{p21}} & S_{\text{p11}} \end{bmatrix} \tag{3.19}$$

When left and right pads are connected back-to-back using Eq. (3.19), virtual-thru response can be represented as;

$$[S_{\text{thru}}] = \begin{bmatrix} S_{\text{p11}}(1 + S_{\text{thru,21}}) & S_{\text{thru,21}} \\ S_{\text{thru,21}} & S_{\text{p11}}(1 + S_{\text{thru,21}}) \end{bmatrix} \tag{3.20}$$

$$S_{\text{thru,21}} = S_{\text{p21}}^2/(1 - S_{\text{p11}}^2) \tag{3.21}$$

From the above two equations and virtual-thru results, S_{p11} and S_{p21} can be calculated easily. After calculating pad S-parameters and de-embedding from 200µm transmission line structure, transmission line characteristics are calculated as presented above. α and β, and hence Q-factor of transmission line are obtained exactly same with Π-, and T-model of pad parasitics de-embedding as in Fig. 3.5. However, characteristic impedance is again different than previous two models and presented in Fig. 3.5(a). This assumption lead a much more accurate characteristic impedance as compared with the other models and theory. So for this specific 65nm process, de-embedding using symmetrical pad approach can be used safely together with transmission line characteristics.

As mentioned in the beginning of this section, de-embedding regarding two processes are investigated. From here on, the second process, also 65nm standart CMOS, is investigated. This process is used in the rest of the structures in this work. Transmission line width for this process is 2.5µm and the signal metal thickness is 3.4µm. De-embedding is done using again 200µm and 400µm length transmission lines. The above mentioned three methods (Π-model, T-model, and symmetrical pad response) are followed. In Fig. 3.7, pad parasitic components in terms of real and imaginary parts are illustrated. One can compare with the previous process that, only the parasitic

resistance is similar. On the other hand, in the second process parasitic component values have increased. After using three de-embedding calculation methods, tranmission line characteristics for 200μm length have been calculated and presented in Fig. 3.8. Again independent of de-embedding calculation α, β, and hence Q-factor are same. As comparing with the previous process one can conclude that tranmission line in this process have less loss, higher Q-factor, but slower waves. Fig. 3.8(a) presents the calculated characteristic impedance after de-embedding. It can be observed that none of the three has a good response as compared with the theory of flat characteristic impedance at higher frequencies. Copmparing with the previous process, it can be concluded that T-model has better accuracy than Π-model for this process. In fact, T-model is better than other two pad models. However, in order to accurately determine the pad parasitics and transmission line characteristics. Current de-embedding results have to be improved. For this reason, a numerical pad-parasitic calculation method is introduced [31], and presented here.

As it can be observed from Fig. 3.8(a) theoretical characteristic impedance (flat line) lies between T-model and symmetrical pad response model. Moreover, T-model has better accuracy than other two. For the new pad parasitic calculation method, the general double-T-type (Fig. 3.6) is assumed. It is already pointed out above that using virtual-thru results only two parameters can be calculated. By adding another degree of freedom outside of the system (i.e. externally controllable optimization parameter k) three components can be solved using the results of T-model, since it is more accurate. The first assumption is to relate $Z_{s2'}$ with $Z_{s1'}$ as in the following equation;

$$Z_{s2'} = kZ_{s1'} \tag{3.22}$$

Note that k is between 0 and 1. Using Eq. (3.22) and some mathematical manipulations other two pad parasitics can be solved using T-model parameters Z_{s1} and Y_{sh1} as;

$$Z_{s1'} = Z_{s1} + k/Y_{sh1} - (Z_{s1} + 1/Y_{sh1})\left(\frac{k - 1 + \sqrt{k^2 + 2k + 1 + 4kZ_{s1}Y_{sh1}}}{2(1 + Z_{s1}Y_{sh1})}\right) \tag{3.23}$$

$$Y_{sh'} = \frac{\left(k - 1 + \sqrt{k^2 + 2k + 1 + 4kZ_{s1}Y_{sh1}}\right)Y_{sh1}}{2k(1 + Z_{s1}Y_{sh1})} \tag{3.24}$$

Note that when $k = 0$, $Z_{s2'} = 0$ which means the three element model degraded to two element T-model. Moreover, when $k = 1$, $Z_{s2'} = Z_{s1'}$ which is the symmetrical pad response. It should be like this since flat characteristic impedance level is between

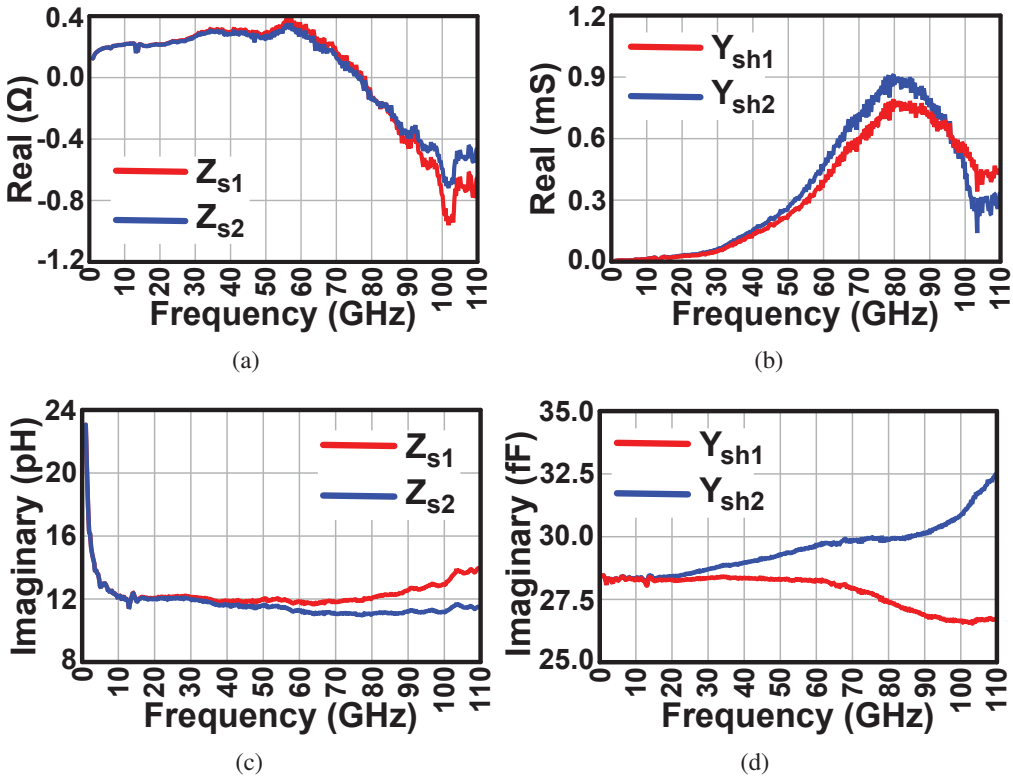


Figure 3.7: Calculated pad parasitic parameters for the second process (red lines represent parasitic components calculated from T-Model and blue lines represent parasitic components calculated from Π-Model) for two different calculation method (a) real part of series parasitic components (Ω), (b) real part of shunt components (mS), (c) imaginary part of series components (pH), and (d) imaginary part of shunt components (fF).

T-model response and symmetrical pad response. After that k is adjusted to obtain flat characteristic impedance. Note that k value cannot be assigned to 0, 0.5, and 1 because the numerical calculations crush at these points. In order to find accurate de-embedding results the k value assigned to 0.2, 0.25, 0.3 and 0.4. Related pad parasitic values in terms of imaginary parts are given in Fig. 3.9(a) for series parasitic components, and in Fig. 3.9(b) for shunt parasitic component. Note that for the sake of simplicity real parts are not shown. They follow similar behavior; however, the variations are small since the values are very close to each other.

Using the found parasitic values for different k, de-embedding processes have done on 200μm tranmission line as used above for Π-, T-model, and symmetrical pad response approaches. Since the de-embedding calculation based on same virtual-thru response does not change complex propagation constant the values are not given in here. However, as mentioned, found characteristic impedance change for different

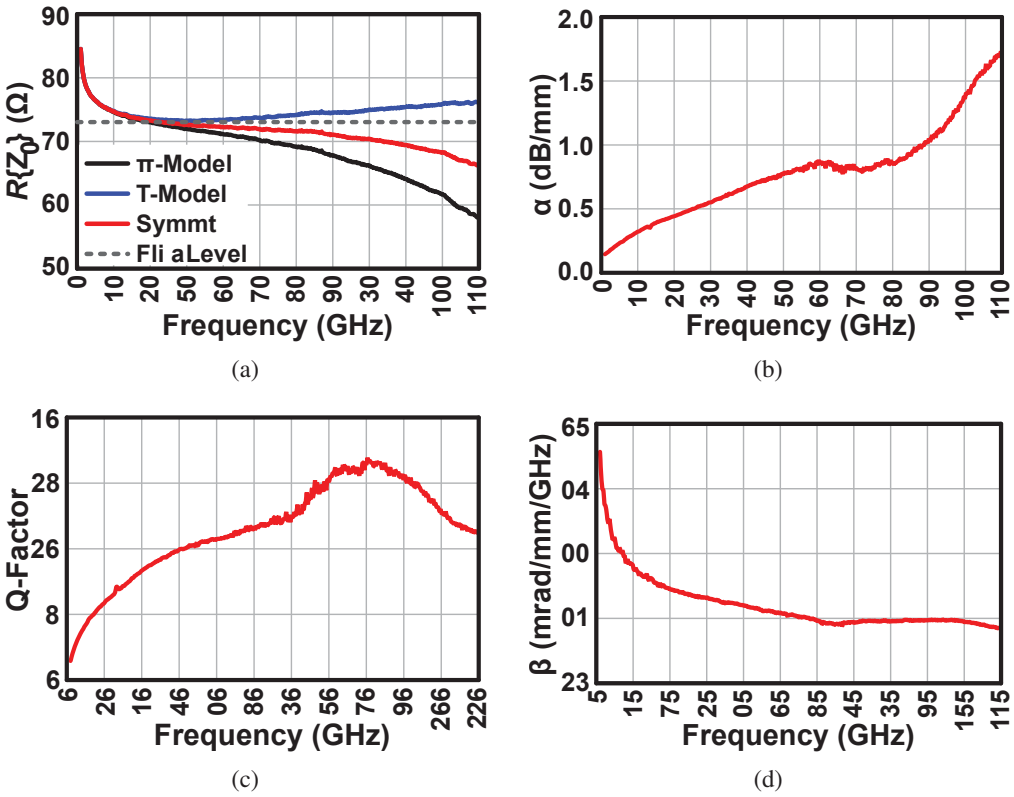


Figure 3.8: Obtained transmission line characteristics for the second process (a) real part of characteristic impedance (Ω)(black line is from Π-model, blue line is from T-model, red line is from symmetry assumption, dashed gray line is for flat leveling), (b) loss term α (dB/mm), (c) quality-factor, and (d) propagation constant β (mrad/mm/GHz).

de-embedding calculations. Characteristic impedance variations in terms of k variations in comparison with T-model results are illustrated in Fig. 3.9(c). One can observe that best flat response can be achieved with $k = 0.25$. Hence, this de-embedding and pad parasitic response can be used in other device characterizations.

De-embedding results might change from process to process, device to device. In our calculation method, we have used the T-model results, because the flat characteristic impedance line falls in between the symmetrical and T-model results. For some other process, the case might be in between Π-model and symmetrical response, or in the first process case it might be exactly the symmetrical response case. In order to provide a general approach for virtual-thru de-embedding method, an algorithm is noted here.

1. Apply L-2L method on the measured transmission lines to obtain virtual-thru response of the pads.

2. Calculate pad parasitics from Π-model, T-model, and symmetrical response

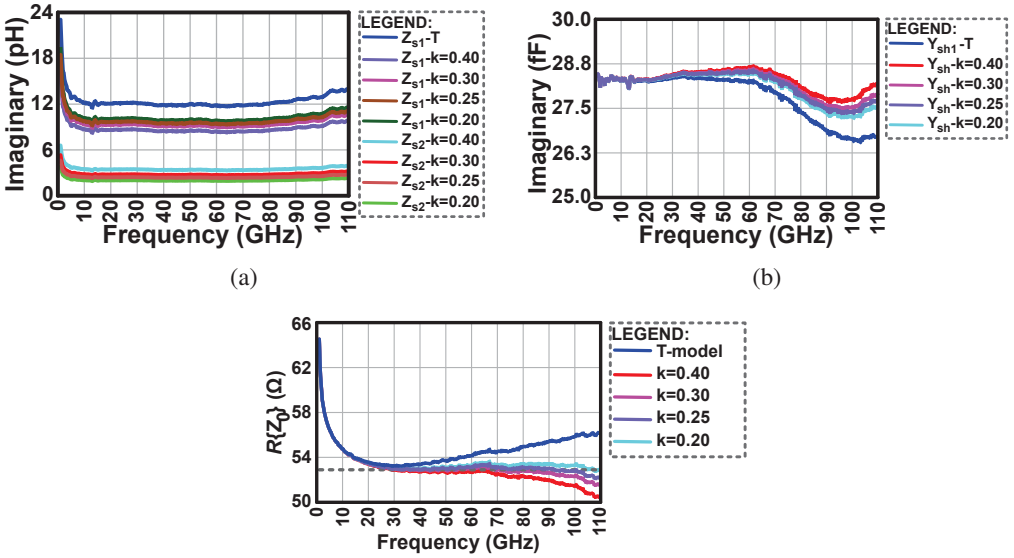


Figure 3.9: Pad parasitics variation and related de-embedding results (a) imaginary part of series components variations in terms of k compared with T-model series parasitic (b) imaginary part of shunt component variations in terms of k compared with T-model shunt parasitic, and (c) related transmission line characteristic response after de-embedding for different k values.

approach.

3. De-embed these three methods separately and compare with each other in terms of transmission line characteristic impedance. If one of these response is accurate at high frequencies, one can use that pad parasitics and concluded transmission line characteristics for further.

4. If the characteristic impedance is not accurate enough for specific applications, Observe the flat characteristic impedance line.

   (a) If the line falls in between Π-model and symmetrical response modify Eqs. (3.22)-(3.24) for Double-Π type from calculated Π-model parasitic parameters, and obtain a reasonable and accurate response by adjusting value k, which is from 0 to 1, Π-model parameters to symmetrical pad response, respectively.

   (b) If the line falls in between T-model and symmetrical response, use Eqs. (3.22)-(3.24) for Double-T type from calculated T-model parasitic parameters, and obtain a reasonable and accurate response by adjusting value k, which is from 0 to 1, T-model parameters to symmetrical pad response, respectively.

Since an accurate de-embedding results are obtained, other devices can be modeled. In the next section, transistor modeling approach is introduced briefly.

3.2.2 Transistor Model

As mentioned above de-embedding method is the first and most important phase for device characterization. For this reason, many researchers pay attention to de-embedding in transistor measurements [35, 36]. In these kind of approaches every device characterization phase needs its own de-embedding method, which consumes area, and time. It is noted in this work that tile-based design is used and hence transistors can also be characterized with obtained transmission line models and pad parameters as provided in [37]. In our work, transistors are adjusted as common-source so that they can be measured as two-port devices up to 110 GHz. A simple characterization structure is provided in Fig. 3.10. Note that gate bias is provided from the port connected to gate and DC feed is provided from the port connected to drain of transistor. DC feed voltage is set to 1 V, and gate bias is swept from 0 to 1 V with 0.05 V steps. Upon characterization of transistors for different gate biases, one has to de-embedded the additional apparatus connected to transistors, i.e. transmission lines with 50 μm length and pad parasitics from both sides. After that the remaining work is to model the transistors with different gate biases. One common approach is to model the transistor parasitics using the core transistor from PDK as given in Fig. 3.11(a). This model is simple, however, it cannot be very accurate for high frequencies since lumped constant components are used. Even if the lumped conponents have frequency dependence, it still cannot model accurately in the whole frequency band and for different gate bias voltages, because in a CMOS based transistors the parasitics related with substrate are very unpredictable. In [38], a so called “Y-Wrapper" model is used. This model is obtained by subtracting PDK transistor response in terms of Y-parameters from measurement results. It is then numerically modeled for different gate biases and frequency dependency. It is illustrated in Fig. 3.11(b). This model is much more accurate up to 110 GHz and for different gate biases, because it is obtained from measurement results in which the unpredictable substrate effects are included. The main drawback of this model is that only admittance parapmeters for a transistor are considered, hence, linearity and noise contribution cannot be accurately taken into account caused by gate parasitics in the simulations. Addressing this issues, in [39], transistor parasitics are calculated for gate-source admittance, gate-drain admittance, drain-bulk admittance and gate parasitic impedance. One can calculated for four parameters, because from the measurements of two-port transistors one can only get four results owing to transistors characteristics which are

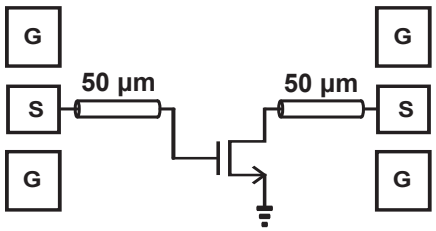


Figure 3.10: Simple transistor characerization structure. Gate bias is provided from the port connected to gate of transistor and DC feed is provided from the port connected to drain of transistor.

nonreciprocal and unsymmetrical devices (S_{11}, S_{12}, S_{21}, S_{22}). Using some matrix manipulations and calculations the mentioned four parasitics can be calculated. Note that the details are not given in here, and for more details one can refer to [39]. The parasitics obtained for different gate bias conditions up to 110 GHz can be numerically modeled based on frequency and gate bias dependency. This method is helpful during design phase because this model can give accurate parasitics values depending on different simulation conditions. The modeling of transistor is briefly mentioned in this section. The next section addresses the modeling approaches for passive devices other than transmission lines.

3.2.3 Passive Device Model

As already discussed in the introduction part of this work, every device model accuracy is important to achieve a predictable and working systems. For this reason both active and passive device modeling are necessary. Transistors, active devices, modeling approach has already been introduced in the previous section. In this section, passive device modeling approaches are introduced. These devices are transmision line based corners, tee-junctions, metal-insulator-metal (MIM) transmision lines, DC cut capacitors, bias resistor connected transmission lines and etc. Moreover, every device characterization modeling phase has to be carefully thought starting from characterization structure, seperately.

Transmission Line Corner Model

Transmission line based corners are used mainly for signal routing. The input and output trasnmission line width is 2.5 µm, same as the normal transmission line width used in this process. Their response is basically different than normal transmission lines because of the additional parasitics seen at bending places. In order to model corners,

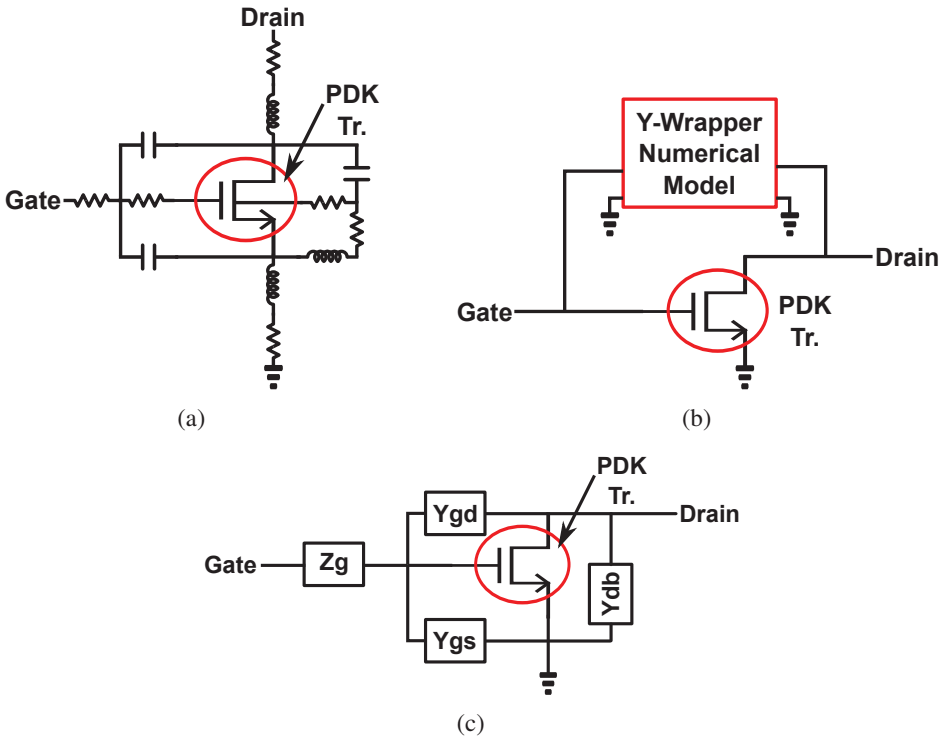
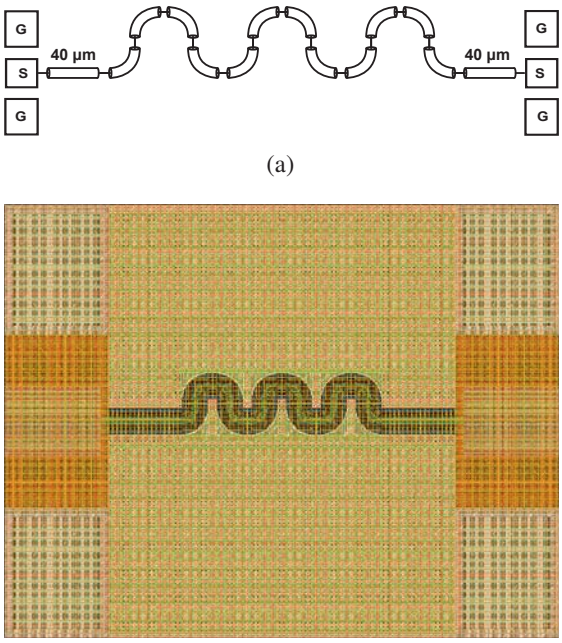


Figure 3.11: Transistor models (a) lumped model, (b) “Y-wrapper" Model, and (c) parasitics model including gate impedance.

a test element group (TEG) is constructed. The illustration of this TEG can be seen in Fig. 3.12 in terms of schematic and layout illustrations. As it can be observed from this figure that there are 12 corner structures are connected with each other back-to-back. This kind of connection can be safely done because in theory corner response is symmetrical and reciprocal. The number of corner structures connected in series is decided by the minimum distance between pad to pad which is around 200 µm in order to avoid coupling between the measurement probes. The width of one corner is around 20 µm and on the same line 6 corners are present which result in 120 µm distance. In order to achieve, 200 µm total width between the pads 40 µm length transmission lines are added on both left and right sides. One may ask, instead of 12 corners why not connect 16 or 20 corners together to achieve the desired pad to pad distance. As close as the structures to probing pads, as possible as the undesired coupling from probes to structures inside the measured TEG. In order to avoid again undesired coupling, this time from pad to corner, this TEG structure is chosen.

This structure is manufactured using 65 nm process (as mentioned in the de-embedding section of this chapter with the second process) and measured from 1 to 110 GHz. Fig. 3.13 presents a simple corner model based on transmission line sections.



(a)

(b)

Figure 3.12: Illustration of corner characterization TEG (a) schematic, and (b) layout.

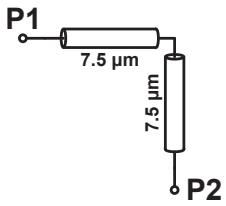


Figure 3.13: Simple corner model based on transmission line sections.

To obtain the corner model first of all the pads and additional transmission lines (40 µm) from left and right sides of the measurement results are de-embedded. The remaining response from measurement results are optimized with transmission line models and corner response is obtain by two transmission line sections having 7.5 µm each. To give a comparison between models and measurement results, the TEG structure is reconstructed using models from pad parasitics, transmission lines and corner models. This model results and measurement results are compared with each other in Fig. 3.14. Both return loss results show that model and measurement results well match with each other. However, return loss results have disagreement between 90 to 110 GHz. Moreover, insertion loss comparisons show that there is a disaggrement starts from 70 GHz. In the remaining part of frequency band the model and measurement results

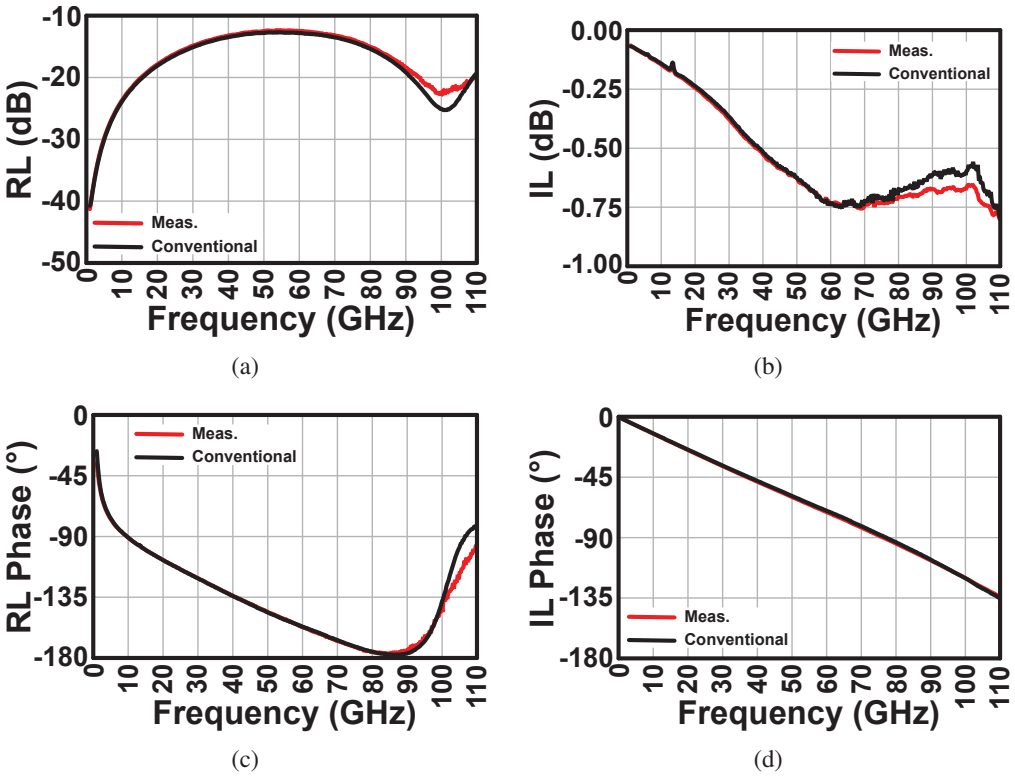


Figure 3.14: Corner Characterization TEG measurement results in comparison with device models (red lines present measurement results and black lines present model results) (a) magnitude of return loss comparisons, (b) magnitude of insertion loss comparisons, (c) phase of return loss comparisons, and (d) phase of insertion loss comparisons.

well-match with each other.

Transmission Line Tee-Junction Model

Transmission line tee-junction is used for several reasons in millimeter-wave circuits. One of the most common use is to implement a short circuited or open circuited shunt transmission lines for the purpose of matching between stages or within stages. For this reason accuracy of tee-junction model is very effective on the overall circuit performances. Fig. 3.15 illustrates the geometry of used tee-junction. Note that width of the signal lines in all three ports are adjusted to be 2.5 μm, same as the transmission line width. Gray areas in this figure represents grounds. Metal layer 1 and 2 are also common ground for all structures.

As it can be observed from Fig. 3.15, this device is a three-port device. The modeling of this device made from the measurements using two-port vector network

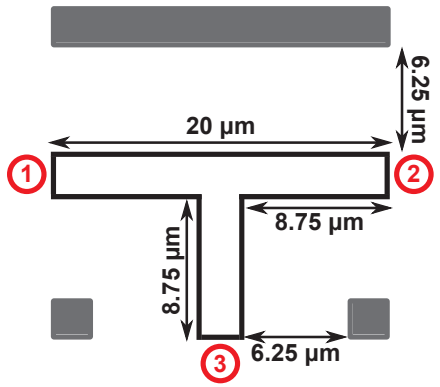


Figure 3.15: Illustration of used tee-junction geometry.

analyzer (VNA) to characterize the device up to 110 GHz. Although four-port VNAs working till 110 GHz are commercially available, it still is not very common both in academia and industry. Even if the measurements are conducted with a four-port VNA the accuracy of the measurements would be questionable because of the decreased system dynamic range for VNA for four-port, and calibration accounting 90° orthogonally placed probes would degrade the accuracy in terms of broadband measurement results. Hence, two TEGs are constructed for modeling purpose of tee-junction, which are provided in Fig. 3.16. Note that in these structures devices other than tee-junction are transmission lines and pads, which are characterized accurately. No other devices are used in these structures to decrease the source of error.

Chip micrographs for these two structures are provided in Fig. 3.16(c), and Fig. 3.16(d) for structures illustrated in Fig. 3.16(a) and Fig. 3.16(b), respectively. Using the two structures in Fig. 3.16, simple model presented in Fig. 3.17, transmission line models and pad models, transmission line lengths in tee-junction are adjusted to give optimum matching between measured and model S-parameters for both structures. The optimum line lengths are also given in Fig. 3.17. Note that physical transmission line lengths and model line lengths are different which is expected. Obtained results are compared with measurements results and given in Fig. 3.18.

From Fig. 3.18, it can be concluded that model results and measurement results well match with each other up to 70 GHz for both structures. On the other hand, comparisons show that model is not very accurate after 70 GHz. Another device to be characterized is metal-insulator-metal (MIM) transmission line which is used for DC and RF decoupling, and the conventional modeling approach for this device is presented in the next section.

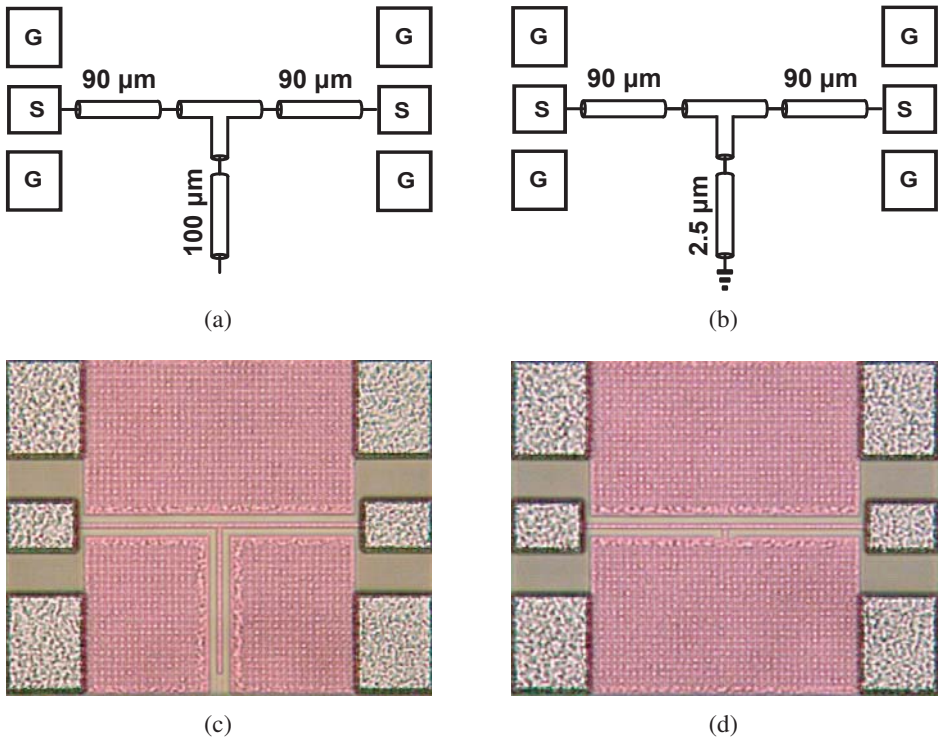


Figure 3.16: Tee-junction modeling TEGs (a) port 3 is terminated with open circuited 100 µm transmission line (b) port 3 is terminated with short circuited 2.5 µm transmission line, (c) chip micrographs of (a), and (d) chip micrograph of (b).

Metal-Insulator-Metal Transmission Line Model

Most common ways to decouple DC and RF in amplifiers or any other circuits are to use decoupling capacitors or RF-choke inductors. Eventhough these devices are properly modeled for mm-wave frequency range, still the surrounding parasitics and connected line parasitics strongly affect these devices performances in terms of resonance frequencies, isolation, loss, noise transmission and etc. Moreover, again due to the parasitics these devices might not be considered as lumped after characterization phase. Simulation accuracy can also decrease considerably because of undesired parasitics in the layout. In [40], a high attenuation power line is introduced. This transmission line like structure can realize a very low characteristic impedance for power line, hence the isolation (decoupling) between DC and RF can be achieved in a wide-band fashion without resonances in the band of interest. It can also ground the end of RF port owing to again low characteristic impedance feature. Thus, the performances of mm-wave circuits can be elevated. Moreover, this low impedance decoupling line is applied successfully on a differential low-noise amplifier [41]. This high-attenuation power line

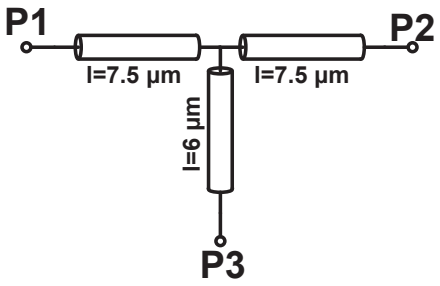


Figure 3.17: Simple tee-junction model based on transmission lines.

uses finger capacitors, and MOS capacitors to increase the per-unit-length capacitance of transmission line and hence decrease the characteristic impedance. Also the parasitic resistance on these finger capacitors increase the attenuation constant of this transmission line which is an essential feature of DC power supply networks to isolate more DC and RF signals from eash other. In our applications, a similar structure is used. Same with the previous case the signal (the line connected for both DC and RF) line is wider (12 µm) than normal transmission line (2.5µm) to decrease the inductive component and characteristic impedance of DC feed transmission line. Moreover, similarly, finger capacitors are used within the device to increase capacitance and parasitic resistance components of the line, for the purposes of decreasing characteristic impedance and increasing the attenuation constant of the line. A geometrical representation can be seen in Fig. 3.19. In this illustration, the top metal layer is shown white area, and gray lines represent lower metal layers. Finger capacitors are shown within the red circle. Other than the structure introduced [40], in this structure MOS capacitors are not used. Instead metal-insulator-metal (MIM) capacitors are used for more stable capacitance values. That is because MOS and finger capacitance variations according to the process is much more than MIM capacitance variations. This MIM capacitance layer can be observed in Fig 3.19 in blue areas. Since MIM capacitors are used in this structure and the structure itself is very similar to a normal transmission line, the device is named as MIM transmission line. A general use for MIM transmission line is provided in a general common-source amplifier stage in Fig. 3.20. MIM transmission line is represented as a dashed transmission line in this figure.

As mentioned before, one of the essential feature of this device is its low characteristic impedance which is around 1 to 3 Ω. Because of this low impedance, accuracy of direct two port measurements are questionable. In fact, they are not accurate. In order to prove this fact, two TEGs are constructed. In one TEG a 10 µm MIM TL and in the other 40

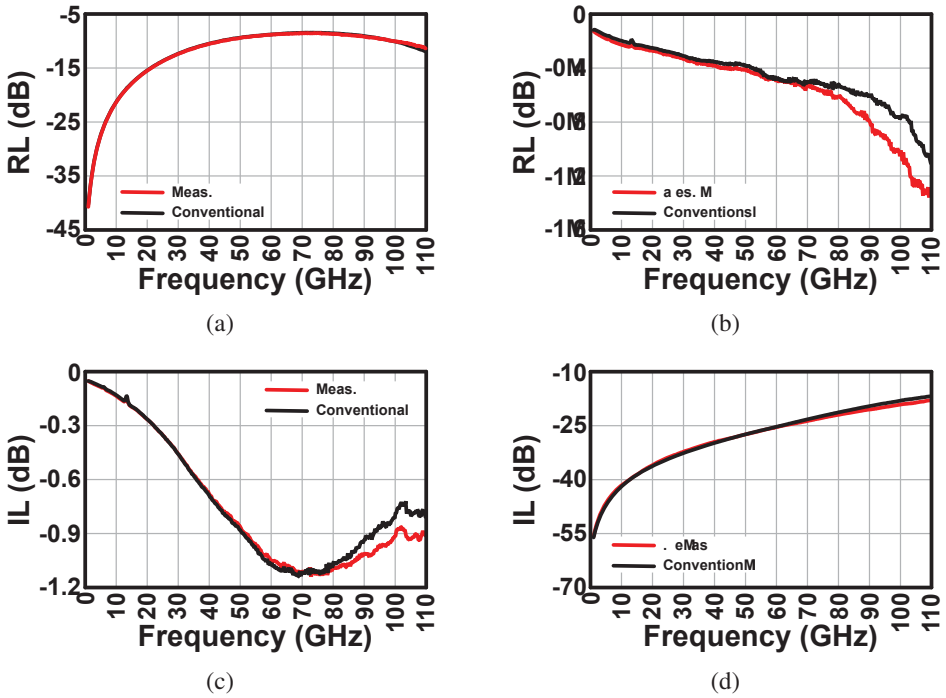


Figure 3.18: Tee-junction characterization TEG measurement results in comparison with device models (red lines present measurement results and black lines present model results) (a) magnitude of return loss comparisons for tee-junction terminated with open circuited transmission line, (b) magnitude of return loss comparisons for tee-junction terminated with short circuited transmission line, (c) magnitude of insertion loss comparisons for tee-junction terminated with open circuited transmission line, and (d) magnitude of insertion loss comparisons for tee-junction terminated with short circuited transmission line.

μm MIM TL are connected between two 45 μm tranmission lines and pads from both sides as shown in Fig. 3.21. The additional 45 μm TL and pads from both TEGs are de-embedded. Obtained 10 μm MIM TL response is cascaded four times and compared with directly obtained 40 μm MIM TL response in Fig. 3.22. Theoretically cascaded four 10μm and 40μm MIM TLs should provide the same response. However, as it can be observed from the figure, because of the inaccuracy of the measurements, they do not provide the same response. Especially after around 30 GHz, since as the frequency increases system dynamic range of the VNAs decreases. In order to accurately determine the characteristics of MIM TL, two different TEGs are constructed as in Fig. 3.23. Chip photo of related TEGs are also provided in the same figure. In order to model MIM TL, a lumped-constant based model is assumed as in Fig. 3.24.

Note that L_s and R_s present the series components, and L_p, R_p, and C_p are the shunt

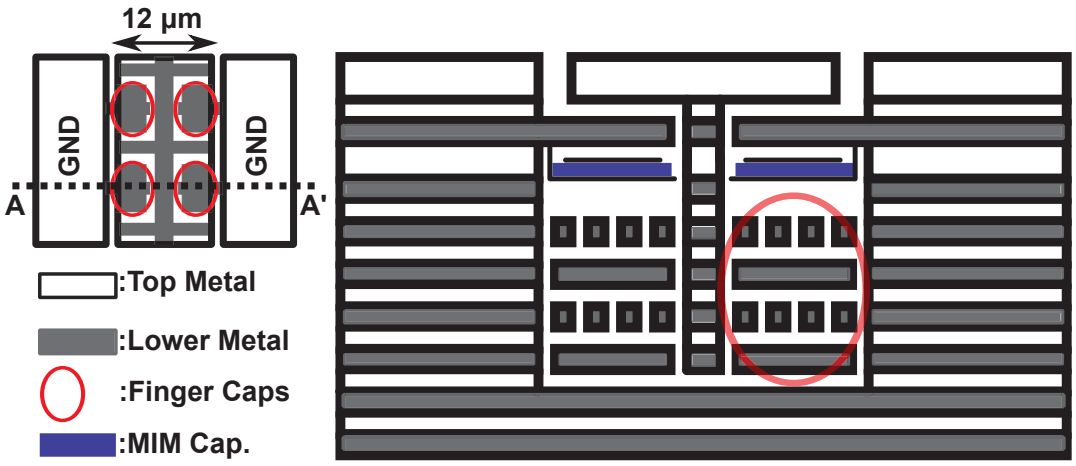


Figure 3.19: Illustration of metal layers and MIM capacitor layers for MIM transmission line.

components of MIM TL model. Together with transmission line, tee-junction, and pad models, S-parameter response of MIM TL model components are optimized to their best to achieve similar results with measurements. The optimized lumped values are as follows; L_s = 0.08pH, R_s = 10 Ω, L_p = 16pH, R_p = 10 Ω, and C_p = 15fF.

Comparisons between model based and measurement S-parameters can be found in Fig. 3.25. It can be observed that model and measurement results match well, except resonance frequencies and high frequencies.Difference for two 40 μm MIM TL connected TEG between model and measurements are larger than other TEG results. The difference between model and measurement results getting larger especially after 70 GHz, and mostly observed in insertion loss case. Even so, for a device with low impedance values this method can be used [42], and it is more accurate than direct two-port measurements.

Almost all of the essential devices for a mm-wave amplifier are introduced and their models are extracted. The methods for model extraction for different devices need different approaches. In a mm-wave amplifier, there are other devices like capacitors and bias resistors. In here their models and characterizations are not introduced. Briefly, capacitors are modeled using direct two-port measurements within certain length of transmission lines and pads. After de-embedding of additional components a capacitor can be easily modeled using lumped components. Bias resistor connected transmission lines, which are used for gate bias connections before transistors, are physically cascaded and their responses are achieved from measurements easily.

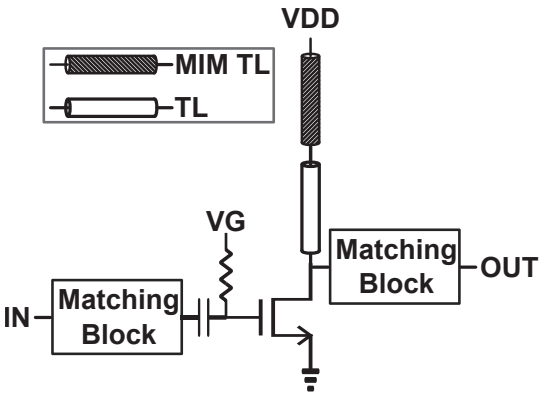


Figure 3.20: Representation of a simple and general common-source amplifier stage with matching blocks and other components. MIM TL is used for DC to RF decoupling.

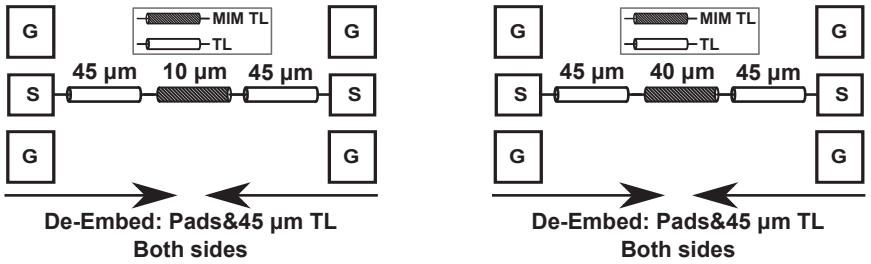


Figure 3.21: Direct two-port characterization TEGs for MIM TL (a) 10µm MIM TL is placed, and (b) 40µm MIM TL is placed.

3.2.4 Application of Conventional Device Models on a V-Band Amplifier

A V-Band amplifier is designed with the developed models. The schematic of the amplifier is presented in Fig. 3.26. The chip is manufactured in 65nm standard bulk CMOS and the chip photo is presented in Fig. 3.27. The amplifier is measured with VNA up to 110GHz.

Measurement results are compared with the modeled results in Fig. 3.28. It can be observed from Fig. 3.28(a) that the input reflection S-paraemeters are well matched up to 110GHz. The results of gain are presented in Fig. 3.28(c) and Fig. 3.28(d). The results for model and measurements are well-matched. On the other hand, the comparison of output reflection S-parameters of model and measurement results show that there is difference after around 70GHz, and they are illustrated in Fig. 3.28(b).

It can be concluded that the models are working very accurately for V-band

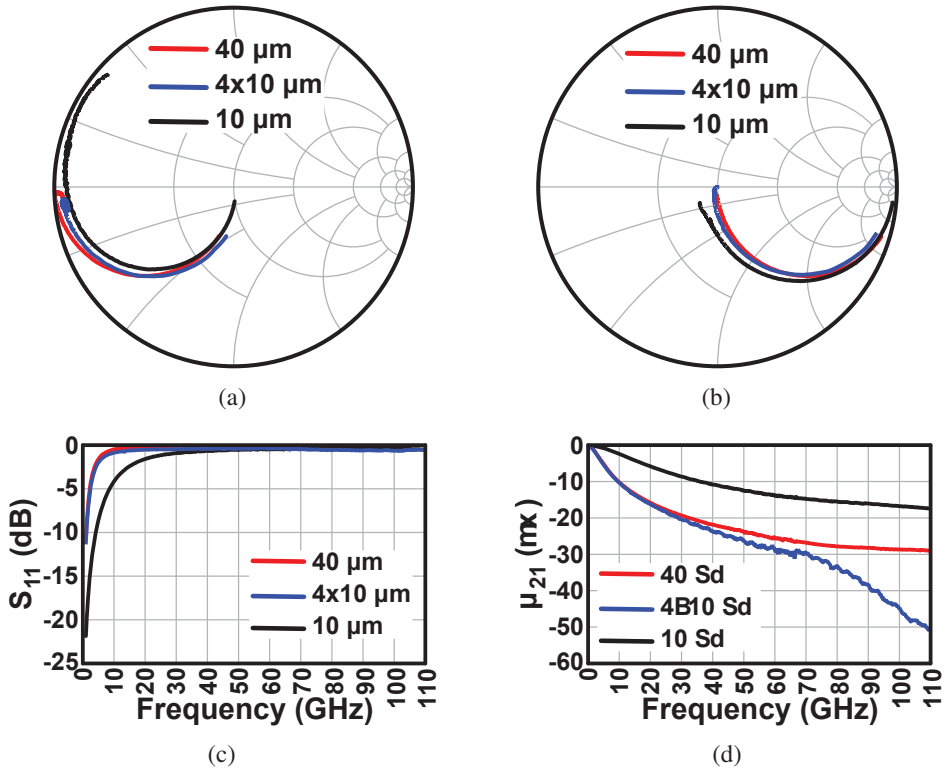


Figure 3.22: Comparison of 10µm, four times cascaded 10µm, and 40µm MIM TL (a) return loss on smith chart from 1 to 110 GHz, (b) insertion loss on smith chart from 1 to 110 GHz, (c) magnitude (dB) of return loss, and (d) magnitude (dB) of insertion loss.

applications for amplifiers.

3.2.5 Application of Conventional Device Models on a W-Band Amplifier

In order to check the validity of the conventional models for W-band applications, a W-Band amplifier is designed with the developed models. The schematic of the amplifier is presented in Fig. 3.29. The chip is, again, manufactured in 65nm standard bulk CMOS and the chip photo is presented in Fig. 3.30. The amplifier is measured with VNA up to 110GHz.

Measurement results are compared with the modeled results in Fig. 3.31. It can be observed from all of the graphs that the device models developed are not working well for W-band frequency region. Hence, in the next section improved models and proposed characterization approaches are presented.

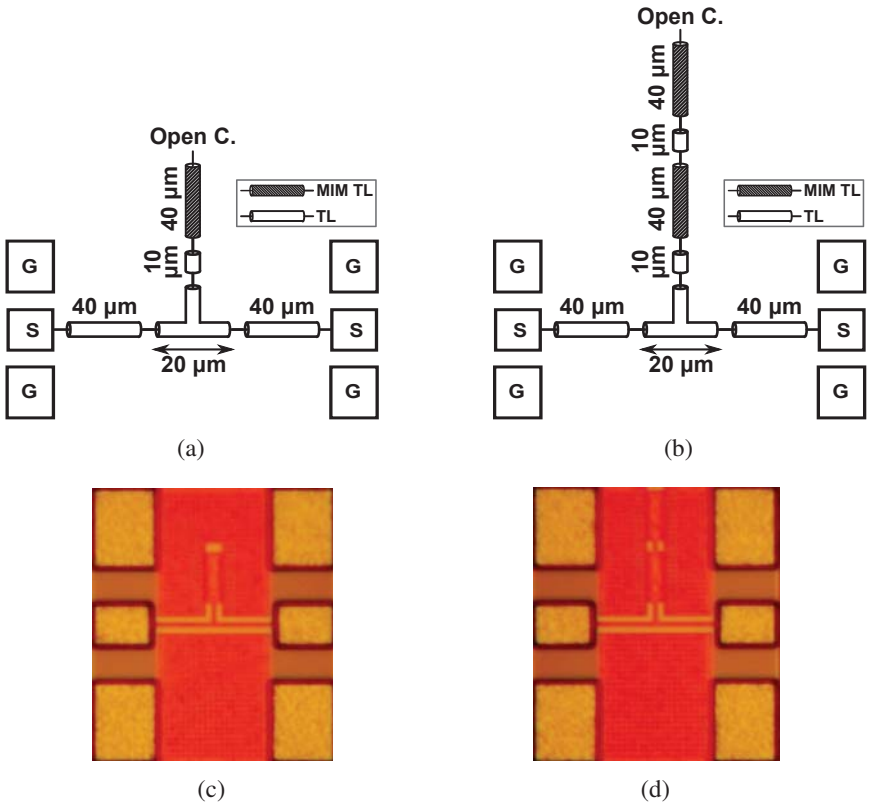


Figure 3.23: Shunt characterization TEGs for MIM TL (a) 40 µm MIM TL is placed on the third port of tee-junction, (b) two 40 µm MIM TL is placed on the third port of tee-junction, (c) chip photo of (a), and (d) chip photo of (b).

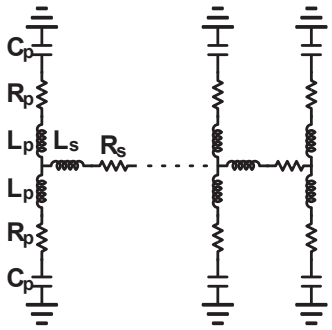


Figure 3.24: Assumed lumped model for MIM TL characterization.

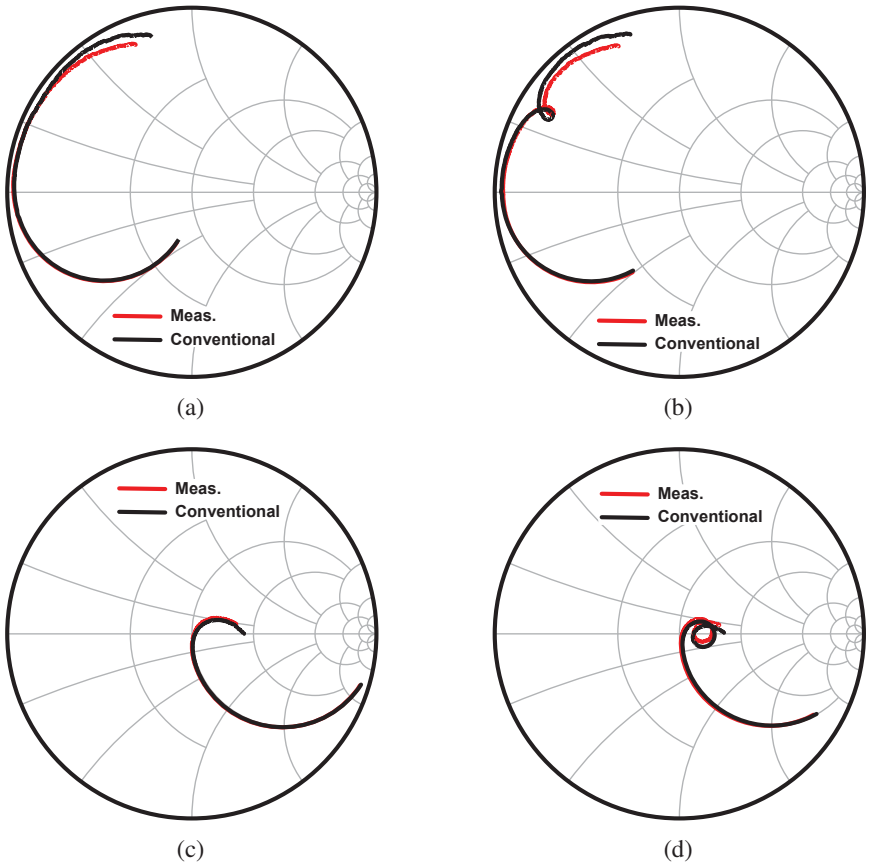


Figure 3.25: S-parameter comparison results of model and measurements on smith charts from 1 to 110 GHz (a) 40 μm MIM TL connected TEG return loss, (b) two 40 μm MIM TL connected TEG return loss, (c) 40 μm MIM TL connected TEG insertion loss, and (d) two 40 μm MIM TL connected TEG insertion loss.

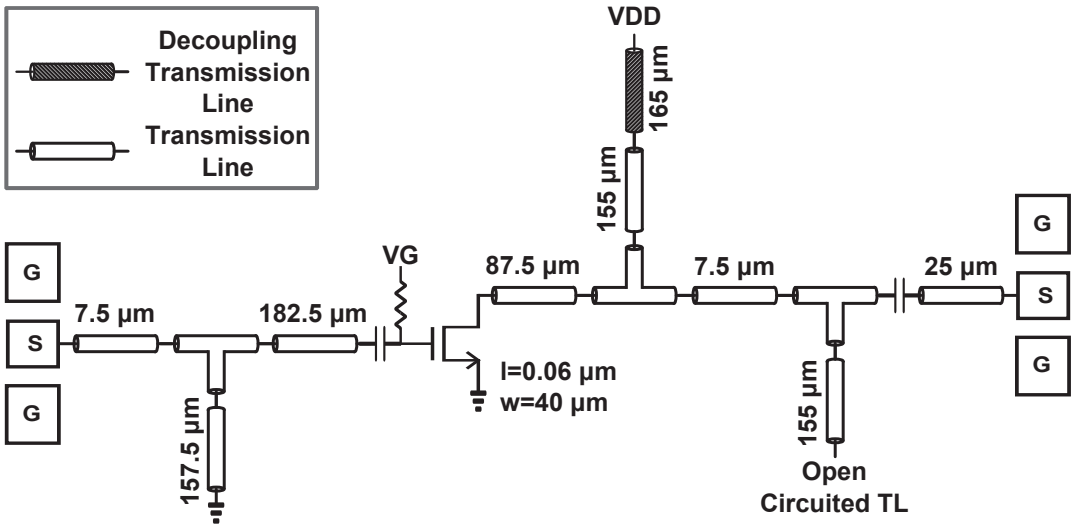


Figure 3.26: Schematic of the designed V-Band Amplifier.

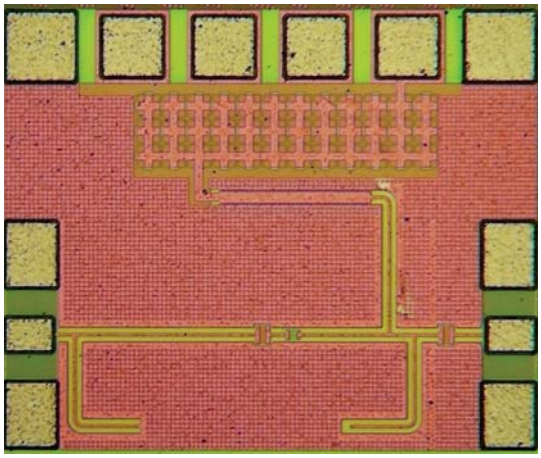


Figure 3.27: Chip photo of the designed V-Band Amplifier.

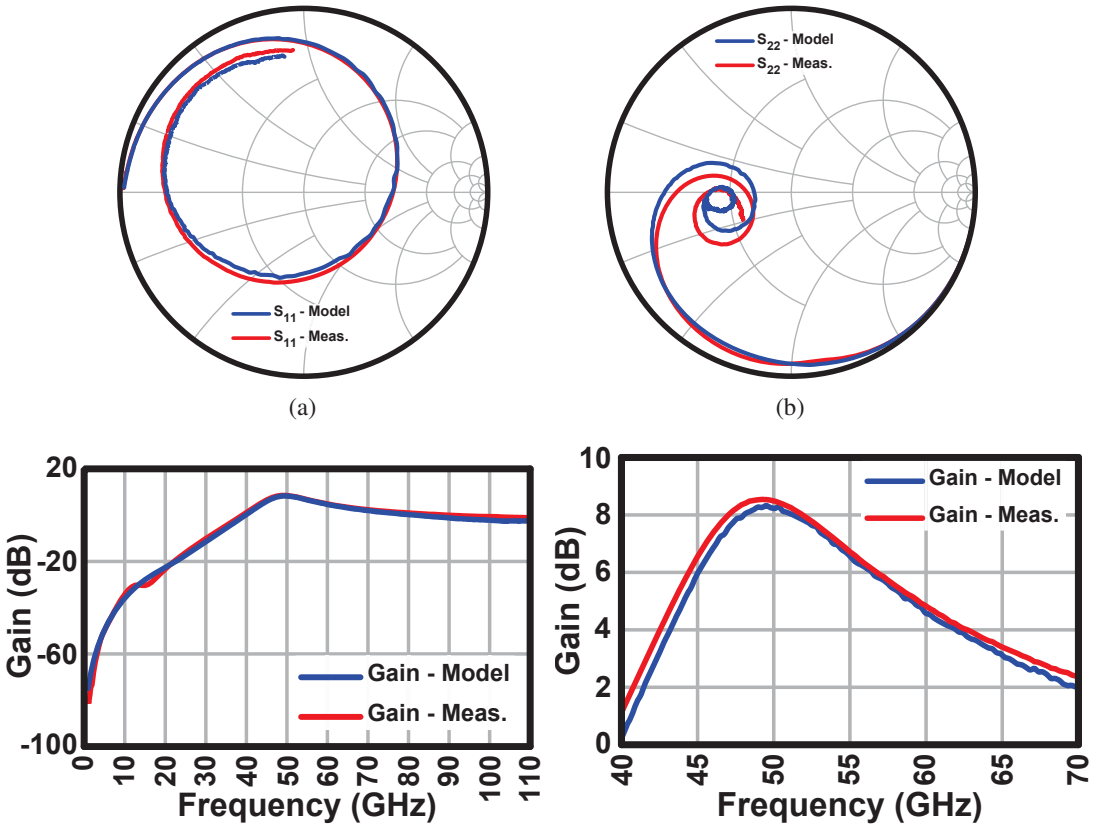


Figure 3.28: S-parameter comparison results of model and measurements for V-Band one-stage amplifier. (a) Input reflection parameters comparison on Smith Chart, (b) Output reflection parameters comparison on Smith Chart, (c) Gain comparison up to 110GHz, and (d) zoomed in version of the Gain.

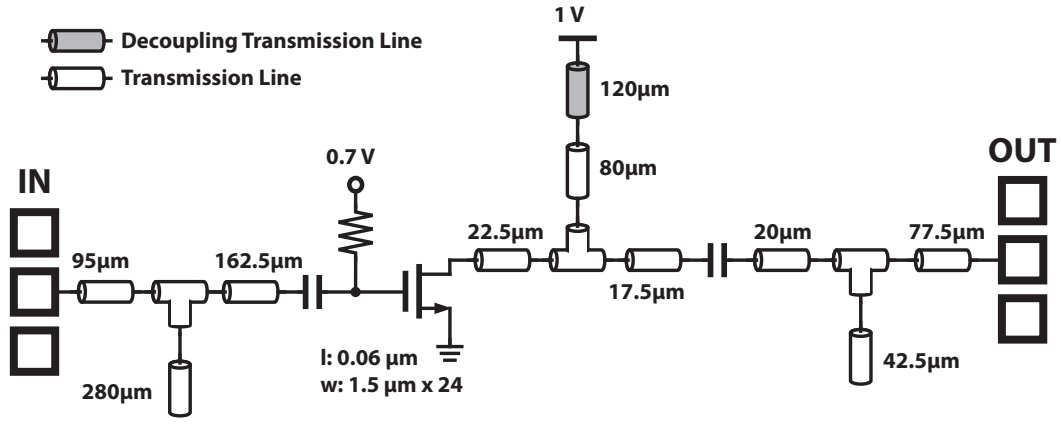


Figure 3.29: Schematic of the designed W-Band Amplifier.

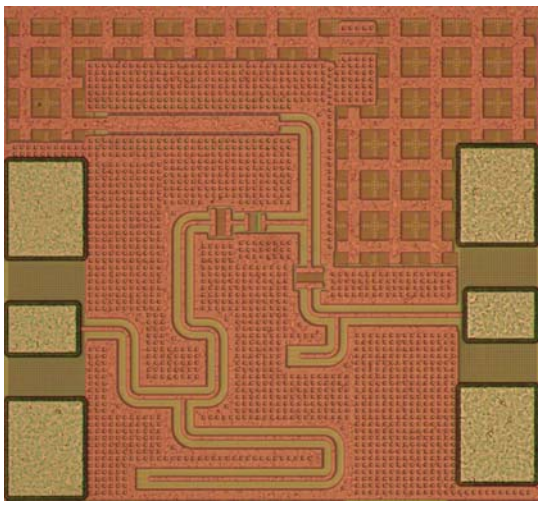


Figure 3.30: Chip photo of the designed W-Band Amplifier.

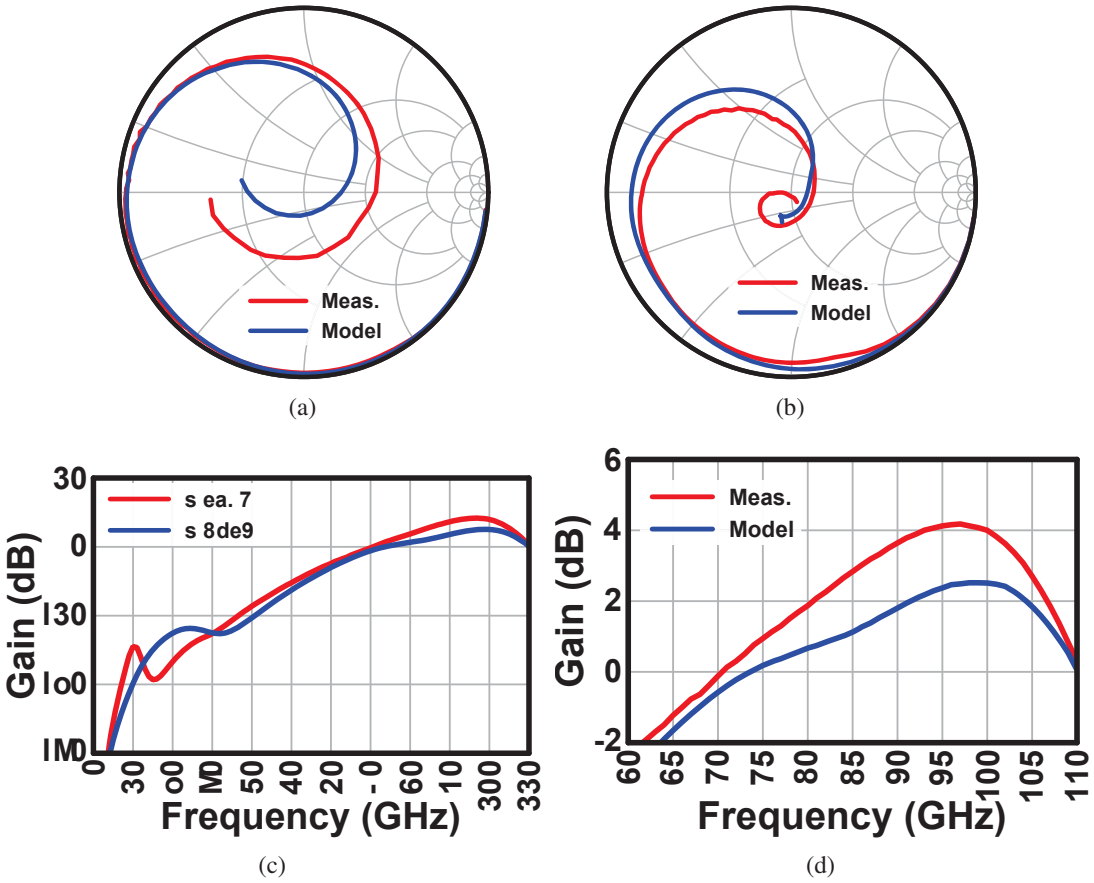


Figure 3.31: S-parameter comparison results of model and measurements for W-Band one-stage amplifier. (a) Input reflection parameters comparison on Smith Chart, (b) Output reflection parameters comparison on Smith Chart, (c) Gain comparison up to 110GHz, and (d) zoomed in version of the Gain.

3.3 Proposed Device Models

In this section, improvement of device models are introduced with different methods than previous conventional methods. Firstly, improvement on transmission line modeling, de-embedding and pad parasitic modeling are introduced. Than, corner characterization method is introduced. After corner characterization, tee-junction characterization is studied and their effects on the designed amplifier simulation results are investigated. Finally, metal-insulator-metal transmission line is characterized accurately with shunt characterization method and, similarly, its effect on amplifier is given.

3.3.1 Improved Pad Parasitic De-Embedding and Transmission Line Models

The main reason of the difference between the model and measurement results at W-band is because of the non-accurate transmission line models after around 70GHz. Mainly, loss factor does not reflect theoretical predictions. As a result, the de-embedding accuracy for other active and passive device characterizations is also decreasing. In order to solve this issue, L-2L de-embedding method is applied again [29] with longer transmission lines. The reason longer transmission lines are used is to decrease the probe-to-probe couplings and multi-reflections inside the device under test. 3.8mm and 1.95mm transmission lines are used to increase the transmission line model accuracy. After the de-embedding of pad parasitics as described in the above section, the transmission line characteristics are achieved.

3.3.2 Corner Characterization

The characterization TEG for corner device is provided again in the following Fig. 3.33. Remember from conventional device model chapter that corners are modeled as simple transmission lines by optimizing the model transmission line lengths using measurement results. From that model there is a deviation between model and measurement S-parameter results. In here, a direct solution for corner is applied. First, as in Fig. 3.33, de-embed the pad parasitics and additional 40 μm transmission lines based on the de-embedding results. The remaining response belongs to 12 cascaded symmetrical and reciprocal corner devices. By solving the remaining response for one corner, corner characterization can be done in terms of S-parameters. The S-parameter results of a corner is obtained by using eigen-value decomposition on the remaining response after de-embedding and the results are presented in Fig. 3.34 in comparison

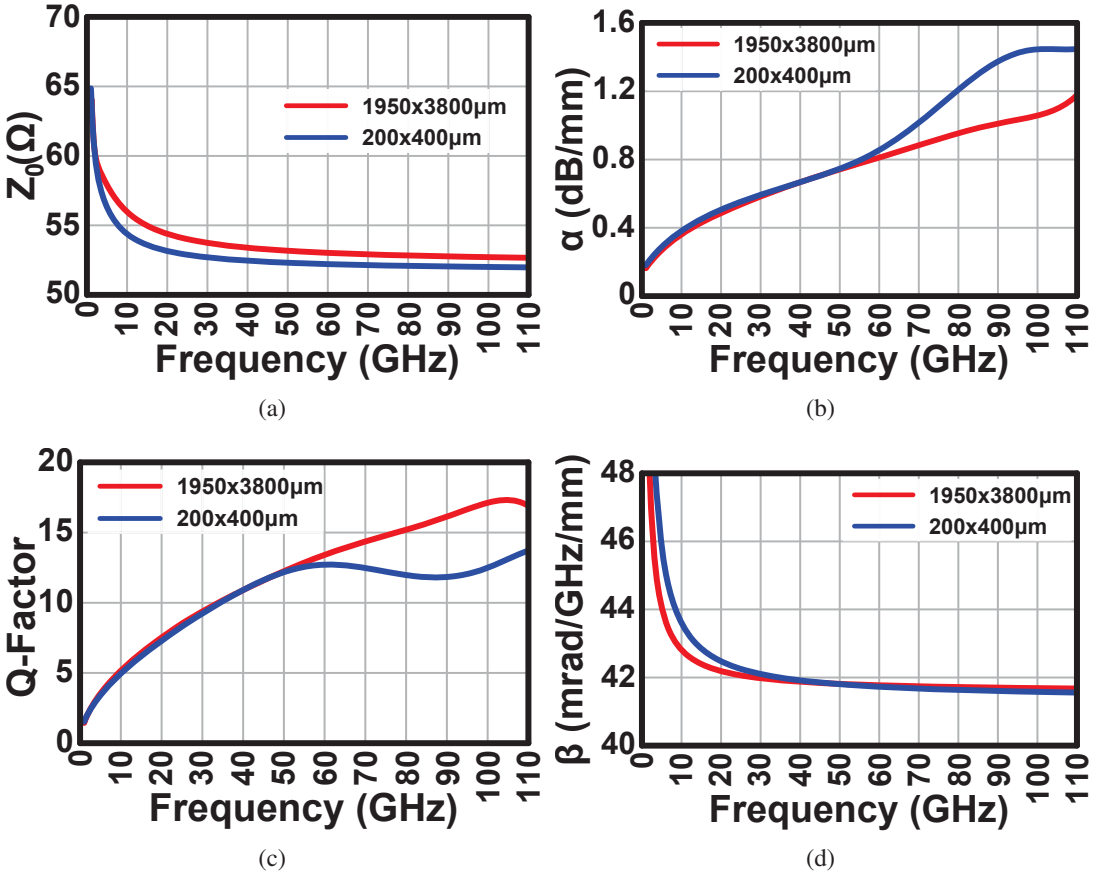


Figure 3.32: Transmission line model parameters acquired with L-2L method for two cases of 200x400µm, and 1950x3800µm. (a) Transmission line characteristic impedance magnitude, (b) loss factor, (c) quality factor, and (d) propagation constant.

with conventional corner model based on transmission lines. After the corner is characterized, 12 of them are cascaded in the simulation environment together with pad parasitics and additional transmission lines and the results are compared with measurement results. As expected they are exactly the same with each other. Since the measurement results are given in Chapter 2, and the characterized results are exactly the same with measurement results the results are not given in here. For the results please refer to second chapter. Red lines in these figures present the characterized results of corners and black lines present the conventional model.

It can be observed that for return loss after 50 GHz the direct characterization and model results starts to deviate from each other. Similarly, for insertion loss the difference starts from 30 GHz. Phase of insertion loss is almost same with each other, however, phase of return loss is very different from each other. Although the results are different

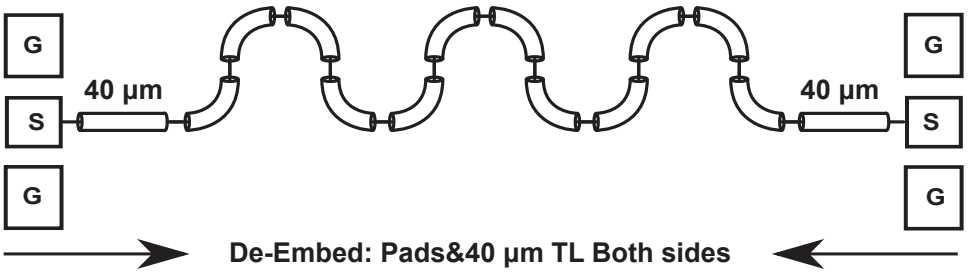


Figure 3.33: Corner characterization TEG, and de-embedding of additional fixtures.

from each other mostly even before 50 GHz, the differences are small. When the characterized corner results are inserted in the simulation results of the amplifier, there is no significant change. This is expected because, as pointed out above, the characterized corner results and modeled results are very close to each other. The difference in value is not so significant, hence the effect is not significant. One can conclude that conventional model is consistent for W-band also. Since the difference is not significant (in fact almost same), the comparison results for amplifier are not provided in here. However, there are several other devices to be improved and tried. For that reason, in the next section tee-junction is characterized and investigated.

3.3.3 Tee-Junction Characterization

Remember the conventional tee-junction model is based on transmission lines. It is done by adjusting the lengths of transmission lines to achieve as similar as the measurement results of two characterization TEGs for tee-junction. In one TEG, third port of tee-junction is terminated with 100 µm open circuited transmission line, and in the other third port of tee-junction is terminated with 2.5 µm short circuited transmission line to ground. Modeled results of these TEGs and measurement results show good agreement up to around 70 GHz. However, the results starts to differ from each other after 70 GHz. So there is room for improvement especially for W-band. Using these two TEGs and the proposed characterization approach in here, tee-junction can be characterized more accurately (which is shown below). Again, these two TEGs are used, because of unwanted error sources from other TEGs, multi-port measurements and multi-port de-embedding.

Geometry of tee-junction is illustrated again in this chapter in Fig. 3.35(a), and the conventional tee-junction model is shown in Fig. 3.35(b). In this proposed characterization method, mainly short circuited transmission line terminated tee-junction characterization TEG is used, and other TEG is used for verification. The

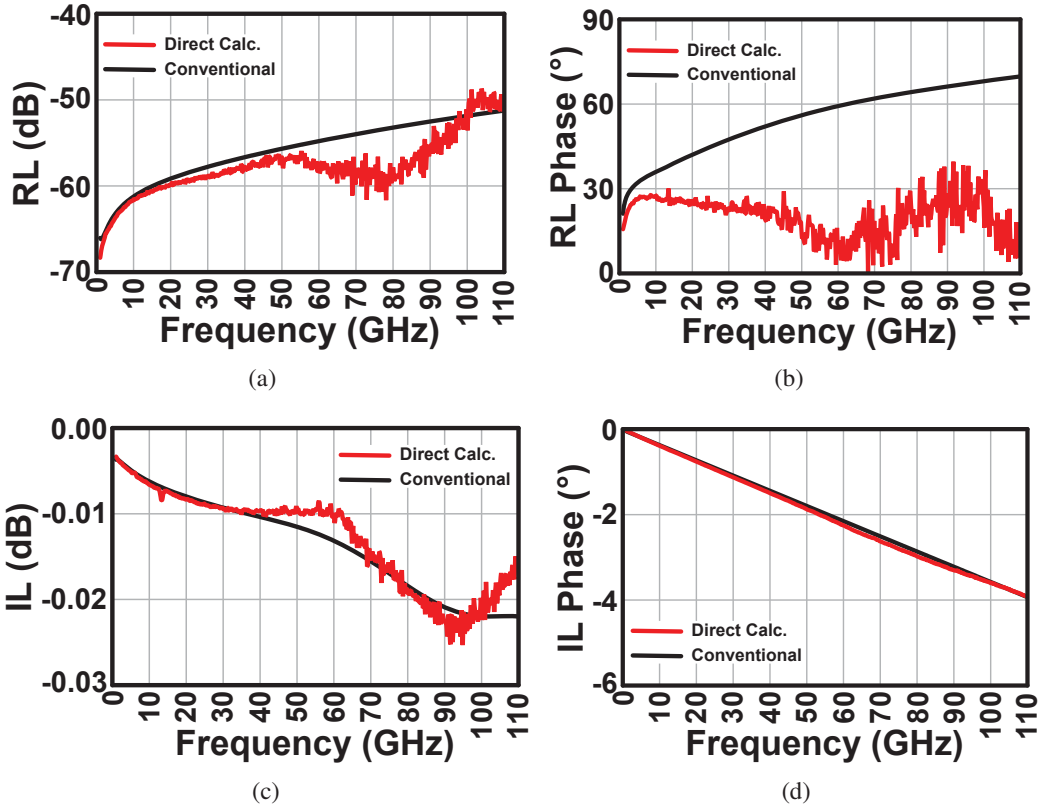
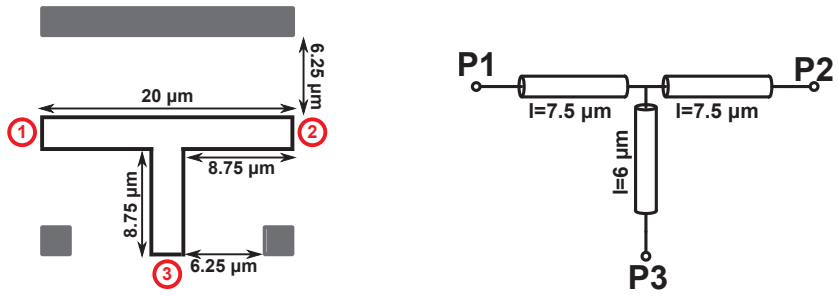


Figure 3.34: S-parameter comparison of corner between direct characterization (red lines) and conventional model (black lines) (a) return loss in magnitude (dB), (b) return loss phase (°), (c) insertion loss in magnitude (dB), and (d) insertion loss phase (°).

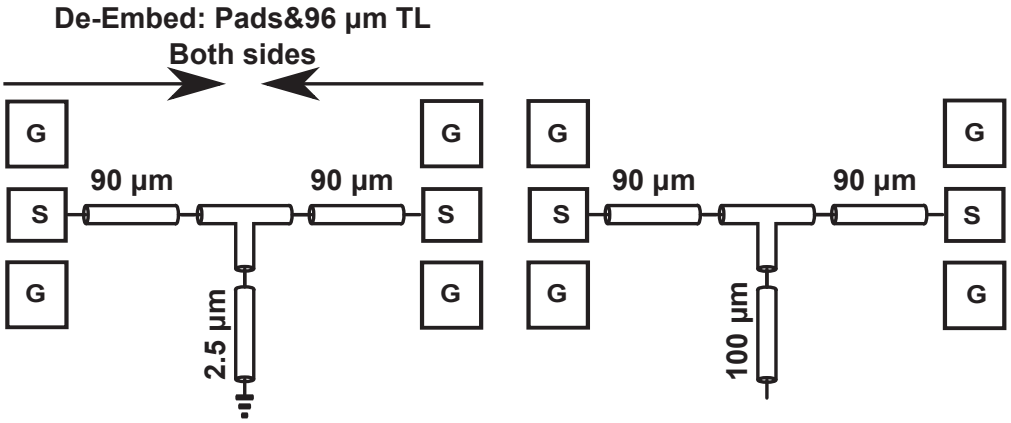
characterization TEG is illustrated in Fig. 3.36(a), and verification TEG is shown in Fig. 3.36(b). For this characterization method the proposed tee-junction model is illustrated in Fig. 3.37, assuming that tee-junction when terminated at its port 3 has symmetrical and reciprocal response. Moreover, tee-junction as a three-port device has symmetrical S-parameter responses for ports 1 and 2.

Note that in this model, lumped components are assumed in the model. For this reason, the de-embedding is done more than the combined transmission line length which is 90 μm. To support the lumped element model, pad parasitics and 96 μm length transmission line is de-embedded, more than the connected transmission line length. This additional 6 μm transmission line length is shown in the model itself. After this de-embedding the remaining response is corresponds to the remaining model within the red dotted line sin Fig. 3.37, now the reference ports are moved to this red dotted lines. The remaining S-parameters can be converted to Z-parameters as in the following equation;



(a) (b)

Figure 3.35: Tee-junction (a) geometry revisited, and (b) conventional model revisited.



(a) (b)

Figure 3.36: Tee-junction TEGs (a) TEG for characterization, and (b) TEG for verification.

$$stoz(S_{\text{de-em}}) = \begin{bmatrix} Z_{11} & Z_{12} \\ Z_{12} & Z_{11} \end{bmatrix} \begin{bmatrix} Z_1 + Z_2 + Z_{\text{short}} & Z_2 + Z_{\text{short}} \\ Z_2 + Z_{\text{short}} & Z_1 + Z_2 + Z_{\text{short}} \end{bmatrix} \tag{3.25}$$

where Z_1 is the series component in the model, and Z_2 is the component to the third port after the junction, and Z_{short} is the impedance from the reflection of the short circuited 8 µm transmission line. That is Z_{12} is the series connection of Z_2 and Z_{short}. From this equation one can easily calculate the series component Z_1 by the following equation;

$$Z_1 = Z_{11} - Z_{12} \tag{3.26}$$

Remember that Z_{short} is the impedance from the reflection of the short circuited 8 µm transmission line, for which the length is the total length of short circuited 2.5 µm shunt connected transmission line and 5.5 µm additional transmission line to realize Z_2 as lumped constant. These additional transmission line lengths are adjusted to give more

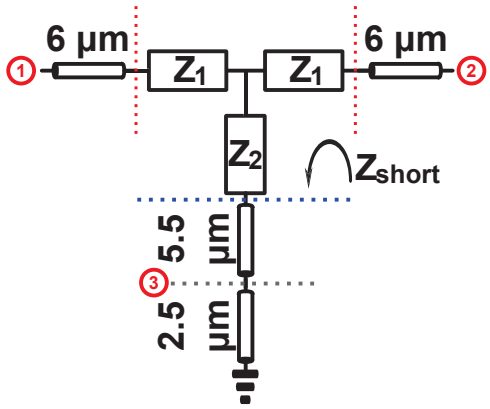


Figure 3.37: Proposed tee-junction model.

accurate results for the verification TEG (Fig. 3.36(b)). Z_{short} can be calculated from the transmission line models while short circuited. Than Z_2 can be calculated as follows;

$$Z_2 = Z_{12} - Z_{short} \tag{3.27}$$

After calculating the model parameters and combine with additional transmission lines, the new tee-junction model is obtained. In order to compare this new model with conventional model and measurement results, the TEGs are reconstructed based on transmission line model, pad model, and tee-junction models. The S-parameter comparison results are presented in Fig. 3.38. Since the model is directly calculated from short circuited transmission line terminated TEG, S-parameters are exactly the same with measurements results as can be observed from Figs. 3.38(b) and 3.38(d), respectively for return loss and insertion loss. Moreover, for the verification TEG, i.e. open circuited 100 µm length transmission line terminated TEG, the return loss results and insertion loss results for the proposed model is much more accurate than conventional model in the overall frequency band especilly in W-band. With this proposed model tee-junction can be characterized more accurately than conventional model based on the measurement results of characterization TEGs.

In order to understand this reason, a safe and most accurate proposal is a full three-port S-parameter characterization of tee-junction based on two-port measurement results. A full characterization method using only open circuited transmission lines terminated at port 3 of tee-junction with three different lengths can accurately characterize tee-junction S-parameters, as can be observed from Fig. 3.39. Note that short circuited transmission lines are not used because of accuracy issues about measurements.

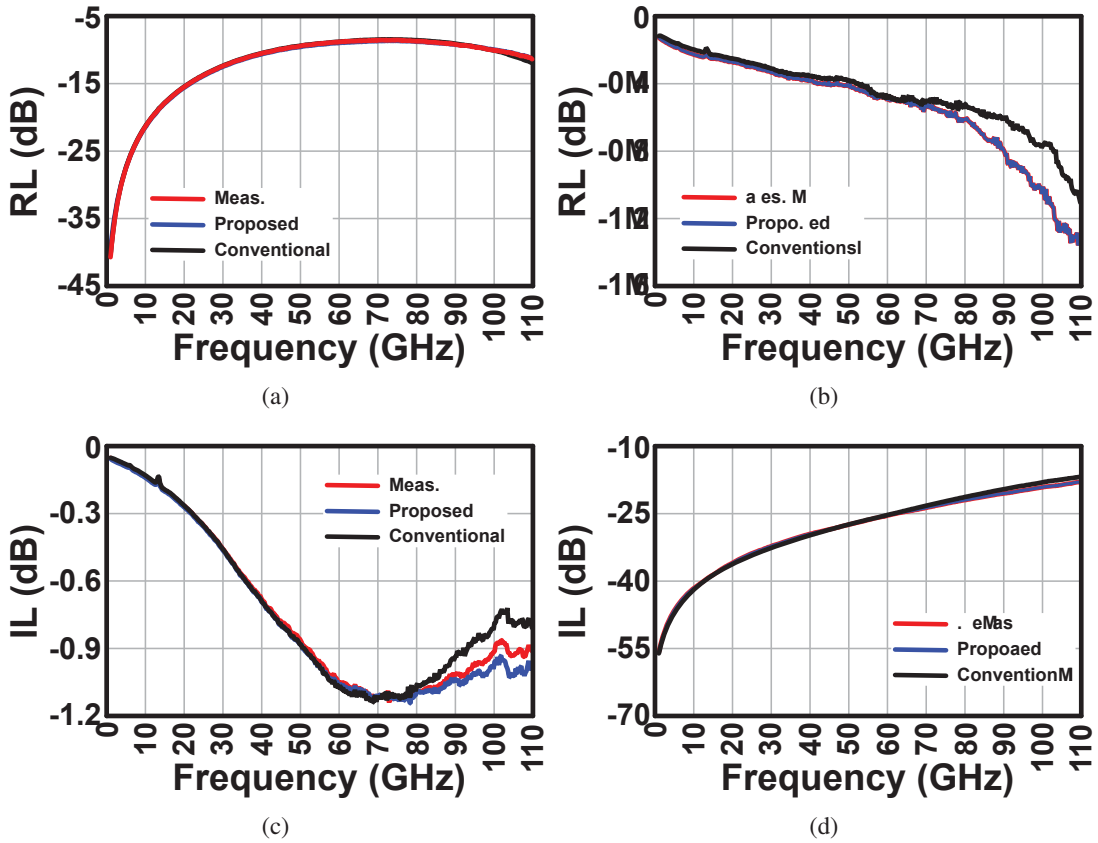


Figure 3.38: S-parameters comparison results between proposed model (blue lines), conventional model (black lines), and measurement results (red lines) (a) open circuited transmission line terminated TEG return loss magnitude (dB), (b) short circuited transmission line terminated TEG return loss magnitude (dB), (c) open circuited transmission line terminated TEG insertion loss magnitude (dB), and (d) short circuited transmission line terminated TEG insertion loss magnitude (dB).

3.3.4 Metal-Insulator-Metal Transmission Line Characterization

Metal-insulator-metal (MIM) TL is mainly used for DC to RF decoupling and isolation, as it is noted in the previous chapter. Other than decoupling duty of MIM transmission line, it is also used in the inter-stage matching blocks to provide a virtual ground like impedance for short circuited transmission line realization, and owing to its high losses the stability factor is improved for the amplifier. For these reasons, accurate model of MIM TL is very important. Moreover, remember from the previous section that MIM TL models are not very accurate especially at W-band. Although MIM transmission line is a distributed component, conventional model is based on

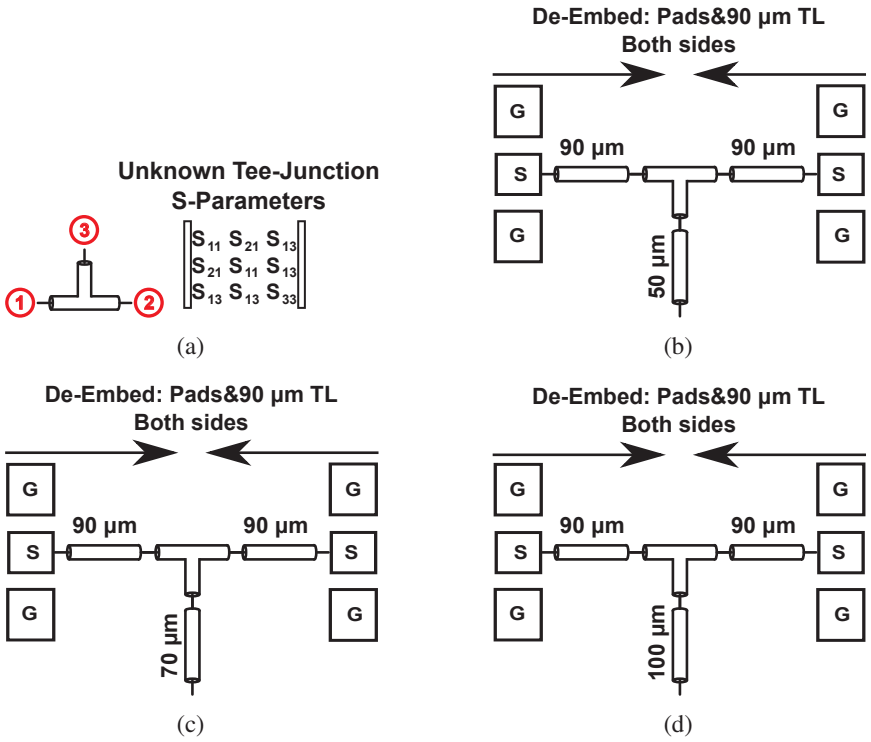


Figure 3.39: Proposed full characterization method (a) tee-junction port definitions and unknown S-parameters, (b) characterization TEG with open circuited 50 µm transmission line terminated at port 3, (c) characterization TEG with open circuited 70 µm transmission line terminated at port 3, (d) characterization TEG with open circuited 100 µm transmission line terminated at port 3.

lumped-constant parameters optimized using the two measurement results, with very good accuracy up to around 70GHz. In here, MIM TL is accurately characterized based on the same TEGs measurement results. The two TEGs are revisited in here, in Fig. 3.40, together with their related de-embedding methods. Symmetrical ports (port 1 and 2) of tee-junctions in these two TEGs are connected to probing pads with 40µm TLs. Third port of tee-junction in Fig. 3.40(a) is terminated with a 10µm TL with 40µm MIM TL whose other port is left open. In the other TEG, shunt part of previous TEG is repeated two times. The first step upon characterization of MIM TL is to de-embedded these additional parts in TEGs, which are pad parasitics and 40µm TLs from both sides. The remaining structures can be observed in Fig. 3.41.

In the following calculation method MIM TL is assumed to be symmetrical and reciprocal. Its S-parameters based on this assumption can be given as follows;

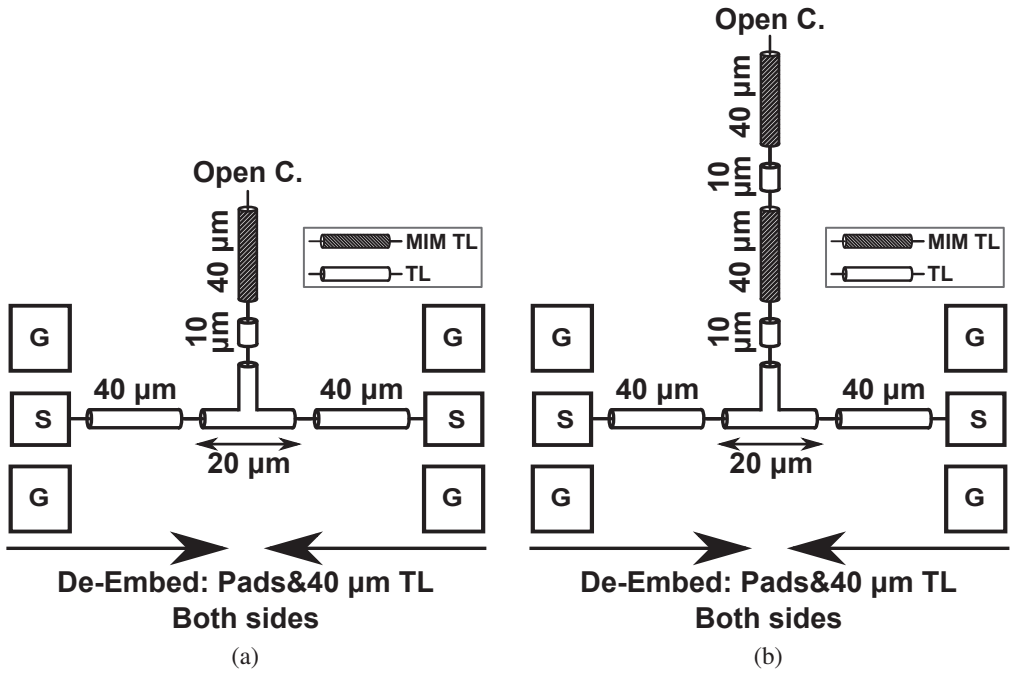


Figure 3.40: MIM TL characterization TEGs and related de-embedding illustration (a) 40µm MIM TL shunt connected to third port of tee-junction, and (b) two 40µm MIM TLs shunt connected to third port of tee-junction a 10µm TL in between.

$$[S_{\text{MIM-TL}}] = \begin{bmatrix} S_{\text{MIM-TL},11} & S_{\text{MIM-TL},21} \\ S_{\text{MIM-TL},21} & S_{\text{MIM-TL},11} \end{bmatrix} \tag{3.28}$$

In this characterization method, the basic idea is to find S-parameters of MIM TL from the reflection characteristics that one can obtain from the measurement results of two TEGs. For that reason the common structure used in here can be observed in Fig. 3.42.

This structure is a three-port structure, which is a combination of a tee-junction and a 10µm TL connected at the third port of tee-junction. Note that to further proceed tee-junction three port S-parameters are known beforehand along with the TL model. That is to say all parameters of this structure is known beforehand. The used tee-junction model is the conventional one, since the proposed one did not provide good results in terms of amplifier characteristics. This three-port structure can be presented in terms of S-parameters as follows;

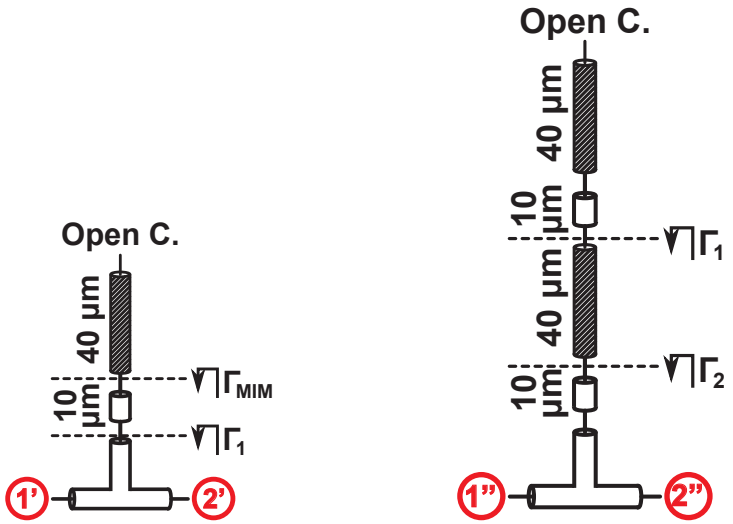


Figure 3.41: Remaining structure after de-embedded of additional fixtures from TEGs (a) 40µm MIM TL shunt connected, and (b) two 40µm MIM TLs shunt connected.

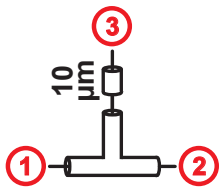


Figure 3.42: Used common structure in the above presented characterization TEGs for MIM TL.

$$[S_{\text{T-TL}}] = \begin{bmatrix} S_{11} & S_{21} & S_{13} \\ S_{21} & S_{11} & S_{13} \\ S_{13} & S_{13} & S_{33} \end{bmatrix} \tag{3.29}$$

As it can be observed from the above equation ports 1 and 2 are symmetrical. Assuming that this three port structure is terminated with a device having reflection coefficient Γ, the structure is now a two port structure and S-parameters for two port can be written in terms of known three port S-paremeters S_{11}, S_{21}, S_{13}, S_{33}, and unknown reflection parameter Γ as in the following equation;

$$[S^{3,\Gamma}_{\text{T-TL}}] = \begin{bmatrix} S_{11} & S_{21} \\ S_{21} & S_{11} \end{bmatrix} + \frac{{S_{13}}^2}{1/\Gamma - S_{33}} \begin{bmatrix} 1 & 1 \\ 1 & 1 \end{bmatrix} \tag{3.30}$$

where $[S^{3,\Gamma}_{\text{T-TL}}]$ means that known three port structure is terminated at its port 3 with a device having reflection coefficient of Γ. The reflection coefficient of MIM TL ($\Gamma_{\text{MIM-TL}}$) when open circuited at one end can be calculated using parameters in Eq. (3.28) like below equation;

$$\Gamma_{\text{MIM-TL}} = S_{\text{MIM-TL},11} + \frac{S^2_{\text{MIM-TL},21}}{1 - S_{\text{MIM-TL},11}} \tag{3.31}$$

$\Gamma_{\text{MIM-TL}}$ can be calculated from the de-embedded results of characterization TEGs provided in Fig. 3.41(a). This result can be given in the equation below;

$$[S^{\Gamma_{\text{MIM-TL}}}_{\text{Meas}}] = \begin{bmatrix} S_{11} & S_{21} \\ S_{21} & S_{11} \end{bmatrix} + \frac{{S_{13}}^2}{1/\Gamma_{\text{MIM-TL}} - S_{33}} \begin{bmatrix} 1 & 1 \\ 1 & 1 \end{bmatrix} \tag{3.32}$$

Hence, reflection coefficient can be calculated using measured S-parameters from either return loss or insertion loss results;

$$\Gamma_{\text{MIM-TL}} = \frac{1}{S_{33} + \frac{S^2_{13}}{S^{\Gamma_{\text{MIM-TL}}}_{\text{Meas},11} - S_{11}}} \tag{3.33}$$

In a similar way, Γ_2 shown in Fig. 3.41(b) can be calculated form the corresponding measurement results as follows;

$$\Gamma_2 = \frac{1}{S_{33} + \frac{S^2_{13}}{S^{\Gamma_2}_{\text{Meas},11} - S_{11}}} \tag{3.34}$$

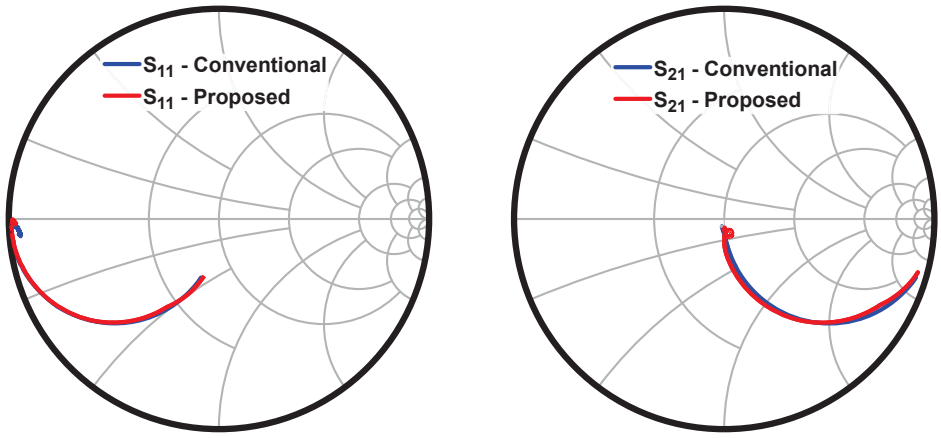
In order to proceed further one can relate Γ_2 to MIM TL S-parameters and Γ_1 reflection coefficient shown in Figs. 3.41(a) and 3.41(b) as in Eq. (3.35). Furthermore, Γ_1 can be found by terminating a 10μm TL with $\Gamma_{\text{MIM-TL}}$. S-parameters of a 10μm TL is given in Eq. (3.36). Hence, Γ_1 can be written as in Eq. (3.37) and can be calculated because all parameters are known.

$$\Gamma_2 = S_{\text{MIM-TL},11} + \frac{S^2_{\text{MIM-TL},21}}{1/\Gamma_1 - S_{\text{MIM-TL},11}} \tag{3.35}$$

$$[S_{\text{TL-10μm}}] = \begin{bmatrix} S_{\text{TL-10μm},11} & S_{\text{TL-10μm},21} \\ S_{\text{TL-10μm},21} & S_{\text{TL-10μm},11} \end{bmatrix} \tag{3.36}$$

$$\Gamma_1 = S_{\text{TL-10μm},11} + \frac{{S_{\text{TL-10μm},21}}^2}{1/\Gamma_{\text{MIM-TL}} - S_{\text{TL-10μm},11}} \tag{3.37}$$

Now, with calculated three parameters of reflections Γ_1, Γ_2, and $\Gamma_{\text{MIM-TL}}$, S-parameters



(a) (b)

Figure 3.43: Found S-parameters of MIM TL illustrated on smith charts (red lines present proposed method results and blue lines present drom direct two port measurement results from 1 to 110 GHz) (a) return loss, (b) insertion loss.

of MIM TL can be calculated as in the following two equations;

$$S_{\text{MIM-TL},11} = \frac{\Gamma_2 - \Gamma_{\text{MIM-TL}}\Gamma_1}{1 + (\Gamma_2 - \Gamma_{\text{MIM-TL}} - 1)\Gamma_1} \tag{3.38}$$

$$S_{\text{MIM-TL},21} = \sqrt{(\Gamma_{\text{MIM-TL}} - S_{\text{MIM-TL},11})(1 - S_{\text{MIM-TL},11})} \tag{3.39}$$

Using two characterization TEGs measurement results from Fig. 3.40, the above proposed calculation method is applied and S-parameters of MIM TL are found. The results are presented in Fig. 3.43 using red color lines from 1 to 110 GHz.

In order to compare the results, direct series connected 40μm MIM TL S-parameters are found as shown in Fig. 3.44 after de-embedding of pad parasitics and additional 45μm length TLs. The results are also presented in Fig. 3.43 using blue lines. As it can be observed there are differences between the two results. In order to compare, using the conventional and proposed MIM TL models, pad parameters and TL models the shunt characterization TEGs (Fig. 3.40) are reconstructed in the simulation environment. Both results are compared together with measurement results. The results are presented in Fig. 3.45 using red lines for measurements, blue lines for proposed method and black lines for conventional results from 1 to 110 GHz. As it can be seen the proposed method can achieve very accurate results in comparison with conventional method from 1 to 110 GHz for both shunt characterization structures.

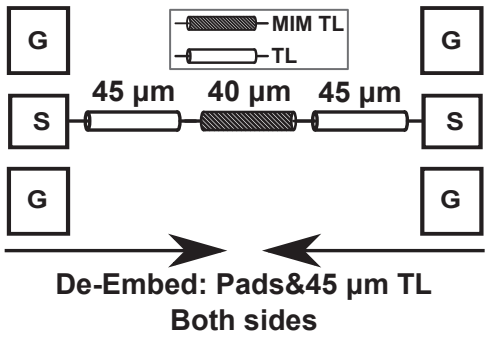


Figure 3.44: Direct series connected characterization TEG.

3.3.5 Application of Updated Device Models on a W-Band Amplifier

The updated device models are applied on the same W-band amplifier presented in the above sections. The schematic of the amplifier is presented in Fig. 3.29. The chip photo is presented in Fig. 3.30. The amplifier is measured with VNA up to 110GHz.

Measurement results are compared with the model results in Fig. 3.46. It can be observed from all of the graphs that the device models developed are well-matched thanks to the improvements on the device models that are explained in the above section.

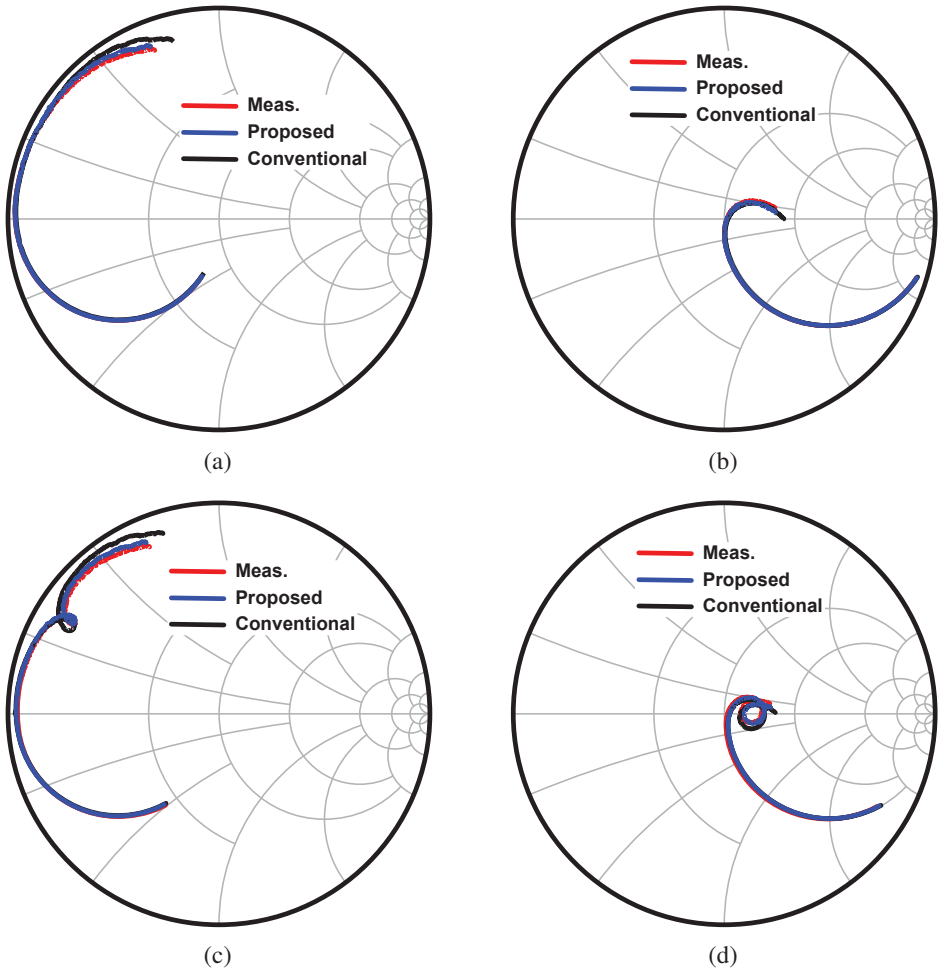


Figure 3.45: Shunt characterization TEGs comparison for proposed (blue lines), conventional models (black lines), and measurement results (red lines) from 1 to 110 GHz on smith charts (a) 40μm MIM TL shunt connected TEG return losses, (b) 40μm MIM TL shunt connected TEG insertion losses, (c) two 40μm MIM TLs shunt connected TEG return losses, and (d) two 40μm MIM TLs shunt connected TEG insertion losses.

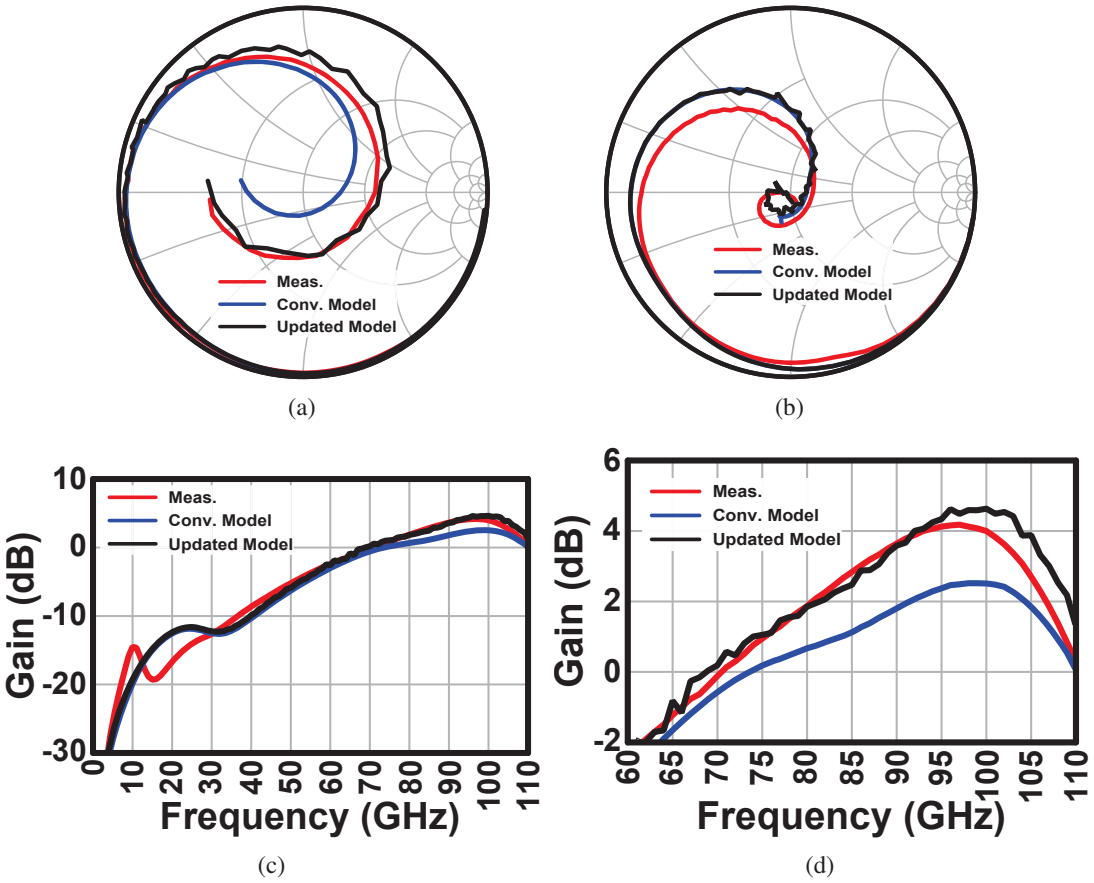


Figure 3.46: S-parameter comparison results of conventional model, updated model and measurements for W-Band one-stage amplifier. (a) Input reflection parameters comparison on Smith Chart, (b) Output reflection parameters comparison on Smith Chart, (c) Gain comparison up to 110GHz, and (d) zoomed in version of the Gain.

3.4 Differential Device Characterizations and Applications on Differential Amplifiers

In wireless tranceiver and many other systems, single-ended or differential circuits are used according to the needs and specifications. For instance, in [9], power amplifier and low-noise amplifier are designed as single-ended to decrease area, increase the flexibility on layout, and decrease the complexity of wire-bond connections from chip to board hence decreasing the wire-bond parasitics and amplitude and phase imbalance between differential signals. On the other hand, differential amplifiers are also used, e.g. to realize RF amplifiers, which are connected to mixers, and local oscillator buffers to mixers due to requirements of higher order modulations and the needs of differential signaling. Other than using single-ended circuit topologies, transceivers can also be realized as fully differential [10] to decrease substrate, DC feed and bias noise contributions form supplies, thus with increased signal to noise ratios. For both cases, differential amplifiers play a vital role in their specific applications. One of the commonly used topology in differential amplifiers is capacitive cross coupled differential amplifiers, this topology uses neutralization technique to increase the gain of the amplifier by introducing negative capacitances to gate-to-drain parasitic capacitance of transistors.As a result the gain of the amplifier is increased. An example circuit schematic for crossing part is given in Fig. 3.47. In the schematic the circuit is symmetrical, however, when the layout of this circuit is considered the crossing part may behave asymmetrical. This is because of amplitude and phase imbalance occurred in the crossing part even if the rest of the circuit is symmetrical, this phenomena also decrease circuit performance. Especially phase imbalance is critical when exactly 180° phase is desired between differential signals. For the sake of symmetry in differential amplifiers a cross-line and its characterization is introduced in here. Before introducing cross-line structure and its characterization, in the next sub-section virtual-thru de-embedding method is extended for four-port Ground-Signal-Signal-Ground pads using mixed-mode S-parameters and their properties.

3.4.1 Four-Port Ground-Signal-Signal-Ground De-Embedding

A physical thru de-embedding method is examined for four-port networks in [43]. After measurement of direct thru structure mixed-mode S-parameter conversions are applied and pure common and differential modes are extracted from mixed-mode S-parameters. By using a Π-model for the two different modes pad parasitics are calculated. Unfortunately, as it is same case with two-port networks a direct thru

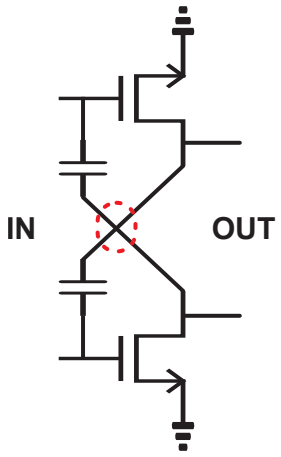


Figure 3.47: An example capacitive cross coupled differential amplifier (crossing part is shown with red dashed circle).

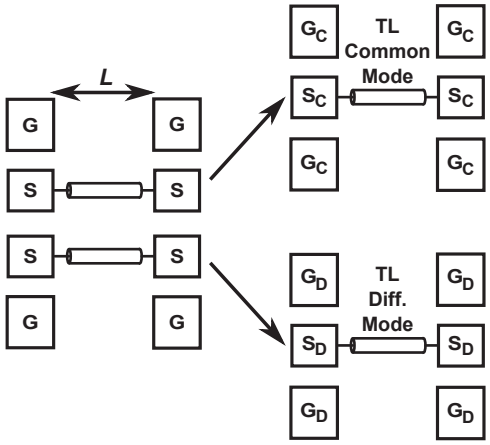
connection is affected by undesired coupling between probes. Moreover, if there is a transition is included between the pads, after some frequency point the pad parasitics cannot be assumed lumped constant, hence the de-embedding would be a task more harder than previous cases. For this reason, L-2L de-embedding method is extended for four-port networks and GSSG pads. Using this method, virtual-thru connection of four-port pads can be calculated in terms of differential mode, common mode, and as a four-port network. The illustration of four-port transmission line structures for virtual-thru method is illustrated in Fig. 3.48. Since these structures' S-parameters responses are symmetrical and reciprocal four-port S-parameters network representation together with pad responses can be given as;

$$[S_{\mathrm{GSSG,TL}}] = \begin{bmatrix} S_{11} & S_{12} & S_{13} & S_{14} \\ S_{12} & S_{11} & S_{14} & S_{13} \\ S_{13} & S_{14} & S_{11} & S_{12} \\ S_{14} & S_{13} & S_{12} & S_{11} \end{bmatrix} \tag{3.40}$$

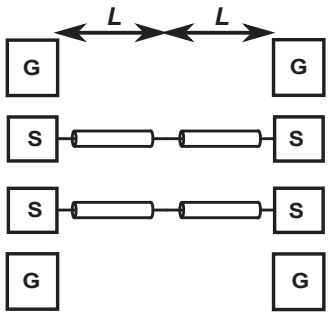
The conversions from single-ended to mixed-mode S-parameters conversion for any four-port network can be given as [44];

$$[S_{\mathrm{MM}}] = [M][S][M]^{-1} = \begin{bmatrix} S_{\mathrm{dd}} & S_{\mathrm{dc}} \\ S_{\mathrm{cd}} & S_{\mathrm{cc}} \end{bmatrix} \tag{3.41}$$

where $[S_{\mathrm{MM}}]$ is the mixed-mode S-parameters which is calculated from four-port single-ended S-parameters denoted as $[S]$. S_{dd} is pure differential mode of the network, and



(a)



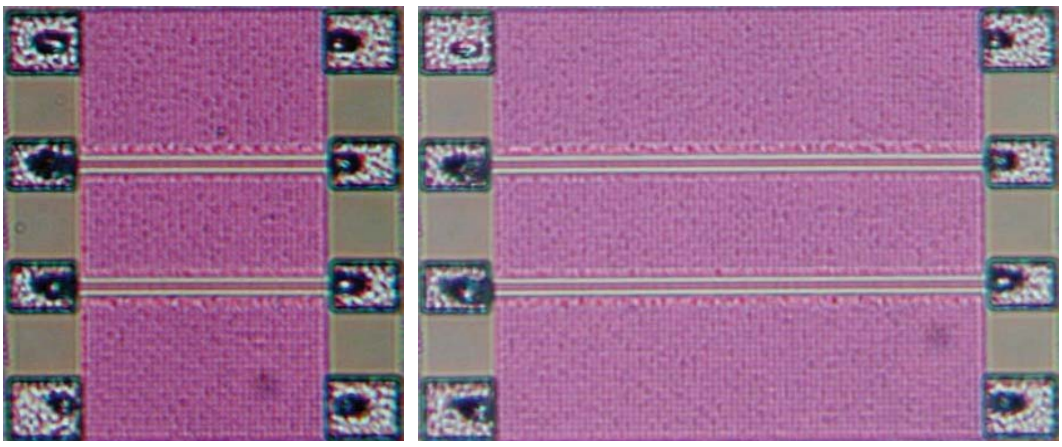
(b)

Figure 3.48: Four-port TL structures used for de-embedding (a) with length "L" and illustration of common and differential mode separation, and (b) with length "2L" (Note that two TLs are connected in series for illustration purposes regarding lengths).

S_{cc} is pure common mode of the network. Moreover, S_{dc} and S_{cd} defines the two mode conversion of the network. These pure modes and mode conversions are all two by two matrices. Furthermore, $[M]$ is defined as in the following equation;

$$[M] = \frac{1}{\sqrt{2}} \begin{bmatrix} I & -I \\ I & I \end{bmatrix} \tag{3.42}$$

where I is two by two identity matrix. When one apply this conversion on a S-parameter matrix given in Eq. (3.40), it can be observed that the mode conversions are 0. As a result, two-fold symmetrical and reciprocal networks can be defined as two separate two-port networks based on pure differential and common modes. An example is illustrated for "L" length four-port TL networks in Fig. 3.48(a). Note that same can be applied for structure "2L". The measurements are done using four-port VNA up to 67 GHz, and the measured structures chip micrographs are given in Fig. 3.49. After the modes are separated for the



(a) (b)

Figure 3.49: Chip micrographs for four-port TL structures (a) with length "L", and (b) with length "2L".

two structure, virtual-thru responses for both modes can be calculated as treating them separate two-port networks. The applied virtual-thru responses are illustrated in Fig. 3.50.

From Fig. 3.50(a), when the calculations are done differential thru connection of left and right pads are obtained. Similarly, from Fig. 3.50(b) common mode thru connections of left and right pads are obtained. The rest is same with two-port de-embedding case, however, pad parasitics are extracted for the two modes, i.e. two different two-port networks. Both Π-, and T-model for pad models are calculated form Y-, and Z-parameters of the networks. Using both models de-embeddings are done for both modes and TL characteristics are compared with each other. Fig. 3.51(a) presents the obtained characteristic impedance for both modes considering two different pad models. Since there is a large ground plane between the two transmission line in the structure, both common mode and differential mode should be around 50Ω. It can be observed from this figure that T-model has better accuracy as compared to Π-model for both common and differential mode of the four-port network. The mean values of characteristic impedance ($Z_{ch} = \sqrt{Z_{cc}Z_{dd}}$) results proves also that T-model has better accuracy while observing the two-port TL characteristic impedance. Note that the algorithm presented for two-port de-embedding case in section 3.2.1 cannot be applied in here, since both T-model and Π-model are above than flat characteristic impedance value for differential mode and below for common mode.

Fig. 3.51(c) provides results for loss term of both modes and for comparison two-port TL loss term is provided. The results show well agreement with each other which should be the case since there is a large ground plane between the TL and the coupling between

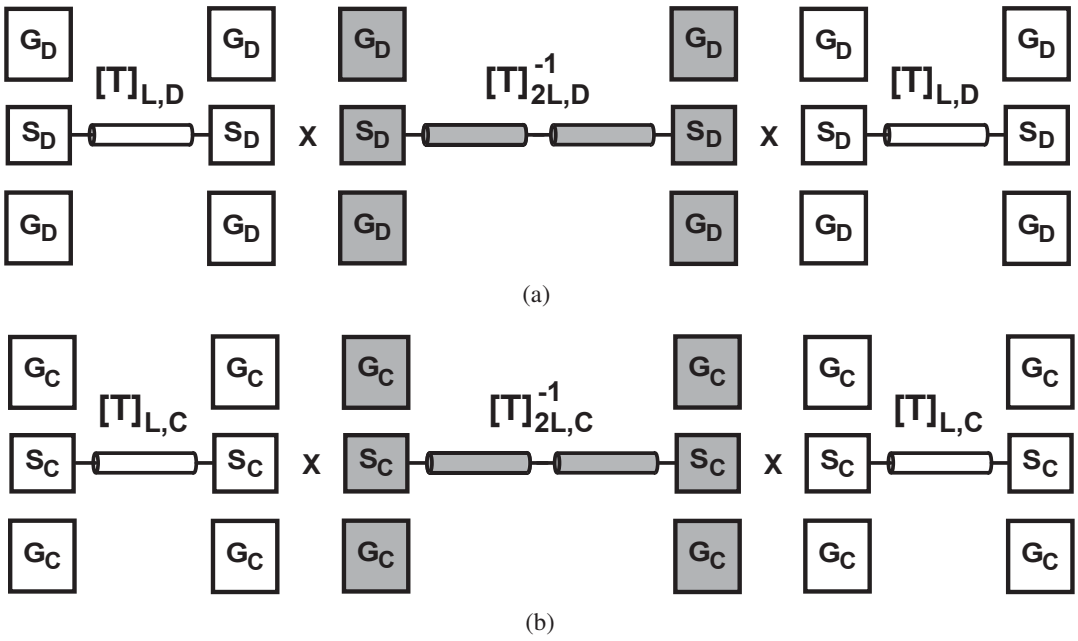


Figure 3.50: Illustration of virtual-thru method application on mixed-mode S-parameters (a) application on differential mode, and (b) application on common mode (gray figures presents inverse T-parameters of the corresponding network).

TLs are considered to be very low. One can observe similar facts in Fig. 3.51(d) which provides results for propagation constant up to 67 GHz. For the de-embedding of GSSG pads T-model for pure modes are assumed. This pad model for four-port GSSG is used in the rest of this section. Next section introduced electrically symmetrical cross-line structure to be used in differential amplifiers.

3.4.2 Cross-Line Structure and Characterization Method

As it is mentioned in the beginning of this section, for differential amplifiers to provide well behaved characteristics, phase and amplitude imbalance should be as low as possible. For this reason, an electrically symmetrical cross-line is introduced in Fig. 3.52. In Fig. 3.52(a), an illustration with port numbering is presented. White areas in this figure present top metal layer and a lower metal connection with vias. Furthermore, gray areas are a lower metal layer connecting ports 1 to 4 and 2 to 3. This structure is electrically symmetrical and the S-parameters of this structure has similar S-parameters presented in Eq. (3.40). It can be observed that this structure can be fully described by four different S-parameters, and to characterize this structure two different characterization TEGs are constructed. A general representation for characterization TEGs are given in Fig. 3.53(a).

Leftmost and rightmost cross-lines are connected to GSSG pads with transmission lines.

In one characterization structure (Fig. 3.53(b)) four cross-line are connected in series to each other, and in the other (Fig. 3.53(c)) eight cross-line are connected to each other. Several cross-line structures are connected to each other to decrease possible errors from de-embedding of pads and transmission line fixtures. The series connected device values are selected to easily calculate the virtual-thru connection of fixtures which are not characterized before using L-2L method. Virtual-thru connection of fixtures are illustrated in 3.54. To calculate this fixture response, the measured four-port single-ended response of TEGs are converted to mixed-mode S-parameters.

Since, again, there is no mode conversion, mixed-mode S-parameters of these TEGs can be divided into two separate two-port responses as differential and common modes. From the separated responses, fixture response can be calculated for both modes. T-parameters of the two characterization TEGs can be written for differential mode as follows;

$$[T]_{4U,dd} = [T]_{LP,dd}[T]_{F,dd}[T]^{4}_{C,dd}[T]_{F,dd}[T]_{RP,dd} \tag{3.43}$$

$$[T]_{8U,dd} = [T]_{LP,dd}[T]_{F,dd}[T]^{8}_{C,dd}[T]_{F,dd}[T]_{RP,dd} \tag{3.44}$$

The subscripts LP, RP, F, and C are for left-, right-pad, fixture CPWs, and cross-line. By using the following equation differential response of virtual-thru connection of fixtures can be calculated as;

$$[T]_{PF,dd} = [T]_{4U,dd}[T]^{-1}_{8U,dd}[T]_{4U,dd} \tag{3.45}$$

$$[T]_{PF,dd} = [T]_{LP,dd}[T]_{F,dd}[T]_{F,dd}[T]_{RP,dd} \tag{3.46}$$

where subscript PF is related with left-pad, fixtures and right-pad combinations. One can calculate the common mode of the fixtures with pads responses using the same set of equations (replace “dd” with “cc”). To calculate cross-line one needs to de-embed the pad parasitics and fixture effects. The fixture effects can be solved assuming symmetry property for fixtures after de-embedding pad responses in both pure modes. So that fixture effects are solved by assuming symmetry property after the de-embedding. As a next step, the pad parasitics and fixtures are de-embedded from four repeated characterization TEG. The remaining response is only the four repeated cross-line responses, which can be solved easily since the device is symmetrical. Both modes are solved for one cross-line. In order to verify the characterization results, mixed-mode parameters of cross-line is converted back to single-ended four-port response from mixed-mode S-parameters response. The characterized pad results, fixture responses and cross-line are combined in a simulation environment same with eight repeated characterization TEG. The model

results and measurement results for this structure are compared in Fig. 3.55. The results show well agreement for all S-parameters up to 67 GHz.

3.4.3 Application on a 60GHz Differential Amplifier

In order to check the validity of the characterization of cross-line and pads, a 60GHz differential amplifier is designed and fabricated on 65nm CMOS. Transmission lines, other passives, and transistors are single-ended models. Fig. 3.56 illustrates the chip photo of the amplifier. GSSG input and output pads are used for RF ports of the differential amplifier. GP4G DC pads are used for VDD feed, gate biases of the transistors. The measurements are conducted with four-port VNA (Keysight PNA-X) up to 67GHz.

The simulation and differential measured results are illustrated in Fig. 3.57 up to 67GHz. Red lines present the simulation results. Black lines present the measured differential results. The measured and simulated differential input return loss is presented in Fig. 3.57(a) up to 67GHz. It can be observed that simulation and measured results are close to each other and the matching around 60GHz is close to the center of Smith Chart. Similarly, Fig. 3.57(b) presents the comparison between the simulated and measured differential output port return loss. Again, the measured and simulated results are close to each other. Moreover, matching works fine near the center of the Smith Chart around 60GHz frequency region. Fig. 3.57(c) presents the comparison between simulated and measured differential gain characteristics up to 67GHz. They are very close to each other. One can conclude that the differential de-embedding and passive cross-line characterizations are accurate for differential amplifiers up to 67GHz. The zoomed in version of the gain from 50 to 67GHz is provided in Fig. 3.57(d).

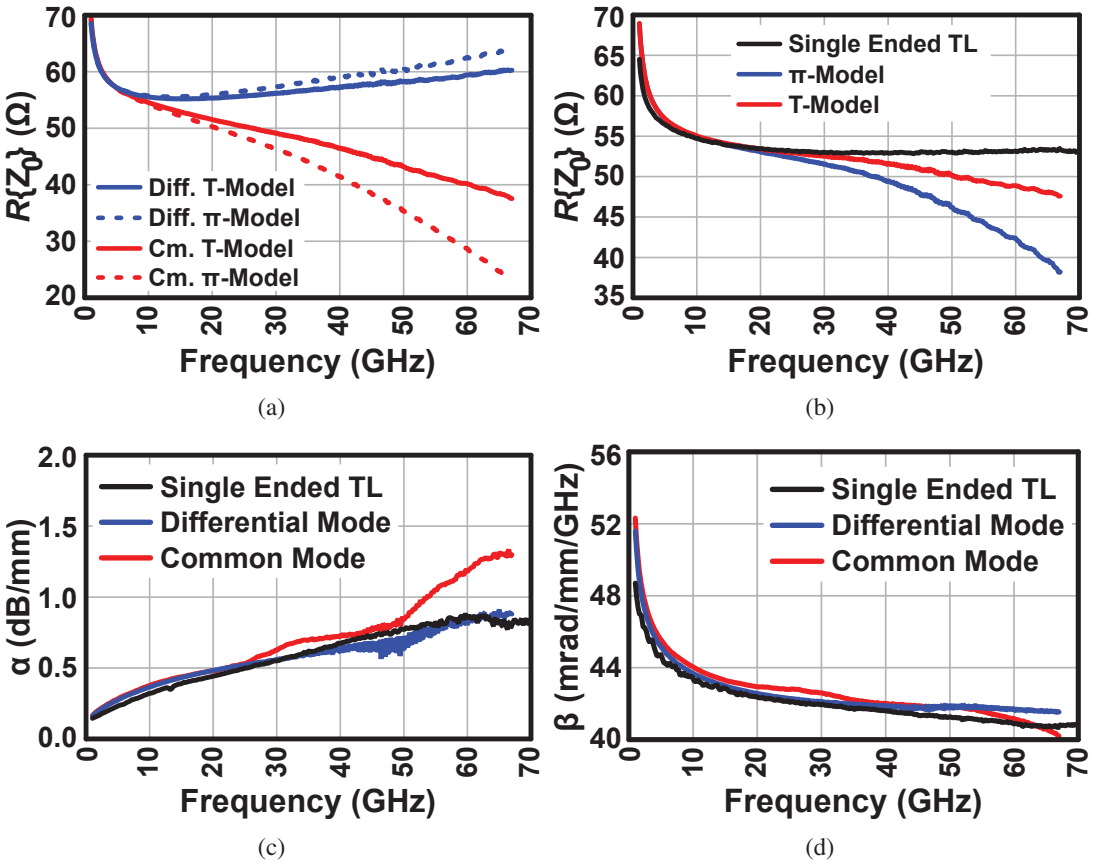
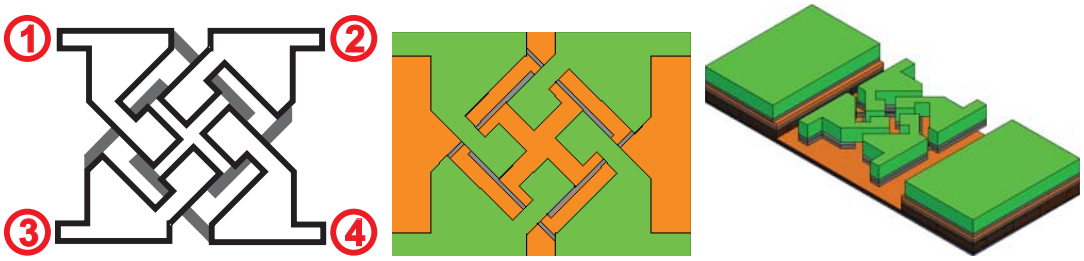
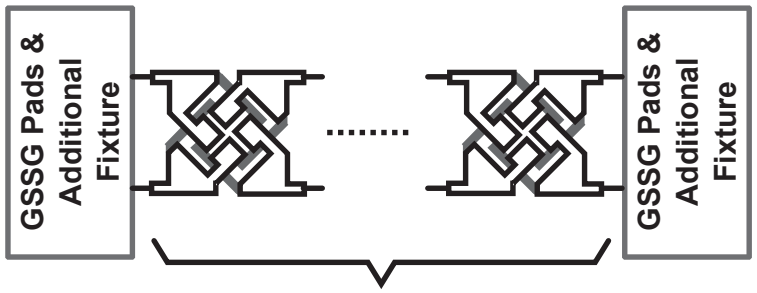


Figure 3.51: Calculated TL characteristics for differential and common mode after de-embedding (a) calculated characteristic impedance for differential mode (blue lines) and common mode (red lines) considering Π-model for pads (dashed lines) and T-model for pads (solid lines), (b) mean characteristic values for both modes considering Π-model (blue line) and T-model (red line) in comparison with two-port transmission line (black line), (c) loss term of differential (blue line) and common mode (red line) in comparison with two-port TL (black line), and (d) propagation constant of differential (blue line) and common mode (red line) in comparison with two-port TL (black line)

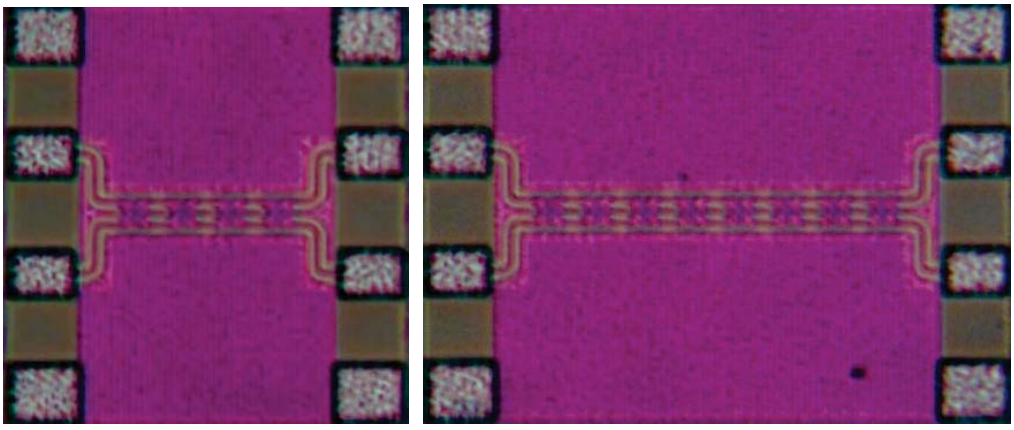


(a) (b) (c)

Figure 3.52: Illustration of symmetrical cross line (a) with port numbering, (b) top view of cross-line (green areas are top metal layer, gray areas are for lower metal layer, and orange areas are for ground connections first two metal layers), and (c) bird-eye-view of the structure.



(a)



(b) (c)

Figure 3.53: Illustration of characterization structures (a) a general representation of characterization TEGs, (b) four repeated cross-line is connected in series and fixture transmission lines with probing pads are added to left and right sides, and (c) eight repeated cross-line characterization structure.

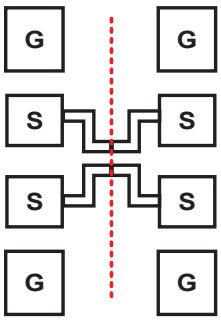


Figure 3.54: Obtained virtual-thru connection of left and right fixtures used in characterization structures.

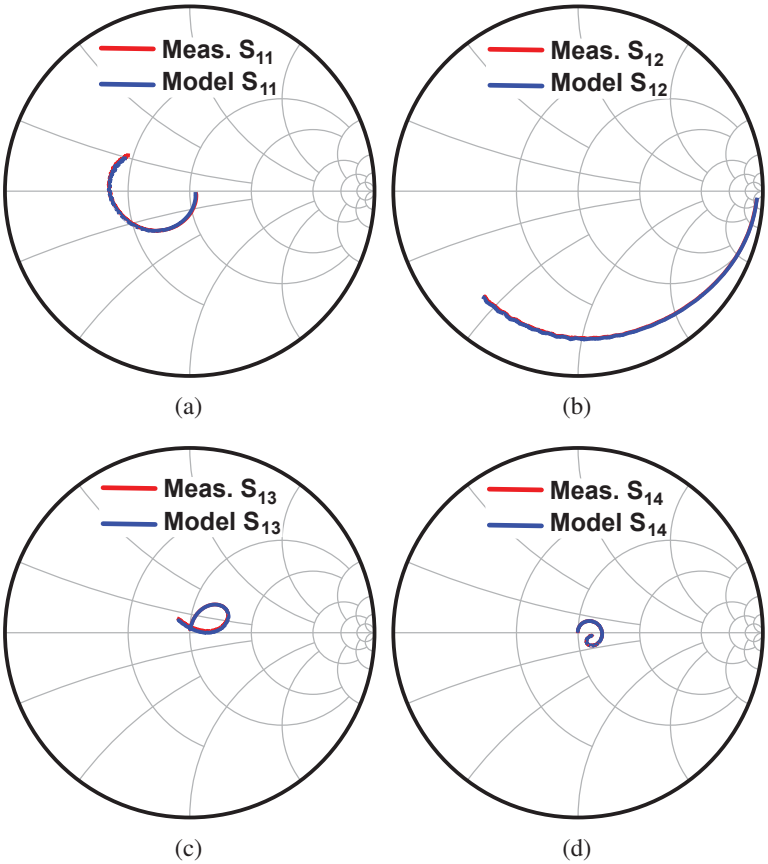


Figure 3.55: S-parameter comparison between model (blue lines) and measurement (red lines) results of eight repeated cross-line up to 67 GHz (a) S_{11}, (b) S_{12}, (c) S_{13}, and (d) S_{14}.

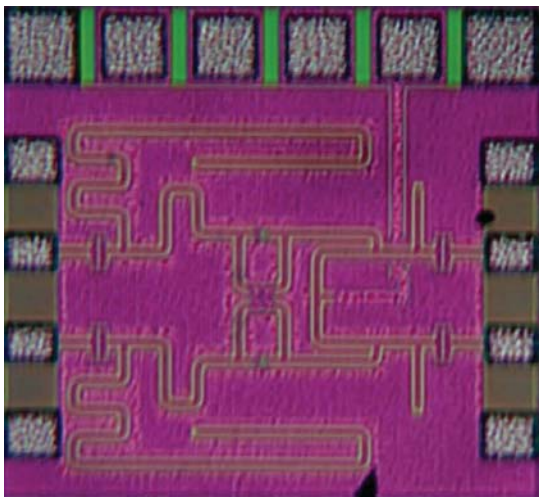


Figure 3.56: A 60GHz differential amplifier chip photo in 65nm standard bulk CMOS.

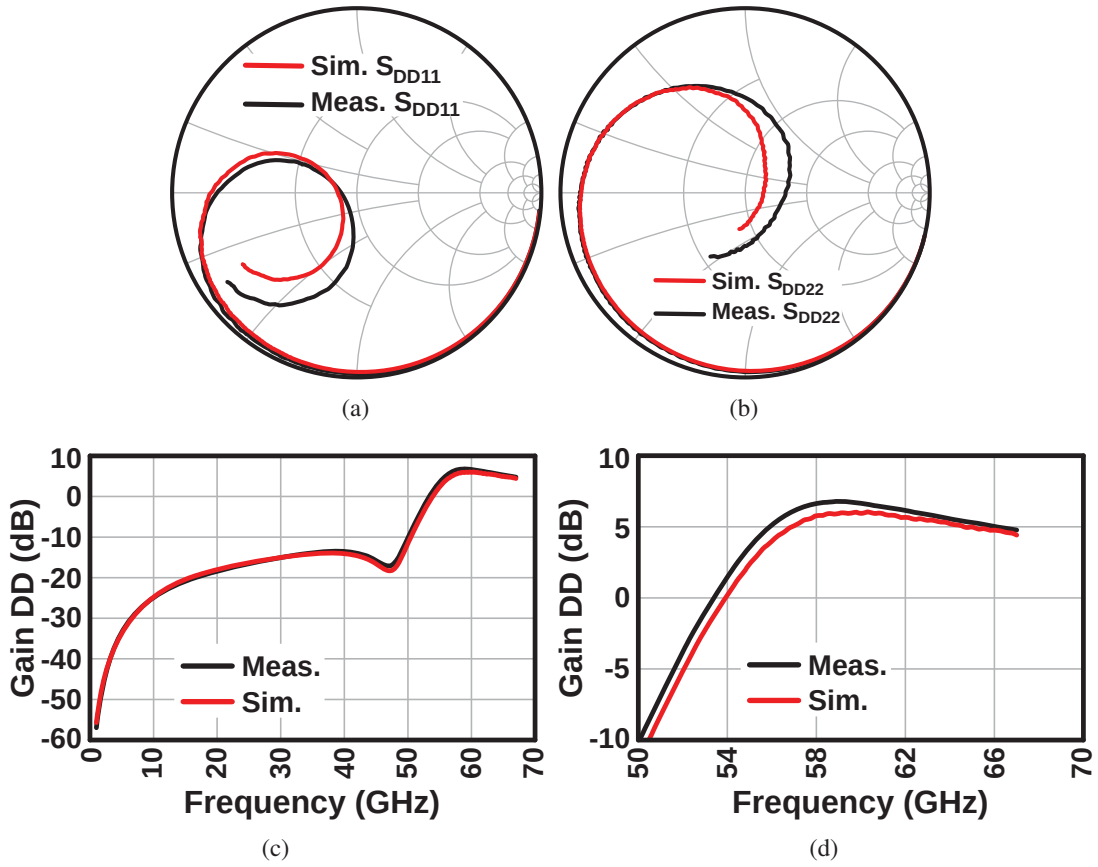


Figure 3.57: S-parameter comparison between model simulation results (red lines) and measurement (black lines) results of a 60GHz differential amplifier (a) differential S_{11} up to 67GHz on Smith Chart, (b) differential S_{22} up to 67GHz on Smith Chart, (c) differential S_{21} (Gain in dB) up to 67GHz, and (d) Zoomed in version of gain from 50 to 67GHz in frequency axis -10 to 10dB in gain axis.

3.5 Multi-Port Passive Device Characterization Approaches Based on Two-Port VNA Measurements

In this section, multi-port devices are characterized using measurement results of a two-port Vector Network Analyzer (VNA) with the multi-port devices terminated using open, short, open-circuited stubs and short-circuited stubs. The open-circuited and short-circuited stubs are terminations with transmission lines (TLs), which are characterized along with Ground-Signal-Ground pads based on L-2L de-embedding method. New characterization methods for two different four-port devices are introduced along with their respective theory. The methods are validated using simulation and/or measurement results. One of the characterized four-port device is the cross-line used in differential capacitive cross-coupled amplifiers, as introduced and characterized differentially in the section above. Two-characterization structures are required for accurate characterization based on theoretical calculations. The other characterized four-port device is a Crossing Transmission Line (CTL), mainly used for over-pass or under-pass of RF signals. A modeling approach based on lumped components is done for this device with two measured two-port characterization structures. Moreove, four measurement results are used to characterize the CTL based on four different characterization structures. The S-parameter response of the CTL is found. To compare the results, reconstructed responses compared with the measurements. Results show good agreement between the measured and modeled results from 1 GHz to 110 GHz. Finally, the importance of this accurater characterization is investigated based on the LO leakage performance of a 60GHz double balanced mixer.

3.5.1 Introduction

One should have well-defined device characteristics and/or models for all of the basic building blocks beforehand, to achieve the desired performance of a TRX, and work thoroughly at mm-Wave frequencies. In a mm-Wave TRX, the basic-building blocks may have two or more than two ports; such as, transmission lines (TLs) as an example of a two-port devices, tee-junctions, transistors, baluns, couplers, cross-line, crossing transmission lines (CTLs) are examples of three- and four-port devices. Moreover, to accurately characterize these devices a manufacturing and measurement cycle should be completed. One of the main issues about this cycle is related to the measurements. De-embedding of unwanted errors to achieve the intrinsic characteristic of the devices is an important procedure [29, 30, 35, 45–48]. For two-port devices, *e.g.* TLs, this procedure is relatively easy compared to three- or four- ports. One can both de-embed

and achieve TL characteristic with two Test Element Groups (TEGs); by using L-2L de-embedding procedure [29, 30, 45]. On the other hand, as mentioned above, the characterization is not that easy for multi-port devices. One can have several choices for modeling or characterization of four-port devices [49–55]. Among them, measuring directly with a four-port Vector Network Analyzer (VNA) with differential or single excitations seems to be the easiest choice. However, there are several issues with this approach. One of which is that multi-port VNAs are commercially available; however, two-port VNAs are, still, the most common instrumentation both in academy and industry. Although differential probing offers good attributes to measurements, one should consider the de-embedding issue, in which several crosstalk and coupling effects are included [46–48]. Hence, the number of TEGs needed for de-embedding is increased, and affects the accuracy of the device characteristics. Decreased dynamic range for multi-port measurements up to mm-Wave frequencies; *e.g.* 110 GHz is another important issue, because the dynamic range is directly related to the measurement accuracy. Typical dynamic range values of two- and four-port measurements up to 67 GHz are around 110 to 120 dB. At relatively higher frequencies, two-port measurements have still good dynamic ranges. Nevertheless, unfortunately, four-port measurement dynamic ranges may decrease to the order of 80 dB [56]. Another way to characterize multi-port devices is using one-, or two-port measurements, of which the previous works are described in the following section.

3.5.2 Previous Works on Multi-Port Device Characterization Techniques

One of the pioneering works [53], on characterization of multi-port devices using one- or two-port measurements suggest using various 2-port combinations of the device to be characterized having unconnected ports to be terminated with different reflective loads unlike matched loads, addressing the issue of mismatch, even a little bit, on system impedance matched loads affecting the accuracy considerably along an ultra-wideband frequency range. In this case, the number of TEGs to be manufactured (excluding the TEGs for load characterization) is given as [53];

$$N(N-1)/2 \tag{3.47}$$

where N is the number of ports of the device to be characterized. For instance, for $N = 4$, *i.e.* device is a four-port device, necessary number of characterization structures can be calculated from Eq. (3.47) as 6.

Because of considerably large number of TEGs and the need for knowledge about

the reflective terminations, many researches tried to find an optimum solution to this problem. In [52], for example, a three-port balun is characterized with one-port measurements from the single-end port of the balun due to the restrictions caused from the coupling effect on measurements related to the differential side. For that reason 7 structures are needed, and knowledge on loads is a must. In [54], a topology that enables to measure all two-port combinations with prior knowledge on just one load is presented. Even though this method is compact and useful for coaxial applications, the use of this approach is not cost effective for CMOS devices, which is necessary to be implemented over and over again for every device. Moreover, considering a possible application on CMOS technology, the accuracy of the measurements might easily be affected by the characteristics of transistors and other interconnects used in the switching matrix. Another approach on this topic is measuring the two-port combinations without terminating the other ports [50, 51]. Considering the non-coaxial application of this method [51], there are several TEGs; one of them is the device to be characterized, three for TRL calibration, and four different virtual loads for optimized S-parameter reconstruction are necessary. For this method to fully reconstruct the S-matrix several data manipulations are to be done, especially to remove the glitches, and to fix the ill-conditioned results caused from high reflections of non-terminated ports. Furthermore this method cannot be used for relatively small devices accurately.

3.5.3 Cross-Line Characterization Based on Two-Port VNA Measurements

Cross-line structure, which is mainly used in differential capacitive cross-coupled amplifiers, are detailed in section 3.4.2. In that section, the cross-line characterization is explained for differential measurements and characterization methods. In here, a method to extend the characterization method up to 110GHz is explained based on two-port VNA measurements. The cross-line structure is shown in Fig. 3.52. Since the cross-line is electrically symmetrical and reciprocal the S-parameters representation have only four different values and presented in Eq. (3.48) in simplified form.

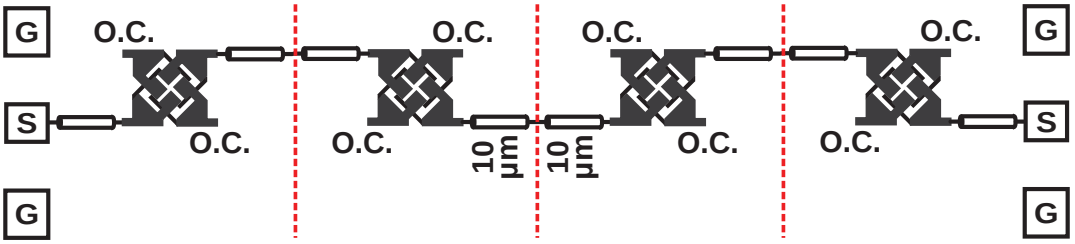
$$S_{\text{Cross-Line}} = \begin{pmatrix} S_{11} & S_{21} & S_{31} & S_{41} \\ S_{21} & S_{11} & S_{41} & S_{31} \\ S_{31} & S_{41} & S_{11} & S_{21} \\ S_{41} & S_{31} & S_{21} & S_{11} \end{pmatrix} \tag{3.48}$$

The number of unknowns from this assumption is four, which are S_{11}, S_{21}, S_{31}, and S_{41}. Two different characterization structures are enough for accurate characterization

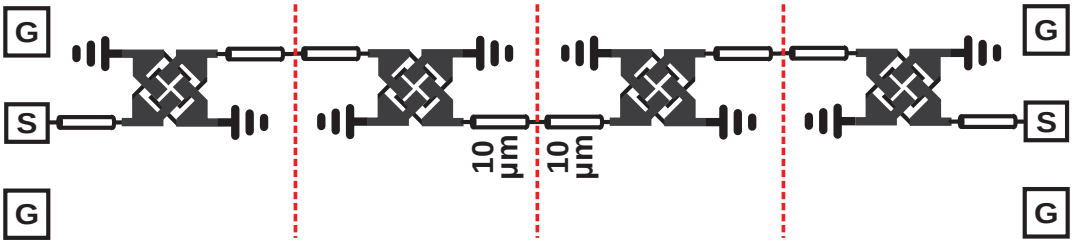
after a careful considerations for two-port measurements. The structures are provided in Fig. 3.58. In both structures cross-line is used four times. Basically, there are two important reasons behind this. The first one is that the pad to pad distance should be around 200μm to avoid cross-talk between probe tips. The other reason is that using several times would decrease possible errors from de-embedding and transmission line modeling which are needed for characterization. Fig. 3.58(a) represents the characterization structure used open circuit as termination for the unused ports of the device. In this TEG, open circuited terminations are used, which are assumed to be perfect open. Since the device is symmetrical and reciprocal and to make the connections easily, in one cross line open circuited terminations is used on ports 3 and 4 and in the other open circuited terminations are used on ports 1 and 2. Finally they are connected to RF pads for measurement purposes. Fig. 3.58(b) represents the characterization structure used short circuit as termination for the unused ports of the device. In this TEG, short circuited terminations are used, which are assumed to be perfect short. Since the device is symmetrical and reciprocal and to make the connections easily, in one cross line open circuited terminations is used on ports 3 and 4 and in the other open circuited terminations are used on ports 1 and 2. Finally they are connected to RF pads for measurement purposes. Note that in the two characterization TEGs there are four cross-line repeated with the same load terminations. As mentioned before, this is required for more accurate characterization of the devices. Fig. 3.58(c) illustrates the characterization TEG manufactured in 65nm standard bulk CMOS fabrication implemented as in Fig. 3.58(a). Similarly, Fig. 3.58(d) illustrates the characterization TEG manufactured in 65nm standard bulk CMOS fabrication implemented as in Fig. 3.58(b). In all characterization TEGs, transmission lines with a length of 10μm are connected to the unterminated ports of the devices. The leftmost and rightmost devices are connected to measurement pads. In both structures, either ports 1 and 4 or 2 and 3 are terminated. Basically, they provide the same resultant S-parameters. This can be proved starting from the following equation [50];

$$[S_{\text{Reduced}}] = [S_{\text{JJ}}] + [S_{\text{JK}}]([\Gamma_{\text{KK}}]^{-1} - [S_{\text{KK}}])^{-1}[S_{\text{KJ}}] \tag{3.49}$$

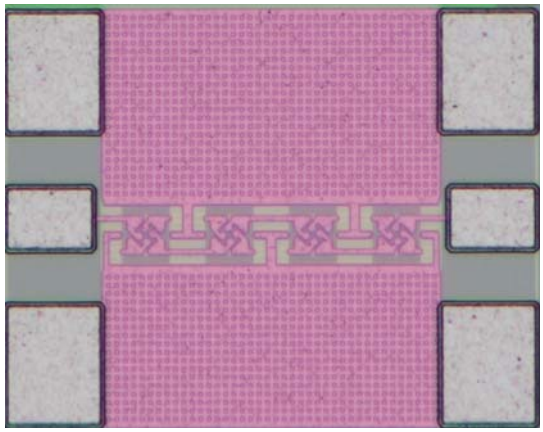
$[S_{\text{Reduced}}]$ is the two-port S-parameter of the terminated four-port device. The subscripts JJ is for the unterminated ports, and KK is for the terminated ports. For instance, when ports 2 and 3 is terminated for the device mentioned here JJ is 1 and 4, and KK is 2 and 3. The subscripts JK and KJ is the related S-parameters between the terminated and unterminated ports of the device. It is mentioned that either termination of ports 1 and 4 or ports 2 and 3 result in the same S-parameters, because in either case



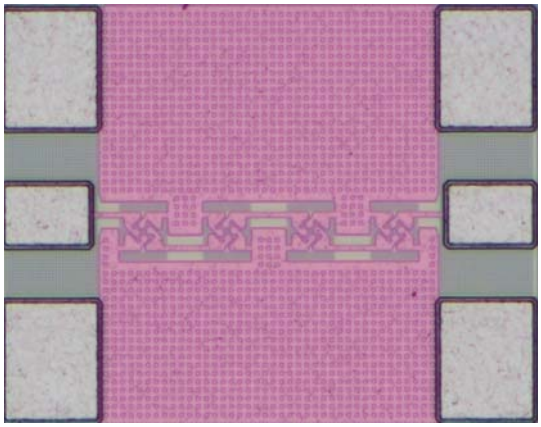
(a)



(b)



(c)



(d)

Figure 3.58: Characterization structures for cross-line in each structure cross-line is repeated four times, and either ports 2 and 3 are terminated or ports 1 and 4 are terminated (a) characterization structure with open circuited (O.C.) terminations used, (b) characterization structure with short circuited terminations used, (c) chip photo of (a), and (d) chip photo of (b).

the related matrices are same as provided below;

$$[S_{JJ}] = [S_{KK}] = \begin{pmatrix} S_{11} & S_{41} \\ S_{41} & S_{11} \end{pmatrix} \tag{3.50}$$

$$[S_{JK}] = [S_{KJ}] = \begin{pmatrix} S_{21} & S_{31} \\ S_{31} & S_{21} \end{pmatrix} \tag{3.51}$$

Moreover, in both case the ports are terminated with same reflections either open circuit or short circuited, for which the related termination matrices ($[\Gamma_{SS}]^{-1}$ is for short circuited and $[\Gamma_{OO}]^{-1}$ is for open circuited terminations) can be given as follows;

$$[\Gamma_{OO}]^{-1} = \begin{pmatrix} 1 & 0 \\ 0 & 1 \end{pmatrix} \tag{3.52}$$

$$[\Gamma_{SS}]^{-1} = \begin{pmatrix} -1 & 0 \\ 0 & -1 \end{pmatrix} \tag{3.53}$$

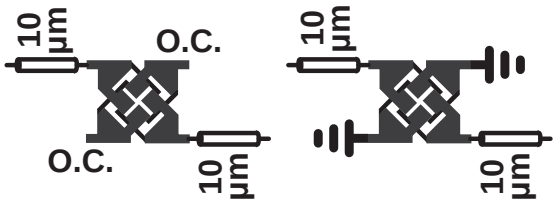
It can be considered that terminating ports 1 and 2, and 3 and 4 would be a similar idea for characterization structure generation and the results can be calculated similarly. It is true however, the values of S-parameters between ports 1 and 2, and 3 and 4 are coupling and they are very small which would result in decreased accuracy. That is why in this work; pairs of ports 1 and 4, and 2 and 3 are selected. Next, the full four-port S-parameters calculations are introduced with the method.

After measuring the two characterization structures (Fig. 3.58(c) and 3.58(d)) with a two-port VNA up to 110GHz, the deembedding of pad responses have to be done. Note that the pads and transmission lines are characterized beforehand of this work. The remaining responses for the measurement results can be given as in the following equations in terms of T-parameters.

$$[T_{MO}] = [T_{LP}][T_{CLO}]^4[T_{RP}] \tag{3.54}$$

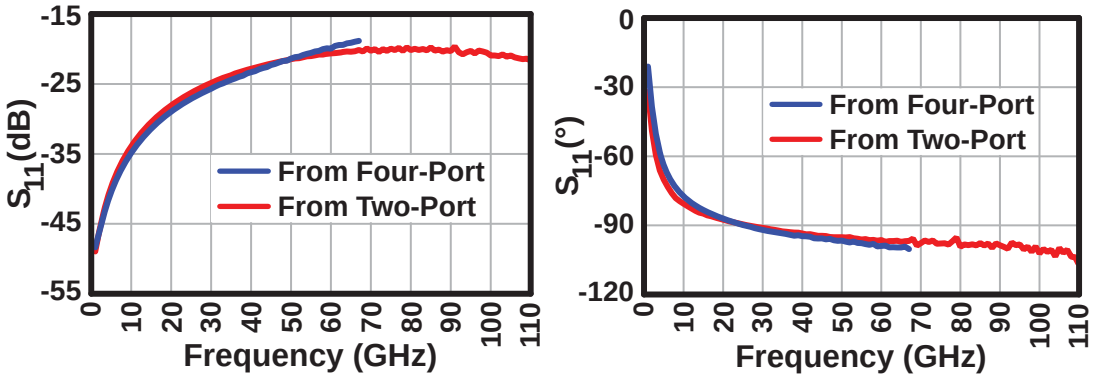
$$[T_{MS}] = [T_{LP}][T_{CLS}]^4[T_{RP}] \tag{3.55}$$

$[T_{MO}]$ is the T-parameters for the measured structure in Fig. 3.58(c) where open circuit is used for terminations. Similarly, $[T_{MS}]$ is the T-parameters for the measured structure in Fig. 3.58(d) where short circuit is used for terminations. $[T_{LP}]$ and $[T_{RP}]$ are the T-parameters for the left and right pads. $[T_{CLO}]$ and $[T_{CLS}]$ are the T-parameters for cross-line open circuited and short circuited, respectively. After the de-embedding the remaining responses are $[T_{CLO}]^4$ and $[T_{CLS}]^4$ 4 which can be easily solved for $[T_{CLO}]$ and $[T_{CLS}]$, the remaining responses are illustrated in Fig. 3.59(a) and 3.58(d) respectively. In order to continue for characterization, the additional transmission lines from both sides for the two cases have to be de-embedded. Only terminated cross-line results remain, which can be represented with S-parameter matrices as S_{CO} and S_{CS}. The S-parameters can be provided in detail using Eq. (3.49) and (3.49) as follows;



(a) (b)

Figure 3.59: Remaining responses after de-embedding and solving for one structure (a) cross-line terminated ports with open circuit, and (b) cross-line terminated ports with short circuit.



(a) (b)

Figure 3.60: Cross-line S-parameter comparison between calculated from four-port measurements (blue lines), and from two-port measurements of the proposed method (red lines), (a)magnitude of (return loss) S_{11}, (b)phase of S_{11}.

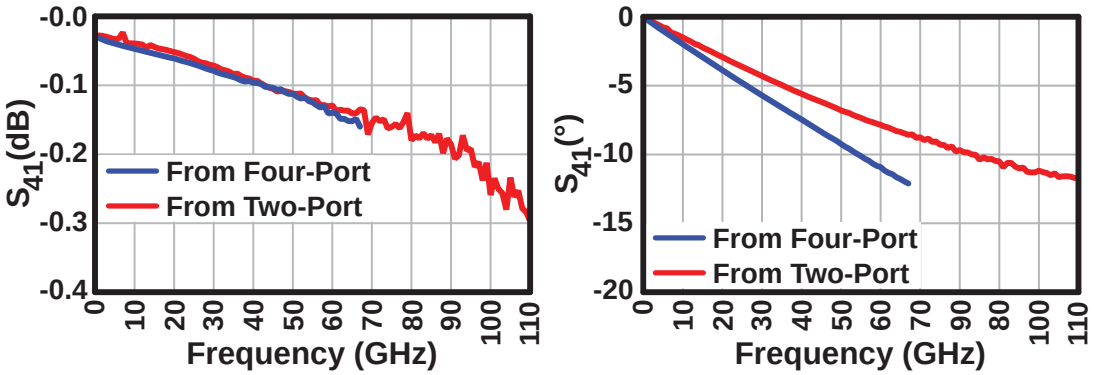
$$S_{CO,11} = S_{11} + \frac{(1 - S_{11})(S_{21}{}^2 + S_{31}{}^2) + 2S_{21}S_{31}S_{41}}{(1 - S_{11})^2 - S_{41}{}^2} \tag{3.56}$$

$$S_{CO,21} = S_{41} + \frac{2S_{21}S_{31}(1 - S_{11}) + S_{41}(S_{21}{}^2 + S_{31}{}^2)}{(1 - S_{11})^2 - S_{41}{}^2} \tag{3.57}$$

$$S_{CS,11} = S_{11} + \frac{-(1 + S_{11})(S_{21}{}^2 + S_{31}{}^2) + 2S_{21}S_{31}S_{41}}{(1 + S_{11})^2 - S_{41}{}^2} \tag{3.58}$$

$$S_{CS,21} = S_{41} + \frac{-2S_{21}S_{31}(1 + S_{11}) + S_{41}(S_{21}{}^2 + S_{31}{}^2)}{(1 + S_{11})^2 - S_{41}{}^2} \tag{3.59}$$

The four unknowns (S_{11}, S_{21}, S_{31}, and S_{41}) of cross-line can be calculated using known values of $S_{CO,11}$, $S_{CO,21}$, $S_{CS,11}$, and $S_{CS,21}$ and using Eqs. (3.56)-(3.59). The equations for unknowns are given below.



(a) (b)

Figure 3.61: Cross-line S-parameter comparison between calculated from four-port measurements (blue lines), and from two-port measurements of the proposed method (red lines), (a)magnitude of (insertion loss) S_{41}, (b)phase of S_{41}.

$$S_{CO,T} = S_{CO,11} + S_{CO,21} \tag{3.60}$$

$$S_{CS,T} = S_{CS,11} + S_{CS,21} \tag{3.61}$$

$$S_{CO,D} = S_{CO,11} - S_{CO,21} \tag{3.62}$$

$$S_{CS,D} = S_{CS,11} - S_{CS,21} \tag{3.63}$$

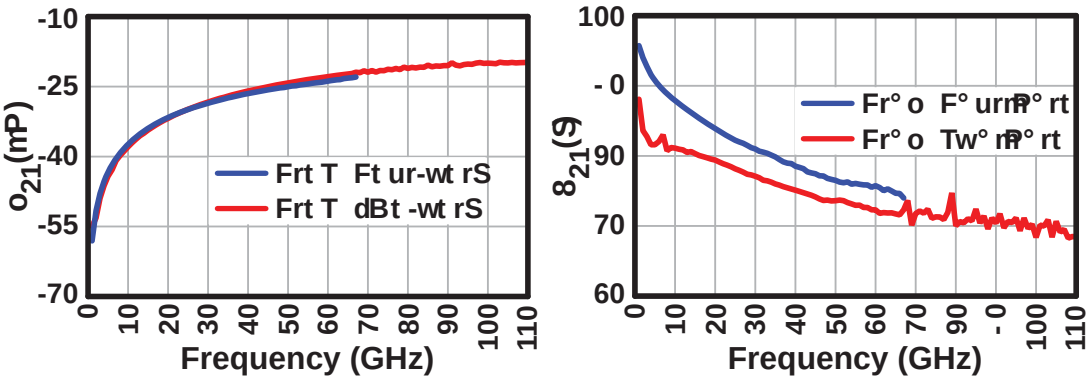
$$C_1 = \frac{S_{CO,T} + S_{CS,T}}{2 + S_{CO,T} - S_{CS,T}} \tag{3.64}$$

$$C_2 = \frac{S_{CO,D} + S_{CS,D}}{2 + S_{CO,D} - S_{CS,D}} \tag{3.65}$$

$$S_{11} = \frac{C_1 + C_2}{2} \tag{3.66}$$

$$S_{41} = \frac{C_1 - C_2}{2} \tag{3.67}$$

$$C_3 = \sqrt{\frac{(S_{CO,T} - S_{CS,T})(1 - C_1{}^2)}{2}} \tag{3.68}$$



(a) (b)

Figure 3.62: Cross-line S-parameter comparison between calculated from four-port measurements (blue lines), and from two-port measurements of the proposed method (red lines), (a)magnitude of S_{21}, (b)phase of S_{21}.

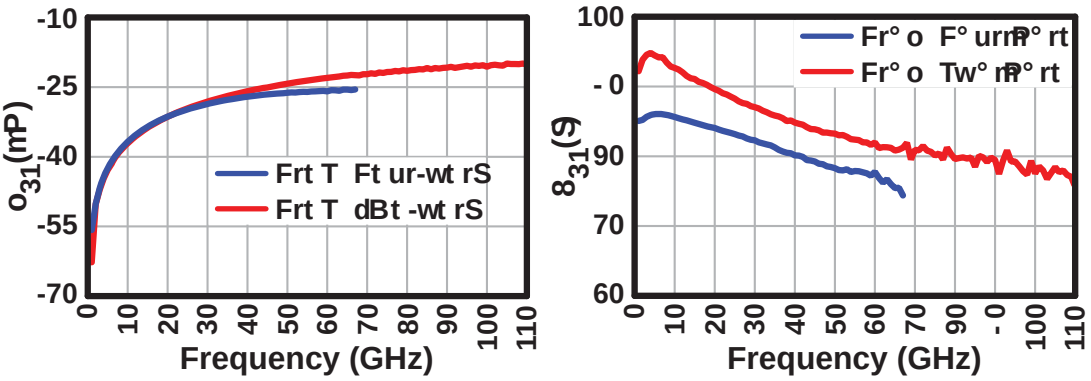
$$C_4 = \sqrt{\frac{(S_{CO,D} - S_{CS,D})(1 - C_2{}^2)}{2}} \tag{3.69}$$

$$S_{21} = \frac{C_3 + C_4}{2} \tag{3.70}$$

$$S_{31} = \frac{C_3 - C_4}{2} \tag{3.71}$$

Using Eqs. (3.60) through (3.71), the four unknown S-parameters of cross-line can be calculated. In the following part the results of this method with a comparison (characterized cross-line based on differential de-embedding and characterization method) are provided.

The method described above is followed and the unknown S-parameters of cross-line is calculated from the two-port measurements. The results are presented in Fig. 3.60(a)-3.63(b) in red lines in comparison with the S-parameters calculated from four-port measurements with the method described in the above section represented with blue lines. The results from two-port measurements are calculated up to 110GHz, while the results calculated from four-port measurements are up to 67GHz since the four-port VNA works up to this frequency. As it can be observed from Fig. 3.60(a) and (b) that the return loss results are very close to each other, except there is some difference after 50GHz both in magnitude and phase. S_{21} magnitude is very close or the two cases, and the phase is different than each other. Similarly, S_{31} magnitude are in good agreement, however there is difference after 40GHz. The phase is also different in the overall



(a) (b)

Figure 3.63: Cross-line S-parameter comparison between calculated from four-port measurements (blue lines), and from two-port measurements of the proposed method (red lines), (a)magnitude of S_{31}, (b)phase of S_{31}.

frequency region. On the other hand, insertion loss, which is S_{41}, well-matched in magnitude, and a little difference in phase domain. The reason of the difference between S_{21} and S_{31} is because of the coupling effects on the four-port measurements. These comparisons shows that the method is accurate. In the next section, another four-port passive characterization is introduced along with its theory with a similar approach.

3.5.4 Crossing Transmission Line (CTL) Characterization Based on Two-Port VNA Measurements

The CTL device previously [55] modeled by using lumped equivalent circuit model. The model is found while optimizing the S-parameter responses of the measured structures and their modeled versions. The model matched well from 20 to 70 GHz. Unfortunately, in other frequency regions the deviation between the measured and modeled versions gets larger. Also for this reason, a full four-port, accurate, and broadband up to 110 GHz characterization of CTL is needed. Moreover, considering the applications after 70 GHz, such as automotive radar, wireless transceivers, and etc. the CTL device should be fully and accurately characterized.

In this section, regarding the above approaches, a new characterization method for CTL, which is a four-port device, (Fig. 3.64) is presented with minimum number of TEGs possible for two port measurements considering CMOS implementation aspects, and compact layout. Four TEGs are used for characterization of CTL.

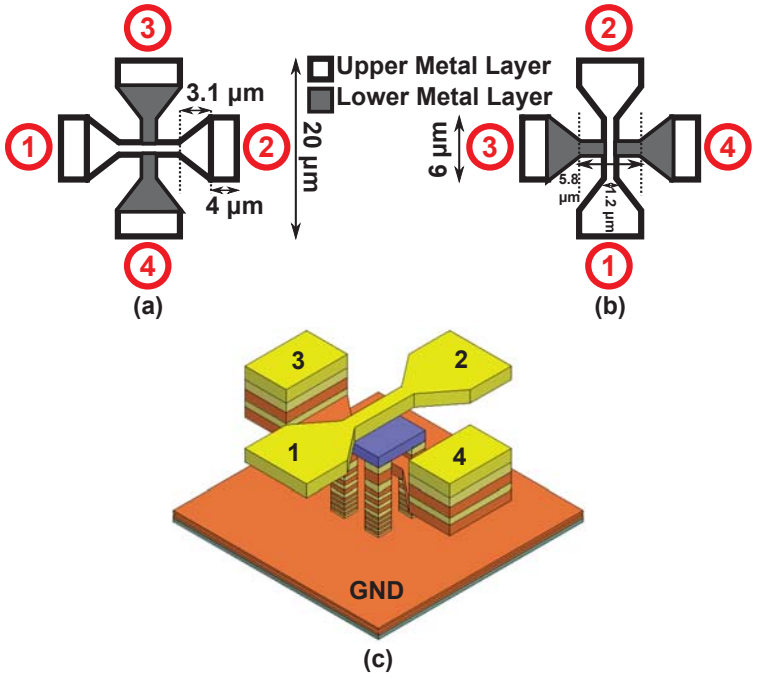


Figure 3.64: Detailed structure of crossing TL, and orientations of (a) upper layer thru connected, (b) lower layer thru connected, and (c) 3-D illustration of the CTL device.

Structure and Topologies of TEGs

The detailed geometrical specification of CTL is given in Fig. 3.64(a), (b) for two different horizontal orientations, in order to construct compact TEGs. Note that the white area represents the top metal, and the gray area represents a lower metal layer. The device has 5 unknowns in representation of S-parameters. This is proven by [57], which uses a full-wave analysis, or it can easily be shown with an EM simulation. The S-matrix of this device is represented as [57];

$$S_{\text{CTL}} = \begin{pmatrix} S_{11} & S_{12} & S_{13} & S_{13} \\ S_{12} & S_{11} & S_{13} & S_{13} \\ S_{13} & S_{13} & S_{33} & S_{34} \\ S_{13} & S_{13} & S_{34} & S_{33} \end{pmatrix} \tag{3.72}$$

Note that S_{13}, S_{14}, S_{23}, S_{24}, S_{31}, S_{32}, S_{41}, and S_{42} are all equal. Thus, only S_{13} is used for simplicity. Each orientation is used for two TEGs; in total four TEGs are used for characterization. As it can be seen from Fig. 3.64, CTL structure is too small for measurements without crosstalk, as probe-to-probe distance should be more than 100µm, at least [29, 45]. Thus, the above mentioned four TEGs are constructed each of which

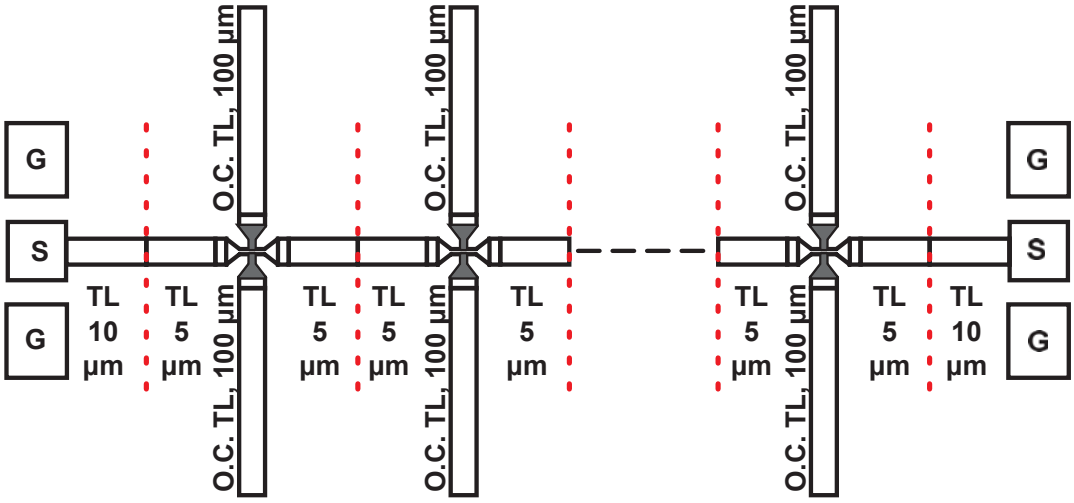


Figure 3.65: An illustration of the manufactured TEG: six of the structures Fig. 3.69(a) are interconnected with 10µm length TLs. Connected to pads with 15µm length TLs.

has six CTLs. Having more than one CTL in one TEG is also helpful to acquire accurate characterization; otherwise, the effect of one would not be enough for accuracy. In [58], coupling between transmission lines for the same CMOS process is studied via EM simulations. It is shown that the coupling between transmission lines closely placed even with a 5µm ground is around -40 dB, which is a negligible value. Even if the six CTL devices are connected directly without transmission lines in between, the effect of coupling between transmission lines, which acts as terminations, would be low enough to be neglected. However, to ensure the safety of characterization, TLs are added between CTLs. It is better to note that, for other processes or other TL configurations, coupling between TLs has to be studied. After that, the length of inter-connection TLs has to be decided. The CTLs are connected to each other with 10µm TLs. The leftmost and rightmost CTLs are connected to pads with 15µm TLs. As a result, TEGs have 200µm length, in total. Illustrations of these TEGs are provided in Fig. 3.65-3.68.

To characterize the CTL with two-port measurements, ports 3 and 4 for Fig.3.64(a), and ports 1 and 2 for Fig. 3.64(b) orientations, terminated with loads as open circuited and short circuited TLs with lengths of 100µm, and 10µm, respectively. For each orientation of CTLs, one open-circuited and one short-circuited TL are used. Fig. 3.69(a)-(d) represent these four variations.

Since L-2L de-embedding method is used for both pad and TL characterization; one does not need additional TEGs for load characterization. Instead scaling of TLs is used, not only for TLs used for terminations but also for TLs used for interconnections between

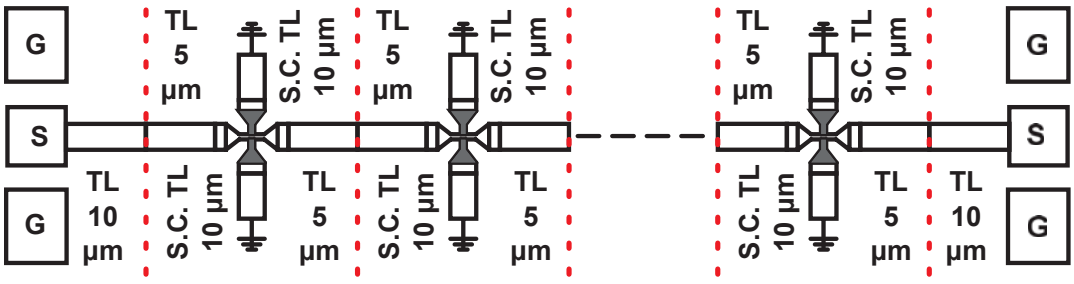


Figure 3.66: An illustration of the manufactured TEG: six of the structures Fig. 3.69(b) are interconnected with 10µm length TLs. Connected to pads with 15µm length TLs.

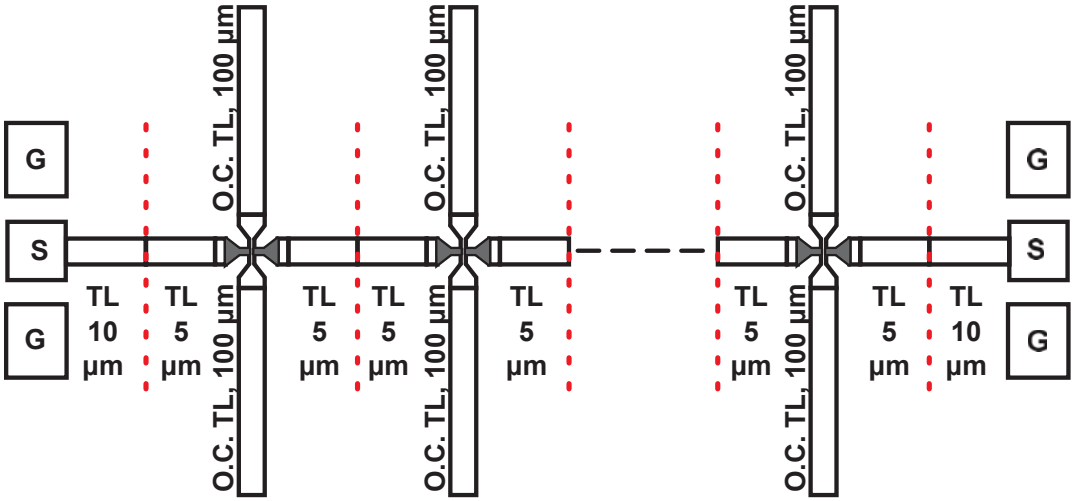


Figure 3.67: An illustration of the manufactured TEG: six of the structures Fig. 3.69(c) are interconnected with 10µm length TLs. Connected to pads with 15µm length TLs.

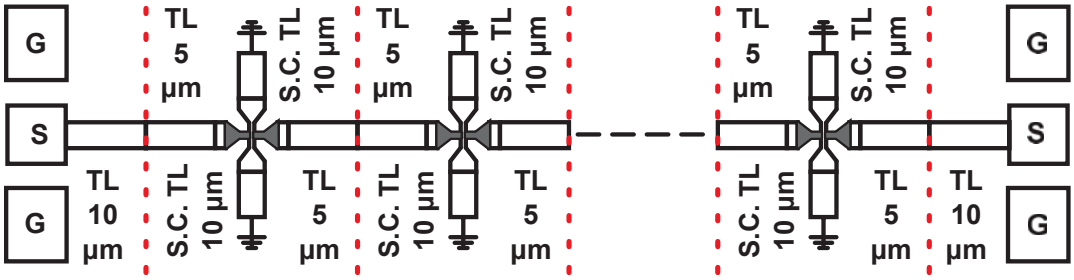


Figure 3.68: An illustration of the manufactured TEG: six of the structures Fig. 3.69(d) are interconnected with 10µm length TLs. Connected to pads with 15µm length TLs.

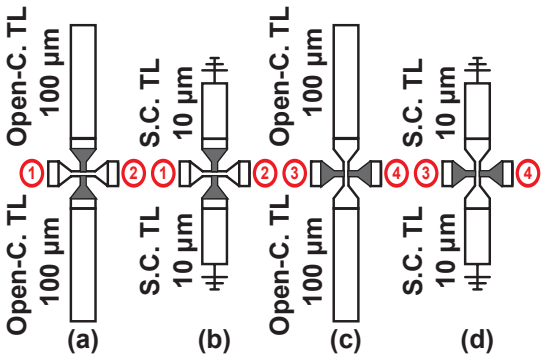


Figure 3.69: Illustrations of terminated CTLs. (a) Orientation Fig. 3.64(a) is connected through, ports 3 and 4 are terminated with open-circuited TLs, (b) orientation Fig. 3.64(a) is connected through, ports 3 and 4 are terminated with short-circuited TLs, (c) orientation Fig. 3.64(b) is connected through, ports 1 and 2 are terminated with open-circuited TLs, (d) orientation Fig. 3.64(b) is connected through, ports 1 and 2 are terminated with short-circuited TLs.

CTLs [33].

Calculation of Terminated CTL Results

Remember that in each TEG, there are six CTLs. In order to obtain the terminated CTL characteristics, several calculation steps are needed. Figures 3.65-3.68 show that the topologies are constructed with six cascaded symmetrical and reciprocal networks. These networks of the four cases can be observed in Fig. 3.70(a)-(d) (Respectively for Fig. 3.65-3.68). The network representation of these structures can be given as;

$$[T_{\mathrm{NT}}] = [T_{\mathrm{L,5\mu m}}][T_{\mathrm{T,CTL}}][T_{\mathrm{L,5\mu m}}] \tag{3.73}$$

where $[T_{\mathrm{NT}}]$ is the network in Fig. 3.70(a)-(d), and $[T_{\mathrm{T,CTL}}]$ is the terminated CTL for four cases in general, which are illustrated in Fig. 3.69(a)-(d).

Moreover, on the leftmost and rightmost sides of these cascaded structures 10µm length TLs are added to achieve a total length of 200µm, and pads are added (Fig. 3.65-3.68). The overall T-parameters representations of the structures in general can be given as;

$$[T_{\mathrm{M,TEG}}] = [T_{\mathrm{lpad}}][T_{\mathrm{L,10\mu m}}][T_{\mathrm{NT}}]^6[T_{\mathrm{L,10\mu m}}][T_{\mathrm{rpad}}] \tag{3.74}$$

Note that $[T_{\mathrm{M,TEG}}]$ is the T-parameters of measured TEGs, in general; and $[T_{\mathrm{NT}}]^6$ is the cascaded T-matrix of the six networks. In order to obtain $[T_{\mathrm{NT}}]^6$ from the measurements,

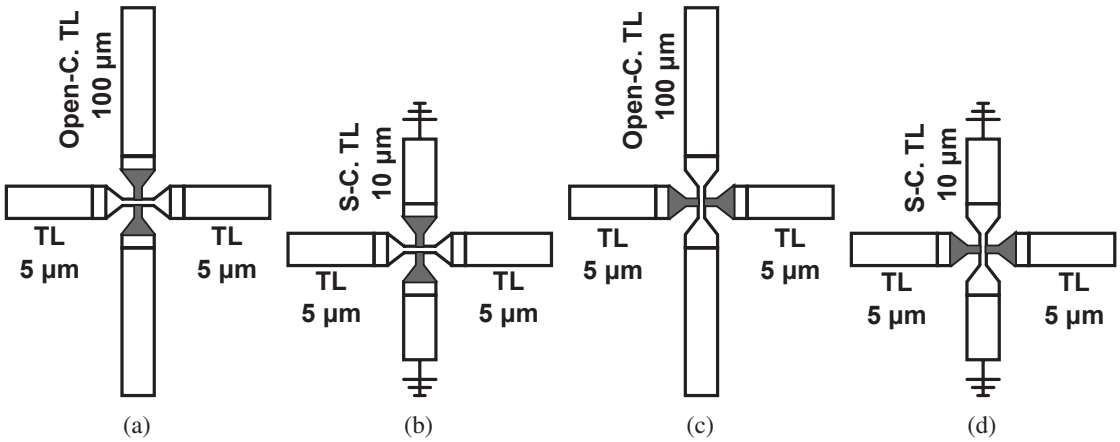


Figure 3.70: An illustration of the symmetrical and reciprocal networks including CTLs (a)-(d), constructed as Fig. 3.69(a)-(d) connected with TLs on the left and right sides.

one must de-embed the pads and additional 10µm length TLs, one can observe the reason in Fig. 3.65-3.68.

$$[T_{\mathrm{NT}}]^6 = [T_{\mathrm{L,10\mu m}}]^{-1}[T_{\mathrm{lpad}}]^{-1}[T_{\mathrm{M,TEG}}][T_{\mathrm{rpad}}]^{-1}[T_{\mathrm{L,10\mu m}}]^{-1} \tag{3.75}$$

Since the cascaded response of six networks is found, one can calculate for one; *i.e.* $[T_{\mathrm{NT}}]$. The calculations for four different structures can be done using the following equation;

$$[T_{\mathrm{NT}}] = \{[T_{\mathrm{NT}}]^6\}^{1/6} \tag{3.76}$$

Please note that this procedure can be done under the assumption of negligible or no coupling between the stages. For that reason, the coupling between the stages is investigated with the help of EM simulations to proceed further in the calculations presented in subsection 3.5.4.

Method for Four-Port CTL Characterization

Remember from Eq. (3.72), there are five unknowns to be found in order to fully characterize the CTL device. For devices having more than two-ports, and measured with two-port VNA; the measured S-parameters can be represented in terms of n-port S-parameters and load reflective characteristics as described in [50];

$$[S_{\mathrm{m}}] = [S_{\mathrm{JJ}}] + [S_{\mathrm{JK}}]([\Gamma_{\mathrm{KK}}]^{-1} - [S_{\mathrm{KK}}])^{-1}[S_{\mathrm{KJ}}] \tag{3.77}$$

where $[S_{\mathrm{m}}]$ is a two-by-two S-parameters matrix of a multi-port device measured with two-port and terminated with loads in the other ports. Note that subscript KK related to terminated ports and JJ is related to the measured ports. Moreover, $[\Gamma_{\mathrm{KK}}]^{-1}$ is a diagonal two-by-two matrix, which is associated with the reflective parameters of loads. In here, the terminated ports are either loaded with open-circuited stubs or short-circuited stubs. The corresponding matrices are presented in Eqs. (3.78), (3.79). $[\Gamma_{\mathrm{S}}]^{-1}$ is the inverse matrix of short-circuited stubs reflective characteristics, and $[\Gamma_{\mathrm{O}}]^{-1}$ is the open-circuited counterpart. For example, considering S-parameters representation of CTL in Eq. (3.72), and assuming that the CTL device is measured from ports 1 and 2 and terminated with loads on ports 3 and 4, $[S_{\mathrm{JJ}}]$, and $[S_{\mathrm{KK}}]$ can be related as in Eqs. (3.80) and (3.81), respectively. For any case $[S_{\mathrm{JK}}]$ is equal to $[S_{\mathrm{KJ}}]$, as it can be seen in Eq. (3.72), and presented in Eq. (3.82). $[S_{\mathrm{JJ}}]$ and $[S_{\mathrm{KK}}]$ changes according to the orientations mentioned in Fig. 3.64(a), (b).

$$[\Gamma_{\mathrm{S}}]^{-1} = \begin{pmatrix} 1/\Gamma_{\mathrm{S}} & 0 \\ 0 & 1/\Gamma_{\mathrm{S}} \end{pmatrix} \tag{3.78}$$

$$[\Gamma_{\mathrm{O}}]^{-1} = \begin{pmatrix} 1/\Gamma_{\mathrm{O}} & 0 \\ 0 & 1/\Gamma_{\mathrm{O}} \end{pmatrix} \tag{3.79}$$

$$[S_{\mathrm{JJ}}] = \begin{pmatrix} S_{11} & S_{12} \\ S_{12} & S_{11} \end{pmatrix} \tag{3.80}$$

$$[S_{\mathrm{KK}}] = \begin{pmatrix} S_{33} & S_{34} \\ S_{34} & S_{33} \end{pmatrix} \tag{3.81}$$

$$[S_{\mathrm{JK}}] = [S_{\mathrm{KJ}}] = \begin{pmatrix} S_{13} & S_{13} \\ S_{13} & S_{13} \end{pmatrix} \tag{3.82}$$

Using Eqs. (3.78)-(3.82), one can have the measured results represented by four-port S-parameters, and known reflections of loads for all measured cases (Fig. 3.69(a)-(d)) as;

$$[S_{\mathrm{m}}^{12,\mathrm{O}}] = \begin{pmatrix} S_{11} & S_{21} \\ S_{21} & S_{11} \end{pmatrix} + \frac{2S_{13}^2}{1/\Gamma_{\mathrm{O}} - S_{33} - S_{43}} \begin{pmatrix} 1 & 1 \\ 1 & 1 \end{pmatrix} \tag{3.83}$$

$$[S_{\mathrm{m}}^{12,\mathrm{S}}] = \begin{pmatrix} S_{11} & S_{21} \\ S_{21} & S_{11} \end{pmatrix} + \frac{2S_{13}^2}{1/\Gamma_{\mathrm{S}} - S_{33} - S_{43}} \begin{pmatrix} 1 & 1 \\ 1 & 1 \end{pmatrix} \tag{3.84}$$

$$[S_{\mathrm{m}}^{34,\mathrm{O}}] = \begin{pmatrix} S_{33} & S_{43} \\ S_{43} & S_{33} \end{pmatrix} + \frac{2S_{13}^2}{1/\Gamma_{\mathrm{O}} - S_{11} - S_{21}} \begin{pmatrix} 1 & 1 \\ 1 & 1 \end{pmatrix} \tag{3.85}$$

$$[S_{\mathrm{m}}^{34,\mathrm{S}}] = \begin{pmatrix} S_{33} & S_{43} \\ S_{43} & S_{33} \end{pmatrix} + \frac{2S_{13}^2}{1/\Gamma_{\mathrm{S}} - S_{11} - S_{21}} \begin{pmatrix} 1 & 1 \\ 1 & 1 \end{pmatrix} \tag{3.86}$$

Note that $[S_{\mathrm{m}}^{12,\mathrm{O}}]$ is obtained CTL result in which ports 3 and 4 are terminated with 100μm open-circuited TLs, $[S_{\mathrm{m}}^{12,\mathrm{S}}]$ is obtained CTL result in which ports 3 and 4 are terminated with 10μm short-circuited TLs, $[S_{\mathrm{m}}^{34,\mathrm{O}}]$ is obtained CTL result in which ports 1 and 2 are terminated with 100μm open-circuited TLs, and lastly $[S_{\mathrm{m}}^{34,\mathrm{S}}]$ is obtained CTL result in which ports 1 and 2 are terminated with 10μm short-circuited TLs. Using these equations all of the unknowns of CTL can be found. For that reason a set of equations are derived. First of all, subtract $S_{\mathrm{m},11}^{12,\mathrm{S}}$ (using Eq. (3.84)) from $S_{\mathrm{m},11}^{12,\mathrm{O}}$ (using Eq. (3.83)) like in Eq. (3.87), and re-arrange like in Eq. (3.88) in which C_1 is a known coefficient calculated by measurement results and load reflection coefficients, given in Eq. (3.89). Similarly, subtract $S_{\mathrm{m},11}^{34,\mathrm{S}}$ (using Eq. (3.86)) from $S_{\mathrm{m},11}^{34,\mathrm{O}}$ (using Eq. (3.85)) like in Eq. (3.90), and re-arrange like in Eq. (3.91) in which C_2 is also a known coefficient given in Eq. (3.92).

$$S_{\mathrm{m},11}^{12,\mathrm{O}} - S_{\mathrm{m},11}^{12,\mathrm{S}} = \frac{2S_{13}^2(1/\Gamma_{\mathrm{S}} - 1/\Gamma_{\mathrm{O}})}{(1/\Gamma_{\mathrm{S}} - S_{33} - S_{43})(1/\Gamma_{\mathrm{O}} - S_{33} - S_{43})} \tag{3.87}$$

$$C_1/\Gamma_{\mathrm{S}} - C_1(S_{33} + S_{43}) = \frac{2S_{13}^2}{1/\Gamma_{\mathrm{O}} - S_{33} - S_{43}} \tag{3.88}$$

$$C_1 = \frac{S_{\mathrm{m},11}^{12,\mathrm{O}} - S_{\mathrm{m},11}^{12,\mathrm{S}}}{1/\Gamma_{\mathrm{S}} - 1/\Gamma_{\mathrm{O}}} \tag{3.89}$$

$$S_{\mathrm{m},11}^{34,\mathrm{O}} - S_{\mathrm{m},11}^{34,\mathrm{S}} = \frac{2S_{13}^2(1/\Gamma_{\mathrm{S}} - 1/\Gamma_{\mathrm{O}})}{(1/\Gamma_{\mathrm{S}} - S_{11} - S_{21})(1/\Gamma_{\mathrm{O}} - S_{11} - S_{21})} \tag{3.90}$$

$$C_2/\Gamma_{\mathrm{S}} - C_2(S_{11} + S_{21}) = \frac{2S_{13}^2}{1/\Gamma_{\mathrm{O}} - S_{11} - S_{21}} \tag{3.91}$$

$$C_2 = \frac{S_{\mathrm{m},11}^{34,\mathrm{O}} - S_{\mathrm{m},11}^{34,\mathrm{S}}}{1/\Gamma_{\mathrm{S}} - 1/\Gamma_{\mathrm{O}}} \tag{3.92}$$

After this step, left hand side of Eq. (3.84) is replaced for its right side in $S_{\mathrm{m},11}^{12,\mathrm{O}}$ (using Eq. (3.87)) as given in Eq. (3.93). In this equation, the number of unknowns decreased from five to three. However, it is not enough for the solution of S_{11}. $S_{33} + S_{43}$ term in this equation is replaced using the summation of $S_{\mathrm{m},11}^{34,\mathrm{O}} + S_{\mathrm{m},21}^{34,\mathrm{O}}$ as in Eq. (3.94), in which the rightmost term is replaced with Eq. (3.91). The resultant equation is arranged for the ease of solution given in Eq. (3.95). Now, the equation has two unknowns, which is easy to solve with the help of Eq. (3.96). Summing the two equations Eqs. (3.95), and (3.96) will

result in one unknown S_{11} term, and known values. Since S_{11} is found one can obtain S_{21} from Eq. (3.96). To achieve S_{33} characteristic, Eq. (3.91), since S_{11} and S_{21} are known already from above description, is subtracted from $S^{34,O}_{m,11}$. Similarly, to obtain S_{43} S-parameter, Eq. (3.91) is subtracted from $S^{34,O}_{m,21}$. The only remaining parameter, now, is S_{13}. This parameter can be calculated from many approaches. To give an example, refer to Eq. (3.97).

$$S^{12,O}_{m,11} = S_{11} + C_1/\Gamma_S - C_1(S_{33} + S_{43}) \tag{3.93}$$

$$S_{33} + S_{43} = S^{34,O}_{m,11} + S^{34,O}_{m,21} - 2\frac{2S^2_{13}}{1/\Gamma_O - S_{11} - S_{21}} \tag{3.94}$$

$$S_{11}\Big(\frac{1}{2C_1C_2} - 1\Big) - S_{21} = S^{12,O}_{m,11}/2C_1C_2 - 1/2C_2\Gamma_S + (S^{34,O}_{m,11} + S^{34,O}_{m,21})/2C_2 - 1/\Gamma_S \tag{3.95}$$

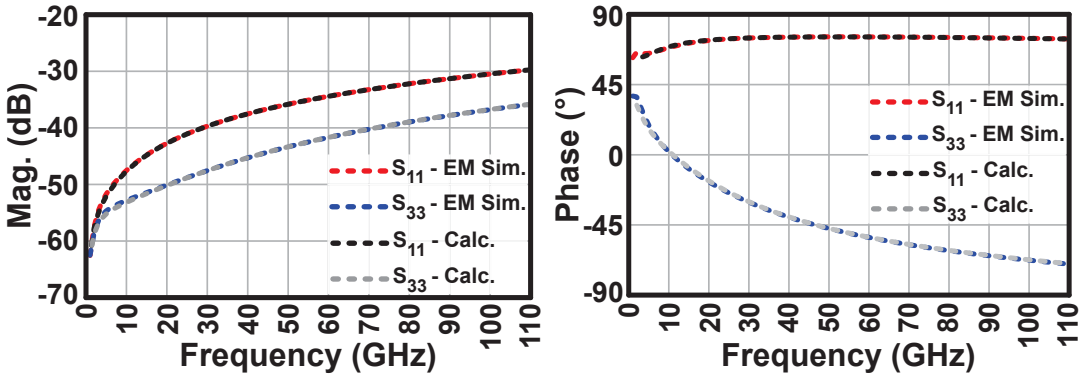
$$-S_{11} + S_{21} = -S^{12,O}_{m,11} + S^{12,O}_{m,21} \tag{3.96}$$

$$S_{13} = \sqrt{\frac{(S^{34,O}_{m,11} - S_{33})(1/\Gamma_O - S_{11} - S_{21})}{2}} \tag{3.97}$$

After this last step, all of unknowns for the four-port device CTL are found, and fully characterized. In the next subsections the characterized S-parameters for CTL are given. Moreover, comparisons between the measured and characterized structure are provided in the following subsections. Before that in the next subsection the method is validated via simulations. For the validation the simulations are used, because direct measurement of CTL device with four-port VNA will not be accurate enough as described in the introduction. Additionally, the impedance of this device is much lower that the other passive devices; such as, TL and pads. Thus the accuracy would be much lower when it is actually measured and it would not be a proper comparison.

Validation Using EM Simulation Results

In order to validate the method, first of all, the CTL device is constructed in an EM simulation environment and simulated. The results of the EM simulation is presented in Fig. 3.71-3.73. Fig. 3.71(a), (b) represents the reflections magnitude and phase, respectively. Fig. 3.72(a), (b) represents the insertion loss and phase, accordingly. Finally, Fig. 3.73(a), (b) illustrates the coupling magnitude and phase. The EM

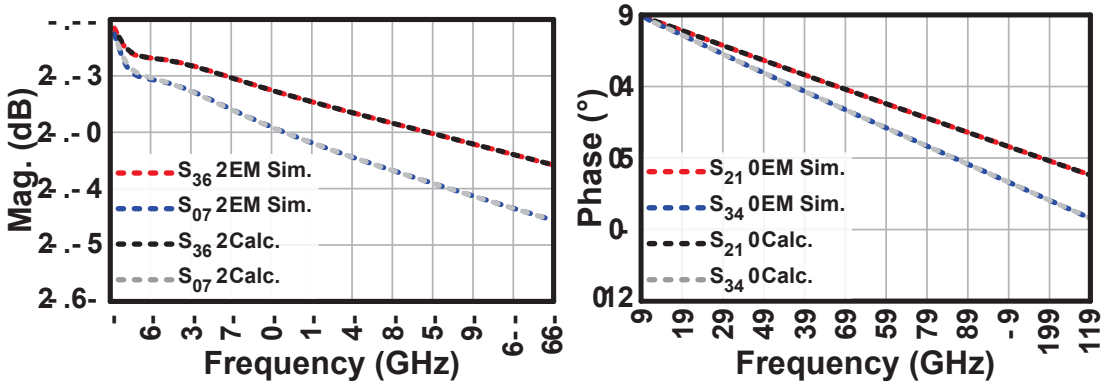


(a) (b)

Figure 3.71: EM simulated and calculated using the method S-parameters of CTL : (a) magnitude (dB) S_{11}, and S_{33}, (b) phase (degree) S_{11}(red and blue lines represents the EM simulation results, and black and gray lines represents the calculated results using the proposed method).

simulation results are illustrated using red and blue lines. Using this EM simulation result and the characterized pad and TL results, the TEGs are constructed in a circuit simulation environment (Keysight ADS) as in Fig. 3.65-3.68. The two-port results of the models constructed with EM simulated CTL are simulated for the four TEGs. Using these two-port results the all procedure described above is followed and S-parameters are calculated. The S-parameter of EM simulated CTL is reconstructed as illustrated in Fig. 3.71-3.73 with black and gray lines. As it can be observed from this figure that there is very little difference between the EM simulation and calculated results of CTL up to 15 GHz. The reason behind this insignificant difference is because of numerical calculation errors, because the values are relatively small. After this frequency the two results are well-matched.

With this phase the method is validated and is applied to real measurement results as presented in the next sub-section. Nevertheless, as it was noted it is important to prove that there is no coupling or negligible coupling to calculate for one terminated CTL device. For that reason, in EM simulator environment, two stages of Fig. 3.70(a) is constructed and simulated, and six stages of the same structure is constructed and simulated. After that two-stage version is series cascaded three times and compared with monolithically simulated six-stages. The results are presented in Fig. 3.74 and 3.75. As one can observe from the graphs that the difference between the two cases are very small, which may be caused from the difference between the convergence conditions of the two simulations. It can be concluded that the coupling between the stages are very low or there is no coupling. Hence the coupling can be neglected and the above calculation procedure for one stage



(a) (b)

Figure 3.72: EM simulated and calculated using the method S-parameters of CTL :(a) magnitude (dB) S_{21}, and S_{43}, (b) phase (degree) S_{21}, and S_{43} (red and blue lines represents the EM simulation results, and black and gray lines represents the calculated results using the proposed method).

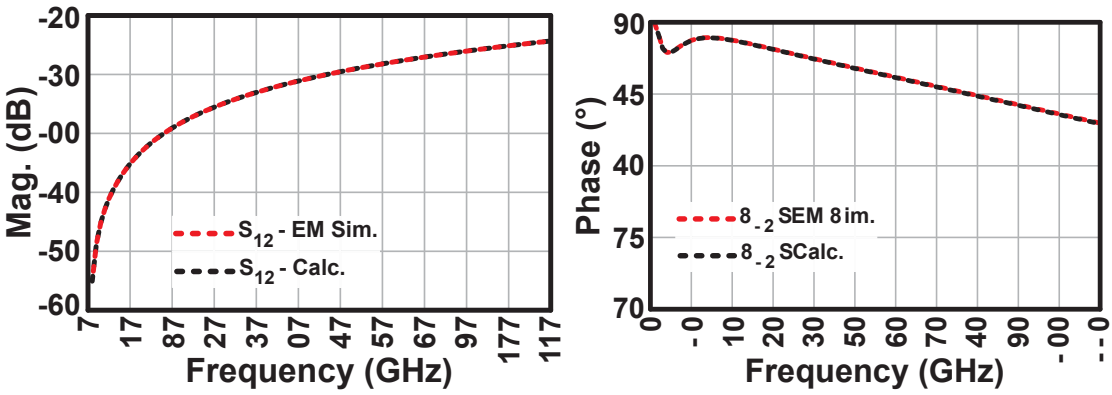
can be used.

Experimental Results Using Measurement Results

The chip micrographs for all four topologies are provided in Fig. 3.76(a)-(d), for the respective illustrations in Fig. 3.65-3.68. These devices are manufactured with 65 nm CMOS process. The measurements are done with two-port VNA. After that, the method presented in the previous section is followed and CTL is characterized as a four-port device. The S-parameter results of CTL are presented in Fig. 3.77 and 3.78, in both magnitude (dB) and phase (degree). One can observe that the insertion loss of the lower metal connection (S_{43}) is higher than the upper metal one (S_{21}), as expected.

One other observation is that the coupling between the upper and lower metal layers are small. It is a desirable result for underpass and overpass applications. This also is expected since the overlapping area is 1.2-by-1.2μm^2, and the lines are orthogonal to each other.

Reconstructions of the TEG topologies in terms of calculations are done and they are compared with the actual measurement results. The reconstruction can be done with calculations using the above-presented equations, or it can also be done in a circuit simulator environment (*e.g.* Keysight ADS). The comparison of characterized results and the measurement results are presented in Fig. 3.79-3.86, respective for Fig. 3.65-3.68, in terms of return losses and insertion losses, in magnitudes (dB) and phases (degree). As it can be observed from these figures, the modeled results and the measured



(a) (b)

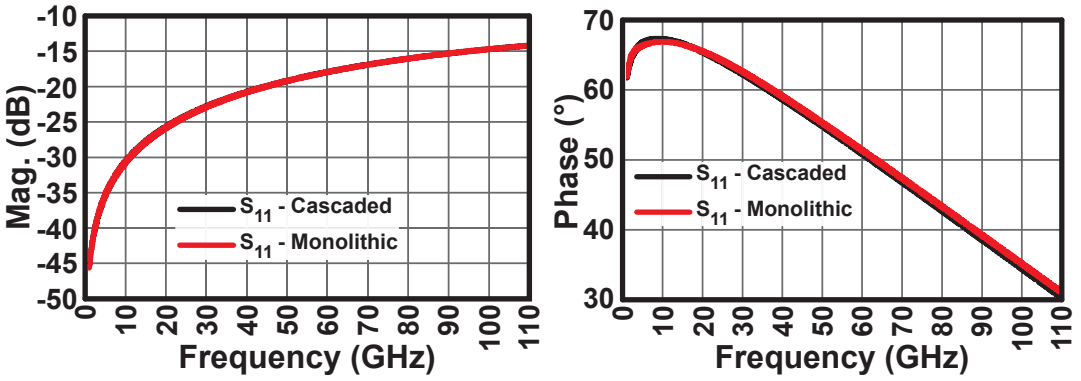
Figure 3.73: EM simulated and calculated using the method S-parameters of CTL :(a) magnitude (dB) S_{13}, and (b) phase (degree) S_{13} (red and blue lines represents the EM simulation results, and black and gray lines represents the calculated results using the proposed method).

results matches perfectly starting from 1 to 110GHz, for all of the cases, as expected.

3.5.5 Crossing Transmission Line (CTL) Modeling Based on Two-Port VNA Measurements

In this subsection, a method to model the CTL with lumped components is introduced. Two of the above subsection introduced characterization structures are used for modeling of the CTL. The other two are used for verification. The geometrical details of CTL is given in Fig. 3.64 with port numbering. The structures used in this modeling approach are Fig. 3.65 and 3.67. In these structures, again, two orientations of CTL are used and the unconnected ports of the CTLs are terminated with 100μm open-circuited transmission lines. The modeling and verification flow is illustrated in Fig. 3.87. For the model construction, two measurement results are used at the same time from two different TEGs which are CTL orientation in Fig. 3.64(a) with ports 3 and 4 are terminated with 100μm length open-circuited TLs, and in the other, CTL orientation in Fig. 3.64(b) with ports 1 and 2 are terminated with 100μm length open-circuited TLs, shown in Fig. 3.87(a), and (b), respectively. The transmission lines used in the model extraction and pad parasitics model are characterized beforehand as explained in this chapter. For validation, measurements of TEGs, in which open-circuited TLs are replaced with short-circuited 10μm length TLs, shown in Fig. 3.87(c), and (d), are compared with the extracted model.

Fig. 3.88 represents the lumped equivalent model of crossings. Note that subscripts



(a) (b)

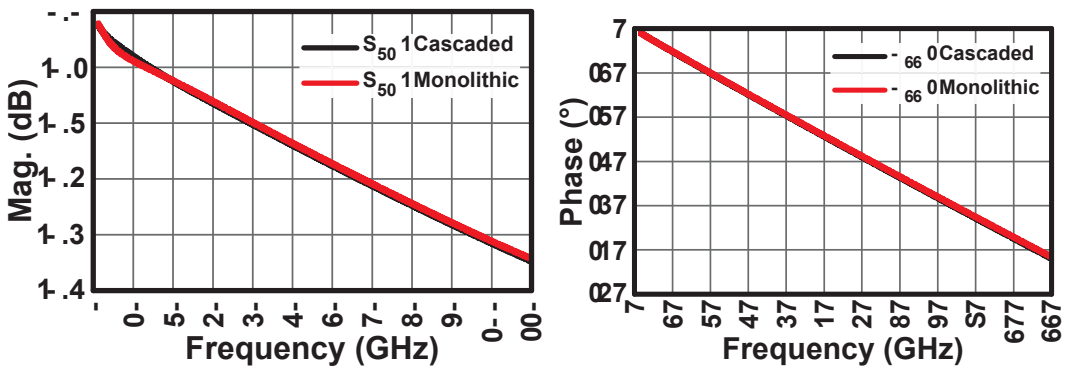
Figure 3.74: S-Parameter comparison between monolithically EM simulated six-stage of Fig. 3.70(a)(red lines) and three times cascaded of EM simulated two-stage of Fig. 3.71(a)(black lines):(a)magnitude (dB) S_{11}, (b)phase (degree) S_{11}.

Table 3.1: Optimized lumped component values for CTL.

L_{UP}	2.86pH	L_{LW}	2.13pH	C_1	2.05fF
R_{UP}	0.18Ω	R_{LW}	0.27Ω	C_2	0.05fF
C_{UP}	105fF	C_{LW}	175fF	C_{COUP}	1.64fF

UP is for the upper layer lumped components, and LW is for the lower layer lumped components. Although the dimensions of CTL are small, one should not neglect the parasitic shunt capacitances to ground, and hence C_1 and C_2 are added for upper and lower layers, accordingly. Moreover, C_{COUP} models for the capacitive coupling between the crossing TLs. Using this model the values of the lumped components are optimized using the measurement results of Fig. 3.65, 3.67; and the results are given in Table 3.1. The same lumped model is used for every CTL, and the connections with transmission lines are done in the simulation environment. As mentioned above, the transmission lines and pads used in this structure are modeled beforehand accurately up to 110GHz. These models are used in the simulation environment and based on the two measurement results the lumped component values are optimized to match the simulated S-parameters with the measured S-parameters as close as possible.

The modeled CTL S-parameters responses along with comparisons of the characterized structure are provided in Fig. 3.89 and 3.90. The characterized results are presented with solid lines and the modeled CTL S-parameters results are presented in dashed lines. Fig. 3.89(a) presents the magnitude of return loss of S_{11}, return loss of S_{33}, and coupling of S_{13}. It can be observed that the model results and characterized results show difference. These differences seems to be large, however, note that the magnitude



(a) (b)

Figure 3.75: S-Parameter comparison between monolithically EM simulated six-stage of Fig. 3.70(a)(red lines) and three times cascaded of EM simulated two-stage of Fig. 3.71(a)(black lines):(a)magnitude (dB) S_{21}, and (b)phase (degree) S_{21}.

values are already very small. Hence, in number these differences are not so large. Fig. 3.89(b) shows the phase comparison of these S-parameters. Phase of the coupling is close for the model and characterized versions. The behavior of the phase of S_{33} is similar for the two cases. The phase of S_{11} are very close after 70GHz up to 110GHz for the modeled and the characterized cases. Unfortunately, the difference is large before 70GHz when going down to the low frequency regions.

Fig. 3.90(a) presents the magnitude of insertion loss of S_{21}, and insertion loss of S_{43}. It can be clearly observed that the starting value of the insertion loss and up to 110GHz there are differences between the modeled and characterized versions. Again, in these figures, the solid lines are the characterized results and the dashed lines are the modeled versions. Although, up to 70GHz the behavior of the insertion losses follow each other for the modeled version and the characterized version, the difference gets largers as the frequency increases up to 110GHz. Fig. 3.90(b) presents the phase of insertion loss of S_{21}, and insertion loss of S_{43}. The two cases are close to each other. However, yet again, after 70GHz region the differences between the model and characterized versions increase slowly. Considering these S-parameters comparisons of CTL between the model and characterized version, one can say that accurate ultra-broadband lumped model even for a small device is not an easy task.

Using the extracted lumped model of the CTL, transmission lines and pad parasitics, in simulation environment the measured structures are reconstructed based on cascaded networks. Next the comparison between the measurements and model based results of the TEGs are given. First the comparison results for the TEGs used for model extraction are going to be provided. The measurement results of the structures in Fig. 3.88(a) and

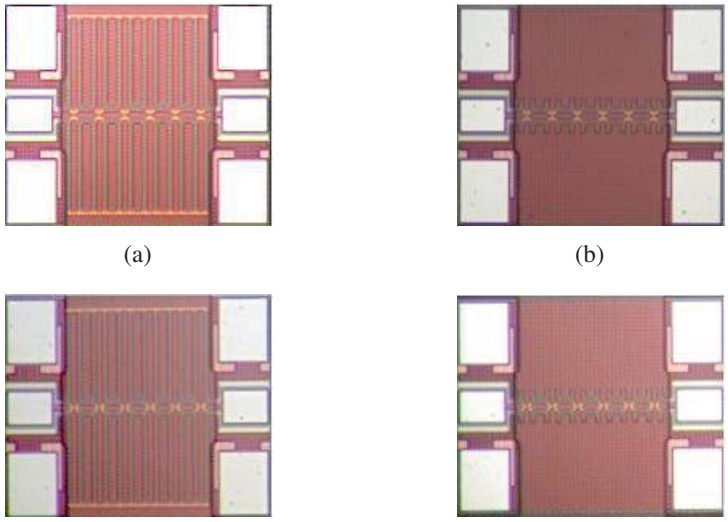
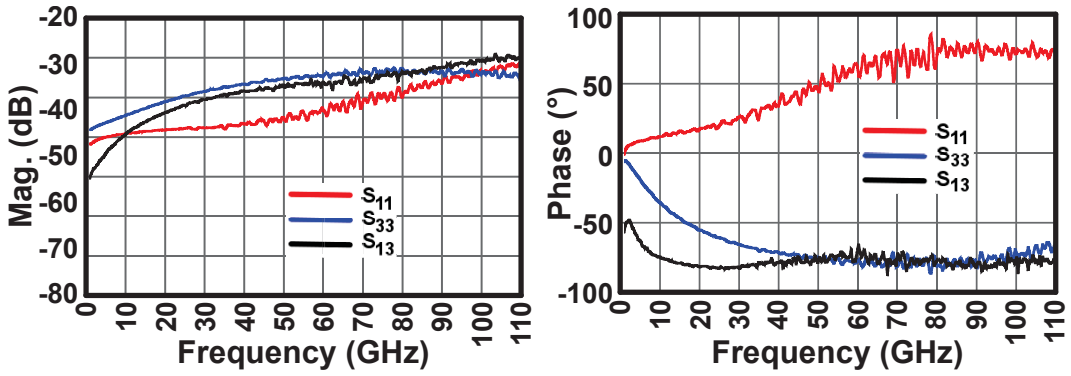


Figure 3.76: Chip micrograph (a)-(d), respectively for Fig. 3.65-3.68.

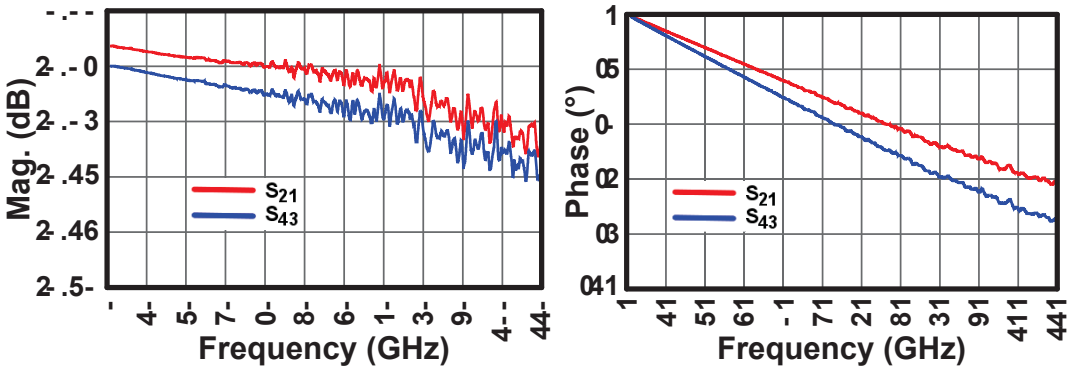
(b) are compared with the reconstructed model results. Fig. 3.91(a) shows the comparison of reconstructed model based simulation results and the measurement results of the two orientations for CTL, like in Fig. 3.88(a), and (b). Red line represents the measurement results of (a), whereas the blue line represents the model based reconstructed return loss in magnitude. Similarly, green line shows the measurement results of orientation (b) and the purple line shows the model based reconstructed return loss in magnitude. Results are well matched between 10 to around 80GHz frequency region. However, there are deviations up to 10GHz and after 80GHz. These differences are caused of the difficulty to achieve ultra-broadband model with lumped components. Fig. 3.91(b) illustrates the comparison of the phase of return losses for the two TEGs mentioned above. In the case of phase responses the difference starts from around 90GHz. Fig. 3.92(a) shows the comparison of insertion loss between the reconstructed model S-parameters and measurement results of the two TEGs. For orientation (a) there is difference after 80GHz whereas for orientation (b) model and measurement well matches. For both cases, there is difference from DC to 10GHz which cannot be avoided as the lumped model cannot represent ultra-broadband. Fig. 3.92(b) illustrates the phase comparison of the insertion losses. There is no significant difference.

In order to verify the models, another two TEGs are used for verification. Fig. 3.88(c) and (d) are used for this case. The terminations used in the TEGs are short-circuited transmission lines with a length of 10μm. Again, the two orientations of CTL are used



(a) (b)

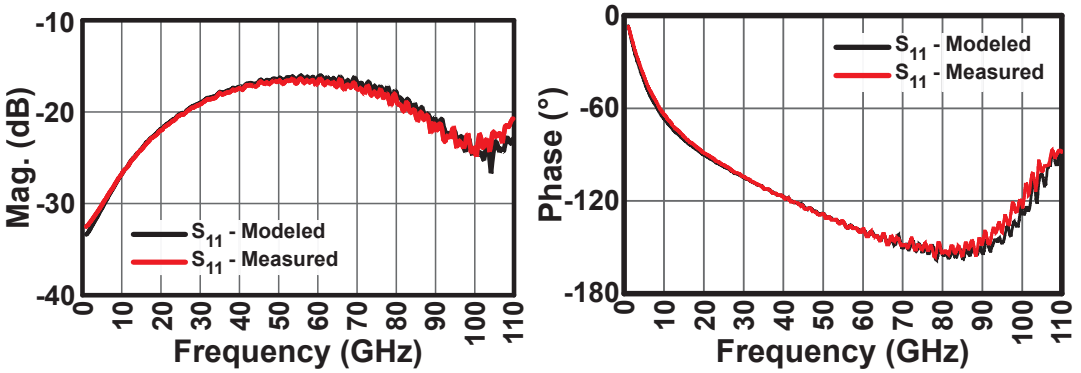
Figure 3.77: Characterized S-parameters of CTL: (a)magnitude (dB) S_{11}, S_{13}, and S_{33}, (b)phase (degree) S_{11}, S_{13}, and S_{33}



(a) (b)

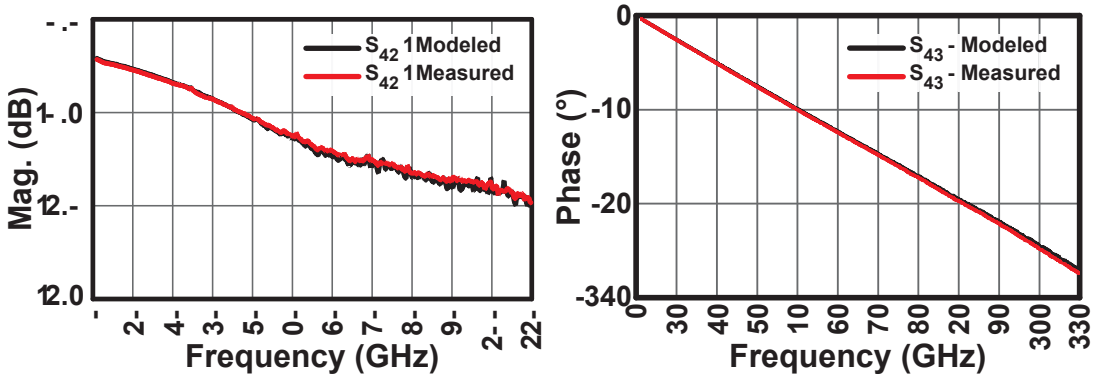
Figure 3.78: Characterized S-parameters of CTL:(a)magnitude (dB) S_{21}, and S_{43}, (b)phase (degree) S_{21}, and S_{43}.

for the two TEGs. The TEGs are measured with a VNA up to 110GHz. Fig. 3.93(a) represents the comparison of the return losses for the verification TEGs. The red line represents the measured return loss magnitude in dB for TEG in Fig. Fig. 3.88(c) and blue line represents the modeled version of the same TEG. The model and measured results have mismatch after 80GHz and up to around 10GHz from DC. The green line represents the measured return loss magnitude in dB for TEG in Fig. Fig. 3.88(d) and purple line represents the modeled version of the same TEG. The measured results and model well matched. Fig. 3.93(b) represents the comparison of the return losses phase for the verification TEGs. There are differences after 90GHz. Other regions are well matched. Note that color code is same as before. Fig. 3.94(a) represents the comparison of the insertion losses magnitude for the verification TEGs. For both cases, there is mismatch



(a) (b)

Figure 3.79: Comparison between measurements and characterized of Fig. 3.65: (a)magnitude of S_{11} in dB, (b)phase of S_{11} in degrees.



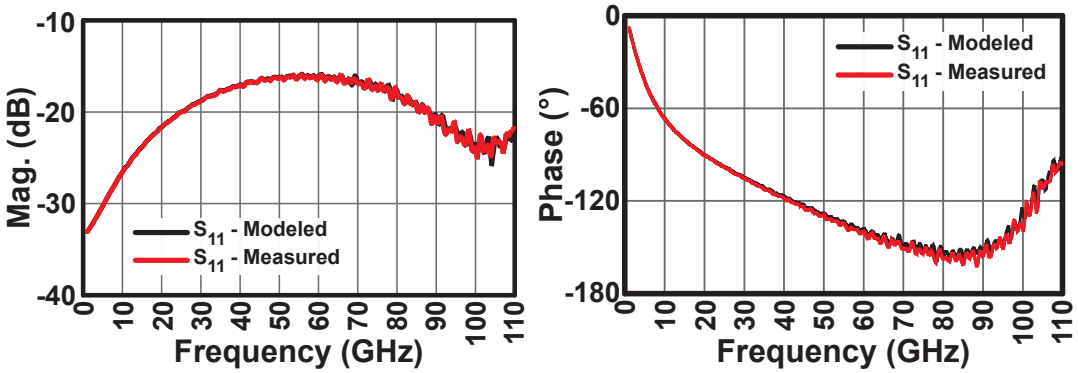
(a) (b)

Figure 3.80: Comparison between measurements and characterized of Fig. 3.65:(a) magnitude of S_{21} in dB, and (b) phase S_{21} in degrees.

from DC to 10GHz. For the TEG in Fig. 3.88(d) other regions are well matched. For the other TEG, there is mismatch after 80GHz. Fig. 3.94(b) represents the comparison of the insertion losses phase for the verification TEGs. Results are well matched.

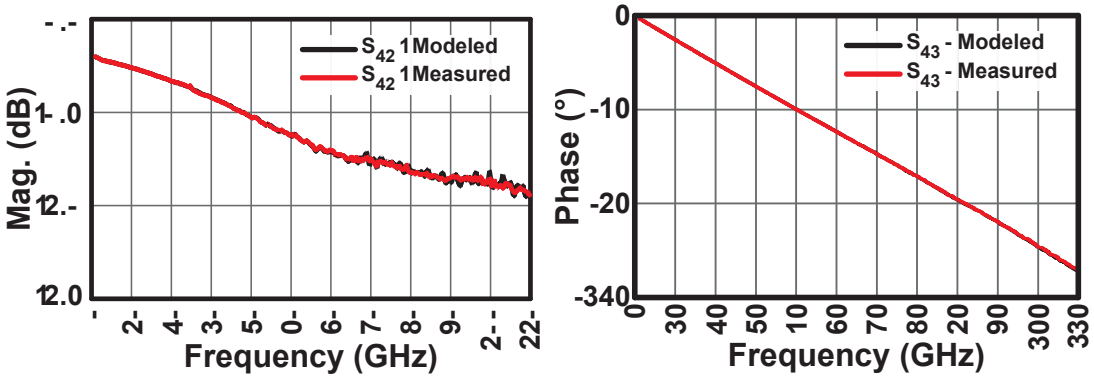
3.5.6 Crossing Transmission Line (CTL) Application on Millimeter-Wave Mixer

In order to observe the effect of CTL with full characterization on circuit performance, a passive balanced mixer is studied via simulations. The mixer considering layout aspects is illustrated in Fig. 3.95. The transistors have 60nm of gate length and gate width of 2μm by 10 fingers. The TLs are placed considering the layout aspects,



(a) (b)

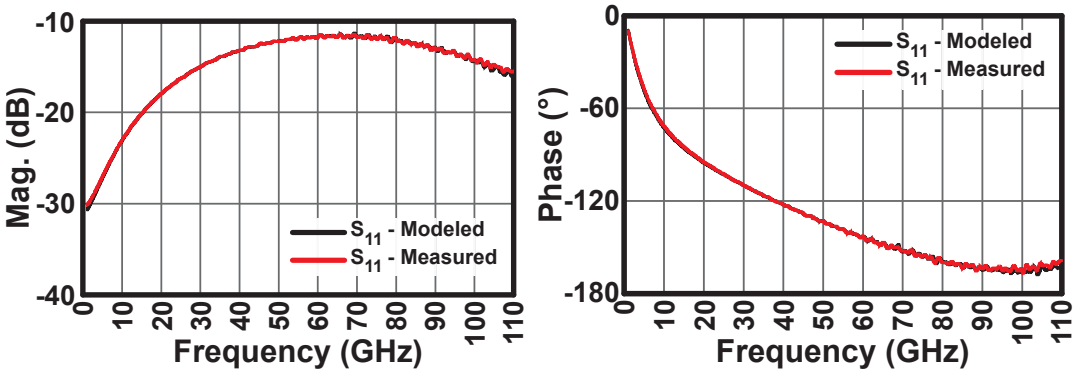
Figure 3.81: Comparison between measurements and characterized of Fig. 3.66:(a)magnitude of S_{11} in dB, (b)phase of S_{11} in degrees.



(a) (b)

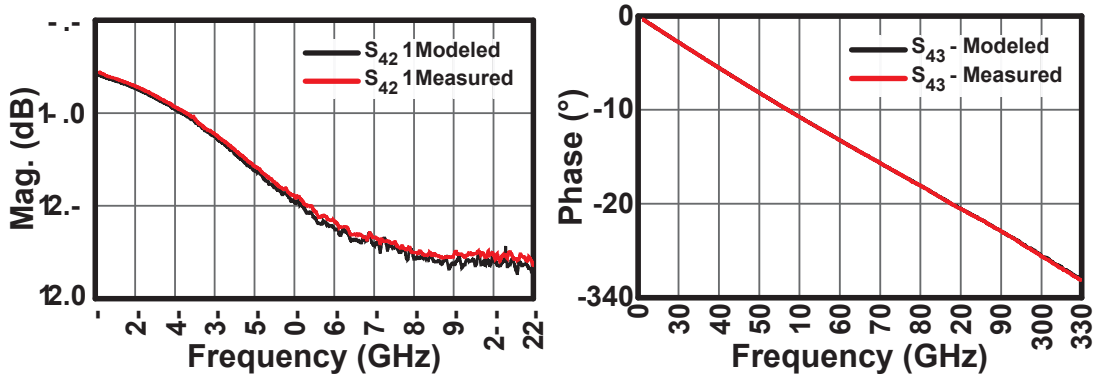
Figure 3.82: Comparison between measurements and characterized of Fig. 3.66:(a)magnitude of S_{21} in dB, (b)phase S_{21} in degrees.

routing, and matching purposes. As described in introduction part, even slight differences on device characteristics may cause, for example the LO leakage to behave differently. For this reason, LO leakage is simulated for three cases as; circuit without CTLs, circuit with EM simulated, and calculated CTL response. The results are presented in Fig. 3.96. One can observe that the difference between the mixer with CTLs and without CTLs are very large. Also, there is 5 to 9dB difference between the calculated and EM simulated CTL responses from 40 GHz to 70 GHz LO frequency. The modeled and characterized ones are close to each other. However, as the frequency increases the difference between the two increases. This is because the lumped component based model cannot represent full band coverage.



(a) (b)

Figure 3.83: Comparison between measurements and characterized of Fig. 3.67:(a)magnitude of S_{11} in dB, (b)phase of S_{11} in degrees.

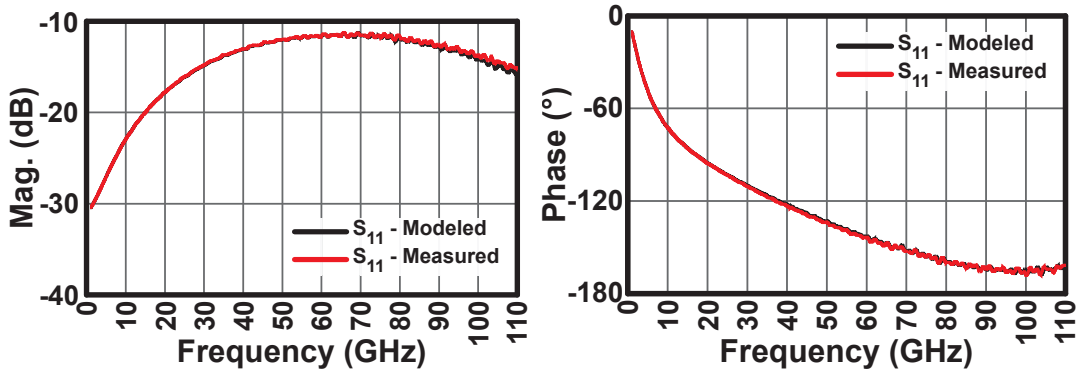


(a) (b)

Figure 3.84: Comparison between measurements and characterized of Fig. 3.67:(a)magnitude of S_{21} in dB, (b)phase S_{21} in degrees.

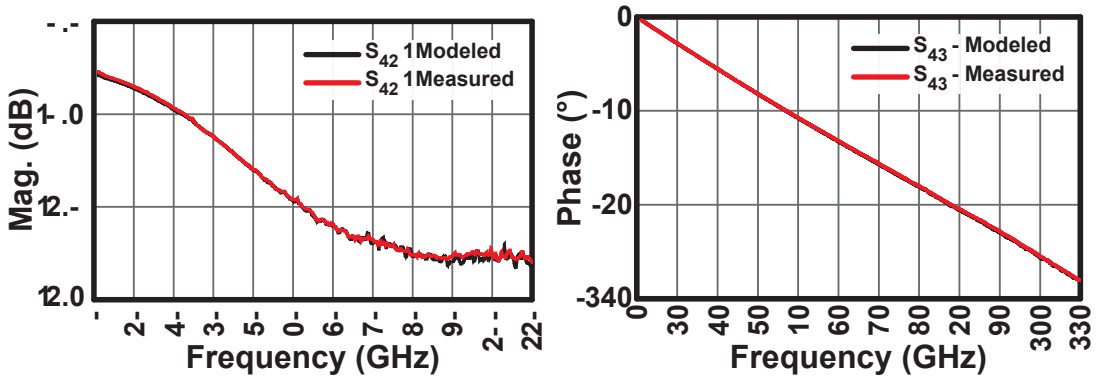
3.5.7 Conclusions on Multi-Port Device Modeling and Characterization

Characterization of a multi-port device is not easy, for both two-port and four-port VNAs. Because of the decreased dynamic range of multi-port VNAs after 67 GHz, accurate measurements cannot be done. Moreover, considering differential measurements the de-embedding of GSSG pads is a hard task. Characterization using two-port VNA measurements has its own issues. The numbers of devices to be manufactured, knowledge on loads are the disadvantages of this approach. In here, new methods to characterize multi-port devices are presented. L-2L de-embedding method is used for GSG pad and TL characterization. This characterized TLs are used both as for



(a) (b)

Figure 3.85: Comparison between measurements and characterized of Fig. 3.68:(a)magnitude of S_{11} in dB, (b)phase of S_{11} in degrees.



(a) (b)

Figure 3.86: Comparison between measurements and characterized of Fig. 3.68:(a)magnitude of S_{21} in dB, (b)phase S_{21} in degrees.

terminations of the unconnected ports of the devices and interconnection purposes. Theories to reconstruct the S-parameter response of the CTL with four measured structures, and cross-line with two measured structures are introduced. To validate the method for cross-line, a comparison of the found S-parameters are done with the four-port measurement results version, and it can be seen that they are in a well agreement. To validate the method for CTL, CTL is constructed in an EM simulator environment and simulated. Using this four-port result, the TEGs are reconstructed with TL and pad characteristics and the method is followed. The found S-parameters well matches with the EM simulation results of CTL. It can be pointed that the proposed method works fine up to 110GHz. Thus the method is validated. The response of the CTL is found from the measurement results. In order to compare the characterization

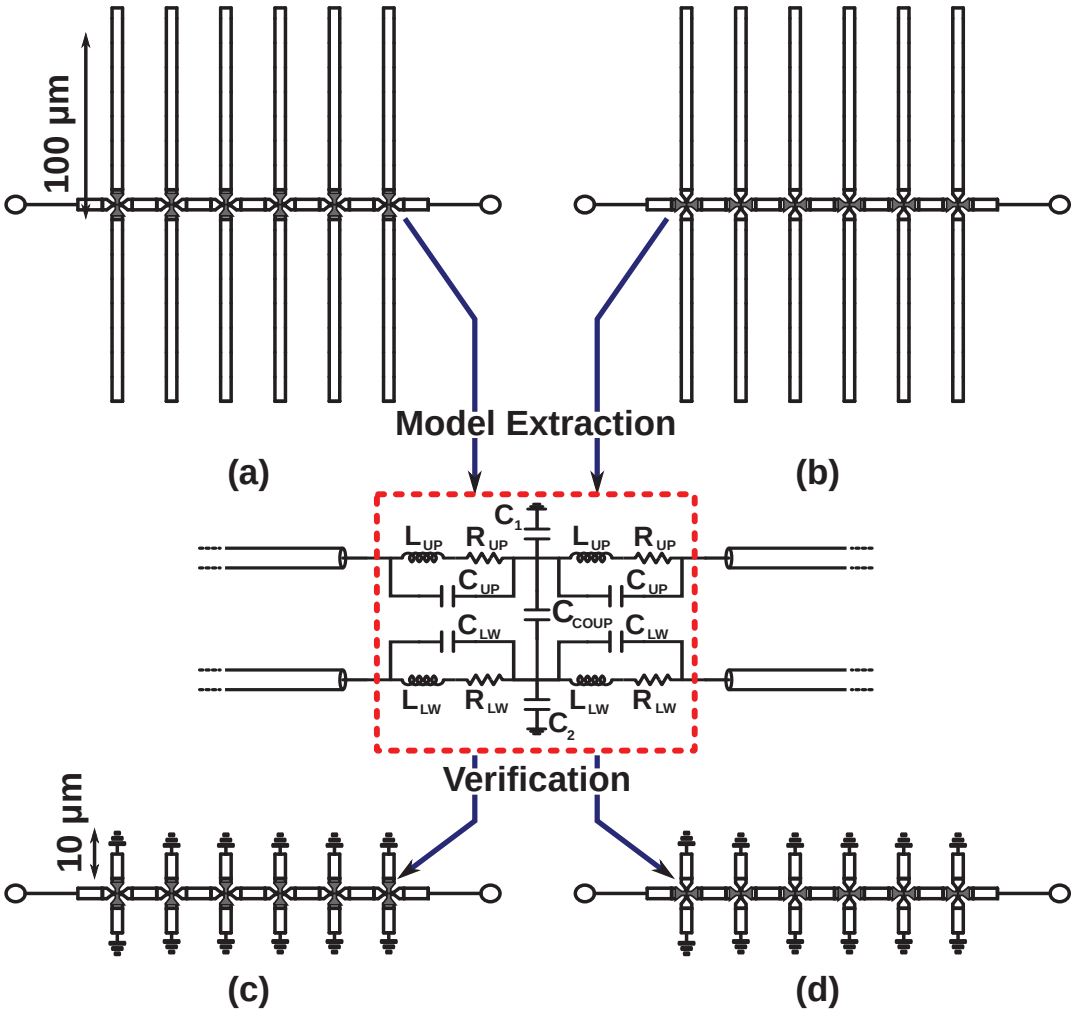


Figure 3.87: An illustration of the manufactured TEGs, and crossing TL model extraction and validation flow (middle). (a)CTL orientation as in Fig. 3.64(a), ports 3 and 4 connected to open circuited TLs, (b)CTL orientation as in Fig. 3.64(b), ports 1 and 2 connected to open circuited TLs, (c)CTL orientation as in Fig. 3.64(a), ports 3 and 4 connected to short circuited TLs, (d)CTL orientation as in Fig. 3.64(b), ports 1 and 2 connected to short circuited TLs.

results of the CTL, the TEG responses are reconstructed in an circuit simulator environment. These results are compared with the measurement results, which are well-matched from 1 to 110GHz.

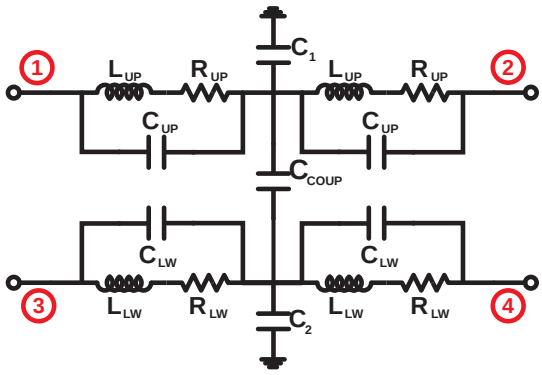
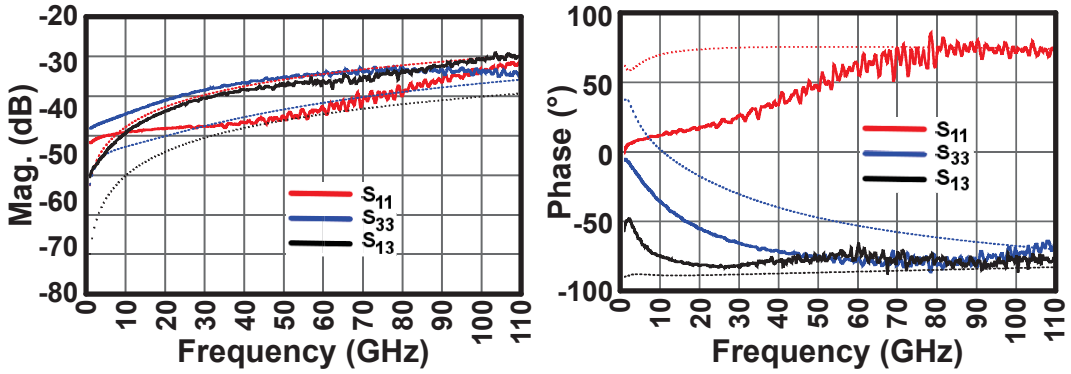
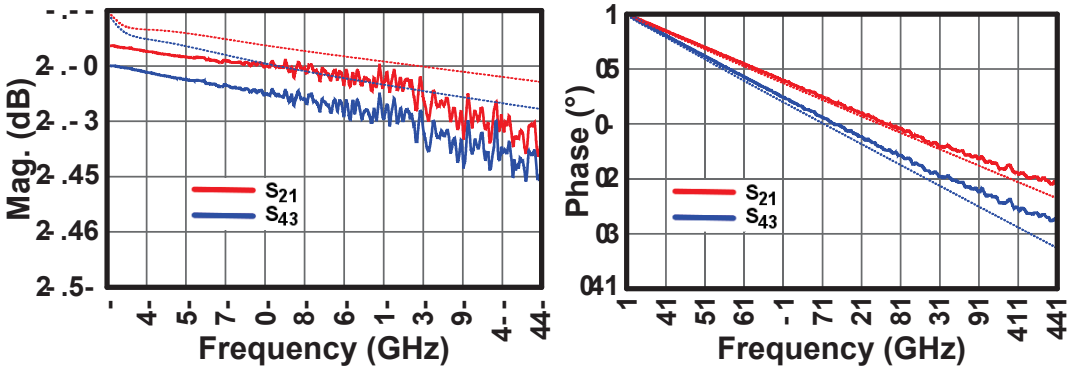


Figure 3.88: Lumped equivalent circuit model for CTL, orientation is illustrated in Fig. 3.64(a) and (b).



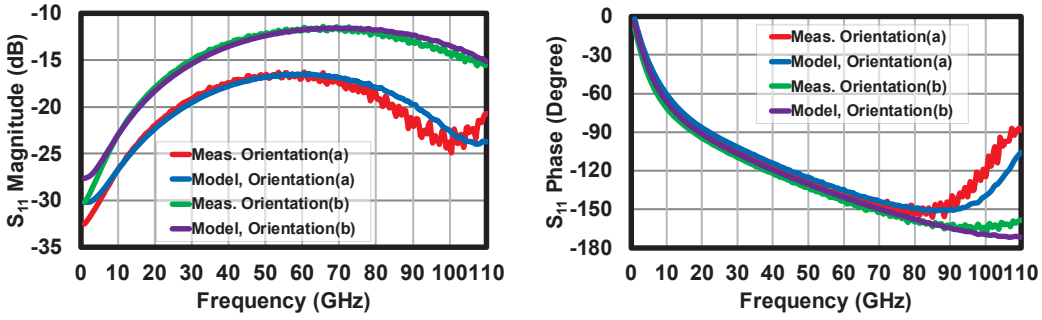
(a) (b)

Figure 3.89: Comparison of characterized and modeled S-parameters of CTL: (a)magnitude (dB) S_{11}, S_{13}, and S_{33}, (b)phase (degree) S_{11}, S_{13}, and S_{33}



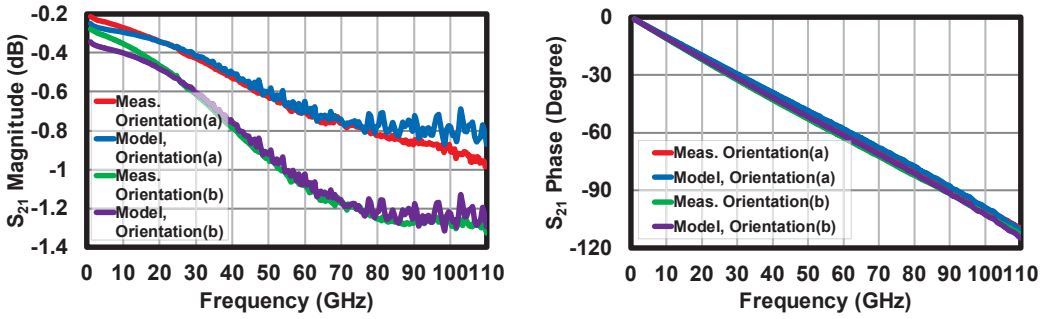
(a) (b)

Figure 3.90: Comparison of characterized and modeled S-parameters of CTL:(a)magnitude (dB) S_{21}, and S_{43}, (b)phase (degree) S_{21}, and S_{43}.



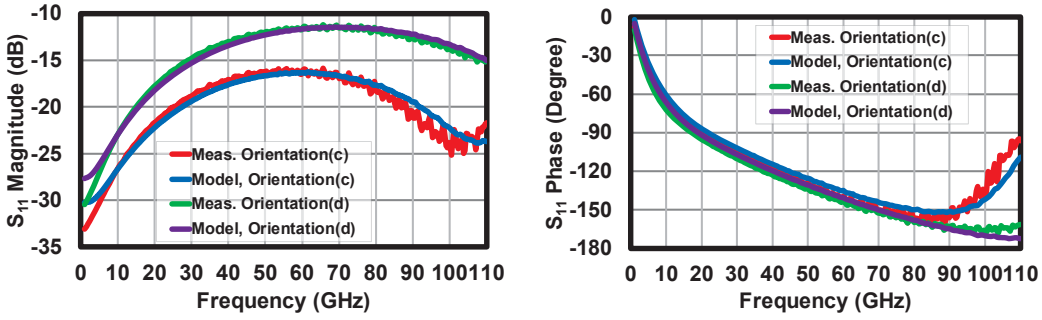
(a) (b)

Figure 3.91: Comparison between measurements and modeled S-parameters of Fig. 3.88(a) and (b):(a)magnitude of S_{11} in dB, (b)phase S_{11} in degrees.



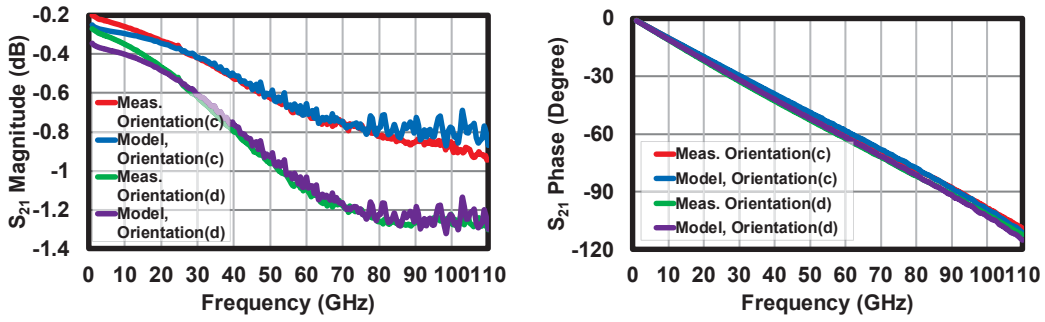
(a) (b)

Figure 3.92: Comparison between measurements and modeled S-parameters of Fig. 3.88(a) and (b):(a)magnitude of S_{21} in dB, (b)phase S_{21} in degrees.



(a) (b)

Figure 3.93: Comparison between measurements and modeled S-parameters of Fig. 3.88(c) and (d):(a)magnitude of S_{11} in dB, (b)phase S_{11} in degrees.



(a) (b)

Figure 3.94: Comparison between measurements and modeled S-parameters of Fig. 3.88(c) and (d):(a)magnitude of S_{21} in dB, (b)phase S_{21} in degrees.

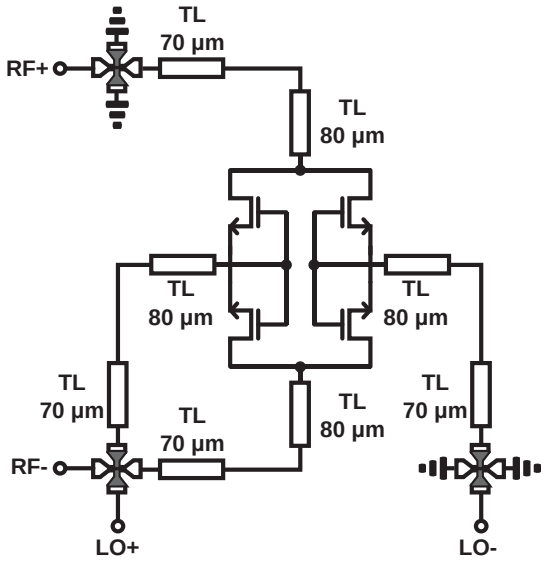


Figure 3.95: An example passive balanced mixer with three CTL devices.

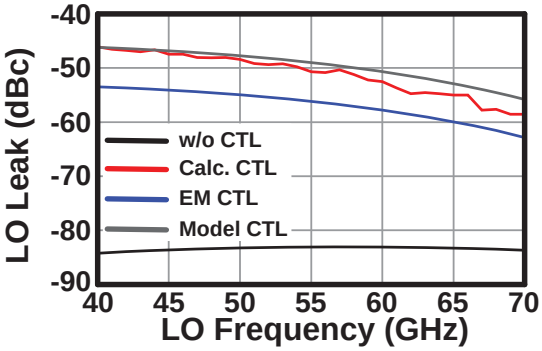


Figure 3.96: LO leakage response of the mixer without any CTLs (black line), with EM simulated response of CTL (blue line), with modeled response of CTL and with calculated response of CTL (red line).

3.6 Conclusions on Device Modeling Chapter

This chapter mainly focuses on device characterization for millimeter-wave CMOS circuit design. First, analysis on de-embedding is done based on virtual-thru response obtained form L-2L method. It is seen that the complex propagation constant for transmission lines are not depended on the model of pad parasitics, instead it is depended on virtual-thru response itself. It is also observed that de-embedding is not always give the similar results for different CMOS processes. Than double-T type pad model is introduced with its theory for accurate characterization impedance modeling for transmission lines. Moreover, a de-embedding algorithm is provided for different processes to achieve accurate transmission line characteristics and pad parasitics model based on three element pad models. After a throughout investigated analysis on de-embedding, conventional device models are revisited and it is found that device model based simulations and measurement results have mismatch at W-band frequencies. After the small-signal measurements of the amplifier it is seen that the responses of simulation and measurement results well matched up to around 70 GHz. However, the results start to differ from each other after 70 GHz. In order to prove the simulation accuracy for the amplifiers, pad parasitics, de-embedding method, transmission line characteristics, transmission line corners, transmission line tee-junctions, and metal-insulator-metal transmission line models are improved with different methods than used in conventional model extraction. For tee-junction, a distributed and lumped constant combination model is developed from short circuited transmission line terminated at tee-junction‘s third port, the de-embedding transmission line lengths are adjusted to give accurate response for both characterization structure and verification structure. More accurate tee-junction model is obtained. Other than tee-junction, MIM transmission line is also characterized very accurately using shunt characterization method. In this method two measurement results from the two TEGs are used to fully characterize MIM transmission line by calculating the reflections from the third port of tee-junction. Using the calculated reflection coefficients MIM transmission line S-parameters are calculated. The accuracy according to the characterization TEGs measurement results are more than conventional method. This new MIM transmission line model is included in the simulations and the results are compared with conventional models based simulations results and measurements.

Furthermore, differential Ground-Signal-Signal-Ground de-embedding is proposed with virtual-thru method with the help of mixed-mode S-parameters and solving using two-port networks instead of four-port networks. This de-embedding method is applied for characterization of symmetrical crossing used in differential amplifiers to decrease

the amplitude and phase imbalance.

Chapter 4

Millimeter-Wave and Sub-Terahertz Amplifier Design

4.1 Design of Ultra-Wideband (UWB) W-band Low-Noise Amplifier

4.1.1 Introduction

Remember that the device models mostly accurate up to around 70GHz from previous chapter. However, there are little deviations between the measurement results of TEGs and models after 70GHz. In order to check the validity of the device models after 70GHz, an UWB W-band low-noise amplifier (LNA) is designed with high gain. The UWB characteristics are aimed for gain, input and output return losses, noise figure and even for input-output power performances of LNA. The target characteristics for LNA is given in Table 4.1. Target performances are challenging considering UWB performances.

Before introducing the design of W-Band LNA, previous works are introduced. Note that only amplifiers with UWB performances are aimed. There are several ways to achieve UWB amplifier design. Most common ways are multi-stage common-source topology [59], single-ended multi-stage cascode topolgy [60–62], differential based cascode topology [63, 64] or several ways combination technique [65, 66]. In general, common-source topology has less gain than cascode topology. Cascode topology has several advantages compared to common-source. These advantages are; higher-gain, higher isolation while reducing the Miller capacitance effect and increasing stability of the amplifier. On the other hand, in order to achieve full performance from a cascode stage higher DC power feed voltage is needed, hence the cascode stages have less

Table 4.1: Target Specifications for W-band LNA.

Performance	Target
BW (3 dB)	75-110 GHz
S_{11}	< -10 dB
S_{22}	< -10 dB
Gain	> 20 dB
NF	< 8 dB
P_{DC}	< 70 mW
$OP1_{dB}$	> 0 dBm
IIP_3	> -12 dBm

power-added-efficiency (PAE) which consumes more power. Moreover, the cascode stage of transistors are hard to characterize, and thus the designed (simulated) results and measurement results might be very different than each other. In either topology, UWB characteristics can be achieved by cascading multi-stages and adjusting the inter-stage, input and output matching networks. Several way power combination technique can also achieve UWB characteristics for an amplifier. This techniques should be used when very high output powers are desired. Its DC power consumption is much higher than single ended or differential topologies. In this work, a low power consumption and high gain LNA is desired. Furthermore, common-gate transistor modeling is not accurate. For these reasons, cascode topology is eliminated. Since, this is an LNA design several way power combination technique is also eliminated, to avoid high power and area consumption. However, flat and high gain target is challenging and it cannot be easily achieved by common-source topology (even with several cascaded stages) considering that the transistors maximum available gain drops to very low values especially at very high frequencies. There are some methods to boost the gain of a transistor within the certain limits [28], such as; neutralization or unilateralization to cancel the gate-to-drain parasitic capacitance or increase the isolation by adding an embedding network to a transistor. There is also a method to achieve the maximum achiavable gain of a transistor which is introduced for CMOS applications [13, 28, 67]. In [28] inductors are proposed to connect between gate and drain of a transistor which is effectively a parasitic capacitance cancellation method also achieves the optimum conditions to achieve more gain from a transistor. In [67] same method is applied with transmission lines. In this work, also same methodology is applied with several differences in the design approach to achieve UWB amplifier performances compared to the previous two works mentioned in which only one frequency is aimed to boost the gain. In the next subsection, the size selection of the transistor is investigated.

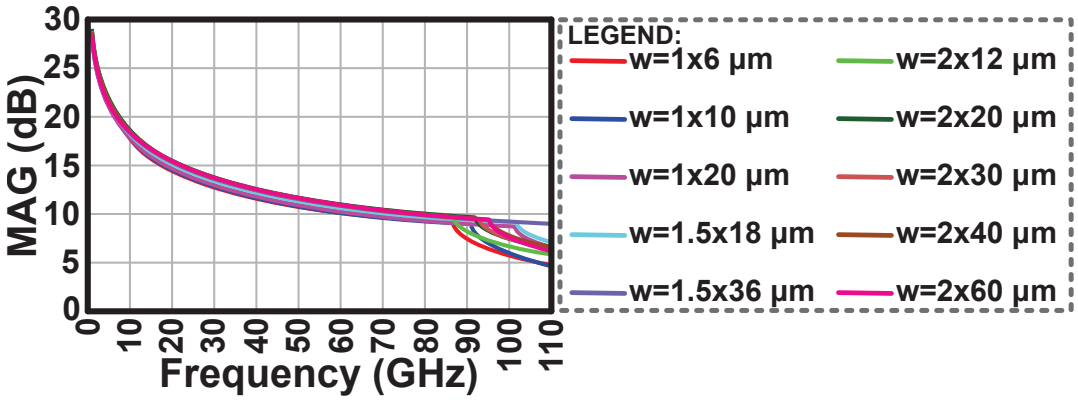


Figure 4.1: Maximum available gain comparisons for different transistor sizes (AxBµm means that A is one finger width, and B is the total width).

4.1.2 Transistor Size Considerations

Several transistors MAG response is given in Fig. 4.1 from the models as explained in Chapter 3. From the figure, only transistor with a width of 36µm (1.5µm × 24) does not trip to maximum available gain region (the corner points on the MSG/MAG responses of other transistors).

Moreover, considering the whole W-band, 36µm (1.5µm × 24) transistor provide highest gain. Note that there are other wider transistors modeled, however it is well known that wider the transistor lower the gain in high frequencies, and hence in here transistor with high gain at W-Band are considered.

However, as described in Chapter 2, in order to decrease the number of stages of the amplifier, and hence to decrease the silicon area occupation and power consumption, maximum achievable gain (MACG) is aimed in this work. In order to provide a quantitative results for MACG, same transistors gain results used in the previous MSG/MAG figure are calculated according to the equations presented in Chapter 2. Found values are presented in Fig. 4.2. As expected, transistor with a width of 36µm (1.5µm × 24) have the highest MACG. Thus, in this work, this transistor is used for LNA design.

Remember from Table 4.1 that it is desired to design an UWB amplifier with all of the performances given in the table from 75 to 110GHz. As it is expected there are several trade-offs while designing an UWB amplifier (in fact for all amplifiers or any other circuits, however for a large bandwidth as the target trade-offs are more severe). The topology used in the design is the positive feedback common-source amplifier. For a simple common-source topology at these frequencies gain cannot be a trading item.

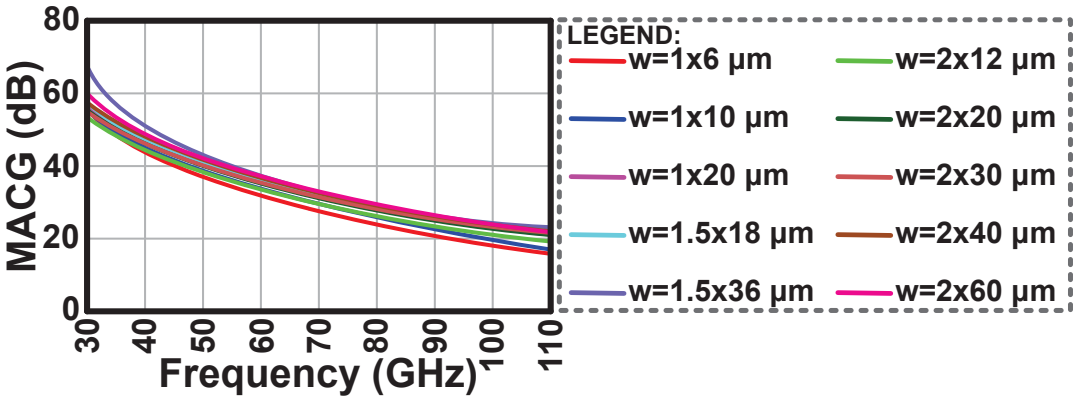


Figure 4.2: Maximum achievable gain comparisons for different transistor sizes (AxBµm means that A is one finger width, and B is the total width).

However, if one can successfully implement feedback based common-source topology aiming to obtain maximum achievable gain definition, one can sacrifice from gain while achieving the defined target. For this reason a detailed description on the design of amplifier is provided in the next section.

4.1.3 Design and Simulation Results of Amplifier

Like in every amplifier design, the first step is to choose an appropriate transistor size according to the needs of circuit. In this work, transistor with a total width of 36µm (1.5µm×24, gate length of 60 nm) is chosen according to its gain performance for different gain definitions. It has the highest gain among all of the transistors investigated in the above section. Moreover, almost all of the transistors noise performance are very close to each other from 2 to 4 dB for the bandwidth of 75 to 110GHz, respectively for noise figure values. Moreover, for an LNA of concern to decrease the noise figure the gain of the first two to three stages is important. The amplifier designed in this work is based on positive feedback common-source topology, similarly with [28, 67]. The feedback part is based on transmission lines. However, in [28, 67] there is no gate bias control on the amplifiers, for both work the amplifier is fed with only DC power feed which is gate bias transistor drain voltage at the same time. So that the transistors are always in deep saturation region, hence the efficiency of the amplifiers are low. Which is not desired for our purposes. In this work, gate bias network of a DC cut capacitor with 150fF capacitance value and 5kΩ bias resistor connected transmission line with a length of 5µm are used to bias the transistor and separate the DC power feed and gate bias as shown in Fig. 4.3. As mentioned in the above section, no matter the embedding network

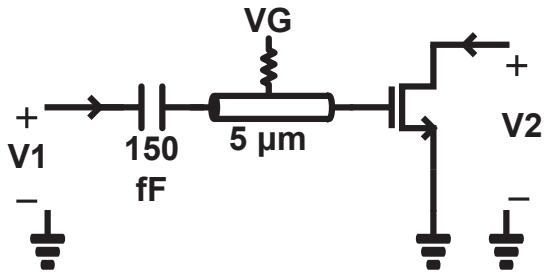


Figure 4.3: Transistor with DC feed networks and voltage and current annotations for optimum condition calculation.

is the transistors optimum parameters do not change. However, the nature of requirement on the embedding network changes. To observe this fact, optimum conditions for 36µm width transistor with and without DC feed network are calculated. Fig. 4.4(a) presents the calculated maximum achievable gain results for the two conditions. It can be observed that it changes very slightly that it can be neglected. This also proves that the maximum achievable gain is directly related with transistors inherent parasitics and parameters.

Fig. 4.4(b) presents the optimum condition for ratio of input and output voltages. As it can be seen, the optimum condition for voltage magnitude ration changes considerably for the remaining embedding passive, lossless and reciprocal network. On the contrary, optimum phase condition does not change considerably as seen in Fig. 4.4(c). Since the magnitude condition decreased significantly, surrounding network can cause problems in terms of stability of the amplifier. This is, most probably, the reason why positive feedback topology is not used with a bias network.

In order to enhance the stability of the amplifier, a few techniques are used and presented below. This is explained along with the explanation of design. Considering the very high frequencies and the gain of transistors, desired UWB matching and gain characteristics a five stage feed-back common-source topology is designed, and a general illustration is given in Fig. 4.5.

Although the inter-stage matching network is not shown in here, it is introduced below. Before going into the matching networks, used topology of the amplifier is investigated and the design procedure for amplifying stages are introduced. Fig. 4.6 shows the topology used with its components. Transmission lines are used for design, whose modeling and characterization approach introduced in the chapter before. Transmission line with length “T1” is placed before the DC cut capacitor and after the tee-junction which is used to connect the positive feedback network from drain to gate. Transmission line with length “T2” is placed before the tee-junction (which its unconnected port in this figure is connected to the following stage via inter-stage

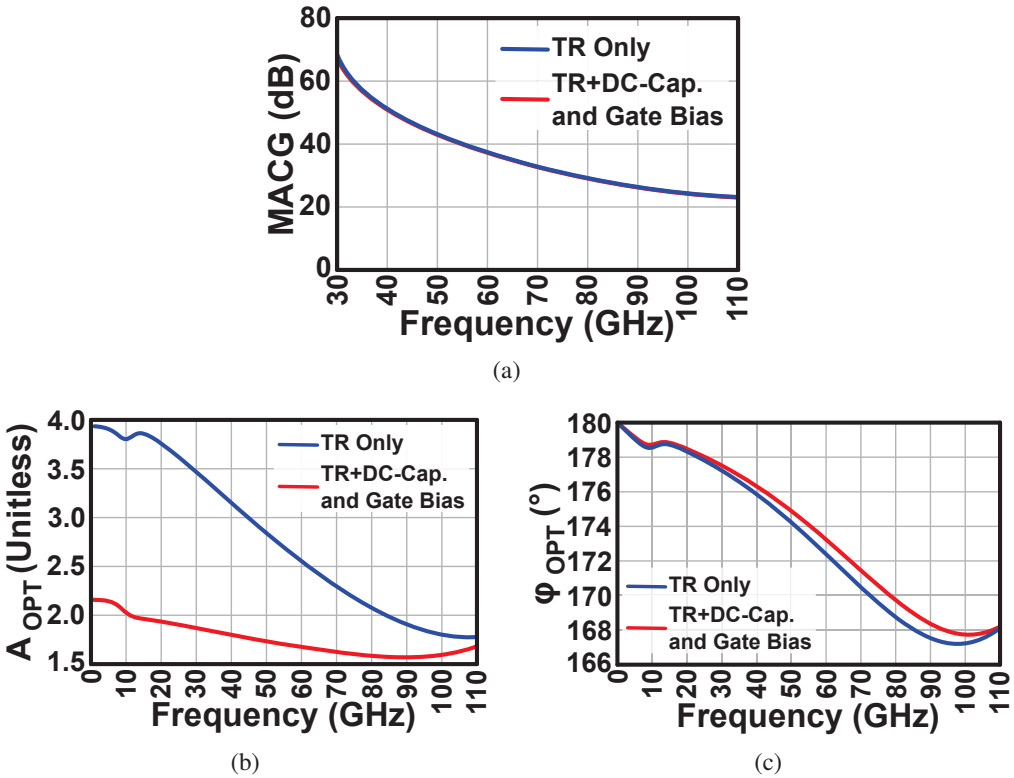


Figure 4.4: Calculated optimum conditions for transistor with and without bias network (a) maximum achievable gain, (b) A_{opt}, and (c) ϕ_{opt}.

matching network or for the last stage it is connected to the output port via again matching network) and after the transistor. Other port of the mentioned tee-junction is connected to another tee-junction whose one port is connected to the DC feed network and the other port is connected to the positive feedback transmission line via a transmission line with a length of "T3". Note that the length of feed-back transmission line is automatically decided by the lengths of above three transmission lines and 60μm more. In order to lessen the layout effort of this amplifier, a corner is assumed in the feed-back path, and transistor, capacitor and gate bias network has a total length of 60μm.

Moreover, as introduced in conventional device model chapter a 120μm length metal-insulator-metal transmission line is connected between DC power line to isolate DC and RF signals. MIM TL is lossy, hence it is helpful to stabilize the amplifier, and 120μm length is decided according to the stability of the amplifier. MIM TL is connected to the tee-junction below with a transmission line length of "T4". This transmission line lengths are introduced because adjusting these lengths, one can adjust optimum conditions (A_{opt} and ϕ_{opt}), hence gain of the stages. Furthermore, matching can also be adjusted. The

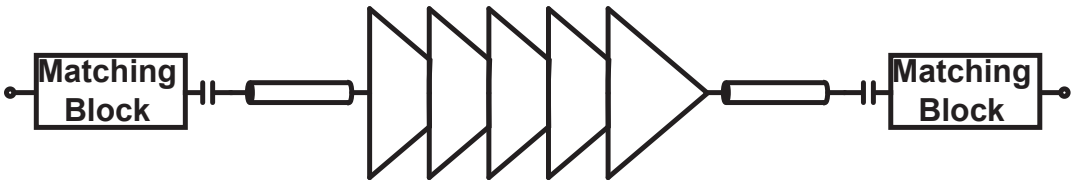


Figure 4.5: A general schematic representaiton of the amplifier.

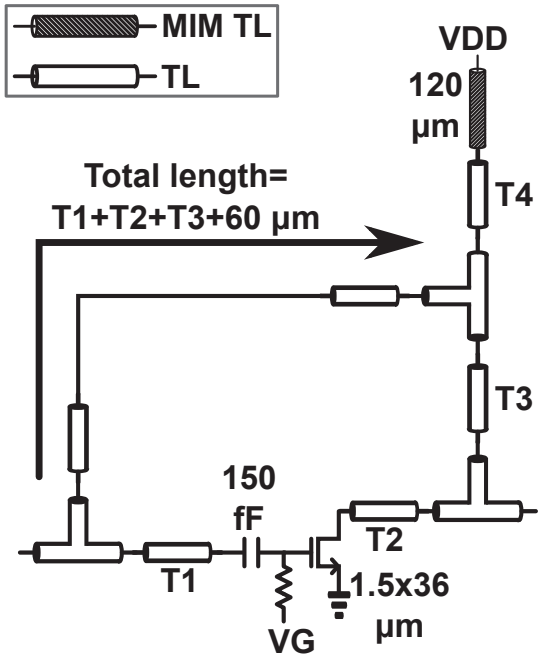


Figure 4.6: Positive feedback common-source topology with its components.

effect of transmission line lengths are investigated on the optimum conditions and can be summarized as follows:

1. When "T1" is increased, frequency of maximum point for voltage ration value A ($|V_2|/|V_1|$) remains almost constant. Maximum point's value remains almost constant. Frequency of intercept point between ϕ_{opt} and current phase condition ϕ decreases. Note that the center frequency of gain is very near this first intercept point. For that reason, the center frequency of gain decreases, however, the gain increases. This is expected since when the frequency decreases gain increases according to the transistor's characteristics.

2. When "T2" is increased, frequency of maximum point for voltage ration value A is decreased. Different than above case, maximum value for voltage ration increases

Table 4.2: Adjusted transmission line lengths.

Lengths	First-Stage	Second-Stage	Third-Stage	Fourth-Stage	Fifth-Stage
T1	67.5	172.5	65	72.5	17.5
T2	12.5	25	92.5	85	27.5
T3	62.5	57.5	110	7.5	130
T4	340	295	200	140	85

hence gets closer to optimum value. Thus, the gain increases more than the above adjustment, but similarly center frequency of gain decreases since the intercept frequency point between ϕ values decreases. One interesting effect of this adjustment is, ϕ value gets steeper which will cause the gain to increase more at the optimum value, however, the bandwidth of the gain decreases.

3. When "T3" is increased, frequency of maximum point for voltage ration value A is decreased. Similar with "T1", the maximum point's value remains almost constant. Frequency of intercept point between ϕ_{opt} and current phase condition ϕ decreases. Hence, center frequency of gain decreases and naturally gain increases a little.

4. When "T4" is increased, frequency of maximum point for voltage ration value A is decreased. Maximum point's value increases. It does not have effect on the frequency of intercept point between ϕ_{opt} and current phase condition ϕ. So that, center frequency of gain does not change, however, since voltage ration increases gain increases. Moreover, ϕ becomes steeper and gain increases with decreased gain bandwidth and flatness. This transmission line have significant effect on the matching also.

The first stage gain center frequency is decided to be around 80GHz with a moderate gain. The center frequency is not near middle of W-Band, since the first stage's gain is important for noise figure also. A middle point in W-Band is chosen to keep the noise figure below certain value in the overall W-Band. The second and third stages center frequency is adjusted around 60GHz (note that after cascading every stage and matching between the stages this value would increase to around 75GHz) to have high gains. Second stage gain is desired to be higher than third stage, however, its bandwidth would be lower in this case. Stage four is desired to be around 80GHz with a flat gain bandwidth to preserve flatness in the overall band. Stage five has also same duty with a center frequency around 70GHz. The adjusted lengths for every stage are given in Table 4.2.

Resultant voltage ration conditions (A values), phase conditions (ϕ values) of transistors for five stages in comparison with optimum conditions are provided in Fig.

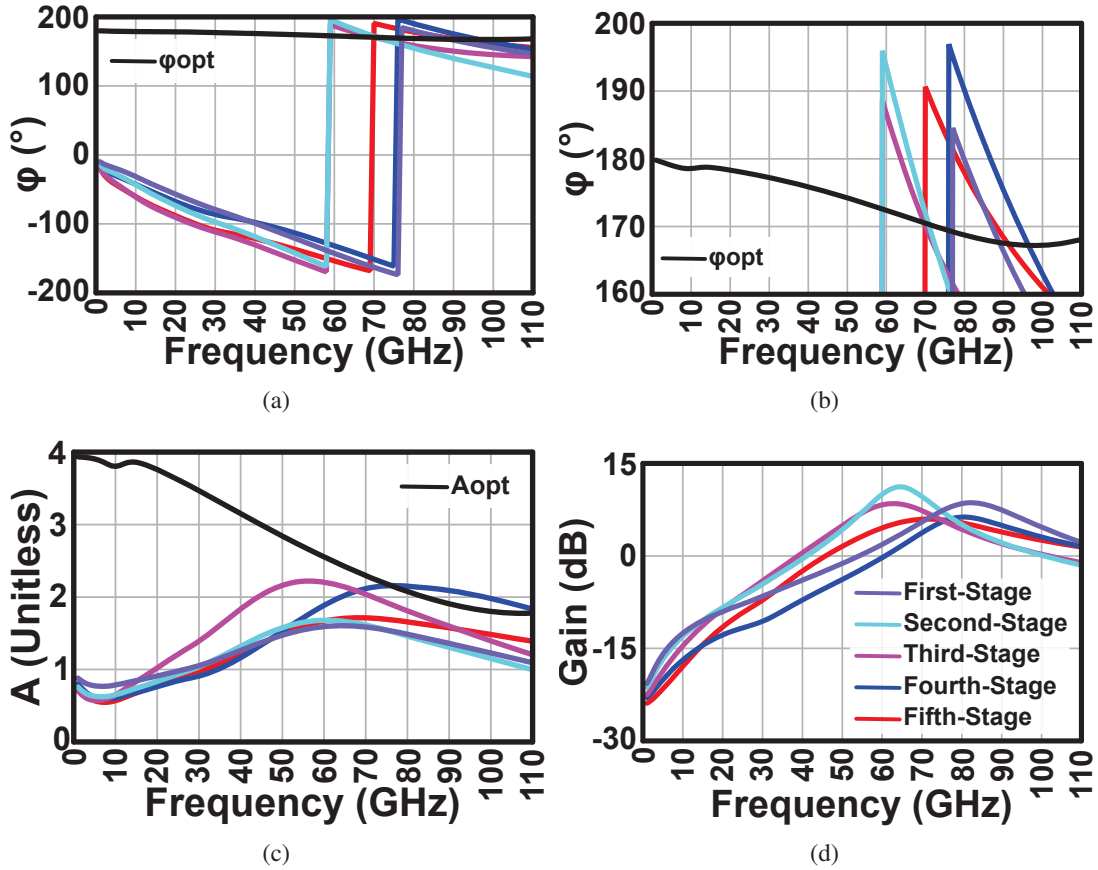


Figure 4.7: Amplifier stages condition and gain responses after transmission line adjustment (Table 4.2) (a) phase condition of stages in comparison with optimum phase condition, (b) zoom in version of phase conditions, (c) voltage ration conditions of stages in comparison with optimum voltage ration condition, and (d) resultant gain of stages.

4.7 together with resultant gain of stages. The first intercept point of phase conditions with optimum phase condition of transistor are 77, 59, 59, 76, and 70GHz respectively from first stage to fifth stage. Moreover the second intercept point for stages are 89, 71, 70, 96, and 91GHz, respectively from first stage to fifth stage. Resultant center frequencies of gain responses for stages are 82.5, 64.5, 62.5, 80.5, and 71.5GHz respectively from first to fifth stage. As it is mentioned above in the effect of transmission line lengths on amplifier stages, the center frequency of gain responses are very close to first intercept point, and between the two intercept points. Moreover it can be observed that the most steep phase response is given for second stage which resulted higher gain and lower bandwidth. This can be clearly seen when the phase responses of second and third stages and gain responses are observed. Furthermore, as it can be observed, wider the bandwidth between the first and second intercept points flatter the

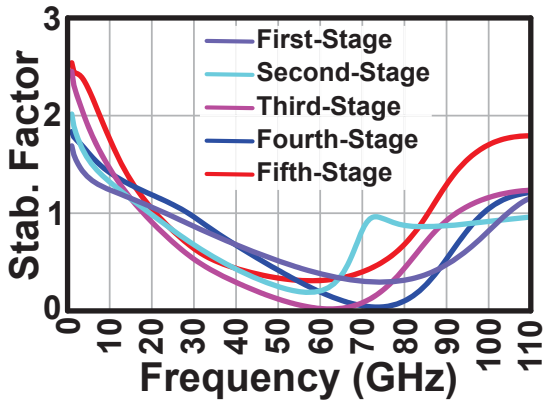


Figure 4.8: Resultant stability factor of the stages without cascaded and matching blocks.

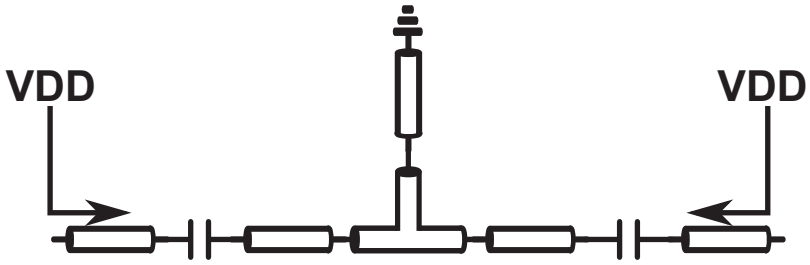


Figure 4.9: Conventional short-circuited shunt connected matching block considering DC cut from power feed.

gain. The gain of first three stages are 8.6, 11.2, and 8.5dB correspondingly. They are very close to MAG values of transistor even with considerably long transmission lines. This proves that transistor is forced to give more than the classical gain. From the beginning it is mentioned that UWB performance target is challenging however with this method sacrificing from the gain (not from the classical gain definition) UWB performances can be achieved. Fig. 4.8 shows the current stability factor of the amplifiers without matching circuitry, they can be improved after cascading and input, output matching blocks are added. Even so, while designing matching blocks care must be taken on overall amplifier stability factor.

According to results the best inter-stage network is found to be inductive. The easiest way is to include a short-circuited shunt transmission line between the stages. The conventional way to do that in a feedback amplifier is to include DC cut capacitors before and after the short circuited shunt connected transmission line to provide power flow to ground as illustrated in Fig. 4.9.

However, this method is area consuming, and added series DC cut capacitors may

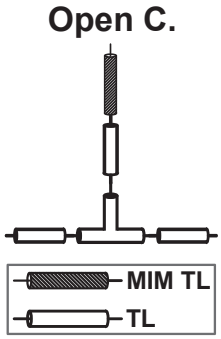


Figure 4.10: MIM TL terminated open-circuited shunt transmission line matching block realizing short circuit.

result in unwanted return loss responses. In order to realize, short-circuited shunt transmission line, instead of terminating the line with ground, one can terminate with MIM TL. Since MIM TL has very low characteristic impedance, it can realize near ground response at the terminated end of transmission line. Moreover, since the other end of MIM TL left open circuited, one can exclude DC cut capacitors. The desired matching block can be observed in Fig. 4.10. Addition of MIM TL also helpful to stabilize the amplifier since it has very large loss, penetrated waves to MIM TL decreases in power considerable before reflected back to amplifier. This matching block is used in all inter-stage, and input and output matching blocks.

All of the transmission line lengths are adjusted to achieve the target performance and simulation results are provided in here. Input and output return loss performances of LNA are presented in Fig. 4.11, all five transistors are biased at 0.7V with 1V DC feed. As it can be observed after 75GHz (black markers on smith charts) traces are very close to 50Ω point on Smith Charts. Moreover, input and output return loss responses in terms of magnitude (dB) shows that in the desired W-Band (75 to 110GHz) the results are less than -10 dB, which is the target assigned at the beginning.

The simulated gain results are given in Fig. 4.12(a) from 1 to 110GHz and in Fig. 4.12(b) from 60 to 110GHz. The resultant gain is flat from 74 to 110GHz with 20dB to 23dB, when all gate biases are 0.7V. As mentioned above, stability factor of the LNA might be a problem since the topology is based on feedback. Resultant stability factor of LNA from 60 to 110GHz can be observed in Fig. 4.12(c). Only this frequency region is given, because in the other frequency regions stability factor is much more than presented values, hence the amplifier is stable in all frequencies. Moreover the least stability factor is more than 70, which is adjusted with matching blocks to be on the safe side even after manufacturing of LNA. Noise figure of LNA is illustrated in Fig. 4.12(d).

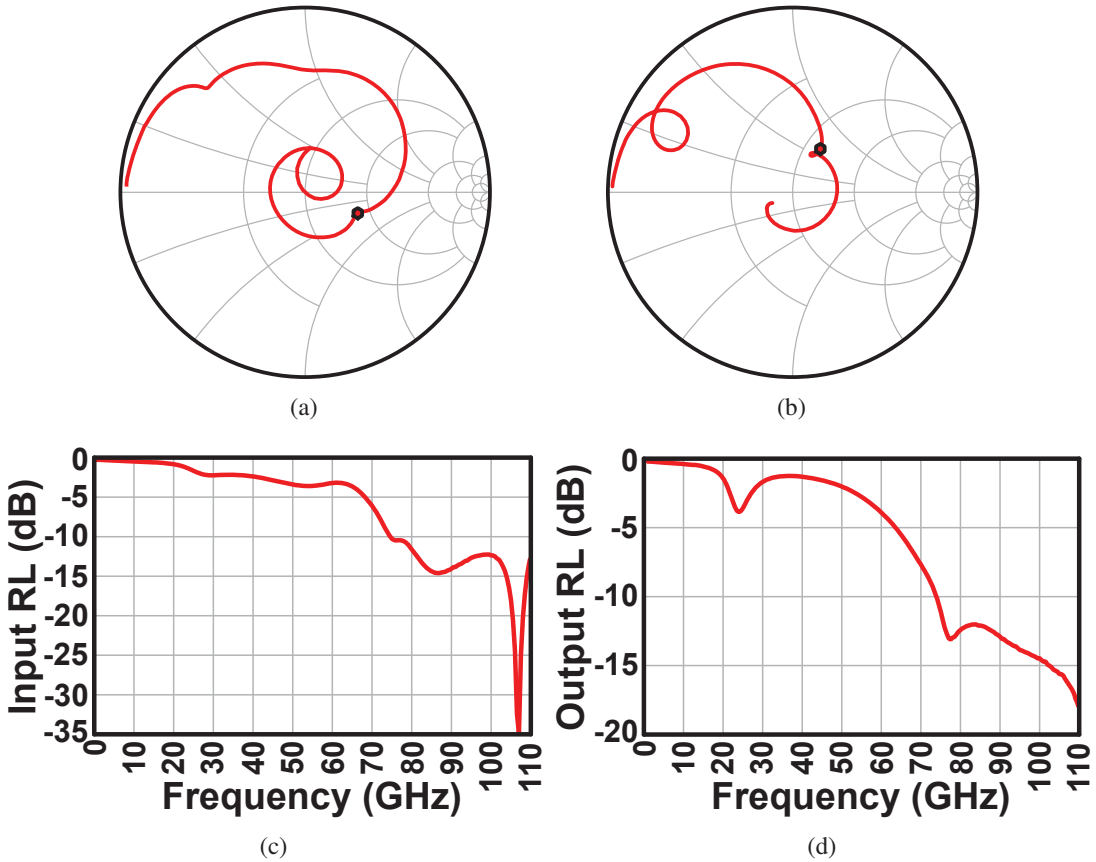


Figure 4.11: Simulated LNA input and output return loss results form 1 to 110GHz (all gate biases 0.7V) (a) input return loss on smith chart (black marker is at 75GHz), (b) output return loss on smith chart (black marker is at 75GHz), (c) input return loss magnitude, and (d) output return loss magnitude.

It can be observed than noise figure is less than 8dB in W-Band (75 to 110GHz). As a conclusion on the design of LNA, it can be commented that target UWB performances are achieved with five-stage positive feedback common-source topology of amplifier. The DC power consumption of LNA from 1V power supply is 65mW, which is also lower than the targeted value. Note that for the sake of simplicity input and output power simulation results are not included in here. Maximum saturated output power is around 4.5dBm, and output 1dB compression point is 0.8dBm. Moreover, IIP3 is around -12dBm.

Simulated performance of LNA is compared with previous works from literature. Note that, several way combining architectures and other process related works are omitted in the comparison in order to make a fair comparison. The comparison is presented in Table 4.3. It can be observed that our works can achieve a flat response with

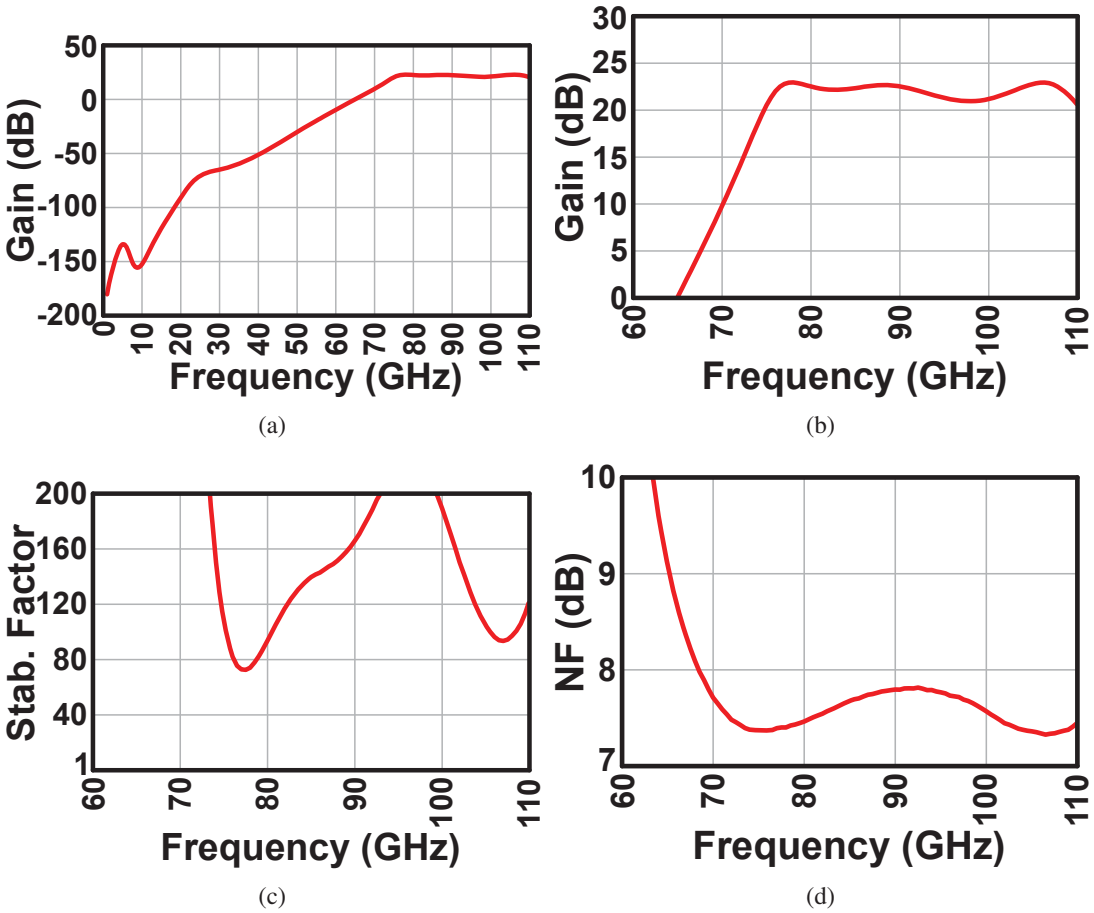


Figure 4.12: Simulated LNA gain, stability factor, and noise figure responses (all gate biases 0.7V) (a) gain results of LNA from 1 to 110GHz, (b) focus on gain results from 60 to 110GHz, (c) stability factor results form 60 to 110GHz, and (d) noise figure results from 60 to 110GHz.

the widest frequency band, with a low DC power consumption and competitive noise figure performance. Return loss comparison is not included in here, however, current LNA design is more successful than others. That is also because current design can achieve with five stages, hence area is increased a little as compared to other works.

This design is manufactured with 65 nm standard CMOS process. The layout of amplifier is presented in the following figure. The width of amplifier is 0.66mm and the length of amplifier is 0.8mm, resulting in a total area of 0.528mm^2. In the next section, the small-signal S-parameters measurement results are presented in comparison with simulation results.

Table 4.3: Simulated performance comparison with other works.

REF	[61]	[62]	[59]	[60]	This Work
Tech.	90 nm	65 nm	65 nm	130 nm	65 nm
Topology	3-stage Cascode	4-stage Cascode	3-stage CS	2-stage Cascode	5-stage FB-CS
Gain (dB)	14-17	20-25	24	6	20-23
3-dB BW (GHz)	86-108	75-120	79-106	75-95	74-110
P_{sat} (dBm)	4	-	14.8	8.1	4.5
OP1dB (dBm)	2	-	12.5	6.3	0.8
P_{DC} (mW)	54	48	163	338	65
NF (dB)	-	6-8	-	-	≈ 7.5

4.1.4 Small Signal Measurement Results

Manufactured LNA is measured with a VNA measurement setup up to 110GHz. The simulation results and measurement results are compared in Figs. 4.14, 4.15, blue lines in figure are obtained from measurement results and red lines are from the simulation results.

Note that all gate biases this time is 0.8V. ID-VD performance of transistors are measured and threshold voltage of transistors are found to be 0.38V (originally from PDK it is 0.4 V). This change cause the transistors provide more gain than simulated. Hence comparisons are done 0.8V gate biases for which transistors are more saturated, and the rate of change in the gain are less.

Fig. 4.14 presents input and output return loss results. It can be seen that the simulated and measured results clearly follow with each other up to around 70GHz. After this frequency they start to deviate from each other. For example, input return loss in the simulations has a resonance around 105GHz. However, from the measurements this can be seen around 98GHz. There is relatively large frequency shift. Furthermore, in the output return loss there is a resonance occurs from the measurements which is not there in the simulation results. Still, output return loss is less than -10dB in the overall W-Band. Input return loss is less than -10dB from 75 to around 100GHz. After 100GHz because of the frequency shift input return loss pass -10dB level to around -6dB. Figs. 4.15(a), 4.15(b) illustrates the gain response. Note that, simulation and measurement results follow each other up to around 80GHz. After this point they also deviate from each other. Measurement results gets higher than simulated results, and bandwidth gets smaller in comparison with simulation results. Fig. 4.15(c) shows the comparison of stability factor of the amplifier. It can be seen that amplifier is stable even after manufacturing. However, the value is very close to 1 (below that point stability of amplifier is questionable). Remember from the conventional device modeling section

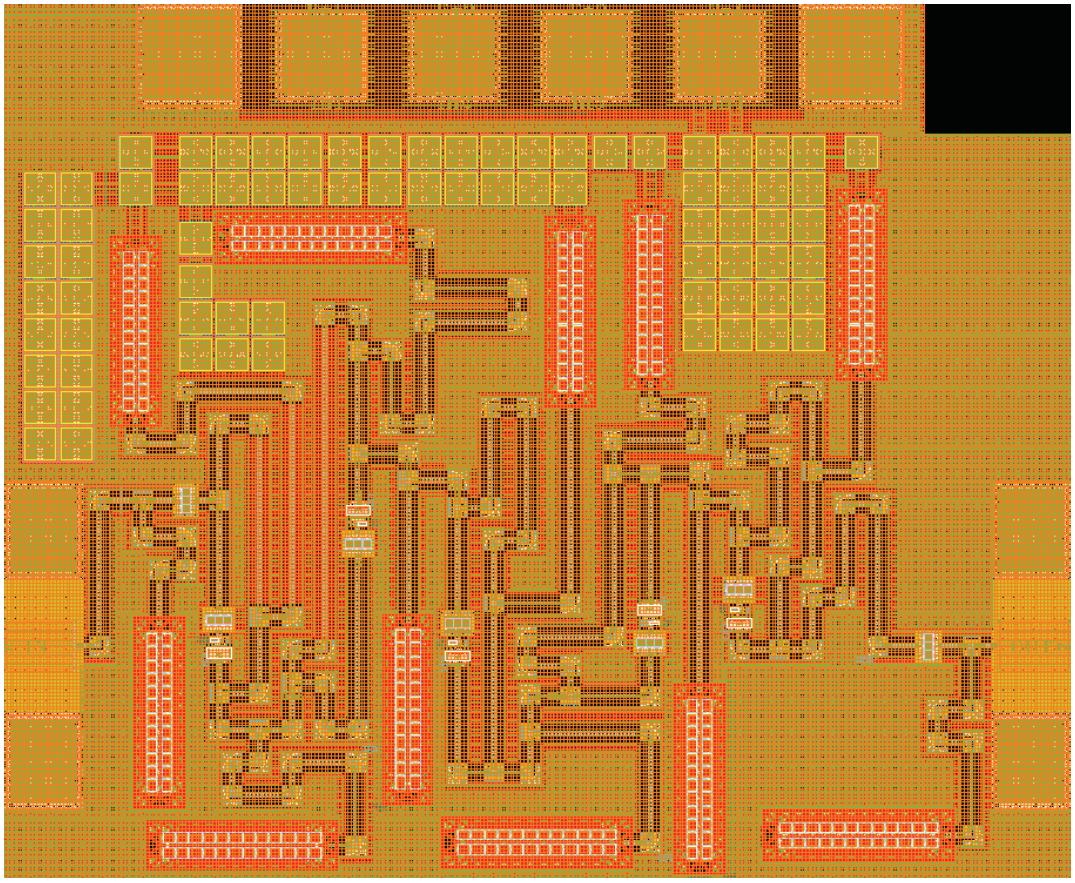


Figure 4.13: Layout of fabricated LNA (length is 0.8mm and width is 0.66mm, total area 0.528mm^2).

that, in most of the device modeling cases the measurement and model results deviate from each other after 70GHz. For this reason, the modeling of devices has to be studied after 70GHz to achieve much more accurate results than conventional models. Investigations are needed to solve this problem on amplifier, by accurately modeling the devices especially for W-Band. For these reasons, in the next chapter device modeling for passives are improved and their effects on amplifier are verified.

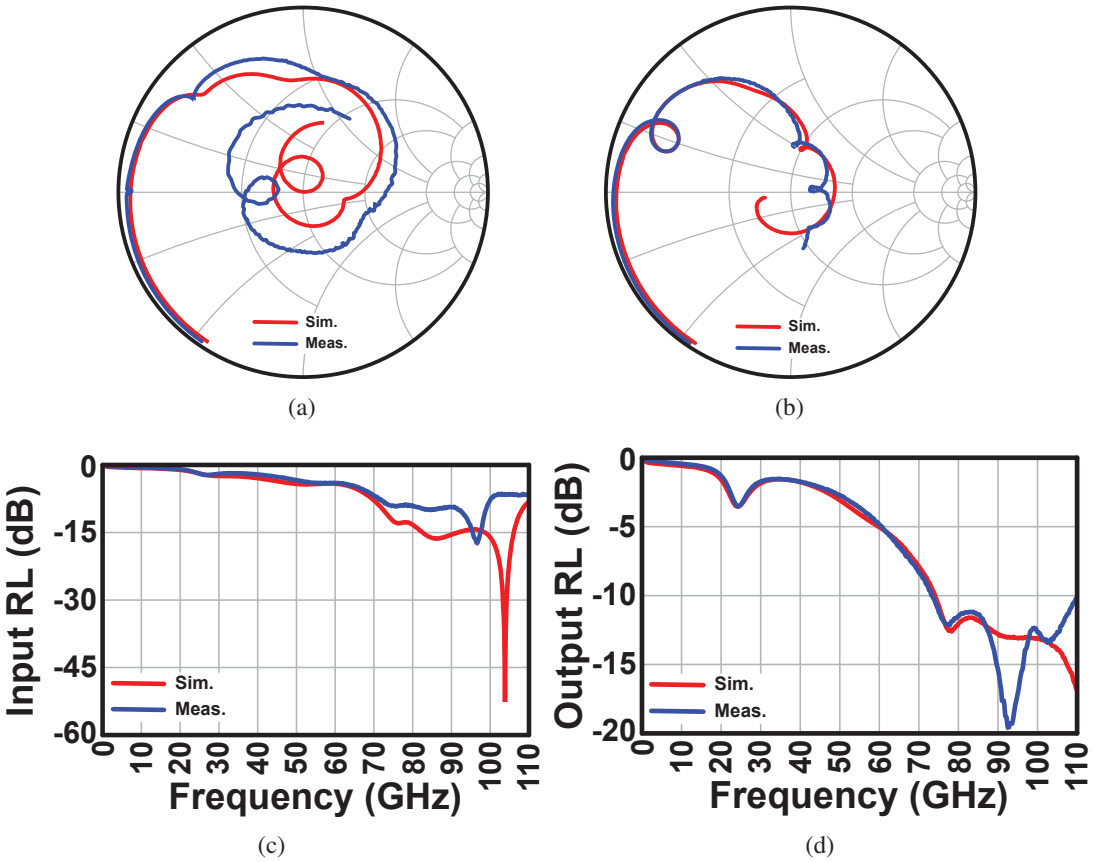


Figure 4.14: S-parameter comparison results between design and measurements of LNA's input and output return loss results form 1 to 110GHz (all gate biases 0.8V, blue lines are from measurement results and red lines are from simulation results), (a)input return loss on Smith Chart, (b)output return loss on Smith Chart, (c)input return loss magnitude (dB), and (d)output return loss magnitude (dB).

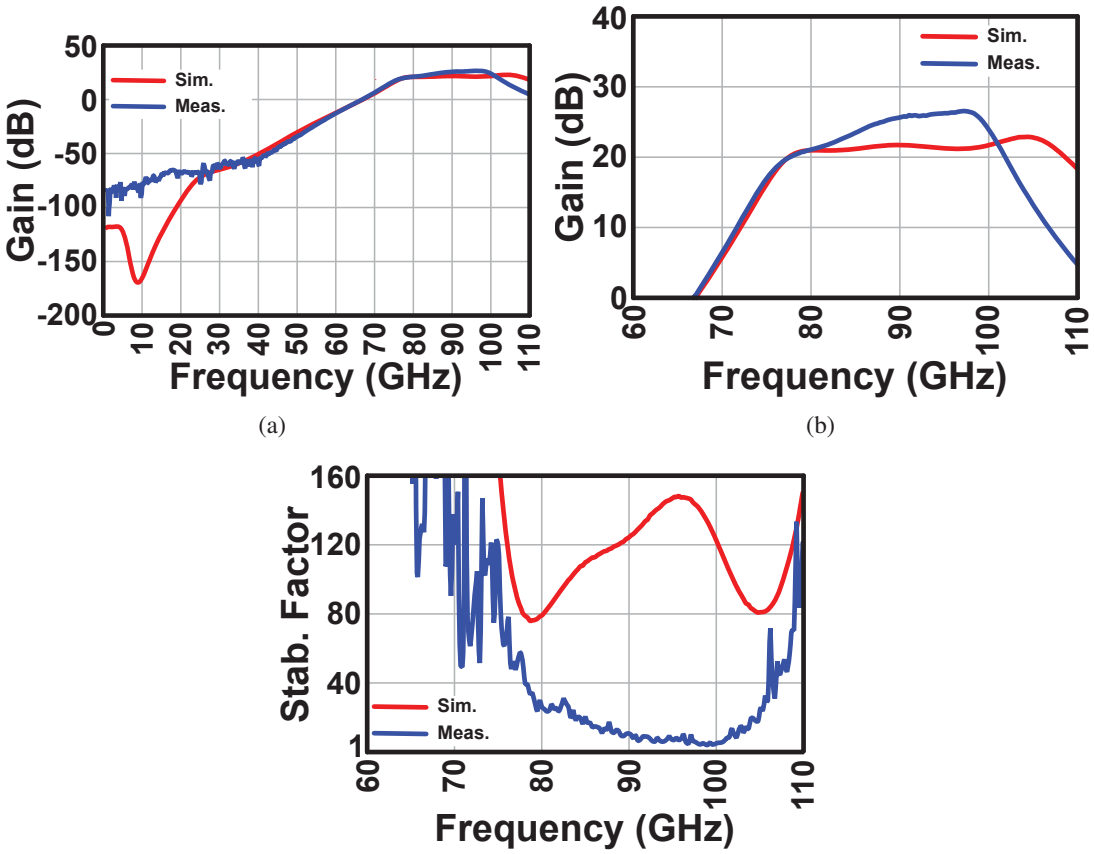


Figure 4.15: S-parameter comparison results between design and measurements of LNA's gain, stability factor, and noise figure responses (all gate biases 0.8V, blue lines are from measurement results and red lines are from simulation results), (a) gain results of LNA from 1 to 110GHz, (b)focus on gain results from 60 to 110GHz, and (c)stability factor results form 60 to 110GHz.

4.2 Sub-Terahertz Amplifiers

4.2.1 Introduction

This section presents the world-first 300GHz amplifier realized by 65-nm standard bulk CMOS technology. The amplifier has gain from 273GHz to 301GHz, and the peak gain is 21dB at 298GHz. The amplifier employs a 16-stage positive-feedback common-source topology. Transistor layout is optimized for minimizing gate and channel resistance, and the maximum operating frequency fmax can be increased up to 317GHz. The power consumption is 35.4mW from a 1.2V supply.

CMOS realization of the terahertz circuits and systems is a promising technology for various applications such as ultra-high-speed wireless communication, imaging, spectroscopy, etc. Recently, 300GHz wireless transmitters and receiver in 40nm bulk CMOS have been reported with several-tens Gb/s data rate [68–70]. However, these transceivers do not include any 300GHz amplifier. So far, the maximum gain frequency by bulk CMOS technology is up to 277GHz [71], and a 300GHz amplifier realized by a cheap bulk CMOS is highly demanded.

4.2.2 Sub-Terahertz Amplifier Considerations

The conventional sub-terahertz amplifiers [71–74] use the same approach to obtain maximum achievable gain (as described before in this chapter) from the transistor (Fig. 4.16). In this figure, the core part of the amplifier is shown. Transmission lines are used in order to satisfy the requirements for maximum achievable gain conditions. However, in this case, the gate and drain voltages of the transistor have to be same, which greatly degrades the desired NF, gain, $f_{\max}$, and linearity performances.

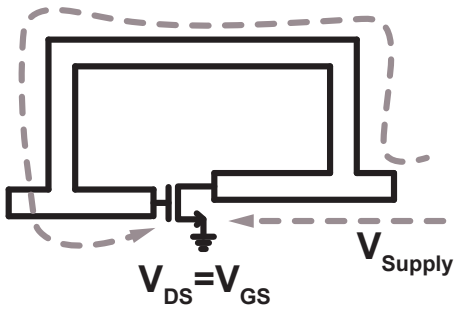


Figure 4.16: Conventional feedback CMOS amplifier circuit schematic for sub-terahertz amplifiers.

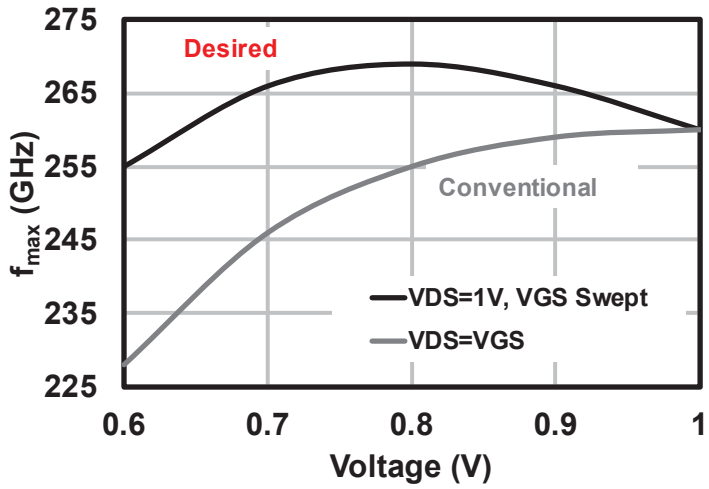


Figure 4.17: Comparison of f_{max} (GHz) for a transistor with a size of 6μm (1μm × 6) for $V_{DS} = V_{GS}$ (the conventional case) and for $V_{DS} = 1V$ & controllable V_{GS}.

Fig. 4.17 represents the comparison of f_{max} for two different cases in simulations. The gray line represents the conventional approach, for which $V_{DS} = V_{GS}$, no control over the gate bias for the transistors. The black line represents the f_{max} values for $V_{DS} = 1V$ and V_{GS} is swept from 0.6 to 1V. This case is desired for sub-terahertz amplifiers. It can be observed that maximum value is reached to be around 270GHz for the desired case when the gate bias is around 0.8V. On the other hand, for the conventional case, the maximum value is reached at 1V and is around 260GHz. There is 10GHz difference in f_{max} for the two different cases. f_{max} strongly affects the gain of the transistors. For example gain of the same transistor at 240GHz might differ 1 to 2dB because of the difference in f_{max}. Hence, higher f_{max} is desirable for higher gain. The power consumption per transistor should also be in mind. For higher f_{max}, conventional case dissipates more power than the desired case.

Fig. 4.18 represents the comparison of NF_{min} for two different cases in simulations. The simulations are done at 40GHz because the PDK transistors cannot represent accurate noise characteristics for mm-wave frequency region. The gray line represents the conventional approach, for which $V_{DS} = V_{GS}$, no control over the gate bias for the transistors. The black line represents the NF_{min} values for $V_{DS} = 1V$ and V_{GS} is swept from 0.6 to 1V. Considering LNA design, NF should be as minimum as possible and gain per stage should be as high as possible. Considering the f_{max} comparison along with NF_{min} comparisons, it is desired that the gate bias should be controllable such that the gate can be biased at minimum possible noise contribution per transistor and at the same

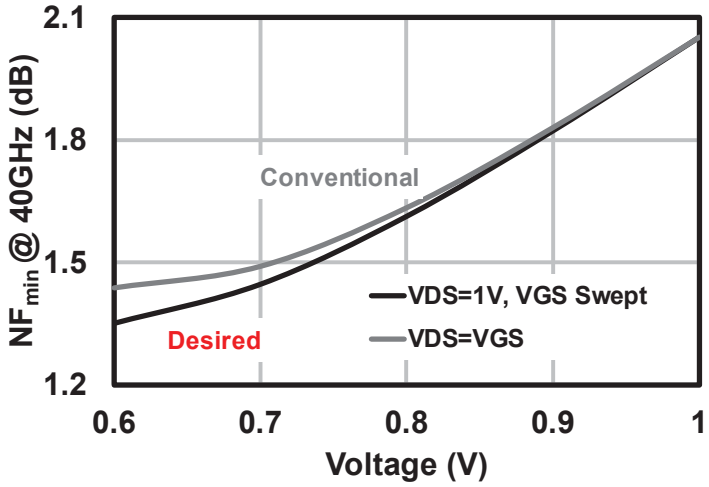


Figure 4.18: Comparison of NF_{min} (dB) at 40GHz for a transistor with a size of 6μm (1μm × 6) for $V_{DS} = V_{GS}$ (the conventional case) and for V_{DS} = 1V & controllable V_{GS}.

time higher gain can be satisfied. This case is desired for sub-terahertz amplifiers. The difference between the two cases are obvious for lower bias voltages. When the bias voltage increases, the difference between the two cases are not different in value.

Fig. 4.19 represents the comparison of OIP_3 for two different cases in simulations. The simulations are done at 240GHz since the f_{max} of the transistor can be maximum 270GHz, and gain is required from the transistor. The gray line represents the conventional approach, for which $V_{DS} = V_{GS}$, no control over the gate bias for the transistors. The black line represents the OIP_3 values for V_{DS} = 1V and V_{GS} is swept from 0.6 to 1V. Considering linearity of the amplifiers, OIP_3 should be as high as possible and gain per stage should be as high as possible. Considering the f_{max} comparison along with OIP_3 comparisons, it is desired that the gate bias should be controllable such that the gate can be biased for higher linearity per transistor and at the same time higher gain can be satisfied. This case is desired for sub-terahertz amplifiers since the SNDR requirements of the transceivers are very stringent at sub-terahertz frequency region. The difference between the two cases are obvious for lower bias voltages.

For these reasons, biasing scheme is a must considering sub-terahertz systems for which every dB counts for the performance. In order to realize a 300GHz amplifier with bias control scheme, the transistor layout and parasitics is to be optimized to reach higher f_{max} and hence, higher gain. Moreover, DC-cut capacitors, transmission lines and any other passive to be used in the amplifier are to be designed low loss. Fig. 4.20 shows

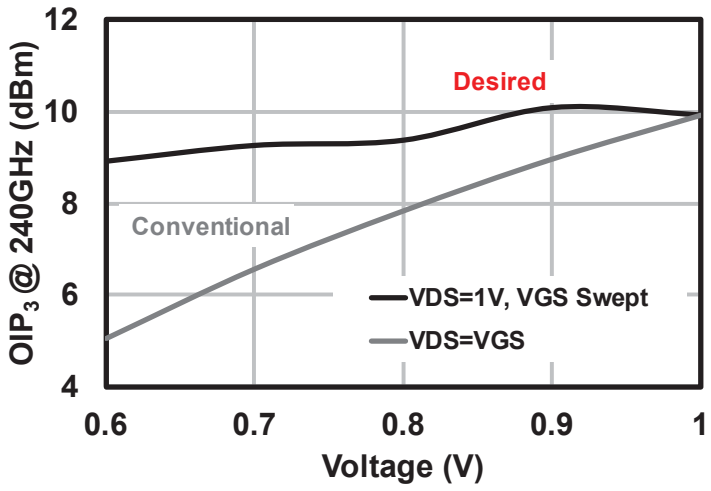


Figure 4.19: Comparison of OIP_3 (dBm) at 240GHz for a transistor with a size of 6μm (1μm × 6) for $V_{DS} = V_{GS}$ (the conventional case) and for V_{DS} = 1V & controllable V_{GS}.

the core circuit schematic of the desired sub-terahertz amplifier topology. Other than f_{max}, the corner gain frequency for the amplifiers should also be increased such that the gain for higher frequencies would be increased. In the next subsection, transistor layout optimization is discussed. Moreover, transmission line structure, model, and de-embedded transmission line characteristics are presented.

4.2.3 Device Considerations

Figure 4.21 shows the conventional (PDK) layout structure. The minimum channel length of 60nm and the finger width of 1.0μm is selected for higher gain peak. Fig. 4.22 presents the simulation results of maximum unity gain frequency for transistors biased at 0.7V of an 8 finger transistor with different gate widths. One can observe that the maximum unity gain frequency achieves peak for a transistor width of 1.2μm. On the other hand, maximum unity gain frequencies are very close for transistor widths from 1 to 1.3μm. For high gain at terahertz frequencies with smaller parasitics, 1μm transistor is selected. One of the main parasitics at terahertz frequency region is the drain to substrate junction capacitance, on which terahertz waves can easily couple to the substrate and hence the maximum available gain of the transistor decreases considerably. For this reason also, 1μm is a better choice for decreased junction capacitance. The source and drain connections are on second metal layer (M2) which is very close to poly contacts. Source and drain are connected via M1. Since only M2 layer is used for source and drain

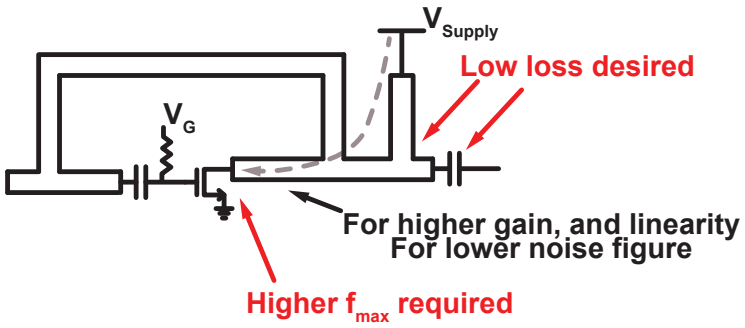


Figure 4.20: Desired feedback CMOS amplifier circuit schematic for sub-terahertz amplifiers.

connections, the resistance is high. The purple area represents the gate metal layer as third metal layer (M3). It surrounds the active area. The gate resistance in this case is high and considering sub-terahertz frequency regions the signal might have different delay time, for example, between the middle part source and drain connections and the end parts of the active area source and drain connections. Moreover, source and drain metal layer (M2) and gate layer metal layer (M3) are very close to each other resulting in higher gate-to-source and gate-to-drain parasitic capacitance.

Figure 4.23 shows the proposed layout structure. The transistor layout optimization is a key of higher frequency characteristics. The minimization of gate resistance is crucial for increasing the corner frequency between MAG and MSG. The minimum channel length of 60nm and the finger width of 1.0μm is selected for higher gain peak. In the proposed layout structure, the number of vias for gate node is increased, and the upper and lower electrodes are tied by M6. The number of vias are increased from one to four compared to conventional layout structure. By this way, via resistance simply decreased by a factor of four. To reduce the overlap capacitance between drain and gate, M2(drain) and M6(gate) are used in consideration of the trade-off between the overlap capacitance and via resistance. Wider metal layer is used for gate connections to decrease the resistance. Moreover, additional metal path is added between the upper and lower electrodes to reduce the gate resistance and to provide equal time delay for the active area source and drain connections. The metal layer selection and spacing is also carefully optimized based on post-layout simulation. Since the post-layout simulation is not reliable in millimeter-wave frequency region, the simulation is only used for rough layout optimization. The best high-frequency structure is selected based on the measurement result.

Fig. 4.24 shows the de-embedded measurement results of transistor gain

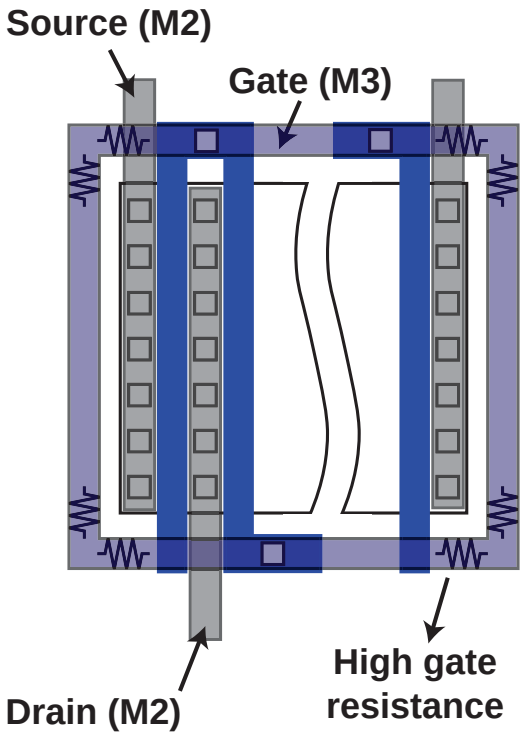


Figure 4.21: Conventional transistor layout.

characteristics in MAG and MSG for the different layout styles shown in Fig. 4.23 and Fig. 4.21. For this measurement, a vector network analyzer (Keysight N522A) with J-band extenders (VDI WR3.4-VNAX) is utilized with two waveguide probes (Cascade Microtech Infinity I325-T-GSG-50-BT) for on-wafer measurement. In this comparison, VDS and VGS are set to 1.0V and 0.7V, respectively. The conventional (PDK) and proposed layout styles are compared both for 1μm finger width and 8μm total channel width. The MSG is not very different for all the layout structures, which is 4.94dB at 240GHz. However, the significant difference can be observed for the corner frequency and the maximum operation frequency, which are around 250GHz and 270GHz for PDK, and are extended up to 270GHz and 317GHz for the proposed structure.

Fig. 4.25 shows the de-embedded measurement results of MAG and MSG for the different sizes for the optimized transistor layout. Different channel widths of 8μm, 10μm, 20μm and 30μm are compared with the same finger width of 1μm, which have $f_{\max}$ of 317GHz, 310GHz, 292GHz, and 278GHz, respectively.

Figure 4.26 shows the low-loss transmission-line structure. The line width and ground structure is optimized for 50Ω characteristic impedance based on EM simulations. Several

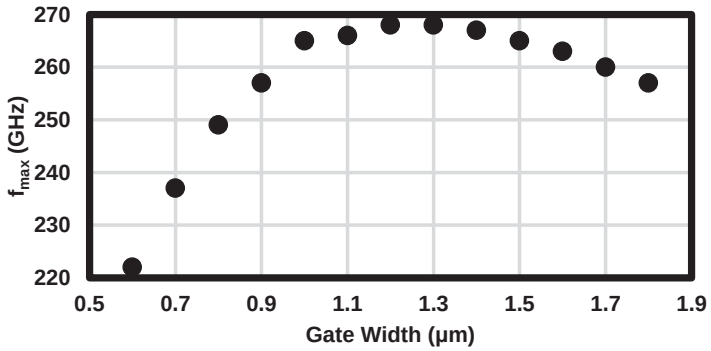


Figure 4.22: Maximum unity gain frequency vs. gate width.

different structures were once fabricated, and the best structure shown in Fig. 4.26 is selected for lower insertion loss. For the measurement, a 25μm × 40μm pad is used for lower parasitic capacitance. For the S-parameter measurement, the same network analyzer is used as the transistor measurement. The multi-line TRL method is utilized for the de-embedding, and the transmission-line lengths of 200μm, 400μm, 1900μm, and 3800μm are used in this modeling. The measured characteristic impedance (Fig. 4.27) is 50Ω at 300GHz, and the loss factor (α) of the transmission line is 2.77dB/mm at 300GHz (Fig. 4.28). Q calculated from α and β (Fig. 4.29) is 20.6 at 300GHz. Bend and junction structures were also fabricated once, and are characterized based on the measurement results.

4.2.4 Design of Sub-Terahertz CMOS Amplifier

Fig. 4.30 shows the details of the designed 300GHz amplifier. A transmission-line based layout style is applied. Layout of the amplifier is designed to be compact with 16-stage. Wideband 2Ω RF and DC isolation transmission lines are employed for the DC feed with a length of 150μm. Additional 2Ω RF resistors are connected between the decoupling transmission line and the DC feed network to provide more isolation and to ensure the stability factor would not be a problem. Used transistor in this case has a total width of 8μm (1μm×8) with the optimized layout since it has the highest $f_{\max}$ and highest corner frequency. Input port of the overall amplifier is matched with short-circuited stub network. Every core os the stages are same design. Except for compact layout purposes the secon one is the horizontally mirror version of the first one. Detailed transmission line lengths are included in the same figure. The output matching network of the amplifier is based on the open-circuited stub network. The capacitors are fringe based and they

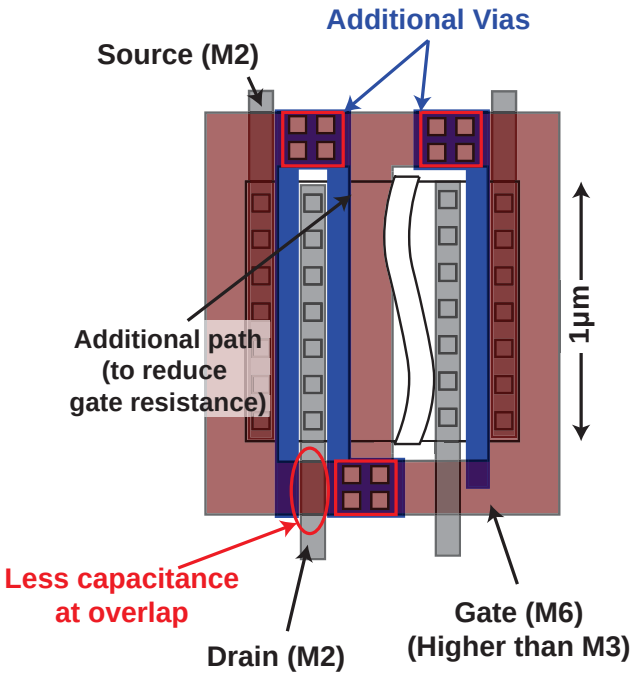


Figure 4.23: Optimized transistor layout.

have much lower loss in comparison with MOM capacitors. The fringe capacitor layout illustration is also given in the same figure.

4.2.5 Measurement Results

The proposed 300GHz CMOS amplifier occupies a total area of $1.12\text{mm}^2 = 0.8\text{mm} \times 1.4\text{mm}$ in 65nm standard bulk CMOS process. The die photo is shown in Figure 4.31. Two ground eight power DC pad (GP8G) is used for the supply voltage and gate bias control. DC pads are located at the top of the chip. Two of the power pads are used for the DC supply (VDD=1V). Four of them are used for the gate bias control. As it can be observed from the figure that the amplifier has a very compact area occupation thanks to the mirroring for one of the two stages. Input RF pad is located at the left hand side of the figure and the output pad is located at the right hand side of the figure. To provide DC supply to lower side of the chip, transmission lines with a DC feed crossings are used after the input pad and before the output pad.

Fig. 4.32 shows the measured S-parameters and stability factor. For the S-parameter measurement, the same network analyzer is used as the transistor and transmission-line measurement. The measured power gain S21 is 0dB at 273GHz, 5dB at 274GHz, 10dB at

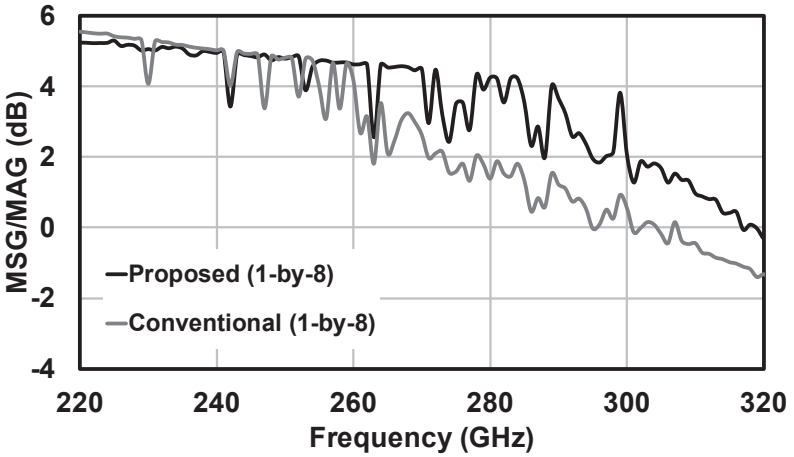


Figure 4.24: MAG/MSG comparisons of different layout transistors (PDK and proposed).

276GHz, 13dB at 290GHz, 18dB at 297GHz, 21dB at 298GHz as peak, 5dB at 300GHz, and 0dB at 301GHz. The input and output return losses S11 and S22 are plotted in both Smith chart and dB-plot, and good impedance matching can be confirmed for both input and output. The plots in Smith chart is also from 260GHz to 320GHz. The noise floor caused by the VNA is around -30dB to -45dB according to Fig. 4.32. The stability factor is calculated from the measured S-parameters, which is 1.079 at 298GHz. For the power measurement, an up-conversion mixer (VDI WR3.4SHM) as a source and an Erickson power meter (VDI PM5) are used. A 156GHz LO signal for the mixer is generated by a frequency tripler (VDI WR6.5x3HP, 110-170GHz) with a driver amplifier (Quinstar QPW-50662030-C1, 20dBm for 50-66GHz). The output power from the mixer is once measured by the power meter through the probes, and the probe loss is subtracted. The saturated output power of the proposed amplifier is -11.70dBm at 295GHz. The power measurements have to be repeated due to some issues during measurement setup.

4.2.6 Conclusions

Table 4.4 shows a performance comparison with the state-of-the-art sub-terahertz CMOS amplifiers [71–74]. The proposed amplifier achieves the highest gain frequency among all the bulk CMOS amplifiers owing to the optimum biasing scheme. The upper band of gain frequency is 300GHz in this work, and the maximum operation frequency $f_{\max}$ is optimized to be 317GHz. The ratio of the upper frequency to $f_{\max}$ is the highest record of 0.95. The total power consumption for the 16 stages is 35.4mW from 1-V supply, and each stage consumes only 2.2mW.

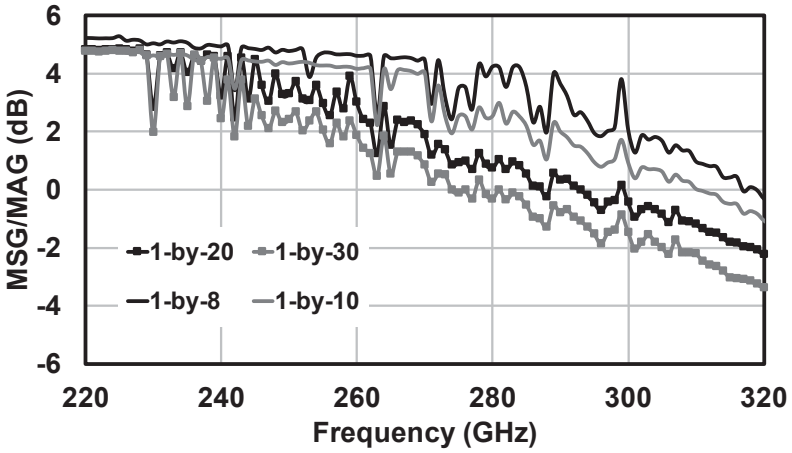


Figure 4.25: MAG/MSG comparisons of different size transistors based on the proposed layout optimization.

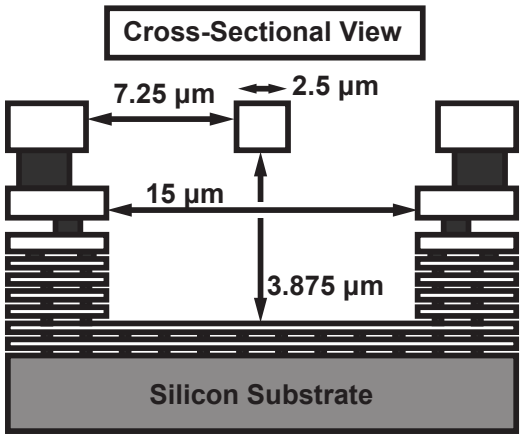


Figure 4.26: Low-loss transmission line structure from cross-sectional view.

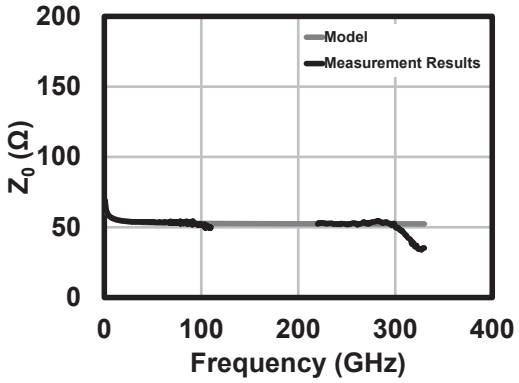


Figure 4.27: Low-loss transmission line characteristic impedance model and de-embedded results comparison up to 330GHz.

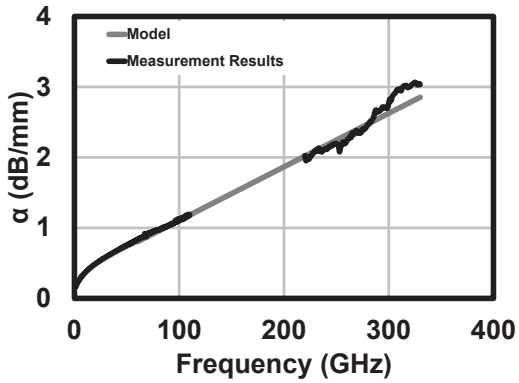


Figure 4.28: Low-loss transmission line loss factor (α) model and de-embedded results comparison up to 330GHz.

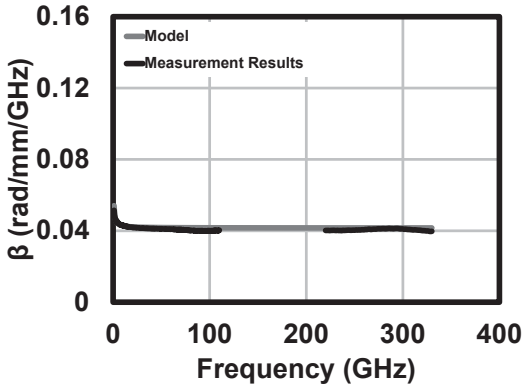


Figure 4.29: Low-loss transmission line propagation constant (β) model and de-embedded results comparison up to 330GHz.

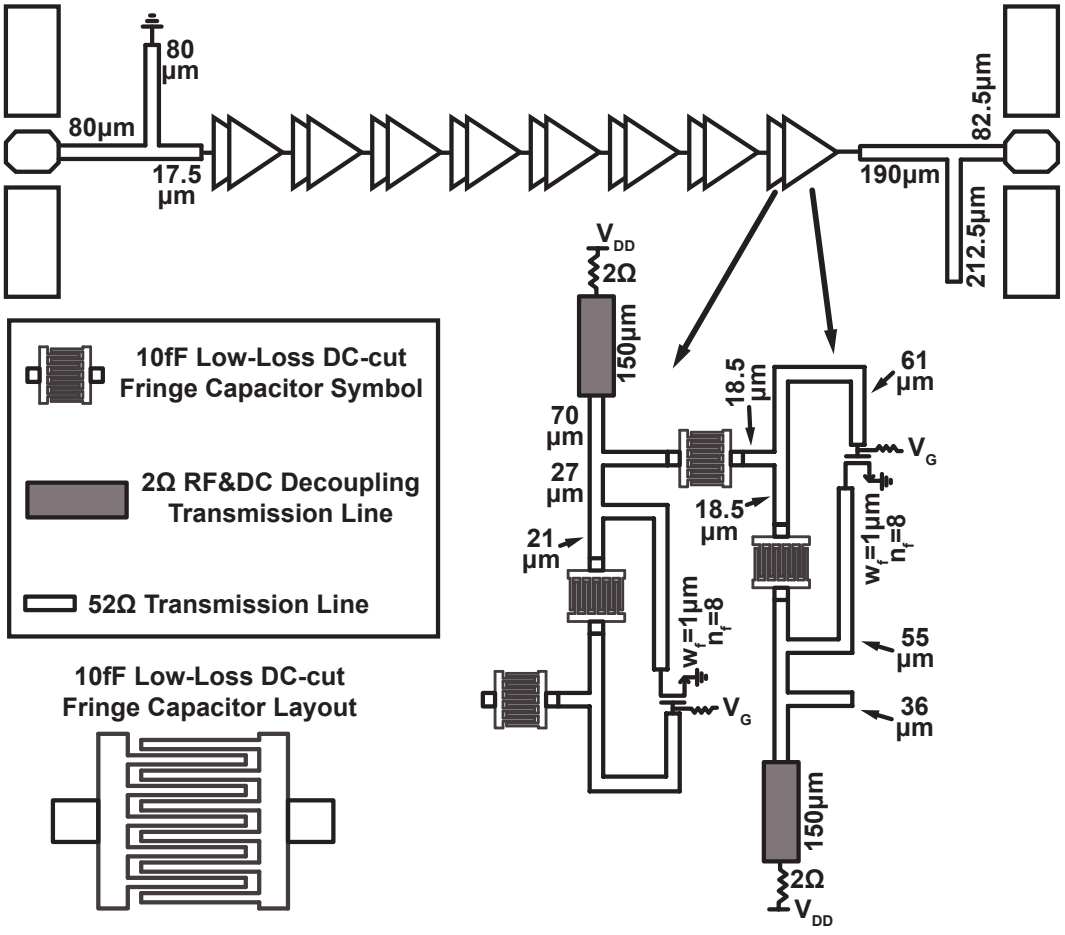


Figure 4.30: Details of the designed 300GHz amplifier.

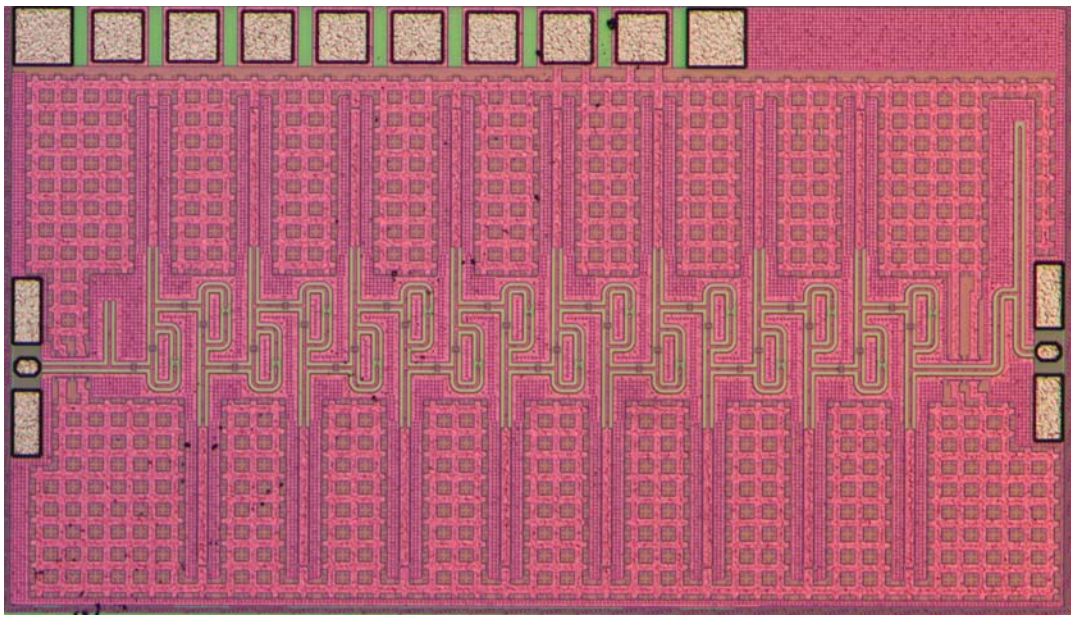


Figure 4.31: Die photo.

Table 4.4: Comparison of sub-terahertz CMOS amplifiers.

Ref.	Frequency [GHz]	Technology	V_{DS} [V]	V_{GS} [V]	f/f_{max}	P_{DC} [mW]	Gain [dB]
[1]	245-277*	65nm CMOS	0.8		0.82	15	10
[2]	244-268*	65nm CMOS	1		0.78	27.6	9.2
[3]	220-270*	65nm CMOS	0.85		0.78**	23.8	13.9
[4]	305-325*	28nm FDSOI	0.7		0.77	28	4.5
This Work	273-301	65nm CMOS	1.2	0.62	0.94	35.4	21

* Estimated from graphs in the respective literature.
** Calculated assuming f_{max} is 345GHz.
[1] Y. Yagishita, et al., APMC2015 [2] H. Bameri, et al., JSSC2017
[3] D.-W. Park, et al., VLSI2017 [4] D. Perveg, et al., GSMM2016

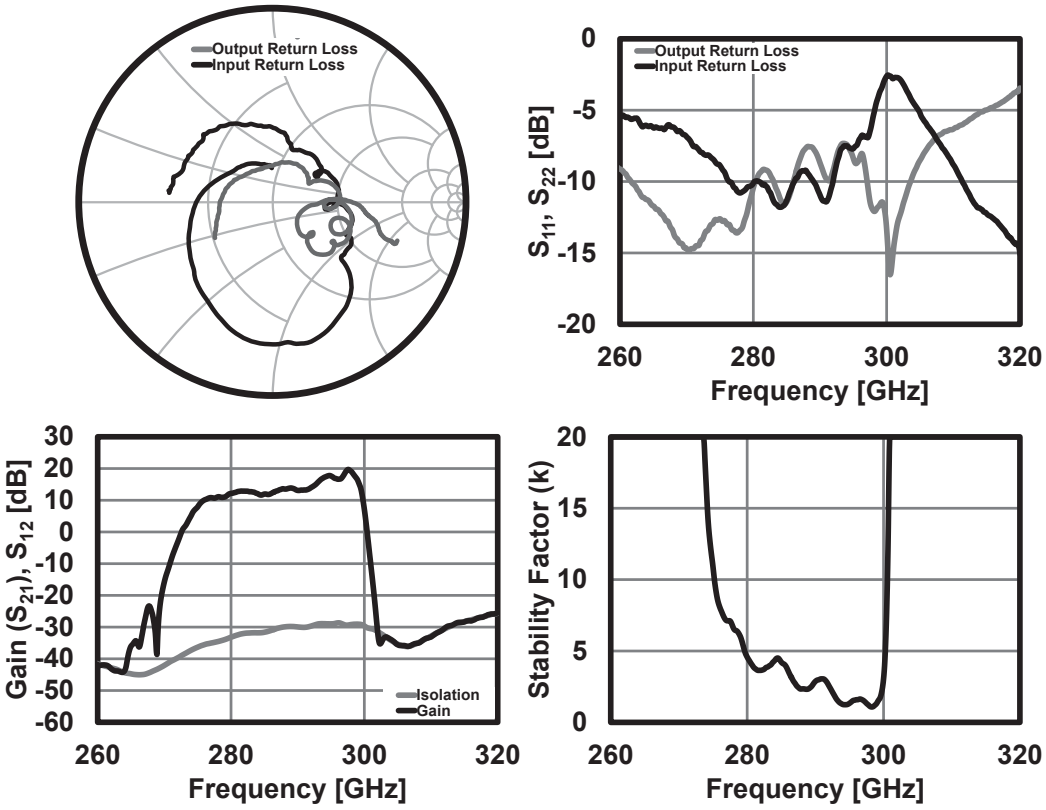


Figure 4.32: S-parameters measurement results from 260 to 320GHz.

4.3 Asymmetrical Bi-Directional LNA/PA

As mentioned before, MIMO systems are being considered in 60GHz by several standards. For instance, with 4-by-4 MIMO using 60GHz TRXs capable of 4-channel bonding using 16QAM around 112Gbps can be achieved. However, MIMO systems are costly in terms of chip area and number of antennas required. Hence, it is necessary to decrease cost. Conventional Bi-Directional transceivers either use SPDT switches between LNA and PA aiming to decrease the number of antennas. Others use bi-directional amplifiers with same gain, noise and linearity characteristics for both ways, hence does not reflect LNA and PA requirements for a wireless link. In here, a 60GHz single-ended bi-directional power/low-noise amplifier for TDD is proposed.

Fig. 4.33 represents the schematic of the asymmetrical bi-directional LNA/PA. Positive feedback is used based on transmission lines. The placement of positive feedback transmission line in each stage changes the gain boosting either for LNA mode or PA mode. In the first stage at the antenna port, the positive feedback is used to boost the gain of LNA mode, because the LNA gain at the first stage has to be higher in order to decrease the overall noise figure of the LNA and hence the whole receiver.In each stage transistor sizes are different based on the requirements of LNA mode or PA mode. For instance, the last stage of the PA, the closest stage to the antenna port has wider transistor width compared to the previous four stages. Overall the bi-directional amplifier has five stages.

The designed asymmetrical bi-directional LNA/PA is manufactured on 65nm bulk CMOS. The layout of the designed amplifier is presented in Fig. 4.34. The total area is $0.82mm^2$, with a width of 0.63mm and a height of 1.3mm.

Measurement results are presented in Fig. 4.35 based on VNA measurements. The results show that different gain requirements can be achieved and the gain of LNA mode is around 20dB maximally. Isolation results are less than -50dB which might be the one of the concerns for a bi-directional amplifier. Return losses are also around 10dB in the band of interest and hence different matching conditions can be satisfied for a TDD system.

Moreover, stability factor results are presented in Fig. 4.36. For an amplifier designed based on positive feedback, the stability factor is more than 30 which ensures the stability of the amplifier in both LNA and PA mode.

This approach can be a great candidate for short-range wireless communications; such as personal area networks. Using full CMOS solutions, the cost of the overall system can be decreased considerably by decreasing the number of antenna by half and the silicon area consumption more than half.

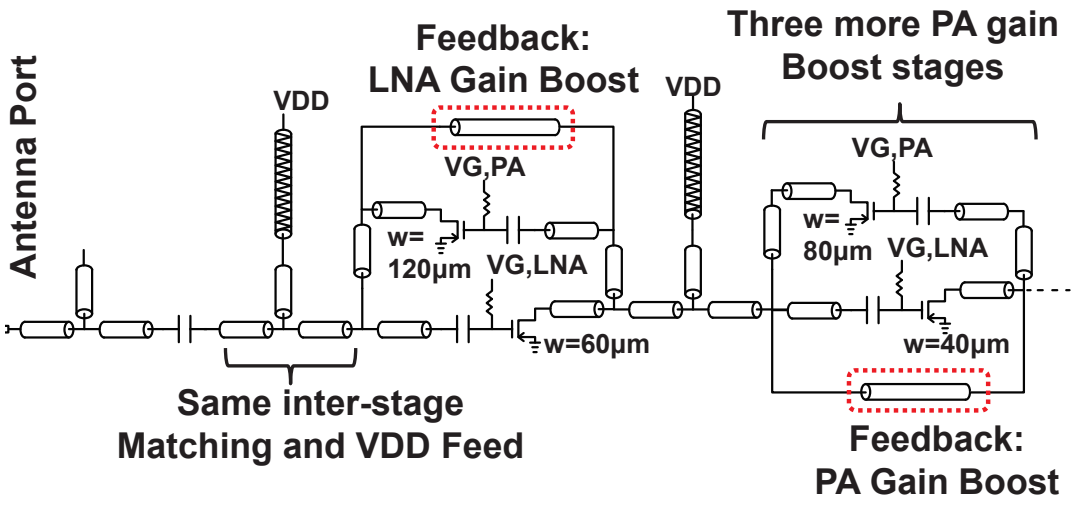


Figure 4.33: 60GHz Asymmetrical Bi-Directional LNA/PA schematic.

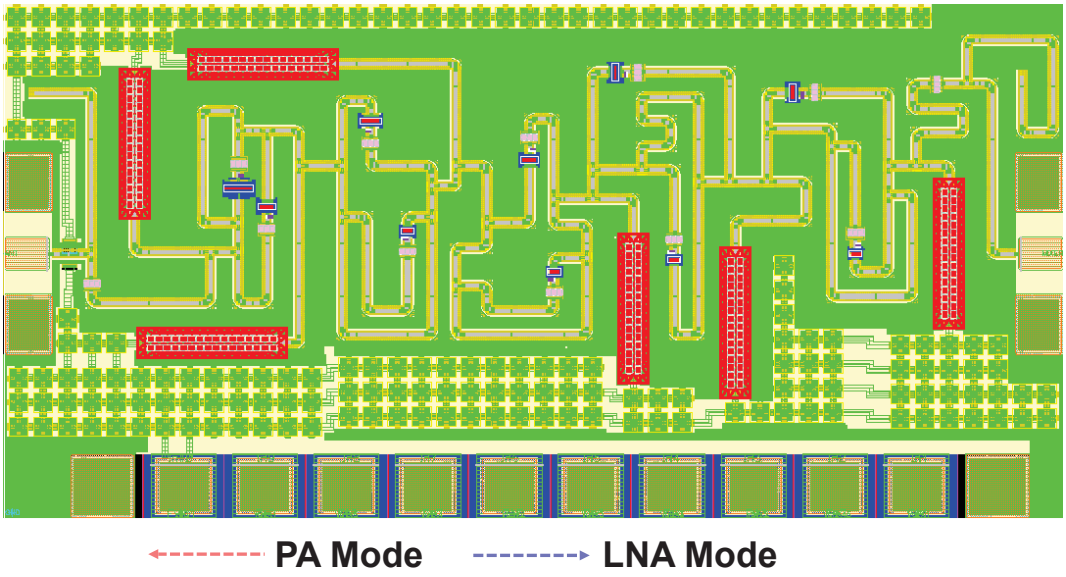


Figure 4.34: 60GHz Asymmetrical Bi-Directional LNA/PA Layout on 65nm bulk CMOS. The area is 0.63mm by 1.3mm.

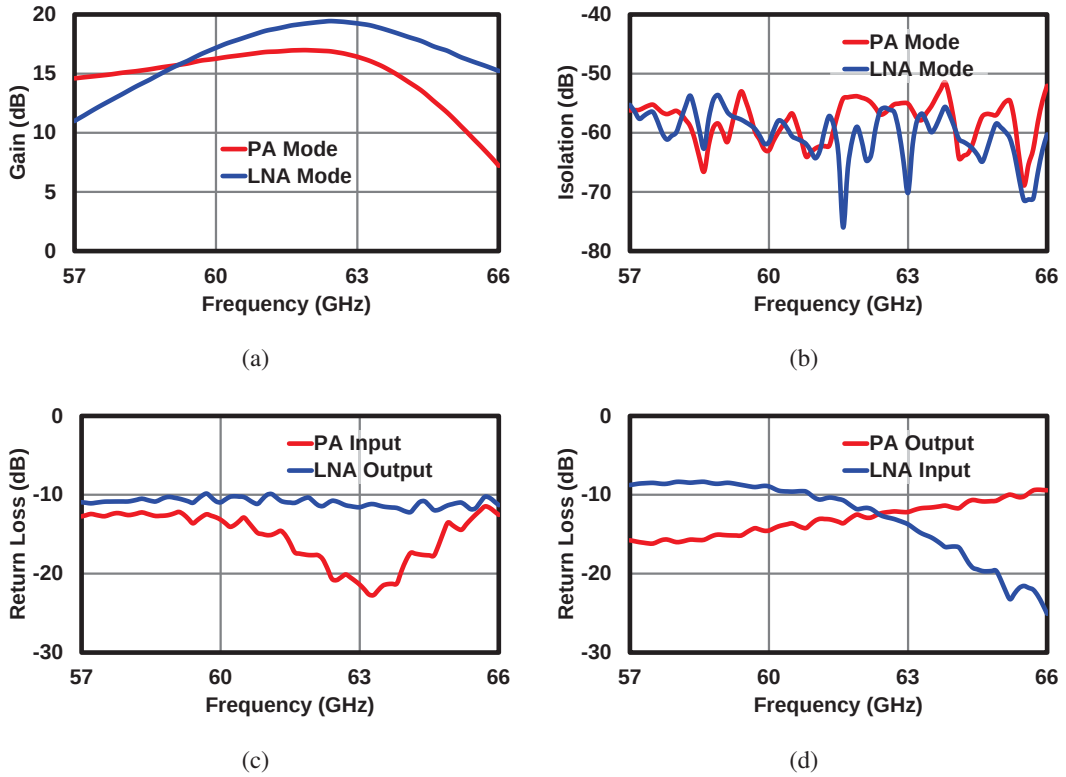


Figure 4.35: Asymmetrical bi-directional LNA/PA measurement results (a) gain, (b) isolation, (c) RL for LNA output and PA input (mixer connection port), and (d) RL for LNA input and PA output (antenna connection port).

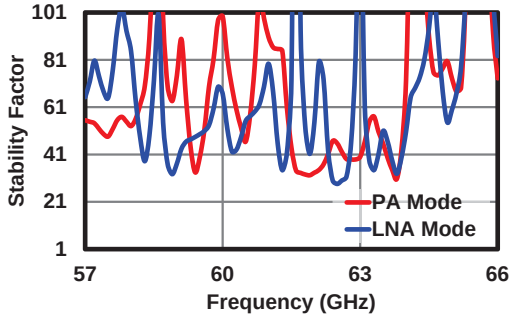


Figure 4.36: Stability factor measurement results for the bi-directional amplifier.

Chapter 5

Ultra-High Data-Rate Frequency-Interleave Transceiver

5.1 Introduction

In order to achieve more data-rate wider bandwidth with higher order modulations is required. Hence, a careful selection of operating frequency, bandwidth and modulation is necessary. The selection process is explained in Chapter 2. In here, W-band frequencies are selected and the transceiver is designed according to this selection. Wider bandwidth is necessary for higher data-rate. For instance, 25GHz bandwidth with 16QAM modulation would result in 100Gb/s data-rate. The requirements on ADCs, DACs, and baseband circuitry are stringent for such a high-bandwidth and higher order modulations while considering a wireless communication system in terms of power consumption, silicon area cost and etc. as a whole. Hence frequency-interleave transceiver architecture is employed in here. More details on reasoning, the issues of the architecture and how to solve them are explained in this chapter. The W-band transceiver, and details about the designed circuits blocks are described in this chapter. A custom test module working at W-band is introduced.

5.2 Frequency-Interleave Transceiver

As it is already mentioned above, 25GHz bandwidth is too wide for a wireless system. Fig. 5.1(a) shows the conventional approach. Two times oversampling is generally required for better EVM and relaxed design of low-pass filter (LPF). Hence, I/Q DACs have to work around 50GS/s and to be 8-bit at least for 25GBaud of data with 16QAM. As the required sampling rate, resolution and bandwidth increase, the power

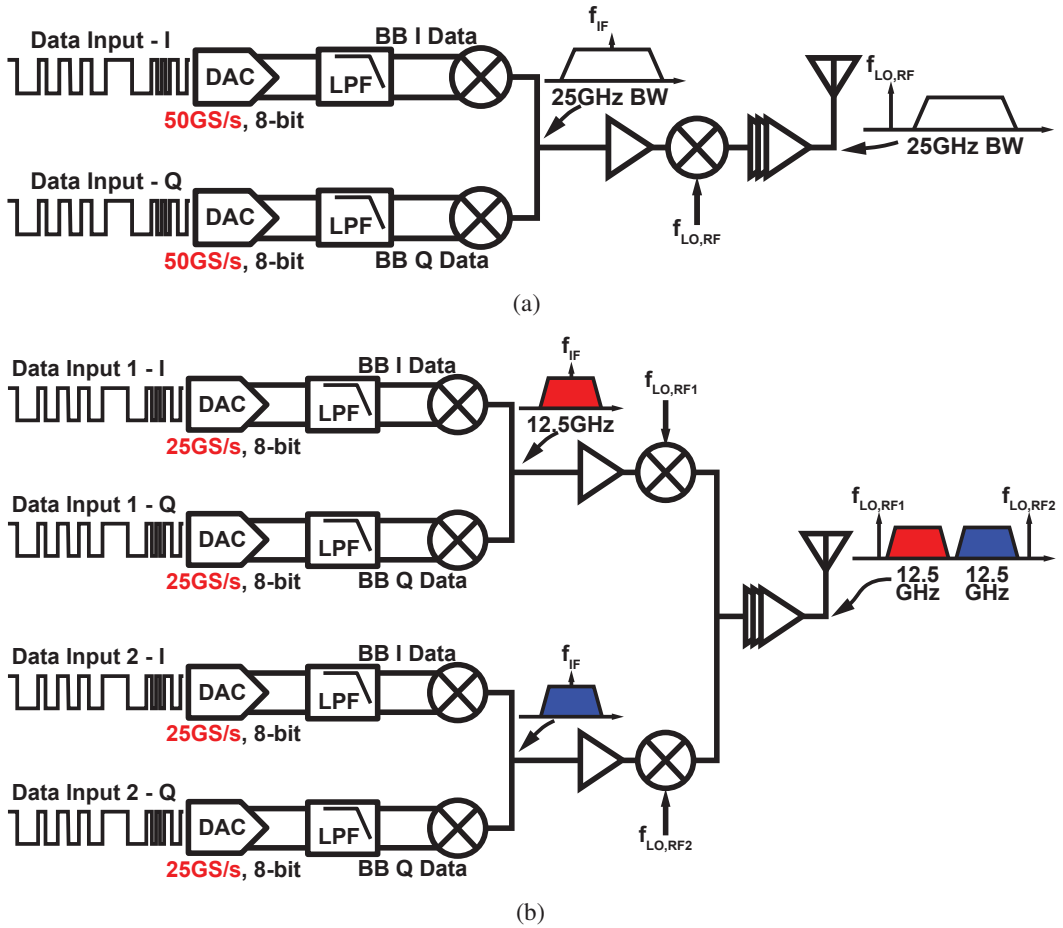


Figure 5.1: Architectures for ultra-wideband transceivers; (a) conventional single stream approach, and (b) frequency-interleave transceiver architecture for relaxed baseband design.

consumption and area increase considerably [75, 76]. Jitter requirements for high-speed converters are stringent [77]. The same issues are there for ADCs [78, 79]. As the bandwidth and resolution of ADCs, DACs, and digital baseband increases, the power consumption and silicon area consumption increase considerably. Hence, to relax the system, frequency-interleaving is employed. Fig. 5.1(b) illustrates the TX. In this work, sampling rate for ADCs and DACs can be halved, and as a result, the power, bandwidth and silicon area consumption can be relaxed.

However, frequency-interleave TRX has several issues to be solved. First of all, as shown in Fig. 5.1(b) two LO signals are required from IF-to-RF and vice versa. A direct approach would be to implement two fundamental signal millimeter-wave PLLs for $f_{\mathrm{LO,RF1}}$ and $f_{\mathrm{LO,RF2}}$. One advantage of this approach is that no harmonics are generated

for LO signals. However, for millimeter-wave the quality factor of the passives is an issue and as a result the phase noise increases for LO signals. For an ultra-wideband system phase noise is an important factor which limits the quality of the communication (limits the SNDR). By implementing two PLLs, the area and power consumption would increase. In here, frequency multiplier approach is used to generate two LO signals from a lower frequency source (or a PLL in a complete system). In this case, the power and silicon area consumption is smaller than the previous approach. However, since the frequency multipliers are used, one has to be very careful about the harmonic generation. Undesired harmonics would cause the SNDR to be degraded and the requirements may not be met. In here, frequency multiplier approach is adopted and for this reason, the issue of these harmonics on a frequency-interleave transceiver is investigated below in detail considering harmonics.

Fig. 5.2(a) represents frequency-interleave TX with LO signals generated from f_{LO} = 20GHz by-3 (60GHz) and by-5 (100GHz). By this way, enough bandwidth is left between two LO signals for ultra-high data-rate communications. Nevertheless, in this case, from both multipliers the 4^{th} harmonic (80GHz) generated in-band causing in-band up-conversion. At the output of low-band (LB) mixer, $f_{IF,LB}$ signal is up-converted to $3f_{LO} - f_{IF,LB}$ and $3f_{LO} + f_{IF,LB}$. Up-converted $3f_{LO} - f_{IF,LB}$ signal is suppressed thanks to the bandpass gain characteristics of PA, and desired $3f_{LO} + f_{IF,LB}$ signal remains. However, due to the in-band 4^{th} harmonic, there are additional two signals. It is similar for high-band (HB). PA output is shown as in Fig. 5.2(b). The undesirable in-band signals greatly deteriorate SNDR. Fig. 5.2(c) illustrates the wideband representation. Black colored data is the summation of undesirable LB and HB data due to 4^{th} harmonic. To solve this issue, lower multiplication factors by-2 and by-3 should be used as given in Fig. 5.3 showing that there is no in-band distortion. However, it is still important to suppress the unwanted harmonics, e.g. fundamental and 3^{rd} harmonic from doubler, and fundamental and 2^{nd} harmonic from tripler. Otherwise, an effect similar to Fig. 5.6 cannot be avoided.

The in-band LO harmonics are, also, an issue on RX. Fig. 5.4 represents this issue. Note that IF amplifiers suppress higher frequencies. For the LB output of RX, the desired signal is $f_{RF,LB} - 3f_{LO}$; similarly, $f_{RF,HB} - 5f_{LO}$ is the desired signal for HB output. Other unwanted signals generated by $4f_{LO}$ lay on the required data. Fig. 5.5 illustrates this work using doubler and tripler. In this work, LO generation is done by doubler and tripler.

Furthermore, it is important to isolate LB and HB parts for both TX and RX. Without proper isolation, there are cross-modulation issues. Fig. 5.6 shows the case for TX. The mixers used in this work is assumed to be passive, and RF-to-LO isolation at mm-wave is about 10dB for passive mixers. Hence, LB LO couples to the HB mixer LO port,

and HB LO couples to the LB mixer LO port. This results in additional up-conversion, and TX SNDR degrades. Fig. 5.7 illustrates the LB and HB outputs of RX with poor isolation between two branches after LNA. In this work, isolation between LB and HB can be increased about 15dB using one-stage RF amplifiers. This effort decreases the coupled LO by 25dB in total. Moreover, TX LO leak should be canceled to decrease cross-modulation.

High TX LO leak cause several problems. Most common ones to be known are the linearity degradation for TX, and radiating high power in adjacent bands. For a frequency-interleave TX, it also causes cross-modulation. Addition to these, high LO leak from TX can cause cross-modulation on RX. Fig. 5.8 illustrates this issue. These LO leaks are radiated from TX and couples to the RX mixers LO drives and results in additional down-conversion. Hence, LO leak cancellation on TX is crucial for both TX and RX. This issue is solved with employing single-IF balanced mixer and explained in subsection 5.4.3.

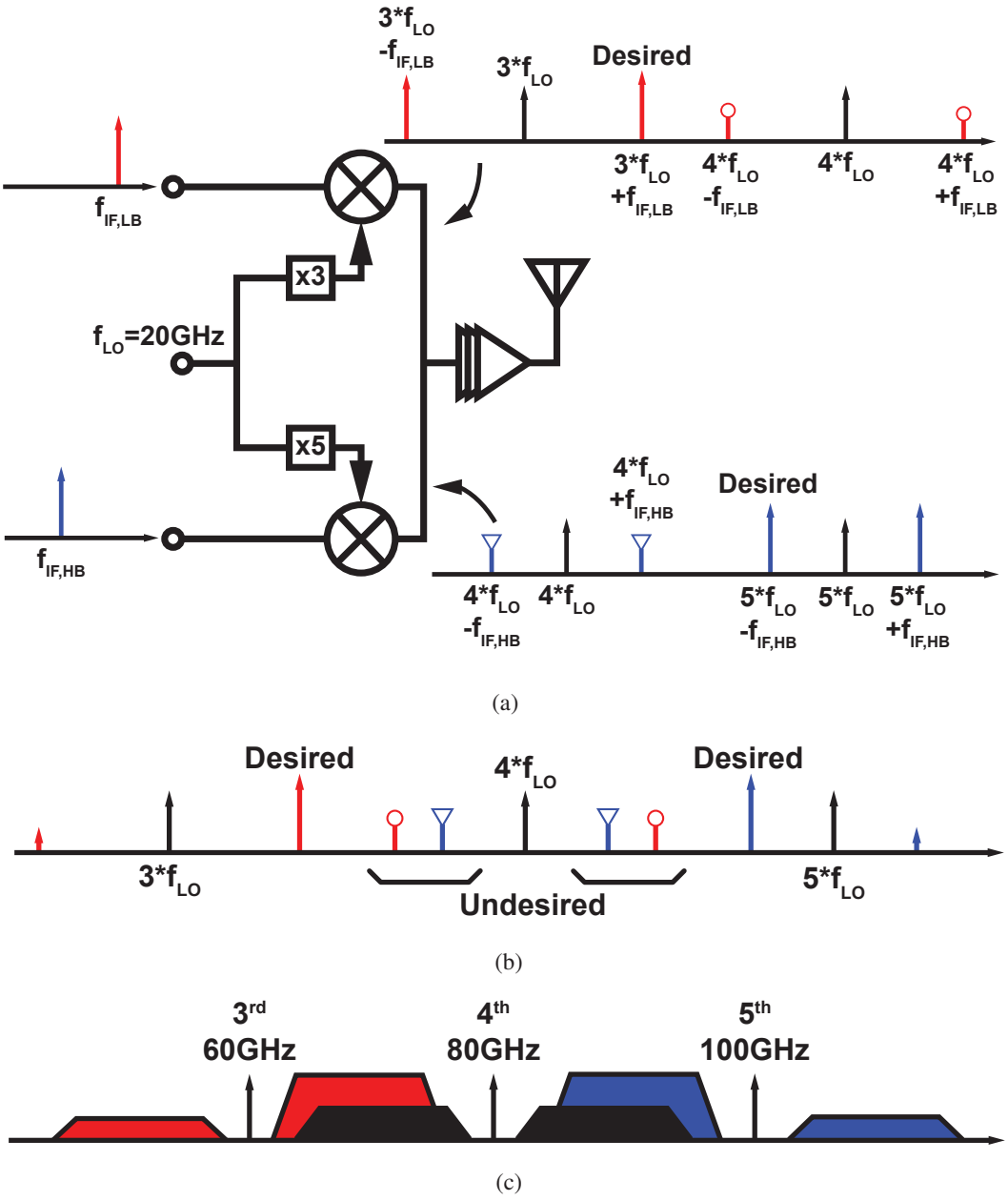


Figure 5.2: LO signal generation for a frequency-interleave transmitter, (a) using one LO with multiplication-by-3 and by-5 which cause in-band modulation due to in-band LO harmonics, and (b) transmitter output tone representation of up-conversion with in-band LO harmonics and modulations, and (c) transmitter output wideband signal representation.

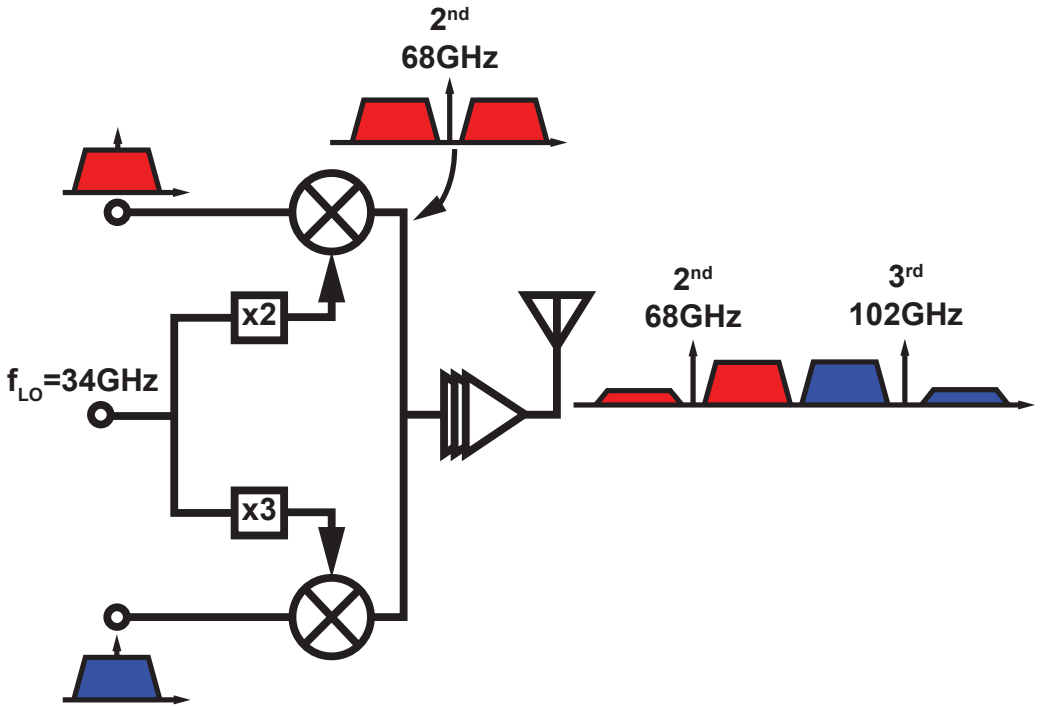


Figure 5.3: This work LO signal generation for a frequency-interleave transmitter with least frequency multiplication by-2 and by-3 eliminating in-band generated harmonics and modulation.

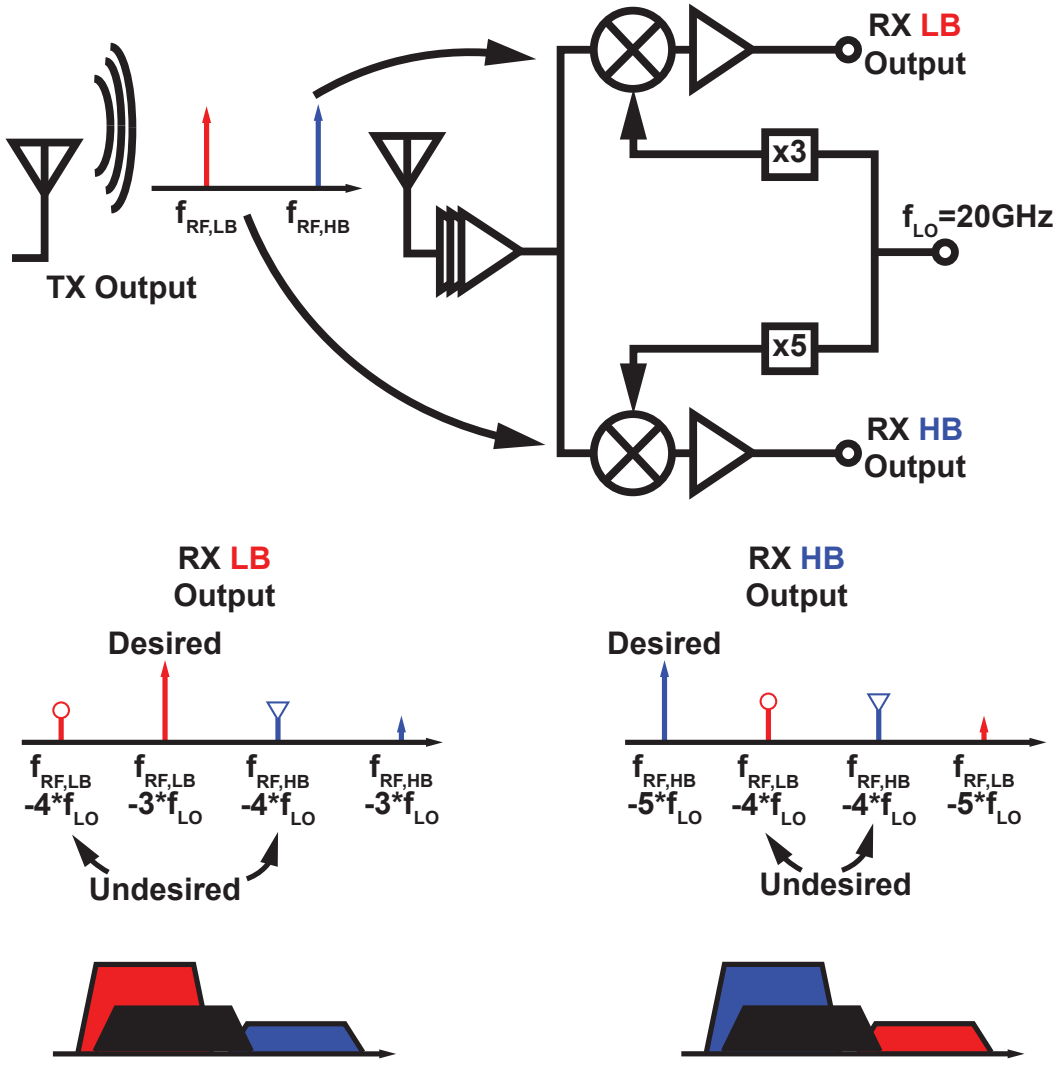


Figure 5.4: LO signal generation for a frequency-interleave receiver using one LO with multiplication-by-3 and by-5 which cause additional in-band down-conversion due to in-band LO harmonics. LB and HB outputs are shown.

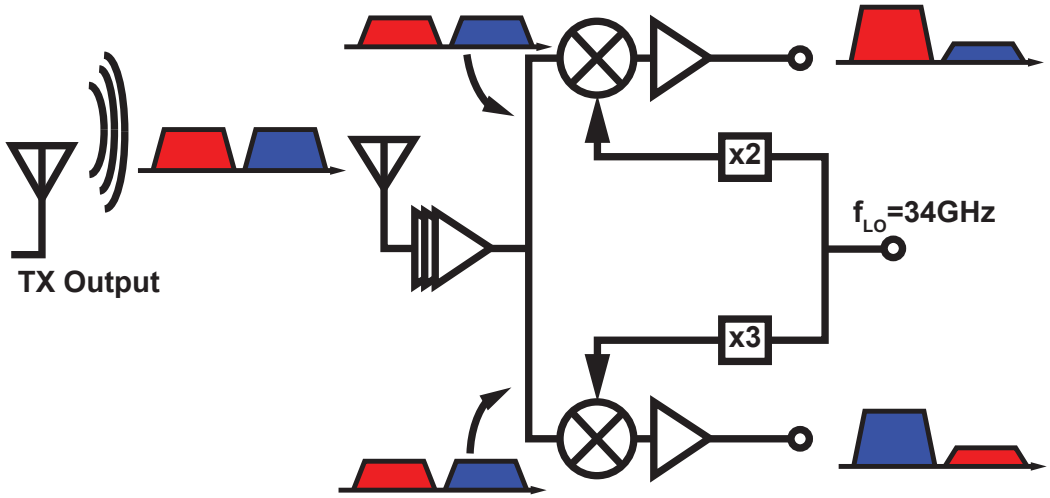


Figure 5.5: This work LO generation for receiver side with least frequency multiplication factors by-2 and by-3 eliminating in-band generated harmonics and modulation.

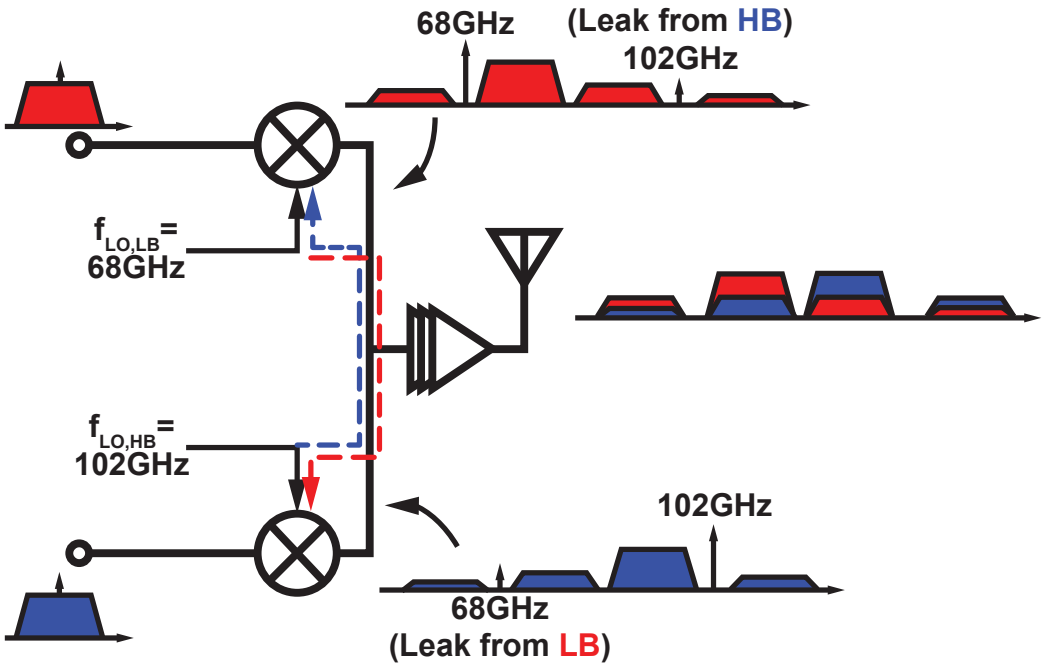


Figure 5.6: The effect of cross-modulation on transmitter due to low isolation between LB and HB.

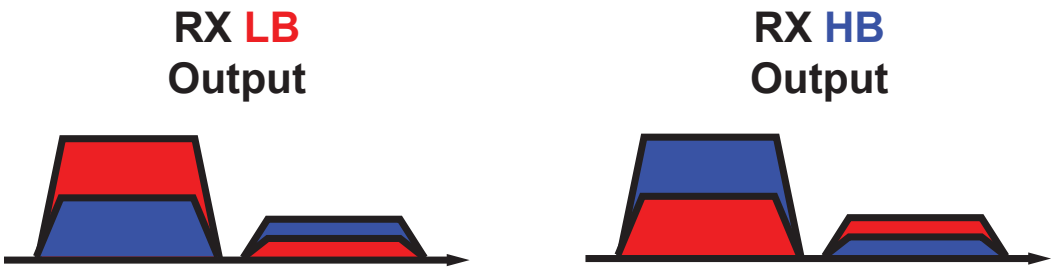


Figure 5.7: LB and HB IF output spectrum representation of RX, due to low isolation between LB and HB after LNA.

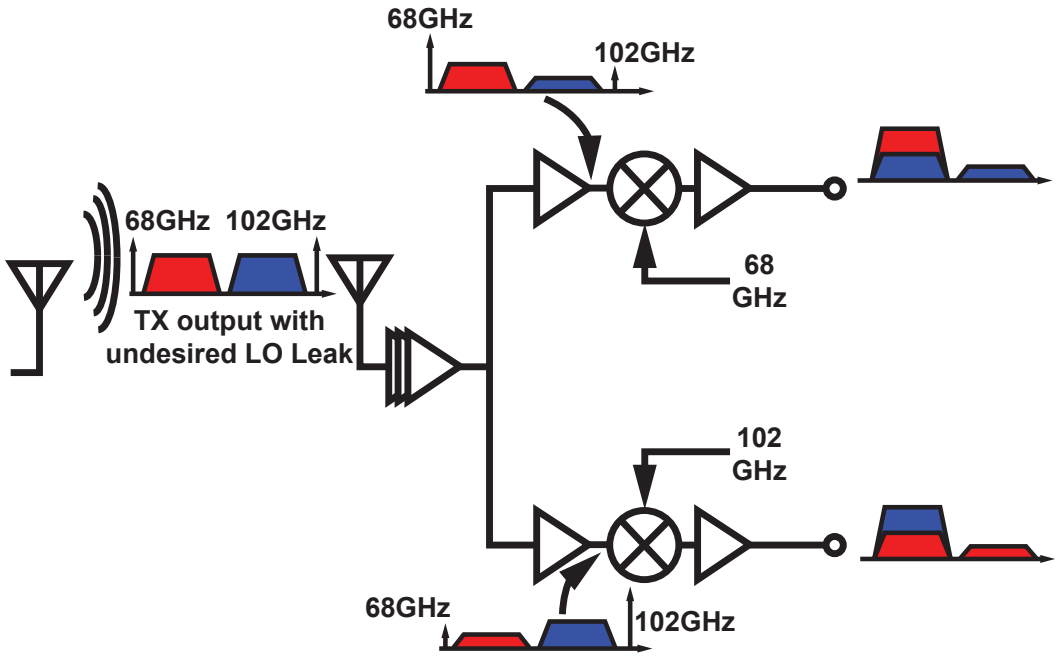


Figure 5.8: Cross-modulation on RX side due to undesirable LO leak from TX.

5.3 W-Band Transceiver

In considerations of the issues described above and the requirements for an ultra-high data-rate wireless communication, the W-band TRX is designed and constructed as illustrated in Fig. 5.9. The data-streams are up- and down-converted with 70GHz and 105GHz LO signals. LB and HB IF signals lie from 0.3 to 17.2GHz with a center frequency of 8.75GHz. Hence the up-converted LB signal lies between 70.3 to 87.2GHz frequency region, and similarly, up-converted HB signal lies between 87.8 to 104.7GHz frequency region. PA is six-stage and works from 70 to 105GHz. Last five stage is positive-feedback CS (PFCS) whereas the first stage is designed as CS to ensure more isolation and hence the stability of the amplifier. The RX has a five-stage PFCS LNA working from 70 to 105GHz. The output of LNA is divided into two paths and one-stage PFCS RF amplifiers follow. LB RF amplifier works from 70 to 87.5GHz and HB RF amplifier works from 87.5 to 105GHz. The gain characteristics of TX RF amplifiers, PA, LNA and RX RF amplifiers help to suppress the up-converted sidebands such as before 70GHz for LB and after 105GHz for HB.

The TX side RF amplifiers, also, designed separately. LB side of TX RF amplifier is just one-stage resistive feed-back CS topology. Since mixer-first TX architecture is adopted in here, resistive feedback RF amplifiers are employed to satisfy wideband matching at inputs of TX [80]. On the HB side of TX, there is additional RF amplifier stage to increase the gain. This is to satisfy same level of gain for both LB and HB branches after the mixers. The detailed design information for mm-wave amplifiers is given in section 5.4.1.

A frequency doubler and a tripler are used to generate up- and down-conversion 70 and 105GHz LO signals from a 35GHz external source. 70GHz is generated using doubler. Transistor non-linearity is used to generate the 2^{nd} harmonic. Transistor for the doubler is 12μm (w_f = 2μm, n_f = 6) and biased at 0.35V having maximum second-order non-linearity, and relatively lower 3^{rd} harmonic product. Doubler has two-stages of LO buffer designed at 70GHz. These buffer stages has two main duty and designed as narrowband; one of which is to increase the LO power to around 0dBm, and suppress the fundamental and 3^{rd} harmonic. Output of buffers divided into two with almost equal power for RX and TX mixer LO inputs. 105GHz is also generated by transistor non-linearity. Transistor for the tripler is 40μm (w_f = 2μm, n_f = 20) and biased at 0.2V having maximum third-order non-linearity and relatively lower 2^{nd} harmonic. For the case of tripler, three-stage buffer is required since the conversion loss is more. Again, buffers are designed narrowband to suppress the fundamental and 2^{nd} harmonic. Output of buffers divided into two for RX and TX mixer LO inputs. Nevertheless, an additional

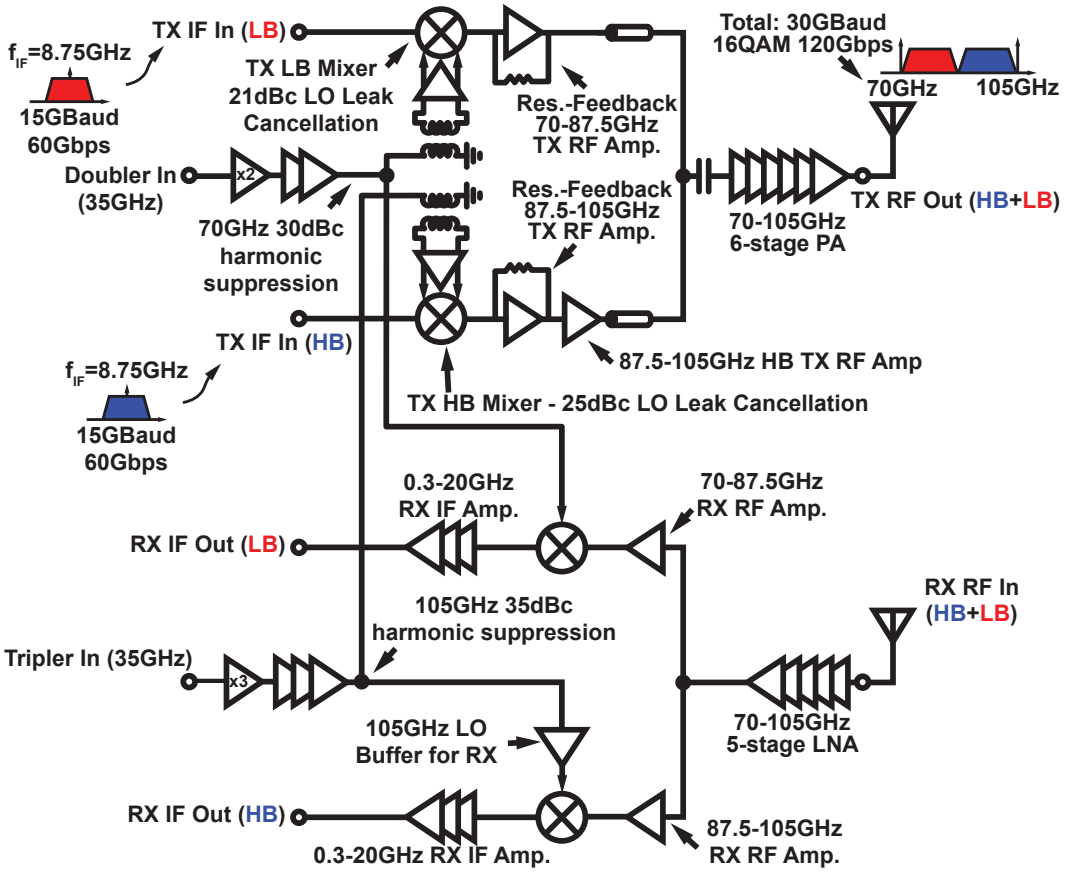


Figure 5.9: W-band frequency-interleave transceiver detailed block diagram.

buffer for RX mixer LO drive is used to satisfy similar conversion gain (CG) for LB and HB branches, because the CG of HB RX mixer is lower than CG of LB RX mixer. Details of frequency multipliers are given in subsection 5.4.4 with design considerations and simulation results. RX IF amplifiers works from 0.3 to 20GHz. Same IF amplifier circuit is used for both LB and HB. Details of the circuit are given in the next subsection. RX RF mixers are passive single-transistors with a size of 12µm (w_f = 2µm, n_f = 6). As explained in the above section, TX LO leak cancellation should be achieved. To do that a single-IF input balanced mixer is proposed. A mm-wave Marchand balun is used for both LB and HB differential LO generation. To compensate the loss of the balun and to balance differential amplitude and phase difference, a capacitive cross coupled differential amplifier is employed for both LB and HB. Negative IF input port of the TX mixers are connected to dummy load, again to satisfy the balance and to use single-ended IF input ports. Details of the circuits implemented in TRX are given in

subsection 5.4.2.

5.4 Building Block Circuitry Design and Results

5.4.1 Millimeter-Wave Amplifiers

Design of high gain mm-wave amplifiers based on CS topology requires cascading of several number of stages owing to the disadvantages of decreased intrinsic gain of transistors and increased passive losses. PFCS topology is generally employed for amplifiers operating near f_{max} [71, 81, 82]. Since the required gain for mm-wave amplifiers in this work is high, PFCS topology is used. By this way, gain from one-stage can be increased considerably. Different than the literature [71, 81, 82], in here DC-cut capacitors are used before the gate to separate gate and drain of transistors to have a control over the transistor gate bias voltages (e.g. Fig. 5.10(b)). To prove that higher gain is possible from a transistor, a one-stage CS amplifier (Fig. 5.10(a)) and a one-stage PFCS amplifier (Fig. 5.10(b)) around 95GHz are designed. In all amplifier designs, MIM-TL is used to isolate DC and RF in an ultra-wideband manner [83]. This decoupling TL has impedance around 2Ω, as a result from RF point of view it is almost close to short-circuited. The gain comparison of the two amplifiers and the MSG/MAG of the same transistor are plotted in Fig. 5.10(c). It can be observed that CS amplifier can get a maximum of around 4dB gain, while PFCS amplifier can get a maximum of around 9dB gain, which is also very close to the MSG/MAG of the transistor. In this work, except the first stage of PA, and resistive feedback TX RF amplifiers, every mm-wave amplifier employ PFCS topology.

Fig. 5.11 shows the basic schematic of the ultra-wideband PA design. The last six-stages of PA use FB CS topology and the first-stage is CS to increase the stability of the amplifier. In every stage between the MIM-TL and V_{DD} line a 2Ω RF resistor is used to enhance stability of the amplifiers. DC block capacitors are 150fF and transistor size for every stage is 36μm (w_f = 1.5μm, n_f = 24). LNA has five-stages of FB CS, and one-stage RF amplifiers are connected for LB and HB branches as illustrated in Fig. 5.12.

5.4.2 Receiver Wideband IF Amplifier

IF data in this work are wideband and hence a 0.3-20GHz IF amplifier is designed for RX. Fig. 5.13 provides the schematic for IF amplifiers. The first two-stages are CS and the last stage is cascode. Inter-stage matching networks are done with series LC network, and to provide wideband gain resistive loads are used. CS stage transistors size is 64μm

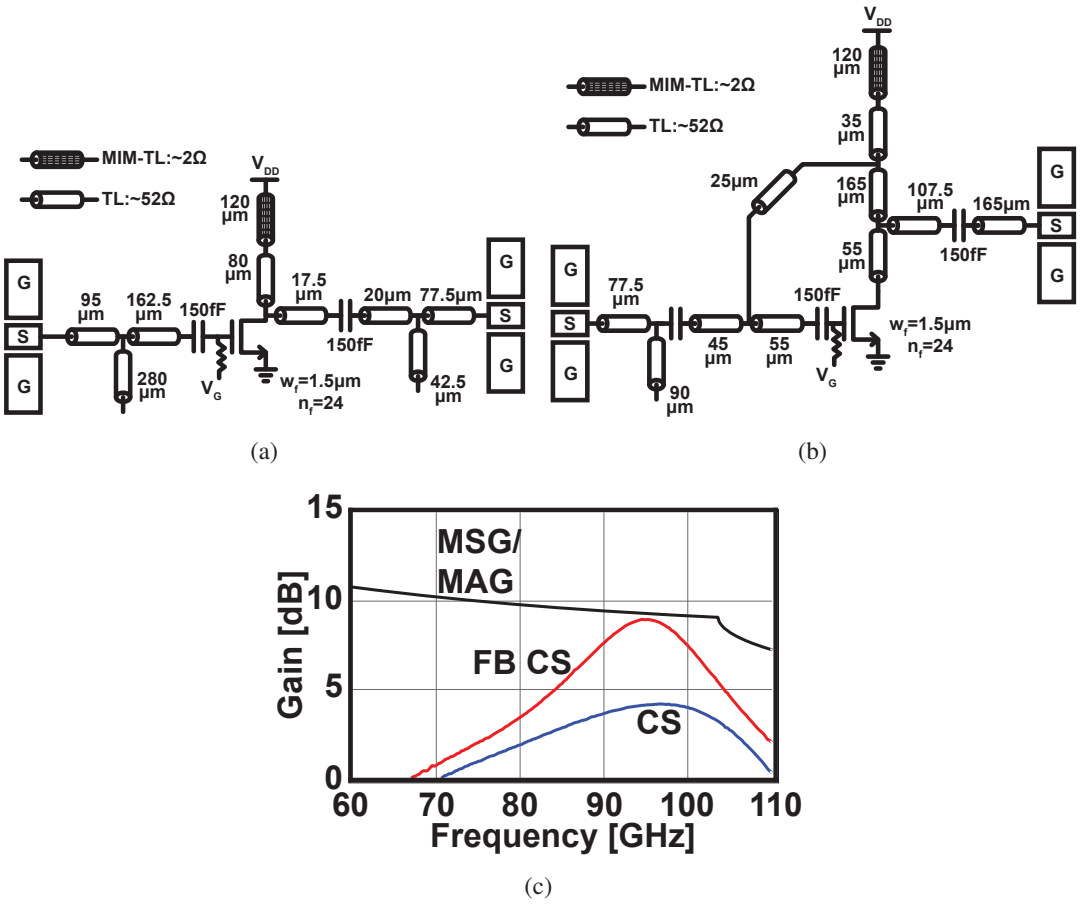


Figure 5.10: Comparison of mm-wave common-source (CS) amplifier and positive feedback common-source (PFCS) amplifier topologies; (a) CS amplifier schematic of a Test Element Group (TEG), (b) PFCS amplifier of a TEG, and (c) gain comparisons of CS (blue line), PFCS (red line) and the Maximum Stable Gain (MSG)/Maximum Available Gain (MAG) of the transistor used in the amplifiers (black line).

($w_f = 2\mu m, n_f = 32$), and the common-gate transistor size is 192µm ($w_f = 6\mu m, n_f = 32$). First two-stages are biased at 0.55V and the last stage is biased at 0.7V.

5.4.3 Single-IF Balanced Mixer

As explained in the above sections, TX LO leak cancellation is crucial for this work to avoid cross-modulations on both TX and RX. One of the straightforward way to suppress the LO leak is to use a bandpass filter (BPF) with very sharp characteristics as shown in Fig. 5.14(a). BPF with very sharp characteristics has too much loss in mm-wave region and hence avoided in here. Another approach is to use a balanced or

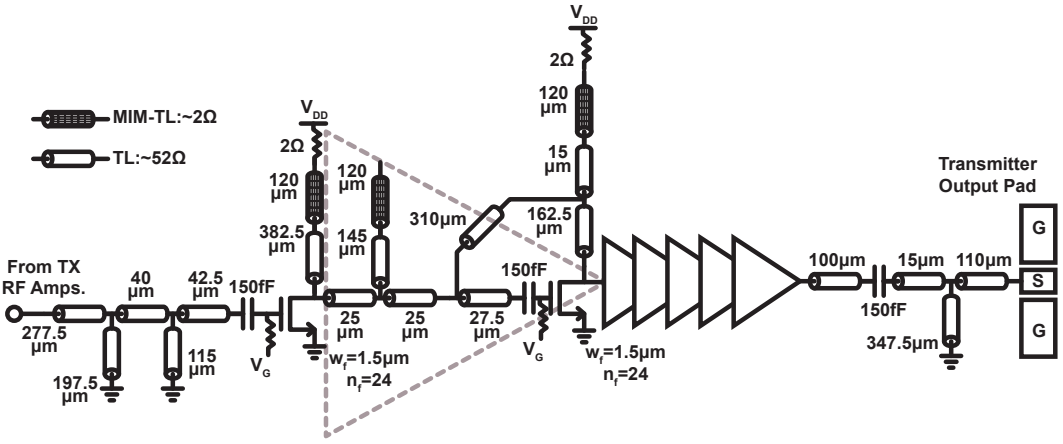


Figure 5.11: Six-stage ultra-wideband PA schematic. First-stage is CS and remaining six-stage is PFCS.

double-balanced mixer. Fig. 5.14(b) shows the double-balance case. For this case, LO leak can be canceled. Nevertheless differential IF and RF ports requires, differential amplifiers. To have ultra-wideband differential IF and RF amplifiers, one has to sacrifice a lot from power and silicon area consumption. Thus, single-ended IF and RF ports are desirable for ultra-wideband TRX. Baluns can be used to convert differential to single-ended. Nonetheless, baluns introduce differential amplitude and phase imbalance and this effect strongly depends on frequency characteristics. Moreover, they are lossy, especially for mm-wave.

In consideration with above issues and the requirements, a single-IF balanced mixer is proposed. Fig. 5.15 provides the basic schematic for this work. The main idea is to use the cancellation effect of a balanced mixer. Only the positive LO drive transistor is responsible for up-conversion, and the IF is inputted to this transistor. The negative LO drive transistor IF port is terminated with a dummy load to provide the differential LO balance, and hence LO leak cancellation. The 50Ω dummy load is for the termination, and 27fF dummy capacitor is for the pad parasitic capacitance. Additional 2.5pF capacitor is connected between ground and 50Ω dummy load to prevent DC short from the DC offset cancellation current sources. The LO leakage cancellation can be achieved using differential LO signal and proper adjustment with bias nodes of mixer and differential buffer transistors as well as the DC offset voltage at the IF ports of the mixers. DC offset voltages are adjusted with the DC current flowing through the 80Ω wideband RF resistors. These also help with the wideband matching of IF input ports of the TX.

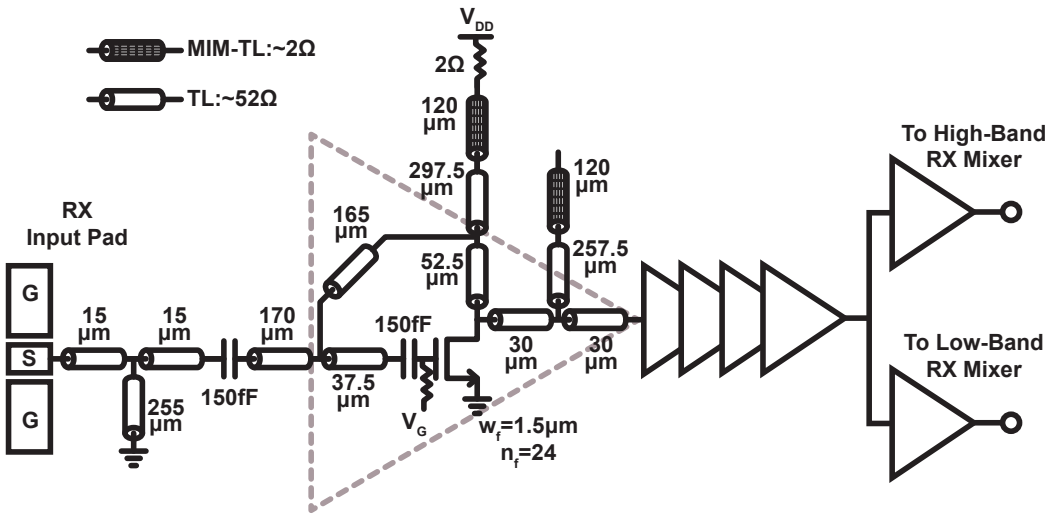


Figure 5.12: Five-stage ultra-wideband LNA and RX RF amplifiers schematic.

5.4.4 Doubler and Tripler Design

Fig. 5.16 illustrates the designed doubler schematic for 70GHz LB LO generation. Doubler transistor has a total width of 12µm ($w_f = 2\mu m, n_f = 6$) and is biased at 0.35V for the highest second-order non-linearity. The buffers used in both doubler and tripler are based on the PFCS topology designed to be narrow bandwidth to suppress the fundamental (35GHz) and undesired harmonics for better TX and RX EVM performances while avoiding cross modulations between LB and HB. In the figure, details of the first stage buffer for doubler is given. Fig. 5.18(a) shows the simulation results for the doubler from which a 29dBc difference between the desired second-order and undesired harmonics can be observed. Fig. 5.17 illustrates the tripler schematic. Tripler transistor has a total width of 40µm ($w_f = 2\mu m, n_f = 20$) and is biased at 0.2V for the highest third-order non-linearity. The simulation results of the tripler input-to-output power characteristics illustrated in Fig. 5.18(b) shows that difference between the desired third-order and undesired harmonics is around 38dBc. The outputs of the doubler and tripler are matched to 25Ω since it is divided into two for TX and RX which are matched to 50Ω. Finally, as mentioned before, an additional buffer is inserted after the tripler to increase the LO power to the RX HB mixer.

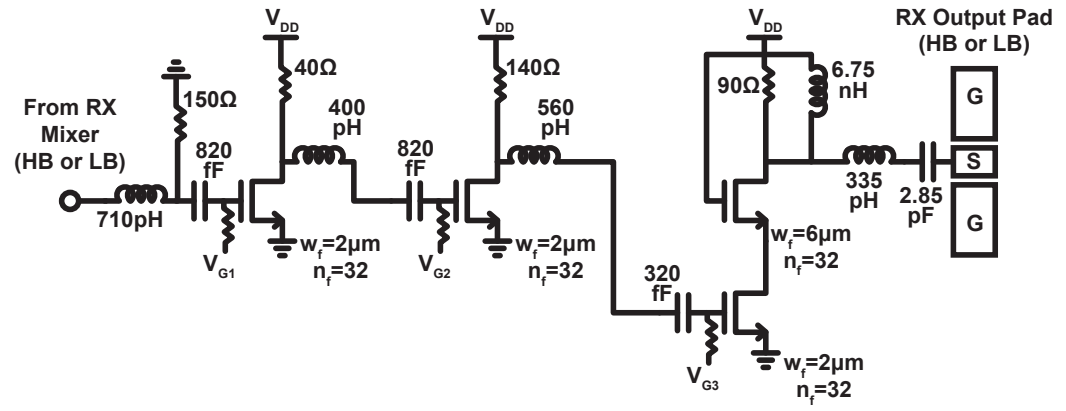


Figure 5.13: Receiver ultra-wideband IF amplifier schematic. Same IF amplifier used for HB and LB.

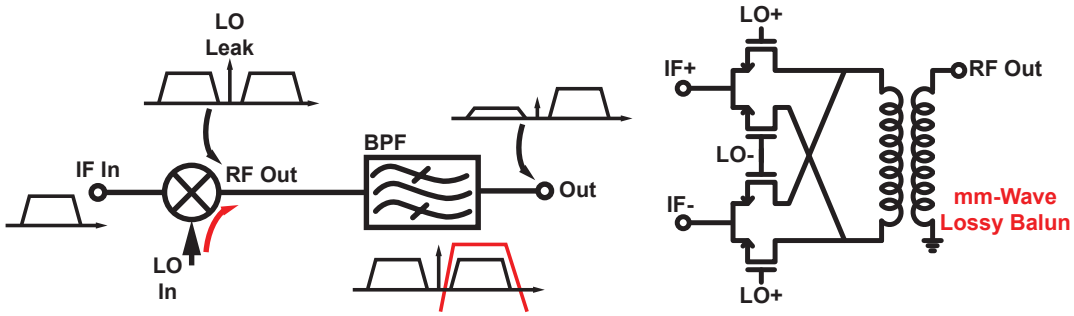


Figure 5.14: Conventional LO leakage suppression approaches; (a) using sharp band-pass filter for a single-ended mixer, or (b) using double balanced mixer.

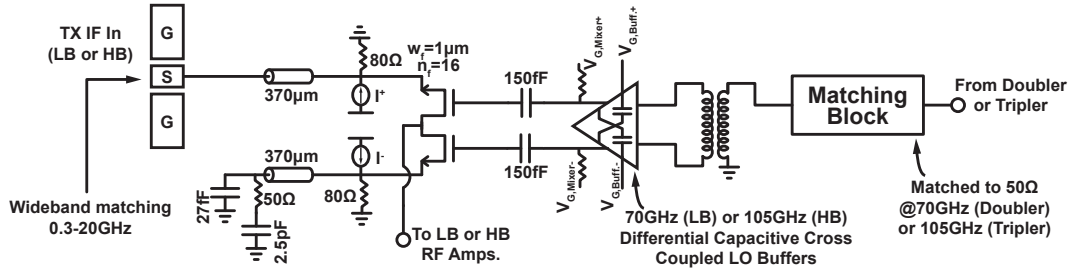


Figure 5.15: Proposed single-IF balanced mixer for LO leakage cancellation using single-ended IF and RF ports.

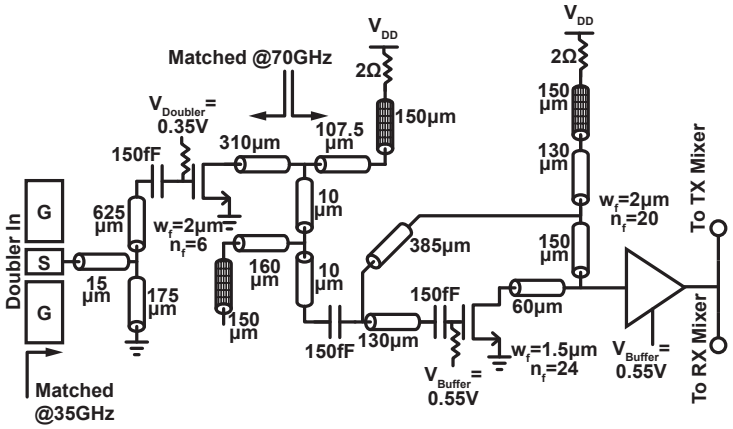


Figure 5.16: Proposed frequency doubler for 70GHz LB LO generation.

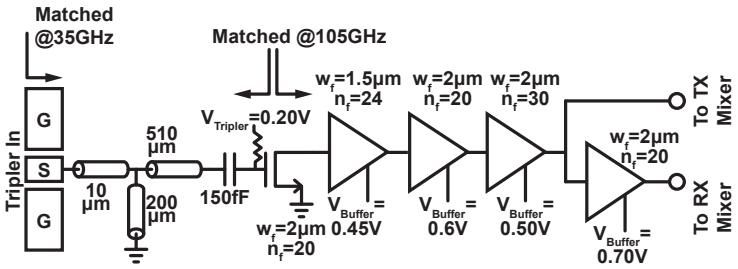
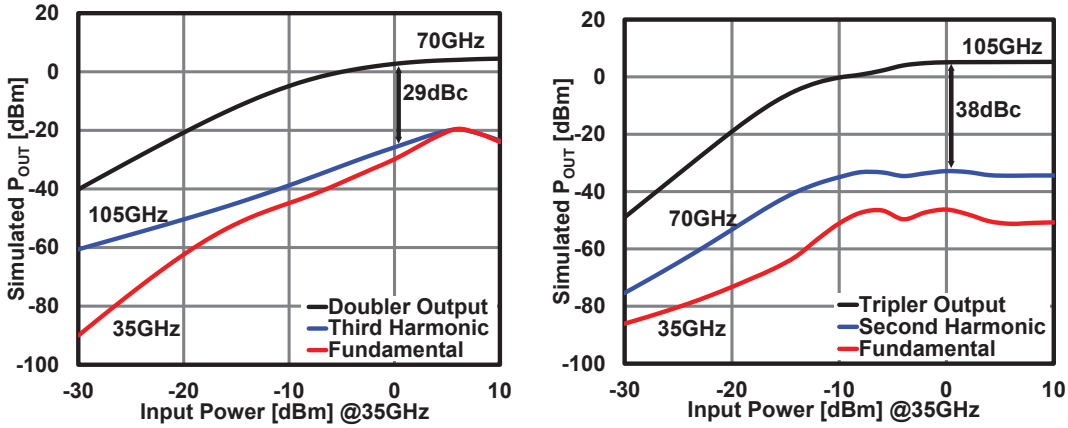


Figure 5.17: Proposed frequency tripler for 105GHz HB LO generation.



(a) (b)

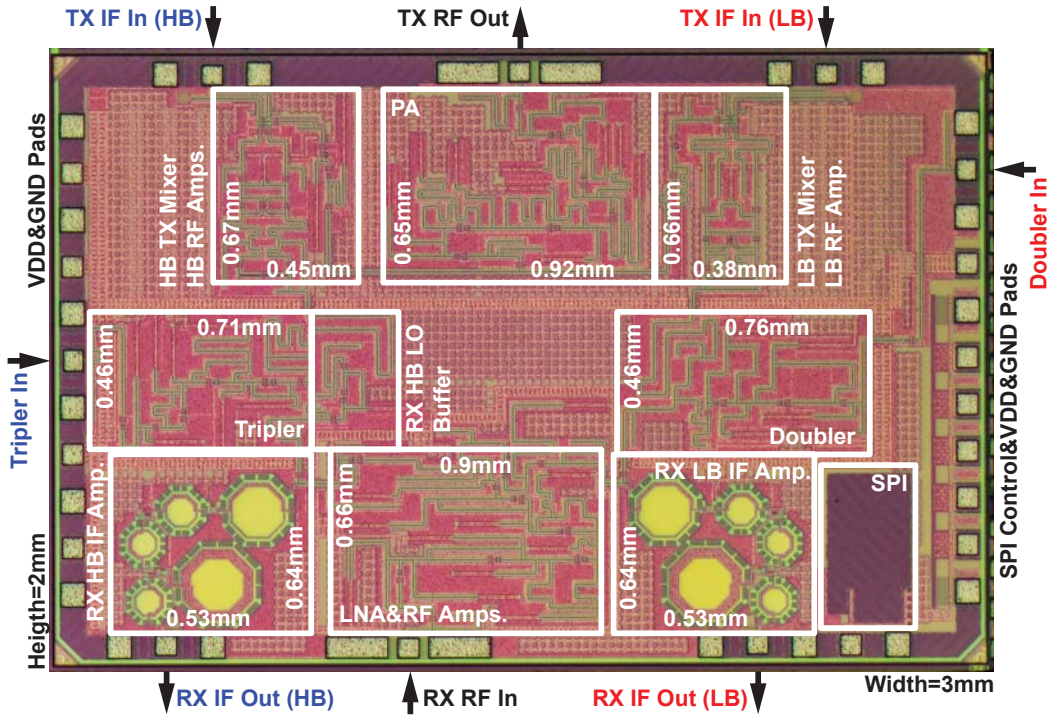
Figure 5.18: Simulation results of (a) doubler desired output power and undesired harmonics vs. input power at 35GHz, and (b) tripler output power and undesired harmonics vs. input power at 35GHz.

5.5 Test Module Design and Implementation

W-band TRX is implemented on 65nm bulk CMOS. Die photo is shown in Fig. 5.19. Total area of the chip is 6mm^2(3mm $\times$ 2mm). Power and area breakdown of the W-Band TRX are also included in the same figure. A customized test module is implemented for W-band TRX. TX and RX are connected to a microstrip on PCB via wirebonds (Fig. 5.20(a)). Transition from microstrip to WR-10 flange makes it easy to conduct measurements, and horn antennas can be connected directly. The transition is designed with EM simulations. Microstrip line width is 0.25mm. PCB material is PTFE (Polythtrafluoroeth-ylene) with $\epsilon_r = 2.17$, and a loss tangent of 0.0009 at 10GHz. The thickness is 0.127mm. There are several transition examples in literature [84–86]. In this work, a back-short probe approach is used, since it has very wideband characteristics with low loss [86]. Details are provided in Fig. 5.20(a) for top view, and Fig. 5.20(b) for cross-sectional view. The width of the PCB part penetrating inside the structure is 1mm and it penetrates 0.68mm. Note that there is no PCB ground under the probe. The depth of the back-short is 0.7mm.

The test module is implemented as shown in Fig. 5.21. Total area of the module is 80mm by 80mm. The IC is silver-epoxy glued in the middle part of the module. DC pin connector is used for external control of the SPI inside the IC. IF and LO ports of the IC are connected to low-loss DC to 40GHz SMPM connectors via 0.375mm wide microstrip lines (50Ω). Left hand side of Fig. 5.21 shows IC, some decoupling capacitors and traces.

In order to test the PCB to waveguide transition, a back-to-back connection of two transition with 14mm length microstrip line is constructed (Fig. 5.22(a)). Fig. 5.22(b) plots the measurement results for insertion loss (IL) has a minimum of -3.9dB up to 102GHz. Fig. 5.22(c) plots the measured return loss (RL) has a maximum of -8dB up to 102GHz.



Transmitter	Area [mm^2]	P_{DC} [mW]
Power Amplifier	0.6	67
HB Mixer&RF Amps.	0.3	17
LB Mixer&RF Amp.	0.25	13
Total	1.15	97

Receiver	Area [mm^2]	P_{DC} [mW]
LNA&RF Amps.	0.59	84
HB&LB IF Amps.	0.68	42
HB LO Buff.	0.1	10
Total	1.37	136

LO Chain	Area [mm^2]	P_{DC} [mW]
Doubler	0.35	7
Tripler	0.33	16
Total	0.68	23

Figure 5.19: Die photo of W-band frequency interleave transceiver occupying an area of 6mm^2, manufactured with 65nm bulk CMOS process. Area and power breakdown of the IC is also included in the figure.

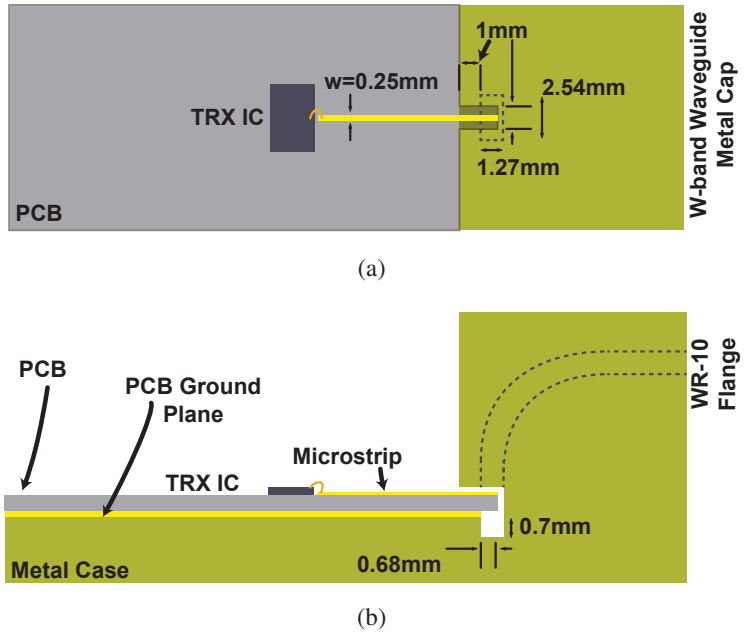


Figure 5.20: Wideband PCB-to-waveguide (WR10) transition; (a) top view, (b) cross sectional view.

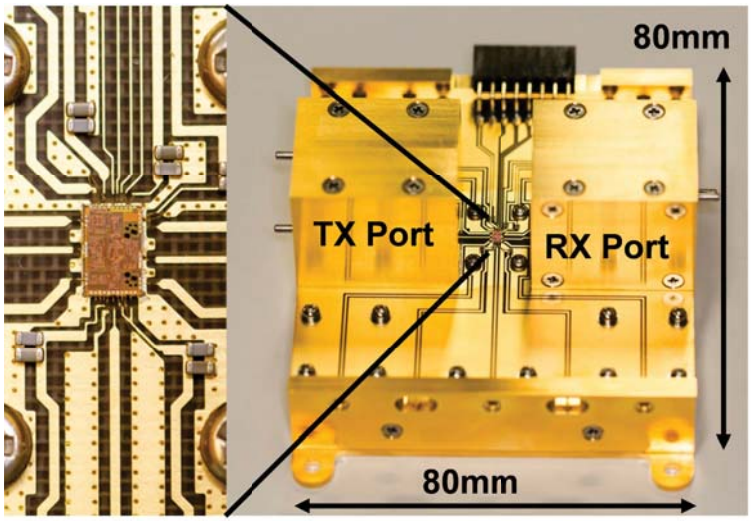


Figure 5.21: Test module implementation for the W-Band frequency-interleave transmitter. Left had side photo is the zoomed in version for the middle part where the IC is integrated and wire bonded to the respectful traces.

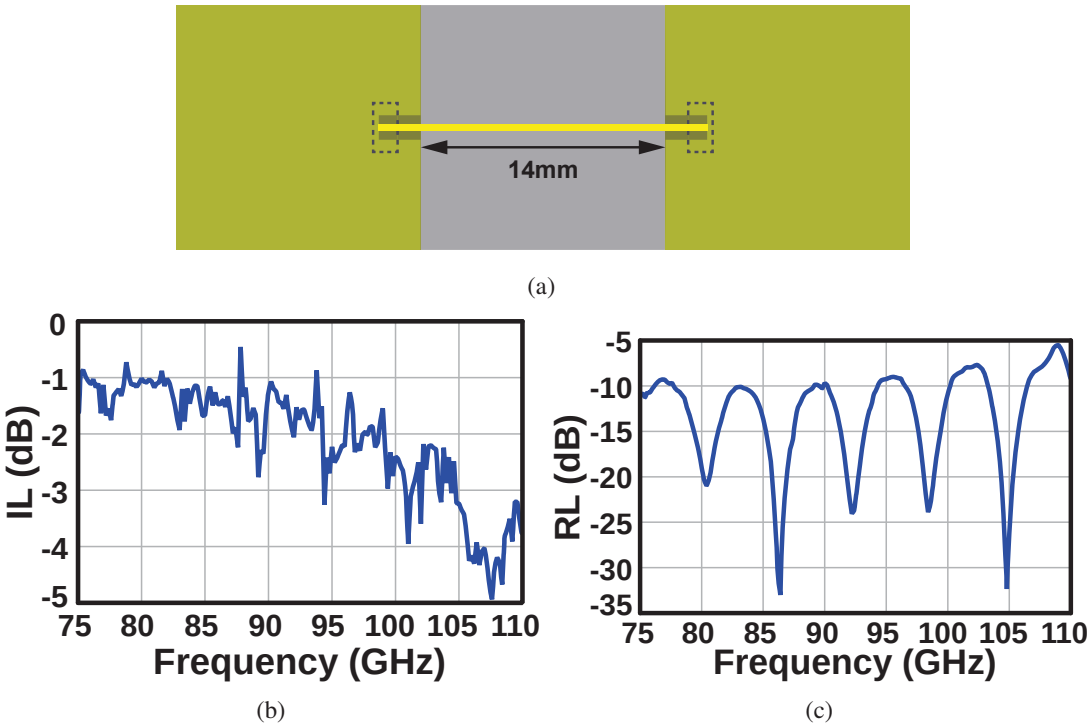


Figure 5.22: (a) Illustration of back-to-back connected two PCB-to-waveguide transitions with 14mm microstrip on PCB, (b) insertion loss (IL) measurement result for (a), and (c) return loss (RL) measurement result for (a).

5.6 Measurement Results

All of the measurements presented from this point are done using the test module. Fig. 5.23 presents the measurement setup for TX conversion gain (CG), power input-output. Output of TX is connected to an external WR-10 mixer. LO for external mixer is generated by a 6× frequency multiplier. 87.5GHz LO is used for both LB and HB cases. IF output of external mixer is connected to spectrum analyzer for CG and power measurements. External part loss are calibrated and de-embedded.

Fig. 5.24(a) presents the CG and power input-output measurement results for LB IF input of 9 GHz (79GHz RF output). Module loss is around 10dB and de-embedded from the measurement results. CG is around -5.4dB and due to the input power limitations OP_{1dB} and P_{sat} could not be measured. Similarly, Fig. 5.24(b) presents the CG and power input-output measurement results for HB IF input of 9 GHz (96GHz RF output). Module loss is around 10dB and de-embedded from the measurement results. CG is around -7.5dB and due to the input power limitations OP_{1dB} and P_{sat} could not be measured.

Fig. 5.25 presents the measurement setup for TX EVM vs. output power (dBm). A 65GS/s 25GHz-BW AWG (Keysight M8195A) is used to generate 5GBaud QPSK and 16QAM IF signals and a 200GS/s 70GHz-BW oscilloscope (Tektronix DPO77002SX) is used to collect the output data. During the TX EVM measurements, the output of TX is connected to 70-84GHz BPF for LB and 93-109GHz BPF for HB before the external W-band mixer which has an LO input at 87.5GHz. The LO for external mixer is generated with frequency multiplier by-six from a signal generator (SG) having 14.58GHz output signal. External SG having and output signal frequency of 35GHz is used for doubler and trjpler inputs. The BPFs employed in this measurement have loss around -2.3dB. The IF output of the external mixer (Millitech MXP-10-RFSFL), which has -13dB conversion loss and 13dB NF, is connected to oscilloscope.

Fig. 5.26 illustrates that the TX achieves the best EVM for 16QAM of -24.3dB at the output power of -7.4dBm for LB, and -21.1dB at the output power of -9.4dBm for HB. Note that the input power to TX is limited up to -2dBm due to AWG, cable and module losses. Hence better TX EVM is possible with higher input power. The 16QAM EVM requirement of -19.5dB is also indicated in the figure, which is 3dB higher than the requirement of TX-to-RX EVM for a BER of 10^{-3}. 5GBaud of data are used for both LB and HB TX EVM measurements for QPSK (triangular markers in the figures) and 16QAM (square markers in the figures). Note that there is 1 to 2dB difference between the QPSK and 16QAM EVM results, which is always expected since there is no amplitude modulation in QPSK and there is amplitude modulation in 16QAM.

RX measurement setup for CG and power input-output is illustrated in Fig. 5.27. RF

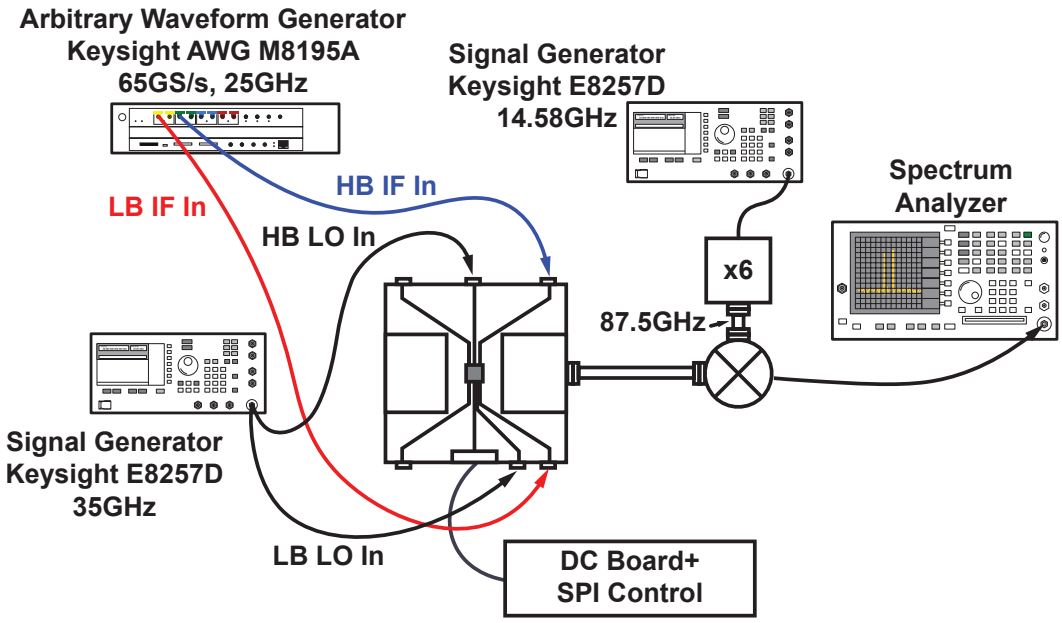


Figure 5.23: Measurement setup for transmitter conversion gain and power input-output.

input to RX is generated with AWG and an external mixer. The 87.5GHz LO drive of external mixer is again generated with a 6× multiplier from a SG with 14.58GHz signal output. The CG and power characteristics are measured with the help of a Spectrum Analyzer. After the measurements de-embedding of the losses from external components is done.

Fig. 5.28(a) presents the CG and power input-output measurement results for LB IF output of 9 GHz (79GHz RF input). Module loss is around 10dB and de-embedded from the measurement results. CG is around 21.3dB and OP_{1dB} is -9.1dBm. Similarly, Fig. 5.28(b) presents the CG and power input-output measurement results for HB IF output of 9 GHz (96GHz RF input). Module loss is around 10dB and de-embedded from the measurement results. CG is around 20.5dB and OP_{1dB} is -12.5dBm.

Fig. 5.29 presents the measurement setup for RX EVM vs. input power (dBm). A 65GS/s 25GHz-BW AWG (Keysight M8195A) is used to generate 5GBaud QPSK and 16QAM IF signals and a 200GS/s 70GHz-BW oscilloscope (Tektronix DPO77002SX) is used to collect the output data. During the RX EVM measurements, the output of external up-conversion mixer, which has an LO input at 87.5GHz and the LO for external mixer is generated with frequency multiplier by-six from a signal generator (SG) having 14.58GHz output signal, is connected to 70-84GHz BPF for LB and 93-109GHz BPF for HB before the receiver RF input. External SG having and output signal frequency of 35GHz is used

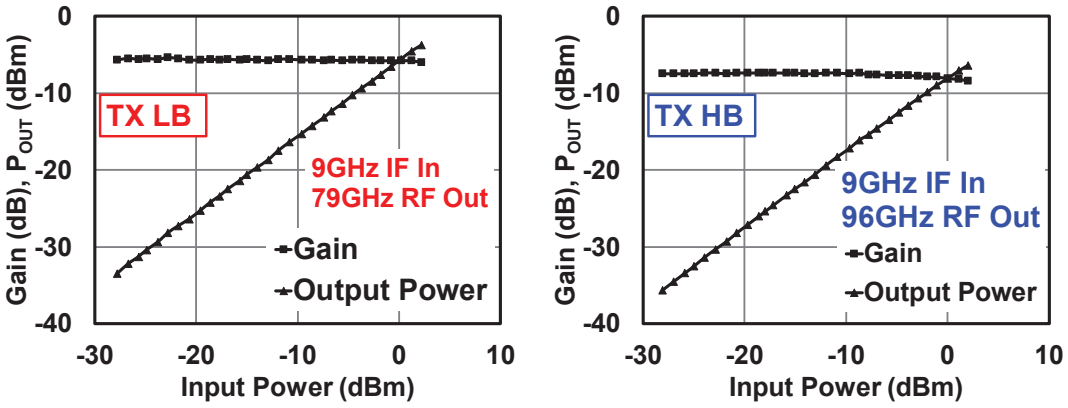


Figure 5.24: Transmitter measurement results; (a) conversion gain and power input-output for low-band IF input of 9GHz (79GHz RF out), and (b) conversion gain and power input-output for high-band IF input of 9GHz (96GHz RF out).

for doubler and trjpler inputs. The BPFs employed in this measurement have loss around -2.3dB. External mixer (Millitech MXP-10-RFSFL) has -13dB conversion loss and 13dB NF.

Fig. 5.30 illustrates that for 5GBaud 16QAM RF signals, the RX has the best EVM of -25.6dB at the input power of -26.3dBm for LB and -24.7dB at the input power of -24.3dBm for HB. For QPSK, EVM results are 1 to 2dB better than 16QAM case.

An example system architecture for W-Band ultra-high data-rate wireless transceiver is shown in Fig. 5.31. One can remember that the IF center frequency used in this work is 8.75GHz. Moreover, RF up- and down-conversion LO is generated from a 35GHz input signal. In a complete system approach, it is possible to use a 17.5GHz PLL to generate the quadrature LO signal for IF center frequency by using divide-by-two circuitry for both LB and HB IF up- and down-conversion mixers, and a frequency doubler can be used to generate the 35GHz LO input signal for doubler and tripler used in this work. Note that LO generation is not focused on this version of the work. The transmitter side digital baseband, DACs, LPFs and IF up-conversion mixers in here are realized with the Arbitrary Wave Generator. Similarly, the receiver side digital baseband, ADCs, VGAs, LPFs and IF down-conversion mixers in here are realized with the high-speed oscilloscope. The measurement setup for transceiver EVM measurements are based on this whole system approach.

For wireless data transmission, WR-10 waveguide horn antenna are connected to TX and RX. Antenna gain is 23dBi. Photo of the measurement setup is shown in Fig. 5.32. Again, the 65GS/s 25GHz-BW AWG (Keysight M8195A) is used to generate QPSK and

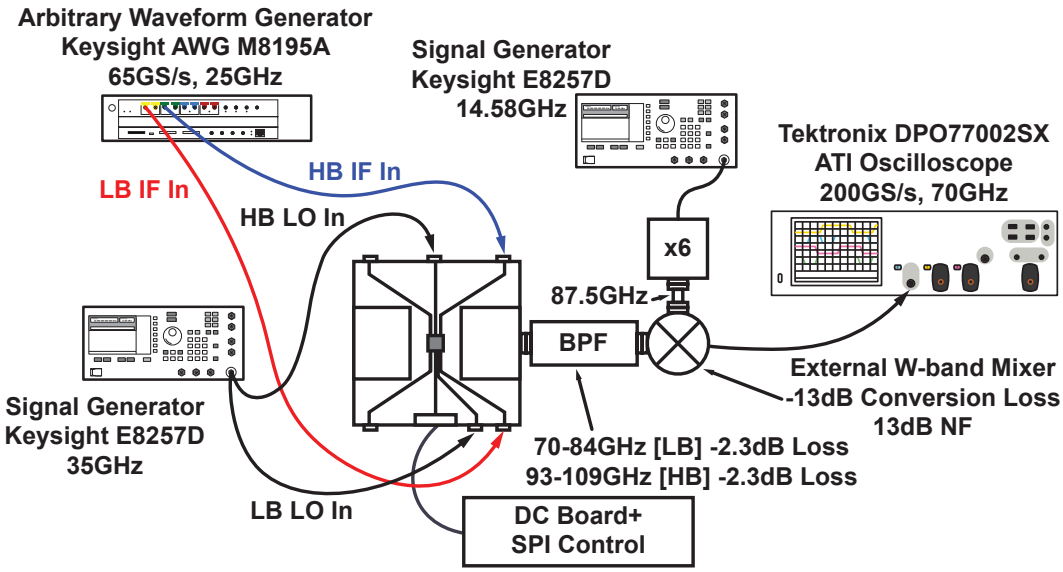
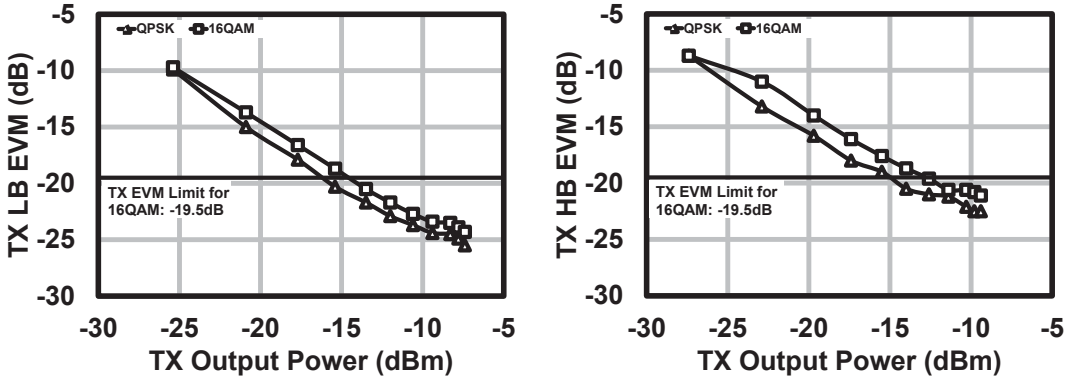


Figure 5.25: Measurement setup for transmitter EVM vs output power.

16QAM IF signals and a 200GS/s 70GHz-BW oscilloscope (Tektronix DPO77002SX) is used to collect the output data. Two 35GHz signal generators are used in the setup. The module on the left hand side is used as TX and the module on the right hand side is used as RX. Equipment on the left hand side is AWG, middle one is the high speed oscilloscope and the right hand side one is one of the SGs used as 35GHz LO input. An external personal computer is used to control AWG and oscilloscope to check the quality of the received data (personal computer could not be included in the photo).

One of the main issue in frequency-interleave transceivers is the cross-modulation as explained in the second section of this chapter. Hence, an indirect way of measuring this is necessary. In here, four different measurement setups are done to check whether cross-modulation has a considerable effect on the quality of the wireless communications. Fig. 5.33 shows the TRX measurement setup representation for checking the EVM of LB channel when both LB and HB TX IF inputs are ON. Second channel of the oscilloscope is used for the reception of LB RX IF output since it has lower noise floor and hence better SNDR in comparison with first and third channels of the oscilloscope. Fig. 5.34 shows the TRX measurement setup representation for checking the EVM of LB channel when only LB TX IF input is ON. HB TX IF input is OFF and it is terminated with wideband external 50Ω. HB IF RX output is also terminated with wideband external 50Ω. When one compares the EVM results for the two cases, cross-modulation can be quantitatively observed. Fig. 5.35 shows the TRX measurement setup representation for checking the



(a) (b)

Figure 5.26: Transmitter EVM measurement results (The 16QAM EVM requirement of -19.5dB is also indicated in the figure, which is 3dB higher than the requirement of TX-to-RX EVM for a BER of 10^{-3}.); (a) LB EVM for 5GBaud QPSK (triangular markers) and 5GBaud 16QAM (rectangular markers), and (b) HB EVM for 5GBaud QPSK (triangular markers) and 5GBaud 16QAM (rectangular markers).

EVM of HB channel when both LB and HB TX IF inputs are ON. Second channel of the oscilloscope is used for the reception of HB RX IF output. Fig. 5.36 shows the TRX measurement setup representation for checking the EVM of HB channel when only HB TX IF input is ON. LB TX IF input is OFF and it is terminated with wideband external 50Ω. LB IF RX output is also terminated with wideband external 50Ω. Communication distance is set to 0.2m in the following measurements.

The TRX EVM measurement results are summarized in the following figures. Fig. 5.37(a) shows the measured LB QPSK TX-to-RX EVM for symbol rates from 4GBaud to 15GBaud. The QPSK EVM requirement of -9.8dB is also indicated in the figure for a BER of 10^{-3}. The roll-off factor for symbol rates from 4GBaud to 12.5GBaud is 0.35, i.e. analog data band-width from 5.4GHz to 16.9GHz. The roll-off factor is 0.25 for 13.5GBaud (16.9GHz analog bandwidth), and 0.13 for 15GBaud (17GHz analog bandwidth). The plot compares when LB and HB are both ON and LB EVM is observed (square marked black solid lines), and only LB is ON and LB EVM (triangular marked red solid lines) is observed for two cases of with and without built-in-software equalization. The TX-to-RX QPSK EVM difference when only LB IF is ON and when both LB and HB IFs are ON is less than 0.9dB for the case of without equalization. Fig. 5.37(b) shows the measured HB QPSK TX-to-RX EVM for symbol rates from 4GBaud to 15GBaud. The plot compares when LB and HB are both ON and HB EVM is observed (square marked black solid lines), and only HB is ON and HB EVM (triangular marked blue solid lines) is observed for two cases of with and without built-in-software

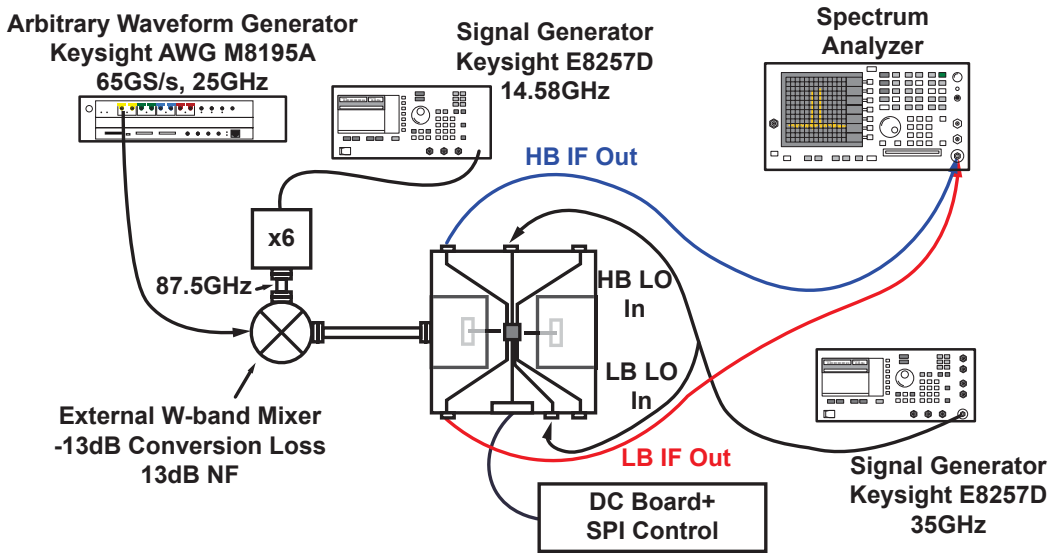
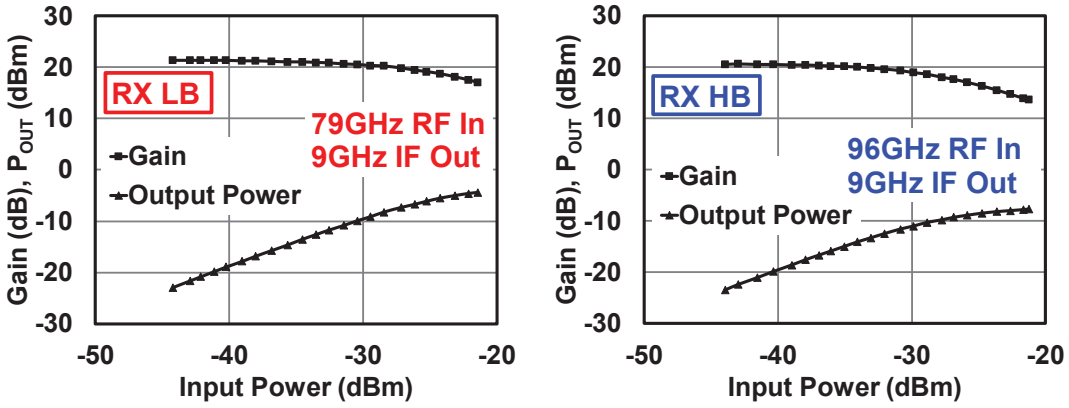


Figure 5.27: Measurement setup for receiver conversion gain and power input-output.

equalization. Similarly, the TX-to-RX QPSK EVM difference for HB is less than 0.6dB for the case of without equalization. These results strongly supports that the contribution of cross-modulation between LB and HB to the TRX performance is negligibly low. For both LB and HB, 15GBaud QPSK can be achieved without any equalization. Hence, the TRX can work ultra-wideband. Fig. 5.38(a) shows the measured LB 16QAM TX-to-RX EVM for symbol rates from 4GBaud to 15GBaud. The 16QAM EVM requirement of -16.5dB is also indicated in the figure for a BER of 10^{-3}. The plot compares when LB and HB are both ON and LB EVM is observed (square marked black solid lines), and only LB is ON and LB EVM (triangular marked red solid lines) is observed for two cases of with and without built-in-software equalization. Fig. 5.38(b) shows the measured HB QPSK TX-to-RX EVM for symbol rates from 4GBaud to 15GBaud. The plot compares when LB and HB are both ON and HB EVM is observed (square marked black solid lines), and only HB is ON and HB EVM (triangular marked blue solid lines) is observed for two cases of with and without built-in-software equalization. For both LB and HB, 8GBaud 16QAM TX-to-RX wireless communication is possible without equalization and 15GBaud 16QAM is possible with built-in-software equalization.

Fig. 5.39 shows the results for 30GBaud QPSK without and with equalization (60Gbps), and 30GBaud 16QAM with equalization (120Gbps). Point A is indicated in Fig. 5.37(a) for LB 15GBaud QPSK. This is achieved without any equalization and the TX-to-RX EVM is measured as -10.8dB. Point B is indicated in Fig. 5.37(b) for HB 15GBaud QPSK. This is achieved without any equalization and the TX-to-RX EVM is



(a) (b)

Figure 5.28: Receiver measurement results; (a) conversion gain and power input-output for low-band IF output of 9GHz (79GHz RF in), and (b) conversion gain and power input-output for high-band IF output of 9GHz (96GHz RF in).

measured as -11.2dB. Point C is indicated in Fig. 5.37(a) for LB 15GBaud QPSK. This is achieved with equalization and the TX-to-RX EVM is measured as -16.7dB. Point D is indicated in Fig. 5.37(b) for HB 15GBaud QPSK. This is achieved with equalization and the TX-to-RX EVM is measured as -16.5dB. Point E is indicated in Fig. 5.38(a) for LB 15GBaud 16QAM. This is achieved with equalization and the TX-to-RX EVM is measured as -16.9dB. Point F is indicated in Fig. 5.38(b) for HB 15GBaud 16QAM. This is achieved with equalization and the TX-to-RX EVM is measured as -17.0dB. Hence, a 120Gbps world fastest full electronic wireless transceiver is realized. Transmitter output spectrum of these data are plotted in the same figure. The whole bandwidth from 70 to 105GHz is almost occupied with information. Additional measurements are shown in Fig. 5.40. Both of these results are measured without equalization. The maximum data-rate that this TRX can achieve without any equalization is realized with 8PSK modulation with 24GBaud of total data bandwidth. Both Lb and HB TX-to-RX EVM are measured as -12.8dB. Using 32QAM modulation a maximum of 60Gbps is possible with a total 12GBaud of data without any equalization.

Fig. 5.41 shows the maximum achievable data-rate vs. distance. 100Gbps can be achieved at 0.3m, whereas 60Gbps is possible at 1.25m. Hence, theoretically, with 53dBi optical lens antenna on both transmitter and receiver side, 100Gbps wireless communication is possible at a distance of 300m.

Table 5.1 compares this work with other high data-rate wireless TRXs [22, 69, 70, 87–92]. Clearly, this work achieves the state-of-the-art wireless transmission data-rate. The power consumption of TX is 120mW, RX is 160mW from a 1V DC feed.

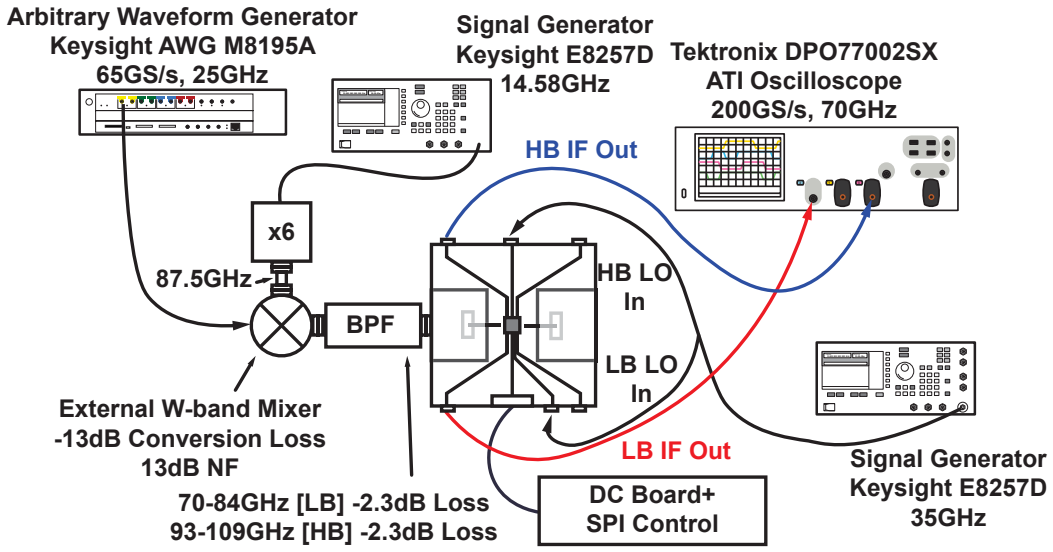
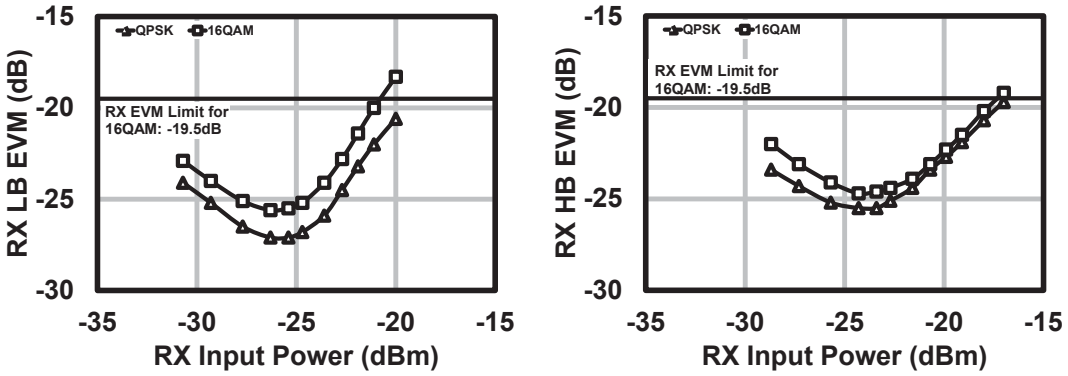


Figure 5.29: Measurement setup for receiver EVM vs input power.

The previous version of this work [93] achieved 56Gbps from 0.1m communication distance (reference work 8 in the comparison table). The main limitation of the previous work is the cross-modulation due to undesired LO harmonics, LO leakage, and SNDR limitation of the transmitter and receiver due to inaccurate models. To achieve 120Gbps, first of all, the simulation models are improved considerably as described in Chapter 3. Additionally, LO harmonic suppression inside the frequency doubler and tripler are improved considerably by careful adjustment of the gate bias for the doubling and tripling transistors. Additionally, the narrowband buffers designed more accurately thanks to the improved models. Moreover, single-IF balanced TX mixers are updated with IF port DC-offset cancellation circuitry (as described above in the circuit blocks section) to cancel the LO leakage from the TX. PA and LNA are redesigned based on improved models to reflect the required SNDR.



(a) (b)

Figure 5.30: Receiver EVM measurement results (The 16QAM EVM requirement of -19.5dB is also indicated in the figure, which is 3dB higher than the requirement of TX-to-RX EVM for a BER of 10^{-3}.); (a) LB EVM for 5GBaud QPSK (triangular markers) and 5GBaud 16QAM (rectangular markers), and (b) HB EVM for 5GBaud QPSK (triangular markers) and 5GBaud 16QAM (rectangular markers).

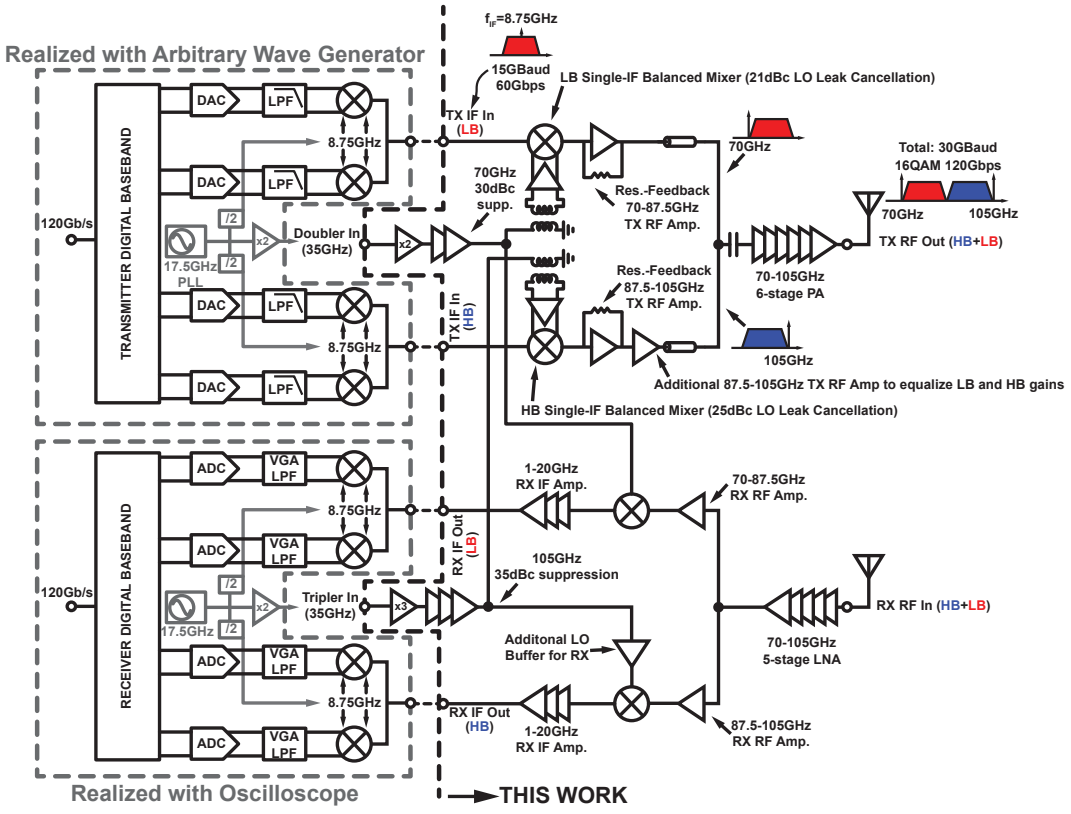


Figure 5.31: An overall system representation of W-Band ultra-high data-rate transceiver.

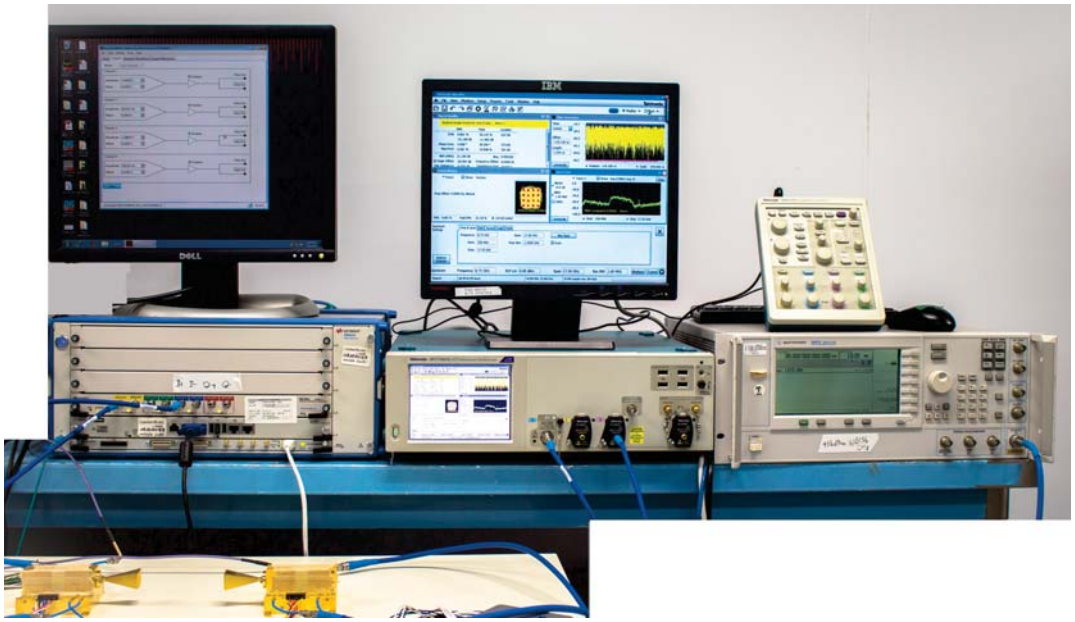


Figure 5.32: Setup for transmitter-to-receiver wireless communication error vector magnitude (EVM) measurements photo.

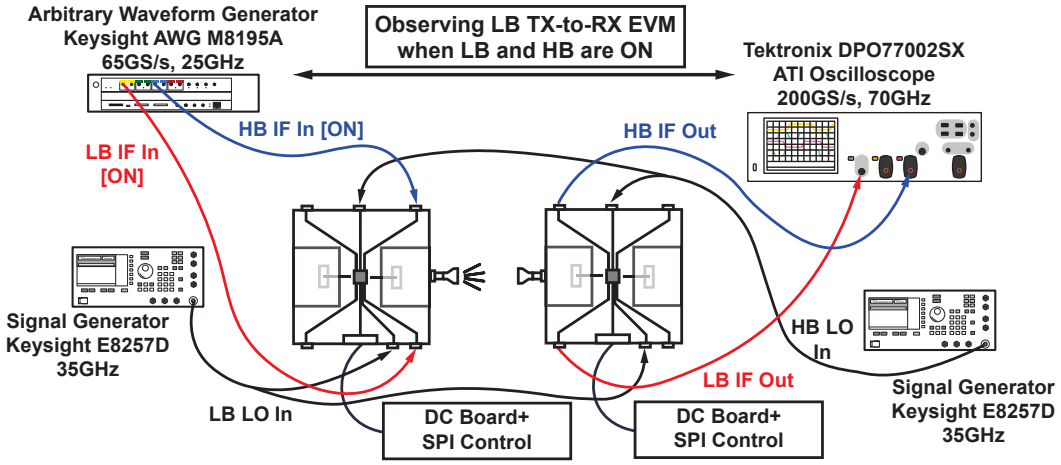


Figure 5.33: Setup for transmitter-to-receiver wireless communication error vector magnitude (EVM) measurements, when both LB and HB IF inputs are ON and EVM observed for LB.

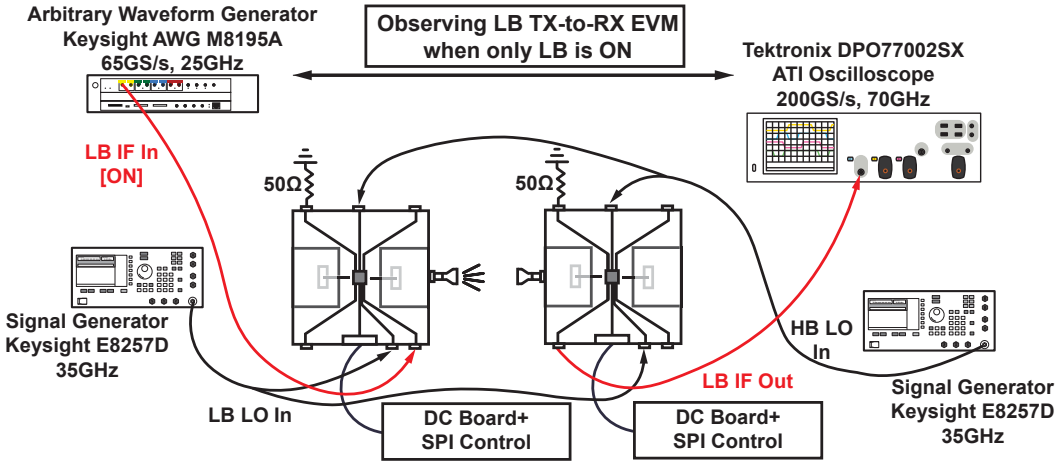


Figure 5.34: Setup for transmitter-to-receiver wireless communication error vector magnitude (EVM) measurements, when only LB IF input is ON (HB IF is OFF) and EVM observed for LB.

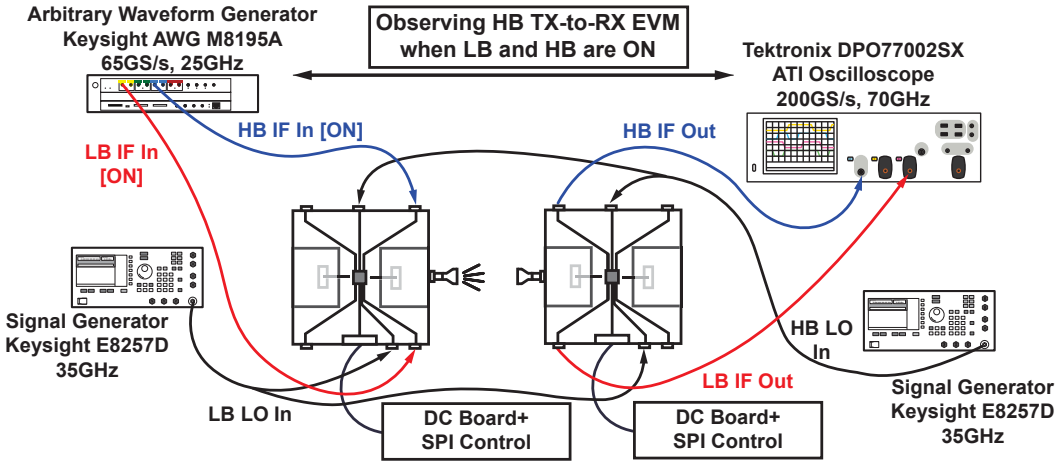


Figure 5.35: Setup for transmitter-to-receiver wireless communication error vector magnitude (EVM) measurements, when both LB and HB IF inputs are ON and EVM observed for HB.

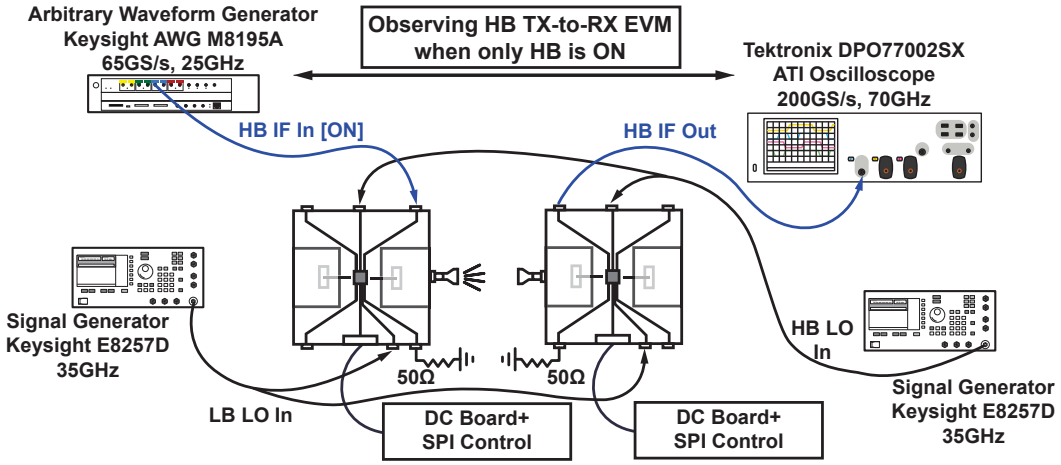
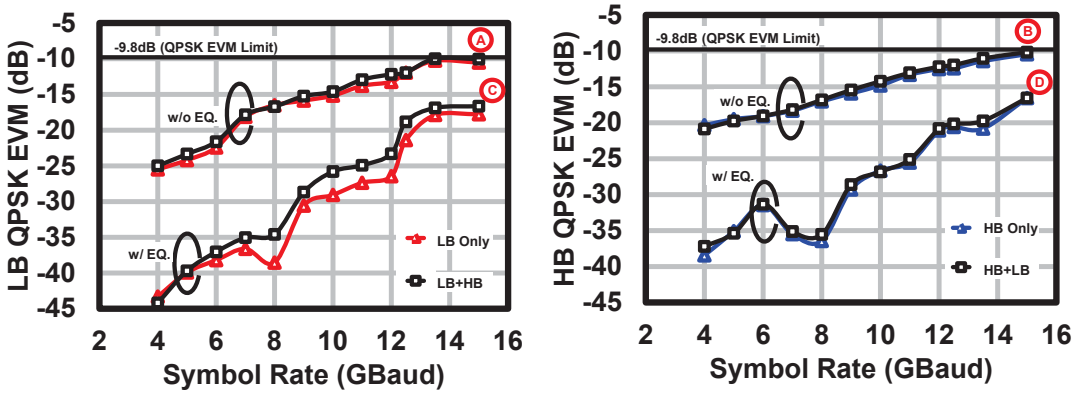
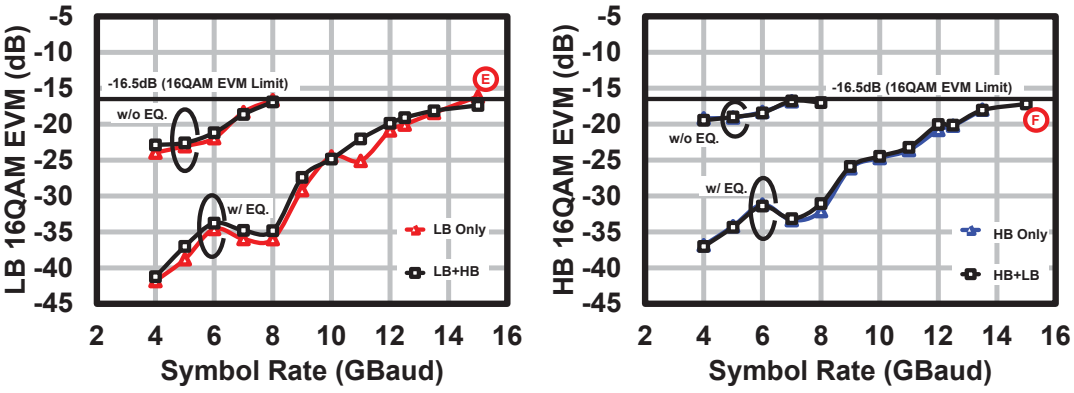


Figure 5.36: Setup for transmitter-to-receiver wireless communication error vector magnitude (EVM) measurements, when only HB IF input is ON (LB IF is OFF) and EVM observed for HB.



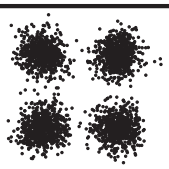
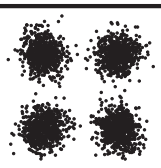
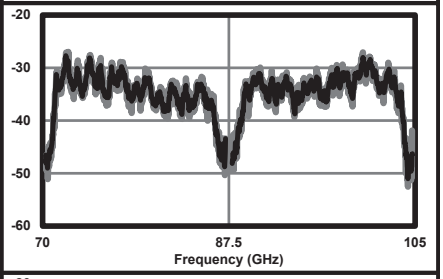
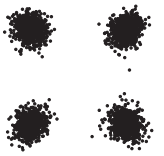
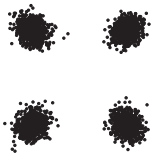
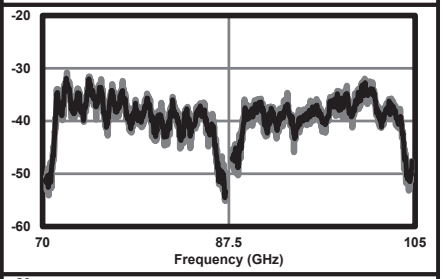
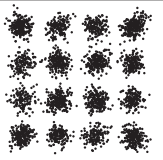
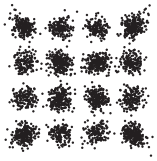
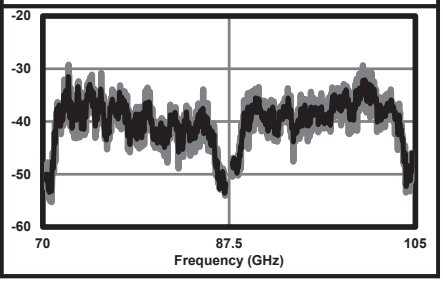
(a) (b)

Figure 5.37: Transceiver EVM measurement results (The QPSK EVM requirement of -9.8dB is also indicated in the figure for a BER of 10^{-3}.). (a) LB EVM for symbol rates from 4GBaud to 15GBaud QPSK. With or without equalization cases are shown when both LB and HB TX IF are ON and LB RX out is observed, and only LB TX IF is ON and LB RX IF out is observed. (b) HB EVM for symbol rates from 4GBaud to 15GBaud QPSK. With or without equalization cases are shown when both LB and HB TX IF are ON and HB RX out is observed, and only HB TX IF is ON and LB RX IF out is observed.



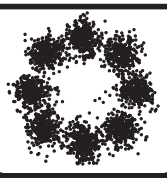
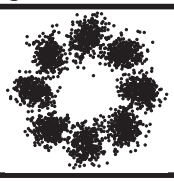
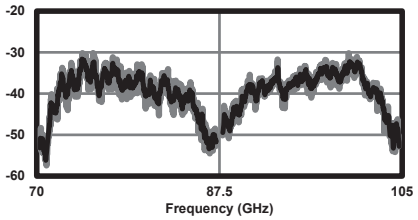
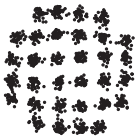
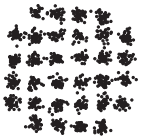
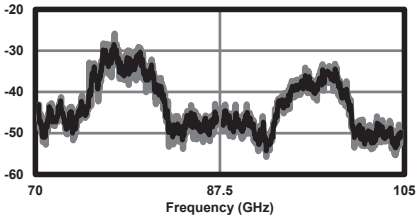
(a) (b)

Figure 5.38: Transceiver EVM measurement results (The 16QAM EVM requirement of -16.5dB is also indicated in the figure for a BER of 10^{-3}.). (a) LB EVM for symbol rates from 4GBaud to 15GBaud 16QAM. With or without equalization cases are shown when both LB and HB TX IF are ON and LB RX out is observed, and only LB TX IF is ON and LB RX IF out is observed. (b) HB EVM for symbol rates from 4GBaud to 15GBaud 16QAM. With or without equalization cases are shown when both LB and HB TX IF are ON and HB RX out is observed, and only HB TX IF is ON and LB RX IF out is observed.

Carrier Freq.	Low-Band 70GHz	High-Band 105GHz	Transmitter Output Spectrum**
TX-to-RX Constellation QPSK*			
Symbol Rate	15GBaud	15GBaud	
EVM	-10.8dB Ⓐ	-11.2dB Ⓑ	
Data Rate	60Gbps		
TX-to-RX Constellation QPSK*			
Symbol Rate	15GBaud	15GBaud	
EVM	-16.7dB Ⓒ	-16.5dB Ⓓ	
Data Rate	60Gbps		
TX-to-RX Constellation 16QAM*			
Symbol Rate	15GBaud	15GBaud	
EVM	-16.9dB Ⓔ	-17.0dB Ⓕ	
Data Rate	120Gbps		

*23dBi horn antennas are used for TX and RX. Communication distance is 0.2m including the loss from module.
**Roll-off factor is 0.13 in all cases above, total occupied band is 70-105GHz, spectrum is normalized for LB&HB.

Figure 5.39: TX-to-RX wireless communication measurement results for 30GBaud QPSK without and with equalization (60Gbps), and 30GBaud 16QAM with equalization (120Gbps).

Carrier Freq.	Low-Band 70GHz	High-Band 105GHz	Transmitter Output Spectrum**
TX-to-RX Constellation 8PSK*			
Symbol-Rate	12GBaud	12GBaud	
EVM	-12.8dB	-12.8dB	
Data-Rate	72Gbps		71-104GHz
TX-to-RX Constellation 32QAM*			
Symbol-Rate	6GBaud	6GBaud	
EVM	-19.6dB	-19.8dB	
Data-Rate	60Gbps		75-100GHz

*23dBi horn antennas are used for TX and RX. Communication distance is 0.2m including the loss from module. Results are obtained without built-in software equalization. ** Roll-off factor is 0.35 in all cases above, spectrum is normalized for LB&HB.

Figure 5.40: TX-to-RX wireless communication measurement results for 24GBaud 8PSK without equalization (72Gbps), and 12GBaud 32QAM without equalization (60Gbps).

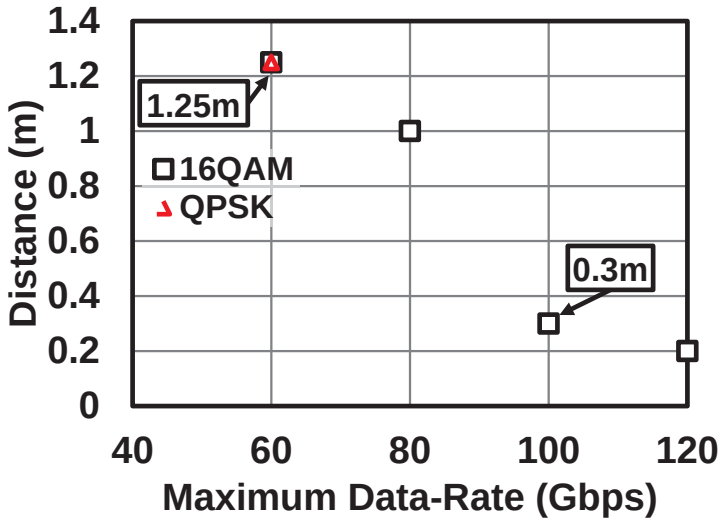


Figure 5.41: TX-to-RX wireless maximum data-rate measurement results for different distance.

Table 5.1: Comparison With Ultra-High Data-Rate Transceivers.

Ref.	Freq. [GHz]	Data-Rate (Modulation)	Symb. Rate [GHz]	TX P_{Out} [dBm]	Technology	P_{DC} [mW]	Die Area [mm^2]	Distance [m]
[87]	123-138	12.5Gb/s (OOK)#	12.5	9.5	55nm BiCMOS	TX: 59 RX: 38	3.2	5**
[88, 89]	235-245	16Gb/s (QPSK)#	8	0	65nm CMOS	TX: 220 RX: 260	4	0.02
[90]	148-162	20Gb/s (QPSK)#	10	-7	45nm SOI	TRX: 345	3.92	N/A*
[69, 70]	285-295	32Gb/s (16QAM)	8	-5.5	40nm CMOS	TX: 1400 RX: 650	8.34	0.01
[91]	56-67	50.1Gb/s (64QAM)	8.35	4.8	65nm CMOS	TX: 169 RX: 139	6	0.01
[92]	74-98	56Gb/s (16QAM)	14	-8.4	65nm CMOS	TX: 260 RX: 300	6	0.1
[22]	208-272	96Gb/s (8PSK)	32	-3.5	35nm GaAs	—	5	40**
This Work	70-105 75-100 73-102 71-104 70-105	60Gb/s (QPSK)# 60Gb/s (32QAM)# 64Gb/s (16QAM)# 72Gb/s (8PSK)# 120Gb/s (16QAM)	30 12 16 24 30	-1.9	65nm CMOS	TX: 120 RX: 160	6	0.2

* Wireline measurements ** With high-gain lens ant. # Without built-in software equalization

[87] N. Dolatsha *et al.*, ISSCC 2017 [88] S. Kang *et al.*, JSSC 2015 [89] S. V. Thyagarajan *et al.*, JSSC 2015
[90] Y. Yang *et al.*, RFIC 2014 [69] K. Takano *et al.*, ISSCC 2017 [70] S. Hara *et al.*, IMS 2017
[91] J. Pang *et al.*, ISSCC 2017 [92] K. K. Tokgoz *et al.*, ISSCC 2016 [22] F. Boes *et al.*, IMMTHz 2014

5.7 Conclusion

World fastest 120Gbps wireless TRX is presented on 65nm bulk CMOS. Frequency-interleave architecture for two data streams is employed while considering to lessen the burden of overall system. Issues of a frequency-interleave wireless TRX architecture is investigated in-depth and a wideband W-band TRX is proposed. Other than regular noise and distortion effects on SNDR of the whole system, cross-modulation is also an important factor that affects the performance of the whole system. Effective solutions to avoid cross-modulation on the TRX are proposed. Side band suppression for LB (up to 70GHz) and HB (after 105GHz) is achieved with the bandpass characteristics of PA, LNA, RF amplifiers and the waveguide interface. PFCS amplifiers are used for mm-wave frequency region to increase gain per stage and decrease the overall area and power consumption. A single-IF balanced mixer topology is proposed for LO leak cancellation while achieving single-ended IF and RF connections. LO leakage cancellation can be achieved by adjusting the gate bias voltages of balanced mixer transistors, differential LO buffers, and the DC offset cancellation current sources at IF ports of balanced mixer transistors. 0.3-20GHz IF amplifiers are designed and implemented in the wideband receiver. The two up- and down-conversion LOs are generated from an external 35GHz source by means of frequency doubling and tripling. Doubler and tripler design are made in considerations of harmonic suppression. First stages of doubler and tripler use the transistor non-linearity to generate the desired harmonics, whereas the following buffer stages designed to be narrowband to suppress the undesired LO harmonics. The suppression plays an important role while considering the cross-modulation issues on a frequency-interleave transceiver. Harmonic suppression value of more than 29dBc for doubler and 38dBc for tripler are realized based on the simulation results. A low-loss PCB to waveguide transition is designed. The results show a maximum of -3.9dB IL for the two transitions. TX, RX, and TX-to-RX measurements are conducted with the customized module. The TX achieves the best EVM for 5GBaud 16QAM of -24.3dB at the output power of -7.4dBm for LB, and -21.1dB at the output power of -9.4dBm for HB. For 5GBaud 16QAM RF signals, the RX has the best EVM of -25.6dB at the input power of -26.3dBm for LB and -24.7dB at the input power of -24.3dBm for HB. TX-to-RX EVM measurements indicate that cross-modulation does not degrade the performance of wireless communications. Only 0.9dB on LB and 0.6dB on HB EVM degradation are observed due to cross-modulations between LB and HB. Comparisons with literature clears that this work achieves the world fastest 120Gbps wireless communication with 65nm standard bulk CMOS. Total core area of the circuitry occupy 3.2mm^2 whereas the whole IC occupies 6mm^2 of

silicon area. TX power consumption is 120mW, and RX power consumption is 160mW.

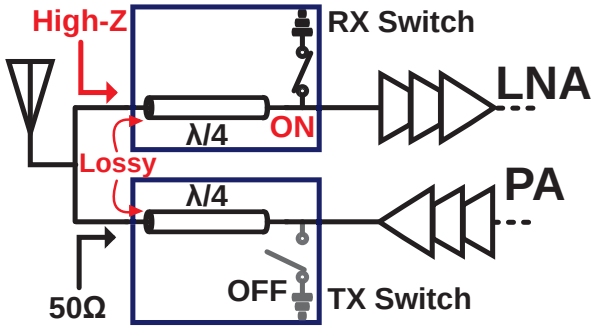
Chapter 6

Transmitter-Receiver Switch

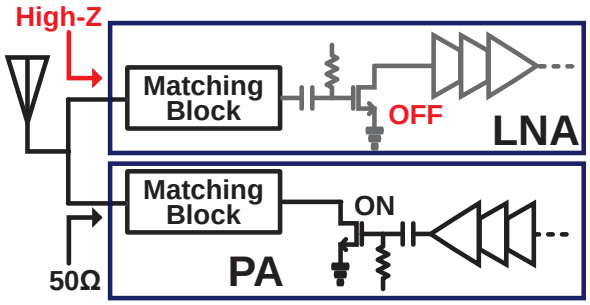
6.1 Introduction

Among millimeter-wave research and development, 60GHz unlicensed frequency region gets more attention due to larger available bandwidths [80, 91, 94–97]. As the demand for higher data-rate increases, requirements for multi-Gb/s mm-wave systems increases. Thus, phased arrays and multi-input multi-output (MIMO) systems become more and more popular. There are several antenna ports for phased array systems, and several transmitters and receivers for MIMO systems. Hence, number of antennas increases considerably in comparison with single transmitter/receiver systems. This also impact on the physical volume of the system and the total implementation cost of the system. As a result, transmit/receive switch for a mm-wave multi-Gb/s system is an advantageous block for sharing antennas [97–107]. It is crucial to decrease the loss of switch, while, also, care should be taken for noise figure (NF) of receiver (RX), and linearity of transmitter (TX). Area should be as small as possible. Although there are other topologies for switch architecture [101, 102, 106, 107], the common topology for antenna switch is based on quarter-wavelength (λ/4) [98–100, 104, 105]. The conventional switches introduce loss especially in mm-wave frequency region when compared to low-frequency applications. Thus, this topology has three main loss contributions for mm-wave applications. One is from the loss of the long λ/4 length (typically 600 to 700μm in standard CMOS) transmission lines (TLs) which can be up to 1dB depending on the process and TL structure, the other two is from the non-ideal ON and OFF impedances and additional parasitics of the switches and due to impedance mismatches. There is also loss in the matching blocks for PA and LNA input and output ports which cannot be avoided. The area consumption is, also, relatively large because of long TLs. Example for the transmitting mode for the conventional switch is shown in

Fig. 6.1(a). The switch on the RX side is ON for the transmit operation making the RX impedance high-Z. In here, an integrated antenna switch with PA and LNA is proposed and illustrated in Fig. 6.1(b). Opposite to the conventional switch operation, in transmitting mode LNA's first stage transistor is used as switch and is OFF. Matching block makes it high-Z impedance. Matching block also matches LNA to 50Ω during the receiving mode. Here, for lower loss and less area consumption, a 60GHz antenna switch is presented by re-using the last stage's transistor of PA and first stage's transistor of LNA and the matching blocks.



(a)



(b)

Figure 6.1: (a) Conventional quarter-wavelength based switching operation for transmitter mode, and (b) proposed integrated antenna switching operation for transmitter mode.

First of all, conventional quarter-wavelength base SPDT switches are investigated in terms of loss in the next section 6.2. The loss terms are related to the long quarter-wavelength transmission line loss, impedance mismatches due to non-ideal transistor switches, and non-ideal transformation of loss transmission line resulting with additional impedance mismatch and related losses. Section 6.3 presents the design and related analysis of the proposed integrated antenna switch architecture. The design approach for the proposed transmitter-receiver switch is introduced with considerations of losses, isolation and etc. The proposed design has lower loss compared to the conventional approach because the lossy long quarter-wavelength transformer is not used

and only there is one loss factor which is the impedance mismatch between the ON state LNA (or PA) and the OFF state PA (or LNA). In section 6.4, the measurement Test Element Groups (TEGs) are explained along with the measurement results. There are three TEGs for this part of the work. One is the overall transmitter-receiver switch architecture. The other two are stand alone LNA TEG and PA TEG for comparing the loss of the combination. Measurement results prove that receive mode has lower loss when compared to the conventional quarter-wavelength switch approach. Finally, section 6.5 concludes the paper with a comparison table of this work and other literature. This comparison clears that the proposed architecture has many advantages such as no additional silicon area occupation, lower loss and etc.

6.2 Conventional SPDT Switch Architecture

Conventional quarter-wavelength based switch is illustrated in Fig. 6.2.

Switch antenna, PA and LNA ports are matched to 50Ω. Moreover, PA and LNA input and output ports are matched to 50Ω with matching networks. In mm-wave frequency region these matching networks are also considerably lossy. The length of quarter-wavelength transmission line is about 600μm to 700μm in standard bulk CMOS process having loss about 0.5dB to 1.5dB depending on the structure of the transmission line. If one considers the total loss factors in this architecture from the last transistor of PA or until the first transistor of LNA, two main loss factors can be considered. One is the total loss of the SPDT switch and the other is the matching networks used in the amplifiers. The SPDT switch transistors can be controlled with a control voltage. Note that the drain of the switch transistors are not connected to DC supply. Otherwise, the switches consumes DC power which is undesirable. Ideal operation for RX mode is described in Fig. 6.3.

In ideal operation, TLs are lossless and switches are either open or short circuited. In the figure, RX mode of operation, PA is turned OFF and LNA is ON. For example, LNA gate biases are set to 0.7V and the matching network designed to match to 50Ω at this condition. V_{ctrl} is set to 1V. Hence, the receiver side switch is turned off having and infinite impedance. In parallel with LNA input impedance, impedance at that node is 50Ω. The transformation equation for a TL with length l is shown below. The impedance transformation of Eq. (6.1) approximates to Eq. (6.2) for a quarter-wavelength lossless TL. Hence the short circuited switch on TX side translates to ∞Ω, and the open circuited switch in parallel with 50Ω LNA input impedance translates to 50Ω and as a result the antenna port is also matched to 50Ω. At this perfect matched condition, there is no loss in the system except the lossy matching networks at mm-wave.

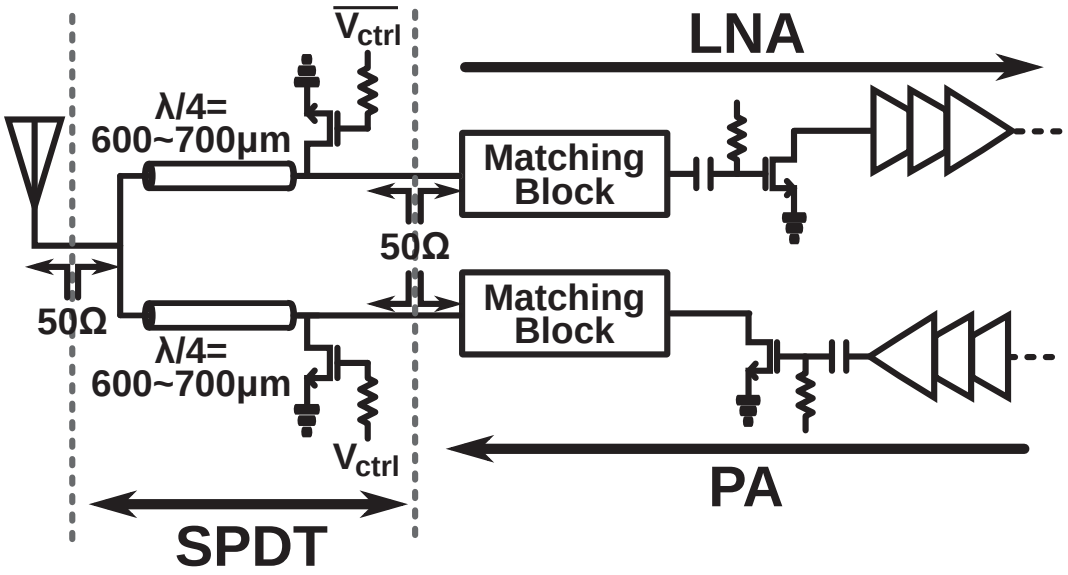


Figure 6.2: Conventional quarter-wavelength based SPDT switch with LNA and PA.

$$Z_{IN} = Z_0 \frac{Z_L + Z_0 \tanh(\gamma l)}{Z_0 + Z_L \tanh(\gamma l)} \tag{6.1}$$

$$Z_{IN} \simeq \frac{Z_0^2}{Z_L} \tag{6.2}$$

However, due to the non-ideal transistor characteristics and lossy TL, the practical case is different than the expected operation. These causes extra losses in the SPDT switch which directly affect the overall system performance. Below, analysis is done first for the non-ideal transistor characteristics with lossless TL, and last the non-ideal transistor characteristics with lossy TL. Fig. 6.4 presents the conventional SPDT switch in RX mode assuming lossless TL and non-ideal transistor switch. PA gate biases are set to 0V. LNA gate biases are set to a desired bias value. Switch transistor for RX side is set to 0V for desired high-Z impedance and the TX side switch transistor gate bias is set to 1V. In this case, a 120μm total width (2μm × 60) transistor is used for analysis. Note that parasitic capacitances are not included in the analysis for the sake of simplicity.

$$R_{EQ,RX} = R_{OFF} // Z_{LNA,ON} = \frac{R_{OFF} Z_{LNA,ON}}{R_{OFF} + Z_{LNA,ON}} \tag{6.3}$$

Fig. 6.5 represents the equivalent impedances connected to SPDT switch. The ON state resistance for the TX side switch transistor is 2.77Ω which translates to 833Ω after quarter-wavelength transmission line transformation. PA OFF state impedance excluded

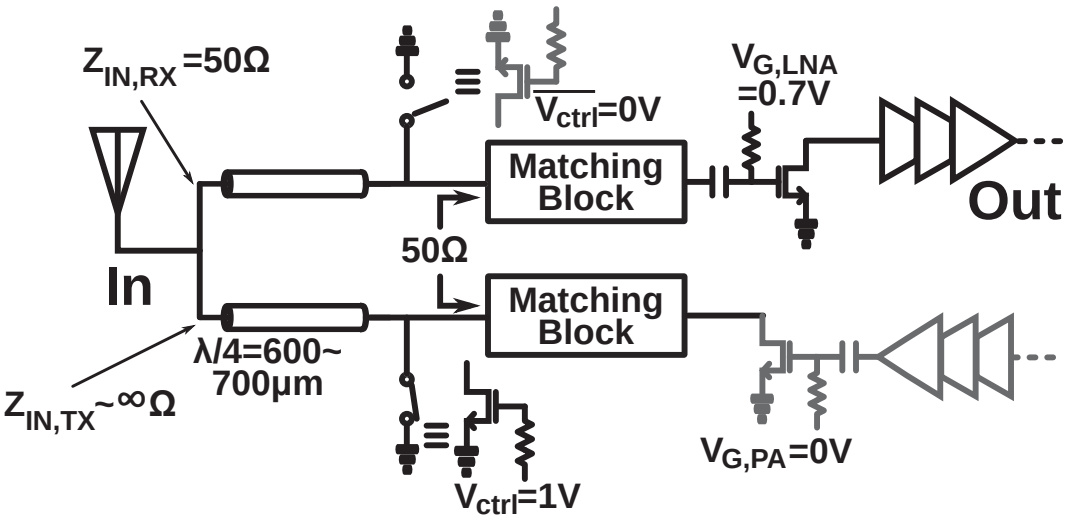


Figure 6.3: Ideal operation representation of conventional SPDT switch for receiver mode.

in the calculation since the ON state impedance of the switch transistor is low enough for this reason. The OFF state resistance of the RX side switch transistor is 152Ω. Since the OFF state resistance is not high-Z as desired, the equivalent RX impedance can be calculated as in Eq. (6.3) as 37.6Ω when the LNA input is matched to 50Ω, as represented in the figure right hand side. The equivalent impedance transforms to 66Ω at the antenna side with the quarter-wavelength transmission line transformation. The switch have loss due to the impedance mismatch between the ON state LNA input impedance and the switch transistor OFF state impedance, and can be calculated as in Eq. (6.4) as -1.23dB. This represented as the loss factor 2 in the figure. Even though the input impedance of the SPDT switch at TX side is relatively high impedance, still not high enough to neglect the loss due to impedance mismatch with the receiver input side impedance of the SPDT switch. Thus, some of the power at the antenna port is lost to TX side and can be calculated similarly as presented in Eq. (6.5). The loss to TX is calculated to be -0.31dB. This loss is indicated as 1 in the same figure.

$$\frac{P_{\text{Switch}}}{P_{\text{TOTAL}}} = \frac{R_{\text{OFF}}}{(R_{\text{OFF}} + Z_{\text{LNA,ON}})} \tag{6.4}$$

$$\frac{P_{\text{TX}}}{P_{\text{TOTAL}}} = \frac{Z_{\text{IN,TX}}}{(Z_{\text{IN,TX}} + Z_{\text{IN,RX}})} \tag{6.5}$$

Eq. (6.2) assumes the line is lossless. However, for mm-wave it is not anymore valid. The property for hyperbolic tangent given in Eq. (6.6) is equal to $1/\tanh(\alpha l)$ when length

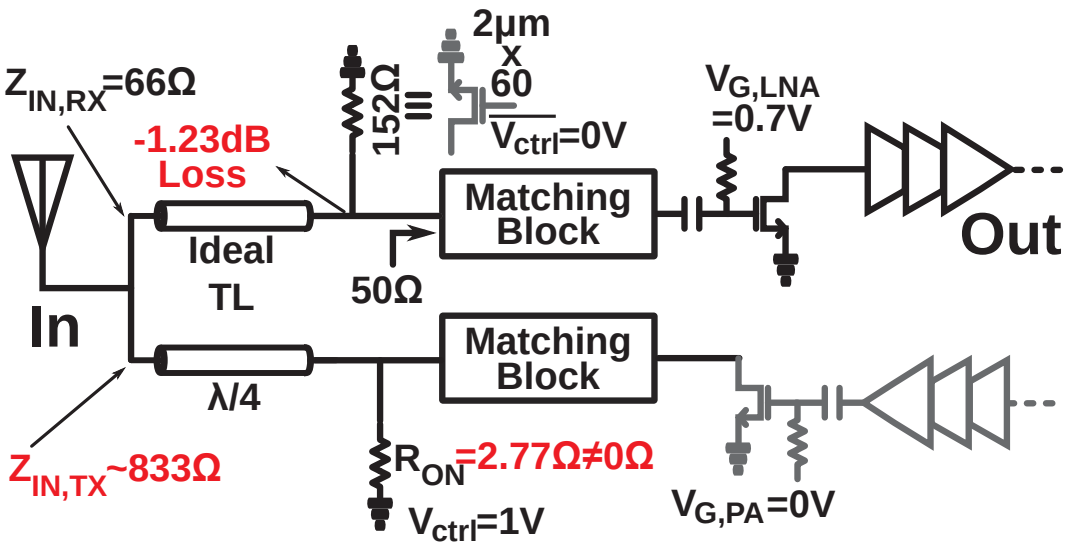


Figure 6.4: Conventional SPDT in RX mode with non-ideal transistor and lossless transmission line

of TL is $\lambda/4$ as shown in Eq. (6.7), and Eq. (6.1) results in Eq. (6.8).

$$\tanh(\gamma l) = \frac{\tanh(\alpha l) + \mathrm{j}\tanh(\beta l)}{1 + \mathrm{j}\tanh(\alpha l)\tanh(\beta l)} \tag{6.6}$$

$$\lim_{l \to \lambda/4} \tanh(\gamma l) = 1/\tanh(\alpha l) \tag{6.7}$$

$$Z_{\mathrm{IN}} \simeq Z_0 \frac{Z_{\mathrm{L}} + Z_0(1/\tanh(\alpha l))}{Z_0 + Z_{\mathrm{L}}(1/\tanh(\alpha l))} \tag{6.8}$$

In our case, TL loss is modeled based on measurements as α=0.82dB/mm at 60GHz. This case is presented in Fig. 6.6. Again the PA is OFF and LNA is set to a desired gate bias condition.

Total quarter-wavelength transmission line loss is -0.52dB for a transmission line length of 630μm. Based on the Eq. (6.8), $Z_{\mathrm{IN,TX}}$ and $Z_{\mathrm{IN,RX}}$ are recalculated as 440Ω and 64Ω, respectively. Hence, the loss of Eq. (6.5) is increased to -0.59dB, almost doubled from the previous case. The increase in this loss due to the decrease OFF state impedance of the SPDT switch TX side input impedance from 833Ω to 440Ω. The three loss factors and equivalent representation of the system is illustrated in Fig. 6.7. Quarter-wavelength transmission line loss is included in the figure as point 3.

The loss terms versus the OFF-state switch impedance described as above are plotted and illustrated in Fig. 6.8 with an assumption of -0.52dB TL loss for a 630μm length.

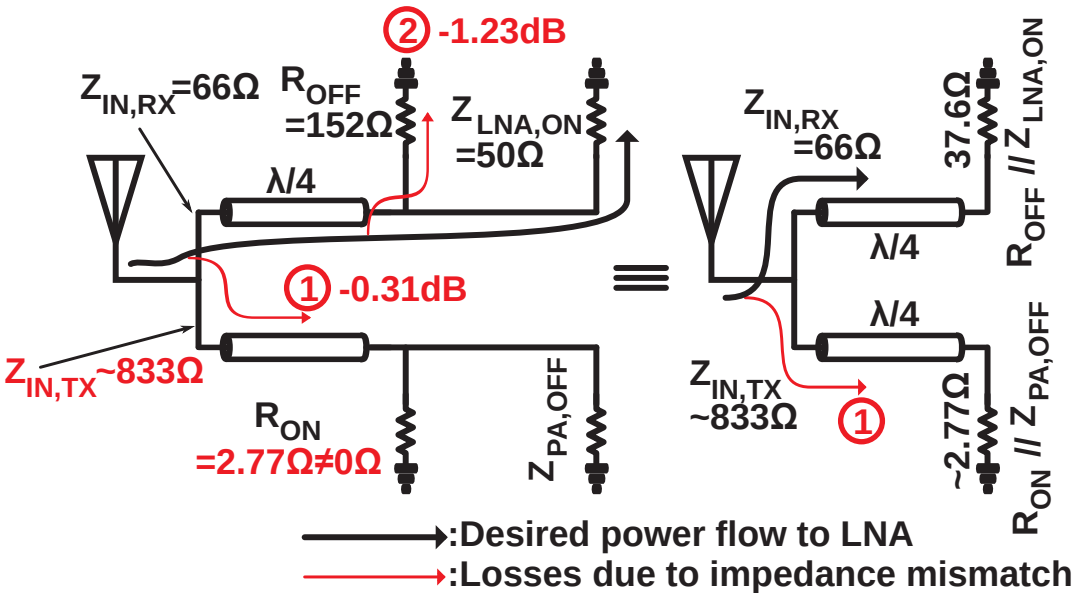


Figure 6.5: Equivalent representation with detailed loss factors due to impedance mismatches.

The OFF to ON impedance ratio of the transistor is simulated to be 55 based on the developed models for millimeter-wave transistors as explained in Chapter 3. Lower side horizontal axis is the OFF state impedance of the switch transistor and the upper side horizontal axis is the equivalent ON state impedance of the switch transistors. As mentioned the ratio is more or less close to 55 for all transistor sizes. The dashed black line in the figure represents the loss to the TX side from the antenna port due to impedance mismatch. This loss is mainly affected by the ON state resistance of the switch transistor since it is transformed to high-Z at the TX port of the SPDT switch. Such that, lower ON state impedance is desirable. The solid gray line represents the loss factor to the switch transistor due to the impedance mismatch between the LNA input and the switch impedance. In this case it has a decreasing attitude as the OFF state impedance increases as expected. Such that, higher OFF state switch transistor impedance is desirable for lower loss to the switch itself. As a result, the solid black line represents the total loss of the SPDT switch. Since the other two loss factors have contradicting behaviour, there is a sweet spot for the total loss. The total loss of a conventional quarter-wavelength based switch results in a minimum of around -2dB. Note that the loss terms from the matching blocks of LNA and PA are not included here.

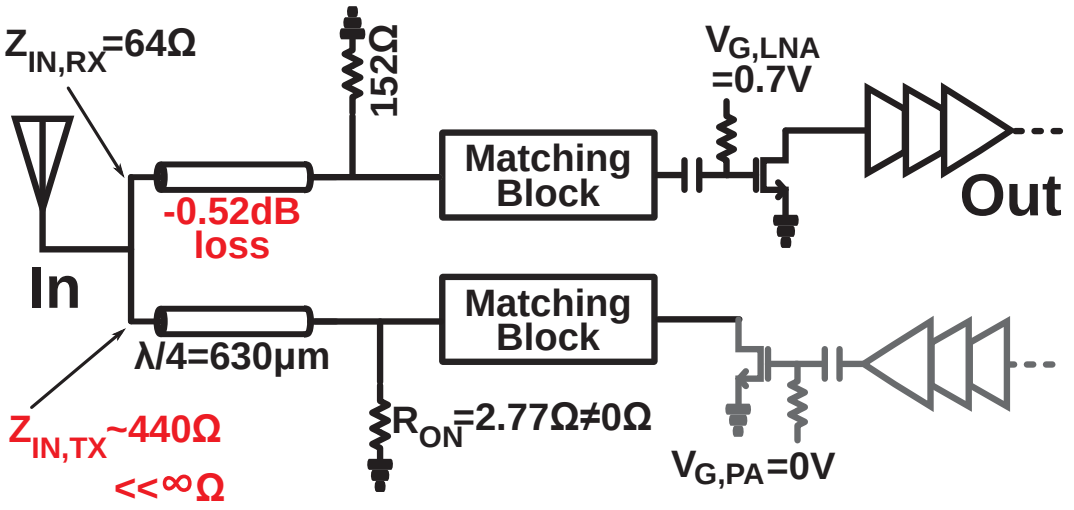


Figure 6.6: Conventional SPDT in RX mode with non-ideal transistor and lossy transmission line causing non-ideal impedance transformation.

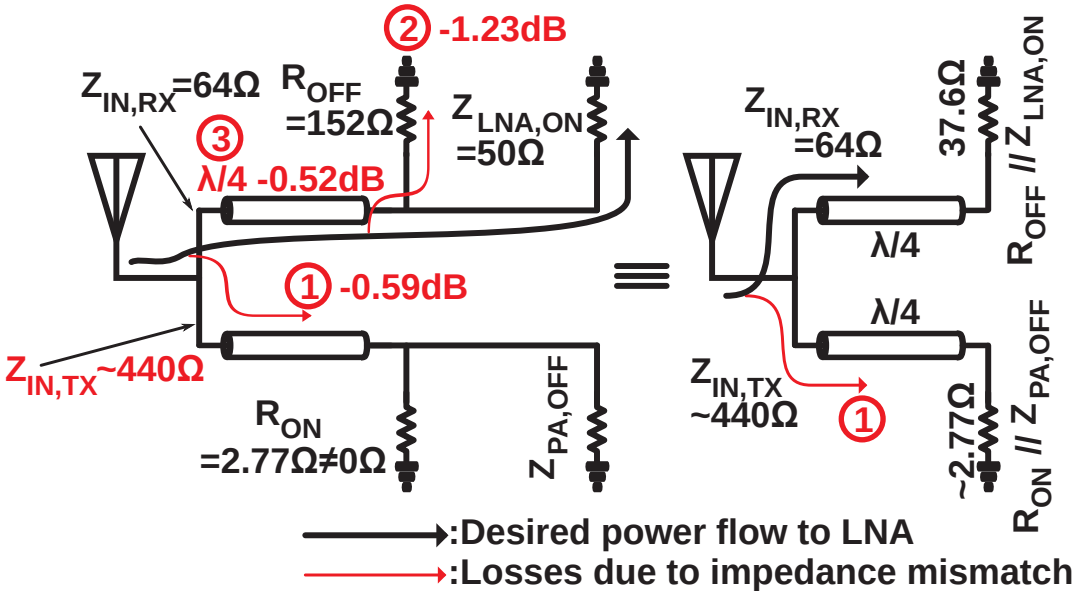


Figure 6.7: Equivalent representation with detailed loss factors due to impedance mismatches and transmission line loss.

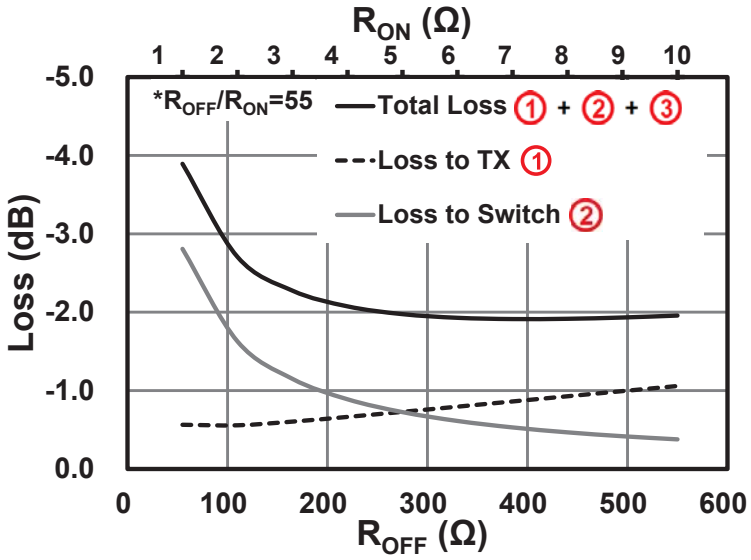


Figure 6.8: Calculated loss factor for the conventional SPDT in Fig. 6.7 vs the switching transistor ON or OFF resistance values.

6.3 Proposed Integrated Antenna Switch

Considering the total loss of a conventional switch on bulk CMOS, in here, lower loss integrated antenna switch architecture is proposed. The concept is illustrated in Fig. 6.9. In the proposed case, matching blocks of LNA input and PA output are designed along with the considerations of switching transistors, that is based on re-using the transistors of PA's last stage and LNA's first stage. The switching biases are different than most transmit/receive switches. In TX mode, the PA transistor gate biases are set to 0.7V considering gain and linearity of TX whereas the LNA gate biases are 0V. For both LNA and PA transistors drain voltage is 1V either for ON or OFF cases. In conventional switches, drain of the transistors are set to 0V (or sometimes, although undesired, floating gate). The size of the PA transistor is selected as 120μm total width (2μm × 60) for higher saturated output power and linearity. In RX mode, the LNA transistor gate biases are set to 0.55V considering NF of RX whereas the PA gate biases are 0V. Again, for both LNA and PA transistors drain voltage is 1V either for ON or OFF cases. The size of the LNA transistor is selected as 36μm total width (1.5μm × 24) for lower NF and gain. The output matching network of PA and input matching network of LNA are directly connected to each other after designed separately to the antenna port pad. While designing the matching networks PA last stage transistor drain ON and OFF impedance, and LNA first stage transistor gate ON and OFF impedance are considering for the switching mode impedances. The output of LNA and input of PA have separate pads for measurements.

Fig. 6.10 represents the impedance seen from the gate of the first-stage transistor of LNA when the biases are 0.55V for RX mode and 0V for TX mode. Furthermore, the impedance seen from the drain of the last-stage transistor of PA when biases are 0V for RX mode and 0.7V for TX mode. The impedance information given in this figure is at 60GHz for all cases. RX mode LNA transistor gate impedance is $Z_{LNA,ON} = (17.7 - j37.1)\Omega$ which can be modeled as parallel connected resistance of 59.8Ω and 92.9fF capacitance. RX mode PA transistor drain impedance is $Z_{PA,OFF} = (4.4 - j33.2)\Omega$ which can be modeled as parallel connected resistance of 243Ω and 81.5fF capacitance. TX mode LNA transistor gate impedance is $Z_{LNA,OFF} = (43.8 - j90.3)\Omega$ which can be modeled as parallel connected resistance of 142Ω and 38fF capacitance. TX mode PA transistor drain impedance is $Z_{PA,ON} = (7.8 - j9.8)\Omega$ which can be modeled as parallel connected resistance of 4.4Ω and 760fF capacitance.

Note that the ON/OFF impedance difference for LNA case is much higher than that of PA. Because of this reason and the importance of RX gain, and NF; the design of LNA input matching block has the priority considering with high ON/OFF LNA input

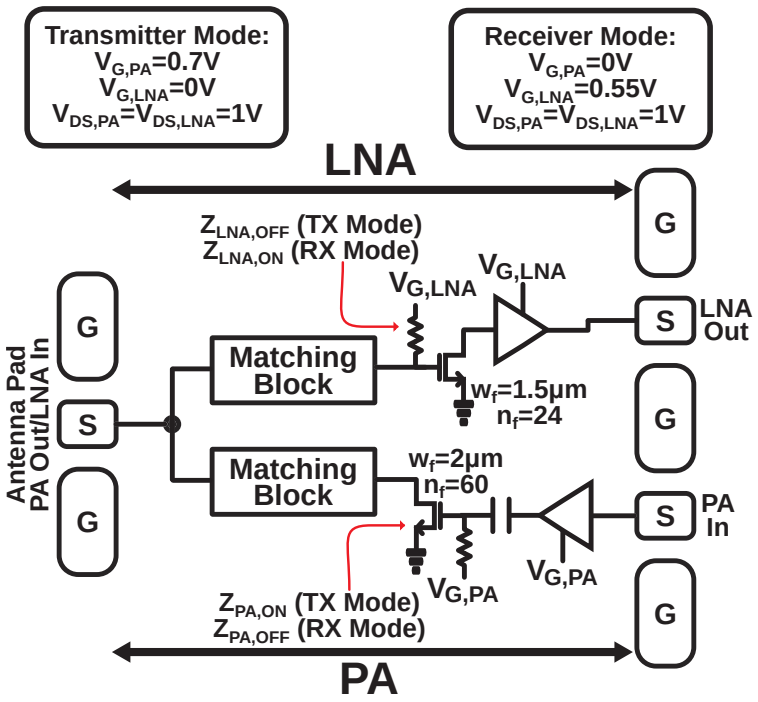


Figure 6.9: Concept of the integrated antenna (transmitter-receiver) switch.

impedance ratio. Considering both the ON and OFF impedances of LNA first-stage transistor, a matching block design is presented in Fig. 6.11.

In the same figure the impedances at 60GHz are indicated. Moreover, design is illustrated based on simulations on Smith Chart in Fig. 6.12.The output of the LNA is matched to 50Ω with the GSG pad when the LNA works in the RX mode that is the gate bias is set to 0.55V. Transistor size used for the LNA has a total width of 36µm (1.5µm × 24). Biasing resistor is 5kΩ and modeled beforehand as explained in Chapter 3. The impedance at the gate of the transistor are indicated as $Z_{LNA,ON}$ = (17.7 − j37.1)Ω and $Z_{LNA,OFF}$ = (43.8 − j90.3)Ω. A 150fF DC cut capacitor is placed before the gate of the transistor for bias and a 115µm TL is placed. The impedance seen from this point is indicated as point '1' before the shunt short-circuited TL. A 157.5µm short-circuited stub is used to match the ON state impedance to 50Ω and that impedance is indicated as point '2'. With the same stub, the OFF state impedance become inductive. However, in this case the ON/OFF ratio is not high as desired. Hence, another series 115µm TL is placed. By this way, the ON state impedance still near 50Ω whereas the OFF state impedance become higher than the previous case. The LNA input impedance labels are $Z_{LNA-IN,ON}$ = (53.2 + j6.8)Ω and $Z_{LNA-IN,OFF}$ = (40.4 + j71.7)Ω. Inductive load is required for the OFF state impedance because when PA and LNA are combined the

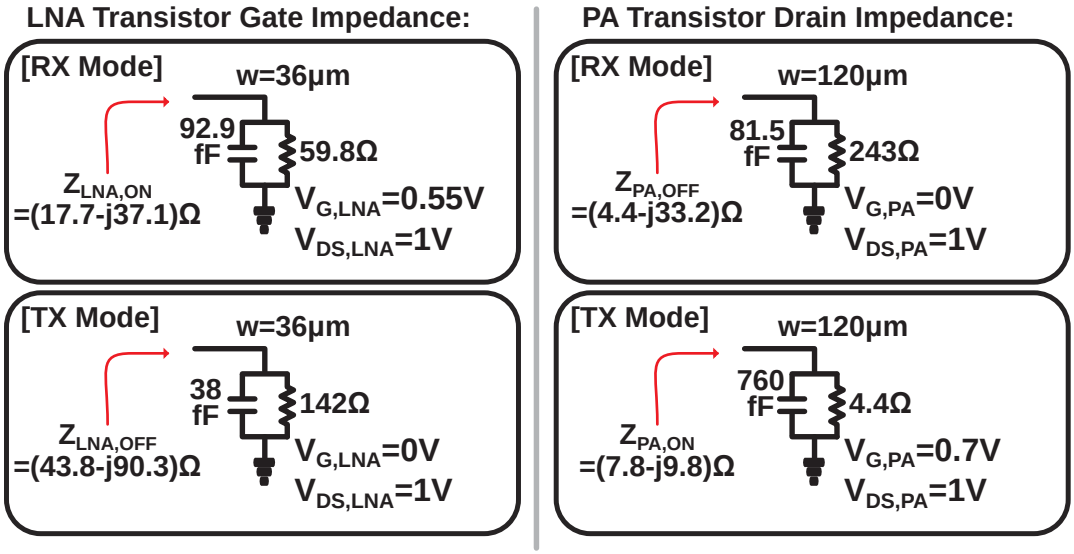


Figure 6.10: LNA first-stage transistor gate impedance for ON and OFF states and PA last-stage transistor drain impedance for ON and OFF states at 60GHz.

parasitic capacitance of the pad has to be accounted (Fig. 6.15).

Fig. 6.13 presents the PA output matching block design. Similarly, the impedance transformations at 60GHz are illustrated in the same figure. Moreover, the impedance transformations for the PA design is shown on Smith Chart in Fig. 6.14. Since the ON/OFF impedances seen from the drain side of the last-stage transistor of PA are very close, higher ON/OFF ratio is more difficult to design as compared to LNA case. The impedance at the drain of the transistor are indicated as $Z_{PA,ON} = (7.8 - j9.8)\Omega$ and $Z_{PA,OFF} = (4.4 - j33.2)\Omega$. A load connected to VDD is used right after the drain and these impedances are labeled as $Z_{PA1,ON}$ and $Z_{PA1,OFF}$. In order to block the DC flowing through the LNA and avoid VDD-GND short circuiting a 150fF of DC cut capacitor is used before the antenna port. To match the impedances after the load and before the DC cut capacitor, a 170µm open-circuited stub is used after a 170µm series TL. These points are indicated as points '2' and '3' in the schematic. PA input port is matched to 50Ω.

The combined schematic is shown in Fig. 6.15. The design is made considering the pad parasitics equivalent to 27fF. Details of the circuit with the other amplifying stages in the PA and LNA are given in the following sections.

The RX mode of the combined circuitry is shown in Fig. 6.16. The PA transistor OFF state equivalent circuit is shown in the figure and the matching blocks are the same as explained before. Thanks to the high impedance of the PA OFF state ($Z_{PA-OUT,OFF} = (29.5 + j66.1)\Omega$), the loss to TX is calculated to be as low as -1.3dB at 60GHz. Whereas

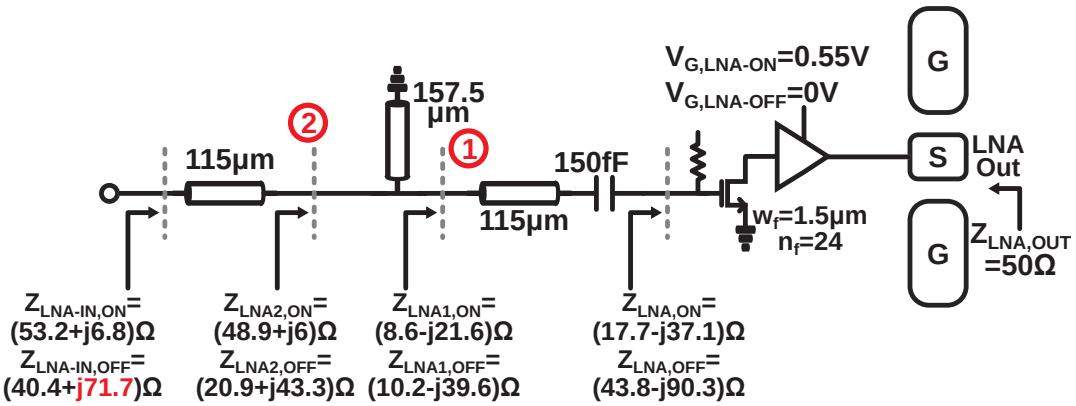


Figure 6.11: Design of LNA input matching block for TRX operation at 60GHz.

the ON state LNA input impedance is close to 50Ω match condition with $Z_{LNA-IN,ON}$ = (53.2 + j6.8)Ω. The combined impedance translates to the antenna port impedance in considerations with the pad parasitics is $Z_{IN,RX}$ = (47 + j11.5)Ω. The return loss in this case is low since impedance value is very close to 50Ω match condition. The loss of -1.3dB value is as low as the loss of a switching transistor in a conventional quarter-wavelength based SPDT switch. The antenna input impedance is very close to 50Ω.

Similarly, the TX mode of the circuitry is shown in Fig. 6.17. The LNA transistor OFF state equivalent circuit is shown in the figure and the matching blocks are the same as explained before. In this case, the ON state output impedance of PA is close to the OFF state impedance of LNA and hence it is not well matched to 50Ω mostly due to the required DC cut capacitor. The loss is around -2.4dB at 60GHz. The ON state output impedance of PA is $Z_{PA-OUT,ON}$ = (38.7 + j39.1)Ω, and the OFF state input impedance of LNA is $Z_{LNA-IN,OFF}$ = (40.4 + j71.7)Ω. The parallel combination of these two impedances translates to the output impedance of the whole system at the antenna port as Z_{OUT} = (48.5 + j33)Ω together with the pad parasitic capacitance, which results in a return loss of around -10dB.

One of the important point to be cleared out is the isolation from PA to LNA, as indicated in Fig. 6.17. The coupled power to the first-stage LNA transistor gate from the PA may open and close the transistor if the output power is large and the isolation is not enough. The value is the threshold value of the transistor which is around 0.4V. The peak voltage amplitude versus the output power from PA is calculated for different isolation values and plotted in Fig. 6.18. For instance, for a TX output power of 3dBm an isolation of 10dB is enough to preserve linearity of the TX mode. For a moderate power mm-wave transceiver system 10dB isolation is enough. However, if more output power system is

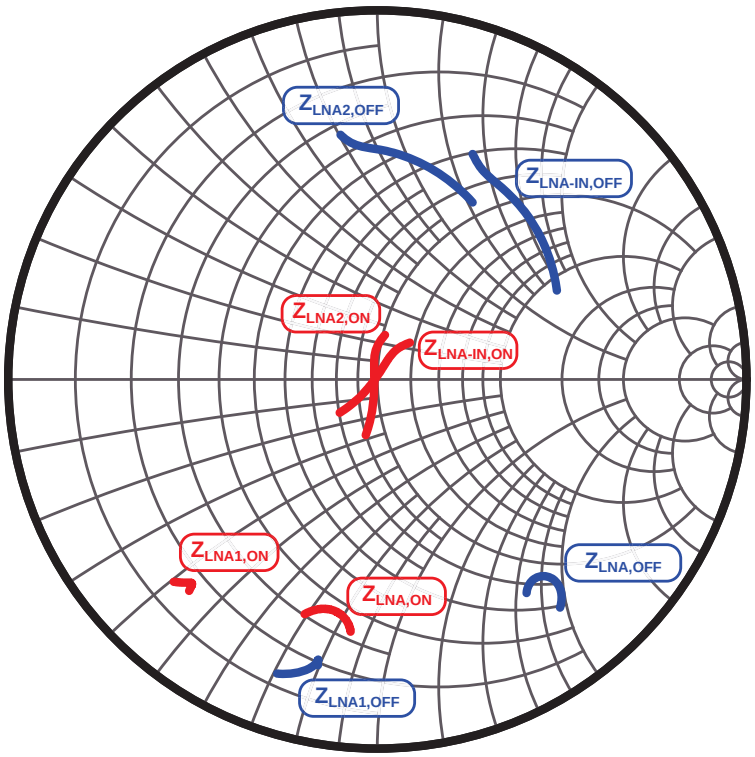


Figure 6.12: Simulated impedance results on Smith Chart from 57 to 66GHz for LNA input matching design.

desired, the isolation should be more as illustrated in Fig. 6.18.

A conceptual design is made for a two-stage LNA and a two-stage PA. The schematic of the antenna switch circuitry is shown in Fig. 6.19. All of the transmission line lengths are included in the figure. MIM transmission lines are used for DC feed networks for DC to RF isolation. As stated in Chapter 3, MIM TLs have very low impedance and wideband characteristics enabling DC to RF isolation. All DC-cut capacitors used in the circuit are 150fF. The LNA transistor size is 36µm (1.5µm$\times$24), and the PA transistor size is 120µm (2µm $\times$ 60).

Based on this circuit, the isolation from the last-stage transistor output of PA to the first-stage transistor input of LNA is simulated and presented in Fig. 6.20(a). The simulated isolation is less than -10dB in the band of interest from 57 to 66GHz. This much isolation is enough for moderate power applications as stated above. Moreover, time domain simulation is made for TX output power of 1.6dBm (simulated OP_{1dB} point) and illustrated in Fig. 6.20(b). The antenna output time domain signal is illustrated in black and has a maximum of around 0.4V, and the coupled time domain signal to the

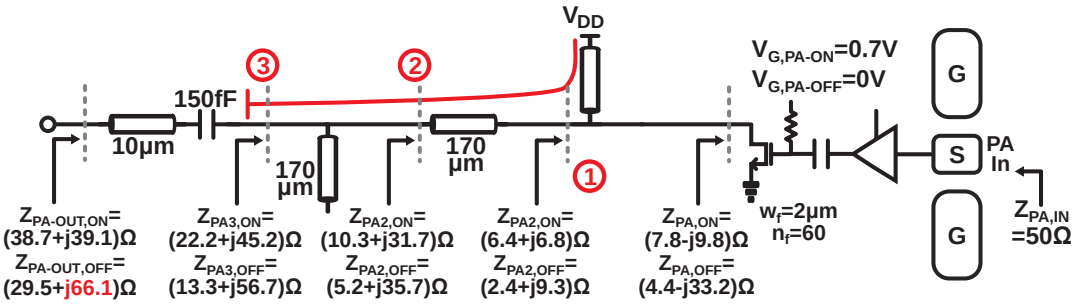


Figure 6.13: Design of PA output matching block for TRX operation at 60GHz.

gate of LNA transistor is shown in red color which has a peak value of around 0.3V ($< V_{th}$=0.4V). The LNA transistor output time domain signal is plotted in blue. One can observe that the peak is less than the input as expected. The design satisfies the requirement for the isolation.

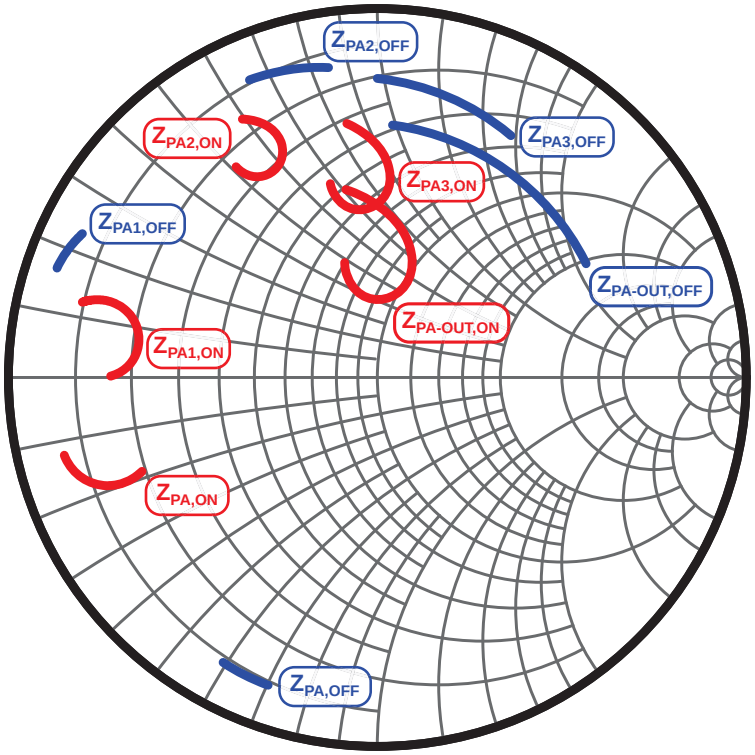


Figure 6.14: Simulated impedance results on Smith Chart from 57 to 66GHz for PA input matching design.

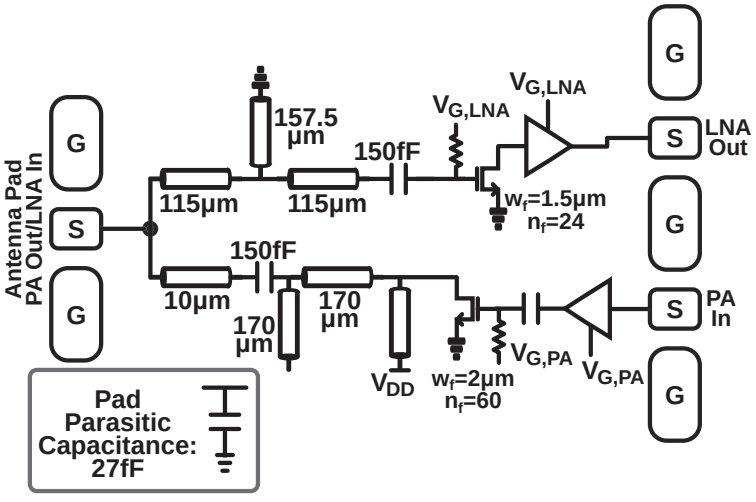


Figure 6.15: The integrated antenna (transmitter-receiver) switch.

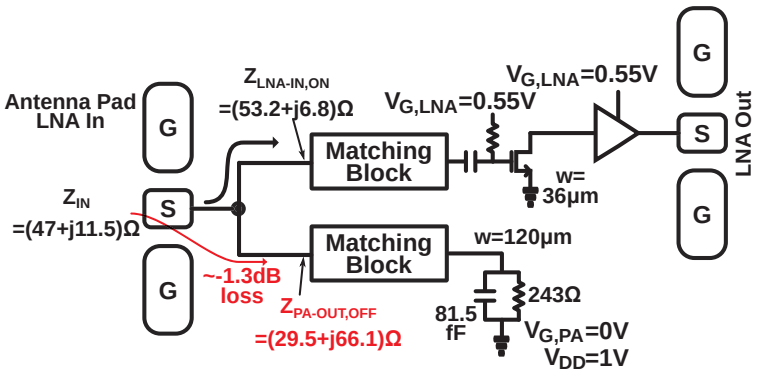


Figure 6.16: The principle of operation when the RX mode is active, the PA's last-stage transistor OFF drain impedance translated to high impedance at antenna side.

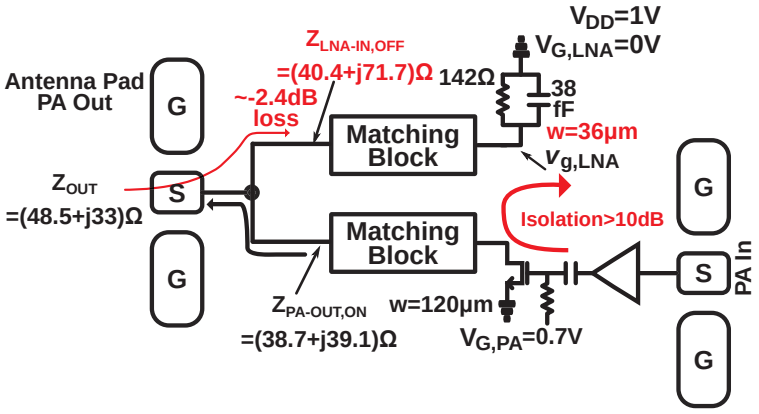


Figure 6.17: The principle of operation when the TX mode is active, the LNA's first-stage transistor OFF gate impedance translated to high impedance at antenna side.

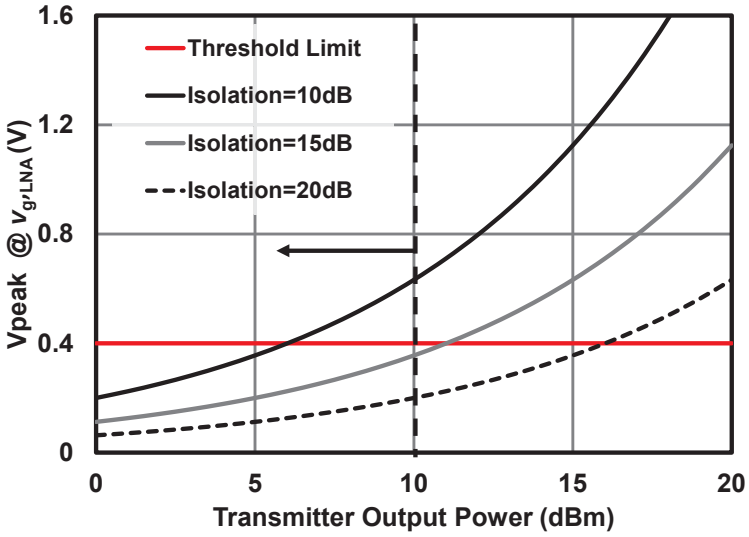


Figure 6.18: Peak voltage amplitude at the gate of LNA for different isolation values from TX to RX versus the output power of TX in dBm.

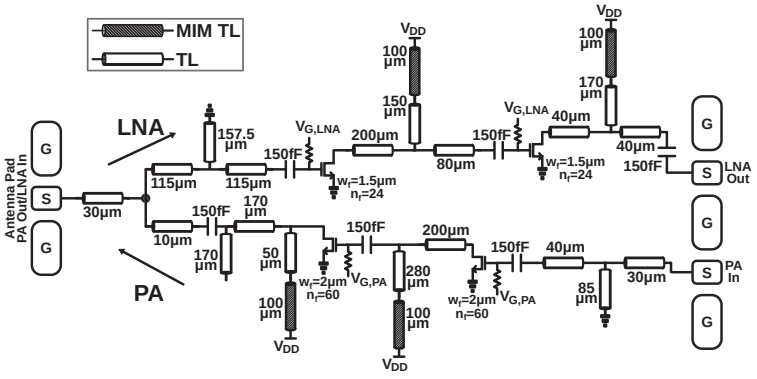
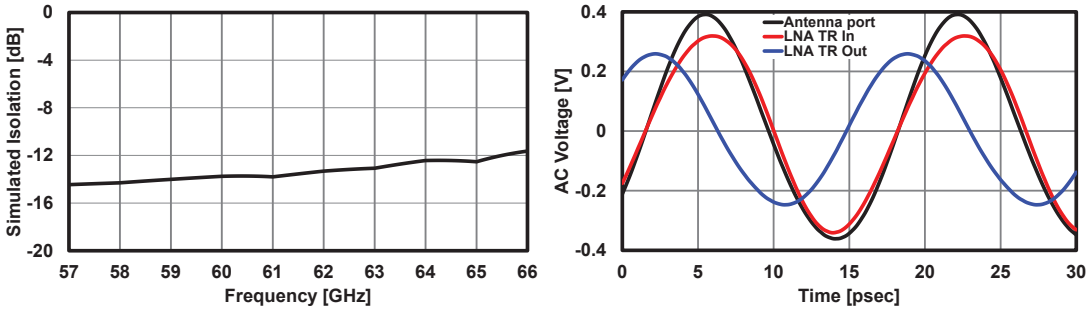


Figure 6.19: Overall schematic for proposed integrated antenna switching circuitry with two-stage PA and LNA.



(a) (b)

Figure 6.20: (a) Simulated isolation from PA last-stage transistor to LNA first-stage transistor, (b) comparison of simulated time domain voltage signals for TX mode at antenna output port (black line), LNA first-stage transistor input (red line) and output (blue line), when PA output power is 1.6dBm (OP_{1dB} point).

6.4 Measurement Structures and Results

LNA only (Fig. 6.21) and PA only (Fig. 6.22) Test Element Groups (TEGs) are implemented for comparison purposes. LNA output pad and PA input pad are incorporated in the design and these ports are matched to 50Ω in considerations with pad parasitics. However, LNA input pad and PA output pad are just added for measurements. After the measurements these pads are de-embedded for fair comparison since the design of PA and LNA does not include those pads. Port names are included in the figures.

All TEGs are implemented in 65nm bulk CMOS process. The overall designed antenna switch (schematic presented in Fig. 6.19) chip photo is shown in Fig. 6.23(a). The total area with pads is 0.78x0.68mm^2. Left hand side has a ground-signal-ground (GSG) pad as the antenna port. On the right hand side, a GSGSG pad is used. Upper signal pad is for the output of LNA and lower signal pad is for the input of PA. Only excess area is the output T-junction which combines them. This clears the area advantage. LNA only TEG chip photo is shown in Fig. 6.23(b), and PA only TEG chip photo is shown in Fig. 6.23(c). First of all, all circuits are measured with a Vector Network Analyzer (VNA). For comparison, as stated above, PA output pad and LNA input pad characteristics are de-embedded from PA only and LNA only TEG measurements.

Fig. 6.24(a) presents the antenna port return loss in RX mode for the switch circuit (red line) in comparison with LNA only TEG input port return loss (blue line) from 57 to 66GHz. As it can be observed when the LNA and PA is combined in considerations with antenna port pad parasitic capacitance, the return loss is close to 50Ω point on Smith Chart. Similarly, Fig. 6.24(b) presents the antenna port return loss in TX mode for the switch circuit (red line) in comparison with PA only TEG input port return loss (blue line) from 57 to 66GHz. PA only TEG return loss results are more far from the center of Smith Chart when compared to the combined circuits return loss results. From the perspective of matching on the antenna port of the switch circuit, one can say that both TX mode and RX mode are well matched. Red lines used in the two figures are for the transmitter-receiver switch circuit and blue lines are for PA or LNA only TEGs.

The measured gain of RX mode of antenna switch circuit (red line) and de-embedded LNA only circuit (blue line) are presented in Fig. 6.25(a). The results are presented from 57 to 66GHz. TRX switch LNA mode gain is around 10dB at 60GHz. The gain difference between the TRX switch LNA mode and the LNA only is between 1.1 to 1.7dB. The minimum value is much smaller than one can achieve with a conventional switch structure. The NF of TRX switch and LNA only TEG is measured and presented in Fig. 6.25(b). The red dots are the NF of TRX switch RX mode and the blue dots are the NF

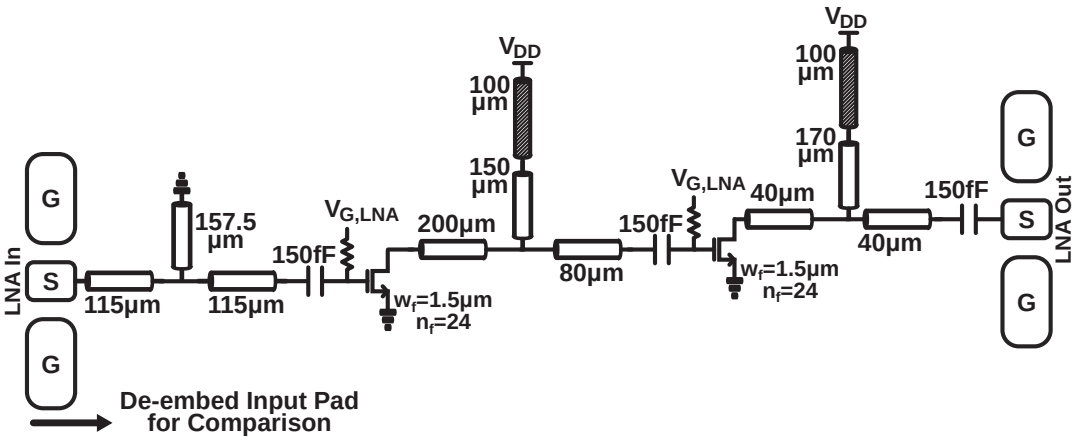


Figure 6.21: Schematics of LNA only Test Element Group (TEG) for comparison.

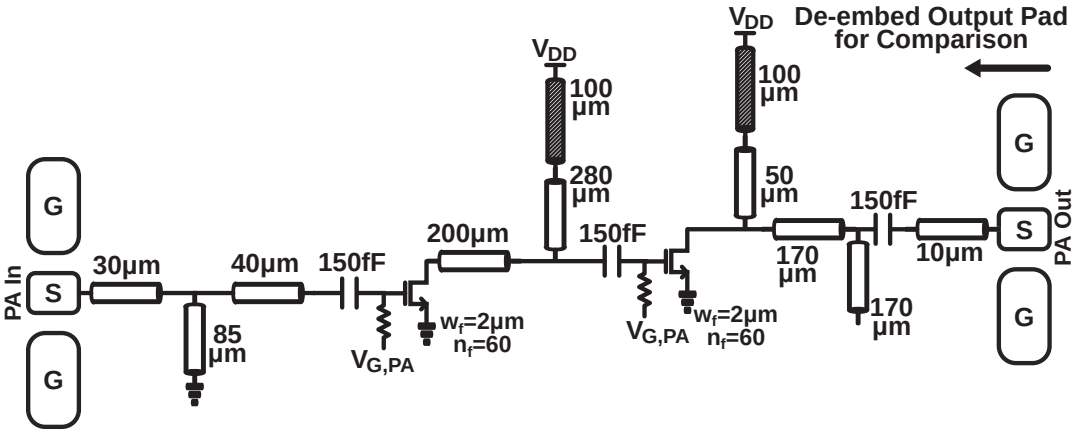


Figure 6.22: Schematics of PA only Test Element Group (TEG) for comparison.

of LNA only TEG. Moreover, black dots represents the NF degradation due to the LNA and PA combination of antenna switch circuitry. The NF degradation aligns with the gain degradation of LNA circuit. The NF of RX mode is measured to be 2.9dB at lowest. LNA only TEG has a NF as low as 1.9dB.

The measured gain of TX mode of antenna switch circuit (red line) and de-embedded PA only circuit (blue line) are presented in Fig. 6.26(a) from 57 to 67GHz. TRX switch PA mode gain has a maximum of around 12dB at 65GHz. PA only measured gain has a maximum of around 14dB around 65GHz. The gain difference between the TRX switch PA mode and the PA only is between 2.3 to 2.7dB. The difference is flat which is desired for a wideband system gain flatness. However, the introduced loss is higher than the LNA case. As explained in the previous section, it is mostly because of matching the PA

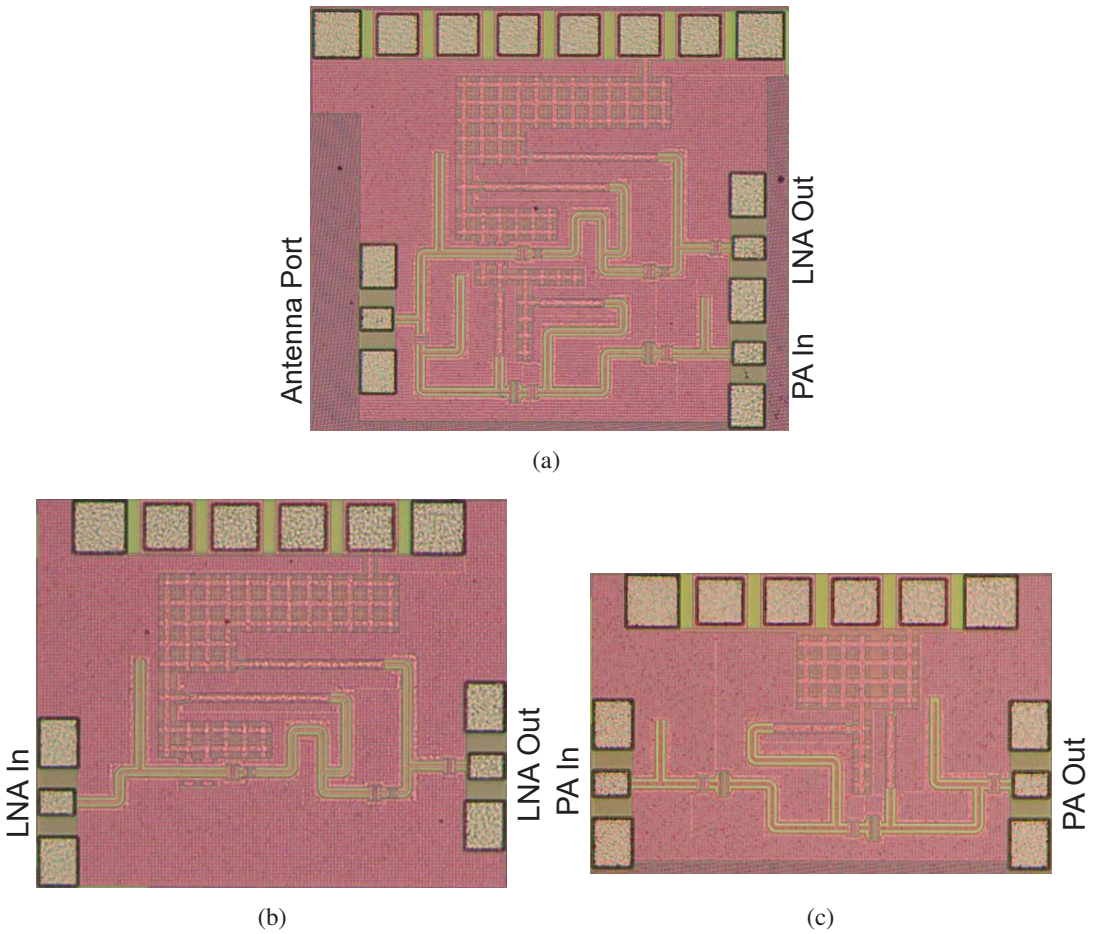
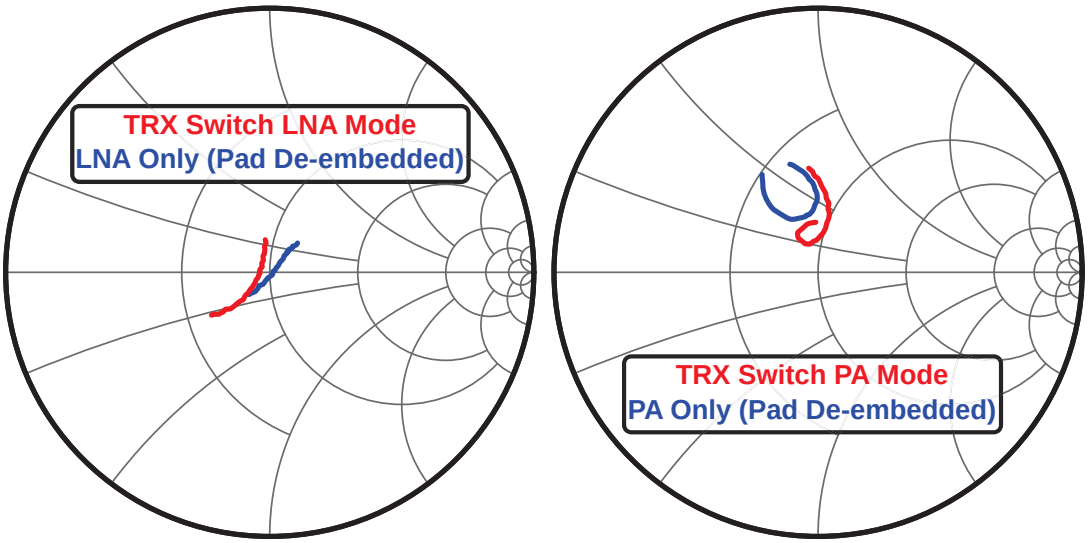


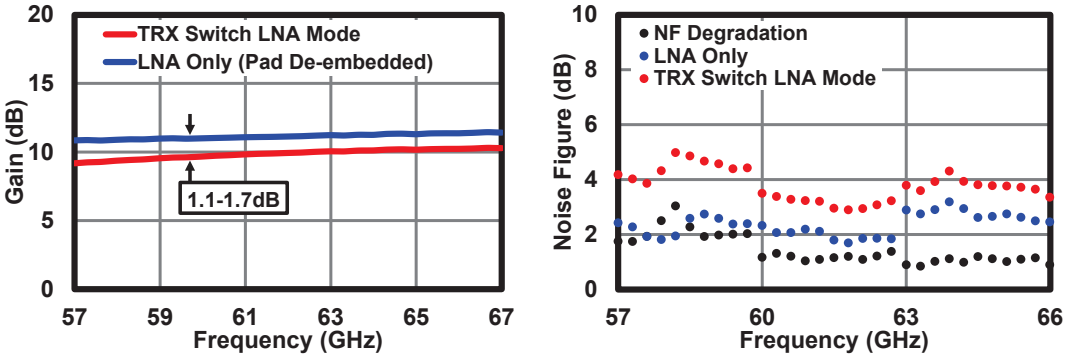
Figure 6.23: Measurement structures; (a) the chip photo for overall switch with a two-stage PA and a two-stage LNA (Fig. 6.19), (b) the chip photo of the two-stage LNA used in the switch circuit (Fig. 6.21), and (c) the chip photo of the two-stage PA in the switch circuit (Fig. 6.22)

for ON state to 50Ω. The main loss contribution is from the reflection and impedance mismatch between OFF state LNA and ON state PA. Fig. 6.26(b) presents the input-output power characteristics of PA only TEG (blue line) and the TRX switch PA mode (red line) at 61.56GHz. The OP_{1dB} of the TRX switch PA mode is 2dBm whereas the PA only TEG has an OP_{1dB} value at 3.1dBm. The degradation in linearity is much lower than the introduced loss by the TRX switch combination which is around -2.3dB. Moreover, one can understand the isolation is not an issue at this OP_{1dB} since the degradation of linearity is lower than the combined switch loss.



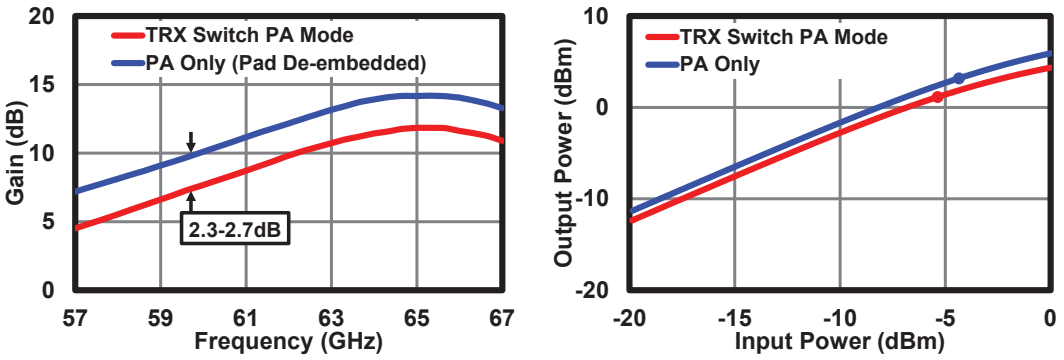
(a) (b)

Figure 6.24: Antenna port return loss comparisons of (a) LNA only as blue line (Fig. 6.23(b)) and LNA mode of antenna switch circuit (Fig. 6.23(a)) as red line (PA is OFF), and (b) PA only as blue line (Fig. 6.23(c)) and PA mode of antenna switch circuit as red line (LNA is OFF).



(a) (b)

Figure 6.25: (a) Measurement results of the gain of LNA only (blue line, Fig. 6.23(b)), LNA mode of antenna switch circuit (red line, Fig. 6.23(a), when PA is OFF). (b) Measured NF of LNA only in blue dots, LNA mode of the antenna switch circuit in red dots, the NF degradation because of the switch in black dots.



(a) (b)

Figure 6.26: (a) Measurement results of the gain of PA only (blue line, Fig. 6.23(c)), PA mode of antenna switch circuit (red line, Fig. 6.23(a), when LNA is OFF). (b) Input-output power relation when only PA in blue line and PA mode of switch circuit in red line.

6.5 Conclusions

Table 6.1 presents the comparison table of the proposed structure with other state-of-the-art switch circuits implemented on CMOS technology. Proposed antenna switch has a loss in RX mode as low as 1.1dB which is the lowest presented in the table. Hence, the NF degradation for RX is the lowest in the presented mode. Considering a complete transceiver system, the proposed architecture presents clear advantage. The minimum NF for this work is measured as 2.9dB. Another clear advantage of the proposed work is the silicon area consumption, since the design does not use any additional switch or transmission lines. As indicated, matching blocks are re-used for switching purposes in consideration with the switch as re-using the transistor of last-stage of PA and first-stage of LNA. For massive MIMO applications or phased array applications, this method helps to save considerable silicon area. The loss in TX mode is higher than expected. One reason is the modeling issue of transistors. By using more accurate models, much lower loss is possible without degradation of TX linearity or gain.

In here, an in-depth analysis is made for the loss of the conventional quarter-wavelength switch circuits. Than, a method to design LNA and PA as an antenna switch is presented. Both PA and LNA ON and OFF impedances are carefully designed to achieve this low loss antenna switching circuit. The presented switch method has several advantages in terms of area, lower loss, and lower NF degradation. Additionally, the TX side insertion loss can be improved by increasing OFF-state LNA input impedance. The simulated isolation value of -14dB shows that the switch can work properly at an output power of OP_{1dB}=2dBm, without any degradation on the linearity other than introduced loss of the switching architecture.

Table 6.1: Comparison with conventional switch architectures.

Ref.	Topology	Freq. [GHz]	RX Loss [dB]	TX Loss [dB]	Area [mm^2]	NF [dB]
This Work	LNA+PA TDD	57-66	1.1-1.7	2.3-2.7	N/A	2.9
[97]	Balun	55-66	1.2-2.3	1.6-2.9	0.024	14
[98]	Quarter-Wavelength	50-70	2	2	0.125	-
[99]	Quarter-Wavelength	53-60	1.5-1.6	1.5-1.6	0.275	-
[101]	Double Shunt & Matching	50-67	1.9	1.9	0.303	-
[102]	Matching Network	57-66	2	2	0.02	-

[97] T. Mitomo et al., ISSCC2012
[98] Y. A. Atesal et al., RFIC2009
[99] M. Uzunkol et al., JSSC2010
[101] C. W. Byeon et al., T-MTT2013
[102] J. He et al., T-MTT2012

Chapter 7

Conclusions and Future Directions

7.1 Conclusions

In this thesis, ultra-high data-rate wireless transceivers are aimed on CMOS manufacturing technology. Theoretical analysis starting from Shannon's theorem stated that for capabilities of a CMOS application in considerations with TX-to-RX SNDR and possible output power from a TX, W-Band frequencies with 16QAM data is the most efficient approach to implement ultra-wideband transceivers. Since the frequencies up to 110GHz is aimed for the design, conventional active and passive device characterization methods are revisited, and it is observed that the characterization and modeling approaches are to be improved. Hence, several new characterization methods are introduced to improve the accuracy of the circuit design. Differential virtual-thru de-embedding method is introduced based on mixed-mode S-parameters for differential device characterizations to be used in differential capacitive cross-coupled amplifiers. Results of the de-embedding and cross-line characterization are eployed in simulation environment in comparison with the measurement results of a differential amplifier at 60GHz shows good agreement up to 67GHz. Additionally, multi-port device characterization and modeling methods are developed using two-port network analyzer measurements in order to accurately extend the multi-port device accuracies. Results of the multi-port characterization methods are well matched with the measurement results.

As mentioned before amplifiers are one of the most important building blocks in a transceiver, and hence, several amplifiers are designed for different frequencies to reflect the requirements of the transceivers. For instance, a W-Band LNA is designed for the ultra-wideband ultra-high data-rate wireless transceiver at W-Band. Design method is based on positive feedback common-source topology, and is explained in detail. A more than 20dB gain wideband LNA with 5-stage positive feedback common-source topology

is measured with a power consumption of 65mW from 1V DC supply. The simulated OP1dB, saturated output power, and NF are 0.8dBm, 4.5dBm and 7.5dB, respectively.

A sub-terahertz amplifier is designed with positive feedback common-source topology. The transistor layout is optimized to increase the maximum unity gain frequency and the corner frequency to obtain more gain from one transistor, and de-embedded results support this claim in comparison with the conventional transistor layout results. The proposed amplifier achieves the highest gain frequency among all the bulk CMOS amplifiers. The upper band of unity gain for the amplifier is measured to be 301GHz, and the maximum unity gain for the transistor used in the amplifier is improved to 317GHz. The amplifier is composed of 16 identical stages consuming 35.4mW from 1.2V DC supply having each stage consuming 2.2mW. The maximum gain is measured at 298GHz with 21dB. Moreover, the minimum frequency with unity gain of the amplifier is measured to be 273GHz.

World fastest 120Gbps wireless TRX is presented on 65nm bulk CMOS. Frequency-interleave architecture for two data streams is employed while considering to lessen the burden of overall system. Effective solutions to avoid cross-modulation on the TRX are proposed. A low-loss PCB to waveguide transition is designed. The results show a maximum of -3.9dB IL for the two transitions. TX, RX, and TX-to-RX measurements are conducted with the customized module. The TX achieves the best EVM for 5GBaud 16QAM of -24.3dB at the output power of -7.4dBm for LB, and -21.1dB at the output power of -9.4dBm for HB. For 5GBaud 16QAM RF signals, the RX has the best EVM of -25.6dB at the input power of -26.3dBm for LB and -24.7dB at the input power of -24.3dBm for HB. TX-to-RX EVM measurements indicate that cross-modulation does not degrade the performance of wireless communications. Only 0.9dB on LB and 0.6dB on HB EVM degradation are observed due to cross-modulations between LB and HB. Comparisons with literature clears that this work achieves the world fastest 120Gbps wireless communication with 65nm standard bulk CMOS. Total core area of the circuitry occupy 3.2mm^2 whereas the whole IC occupies 6mm2 of silicon area. TX power consumption is 120mW, and RX power consumption is 160mW.

A transmitter-receiver architecture is proposed as an antenna switch. Proposed antenna switch has a loss in RX mode as low as 1.1dB which is the lowest presented in the table. Hence, the NF degradation for RX is the lowest in the presented mode. Considering a complete transceiver system, the proposed architecture presents clear advantage. The minimum NF for this work is measured as 2.9dB. Another clear advantage of the proposed work is the silicon area consumption, since the design does not use any additional switch or transmission lines. For massive MIMO applications or phased array applications, this method helps to save considerable silicon area. In here, an

in-depth analysis is made for the loss of the conventional quarter-wavelength switch circuits. Than, a method to design LNA and PA as an antenna switch is presented. The presented switch method has several advantages in terms of area, lower loss, and lower NF degradation. The simulated isolation value of -14dB shows that the switch can work properly at an output power of OP1dB=2dBm, without any degradation on the linearity other than introduced loss of the switching architecture.

7.2 Future Directions

In a not so distant future, wireless communication exceeding 1Tbps would be required for the society for short-, mid-, and long-range distances. Ultra-wideband transceivers are a must to achieve this ultra-high data-rate. Moreover, spectral efficiency has to be improved by means of MIMO, spatial duplexing and etc.

Ultra-wideband transceiver is a must to obtain such high data-rate wireless communications. Fig. 7.1 shows the frequency allocation after around 250GHz. Considering the atmospheric attenuation degradation around 330GHz. There is 80GHz available bandwidth in these frequency regions. Assuming a roll-off factor of 0.25 the available bandwidth for the data can be calculated to be around 64GHz. Hence; BPSK (required EVM=6.8dB), QPSK (required EVM=9.8dB), 16QAM (required EVM=16.5dB), 64QAM (required EVM=22.5dB), and 256QAM (required EVM=28.5dB) modulation schemes can achieve 64Gbps, 128Gbps, 256Gbps, 384Gbps, and 512Gbps, respectively. However, at terahertz wireless communication systems phase noise of the system especially for 64QAM and 256QAM is very stringent. For that reason, in order to achieve 1Tbps or more data-rate one has to implement a hybrid system of CMOS and III-V devices. To achieve 1Tbps wireless communication, an example scenario can be given as in Fig. 7.2. For instance, a single-transceiver capable of transmitting and receiving a total of 64GBaud data with 256QAM, 512Gbps data-rate is possible. Moreover, as in the figure, two transceivers can use the same frequency with different polarization of their own respective antennas; such as, right-hand elliptically polarized (RHEP) and left-hand elliptically polarized (LHEP). This two-transceivers can achieve in total 1.024Tbps data-rate.

The challenges for this kind of system would be the baseband design, the integration technologies between the transceivers and the antenna. For backhaul or fronthaul networking systems, a faster optical to wireless interface would greatly relax the implementation cost and time of the system. One o the issue is the required ultra-wideband characteristics of the system. Hence, frequency-interleaving can greatly relax the design of the overall system design; such as ADC/DAC sampling rate can be

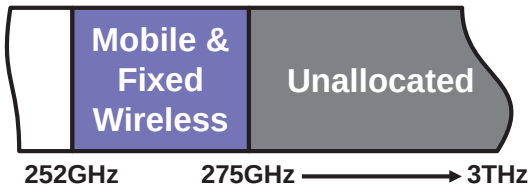


Figure 7.1: Frequency allocation after 252GHz.

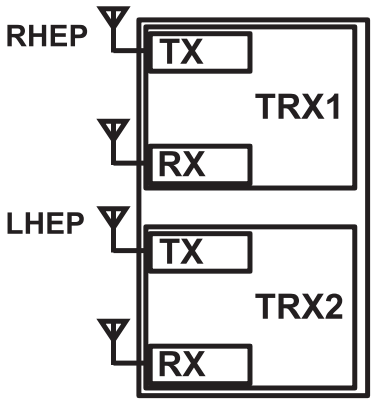


Figure 7.2: Example scenario to increase the data-rate; polarization MIMO.

reduced, similarly since the single stream data has less bandwidth digital baseband clock can be reduced as a result the overall power consumption can greatly decreased. Optimizing the number of frequency-interleaving architecture would also required for the specific system design.

Full CMOS solutions can solve the near-field communication (NFC) for hundreds of Gbps, and short distance applications such as in a room with a single transceiver even at these frequencies. As calculated above, 16QAM with 64GBaud data can achieve 256Gbps. For NFC ultra-high data-rate applications, such as, kiosk downloading, a CMOS sub-terahertz transceiver with on-chip antenna can be a feasible and cheap solution. For short range, full CMOS, solutions, phased-array with on-chip antenna can be a solution. Whereas for mid- and long-range applications, integration technologies have to be considered.

For example, for a communication distance of 100m, optical lens antennas can be a feasible solution with high antenna gain such as 55dBi for transmitter and receiver separately. Assuming an output power of -5dBm from the transmitter, module loss on transmitter and receiver side to be total of 10dB, theoretically 40dB EVM is possible (without considering the imperfections of the transceiver design). For longer range

applications, hybrid integration of CMOS and III-V devices is inevitable. Another challenge for terahertz systems is the integration between antenna and transceivers.

Bibliography

[1] B. Razavi, *RF Microelectronics*. Prentice Hall Communications Engineering and Emerging Technologies Series from Ted Rappaport, 2011.

[2] P. Smulders, "The road to 100 Gb/s wireless and beyond: basic issues and key directions," *IEEE Communications Magazine*, vol. 51, no. 12, pp. 86–91, Dec. 2013.

[3] K. Kazaura, K. Wakamori, M. Matsumoto, T. Higashino, K. Tsukamoto, and S. Komaki, "A Proposal for a Broadband Wireless Access Technology based on Radio-on-FSO Links," *IEEE Globecom Workshops*, pp. 1–6, Nov. 2008.

[4] [Online]. Available: http://www.tele.soumu.go.jp/e/adm/freq/search/share/plan.htm

[5] J. H. Sinsky and P. J. Winzer, "100-Gb/s optical communications," *IEEE Microwave Magazine*, vol. 10, no. 2, pp. 44–57, Apr. 2009.

[6] D. Zibar, A. Caballero, X. Yu, X. Pang, A. K. Dogadaev, and I. T. Monroy, "Hybrid optical fibre-wireless links at the 75-110 GHz band supporting 100 Gbps transmission capacities," *International Topical Meeting on Microwave Photonics/Asia-Pacific Microwave Photonics Conference*, pp. 445–449, Oct. 2011.

[7] K. Okada, N. Li, K. Matsushita, K. Bunsen, R. Murakami, A. Musa, T. Sato, H. Asada, N. Takayama, S. Ito, W. Chaivipas, R. Minami, T. Yamaguchi, Y. Takeuchi, H. Yamagishi, M. Noda, and A. Matsuzawa, "A 60-GHz 16QAM/8PSK/QPSK/BPSK Direct-Conversion Transceiver for IEEE802.15.3c," *IEEE Journal of Solid State Circuits*, vol. 46, no. 12, pp. 2988–3004, Dec. 2011.

[8] S. Emami, R. F. Wiser, E. Ali, M. G. Forbes, M. Q. Gordon, X. Guan, S. Lo, P. T. McElwee, J. Parker, J. R. Tani, J. M. Gilbert, and C. H. Doan, "A 60 GHz CMOS Phased-Array Transceiver Pair for Multi-Gb/s Wireless Communications," *IEEE International Solid-State Circuits Conference*, pp. 164–165, Feb. 2011.

[9] K. Okada, K. Kondou, M. Miyahara, M. Shinagawa, R. Minami, T. Yamaguchi, A. Musa, Y. Tsukui, Y. Asakura, S. Tamonoki, H. Yamagishi, Y. Hino, T. Sato, H. Sakaguchi, N. Shimasaki, T. Ito, Y. Takeuchi, N. Li, Q. Bu, R. Murakami, K. Bunsen, K. Matsushita, M. Noda, and A. Matsuzawa, "Full Four-Channel 6.3-Gb/s 60-GHz CMOS Transceiver With Low-Power Analog and Digital Baseband Circuitry," *IEEE Journal of Solid State Circuits*, vol. 48, no. 1, pp. 46–64, Jan. 2013.

[10] Z. Wang, P.-Y. Chiang, P. Nazari, C.-C. Wang, Z. Chen, and P. Heydari, "A CMOS 210 -GHz Fundamental Trasnceiver With OOK Modulation," *IEEE Journal of Solid State Circuits*, vol. 49, no. 3, pp. 564–580, Mar. 2013.

[11] K. Kang, F. Lin, D.-D. Pham, J. Brinkhoff, C.-H. Heng, Y. X. Guo, and X. Yuan, "A 60-GHz OOK Receiver With and On-Chip Antenna in 90 nm CMOS," *IEEE Journal of Solid State Circuits*, vol. 45, no. 9, pp. 1720–1730, Sep. 2010.

[12] M. Fujishima, M. Motoyoshi, K. Katayama, K. Takano, N. Ono, and R. Fujimoto, "98 mW 10 Gbps Wireless Transceiver Chipset With D-Band CMOS Circuits," *IEEE Journal of Solid State Circuits*, vol. 48, no. 10, pp. 2273–2283, Oct. 2013.

[13] O. Momeni and E. Afshari, "High Power Terahertz and Millimeter-Wave Oscillator Design: A Systematic Approach," *IEEE Journal of Solid State Circuits*, vol. 46, no. 3, pp. 583–597, Mar. 2011.

[14] R. Han and E. Afshari, "A CMOS High-Power Broadband 260-GHz Radiator Array for Spectroscopy," *IEEE Journal of Solid State Circuits*, vol. 48, no. 12, pp. 3090–3104, Dec. 2013.

[15] R. Han, Y. Zhang, Y. Kim, D. Y. Kim, H. Shichijo, E. Afshari, and K. K. O, "Active Terahertz Imaging Using Schottky Diodes in CMOS: Array and 860 -GHz Pixel," *IEEE Journal of Solid State Circuits*, vol. 48, no. 10, pp. 2296–2308, Oct. 2013.

[16] S. Pellerano, J. Javier Alvarado, and Y. Palaskas, "A mm-Wave Power-Harvesting RFID Tag in 90 nm CMOS," *IEEE Journal of Solid State Circuits*, vol. 45, no. 8, pp. 1627–1637, Aug. 2010.

[17] [Online]. Available: ITRS-Reports2013Edition

[18] Y. Nakasha, M. Sato, T. Tajima, Y. Kawano, T. Suzuki, T. Takahashi, K. Makiyama, T. Ohki, and N. Hara, "*W*-band Transmitter and Receiver for 10-Gb/s Impulse Radio With an Optical-Fiber Interface," *IEEE Transactions on Microwave Theory and Techniques*, vol. 57, no. 12, pp. 3171–3180, Dec. 2009.

[19] Y. Kawano, H. Matsumura, S. Shiba, M. Sato, T. Suzuki, Y. Nakasha, T. Takahashi, K. Makiyama, T. Iwai, and N. Hara, "A 20 Gbit/s, 280 GHz wireless transmission in InPHEMT based receiver module using flip-chip assembly," *European Microwave Conference*, pp. 562–565, Sep. 2015.

[20] S. Carpenter, D. Nopchinda, M. Abbasi, Z. S. He, M. Bao, T. Eriksson, and H. Zirath, "A *D*-Band 48-Gbit/s 64-QAM/QPSK Direct-Conversion I/Q Transceiver Chipset," *IEEE Transactions on Microwave Theory and Techniques*, vol. 64, no. 4, pp. 1285–1296, Apr. 2016.

[21] H. J. Song, J. Y. Kim, K. Ajito, N. Kukutsu, and M. Yaita, "50-Gb/s Direct Conversion QPSK Modulator and Demodulator MMICs for Terahertz Communications at 300 GHz," *IEEE Transactions on Microwave Theory and Techniques*, vol. 62, no. 3, pp. 600–609, Mar. 2014.

[22] F. Boes, T. Messinger, J. Antes, D. Meier, A. Tessmann, A. Inam, and I. Kallfass, "Ultra-broadband MMIC-based wireless link at 240 GHz enabled by 64GS/s DAC," *International Conference on Infrared, Millimeter, and Terahertz waves*, pp. 1–2, Sep. 2014.

[23] C. H. Doan, S. Emami, A. M. Niknejad, and R. W. Brodersen, "Millimeter-Wave CMOS Design," *IEEE Journal of Solid State Circuits*, vol. 40, no. 1, pp. 144–155, Jan. 2005.

[24] B. Heydari, M. Bohsali, E. Adabi, and A. M. Niknejad, "Millimeter-Wave Devices and Circuit Blocks up to 104 GHz in 90 nm CMOS," *IEEE Journal of Solid State Circuits*, vol. 42, no. 12, pp. 2893–2903, Dec. 2007.

[25] R. Fujimoto, K. Takano, M. Motoyoshi, U. Yodprasit, and M. Fujishima, "Device Modeling Techniques for High-Frequency Circuits Design Using Bond-Based Design at over 100 GHz," *IEICE Transactions on Electronics*, vol. E94-C, no. 4, pp. 589–597, Apr. 2011.

[26] O. Inac, M. Uzunkol, and G. M. Rebeiz, "45-nm CMOS SOI Technology Characterization for Millimeter-Wave Applications," *IEEE Transactions on Microwave Theory and Techniques*, vol. 62, no. 6, pp. 1301–1311, Jun. 2014.

[27] C. Liang and B. Razavi, "Systematic Transistor and Inductor Modeling for Millimeter-Wave Design," *IEEE Journal of Solid State Circuits*, vol. 44, no. 2, pp. 450–456, Feb. 2009.

[28] O. Momeni and E. Afshari, "A High Gain 107 GHz Amplifier in 130 nm CMOS," *IEEE Custom Integrated Circuits Conference*, pp. 1–4, Sep. 2011.

[29] N. Li, K. Matsushita, N. Takayama, S. Ito, K. Okada, and A. Matsuzawa, "Evaluation of Multi-Line De-Embedding Technique up to 110 GHz for Millimeter-Wave CMOS Circuit Design," *IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences*, vol. E93-A, no. 2, pp. 431–439, Feb. 2012.

[30] R. Minami, C. Han, K. Matsushita, K. Okada, and A. Matsuzawa, "Effect of Transmission Line Modeling Using Different De-Embedding Methods," *European Microwave Conference*, pp. 381–384, Oct. 2011.

[31] S. Kawai, K. K. Tokgoz, K. Okada, and A. Matsuzawa, "L-2L De-embedding Method with Double-T-type Pad Model for Millimeter-Wave Amplifier Design," *IEICE Analog-RF Study Group Workshop*, Mar. 2014.

[32] D. A. Frickey, "Conversions Between *S*, *Z*, *Y*, *h*, *ABCD*, and *T* Parameters which are Valid for Complex Source and Load Impedances," *IEEE Transactions on Microwave Theory and Techniques*, vol. 42, no. 2, pp. 205–211, Feb. 1994.

[33] W. R. Eisenstadt and Y. Eo, "S-parameter-Based IC Interconnect Transmission Line Characterization," *IEEE Transactions on Components, Hybrids, and Manufacturing Technology*, vol. 15, no. 4, pp. 483–490, Aug. 1992.

[34] V. Issakov, M. Wojnowski, A. Thiede, and L. Maurer, "Extension of Thru De-embedding Technique for Asymmetrical and Differential devices," *IET Circuits, Devices and Systems*, vol. 3, no. 2, pp. 91–98, Apr. 2009.

[35] A. Issaoun, Z. Xiong, J. Shi, J. Brinkhoff, and F. Lin, "On the Deembedding Issue of CMOS Multigigahertz Measurements," *IEEE Transactions on Microwave Theory and Techniques*, vol. 55, no. 9, pp. 1813–1823, Sep. 2007.

[36] Q. Liang, J. D. Cresler, G. Niu, Y. Lu, G. Freeman, D. Ahlgren, R. M. Malladi, K. Newton, and D. L. Harame, "A Simple 4-Port Parasitic De-embedding Methodology for High-Frequency Characterization of SiGe HBTs," *IEEE Radio Frequency Integrated Circuits Symposium*, pp. 357–360, Jun. 2003.

[37] K. Matsushita, N. Takayama, N. Li, S. Ito, K. Okada, and A. Matsuzawa, "CMOS Device Modeling for Millimeter-Wave Power Amplifiers," *IEEE Radio-Frequency Integration Technology*, pp. 68–71, Dec. 2009.

[38] K. Katayama, M. Motoyoshi, K. Takano, R. Fujimoto, and M. Fujishima, "Bias-Voltage-Dependent Subcircuit Model for Millimeter-Wave CMOS Circuit," *IEICE Transactions on Electronics*, vol. E95-C, no. 6, pp. 1077–1085, Jun. 2012.

[39] S. Sato, "Towards Achieving Communication Speed of 40Gb/s - Research on 60-GHz CMOS Transmitter (in Japanese)," Master's thesis, Tokyo Inst. of Tech., 2013.

[40] Y. Manzawa, M. Sasaki, and M. Fujishima, "High-Attenuation Power Line for Wideband Decoupling," *IEICE Transactions on Electronics*, vol. E92-C, no. 6, pp. 792–797, Jun. 2009.

[41] Y. Natsukari and M. Fujishima, "36mW 63GHz CMOS Differential Low-Noise Amplifier with 14GHz Bandwidth," *Symposium on VLSI Circuits*, pp. 252–253, Jun. 2009.

[42] S. Maki, S. Kawai, K. Okada, and A. Matsuzawa, "A Millimeter-Wave Shunt Measurement Technique for Low-Impedance Elements," *IEICE Society Conference*, no. C-12-17 (in Japanese), Sep. 2013.

[43] S. Amakawa, H. Ito, N. Ishihara, and K. Masu, "A Simple De-Embedding Method for Characterization of On-Chip Four-Port Networks," *Advanced Metallization Conference*, pp. 105–106, Sep. 2008.

[44] D. E. Bockelman and W. R. Eisenstadt, "Combined Differential and Common-Mode Scattering Parameters: Theory and Simulation," *IEEE Transactions on Microwave Theory and Techniques*, vol. 43, no. 7, pp. 1530–1539, Jul. 1995.

[45] Q. H. Bu, N. Li, K. Okada, and A. Matsuzawa, "Evaluation of l-2l de-embedding method considering misalignment of contact position for millimeter-wave cmos circuit design," *IEICE Transactions on Electronics*, vol. E95-C, no. 5, pp. 942–948, May 2012.

[46] V. Issakov, M. Wojnowski, A. Thiede, and R. Weigel, "Considerations on The De-Embedding of Differential Devices Using Two-Port Techniques," *European Microwave Conference*, pp. 695–698, Oct. 2009.

[47] L. F. Tiemeijer, R. M. T. Pijper, and E. van der Heijden, "Two Multiport De-Embedding Methods for Accurate On-Wafer Characterization of 60-GHz Differential Amplifiers," *IEEE Transactions on Microwave Theory and Techniques*, vol. 59, no. 3, pp. 763–771, Mar. 2011.

[48] Y. Zhang, K. Silvonen, and N. H. Zhu, "Measurement of a Reciprocal Four-Port Transmission Line Structure Using the 16-Term Error Model," *Microwave and Optical Technology Letters*, vol. 49, no. 7, pp. 1511–1515, Jul. 2007.

[49] K. M. Ho, K. Vaz, and M. Caggiano, "Scattering Parameter Characterization of Differential Four-Port Networks Using a Two-Port Vector Network Analyzer," *Electronic Components and Technology Conference*, pp. 1846–1853, Jun. 2005.

[50] C.-J. Chen and T.-H. Chu, "Virtual Auxiliary Termination for Multiport Scattering Matrix Measurement Using Two-Port Network Analyzer," *IEEE Transactions on Microwave Theory and Techniques*, vol. 55, no. 8, pp. 1801–1810, Aug. 2007.

[51] ——, "Measurement of Noncoaxial Multiport Devices Up to Intrinsic Ports," *IEEE Transactions on Microwave Theory and Techniques*, vol. 57, no. 5, pp. 1230–1236, May 2009.

[52] V. Issakov, M. Wojnowski, and G. Sommer, "Technique for accurate characterization of baluns using one-port S-parameters measurements," *European Microwave Conference*, pp. 305–308, Oct. 2011.

[53] J. C. Tippet and R. A. Speciale, "A Rigorous Technique for Measuring the Scattering Matrix of a Multiport Device with a 2-Port Network Analyzer," *IEEE Transactions on Microwave Theory and Techniques*, vol. 30, no. 5, pp. 661–666, May 1982.

[54] I. Rolfes and B. Schiek, "Multiport method for the measurement of the scattering parameters of N-ports," *IEEE Transactions on Microwave Theory and Techniques*, vol. 53, no. 6, pp. 1990–1996, Jun. 2005.

[55] K. K. Tokgoz, L. Kimsrun, S. Kawai, K. Okada, and A. Matsuzawa, "Crossing Transmission Line Modeling Using Two-Port Measurements," *International Conference on Solid-State Devices and Materials*, pp. 900–901, Sep. 2013.

[56] Agilent Technologies, Network Analyzers' Data Sheets, "http://www.home.agilent.com/agilent/."

[57] S. Papatheodorou, J. R. Mautz, and R. F. Harrington, "Full-wave analysis of a strip crossover," *IEEE Transactions on Microwave Theory and Techniques*, vol. 38, no. 10, pp. 1439–1448, Oct. 1990.

[58] N. Fajri, S. Kawai, K. Okada, and A. Matsuzawa, "A research on the coupling of transmission lines in 60 GHz circuit design," *IEICE General Conf.*, vol. C-12-21, Mar. 2013.

[59] K.-J. Tsai, J.-L. Kuo, and H. Wang, "A W-band Power Amplifier in 65-nm CMOS with 27 GHz Bandwidth and 14.8 dBm Saturated Output Power," *IEEE Radio Frequency Integrated Circuits Symposium*, pp. 69–72, Jun. 2012.

[60] B. Wicks, E. Skafidas, and R. Evans, "A 75-95 GHz Wideband CMOS Power Amplifier," *European Microwave Conference*, pp. 230–233, Oct. 2008.

[61] Y.-S. Jiang, Z.-M. Tsai, J.-H. Tsai, H.-T. Chen, and H. Wang, "A 86 to 108 GHz Amplifier in 90 nm CMOS," *IEEE Microwave and Wireless Components Letters*, vol. 18, no. 2, pp. 124–126, Feb. 2008.

[62] D.-R. Lu, Y.-C. Hsu, J.-C. Kao, J.-J. Kuo, D.-C. Niu, and K.-Y. Lin, "A 75.5-to-120.5-GHz, High-gain CMOS Low-Noise Amplifier," *IEEE MTT-S International Microwave Symposium*, pp. 1–3, Jun. 2012.

[63] Y.-S. Jiang, J.-H. Tsai, and H. Wang, "A W-Band Medium Power Amplifier in 90 nm CMOS," *IEEE Microwave and Wireless Components Letters*, vol. 18, no. 12, pp. 818–820, Dec. 2008.

[64] G. Liu and H. Schumacher, "Broadband Millimeter-Wave LNAs (47-77 GHz and 70-140 GHz) Using a T-Type Matching Topology," *IEEE Journal of Solid State Circuits*, vol. 48, no. 9, pp. 2022–2029, Sep. 2013.

[65] Y.-H. Hsiao, Z.-M. Tsai, H.-C. Liao, J.-C. Kao, and H. Wang, "Millimeter-Wave CMOS Power Amplifiers With High Output Power and Wideband Performances," *IEEE Transactions on Microwave Theory and Techniques*, vol. 61, no. 12, pp. 4520–4533, Dec. 2013.

[66] K.-L. Wu, K.-T. Lai, R. Hu, C. F. Jou, D.-C. Niu, and Y.-S. Shiao, "77-110 GHz 65-nm CMOS Power Amplifier Design," *IEEE Transactions on Terahertz Science and Technology*, vol. 4, no. 3, pp. 391–399, May 2014.

[67] O. Momeni, "A 260 GHz Amplifier with 9.2 dB Gain and -3.9 dBm Saturated Power in 65nm CMOS," *IEEE International Solid-State Circuits Conference*, pp. 140–141, Feb. 2013.

[68] K. Katayama, K. Takano, S. Amakawa, S. Hara, A. Kasamatsu, K. Mizuno, K. Takahashi, T. Yoshida, and M. Fujishima, "A 300GHz 40nm CMOS transmitter

with 32-QAM 17.5Gb/s/ch capability over 6 channels," *IEEE International Solid-State Circuits Conference*, pp. 342–343, Jan. 2016.

[69] K. Takano, S. Amakawa, K. Katayama, S. Hara, R. Dong, A. Kasamatsu, I. Hosako, K. Mizuno, K. Takahashi, T. Yoshida, and M. Fujishima, "A 105Gb/s 300GHz CMOS transmitter," *IEEE International Solid-State Circuits Conference*, pp. 308–309, Feb. 2017.

[70] S. Hara, K. Katayama, K. Takano, R. Dong, I. Watanabe, N. Sekine, A. Kasamatsu, T. Yoshida, S. Amakawa, and M. Fujishima, "A 32Gbit/s 16QAM CMOS receiver in 300GHz band," *IEEE MTT-S International Microwave Symposium*, pp. 1703–1706, Jun. 2017.

[71] Y. Yagishita, Y. Kawano, H. Matsumura, I. Soga, T. Suzuki, and T. Iwai, "265-GHz, 10-dB gain amplifier in 65-nm CMOS using on-wafer TRL calibration," *Asia-Pacific Microwave Conference*, vol. 2, pp. 1–3, Dec. 2015.

[72] H. Bameri and O. Momeni, "A High-Gain mm-Wave Amplifier Design: An Analytical Approach to Power Gain Boosting," *IEEE Journal of Solid-State Circuits*, vol. 52, no. 2, pp. 357–370, Feb. 2017.

[73] D. W. Park, D. R. Utomo, J. P. Hong, and S. G. Lee, "A 230-260GHz wideband amplifier in 65nm CMOS based on dual-peak Gmax-core," *Symposium on VLSI Circuits*, pp. C300–C301, Jun. 2017.

[74] D. Parveg, D. Karaca, M. Varonen, A. Vahdati, and K. A. I. Halonen, "Demonstration of a 0.325-THz CMOS amplifier," *Global Symposium on Millimeter Waves ESA Workshop on Millimetre-Wave Technology and Applications*, pp. 1–3, Jun. 2016.

[75] Fujitsu Semiconductor Europe, "Digital to Analog Converter-Factsheet LEIA 55-65 GSa/s 8-bit DAC," Mar. 2012. [Online]. Available: www.fujitsu.com/downloads/MICRO/fme/documentation/c60.pdf

[76] H. Huang, J. Heilmeyer, M. GrÃűzing, M. Berroth, J. Leibrich, and W. Rosenkranz, "An 8-bit 100-GS/s Distributed DAC in 28-nm CMOS for Optical Communications," *IEEE Transactions on Microwave Theory and Techniques*, vol. 63, no. 4, pp. 1211–1218, Apr. 2015.

[77] M. Shinagawa, Y. Akazawa, and T. Wakimoto, "Jitter analysis of high-speed sampling systems," *IEEE Journal of Solid-State Circuits*, vol. 25, no. 1, pp. 220–224, Feb. 1990.

[78] Y. M. Greshishchev, J. Aguirre, M. Besson, R. Gibbins, C. Falt, P. Flemke, N. Ben-Hamida, D. Pollex, P. Schvan, and S. C. Wang, "A 40GS/s 6b ADC in 65nm CMOS," *IEEE International Solid-State Circuits Conference*, pp. 390–391, Feb. 2010.

[79] L. Kull, J. Pliva, T. Toifl, M. Schmatz, P. A. Francese, C. Menolfi, M. BrÃd'ndli, M. Kossel, T. Morf, T. M. Andersen, and Y. Leblebici, "Implementation of Low-Power 6-b 30-90 GS/s Time-Interleaved ADCs With Optimized Input Bandwidth in 32 nm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 51, no. 3, pp. 636–648, Mar. 2016.

[80] K. Okada, R. Minami, Y. Tsukui, S. Kawai, Y. Seo, S. Sato, S. Kondo, T. Ueno, Y. Takeuchi, T. Yamaguchi, A. Musa, R. Wu, M. Miyahara, and A. Matsuzawa, "A 64-QAM 60GHz CMOS transceiver with 4-channel bonding," *IEEE International Solid-State Circuits Conference*, pp. 346–347, Feb. 2014.

[81] O. Momeni and E. Afshari, "A high gain 107 GHz amplifier in 130 nm CMOS," *IEEE Custom Integrated Circuits Conference*, pp. 1–4, Sep. 2011.

[82] O. Momeni, "A 260GHz amplifier with 9.2dB gain and -3.9dBm saturated power in 65nm CMOS," *IEEE International Solid-State Circuits Conference*, pp. 140–141, Feb. 2013.

[83] K. K. Tokgoz, K. Lim, K. Okada, and A. Matsuzawa, "Shunt characterization technique of decoupling transmission line for millimeter-wave CMOS amplifier design," *Asia-Pacific Microwave Conference*, pp. 274–276, Nov. 2014.

[84] E. Topak, J. Hasch, and T. Zwick, "Compact Topside Millimeter-Wave Waveguide-to-Microstrip Transitions," *IEEE Microwave and Wireless Components Letters*, vol. 23, no. 12, pp. 641–643, Dec. 2013.

[85] S. Jameson and E. Socher, "A Wide-Band CMOS to Waveguide Transition at mm-Wave Frequencies With Wire-Bonds," *IEEE Transactions on Microwave Theory and Techniques*, vol. 63, no. 9, pp. 2741–2750, Sep. 2015.

[86] Y. Kawano, H. Matsumura, S. Shiba, M. Sato, T. Suzuki, Y. Nakasha, T. Takahashi, K. Makiyama, and N. Hara, "Flip chip assembly for sub-millimeter wave amplifier MMIC on polyimide substrate," *IEEE MTT-S International Microwave Symposium*, pp. 1–4, Jun. 2014.

[87] N. Dolatsha, B. Grave, M. Sawaby, C. Chen, A. Babveyh, S. Kananian, A. Bisognin, C. Luxey, F. Gianesello, J. Costa, C. Fernandes, and A. Arbabian, "A compact 130GHz fully packaged point-to-point wireless system with 3D-printed 26dBi lens antenna achieving 12.5Gb/s at 1.55pJ/b/m," *IEEE International Solid-State Circuits Conference*, pp. 306–307, Feb. 2017.

[88] S. Kang, S. V. Thyagarajan, and A. M. Niknejad, "A 240 GHz Fully Integrated Wideband QPSK Transmitter in 65 nm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 50, no. 10, pp. 2256–2267, Oct. 2015.

[89] S. V. Thyagarajan, S. Kang, and A. M. Niknejad, "A 240 ghz fully integrated wideband qpsk receiver in 65 nm cmos," *IEEE Journal of Solid-State Circuits*, vol. 50, no. 10, pp. 2268–2280, Oct. 2015.

[90] Y. Yang, S. Zihir, H. Lin, O. Inac, W. Shin, and G. M. Rebeiz, "A 155 GHz 20 Gbit/s QPSK transceiver in 45nm CMOS," *IEEE Radio Frequency Integrated Circuits Symposium*, pp. 365–368, Jun. 2014.

[91] J. Pang, S. Maki, S. Kawai, N. Nagashima, Y. Seo, M. Dome, H. Kato, M. Katsuragi, K. Kimura, S. Kondo, Y. Terashima, H. Liu, T. Siriburanon, A. T. Narayanan, N. Fajri, T. Kaneko, T. Yoshioka, B. Liu, Y. Wang, R. Wu, N. Li, K. K. Tokgoz, M. Miyahara, K. Okada, and A. Matsuzawa, "A 128-QAM 60GHz CMOS transceiver for IEEE802.11ay with calibration of LO feedthrough and I/Q imbalance," *IEEE International Solid-State Circuits Conference*, pp. 424–425, Feb. 2017.

[92] K. K. Tokgoz, S. Maki, S. Kawai, N. Nagashima, J. Emmei, M. Dome, H. Kato, J. Pang, Y. Kawano, T. Suzuki, T. Iwai, Y. Seo, K. Lim, S. Sato, L. Ning, K. Nakata, K. Okada, and A. Matsuzawa, "A 56Gb/s W-band CMOS wireless transceiver," *IEEE International Solid-State Circuits Conference*, pp. 242–243, Jan. 2016.

[93] ——, "A 56Gb/s W-band CMOS wireless transceiver," *IEEE International Solid-State Circuits Conference*, pp. 242–243, Jan. 2016.

[94] R. Wu, R. Minami, Y. Tsukui, S. Kawai, Y. Seo, S. Sato, K. Kimura, S. Kondo, T. Ueno, N. Fajri, S. Maki, N. Nagashima, Y. Takeuchi, T. Yamaguchi, A. Musa, K. K. Tokgoz, T. Siriburanon, B. Liu, Y. Wang, J. Pang, N. Li, M. Miyahara, K. Okada, and A. Matsuzawa, "64-QAM 60-GHz CMOS Transceivers for IEEE 802.11ad/ay," *IEEE Journal of Solid-State Circuits*, vol. 52, no. 11, pp. 2871–2891, Nov. 2017.

[95] K. Okada, K. Kondou, M. Miyahara, M. Shinagawa, H. Asada, R. Minami, T. Yamaguchi, A. Musa, Y. Tsukui, Y. Asakura, S. Tamonoki, H. Yamagishi, Y. Hino, T. Sato, H. Sakaguchi, N. Shimasaki, T. Ito, Y. Takeuchi, N. Li, Q. Bu, R. Murakami, K. Bunsen, K. Matsushita, M. Noda, and A. Matsuzawa, "Full Four-Channel 6.3-Gb/s 60-GHz CMOS Transceiver With Low-Power Analog and Digital Baseband Circuitry," *IEEE Journal of Solid-State Circuits*, vol. 48, no. 1, pp. 46–65, Jan. 2013.

[96] K. Okada, N. Li, K. Matsushita, K. Bunsen, R. Murakami, A. Musa, T. Sato, H. Asada, N. Takayama, S. Ito, W. Chaivipas, R. Minami, T. Yamaguchi, Y. Takeuchi, H. Yamagishi, M. Noda, and A. Matsuzawa, "A 60-GHz 16QAM/8PSK/QPSK/BPSK Direct-Conversion Transceiver for IEEE802.15.3c," *IEEE Journal of Solid-State Circuits*, vol. 46, no. 12, pp. 2988–3004, Dec. 2011.

[97] T. Mitomo, Y. Tsutsumi, H. Hoshino, M. Hosoya, T. Wang, Y. Tsubouchi, R. Tachibana, A. Sai, Y. Kobayashi, D. Kurose, T. Ito, K. Ban, T. Tandai, and T. Tomizawa, "A 2gb/s-throughput CMOS transceiver chipset with in-package antenna for 60GHz short-range wireless communication," *IEEE International Solid-State Circuits Conference*, pp. 266–268, Feb. 2012.

[98] Y. A. Atesal, B. Cetinoneri, and G. M. Rebeiz, "Low-loss 0.13μm CMOS 50-70 GHz SPDT and SP4T switches," *IEEE Radio Frequency Integrated Circuits Symposium*, pp. 43–46, Jun. 2009.

[99] M. Uzunkol and G. Rebeiz, "A Low-Loss 50-70 GHz SPDT Switch in 90 nm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 45, no. 10, pp. 2003–2007, Oct. 2010.

[100] L. Kuang, B. Chi, H. Jia, Z. Ye, W. Jia, and Z. Wang, "Co-Design of 60-GHz Wideband Front-End IC With On-Chip T/R Switch Based on Passive Macro-Modeling," *IEEE Transactions on Microwave Theory and Techniques*, vol. 62, no. 11, pp. 2743–2754, Nov. 2014.

[101] C. W. Byeon and C. S. Park, "Design and Analysis of the Millimeter-Wave SPDT Switch for TDD Applications," *IEEE Transactions on Microwave Theory and Techniques*, vol. 61, no. 8, pp. 2858–2864, Aug. 2013.

[102] J. He, Y. Z. Xiong, and Y. P. Zhang, "Analysis and Design of 60-GHz SPDT Switch in 130-nm CMOS," *IEEE Transactions on Microwave Theory and Techniques*, vol. 60, no. 10, pp. 3113–3119, Oct. 2012.

[103] K. K. Tokgoz, S. Kawai, K. Okada, and A. Matsuzawa, "A low-loss 60GHz integrated antenna switch in 65nm CMOS," *IEEE International Symposium on Radio-Frequency Integration Technology*, pp. 50–52, Aug. 2017.

[104] M. Uzunkol and G. M. Rebeiz, "140-220 GHz SPST and SPDT Switches in 45 nm CMOS SOI," *IEEE Microwave and Wireless Components Letters*, vol. 22, no. 8, pp. 412–414, Aug. 2012.

[105] A. C. Ulusoy, P. Song, R. L. Schmid, W. T. Khan, M. Kaynak, B. Tillack, J. Papapolymerou, and J. D. Cressler, "A Low-Loss and High Isolation D-Band SPDT Switch Utilizing Deep-Saturated SiGe HBTs," *IEEE Microwave and Wireless Components Letters*, vol. 24, no. 6, pp. 400–402, Jun. 2014.

[106] F. Meng, K. Ma, and K. S. Yeo, "A 130-to-180GHz 0.0035mm^2 SPDT switch with 3.3dB loss and 23.7dB isolation in 65nm bulk CMOS," *IEEE International Solid-State Circuits Conference*, pp. 1–3, Feb. 2015.

[107] R. Shu, J. Li, A. Tang, B. J. Drouin, and Q. J. Gu, "Coupling-Inductor-Based hybrid mm-Wave CMOS SPST Switch," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 64, no. 4, pp. 367–371, Apr. 2017.

Appendix A

Publication List

A.1 Journal Papers

- **Korkut Kaan Tokgoz**, Seitaro Kawai, Kenichi Okada, and Akira Matsuzawa, "Design of Low-Loss 60GHz Integrated Antenna Switch in 65nm CMOS," *IEICE Electronics Express* (Accepted, to be published).

- **Korkut Kaan Tokgoz**, Kimsrun Lim, Seitaro Kawai, Nurul Fajri, Kenichi Okada, and Akira Matsuzawa, "Characterization of Crossing Transmission Line Using Two-Port Measurements for Millimeter-Wave CMOS Circuit Design," *IEICE Transactions on Electronics*, Vol. E98-C, No. 1, pp. 35-44, Jan. 2015.

A.2 International Conferences and Workshops (Peer-Reviewed)

- **Korkut Kaan Tokgoz**, Shotaro Maki, Jian Pang, Noriaki Nagashima, Ibrahim Abdo, Seitaro Kawai, Takuya Fujimura, Yoichi Kawano, Toshihide Suzuki, Taisuke Iwai, Kenichi Okada, and Akira Matsuzawa, "A 120Gb/s 16QAM CMOS Millimeter-Wave Wireless Transceiver" *IEEE International Solid-State Circuits Conference*, pp. 168-169, San Francisco, CA, Feb. 2018.

- **Korkut Kaan Tokgoz**, Seitaro Kawai, Kenichi Okada, and Akira Matsuzawa, "A Low-Loss 60GHz Integrated Antenna Switch in 65nm CMOS," *IEEE International Symposium on Radio-Frequency Integration Technology*, pp. 50-52, Seoul, Korea, Aug. 2017.

- **Korkut Kaan Tokgoz**, Jian Pang, Shotaro Maki, Kenichi Okada, and Akira

Matsuzawa, *IEEE International Solid-State Circuits Conference*, Student Research Preview (SRP), San Francisco, CA, Feb. 2017 (Student Travel Grant Awardee).

- **Korkut Kaan Tokgoz**, Shotaro Maki, Seitaro Kawai, Noriaki Nagashima, Yoichi Kawano, Toshihide Suzuki, Taisuke Iwai, Kenichi Okada, and Akira Matsuzawa, "W-Band Ultra-High Data-Rate 65nm CMOS Wireless Transceiver" *IEEE/ACM Asia-South Pacific Design Automation Conference University LSI Design Contest*, pp. 5-6, Chiba, Japan, Jan. 2017 (Best Design Award).

- **Korkut Kaan Tokgoz**, Shotaro Maki, Seitaro Kawai, Noriaki Nagashima, Jun Emmei, Masato Dome, Hisashi Kato, Jian Pang, Yoichi Kawano, Toshihide Suzuki, Taisuke Iwai, Yuuki Seo, Kimsrun Lim, Shinji Sato, Ning Li, Kengo Nakata, Kenichi Okada, and Akira Matsuzawa, "A 56Gb/s W-Band CMOS Wireless Transceiver" *IEEE International Solid-State Circuits Conference*, pp. 242-243, San Francisco, CA, Feb. 2016.

- **Korkut Kaan Tokgoz**, Shotaro Maki, Kenichi Okada, and Akira Matsuzawa, "Characterization of Cross-Line up to 110GHz Using Two-Port Measurement," *IEEE International Symposium on Radio-Frequency Integration Technology*, pp. 97-99, Sendai, Japan, Aug. 2015.

- **Korkut Kaan Tokgoz**, Kimsrun Lim, Yuuki Seo, Seitaro Kawai, Kenichi Okada, and Akira Matsuzawa, "Cross-Line Characterization for Capacitive Cross Coupling in Differential Millimeter-Wave CMOS Amplifiers," *IEEE Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems*, San Diego, CA, Jan. 2015.

- **Korkut Kaan Tokgoz**, Kimsrun Lim, Kenichi Okada, and Akira Matsuzawa, "Shunt Characterization Technique of Decoupling Transmission Line for Millimeter-Wave CMOS Amplifier Design," *IEEE Asia-Pacific Microwave Conference*, Sendai, Japan, Nov. 2014.

- **Korkut Kaan Tokgoz**, Nurul Fajri, Yuuki Seo, Seitaro Kawai, Kenichi Okada, and Akira Matsuzawa, "A Characterization Method of On-Chip Tee-Junction for Millimeter-Wave CMOS Circuit Design," *International Conference on Solid State Devices and Materials*, Tsukuba, Ibaraki, Japan, Sep. 2014.

- **Korkut Kaan Tokgoz**, Kimsrun Lim, Seitaro Kawai, Kenichi Okada, and Akira Matsuzawa, "Crossing Transmission Line Modeling Using Two-Port Measurements," *International Conference on Solid State Devices and Materials*, Fukuoka, Japan, Sep. 2013.

- **Korkut Kaan Tokgoz**, Simsek Demir, and Tayfun Akin, "Surface Micromachining Implementation of S-Band 4-bit Phase Shifter," *MEMSWAVE 2012 - Thirteenth International Symposium on RF-MEMS and RF-Microsystems*, Antalya, Turkey, Jul. 2012.

- **Korkut Kaan Tokgoz**, Cagri Cetintepe, and Simsek Demir, "1-6GHz UWB Phase Shifter Design and Implementation with Surface Micromachining," *Sixth European Conference on Antennas and Propagation*, pp. 2933-2937, Prague, Czech Republic, Mar. 2012.

A.3 International Conferences and Workshops (Not Reviewed)

- **Korkut Kaan Tokgoz**, Shotaro Maki, Seitaro Kawai, Noriaki Nagashima, Yoichi Kawano, Toshihide Suzuki, Taisuke Iwai, Kenichi Okada, and Akira Matsuzawa, "A 56Gb/s W-Band CMOS Wireless Transceiver" *The Eight Multidisciplinary International Student Workshop*, Poster presentation # 9, Tokyo Institute of Technology, Tokyo, Japan, Aug. 2016.

- **Korkut Kaan Tokgoz**, Shotaro Maki, Seitaro Kawai, Noriaki Nagashima, Yoichi Kawano, Toshihide Suzuki, Taisuke Iwai, Kenichi Okada, and Akira Matsuzawa, "A 56Gb/s W-Band CMOS Wireless Transceiver" *Fourth UK-Japan Engineering Education League Joint Workshop*, Tokyo Institute of Technology, Tokyo, Japan, Aug. 2016.

- **Korkut Kaan Tokgoz**, Kimsrun Lim, Kenichi Okada, and Akira Matsuzawa, "On The Variations of Shunt Characterization Technique of Decoupling Transmission Line for Millimeter-Wave CMOS Applications," *Vietnam-Japan Microwave Conference*, Hanoi, Vietnam, Nov. 2014.

- **Korkut Kaan Tokgoz**, Nurul Fajri, YuukiSeo, Seitaro Kawai, Kenichi Okada, and Akira Matsuzawa, "Tee-Junction Characterization on CMOS for Millimeter-Wave Applications," *The Sixth Multidisciplinary International Student Workshop*, A7-4, Tokyo Institute of Technology, Tokyo, Japan, Aug. 2014.

- **Korkut Kaan Tokgoz**, Kimsrun Lim, Kenichi Okada, and Akira Matsuzawa, "On The Variations of Shunt Characterization Technique of Decoupling Transmission Line for Millimeter-Wave CMOS Applications," *Thailand-Japan Microwave*

Conference, Bangkok, Thailand, Nov. 2014 (Young Researcher Encouragement Award).

- **Korkut Kaan Tokgoz**, Kimsrun Lim, Seitaro Kawai, Kenichi Okada, and Akira Matsuzawa, "Modeling of Crossing Transmission Line for Millimeter-Wave CMOS Applications," *Eight AOTULE Meetings and Conference*, Bangkok, Thailand, Oct. 2013.

- **Korkut Kaan Tokgoz**, Kimsrun Lim, Seitaro Kawai, Kenichi Okada, and Akira Matsuzawa, "Modeling of Crossing Transmission Line for Millimeter-Wave CMOS Applications," *The Fifth Multidisciplinary International Student Workshop*, B1-5, Tokyo Institute of Technology, Tokyo, Japan, Aug. 2013 (One of the top 20 presenter to attend Eight AOTULE Meetings and Conference).

A.4 Domestic Conferences and Workshops

- **Korkut Kaan Tokgoz**, Shotaro Maki, Jian Pang, Noriaki Nagashima, Ibrahim Abdo, Seitaro Kawai, Takuya Fujimura, Yoichi Kawano, Toshihide Suzuki, Taisuke Iwai, Kenichi Okada, and Akira Matsuzawa, "A 120Gb/s 16QAM CMOS Millimeter-Wave Wireless Transceiver" *IEEE SSCS Japan Chapter ISSCC Reporting Meeting*, University of Tokyo, Feb. 2018.

- **Korkut Kaan Tokgoz**, Shotaro Maki, Seitaro Kawai, Noriaki Nagashima, Yoichi Kawano, Toshihide Suzuki, Taisuke Iwai, Kenichi Okada and Akira Matsuzawa, "W-Band Ultra-High Data-Rate 65nm CMOS Wireless Transceiver," *IEEE Student Branch Leadership Training Workshop*, Chiba, Japan, Mar. 2017.

- **Korkut Kaan Tokgoz**, Shotaro Maki, Seitaro Kawai, Noriaki Nagashima, Yoichi Kawano, Toshihide Suzuki, Taisuke Iwai, Kenichi Okada and Akira Matsuzawa, "Issue of Cross-Modulation on Wideband Frequency-Interleave Transceivers," *IEICE Society Conference*, C-12-3, Hokkaido University, Sapporo, Japan, Sep. 2016 (IEICE Student Encouragement Prize).

- **Korkut Kaan Tokgoz**, Shotaro Maki, Seitaro Kawai, Noriaki Nagashima, Yoichi Kawano, Toshihide Suzuki, Taisuke Iwai, Kenichi Okada and Akira Matsuzawa, "A 56Gb/s W-Band CMOS Wireless Transceiver," *VDEC Design Award*, University of Tokyo, Tokyo, Japan, Aug. 2016 (Encouragement Award).

- **Korkut Kaan Tokgoz**, Shotaro Maki, Kenichi Okada, and Akira Matsuzawa, "Accurate Characterization Method for Cross-Line on CMOS Based on Two-Port

Measurements," *IEICE General Conference*, C-12, Kyushu University, Fukuoka, Japan, Mar. 2016.

- **Korkut Kaan Tokgoz**, Kenichi Okada, and Akira Matsuzawa, "Millimeter-Wave CMOS Transceiver Toward 1Tbps," *STARC Forum*, Shin-Yokohama, Japan, Nov. 2015.

- **Korkut Kaan Tokgoz**, Kimsrun Lim, Kenichi Okada, and Akira Matsuzawa, "On The Variations of Shunt Characterization Technique of Decoupling Transmission Line for Millimeter-Wave CMOS Applications," *IEICE General Conference*, Ritsumeikan University, Shiga, Japan, C-2, Mar. 2015 (Nominated for IEICE Student Encouragement Prize).

- **Korkut Kaan Tokgoz**, Nurul Fajri, Yuuki Seo, Seitaro Kawai, Kenichi Okada, and Akira Matsuzawa, "A Characterization Method of On-Chip Tee-Junction for Millimeter-Wave CMOS Circuit Design," *IEICE Society Conference*, C-12-30, Tokushima University, Tokushima, Japan, Sep. 2014.

- **Korkut Kaan Tokgoz**, Kimsrun Lim, Seitaro Kawai, Kenichi Okada, and Akira Matsuzawa, "Modeling and Characterization Approaches for Crossing Transmission Line on CMOS," *IEICE Analog-RF Study Group Workshop*, vol. RF2013-3, p. 1, Chuo University, Tokyo, Japan, Mar. 2014.

- **Korkut Kaan Tokgoz**, Kimsrun Lim, Seitaro Kawai, Kenichi Okada, and Akira Matsuzawa, "Crossing Transmission Line Modeling Using Two-Port Measurements," *IEICE Society Conference*, C-12-21, Fukuoka Institute of Technology, Fukuoka, Japan, Sep. 2013.

A.5 Co-Author

A.5.1 Journals and Letters

- Rui Wu, Ryo Minami, Yuuki Tsukui, Seitaro Kawai, Yuuki Seo, Shinji Sato, Kento Kimura, Satoshi Kondo, Tomohiro Ueno, Nurul Fajri, Shotarou Maki, Noriaki Nagashima, Yasuaki Takeuchi, Tatsuya Yamaguchi, Ahmed Musa, **Korkut Kaan Tokgoz**, Teerachot Siriburanon, Bangan Liu, Yun Wang, Jian Pang, Ning Li, Masaya Miyahara, Kenichi Okada, and Akira Matsuzawa, "64-QAM 60-GHz CMOS Transceivers for IEEE 802.11ad/ay," *IEEE Journal of Solid-State Circuits*, vol. 52, No. 11, pp. 2871-2891, Nov. 2017.

- Aravind Tharayil Narayanan, Makihiko Katsuragi, Kento Kimura, Satoshi Kondo, **Korkut Kaan Tokgoz**, Kengo Nakata, Wei Deng, Kenichi Okada, and Akira Matsuzawa, "A Fractional-N Sub-Sampling PLL Using a Pipelined Phase-Interpolator with an FoM of -250dB," *IEEE Journal of Solid-State Circuits*, vol. 51, no. 7, pp. 1630-1640, Jul. 2016.

- Seitaro Kawai, Shinji Sato, Shotaro Maki, **Korkut Kaan Tokgoz**, Kenichi Okada, and Akira Matsuzawa, "Accurate Transistor Modeling by Three-parameter Pad Model for Millimeter-Wave CMOS Circuit Design," *IEEE Transactions on Microwave Theory and Techniques*, vol. 65, no. 6, pp. 1736-1744, Jun. 2016.

A.5.2 Conferences

- Ibrahim Abdo **Korkut Kaan Tokgoz**, Takuya Fujimura, Kenichi Okada, and Akira Matsuzawa, "Comparison Between L-2L and Thru-Reflect-Line De-embedding Methods for W-Band CMOS Amplifier Design," *IEEE International Symposium on Radio-Frequency Integration Technology*, pp. 34-36, Seoul, Korea, Aug. 2017.

- Ibrahim Abdo **Korkut Kaan Tokgoz**, Takuya Fujimura, Kenichi Okada, and Akira Matsuzawa, "A 100-123GHz CMOS Frequency Doubler with 5.5dBm Output Power and High Fundamental Rejection," *IEEE International Symposium on Radio-Frequency Integration Technology*, pp. 138-140, Seoul, Korea, Aug. 2017 (Best Student Paper Award).

- Ibrahim Abdo **Korkut Kaan Tokgoz**, Takuya Fujimura, Kenichi Okada, and Akira Matsuzawa, "112GHz Frequency Doubler with High Output Power and Fundamental Rejection," *IEICE LSI and System Workshop*, University of Tokyo, Tokyo, Japan, May. 2017.

- Ibrahim Abdo **Korkut Kaan Tokgoz**, Kenichi Okada, and Akira Matsuzawa, "A 2.2dBm Output Power 110GHz Frequency Doubler," *IEICE General Conference*, C-12, Meijo university, Nagoya, Japan, Mar. 2017.

- Jian Pang, Shotaro Maki, Seitarou Kawai, Noriaki Nagashima, Yuuki Seo, Masato Dome, Hisashi Kato, Makihiko Katsuragi, Kento Kimura, Satoshi Kondo, Yuki Terashima, Hanli Liu, Teerachot Siriburanon, Aravind Tharayil Narayanan, Nurul Fajri, Tohru Kaneko, Toru Yoshioka, Bangan Liu, Yun Wang, Rui Wu, Ning Li, **Korkut Kaan Tokgoz**, Masaya Miyahara, Kenichi Okada, and Akira Matsuzawa, "A 128-QAM 60GHz CMOS Transceiver for IEEE802.11ay with Calibration of

LO Feedthrough and I/Q Imbalance," *IEEE International Solid-State Circuits Conference*, pp. 424-425, San Francisco, CA, Feb. 2017.

- Aravind Tharayil Narayanan, Makihiko Katsuragi, Kento Kimura, Satoshi Kondo, **Korkut Kaan Tokgoz**, Yuki Terashima, Wei Deng, Kenichi Okada, and Akira Matsuzawa, "A Fractional-N Sub-Sampling PLL using a Pipelined Phase-Interpolator with an FoM of -246dB," *IEEE European Solid-State Circuits Conference*, pp. 380-383, Graz, Austria, Sep. 2015.

- Seitaro Kawai, **Korkut Kaan Tokgoz**, Kenichi Okada, and Akira Matsuzawa, "L-2L De-embedding Method with Double-T-type Pad Model for Millimeter-Wave Amplifier Design," *IEEE Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems*, San Diego, CA, ja. 2015.

- Seitaro Kawai, **Korkut Kaan Tokgoz**, Kenichi Okada, and Akira Matsuzawa, "L-2L De-embedding Method with Double-T-type Pad Model for Millimeter-Wave Amplifier Design," *IEICE Analog-RF Study Group Workshop*, vol. RF2013-3, p. 1, Chuo University, Tokyo, Japan, Mar. 2014 (Original in Japanese).