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論 文 要 旨

THESIS SUMMARY

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要旨（英文 800 語程度）
Thesis Summary（approx.800 English Words ）

In this thesis, millimeter-wave CMOS wireless transceivers and techniques are proposed to achieve data-rates of more than 100Gb/s. More than 100Gb/s data-rates are required for several different applications for the near future. These applications can be divided into two as long-range and short-range. With the increased demand on the user-end for higher data-rates, 5G systems are being considered. To support the infrastructure for 5G systems, as a long-range application, wireless point-to-point backhaul and fronthaul networks achieving ultra-high data-rates have to be implemented since it is very expensive to connect every base-station by fiber-optic cables. An example for short-range application would be the uncompressed video data transfer for 4K, 8K ultra-high definition televisions within a small room as personal area network.

One way to reflect these high data-rate requirements is to use ultra-wideband frequency with high order modulations. Hence, in here, an ultra-wideband 70-to-105GHz wireless transceiver is implemented on 65nm CMOS technology based on frequency-interleaving architecture. This work achieves the world fastest data-rate of 120Gb/s. Frequency-interleaving architecture greatly relaxes the baseband design of the system, and hence; the overall system requirements are relaxed. This approach can be used either for long-range or short-range applications, by simply changing the gain of antennas. For this ultra-wideband transceiver, PA and LNA are designed from 70 to 105GHz. Positive feedback common-source topology is used to decrease the required number of stages for less area and power consumption while maintaining the required gain of the amplifiers. Since two LO signals are used and two up-converted data are combined to be transmitted simultaneously, cross-modulation effects have to be considered. High harmonic suppression doubler and tripler are designed to generate up- and down-conversion LO signals. Harmonic suppression value of more than 29dBc for doubler and 38dBc for tripler are realized, which minimize the cross-modulation between the two data-streams. Single-IF balanced up-conversion mixers with DC-offset cancellation circuitry are employed for LO leakage cancellation on transmitters. Receiver IF amplifiers work wideband from 0.3 to 20GHz. A low-loss PCB to waveguide transition is designed. TX, RX, and TX-to-RX measurements are conducted with the customized test module. Total core area of the circuitry occupies 3.2mm^2 whereas the whole IC occupies 6mm^2 of silicon area. TX power consumption is 120mW, and RX power consumption is 160mW.

For ultra-high data-rate systems, as explained above, ultra-wideband transceivers might be a solution. Considering the frequency allocation regulated by governmental bodies, 300GHz frequency region can be a great candidate since there is no frequency allocation after 275GHz. Moreover, frequency region after 252GHz can be used for mobile or fixed wireless systems. One of the main problems about this frequency region is that, it is difficult to implement full CMOS transceivers with PA and LNA since the maximum unity gain of CMOS transistors are well below 300GHz frequency region and, hence; it is difficult to achieve gain for transistors. For this reason, in here, the transistor layout is optimized to increase the maximum unity gain frequency of the transistors to 317GHz. Thus, the gain of the transistors is increased in the 300GHz frequency band. An amplifier is designed using the optimized transistors. 16-stage positive feedback common-source topology is used for the amplifier. The amplifier has gain from 273GHz to 301GHz, and the peak gain is 21dB at 298GHz. The power consumption is 35.4mW from a 1.2V supply. The proposed amplifier achieves the highest gain frequency among all the bulk CMOS amplifiers. The ratio of the upper frequency to maximum unity gain frequency is the highest record of 0.95. By this way, full CMOS terahertz transceiver solutions are possible with PA and LNA allowing more cost-effective solutions.

As mentioned above data-rates for more than 100Gb/s is also required for future; such as wireless personal area networks. Since these kind of applications are to be adopted by the user end, it is important to consider the systems to be cost effective. Frequency allocation and usage of frequencies is one of the major costs for wireless systems. For this reason, 60GHz frequency region has great potential in that sense, because it is unlicensed and free to use. To achieve data-rates of more than 100Gb/s at this frequency, on the other hand, MIMO application is a must for full CMOS solutions. Again, CMOS manufacturing technology is aimed for lower cost, compactness and monolithic implementation of these systems.

Nevertheless, MIMO systems are costly in terms of number of antennas used and the consumed silicon area. To address these issues, in this thesis, two different solutions are provided. First one is the low-loss transmitter-receiver switch, to decrease the number of antennas to be used in the system by half while considering to preserve the system performance as close as the conventional transceiver approaches which do not have any kind of transmit/receive antenna switch circuitry. The switch circuitry is proposed based on re-using LNA and PA transistors as switching elements with matching block design for TDD transceivers. Switch architecture has no area consumption with 1.1dB minimum loss in RX mode and 2.3dB minimum loss in TX mode.

With the transmitter-receiver switch, the number of antenna for the system can be halved with lower loss in comparison with the conventional methods. However, the silicon area is still the same for the whole transceivers. To address this issue, i.e. to decrease the silicon consumption area while maintaining one antenna per transceiver, an asymmetrical bi-directional amplifier is implemented to be used in bi-directional transceivers. Conventional bi-directional transceivers either use SPDT switches between LNA and PA aiming to decrease the number of antennas. Others use bi-directional amplifiers with same gain, noise and linearity characteristics for both ways, hence does not reflect LNA and PA requirements for a wireless link. In here, a 60GHz single-ended bi-directional power/low-noise amplifier for TDD is proposed. Positive feedback is used based on transmission lines. The placement of positive feedback transmission line in each stage changes the gain boosting either for LNA mode or PA mode. The designed asymmetrical bi-directional LNA/PA is manufactured on 65nm bulk CMOS. The total area is 0.82mm^2. The results show that different gain requirements can be achieved and the gain of LNA mode is around 20dB maximally. Isolation results are less than −50dB which might be the one of the concerns for a bi-directional amplifier. Return losses are also around 10dB in the band of interest and hence different matching conditions can be satisfied for a TDD system. This approach can be a great candidate for short-range wireless communications; such as personal area networks. The cost of the overall system can be decreased considerably by decreasing the number of antenna by half and the silicon area consumption more than half.

For all these complex transceiver systems, amplifiers, and other circuitry working at millimeter-wave and terahertz frequency regions; accurate methods on device layout optimization, de-embedding, characterization and modeling are done for both active and passive devices to achieve robust and accurate wireless transceivers. The characterization of devices is done up to 320GHz.