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A Surge-Less Solid-State DC Circuit Breaker for Voltage Source Converter Based HVDC Systems

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***Abstract*—This paper proposes a dc circuit breaker for voltage source converter (VSC) based high voltage dc transmission (HVDC) systems. Technical challenges for applying dc circuit breakers are to increase blocking voltage and to suppress surge voltage at the current clearing. The proposed dc circuit breaker is a solid-state breaker which consists of a number of semiconductor devices in series. It maintains equal voltage balancing among the devices to apply it to high voltage applications. Moreover, the surge voltage across the circuit breaker is reduced by employing a freewheeling diode. Considering a system rated at 300 MW in power and 250 kV in dc voltage, conduction loss of the proposed circuit breaker is estimated to be 0.045% of the rated power. The value is smaller than the power loss of the VSCs. A downscaled HVDC system rated at 10 kW in power and 360 V in dc voltage was built and tested. A series of experimental results demonstrate the dc fault clearing and rapid restoration of power transmission.**

***Index Terms*—dc circuit breaker, high voltage dc transmission, voltage source converter, fault protection.**

I. Introduction

High voltage dc transmission (HVDC) systems are widely applied to large capacity and long distance power transmissions in recent power systems, and they are also one of the key technologies to utilize remote renewable energy resources such as offshore wind power and large-scale solar power [1]. Conventional HVDC systems adopt line-commutated current-source converters (CSCs) consisting of thyristors. In recent years, a system based on self-commutated voltage-source converters (VSCs) consisting of IGBTs is also applied to many projects because it has advantage in control characteristics and reduction of ac filters and shunt capacitors. Two-level and three-level VSCs have been installed in the 2000s, and modular multilevel converters (MMC) [2], [3] have been also put to practical use since 2010.

Although the VSCs are superior to the CSCs in some characteristics, the VSCs have a drawback in their current control capability during short circuit fault within the dc circuit [4], [5]. In that case, ac circuit breakers are opened to remove the whole HVDC system from the grid [6]. This method has already been demonstrated in a commercial system [7]. However, the method forces the VSCs to take certain amount of time before restarting it and resuming power transmission. Moreover, the converter has to withstand the fault current until the ac breakers clear the fault.

In order to recover from the dc faults in the VSC HVDC systems without opening ac breakers, various dc circuit breakers have been studied [4], [5]. The dc circuit breakers can be grouped in mechanical and solid state solutions. The mechanical dc circuit breakers consist of a conventional ac circuit breaker supplemented with a parallel resonant circuit [8]–[10]. The time to current interruption is typically 30-100 ms, which is too long for protecting low-impedance dc networks. The fault current will rapidly rise and the VSC converters cannot take full fault current for such long time. The mechanical dc circuit breaker might be adequate with CSCs but they are not ideally suitable for VSC networks [11], [12]. Solid-state circuit breakers are a promising option in operation speed in a system rated at several hundred kV [12]–[15].

If the dc breaker immediately interrupts the fault current, the VSCs can continue their operation and restart power transmission just after clearing the fault. If the HVDC system has a multi-terminal dc network, the dc breaker can remove only the fault section. However, there are some problems in surge voltage across the breaker arising from current interruption, and large energy absorption at current interrupting device.

The authors propose a circuit topology for the solid-state dc circuit breaker rated at several hundred kV. It is then applied to a VSC HVDC system to continue converter's operation during the fault and to restart power transmission quickly [16]. The blocking voltage of the breaker is increased by connecting many valve devices in series, together with snubber circuits to maintain voltage balancing among the devices. A freewheeling diode is applied to bypass the fault current. The diode suppresses the surge voltage arising from current interruption, resulting in the reduction of series connected devices and conduction loss. The proposed dc breaker can rapidly remove dc faults in the VSC HVDC system without operating ac breakers. Moreover, it can realize continuous operation of the VSCs to maintain ac voltages by supplying reactive power even during the dc faults. A downscaled HVDC system rated at 10 kW in power and 360 V in dc voltage is built, then a series of tests are executed to verify the operating performance of the proposed system.

II. DC Fault and its Clearing Methods in VSC HVDC Systems

Most of the voltage source converter based high voltage dc transmission (VSC HVDC) systems consist of two-level converters, three-level neutral point clamped (NPC) converters [17], or modular multilevel converters (MMC) with half-bridge inverter cells [6]. All of the existing systems have a drawback that the converters lose their current control capability when a short circuit fault occurs within the dc circuit [4], [5]. The VSCs have small impedance in the dc side because their dc capacitor is parallel to the dc transmission line. When a line-to-ground or line-to-line fault occurs in the dc transmission line, VSC's dc capacitor is discharged by way of the fault point. Then the fault current rapidly increases. Gate block operation of the VSC does not interrupt the fault current because the current flows through the VSC's reverse conducting diodes during the fault. As a result, its ac current increases and the fault affects the ac side. MMCs with half-bridge inverter cells, also, can not interrupt the dc fault current flowing through its reverse conducting diodes.

Three dc fault clearing methods have been considered for VSC HVDC systems [4], [18]. Each method utilizes ac circuit breakers, dc circuit breakers, or an MMC with full-bridge inverter cells.

The most commonly applied method is opening ac circuit breakers to remove the whole HVDC system from the healthy ac grid [6]. This method has already been demonstrated in the Caprivi Link HVDC in Namibia [7]. The system detects and clears the dc fault in 75 ms and resumes power transmission after 700 ms. The converter has to withstand the fault current until the ac breakers clear the fault. Moreover, all the ac circuit breakers have to be opened in a system which shares dc transmission line among multiple converters (multi-terminal dc transmission). Therefore, a dc line fault causes the temporary halt of the whole HVDC system.

Fault clearing by dc circuit breakers has been considered for a long time. If the dc breaker can clear the fault before discharging dc capacitors, the VSCs can continue their operation and resume power transmission just after the fault clearing. Fast opening dc circuit breakers are necessary to realize this method and several configurations have been considered [5], [12]. The turn off speed should be less than several milliseconds when the dc line voltage is several hundred kV. Therefore, it is hard to realize the operation using the conventional mechanical circuit breakers. Solid-state dc circuit breakers have been considered to realize fast opening operation because it does not have moving parts and arc discharge. Hybrid dc circuit breakers which combines a fast mechanical switch and semiconductor switches have been also studied [19], [20] to satisfy both fast opening operation and low conduction loss. A hybrid dc circuit breaker interrupting dc 1.5 kV/4 kA in 300 μs has been realized [21]. Another hybrid dc circuit breaker consists of a number of IGBT modules connected in series using RCD snubber circuits to realize interruption of dc 320 kV/2.6 kA in 2 ms [13] for HVDC applications.

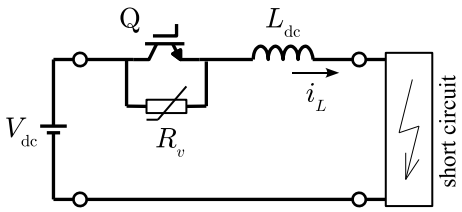


Fig. 1. A dc circuit breaker paralleling a non-linear resistor.

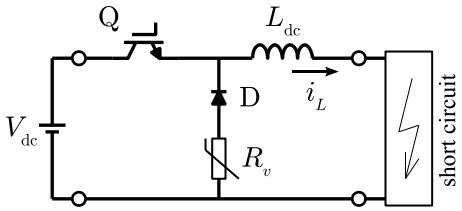


Fig. 2. A dc circuit breaker with a freewheeling diode.

MMCs with full-bridge inverter cells can realize fault clearing by the VSC itself [22], [23]. The system does not need fast fault detection because it can suppress the increase of the fault current. However, the number of power devices is double comparing to the MMCs with half-bridge inverter cells, and it causes the increase of the power loss.

III. DC Circuit Breakers and their Absorbing Energy

A. DC Circuit Breaker Paralleling a Non-Linear Resistor

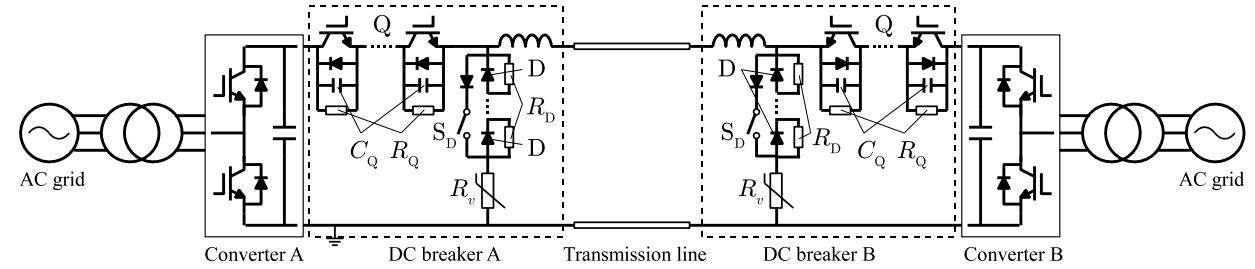
Fig. 1 shows a typical circuit configuration of a solid-state dc circuit breaker [12]. A voltage source $V_{\rm dc}$ supplies dc power to a resistive load by way of inductance $L_{\rm dc}$. $L_{\rm dc}$ is the overall inductance in the dc circuit consisting of the dc circuit breaker, the dc line, and the load. A semiconductor valve device Q is inserted between the source and the load, and a varistor[1] R_v is connected in parallel with it. Q remains on-state during normal condition, and the current i_L flows from the source to the load. Q is turned off when a short circuit fault is detected in the load side. Then the fault current i_L commutates to the varistor R_v. Surge voltage across Q is suppressed to the clamping voltage of the varistor R_v. The clamping voltage is larger than $V_{\rm dc}$, and it is assumed as $V_{\rm dc} + V_{\rm margin}$. Then reverse voltage is applied to $L_{\rm dc}$, and the fault current decreases.

It is assumed that the impedance of the fault point is negligibly small. When Q turns off at time $t = 0$, $V_{\rm margin}$ is applied to $L_{\rm dc}$. Then the inductor current i_L flowing through $L_{\rm dc}$ is shown as a function of time t as follows:

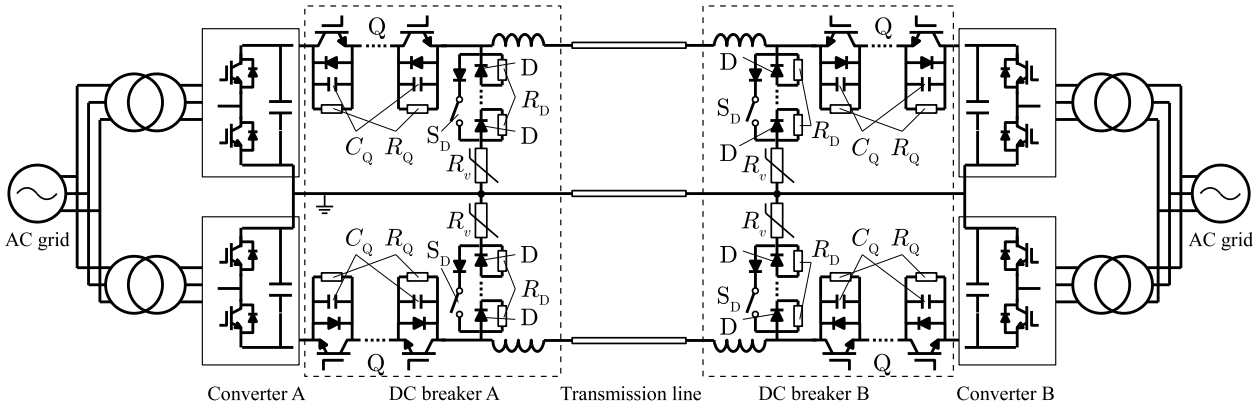
$$i_L = I_0 - \frac{V_{\rm margin}}{L_{\rm dc}} t, \tag{1}$$

where I_0 is the amplitude of the fault current at $t = 0$. The time to turn off the fault current $T_{\rm open}$ is derived by substituting

[1]It is also called as "surge arrester." In this article, "varistor" is used to refer to a non-linear resistor whose resistance varies with its applied voltage.



(a) unipolar configuration



(b) bipolar configuration

Fig. 3. VSC HVDC systems being capable of clearing dc line faults.

$i_L = 0$ to (1) as follows:

$$T_{\rm open} = \frac{L_{\rm dc}}{V_{\rm margin}} I_0. \tag{2}$$

Therefore, $T_{\rm open}$ is inversely proportional to $V_{\rm margin}$.

The energy absorbed in R_v during $T_{\rm open}$ is calculated as follows:

$$W_R = \int_0^{T_{\rm open}} (V_{\rm dc} + V_{\rm margin}) i_R \, dt, \tag{3}$$

where i_R is the current flowing to R_v. Because i_R is equal to i_L during $0 \le t \le T_{\rm open}$, i_L in (1) and $T_{\rm open}$ in (2) are substituted to (3). Then the energy absorbed in R_v is given by

$$\begin{aligned} W_R &= \int_0^{\frac{L_{\rm dc} I_0}{V_{\rm margin}}} (V_{\rm dc} + V_{\rm margin}) \left(I_0 - \frac{V_{\rm margin}}{L_{\rm dc}} t \right) dt \\ &= (V_{\rm dc} + V_{\rm margin}) \left[I_0 t - \frac{V_{\rm margin}}{2 L_{\rm dc}} t^2 \right]_0^{\frac{L_{\rm dc} I_0}{V_{\rm margin}}} \\ &= \left(\frac{V_{\rm dc}}{V_{\rm margin}} + 1 \right) \frac{1}{2} L_{\rm dc} I_0^2. \end{aligned} \tag{4}$$

$V_{\rm margin}$ is usually much smaller than $V_{\rm dc}$ in high power applications in order to reduce the blocking voltage of Q. In such case, the term in the parenthesis of (4) becomes much greater than 1, and W_R is much greater than the stored energy in $L_{\rm dc}$ at $t = 0$, which is $L_{\rm dc} I_0^2/2$. Therefore, the suppression of the voltage across Q increases the energy absorption in the varistor.

B. DC Circuit Breaker with a Freewheeling Diode.

Fig. 2 shows a circuit configuration of the solid-state dc circuit breakers using a freewheeling diode. A freewheeling diode D and a varistor R_v are connected across the dc line. This circuit can reduce the energy absorbed in the breaker with suppressing the surge voltage across the valve device Q.

In normal condition, Q remains on-state and leads the load current i_L. When Q turns off at t = 0 after detecting a fault, the fault current i_L commutates to D. Hence, the current flowing through $V_{\rm dc}$ immediately decreases to zero. The inductance $L_{\rm dc}$ is demagnetized by R_v, and the fault current i_L gradually decreases. When the clamping voltage of R_v is expressed in V_v, The surge voltage across Q is $V_{\rm dc} + V_v$, where $V_{\rm dc}$ is the voltage of the dc source and V_v is the clamping voltage of R_v.

Because $V_{\rm dc}$ does not supply any power after turning off Q, the energy absorbed in the dc breaker at the turn-off operation is equal to the energy stored in $L_{\rm dc}$ by the current I_0. So the energy absorbed in R_v is given by

$$W_R = \frac{1}{2} L_{\rm dc} I_0^2. \tag{5}$$

Since W_R in (5) is smaller than W_R in (4), the rating and volume of R_v can be reduced by applying the freewheeling diode. Because W_R is not the function of the clamping voltage V_v, the surge voltage across Q can be also suppressed by choosing a low value for V_v without increase of W_R.

Since the dc circuit breaker with the freewheeling diode has the aforementioned advantages, the following sections consider to apply it to VSC HVDC systems.

IV. VSC HVDC Systems being Capable of Clearing DC Line Faults

A. System Configuration

Fig. 3 shows the proposed VSC HVDC systems being capable of clearing dc line faults. Voltage source converters are usually selected from a two-level converter, a neutral-point clamped (NPC) converter, and a modular multilevel converter (MMC). Fig. 3 (a) shows a unipolar configuration. The dc breakers A and B are modified based on the circuit topology shown in Fig. 2, and they are inserted between the converter and a dc transmission line to clear the dc line faults. The valve device Q consists of IGBTs and reverse conducting diodes to enable bidirectional power flow. Fig. 3 (b) shows a bipolar configuration, where each pole can independently clear the dc line faults.

In order to realize high blocking voltage, Q and the freewheeling diode D consist of many devices connected in series using snubber circuits as well as the HVDC breaker in [13]. Q and D have resistors R_{Q} and R_{D} in parallel to maintain voltage balancing of the series connected devices in steady states. In addition, Q has snubber capacitors C_{Q} to maintain voltage balancing during turn-off transients by realizing zero-voltage switching of Q [25]. A semiconductor device which has self-power supply and built-in sensor functions has been developed for applying to circuit breakers [24]. Applying the device will simplify the system configuration. A mechanical switch $\mathrm{S_D}$ is connected to D in parallel to keep the line voltage to ground voltage while the breaker opens. While the HVDC breaker [13] connects varistors in parallel with the opening switches Q, the proposed system has a varistor R_v across the dc line in series with the diodes D. As a result, it realizes the reduction of the surge voltage accompanying the current clearing.

B. Current Turn-Off (Breaker's Opening) Operation

A current turn-off operation of the proposed dc circuit breaker is described when a power flows from the converter A in rectifier operation to the converter B in inverter operation. Since the system configuration shown in Fig. 3 is symmetrical, the breakers behave in the same sequence also in the opposite power flow.

Fig. 4 depicts a transition of the current route in the dc breaker A which is located in the sending end. (a) shows a regular current route before a fault. In this case, Q remains on-state and flows load current. (b) shows a current route right after the short circuit fault in the dc line. Then the dc capacitor discharges by way of the fault point, and the current rapidly increases. When the current increase is detected, Q is immediately turned off. The fault current commutates to the snubber capacitors C_{Q}, then the state changes to (c). Each valve device in Q turns off with zero-voltage switching because of C_{Q}. Moreover, the voltages across the devices

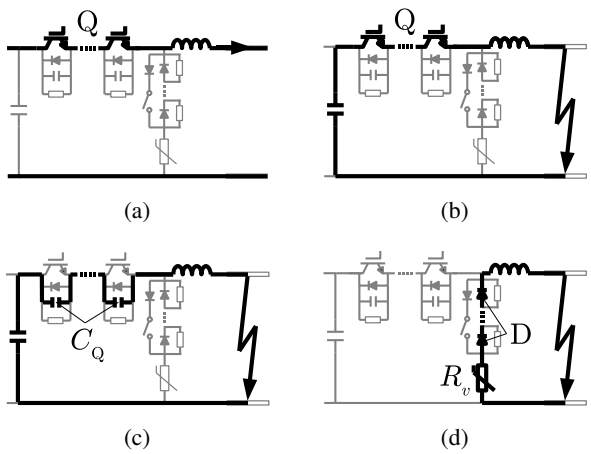


Fig. 4. A transition of the current route in the dc breaker A (sending end).

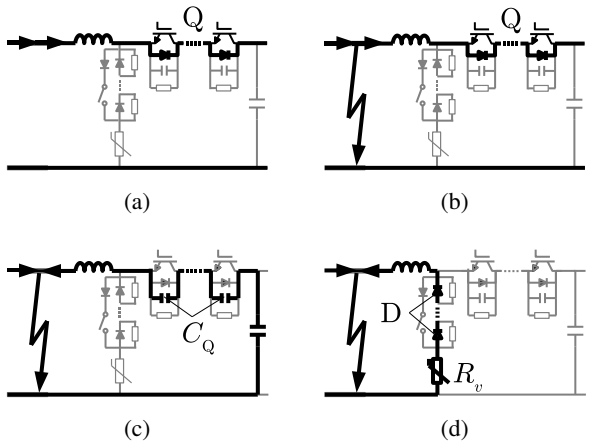


Fig. 5. A transition of the current route in the dc breaker B (receiving end).

are almost equally balanced even if there is small difference among their turn-off time. When C_{Q} is charged enough, the freewheeling diode D turns on. In the state (d), the line inductance is demagnetized by R_v, then the fault current turns off in a certain period of time.

Fig. 5 depicts a transition of the current route in the dc breaker B which is located in the receiving end. (a) shows a regular current route before a fault. In this case, the current flows by way of Q's reverse conducting diodes. Although no forward current flows in Q in this state, the transistors' gate signal is kept on-state in case of power reversal. (b) shows a current route right after the short circuit fault in the dc line. Because a part of the dc current flows to the fault point, the inductor current decreases. When the current decrease is detected, Q's gate signal is turned off. Since no forward current flows in Q, no transition happens at this time. When the inductor current reaches zero, Q's reverse conducting diodes turn off and the state changes to (c). Then the current charges the snubber capacitors C_{Q}. When C_{Q} is charged enough, the freewheeling diode D turns on. In the state (d), the fault current is turned off by the varistor R_v in a certain period of time.

TABLE I
SPECIFICATIONS OF AN IGCT (ABB 5SHY 35L4512) [26].

Peak off-state voltage	V_{DRM}	4,500 V
Permanent dc voltage for 100 FIT failure rate		2,800 V
Max. controllable turn-off current	I_{TGQM}	4,000 A
Max. average on-state current	$I_{T(AV)M}$	2,100 A
Turn-off delay time	$T_{d(\mathrm{off})}$	< 11 μs
On-state voltage (at $I_T = 1.2$ kA, $T_j = 125$ °C)	V_T	1.24 V

TABLE II
A DESIGN EXAMPLE OF THE DC BREAKER RATED AT 300 MVA AND DC 250 KV.

Power rating		300 MVA
Nominal dc line voltage	V_{dc}	250 kV
Number of series connected IGCTs		90
DC voltage across an IGCT	V_{Q}	2.8 kV
Conduction loss at rated power		134 kW
Varistor clamping voltage	V_v	25 kV
Snubber capacitor	C_{Q}	4.1 μF
DC inductor	L_{cb}	25 mH

C. Insulation Recovery and Turn On (Breaker's Reclosing) Operation

After turning off the fault current, the transmission line is maintained to low voltage for certain amount of deionization time in order to recover insulation. A switch $\mathrm{S_D}$ is connected in parallel with D, and it is turned on after the fault detection. $\mathrm{S_D}$ may be consisted of a mechanical switch with low current rating because the fault current do not flows $\mathrm{S_D}$ but flows D. $\mathrm{S_D}$ bypasses the current flowing from R_{Q} to the grounding line after turning off the fault current. Then the dc line voltage is maintained to the clamping voltage of R_v, which is much lower than the nominal dc line voltage.

When $\mathrm{S_D}$ is turned off, the dc line starts to be charged by way of R_{Q}. The voltage increases to the level decided by the ratio of R_{Q} and R_{D}. The dc line can be charged to the nominal dc line voltage by setting as $R_{\mathrm{Q}} \ll R_{\mathrm{D}}$. Then the dc breaker recloses by turning on Q with zero voltage switching.

If the dc line fault still continues, the current flows into the fault point after turning off $\mathrm{S_D}$. Then the dc line voltage will not increase. Hence, the reclosing process can be suspended by monitoring the line voltage after turning off $\mathrm{S_D}$.

D. A Conceptual Design Example

In order to give a rough idea about the proposed dc circuit breaker, the breaker is designed for an HVDC system rated at 300 MVA in power and 250 kV in dc voltage. Specifications of a 4.5-kV integrated gate-commutated thyristor (IGCT, ABB 5SHY 35L4512 [26]) shown in Table I are employed for this design.

When the applied voltage of an IGCT V_{Q} is set to 2.8 kV to satisfy 100 FIT failure rate, 90 devices should be connected in series for blocking dc 250 kV. The IGCT's on-state voltage is 1.24 V at rated dc current 1.2 kA (= 300 MVA / 250 kV). So total conduction loss P_{loss} is

$$\begin{aligned} P_{\mathrm{loss}} &= 1.24\ _{\mathrm{V}} \times 1.2\ _{\mathrm{kA}} \times 90\ _{\mathrm{devices}} \\ &= 134\ \mathrm{kW}, \end{aligned} \tag{6}$$

which is 0.045% of the rated power 300 MVA. The loss of the breakers is smaller than that of converters which is usually around 1-2% of the rated power. However, the heat dissipated at the breaker is still large value. Therefore, some cooling equipments will be necessary to dissipate the heat.

The inductance of the dc circuit breaker L_{cb} is assumed to be 25 mH to limit the maximum rise of the fault current less than 10 kA/ms. Considering time delays of 39 μs for fault detection and 11 μs for IGCTs' turn-off delay, total delay time T_{delay} is assumed to be 50 μs. It is assumed that the fault occurs at the point close to the dc breaker, which is the most severe condition in terms of fault current increase. Increase of the inductor current ΔI_{dc} during the delay time is given by

$$\begin{aligned} \Delta I_{\mathrm{dc}} &= V_{\mathrm{dc}} T_{\mathrm{delay}} / L_{\mathrm{cb}} \\ &= 250\ _{\mathrm{kV}} \times 50\ _{\mu\mathrm{s}} / 25\ _{\mathrm{mH}} \\ &= 0.50\ \mathrm{kA}. \end{aligned} \tag{7}$$

When the overcurrent protection level is set at 1.8 kA which is 150% of the rated current, the turn-off rating required to the breaker is 2.3 kA by adding ΔI_{dc}.

Difference of IGCTs' turn-off delay time influences voltage balancing of the devices. The difference is reported as approximately less than 0.3 μs [27]. Considering the difference of gate drive circuits, total difference in turn-off time is assumed to be 0.5 μs. Charging time of the snubber capacitors T_{charge} is designed to 5 μs to be larger than the difference in turn-off time by a factor of ten. Therefore, the snubber capacitance C_Q to meet the condition is given by

$$\begin{aligned} C_{\mathrm{Q}} &= I_0 \cdot T_{\mathrm{charge}} / V_{\mathrm{Q}} \\ &= 2.3\ _{\mathrm{kA}} \cdot 5\ _{\mu\mathrm{s}} / 2.8\ _{\mathrm{kV}} \\ &= 4.1\ \mu\mathrm{F}. \end{aligned} \tag{8}$$

Clamping voltage of the varistor V_v is designed to 25 kV which is 10% of the dc line voltage. The total voltage across Q is 275 kV (= $V_{\mathrm{dc}} + V_v$) during fault clearing and the value is within Q's blocking voltage 405 kV (= 4.5 kV $\times$ 90). The aforementioned design parameters are summarized in Table II.

Since the overall inductance in the dc circuit is $L_{\mathrm{dc}} = L_{\mathrm{cb}}$, the time to turn-off the fault current T_{open} is given by

$$\begin{aligned} T_{\mathrm{open}} &= L_{\mathrm{cb}} \cdot I_0 / V_v \\ &= 25\ _{\mathrm{mH}} \cdot 2.3\ _{\mathrm{kA}} / 25\ _{\mathrm{kV}} \\ &= 2.3\ \mathrm{ms}. \end{aligned} \tag{9}$$

The energy absorbed in the varistor W_R is obtained from (5) as follows:

$$\begin{aligned} W_R &= \frac{1}{2} L_{\mathrm{cb}} I_0^2 \\ &= \frac{1}{2} \cdot 25\ _{\mathrm{mH}} \cdot (2.3\ _{\mathrm{kA}})^2 \\ &= 66\ \mathrm{kJ}. \end{aligned} \tag{10}$$

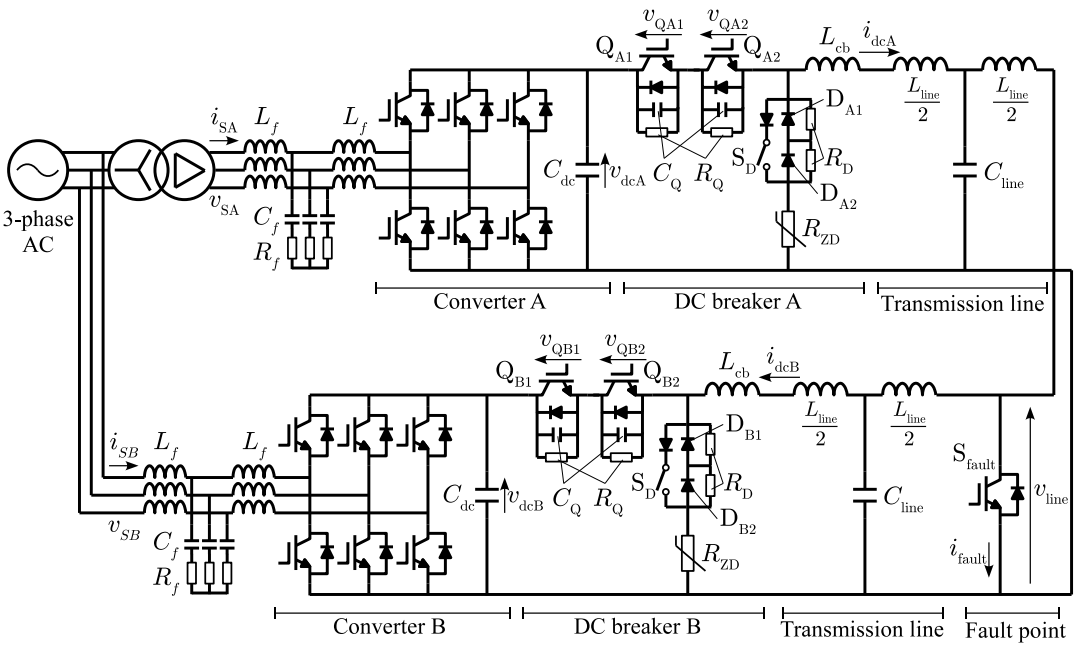


Fig. 6. Circuit configuration of the experimental setup.

When the fault occurs in the distance from the dc breaker, inductive energy stored in the dc transmission line should also be considered. Assuming a fault in a distant of 200 km through a dc transmission line whose inductance is 1.41 mH/km, total inductance including return path $L_{\rm line}$ is 564 mH (refer to Appendix). Since the overall inductance in the dc circuit is $L_{\rm dc} = L_{\rm cb} + L_{\rm line}$, the time to turn-off the fault current $T_{\rm open}$ is given by

$$\begin{aligned} T_{\rm open} &= (L_{\rm cb} + L_{\rm line}) \cdot I_0 / V_v \\ &= (25\ {\rm mH} + 564\ {\rm mH}) \cdot 2.3\ {\rm kA} / 25\ {\rm kV} \\ &= 54\ {\rm ms}. \end{aligned} \tag{11}$$

The energy absorbed in the varistor W_R is obtained from (5) as follows:

$$\begin{aligned} W_R &= \frac{1}{2} \cdot (L_{\rm cb} + L_{\rm line}) \cdot I_0^2 \\ &= \frac{1}{2} \cdot (25\ {\rm mH} + 564\ {\rm mH}) \cdot (2.3\ {\rm kA})^2 \\ &= 1.6\ {\rm MJ}. \end{aligned} \tag{12}$$

The capacity of the varistor W_R should be designed based on the farthest dc fault where the energy absorbed in the varistor is maximum.

V. Experimental Results

Fig. 6 shows the circuit configuration of the experimental setup. The photograph of the setup is shown in Fig. 7. Circuit and control parameters of the experimental setup is shown in Table III. Converter A and B consist of a three-phase two-level converter using a 6-in-1 IGBT module rated at 600 V and 75 A, and their ac terminals are connected to a three-phase ac 200 V source. Although both of the converters are usually

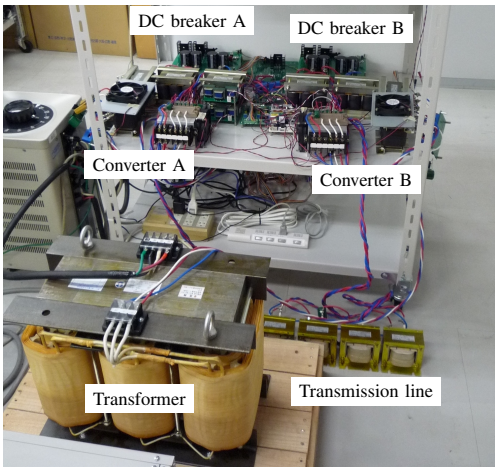


Fig. 7. Experimental setup.

connected to the source by way of a transformer in actual system, the experimental setup omits the transformer of the converter B for simplifying the setup. A semiconductor switch $\rm S_{fault}$ is connected across the dc transmission line to simulate short circuit faults. A dc breaker is inserted between the transmission line and the converter. The dc breaker has two IGBTs $\rm Q_{A1}$ and $\rm Q_{A2}$ which is rated at 600 V (HGTP12N60A4D) and they are connected in series. Zener diodes $\rm R_{ZD}$ whose breakdown voltage is 9.1 V are applied as surge absorbing device instead of varistors because the system voltage is low in the experiment. A electromagnetic mechanical relay is applied to the switch $\rm S_D$.

The controller for the converter A and B consists of a digital signal processor (DSP) (Texas Instruments TMS320C6713),

TABLE III
CIRCUIT AND CONTROL PARAMETERS OF THE EXPERIMENTAL SETUP.

Power rating		10 kVA
AC line-to-line rms voltage	V_S	200 V
Filter inductor	L_f	0.35 mH (2.7%†)
Filter capacitor	C_f	8.2 μF
Filter resistor	R_f	1.0 Ω
Switching frequency		20 kHz
Nominal dc line voltage	V_{dc}	360 V
DC inductor	$L_{\rm cb}$	1.5 mH
DC capacitor	$C_{\rm dc}$	1,800 μF
Balancing resistor of IGBTs	$R_{\rm Q}$	47 kΩ $*^1$ 2.0 kΩ $*^2$
Balancing resistor of diodes	$R_{\rm D}$	470 kΩ
Snubber capacitor	$C_{\rm Q}$	0.47 μF
Inductance of a transmission line	$L_{\rm line}$	0 mH $*^1$ 14.4 mH $*^2$
Capacitance of a transmission line	$C_{\rm line}$	0 μF $*^1$ 6.8 μF $*^2$
Breakdown voltage of varistors	V_{RZD}	9.1 V

† on a three-phase, 200-V, 10-kVA, 50-Hz base
$*^1$ without transmission line, $*^2$ with transmission line

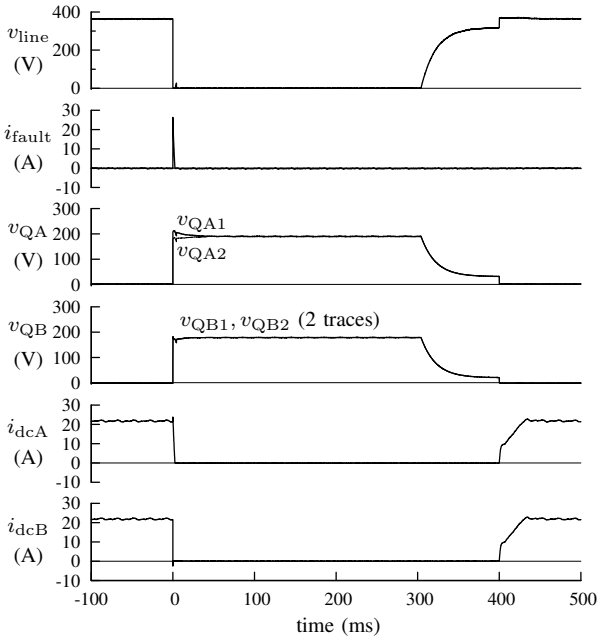


Fig. 8. Experimental waveforms of the dc breakers in the system without line impedance.

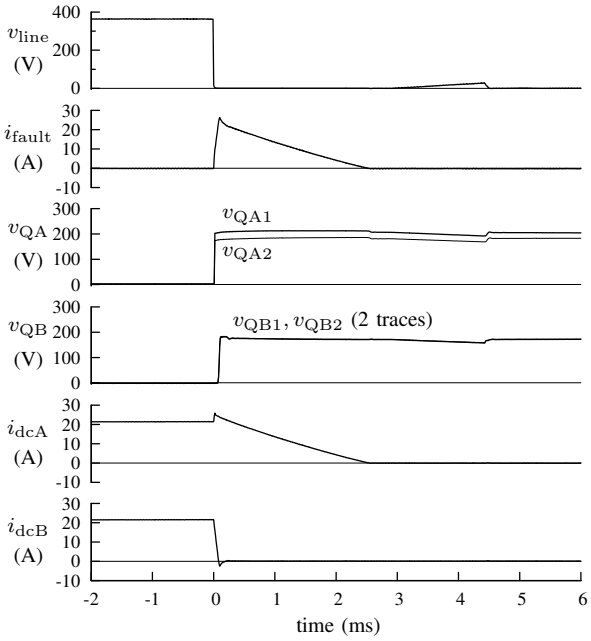


Fig. 9. Experimental waveforms of the dc breakers in the system without line impedance (enlarged time axis).

an field programmable gate array (FPGA) (Xilinx Spartan-3), and AD converters (Analog Devices AD7266). The controller for the dc breaker A and B consist of a FPGA (Xilinx Spartan-3) and an analog detection circuit by a current transducer and operational amplifiers.

The converter in rectifier mode was operated to control its active power flow, and the converter in inverter mode was operated to control the dc line voltage in the experiment. In general, the operation of the dc circuit breakers is not influenced by replacing the control method each other between the inverter and rectifier. Each dc breaker is independently controlled and there is no communication link between the breakers and the converters.

A. Fundamental Operation of the DC Breakers

The experiments in this section are carried out without line impedance ($L_{\rm line} = 0$, $C_{\rm line} = 0$) in order to verify fundamental characteristics of the dc breaker. A short circuit fault occurred in the dc line during 9 kW transfer from the converter A to the converter B.

Fig. 8 shows the waveforms of dc line voltage $v_{\rm line}$, current in the fault point $i_{\rm fault}$, voltages across dc breakers' IGBT $v_{\rm QA1}$, $v_{\rm QA2}$, $v_{\rm QB1}$, $v_{\rm QB2}$, and dc inductor currents $i_{\rm dcA}$, $i_{\rm dcB}$. Fig. 9 is the same waveforms being expanded around $t = 0$. When the converter A sends 9 kW power, $\rm S_{fault}$ was closed at $t = 0$ to simulate a short circuit fault. Then $v_{\rm line}$ dropped to 0 V. At the same time, dc capacitor voltages $v_{\rm dcA}$ and $v_{\rm dcB}$ were applied to the dc inductors $L_{\rm cb}$, resulting in the increase of $i_{\rm dcA}$ and decrease of $i_{\rm dcB}$. The fault was detected by the immediate increase/decrease of $i_{\rm dcA}$ and $i_{\rm dcB}$, and then gate signals of $\rm Q_{A1}$, $\rm Q_{A2}$, $\rm Q_{B1}$, $\rm Q_{B2}$ were turned off. The gate signals of $\rm Q_{A2}$ and $\rm Q_{B2}$ were intentionally delayed by 0.5 μs to simulate variation in turn-off time of the devices. Difference between $v_{\rm QA1}$ and $v_{\rm QA2}$ right after the turn-off was 29 V (8.1% of the dc voltage), and the voltage of the devices are balanced well. No voltage imbalance was observed between $v_{\rm QB1}$ and $v_{\rm QB2}$ because $\rm Q_{B1}$ and $\rm Q_{B2}$ flow the current via their reverse conducting diode and the variation of their gate signals did not affect their operation. It took 15 μs from the beginning of the fault to the IGBTs' turn-off operation, and the dc current increased by 20% during the period. The fault current was commutated to the freewheeling diode at t = 15 μs. Then $i_{\rm dcA}$ and $i_{\rm dcB}$ decreased and reached zero after 2.5 ms. $\rm S_{fault}$ was turned off when its current reached zero in order to simulate fault clearing. $\rm S_D$ was turned on at t = 4.5 ms, and

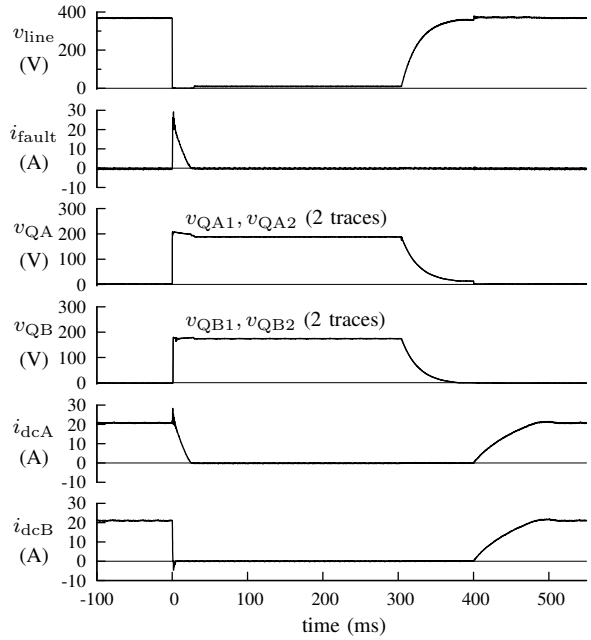


Fig. 10. Experimental waveforms of the dc breakers in the system with the transmission line model.

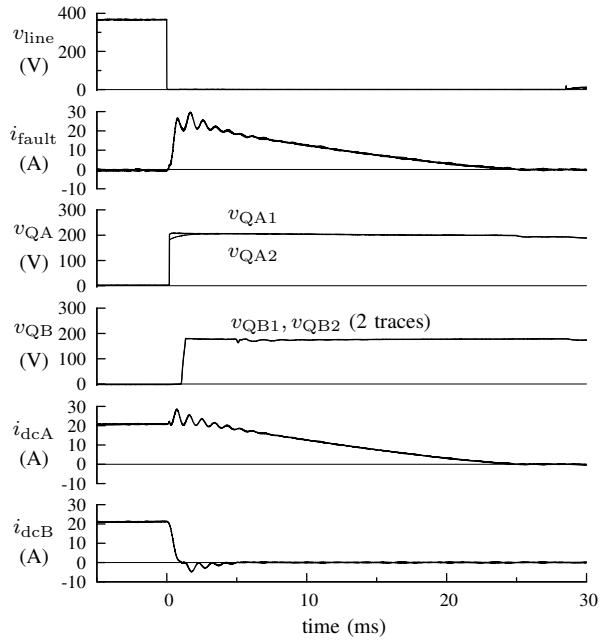


Fig. 11. Experimental waveforms of the dc breakers in the system with the transmission line model (enlarged time axis).

kept the line voltage to almost zero during their deionization time. It was 300 ms in the experiment. Then $\rm S_D$ was turned off and the dc line was recharged by way of $R_{\rm Q}$. Power transfer was resumed at t = 400 ms by turning on $\rm Q_{A1}$, $\rm Q_{A2}$, $\rm Q_{B1}$, and $\rm Q_{B2}$.

The energy absorbed in the breaker was roughly calculated from $i_{\rm fault}$ in Fig. 9. The total charge flowing through the interrupting circuit during the current turn-off was 0.030 C ($= 1/2 \times 24$ A $\times$ 2.5 ms) by approximating the waveform as a right-angled triangle. Voltage drop in the interrupting circuit

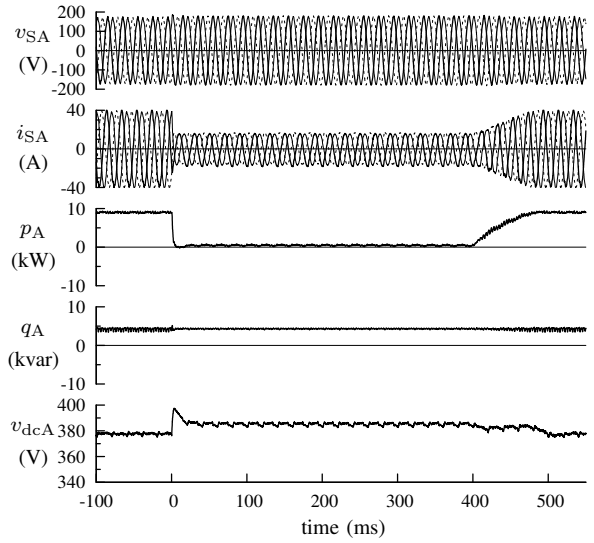


Fig. 12. Experimental waveforms of the converter A (rectifier operation) in the system with the transmission line model.

was 14.1 V, where 9.1 V at the varistor, and 2.5 V each at $\rm D_{A1}$ and $\rm D_{A2}$. Therefore, the energy absorbed in the interrupting devices was 0.42 J (= 0.030 C $\times$ 14.1 V). Theoretical energy absorbed in the dc breaker is given by W_R = 0.43 J ($= 1/2 \times$ 1.5 mH $\times$ (24 A)^2) according to (5) and it agrees with the experimental result.

B. Operation in the DC Transmission System

A transmission line was modeled by T networks and connected to the system as shown in Fig. 6 in order to verify the proposed dc transmission system. One T network is equivalent to 84 km overhead transmission line (refer to Appendix), and the two networks were connected in series to simulate a 168-km line in total. Fault point was located in the middle of the dc line. Capacitance of the dc line increases and it can enlarge its charging time when the breaker closes again. Hence, R_Q was decreased to 2.0 kΩ to finish the charging within 100 ms.

The converter A operated as a rectifier and its reference values were 9 kW for active power and 4 kvar for reactive power. The converter B operated as a inverter and maintained its dc voltage to 360 V. Its reactive power was set to -4 kvar.

Fig. 10 shows experimental waveforms of the dc breakers in the system with the transmission line model. Fig. 11 is waveforms expanded around t = 0. Small oscillation was observed in the fault current $i_{\rm fault}$ during turning off it. However, neither over-voltage nor over-current was observed and all device voltages $v_{\rm QA1}$, $v_{\rm QA2}$, $v_{\rm QB1}$, and $v_{\rm QB2}$ were properly balanced. It took 25 ms to turn off the fault current because the surge energy for demagnetizing the line inductance increased owing to the transmission line.

The energy absorbed in the breaker was roughly calculated from $i_{\rm fault}$ in Fig. 11. The total charge flowing through the interrupting circuit during the current turn-off was 0.30 C ($= 1/2 \times 24$ A $\times$ 25 ms) by approximating the waveform as a right-angled triangle. Because voltage drop in the interrupting circuit was 14.1 V, the energy absorbed in the interrupting

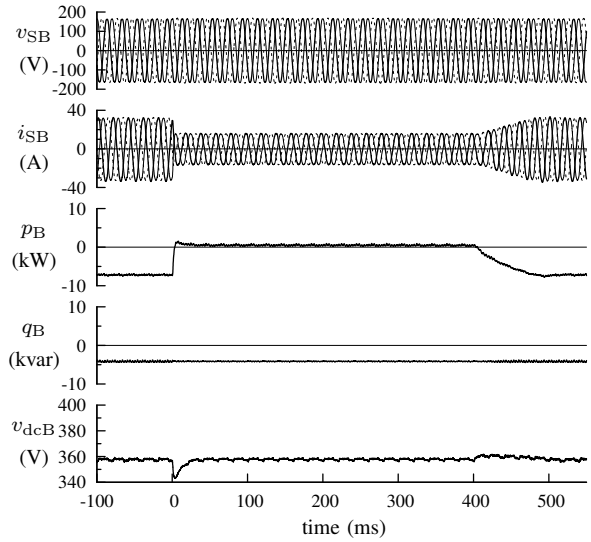


Fig. 13. Experimental waveforms of the converter B (inverter operation) in the system with the transmission line model.

devices was 4.2 J (= 0.30 C × 14.1 V). Theoretical energy absorbed in the dc breaker is given by $W_R = 4.6$ J (= $1/2 \times$ (1.5 mH + 14.4 mH) × (24 A)^2) according to (5) and it almost agrees with the experimental result.

Fig. 12 shows the waveforms of the converter A's ac voltage $v_{\rm SA}$, ac current $i_{\rm SA}$, active power $p_{\rm A}$, reactive power $q_{\rm A}$, and dc capacitor voltage $v_{\rm dcA}$. $v_{\rm dcA}$ increased after the breaker opened around $t = 0$. When it exceeded 380 V which is upper limit of the dc voltage, the converter A switched its operation to regulate the dc voltage. Then $p_{\rm A}$ decreased to zero. When the breaker closed again at t = 400 ms, the dc voltage decreased less than 380 V. Then the converter A resumed 9 kW power transfer. On the other hand, $q_{\rm A}$ was maintained to 4 kvar even during the fault. Because the dc breakers can immediately clear the dc faults, the converter can continue supplying reactive power.

Fig. 13 shows the waveforms of the converter B's ac voltage $v_{\rm SB}$, ac current $i_{\rm SB}$, active power $p_{\rm B}$, reactive power $q_{\rm B}$, and dc capacitor voltage $v_{\rm dcB}$. The converter B continued supplying reactive power $q_{\rm B}$ during the fault as well as the converter A.

VI. Conclusions

This paper proposed a circuit configuration of the dc circuit breaker for the VSC HVDC system to clear dc line faults and quickly resume power transmission. The proposed circuit realizes high blocking voltage by connecting multiple semiconductor devices in series with snubber circuits. It can also reduce the surge voltage accompanying the current clearing by using a freewheeling diode to bypass the fault current. Theoretical analysis showed the reduction of the absorbed energy in the varistor comparing to the conventional circuit without the freewheeling diode. A downscaled VSC HVDC system rated at 10 kVA in power and 360 V in dc voltage was built. The following performance was verified by the experiment: (a) dc fault clearing and rapid restoration of power transmission, (b) equal voltage balancing among series connected devices, and (c) reactive power supply during the dc fault. The proposed circuit is applicable to not only two-level and three-level converters but also modular multilevel converters which are recently put to practical use. Moreover, it is effective in multi-terminal dc transmission systems or HVDC grids because it can remove only the fault section.

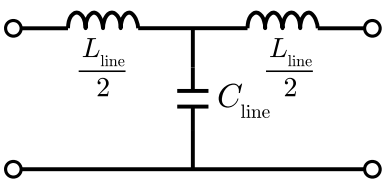


Fig. 14. A transmission line modeled by a T network.

Appendix
Modeling of Overhead Transmission Line

This section shows the derivation of parameters for a T-network transmission line model. An existing overhead dc transmission line of Hokkaido-Honshu HVDC link [28] is modeled. Rating of the line is 250 kV and 1.2 kA, the radius is $r = 16.1$ mm, and the distance between the line is $D = 14.8$. Relative permeability of the air is assumed $\mu_r = 1$. Then the inductance of the line L is theoretically modeled as follows:

$$\begin{aligned} L &= \left(\frac{\mu_r}{2} + 2\ln\frac{D}{r}\right) \times 10^{-7}\ ({\rm H/m}) \\ &= \frac{\mu_r}{20} + 0.4605\log_{10}\frac{D}{r}\ ({\rm mH/km}) \\ &= 1.41\ {\rm mH/km}. \end{aligned} \tag{13}$$

The capacitance of the line C is approximately given by

$$\begin{aligned} C &= \frac{0.02413}{\log_{10}\frac{D}{r}}\ (\mu{\rm F/km}) \\ &= 8.14\ {\rm nF/km}. \end{aligned} \tag{14}$$

These impedances are converted for the downscaled model rated at 360 V and 28 A as follows:

$$\begin{aligned} L' &= 1.41_{\rm mH/km} \cdot \frac{360_{\rm V}}{250_{\rm kV}} \cdot \frac{1.2_{\rm kA}}{28_{\rm A}} \\ &= 0.0870\ {\rm mH/km}. \end{aligned} \tag{15}$$

$$\begin{aligned} C' &= 8.14_{\rm nF/km} \cdot \frac{250_{\rm kV}}{360_{\rm V}} \cdot \frac{28_{\rm A}}{1.2_{\rm kA}} \\ &= 132\ {\rm nF/km}. \end{aligned} \tag{16}$$

Both positive line and ground line can be modeled by a T network as shown in Fig. 14. In that case, the impedances are given by

$$L_{\rm line} = 2L'. \tag{17}$$

$$C_{\rm line} = \frac{C'}{2}. \tag{18}$$

Therefore, the parameters are calculated as $L_{\rm line} = 14.6$ mH and $C_{\rm line} = 5.5$ μF for 84 km overhead transmission line. The experiment was carried out with the parameters $L_{\rm line} = 14.4$ mH and $C_{\rm line} = 5.6$ μF due to available parts.

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