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論 文 要 旨

THESIS SUMMARY

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要旨（英文 800 語程度）
Thesis Summary（approx.800 English Words ）

Computer vision has been utilized to enable many applications and will affect many aspects of human life in the era of big data. Object detection is an essential and expensive process in almost all the computer vision systems. It involves the acquisition, processing, analysis, and understanding of real-world visual information. Standard off-the-shelf embedded processors are hard to meet the trade-offs among performance, power consumption, and flexibility required by object detection applications.

The Application-Specific Instruction-set Processor (ASIP) emerges as a promising solution to balance the performance/power/flexibility trade-offs. This approach combines a software programmable processor and application-specific hardware components. The functional units of ASIPs can execute in parallel and utilize special registers for internal communication. ASIPs can offer better performance and energy characteristic than GPPs/DSPs. The control of functional units in an ASIP is not fixed but taken over by an instruction decoder and a program. ASIPs can provide higher flexibility than ASICs. However, these benefits, in turn, involve a high-cost development flow. The traditional development of ASIP is a very demanding and complex task involving instruction set, micro-architecture, RTL, compiler, and debugger design.

The motivation of this dissertation is to study an efficient ASIP design methodology and to provide a design framework to support the ASIP-based embedded vision processor design. The design framework is based on an Architecture Description Language (ADL) and provides the processor architect with a seamless design flow that covers the software interface with an open source vision library, hardware/software partition, ASIP programming model, hardware/software co-simulation and RTL implementation. Furthermore, on the basis of analyzing the vision algorithms, we provide some design considerations/guidelines to help the processor architect in designing an efficient embedded vision processor. Our thinking includes algorithms consideration, applications understanding, architecture consideration, and design reuse consideration.

To fully demonstrate the efficiency of the proposed framework and our thinking on vision processor design, we develop two ASIPs for embedded vision using the proposed framework as reference implementations. The algorithms are Haar-like features with AdaBoost classifier and Histogram of Oriented Gradients (HOG) features with Support Vector Machine (SVM) classifier. In the two ASIPs, we state the hardware/software partition principle, exploit the hardware-friendly object detection algorithms, perform the hardware/software co-design, and apply the design reusability to improve the design efficiency. The Single Instruction Multiple Data (SIMD) architecture is adopted for fully exploiting data-level parallelism inherent to the target algorithm. Multiple data reuse strategies are introduced to minimize the data movement and improve the power efficiency. Finally, the throughput, area, and power consumption estimation are carried out based on the synthesis results. The experimental results show that the ASIPs achieve 13x to 63x speed-up compared to its baseline processor. When compared with commercial GPP/DSP, the ASIPs have 7x to 113x better throughput, show 10x to 750x better area efficiency and 6x to 184 better power efficiency. Furthermore, the ASIPs show comparable performance with hard-wired designs.

備考 ： 論文要旨は、和文 2000 字と英文 300 語を 1 部ずつ提出するか、もしくは英文 800 語を 1 部提出してください。
Note : Thesis Summary should be submitted in either a copy of 2000 Japanese Characters and 300 Words (English) or 1copy of 800 Words (English).