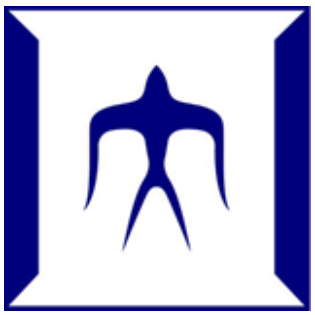
論文 / 著書情報
Article / Book Information

題目(和文)	
Title(English)	Area-Efficient High-Data-Rate Millimeter-Wave Transceivers Using CMOS Bi-Directional Amplifiers for Next-Generation Wireless Communications
著者(和文)	Pang Jian
Author(English)	Pang Jian
出典(和文)	学位:博士(学術), 学位授与機関:東京工業大学, 報告番号:甲第11238号, 授与年月日:2019年6月30日, 学位の種別:課程博士, 審査員:岡田 健一,髙木 茂孝,廣川 二郎,阪口 啓,伊藤 浩之,山尾 泰
Citation(English)	Degree:Doctor (Academic), Conferring organization: Tokyo Institute of Technology, Report number:甲第11238号, Conferred date:2019/6/30, Degree Type:Course doctor, Examiner:,,,,,
学位種別(和文)	博士論文
Type(English)	Doctoral Thesis



Area-Efficient High-Data-Rate Millimeter-Wave Transceivers Using CMOS Bi-Directional Amplifiers for Next-Generation Wireless Communications

by

Jian Pang

A Ph. D. dissertation submitted in partial satisfaction of the requirements for the degree of

Doctor of Philosophy

in

Department of Physical Electronics

in the

Graduate School of Science and Engineering

of

Tokyo Institute of Technology

Supervised by

Prof. Kenichi Okada

Spring 2019

To my family,

Acknowledgment

This thesis summarizes my research on millimeter-wave transceivers during the past five-year Ph.D. study. It is completed with the help and support from so many people. I would like to take this chance to acknowledge them for their supports throughout my entire five-year doctoral course in Tokyo Institute of Technology.

First of all, I would like to thank Prof. Kenichi Okada and Prof. Akira Matsuzawa. They gave me this important chance to join Tokyo Institute of Technology and to be a member of Matsuzawa and Okada Laboratory. During the past five years, Prof. Kenichi Okada gave me so many important advices and comments on my research. He is always pleased to spend his precious time for discussing technical issues until late at night. He guides me not only with his knowledge but also with his cautious attitude towards research. Prof. Matsuzawa always shares his thoughts with us generously, which broaden my vision. His comments on my researches and presentations are always helpful. He kindly invited all lab members to his house every year, which made my life in Japan full of fun. I would like to give my sincere thanks again to Prof. Kenichi Okada and Prof. Akira Matsuzawa.

I would like to thank Assist. Prof. Masaya Miyahara and Assist. Prof. Atsushi Shirane for their technical support. Their advice and opinions to my research are extremely valuable. Also I would like to thank Yoshino Kasuga, Makiko Tsunashima and Ayumi Okubo. Their supports on all kinds of applications are always important for my life in Tokyo Tech.

I would also like to show my gratitude to the Ph.D. committee members, Prof. Shigetaka Takagi, Prof. Jiro Hirokawa, Prof. Kei Sakaguchi, Prof. Hiroyuki Ito, and Prof. Yasushi Yamao for taking their time from their busy schedule to examine my dissertation.

I would give my sincere thanks to the senior students, Aravind Tharayil Narayanan, Dongsheng Yang, Korkut Kaan Tokgoz, Ning Li, Rui Wu, Teerachot Siriburanon, Wei Deng for all the help and support provided to me during my Ph.D. study. Without their help, I could not complete my research in Tokyo Tech.

I would like to thank my group members, Ashbir Aviat Fadila, Daiki Matsumoto, Dongwon You, Joshua Alvin, Junjun Qiu, Masaru Kawabuchi, Rattanan Saengchan, Ryo

Kunozoe, Takeshi Nakamura, Xueting Luo, Yun Wang and Zheng Li for their technical supports. Our final goal could not be achieved without our hardworking and cooperation. Also I would like to thank all the lab members for the valuable discussions.

Finally, I would like to express my deepest gratitude to my parents. They have loved me and trusted me. They always support me and take care of me when I am depressed. If it was not their understanding and help, I could not finish my study in Japan.

Abstract

The exponential growth of data traffic demands an improved data access speed in the next-generation wireless communication networks. Regarding the limited spectrum resource at the under-10-GHz band, the millimeter-wave spectrum with wide available bandwidth are ready for realizing high-speed data communication. However, designing high-data-rate millimeter-wave transceivers with suppressed power and manufacturing costs is extremely challenging considering the enlarged channel bandwidth and the increased free-space-path-loss. Thus, area-efficient millimeter-wave transceivers with optimized error vector magnitude performance are strongly demanded. This thesis presents high-performance and compact-sized millimeter-wave transceiver solutions to the next-generation local area and mobile communication networks.

During the past few years, millimeter-wave transceivers implemented in CMOS process have been deeply researched due to the high integration level and the reduced manufacturing cost. The direct-conversion architecture is also attractive due to the minimized number of building blocks. However, the LO feed through and I/Q imbalance in such transceiver architecture will potentially limit the overall EVM. Therefore, this thesis introduces a CMOS transceiver with automatically calibrated LOFT and I/Q imbalance for short-ranged local area wireless communication. With the proposed compact, low-power and high-accuracy calibration circuits, the maximum single-carrier mode data-rate of 50.1 Gb/s is realized by the calibrated transceiver in 64-QAM. Also, a 128-QAM data rate of 24.64 Gb/s is achieved with a TX-to-RX EVM of -26.1 dB. Compared with the conventional frequency-interleaving architecture and the polarized MIMO solution, the single-element transceiver implementation presented in this thesis benefits from the lower power and manufacturing costs, while maintaining an ultra-high data rate.

To further suppress the chip area considering the MIMO configuration and the beamforming implementation, this thesis also presents a CMOS two-element transceiver chip. Thanks to the bi-directional architecture, The required transceiver die area could be minimized to almost half for a decreased manufacturing cost. The proposed gain-boosted bi-directional amplifier further allows the sharing of interstage passive components. With the help of the designed PA-LNA, the required area for a single-element transceiver in

this work is 3 mm^2 including the pads. The maximum raw data rate realized by this work is 28.16 Gb/s in 16-QAM. High-data-rate solution with minimized system size and manufacturing cost is provided for the next-generation WLAN.

Wireless communication capacity improvements for the next-generation mobile communication network is also significant. This thesis introduces a four-element CMOS phased-array transceiver chip. Accurate beam control with improved steering resolution and suppressed EIRP degradation is achieved by the LO phase shifting architecture. The eight-element transceiver module in this work is capable of scanning the beam from -50° to $+50^\circ$. At a distance of 5 m, the proposed module demonstrates a maximum data rate of 15 Gb/s in 64-QAM. A data link of 6.4 Gb/s in 256-QAM is maintained within a scan angle of -50° to $+50^\circ$. High-speed and stabilized data communications could be provided within all beam scan angles.

The millimeter-wave phased-array and MIMO systems for mobile communication suffer severely from the enlarged array size. The system size, weight along with the manufacturing cost are significantly increased. Thus, this thesis presents a CMOS 4H+4V bi-directional beamformer chip supporting DP-MIMO. The proposed neutralized bi-directional amplifier significantly reduces the required on-chip area. An active bi-directional vector-summing phase shifter is also introduced for improving the phase shifting resolution and suppressing the power and area consumptions. In a 1-m OTA measurement, a 4×4 sub-array module supports single-carrier data-rates of 15 Gb/s and 6.4 Gb/s per polarization in 64-QAM and 256-QAM, respectively. 2×2 DP-MIMO communication with a 400-MHz channel bandwidth is also achieved with a 64-QAM EVM of 4.9%. Thanks to the proposed bi-directional architecture, the required on-chip area for a single-element beamformer is less than 0.6 mm^2. Reduced manufacturing cost and compact system size could be maintained with high data rate.

Contents

List of Figures

List of Tables

Chapter 1

Introduction

Significant evolutions of wireless communication technologies have been experienced by us during the past few years. Newly introduced applications such as AR/VR applications and high definition movie streaming have come though to us and providing us with exciting experiences. Along with the applications, continuous growth on the number of wireless-connected devices has been observed during the past few years and the speed will become even faster in the future. Regarding the outgrowth of wireless devices, the wireless data traffic will also keep increasing exponentially, as predicted in Fig. 1.1 [1]. Therefore, large wireless throughput with low communication latency should be provided

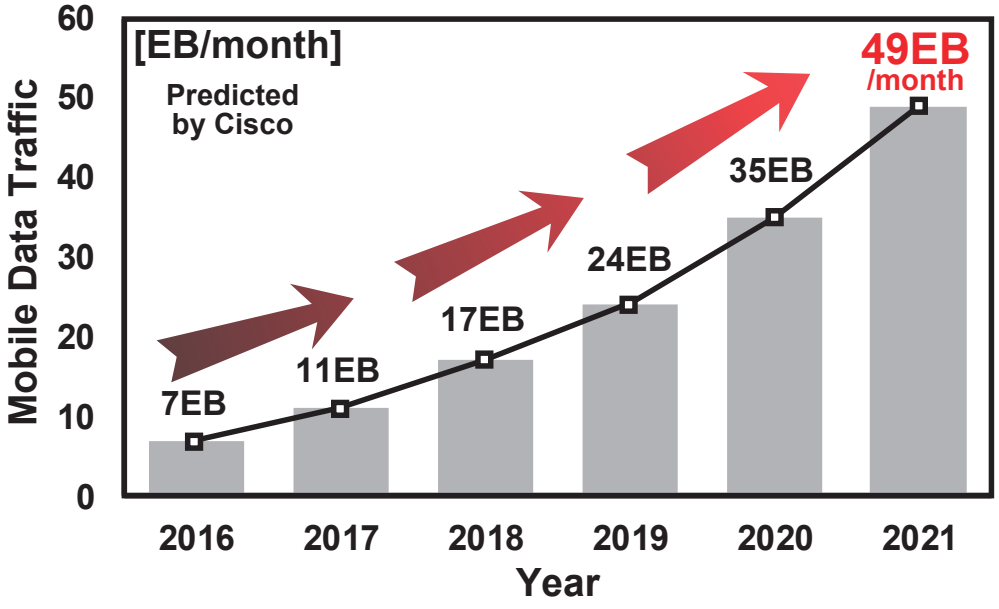


Figure 1.1: Mobile data traffic growth prediction by Cisco.

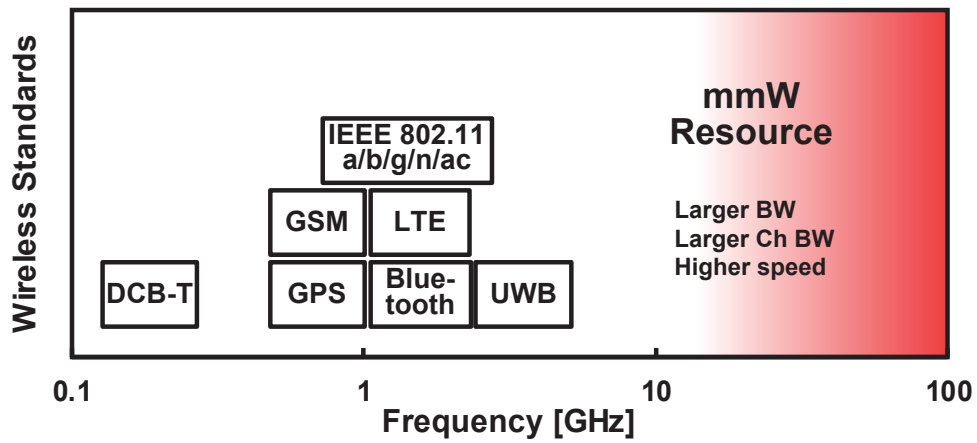


Figure 1.2: Applications at the low frequency band.

by the next-generation wireless communication systems. While, a suppressed manufacturing cost should be kept considering the numerous number of connected devices. Wireless transceivers satisfying the mentioned key characteristics are required to be developed and implemented.

Fig. 1.2 shows the under-10-GHz spetrum. Various applications located at this frequency makes the under-10-GHz spectrum extremely crowed. The limited achievable bandwidth at this frequency therefore can hardly be utilized for multi-Gb/s wireless communication. While, different with the under-10-GHz band, the millimeter-wave spectrum with much wider available bandwidth is one of the most promising candidates for realizing the next-generation wireless communication. The spectrum allocation of the incoming 5th generation mobile network is shown in Fig. 1.3 for explaining the available frequency resource in millimeter-wave band. A four-times-larger maximum channel bandwidth could be utilized in the frequency range 2 (FR2, millimeter-wave band) than the counterpart in frequency range 1 (FR1, under-6-GHz band). The wireless communication capacity could be boosted into the multi-Gb/s region with the millimeter-wave spectrum.

Moreover, developments in complementary metal-oxide-semiconductor (CMOS) processes have been taken place during the past few years. CMOS implementations of millimeter-wave transceivers with high integration level and low manufacturing cost have been introduced for the wireless local area network (WLAN) applications and the mobile communication applications [2–24].

	Band	Frequency Range	Bandwidth	Ch. BW.
FR1	71	617 MHz – 698 MHz	81 MHz	5 MHz ~ 100 MHz
	44	703 MHz – 803 MHz	100 MHz	
	66	1710 – 1780 and 2110 - 2200 MHz	100 MHz	
	40	2300 MHz – 2400 MHz	100 MHz	
	41	2496 MHz – 2690 MHz	194 MHz	
	42	3400 MHz – 3600 MHz	200 MHz	
	43	3600 MHz – 3800 MHz	200 MHz	
	C-band	4400 MHz – 4499 MHz	590 MHz	
FR2	n258	24.25 GHz – 27.50 GHz	3.25 GHz	50 MHz ~ 400 MHz
	n257	26.50 GHz – 29.50 GHz	3.00 GHz	
	n260	37.00 GHz – 38.60 GHz	1.00 GHz	
	n260	38.00 GHz – 40.00 GHz	2.00 GHz	

Figure 1.3: Frequency bands for the incoming 5G.

1.1 Standards and Regulations for Millimeter-Wave Band

The utilization of millimeter-wave spectrum could significantly boosts the achievable data rate. Efforts on establishing the standards and regulations for both WLAN and mobile communication network have been concentrated during the past few years.

Among the millimeter-wave spectrum, the 60-GHz band featuring 14-GHz unlicensed bandwidth has attracted people's attention for ultra-high-speed WLAN applications. Early in 2001, the Federal Communications Commission (FCC) allowed the unlicensed usage of 9-GHz bandwidth (57 GHz to 66 GHz) in 60-GHz band for wireless communication [25]. The available bandwidth is further extended to 14 GHz in 2016 (57 GHz to 71 GHz). Nowadays, the 60-GHz band has been regulated in various counties around the world including USA, Japan, China and Australia. Several standards for commercialization have been established for this band.

Within the 60-GHz standards, IEEE 802.11ad/WiGig is one of the most promising standards targeting multi-Gb/s short-ranged and middle-ranged wireless communications. Fig. 1.4 shows the channel allocation defined in IEEE 802.11ad/WiGig. With the 2.16-GHz channels in 60-GHz band, up to 7 Gb/s wireless data communication has already been realized through the devices such as wireless docking stations and WiFi routers. However, as mentioned in the previous section, the exponential growth of data traffic still demands a much higher wireless communication speed in the not far future. To satisfy the future data transmission capacity, IEEE 802.11ay is the standard to additionally extend

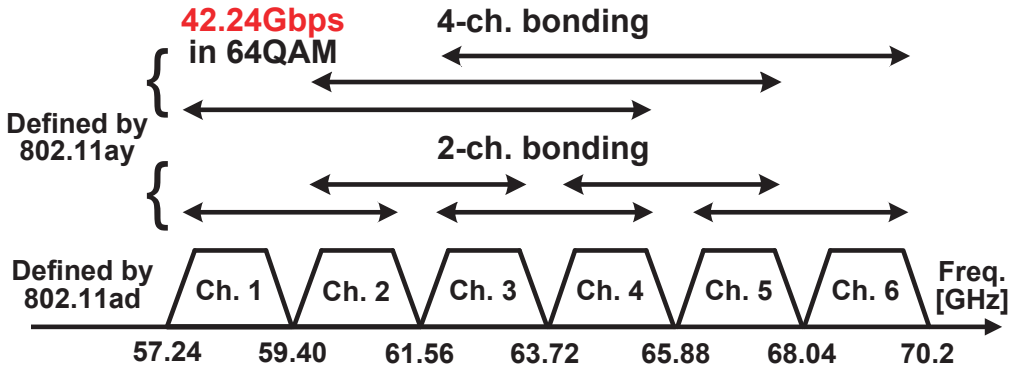


Figure 1.4: Channels defined by IEEE 802.11ad/WiGig and IEEE 802.11ay.

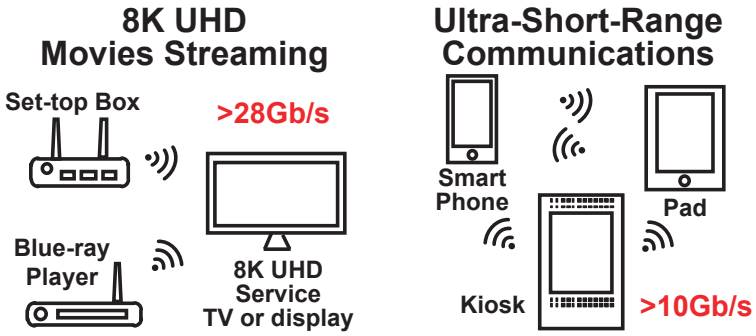


Figure 1.5: Usage scenarios for middle-ranged and short-ranged wireless communications.

the data-rate to over 28 Gb/s. Fig. 1.4 also summarizes the channels defined in IEEE 802.11ay. Basically, the wireless data capacity evolution is taken place in three directions: wider bandwidth, high-order modulation schemes, and spatial multiplexing. Fist of all, the channel bonding technique will be applied to broaden the available signal bandwidth in IEEE 802.11ay. A raw data rate of 42.24 Gb/s could be realized considering 64-QAM 4-channel bonding. Besides the channel-bonding technique, a higher order modulation scheme such as 128 QAM is always desirable to further increase the spectrum efficiency. Last but not least, the multiple-in-multiple-out (MIMO) technique will also be utilized for improving the wireless throughput with additional data streams.

In summary, IEEE 802.11ay using the 60-GHz band is ready to extend the WLAN capacity to over 20 Gb/s. Short-ranged and middle-ranged applications such as ultra-short-range (USR) communications and 8K ultra-high-definition (UHD) movies streaming shown in Fig. 1.5 will be supported in the not future.

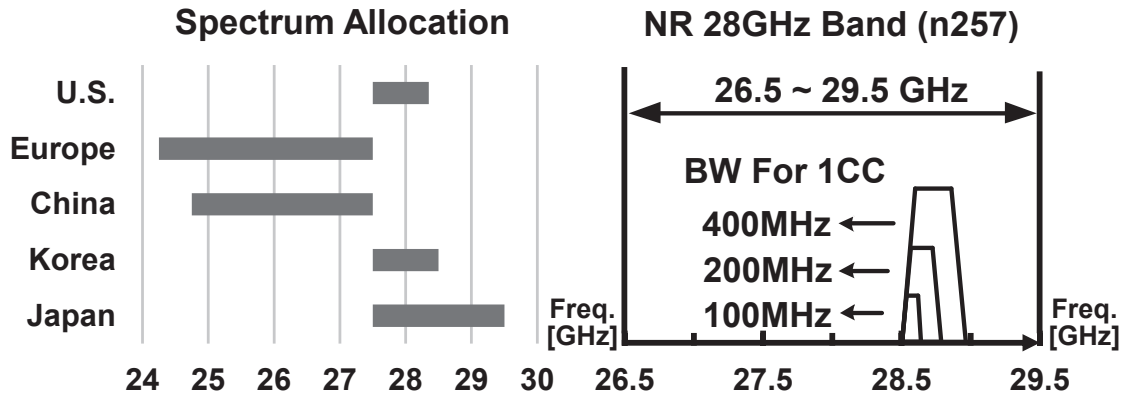


Figure 1.6: (a) 28-GHz spectrum allocation for 5G usage in various countries and (b) 5G NR band n257.

Evolutions of data access speed will also occur in the long-ranged mobile communication networks. The incoming 5G new radio (NR) regulated by the 3rd Generation Partnership Project (3GPP) utilizes the millimeter-wave spectrum to provide high-throughput and low-latency experiences. As already mentioned in the previous section, the newly regulated frequency bands in FR2 feature a lager total available bandwidth and a wider channel bandwidth. The mobile communication capacity could be significantly improved with the 400-MHz maximum channel bandwidth and the orthogonal frequency-division multiplexing (OFDM) technique. Within the FR2, attentions have been focused on the 28-GHz band due to its availability in various countries (Fig. 1.6). The beamforming technique based on the phased-array implementation and the MIMO technique in 5G NR are going to deliver multiple streams with several-Gb/s data rate over a long communication distance.

1.2 CMOS Millimeter-Wave Transceivers

Benefits have been brought to the millimeter-wave wireless transceivers by the fast-evolving CMOS technology. The compound semiconductors are utilized in the past for the millimeter-wave transceiver design due to the devices with high operating frequency. However, such transceiver systems consisting of compound semiconductor components suffer from limited integration level, expensive manufacturing cost and additional packaging cost. Fig. 1.7 demonstrates the roadmap for CMOS technology according to the 2013 International Technology Roadmap for Semiconductors [26]. The improving maximum oscillation frequency ($f_{\max}$) of the transistors in CMOS process against the gate length enables the

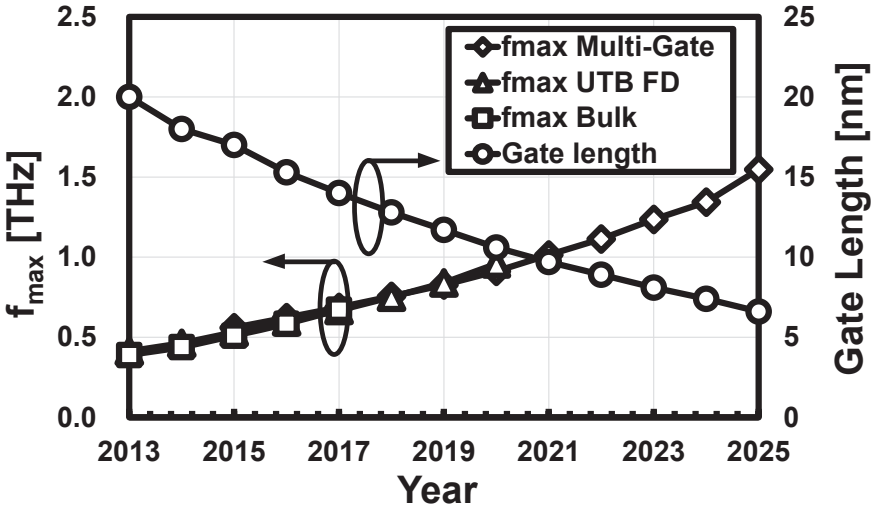


Figure 1.7: Roadmap for CMOS transistors gate length, maximum oscillation frequency (f_{max}) based on ITRS 2013.

transceiver front-end design at the millimeter-wave region. Highly integrated millimeter-wave transceiver systems including the RF front-end, analog baseband and digital baseband circuits could be realized for an minimized manufacturing and packaging costs [10–12].

1.3 Overview of the Thesis

This thesis is developed to present the millimeter-wave transceivers designed for the next-generation wireless communication. In order to achieve high data rate, key ideas are introduced for optimizing the system performance. Moreover, to suppress the manufacturing cost regarding the massive production, the process-level, transceiver-architecture-level, and circuit-level considerations are included in the design progress. Reduced on-chip area and a compact system could be achieved while maintaining a high data rate. The wireless capacity in both the next-generation WLAN and the next-generation mobile network could be significantly improved with minimized costs.

Fig. 1.8 shows the chapter organization of this thesis. Chapter 2 introduces the detailed design parameters for millimeter-wave transceivers. Design challenges for millimeter-wave transceivers are also concluded in Chapter 2. Transceivers introduced in Chapter 3 and Chapter 4 targets the short-range and middle-range scenarios in WLAN, while transceivers in Chapter 5 and Chapter 6 are designed for the long-range communications in mobile network.

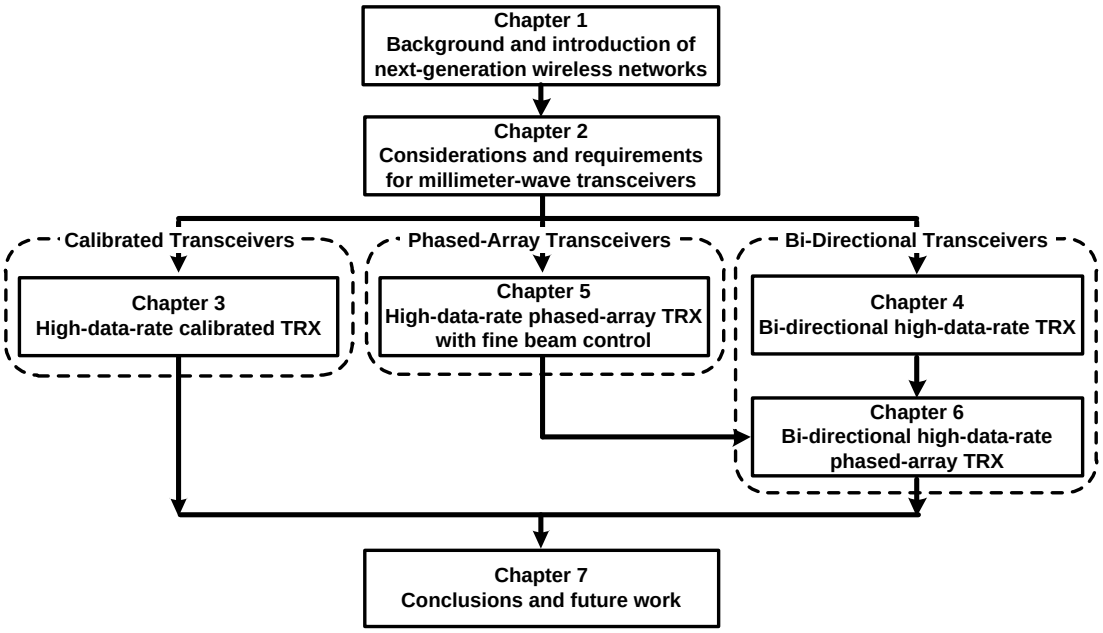


Figure 1.8: Organization of this thesis.

Chapter 3 presents an LOFT and IMRR calibrated transceiver. A compact, accurate and low-power calibration block is introduced in this chapter. Chapter 4 demonstrates an area-efficient transceiver. A bi-directional technique is proposed with compensated RF path gain. Chapter 5 introduces a phased-array transceiver with accurate beam control. Suppressed gain and phase errors could be realized with the LO phase shifting architecture. Chapter 6 shows an area-efficient phased-array transceiver supporting dual-polarized MIMO. A neutralized bi-directional technique is adopted for an improved gain characteristic and an optimized stability.

Finally, this thesis is concluded in Chapter 7. Several future directions are also introduced in Chapter 7.

Chapter 2

Challenges for Millimeter-Wave Transceivers

With respect to the limited spectrum resource at the low frequency band, the millimeter-wave spectrum with wider available bandwidth will be utilized for the next-generation WLAN and mobile communication network. The much wider channel bandwidth and the complex modulation schemes help to improve the wireless communication capacity. However, to realize a high-performance millimeter-wave transceiver within a limited power and manufacturing costs, various design issues are still required to be addressed. This chapter will introduce the design challenges and the corresponding considerations for a millimeter-wave transceiver.

2.1 Error Vector Magnitude

Considerable spectrum resource could be utilized in the millimeter-wave band for improving the wireless capacity. The complex modulation schemes with higher order such as 64-QAM and 128-QAM will also be employed. However, small enough error vector magnitude (EVM) should be maintained from the transmitter to the receiver for such modulation schemes after the demodulation. Thus, improving the system EVM is one of the most important design challenges for the millimeter-wave transceivers. Basically, increasing the modulation order requires an improvement to the system EVM. Fig. 2.1 shows the EVM requirement against the bit error rate (BER) regarding different modulation schemes. To realize a BER of 10^{-3}, EVMs of -22.5 dB, -25.5 dB and -28.4 dB are required for 64-QAM, 128-QAM and 256-QAM, respectively, through the transmitter to the receiver. The transceiver design progress becomes extremely challenging regarding the limited power and cost budgets. During the recent years, the direct-conversion archi-

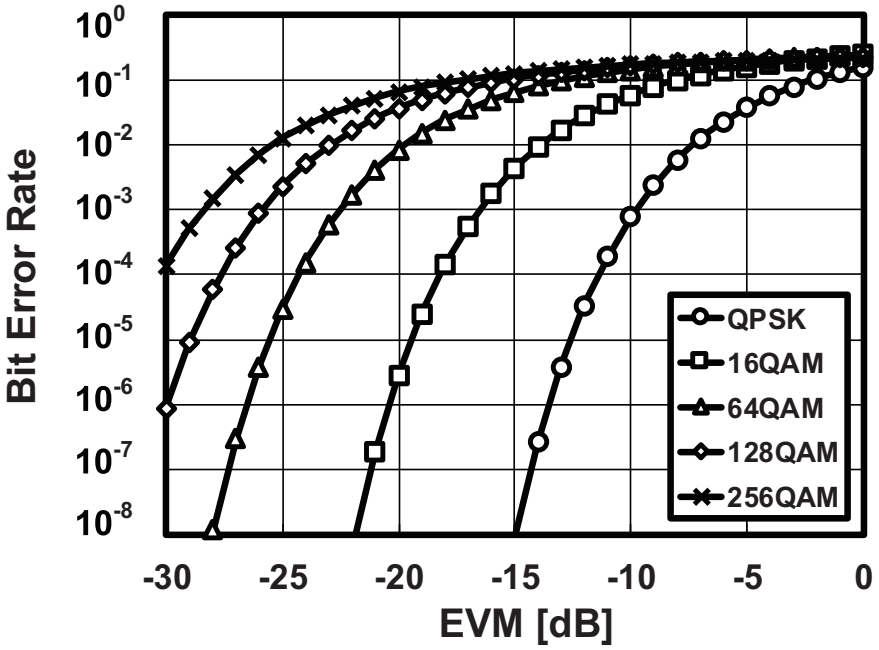


Figure 2.1: Required EVM against BER with different modulation schemes.

tecture is widely adopted for the millimeter-wave transceivers [10, 13, 15, 23, 27–30]. The reduced number of building blocks due to the system simplicity helps to achieve a compact and low-power system. To look into the detailed transceiver design parameters, the following equation could be utilized to represent the EVM of a direct-conversion transceiver $\mathrm{EVM_{TRX}}$ [31]:

$$\mathrm{EVM_{TRX}} \approx \sqrt{\frac{1}{\mathrm{SNDR}^2} + {\varphi^2}_{\mathrm{RMS}} + \mathrm{EVM^2_{LOFT}} + \mathrm{EVM^2_{Image}} + \mathrm{EVM^2_{Flat}}} \tag{2.1}$$

where SNDR represents the signal-to-noise and distortion ratio, ${\varphi^2}_{\mathrm{RMS}}$ stands for the integrated double-sideband (DSB) phase noise of the carrier. $\mathrm{EVM_{LOFT}}$, $\mathrm{EVM_{Image}}$ and $\mathrm{EVM_{Flat}}$ denote the EVMs caused by the LOFT, the I/Q imbalance and the in-band gain response variation.

System SNDR optimization is very important to millimeter-wave transceivers. The much wider channel bandwidth significantly increases the input noise floor. If we take the 5G NR application mentioned in Chapter 1 for example, an 6-dB noise floor increasement could be calculated regarding the 100-MHz channel bandwidth in FR1 and the 400-MHz channel bandwidth in FR2. As a result, to maintain enough transceiver EVM, careful design considerations and evaluations will be required for the gain level, linearity and noise figure.

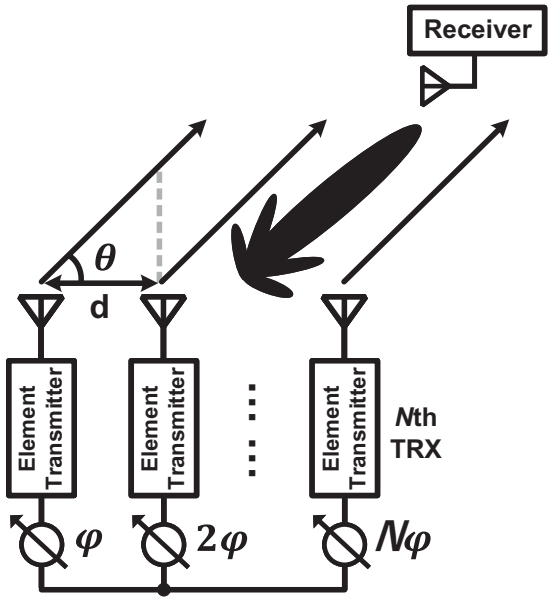


Figure 2.2: Beamforming Technique.

Moreover, the increased requirement on EVM will demand a lower phase noise of the RF phase-locked loop (PLL). Usually, the usage of baseband carrier tracking circuit can suppress the influence of phase noise. However, for OFDM-mode data transmission, the carrier tracking bandwidth will be limited by the sub-carrier spacing. Therefore, stringent phase noise requirements are still need to be satisfied. While on the other hand, the phase noise requirement for single-carrier (SC) mode data transmission can be relaxed due to the wider carrier tracking bandwidth.

Additionally, for transceivers based on the direct-conversion architecture, the LO feedthrough (LOFT) from the mixer mismatch and the image signal from the I/Q imbalance will fall inside the operating bandwidth. The system EVM performance will be potentially degraded. Regarding the complex modulation schemes, special attentions should be paid to the LOFT and I/Q imbalance cancellation regarding the modulation schemes.

2.2 Communication Distance Extension

Link budget estimation is usually necessary for wireless data communications. As mentioned in the previous section, enough EVM should be maintained after the path loss from the transmitter side to the receiver side. It is well-known, the free-space-path-loss (FSPL)

could be represented with the following equation:

$$\text{FSPL} = 20\log(\frac{4\pi Df}{c}) \tag{2.2}$$

In the equation, D, f and c are the communication distance, signal frequency and speed of light, respectively. Against the increasing frequency, rapid growth in FSPL will be induced to the millimeter-wave spectrum. Sequently, beamforming technique for extending the communication distance will be significantly important for middle-ranged and long-ranged wireless applications such as mobile data transmission. As shown in Fig. 2.2, by implementing couples of element-transmitters with different phase shifting, the radiated signal will be added in phase at the receiver antenna. Regarding a certain beam direction θ, the required phase shifting φ between different element-transmitters for a half-wavelength-spaced linear array could be expressed with the following equation:

$$\varphi = k_{\text{f}} d \sin\theta \tag{2.3}$$

where k_{f} represents the propagation constant for frequency f. Due to the in-phase magnitudes added at the receiver input, additional array gain could be provided by the transmitter array. For a N_{TX}-element linear array, the array gain G_{TXarray} could be calculated with $20\log N_{\text{TX}}$.

Similar to the transmitter array, multiple receivers can also be configured into the receiver array for an improved receiving signal level. The received signals from different element-receivers will be added at the combine point in amplitude, which results in a $20\log N_{\text{RX}}$ receiving power improvement. However, different from the transmitter array, the received noise floor from different element-receiver will also be added at the combine point. As a result, when the input noise from different element-receivers are not co-related with each other, an SNR improvement of $G_{\text{RXarray}} = 10\log N_{\text{RX}}$ could be achieved by a N_{RX}-element receiver array.

From the analysis mentioned above, the array size requirement for covering a certain communication distance D with the beamforming technique could be derived. Regarding a certain modulation scheme, the following equation should be satisfied:

$$\begin{aligned} &P_{\text{out}}(\text{dBm}) + G_{\text{TXant}}(\text{dB}) + G_{\text{TXarray}}(\text{dB}) + G_{\text{RXarray}}(\text{dB}) + G_{\text{RXant}}(\text{dB}) \\ &- FSPL(\text{dB}) - NoiseFloor(\text{dBm}) > SNR_{\text{Required}}(\text{dB}) \end{aligned} \tag{2.4}$$

In the equation, P_{out} is the output power for the element-transmitter. Appropriate power back-off regarding the required EVM for a certain modulation scheme should be included in P_{out}. G_{TXant} and G_{RXant} are the antenna gains for transmitter and receiver including

		IEEE 802.11ad	IEEE 802.11ay	
Standard	Channel Bandwidth	2.16GHz	1-ch.: 2.16GHz 2-bonded ch.: 4.32GHz 4-bonded ch.: 8.64GHz	
	Modulation (SC)	16QAM (MCS20)	64QAM* (MCS17)	128QAM*
	TX EVM (SC)	-19.0dB	-24.0dB*	-*
Design Target	TX-to-RX EVM (SC)**	-16.5dB	-22.5dB	-25.5dB
	LOFT Supp.	-26.5dB	-32.5dB	-35.5dB
	IMRR	-26.5dB F_{BB}< 0.88GHz	-32.5dB F_{BB}<0.88GHz(1-ch.) F_{BB}<1.76GHz(2-ch.) F_{BB}<3.52GHz(4-ch.)	-35.5dB F_{BB}<0.88GHz(1-ch.) F_{BB}<1.76GHz(2-ch.) F_{BB}<3.52GHz(4-ch.)
	I/Q Mag. Mismatch	< 0.8dB	< 0.4dB	< 0.3dB
	I/Q Phase Mismatch	< 5°	< 3°	< 2°
	Phase Noise (OFDM)	16QAM: -90dBc/Hz @1MHz	64QAM: -96 dBc/Hz@1MHz 128QAM: -99 dBc/Hz@1MHz	

* Modulation schemes and required EVMs for IEEE 802.11ay are still under discussion
** TX-to-RX EVM is defined with BER of 10^{-3} and is equal to –SNR (MER).

Figure 2.3: Summary of requirement and design target for IEEE 802.11ad/ay

the implementation loss. The *NoiseFloor* in the equation represents the input noise floor for the receiver. It can be found from the equation that the term in the left-hand side is the receiving SNR level. To successfully maintain the data communication, the receiving SNR level should be larger than the required receiver SNR level. Therefore, appropriate array sizes could be estimated based on the above analysis.

Besides the array size, other factors such as receiver linearity, transmitter power-added efficiency, on-chip area and antenna sharing should also be taken into consideration for a high-performance, low-cost and compact phased-array system. Also, regarding the specific applications, the transceiver system requirements can be quite different due to the different usage scenarios. The remaining part of this chapter will introduce the specific design challenges for the next-generation WLAN standard IEEE 802.11ay and the next-generation mobile network 5G NR.

2.3 Challenges for IEEE 802.11ay Transceivers

As introduced in Chapter 1, IEEE 802.11ay features a maximum channel bandwidth of 2.16 GHz. With the channel bonding technique, a maximum channel-bonding bandwidth of 8.64 GHz could be available. Several important usage scenarios for the IEEE 802.11ay standard include the USR data transfer, 8K UHD movies streaming and data center 11ay inter-rack connectivity. As mentioned in the previous section, design considerations for optimizing the system EVM regarding a wider channel bandwidth and a higher modulation scheme will be critical for realizing high data rate. Also an area- and power-efficient design is always demanded by commercial usages.

Fig. 2.3 summarizes the requirements from the IEEE 802.11ad/ay and the design targets. Due to the different modulation schemes and different channel bandwidths defined in IEEE 802.11ad and IEEE 802.11ay, the system requirements will also be different for these two standards. As mentioned previously, higher order modulation schemes basically demand higher EVMs. For streaming the data with modulation schemes of 64-QAM or 128-QAM regarding a BER of 10^{-3}, TX-to-RX EVMs of -22.5 dB and -25.5 dB will be required to be maintained. In this condition, the 2.16-GHz channel bandwidth in IEEE 802.11ad results in a much higher noise floor. Regarding the bonded channels in IEEE 802.11ay, the input noise level for an IEEE 802.11ay application can be even 6 dB higher than an IEEE 802.11ad one. Thus, the SNDR optimization of a transceiver becomes essential within a limited power budget.

Additionally, the increased bandwidth also puts more pressures on the gain flatness of a single-carrier transceiver. A 2.8-dB gain variation within the 8.64-GHz bandwidth can lead to a -16.5-dB EVM_{Flat} [31], which severely limits the overall EVM. Although the utilization of an equalizer at the receiver side can minimize the gain variation, a flat frequency response is still desirable for a wide-band transceiver.

Moreover, a minimized phase noise performance of the PLL is also required for supporting the OFDM mode communication. With a 400-kHz carrier tracking bandwidth, the phase noises of -96 dBc/Hz and -99 dBc/Hz at 1-MHz offset will be required for 64 QAM and 128 QAM, respectively [32].

2.3.1 LOFT and I/Q Imbalance Cancellation

As mentioned in the previous section, direct-conversion transceivers suffer terribly from the LOFT and I/Q imbalance. Thus, to improve the yields, an on-chip calibration block for LOFT suppression and image rejection ratio (IMRR) is usually essential [10, 33]. [10] introduces a transceiver chipset developed for IEEE 802.11ad with a built-in self-calibration circuit. The LOFT suppression and IMRR in [10] are calibrated by reusing the

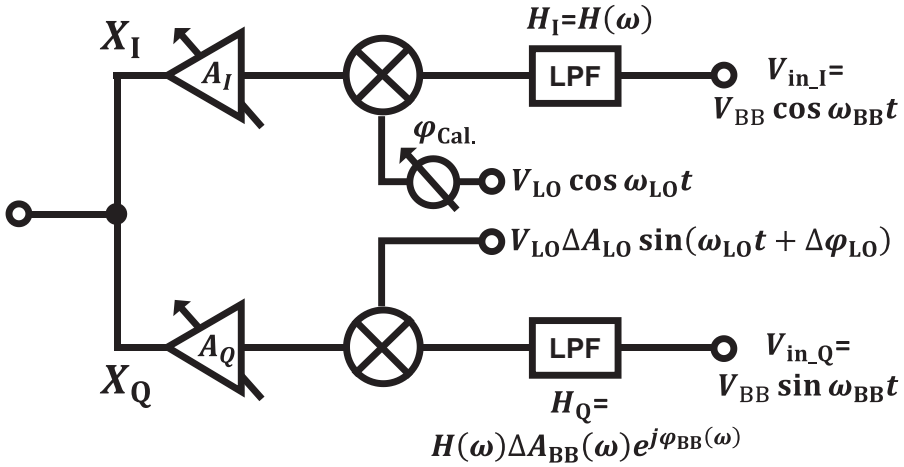


Figure 2.4: I/Q imbalance and RF domain compensation for direct-conversion transceiver.

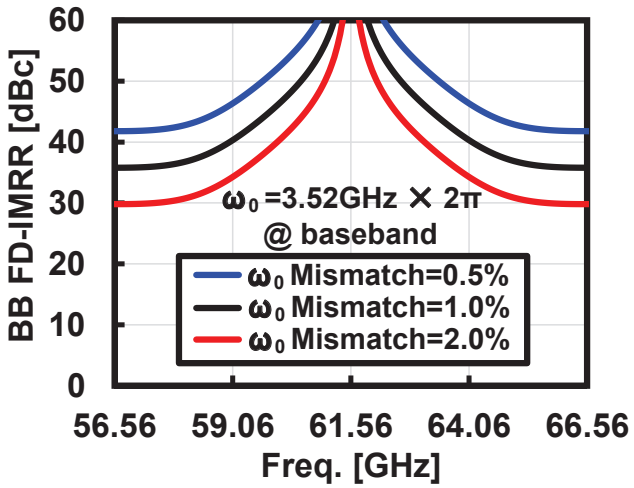


Figure 2.5: Simulated frequency-dependent IMRR with different I/Q cut-off frequency mismatch.

5-bit 3.52 GS/s baseband ADCs. However, the IEEE 802.11ay standard demands a much more rigorous level for the in-band LOFT suppression and IMRR. Whereas, applying the same calibration method to an IEEE 802.11ay transceiver will result in severe inaccuracy and even higher power consumption. Therefore, calibration circuits designed for IEEE 802.11ay demands an accuracy improvement along with a small enough power and area overhead.

Regarding the specific requirements from Fig. 2.3, both the LOFT suppression and the IMRR after calibration should be higher than 32.5 dB for 64-QAM and 35.5 dB for 128-QAM within the signal bandwidth. Due to the fixed frequency of the LOFT, im-

provements for LOFT suppression could be achieved by increasing the resolution of the detection circuits and the tuning circuits. Although, the suppressed LOFT will be degraded over the temperature variation, methods such as background calibration could be introduced for addressing this issue. While, regarding the I/Q imbalance cancellation, more design considerations are required. According to Fig. 2.3, the I/Q magnitude mismatches of less than 0.4 dB and 0.3 dB along with the I/Q phase mismatches of less than 3° and 2° are required for 64-QAM and 128-QAM, respectively. Circuits supporting such high-resolution magnitude and phase tuning will be required to compensate the I/Q imbalance. Usually, the I/Q imbalance of a receiver can be compensated by the digital signal processing (DSP) circuit [34, 35], while for the transmitter, a standalone block for detection and calibration is required. For saving power, an RF domain calibration is usually adopted to calibrate the I/Q imbalance [13]. Fig. 2.4 shows the I/Q imbalance in a transceiver and the corresponding RF domain compensation. From Fig. 2.4, the IMRR can be calculated by comparing the magnitudes of the $(\omega_{LO} - \omega_{BB})$ and $(\omega_{LO} + \omega_{BB})$ components:

$$|IMRR| = \left| \frac{A_I^2 + \Delta A^2 A_Q^2 + 2\Delta A A_I A_Q \cos(\Delta\varphi - \Delta\varphi_{cal})}{A_I^2 + \Delta A^2 A_Q^2 - 2\Delta A A_I A_Q \cos(\Delta\varphi - \Delta\varphi_{cal})} \right| \tag{2.5}$$

In the equation, $\Delta A(\omega) = \Delta A_{LO}\Delta A_{BB}(\omega)$ is the I/Q magnitude mismatch from the baseband and the LO. While, $\Delta\varphi(\omega) = \Delta\varphi_{LO} + \Delta\varphi_{BB}(\omega)$ is the I/Q phase mismatch. A_I, A_Q and $\Delta\varphi_{cal}$ represent the magnitude and phase calibration parameters from the calibration circuit. By selecting the A_I, A_Q and φ_{cal} properly, the I/Q imbalance can be compensated at an RF frequency of $(\omega_{LO} - \omega_{BB})$. However, the calibrated IMRR will degrade rapidly when approaching the pass-band edge of the baseband LPF. The main reason for the degradation is because of the frequency-dependent I/Q imbalance caused by the mismatch between an I path LPF and a Q path LPF [36]. Fig. 2.5 demonstrates the simulated frequency-dependent IMRR (FD-IMRR) with a mismatched cut-off frequency ω_0 between the I and Q path LPFs. Regarding the degraded IMRR from the baseband, even more margins should be included in an RF domain calibration circuit. A larger than 50-dBc detection accuracy will be required for achieving 64-QAM and 128-QAM, which corresponding to a more than 50-dBc detection path sensitivity and a more than 9-bit detection ADC. Fig. 2.5 also implies that the calibration frequency for an RF domain compensation should be selected near the carrier frequency because of the low enough influence from the baseband frequency-dependent I/Q imbalance there. Usually, the cut-off frequency ω_0 mismatch will depend on the layout. Regarding a severe ω_0 mismatch, the overall EVM will be influenced by the image signal. I/Q compensation techniques [37] at the baseband should be considered.

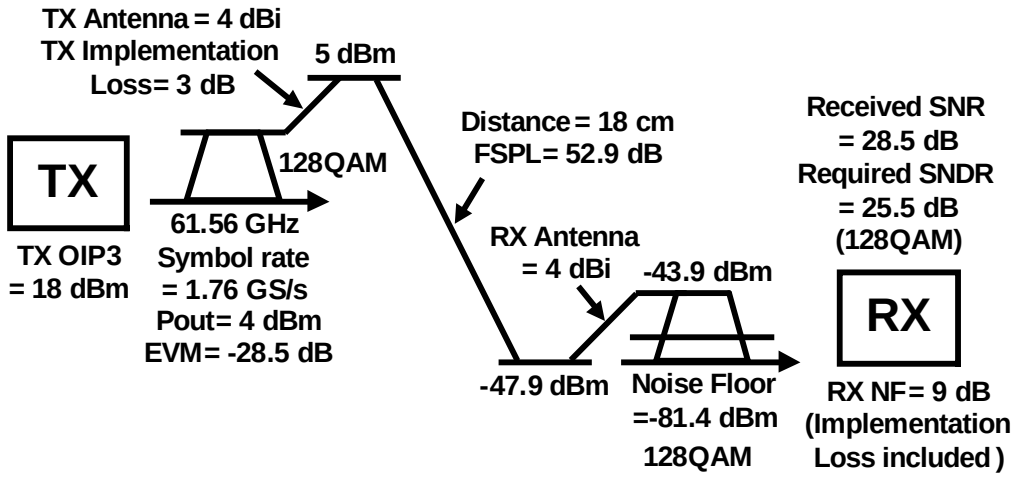


Figure 2.6: Link budget for a data transmission in 128-QAM.

2.3.2 Manufacturing Cost

Besides the system EVM, a compact system size, weight and a suppressed manufacturing cost are always desirable considering the massive production. For short-ranged usage scenarios such as USR communications, the system size and on-chip area requirements could be relaxed due to the limited number of the required element-transceivers. Fig. 2.6 shows a link budget example for the USR data transfer. A CMOS transmitter output power of 4 dBm is assumed in this estimation. The modulation scheme is set to be 128-QAM. After receiving the signal, still 3-dB SNDR margin is remained for the down-conversion and demodulation. A data communication in 128-QAM with a 1-channel bandwidth can be supported in a maximum communication distance of 18 cm. To establish a data link within such a short distance, a single-element transceiver implementation is already enough.

While, considering applications such as streaming the 8K UHD movies, the communication distance needs to be extended. Regarding the increased FSPL of the 60-GHz spectrum, the phased-array transceiver implementation is required. Moreover, for maintaining a high data rate after extending the communication distance, MIMO technique is also one of the most critical techniques for the IEEE 802.11ay. Fig. 2.7 shows the link budget estimation for the usage scenario mentioned above. The communication distance is estimated to be 5 m in consideration of streaming the movie at home. To cover the distance, an array size of 16 is selected for both the transmitter and receiver arrays. A 2×2 MIMO configuration is applied to boost the data rate. The modulation scheme is 16-QAM (MCS12). With the coding rate of 0.5, a data rate of 28.16 Gb/s could be estimated with a four-bonded channel. After the receiving, larger than 21-dB signal-to-

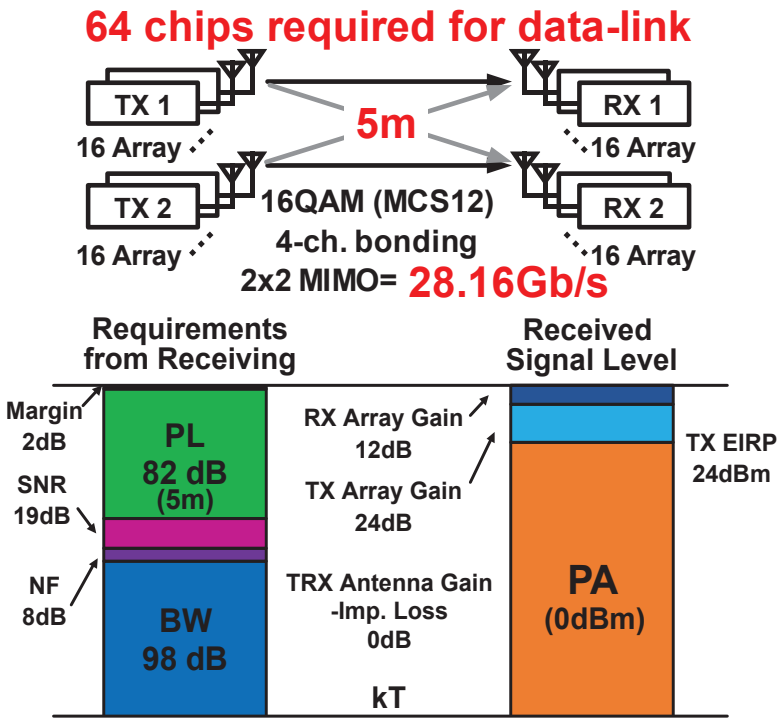


Figure 2.7: Link budget example for streaming 8K UHD movies.

noise ratio (SNR) including the margin can still be maintained for the down-conversion and the demodulation. However, for supporting such a data link, the required number of element-transceivers is doubled due to the 2×2 MIMO configuration. Totally 32 element-transceivers and 64 antennas will be required when there is no TRX switches. As a result, an area-efficient transceiver design along with a compact antenna sharing solution will be extremely necessary for the future WLAN.

2.4 Challenges for 5G NR Phased-Array Transceivers

Significantly improved mobile data access speed will be provided by the incoming 5G. Similar to the WLAN communication, the millimeter-wave spectrum also plays an important role in the future 5G. Techniques such as beamforming, MIMO will be applied for extending the mobile communication capacity to over 10 Gb/s.

However, realizing a 5G millimeter-wave phased-array transceiver also need to address various issues. Firstly, due to the enlarged FSPL, a larger array size will be demanded for covering a long communication distance. Therefore, maintaining a stabilized and high-speed data link within 360° beam angle becomes challenging due to the narrower

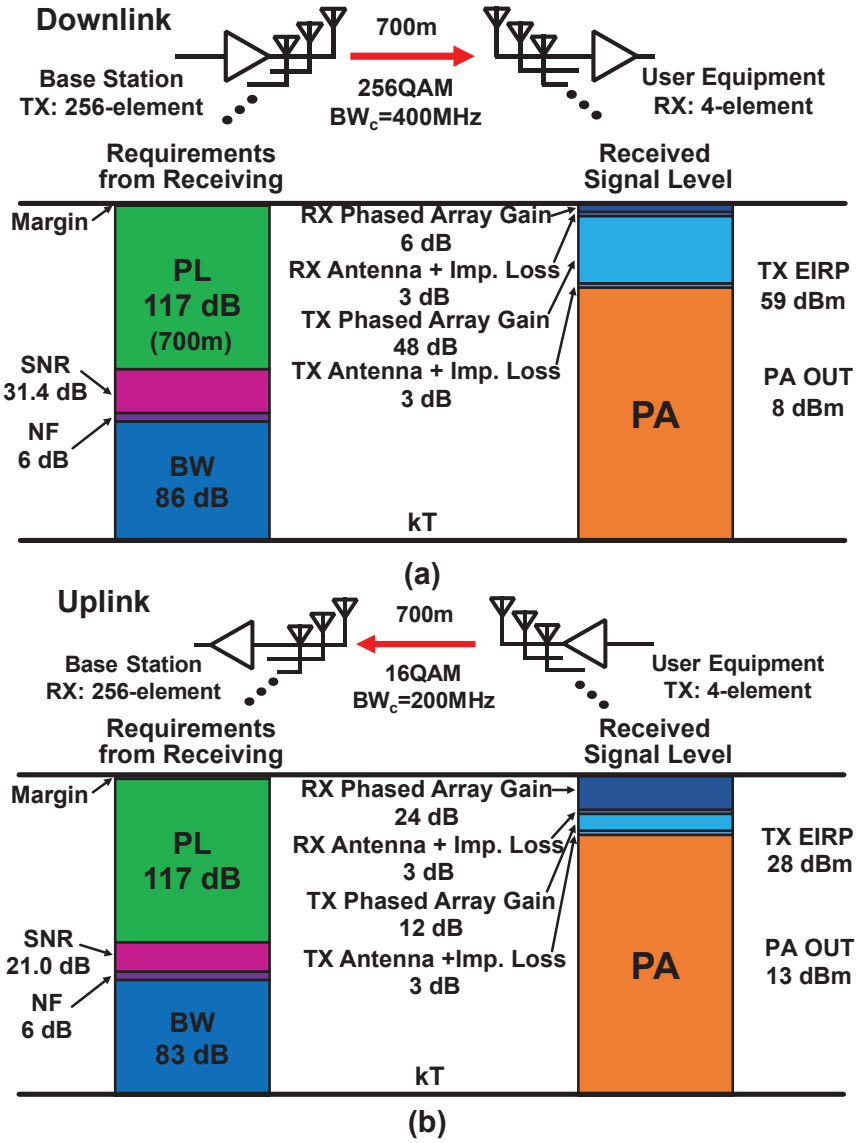


Figure 2.8: Link budget examples for (a) 5G downlink and (b) 5G uplink.

beamwidth. Moreover, if without careful design, the sidelobe and the radiated spurious will generate potential blockers in the space. Accurate beam control with suppressed spurious radiation will be essential for providing stabilized data links. Secondly, Similar to the 60-GHz transceivers, considerations on the NF, linearity and gain flatness for optimizing the EVM are also necessary for 5G millimeter-wave phased-array transceiver. An optimized EVM performance over a long communication distance will be required to be supported over all beam angles. Finally, realizing a compact system size with suppressed manufacturing cost is also challenging for a 5G phased-array transceiver due to

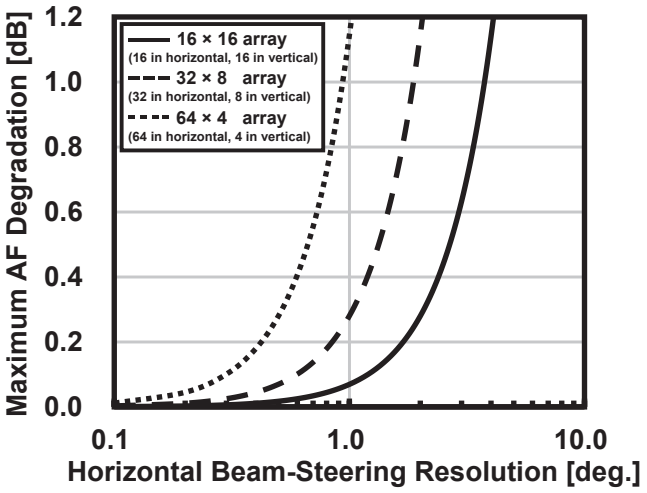


Figure 2.9: Calculated maximum array factor degradation due to the insufficient beam-steering resolution.

the numerous number of elements.

2.4.1 Array Size

To obtain sufficient 5G communication distance, a large array size is required for 5G base station (BS) using a CMOS millimeter-wave phased-array transceiver. The 5G NR standard allows a maximum equivalent isotropic radiated power (EIRP) of 75 dBm/100 MHz to the base station and 43 dBm to user equipment (UE) [38]. Usually, the differential topology power amplifier (PA) is adopted in the 5G transmitter for a larger power delivery. Within a reasonable power consumption, a single-element transmitter output power of around 12 dBm (antenna gain included) can be realized for modulation schemes like 64-QAM or 256-QAM in CMOS process [39, 40]. Thus, an array size of over 256 will be required to realize a 60-dBm EIRP. Fig. 2.8 shows link budget examples for a 400-MHz downlink in 256-QAM and a 200-MHz uplink in 16-QAM. The array sizes are 256 for the BS and 4 for the UE. The communication distance is 700 m, which corresponds to a line-of-sight (LOS) FSPL of 117 dB at 28 GHz. After receiving, the downlink and the uplink still maintain SNRs over 31.4 dB and 21 dB for the down-conversion and demodulation, respectively.

2.4.2 Beam-Steering Resolution

Large-sized millimeter-wave phased-array transceivers with narrow beam width are required in 5G. Insufficient beam-steering resolution in such a large-sized array will cause SNR degradation [3]. Fig. 2.9 shows the calculated maximum array factor (AF) degradation against the horizontal beam-steering resolution for a 256-element array. Considering complex modulation schemes, such as 64-QAM and 256-QAM, the degradation from AF should be kept under 0.1 dB. From Fig. 2.9, a horizontal beam-steering resolution of 1.2° is necessary for a 16×16 array. However, for array sizes of 64×4 and 32×8, a less than 1° resolution, corresponding to a phase tuning resolution larger than 6 bits, will be required. The beam-steering resolution improvement can be achieved by using the averaging effect of a large-sized array, which relieves the requirement on the phase shifting resolution. However, the potentially degraded sidelobe suppression will result in unwanted interference over the whole space [2]. As a result, improvements in the beam-steering resolution and the phase shifting resolution will be required for the 5G phase array transceivers. The related gain error, phase error, power consumption and area consumption should be minimized.

2.4.3 System Size and Manufacturing Cost

Due to the communication distance and the large array size, optimizations on the system size and the die area for a 5G phased-array transceiver become even more important than a 60-GHz IEEE 802.11ay transceiver. Additionally, the single-user MIMO (SU-MIMO) and the multi-user MIMO (MU-MIMO) are both required to be supported by the 5G. If we consider 256 element-transmitters for each data stream, totally over 2000 antennas and over 2000 element-transceivers will be required for supporting the MIMO configuration of up to 8 layers. Unreasonable system size and manufacturing cost will be induced even with the help of the antenna sharing networks. As a result, designing a CMOS 5G array system not only need to consider the reduced RF path gain and the parasitics from the silicon-based CMOS process, but also need to deal with the significantly increased system size along with manufacturing cost.

Chapter 3

LOFT and I/Q Imbalance Calibrated Transceiver

To increase the future wireless communication capacity in WLAN applications, the incoming IEEE 802.11ay standard allows the channel bonding among the channels defined in the 60-GHz band. As mentioned in Chapter 1, a maximum raw data rate of 42.24 Gb/s in 64-QAM can be achieved with a four-bonded channel. However, various challenges are still need to be addressed for realizing such high data rate within a reasonable power budget and a limited manufacturing cost.

Efforts have been concentrated on realizing 60-GHz CMOS transceivers with extremely high data rate during the past few years [10–24]. Recent research includes a transceiver implementation utilizing a dual-polarized multiple-in and multiple-out (DP-MIMO) technique [12]. 27.8 Gb/s in 16-QAM is achieved by doubling the data-rate in a single-polarization stream. Also, A frequency-interleaved (FI) transceiver is reported in [15]. The primary purpose is to relieve the EVM requirement for a single-element transceiver. A 4-channel bonding data-rate of 42.24 Gb/s is realized with two transceiver elements. However, both two works mentioned above suffer from large power consumption due to an additional front-end element. Also, two other 7.04 GS/s analog-to-digital converters (ADCs) will be required at the baseband, which makes the architectures even more power-hungry. Furthermore, the additional transceiver element occupying redundant on-chip area will in turn increase the manufacturing cost. Although realizing the 4-channel bonding with a single-element transceiver requires a 14.08 GS/s time-interleaved ADC, a power consumption of 69.5 mW for a 20 GS/s 6-bit ADC is still reasonable considering the whole system power budget [41]. The single-element transceiver implementation also helps to suppress the total cost of the system.

Due to the system simplicity, direct-conversion architecture is attractive for achieving

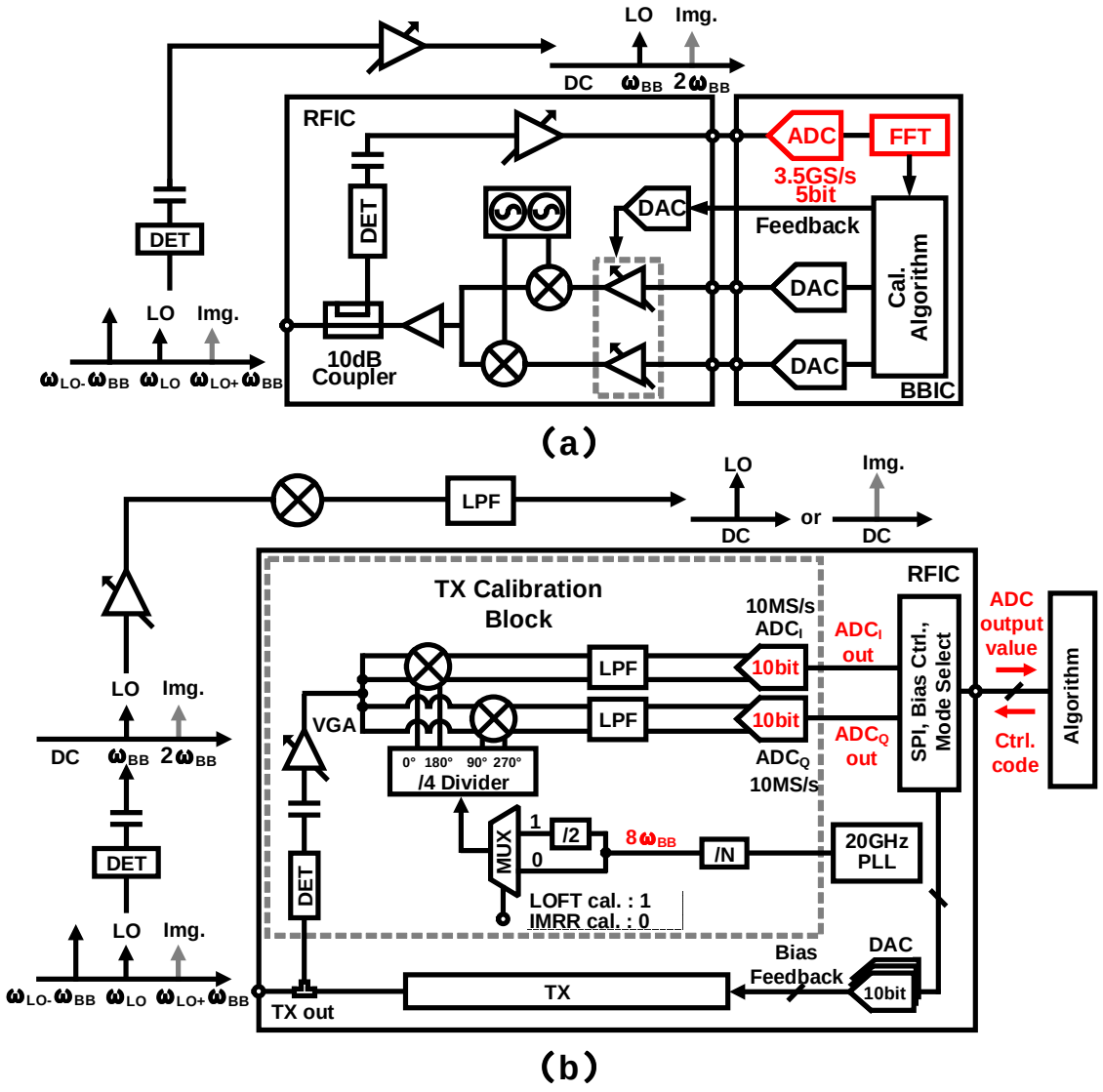


Figure 3.1: Block diagrams of (a) the traditional calibration method for LOFT and image calibration, (b) the proposed calibration method.

60-GHz transceivers with low manufacturing cost [10, 13, 15, 23, 27–30]. The power consumption could also be reduced by the limited number of transceiver building blocks. However, as mentioned in Chapter 2, such kind of transceiver suffers terribly from the LOFT and I/Q imbalance. For improving EVM, the LOFT and image signal are required to be well-suppressed. Usually, to improve the yields, an on-chip calibration block for LOFT suppression and IMRR is essential [10, 33]. [10] introduces a transceiver chipset developed for IEEE 802.11ad with a built-in self-calibration circuit. The LOFT suppression and IMRR in [10] are calibrated by reusing the 5-bit 3.52 GS/s baseband ADCs. Whereas, applying the same calibration method to an IEEE 802.11ay transceiver will

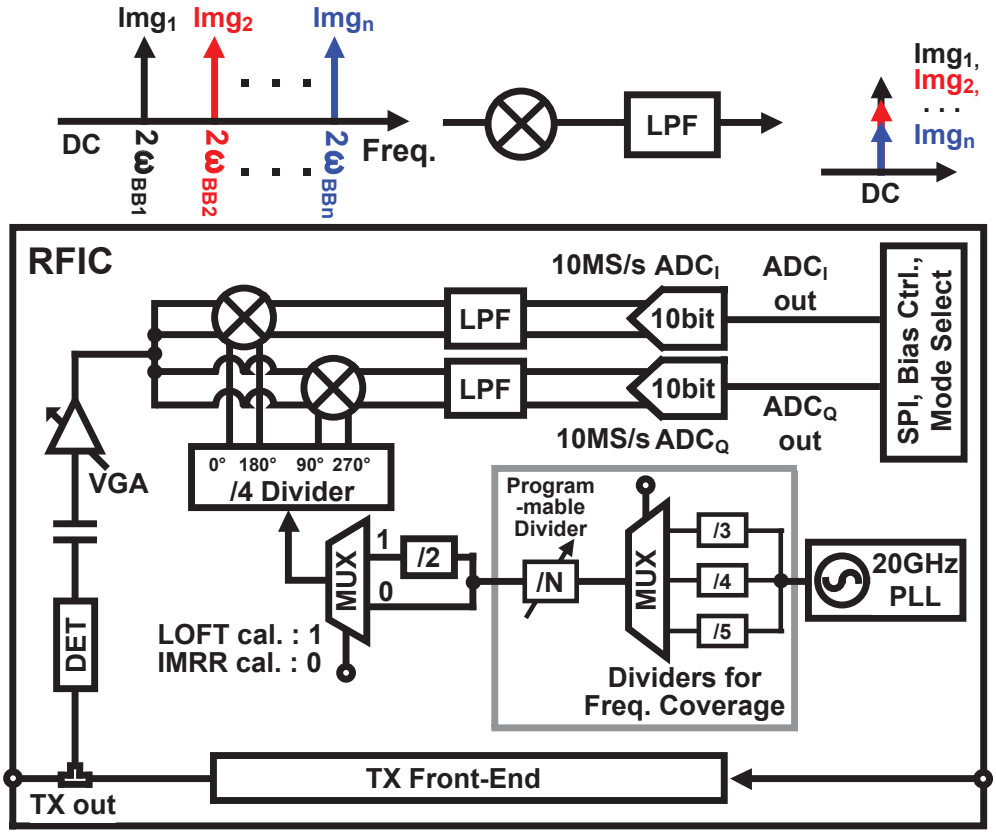


Figure 3.2: Extension of the proposed calibration method for FD-IMRR detection.

result in severe inaccuracy and even higher power consumption. Therefore, calibration circuits designed for IEEE 802.11ay demands an accuracy improvement along with a small enough power and area overhead.

To address the issue mentioned above, a 60-GHz CMOS transceiver designed for the IEEE 802.11ad/ay is introduced in this chapter. A compact calibration block featuring high accuracy and low power consumption for LOFT and I/Q imbalance is presented. Thanks to the suppressed impairments by the proposed calibration, the transceiver realizes a single-carrier (SC) mode data-rate of 24.64 Gb/s in 128-QAM with a TX-to-RX EVM of -26.1 dB. A 4-channel bonding raw data-rate of 42.24 Gb/s is also achieved by the calibrated transceiver. The maximum data-rate realized by this work is 50.1 Gb/s with 8.35-GSymbol/s symbol rate in 64-QAM. Higher-order modulation schemes and broader signal bandwidth are realized for a significantly increased data-rate. At the same time, the power and area costs are well-suppressed for the next generation WLAN system.

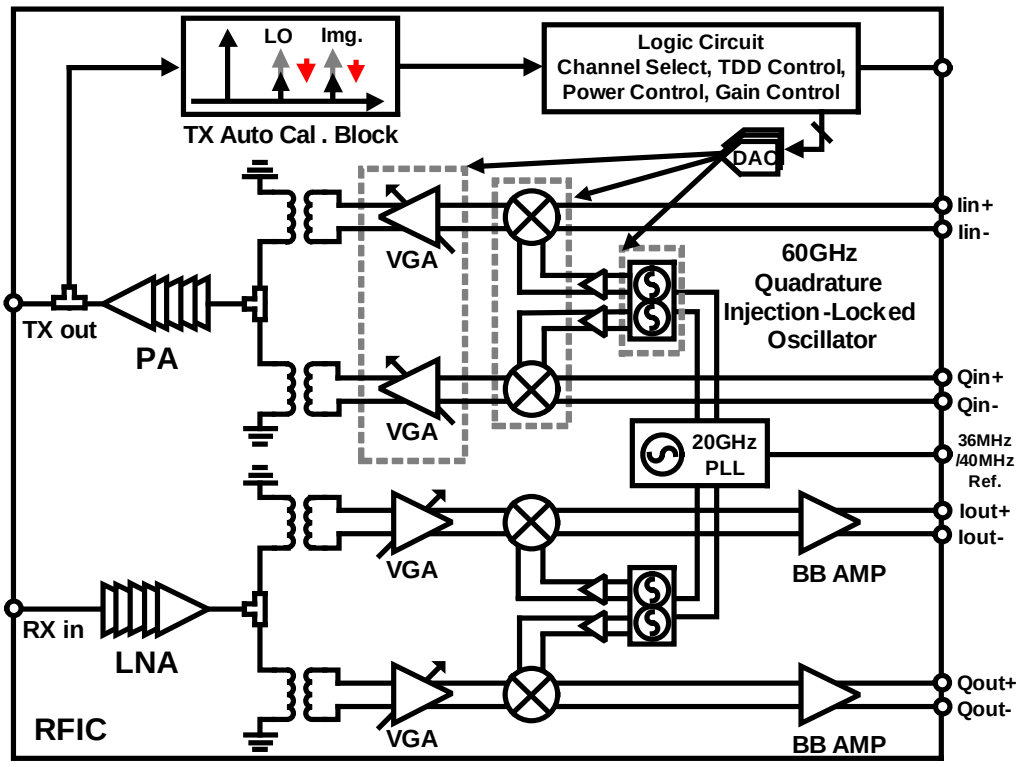


Figure 3.3: Block diagram of the proposed 60-GHz transceiver.

3.1 Proposed LOFT and I/Q Imbalance Calibration Architecture

Fig. 3.1(a) shows the traditional calibration method for LOFT and I/Q imbalance calibration [10]. In [10], the LOFT and image signal after detection are directly processed by the ADC and the fast Fourier transformer (FFT) circuit. A 5-bit baseband ADC for I/Q demodulation is reused due to power saving. Although the traditional method includes a FD-IMRR calibration, poor resolution of the ADC still leads to a severe calibration inaccuracy. Accuracy improvement in the traditional approach can be realized with a higher resolution detection ADC. However, the cost is the increased power consumption and on-chip area. Fig. 3.1(b) shows the proposed calibration method. In this work, a small portion of the TX output will be coupled to the input of the detector. If a baseband test-tone signal with a frequency of ω_{BB} is assumed, LOFT and image signal frequency will be detected at ω_{BB} and $2\omega_{BB}$. Different from the traditional method, the detected LOFT and image signal will be down-converted to DC by an area-efficient quad-phase mixer. Thus, two 10-bit, 10 MS/s successive approximation (SAR) ADCs can be utilized for a quick and accurate calibration. Compared with the 67-mW ADC and the power-hungry

TX	Up-Conversion Mixer	RF Buffer	PA	Board Loss	Total
Power Gain [dB]	-13.00	3.00	28.70	-9.80	
Cumulative Gain [dB]	-13.00	-10.00	18.70	8.90	8.90
NF [dB]	13.00	8.00	8.40	9.80	
Cumulative NF [dB]	13.00	21.00	22.67	22.68	22.68
OIP3 [dBm]	3.00	13.00	18.00	100.00	
Cumulative OIP3 [dBm]	3.00	5.21	17.89	8.09	8.09

RX	Board Loss	LNA	RF Buffer	Down-Convesion Mixer + BB Amp	Total
Power Gain [dB]	-9.80	25.88	3.00	5.00	
Cumulative Gain [dB]	-9.80	16.08	19.08	24.08	24.08
NF [dB]	9.80	4.90	8.00	14.30	
Cumulative NF [dB]	9.80	14.70	14.72	14.77	14.77
OIP3 [dBm]	100.00	1.70	13.00	7.00	
Cumulative OIP3 [dBm]	100.00	1.70	4.10	4.91	4.91

Figure 3.4: Level diagram design of the proposed transceiver.

FFT logic circuit utilized in the traditional method [10], the calibration block in this work only consumes 3.1 mW and 0.2-mm^2 area. Power-efficient and high-accuracy calibration is realized with a compact chip size.

As mentioned in Chapter 2, the FD-IMRR due to the baseband cutoff frequency mismatch can limit the system EVM. The proposed calibration method can also be applied for FD-IMRR calibration. The block diagram of the FD-IMRR calibration is shown in Fig. 3.2. With a series of frequency dividers for covering the required calibration LO frequencies, the proposed circuit can support the baseband frequency sweep. The FD-IMRR due to the baseband cut-off frequency mismatch can be compensated by the capacitance tuning [10]. In this condition, a wide operating bandwidth will be required for the detector. Regarding the potentially degraded frequency response of the detector, the NF of the calibration path can be improved by applying a pre-amplifier before the detector.

3.2 Circuit Implementation

Fig. 3.3 shows the topology of the proposed direct-conversion 60-GHz transceiver. The transmitter in this work consists of a 5-stage PA, I/Q RF variable gain amplifiers (VGAs) and I/Q double-balanced passive mixers. The receiver consists of a 5-stage low noise amplifier (LNA), I/Q RF VGAs, I/Q double-balanced active mixers and I/Q baseband amplifiers. The transceiver design in this work mainly focuses on ch.1 to ch.4 defined

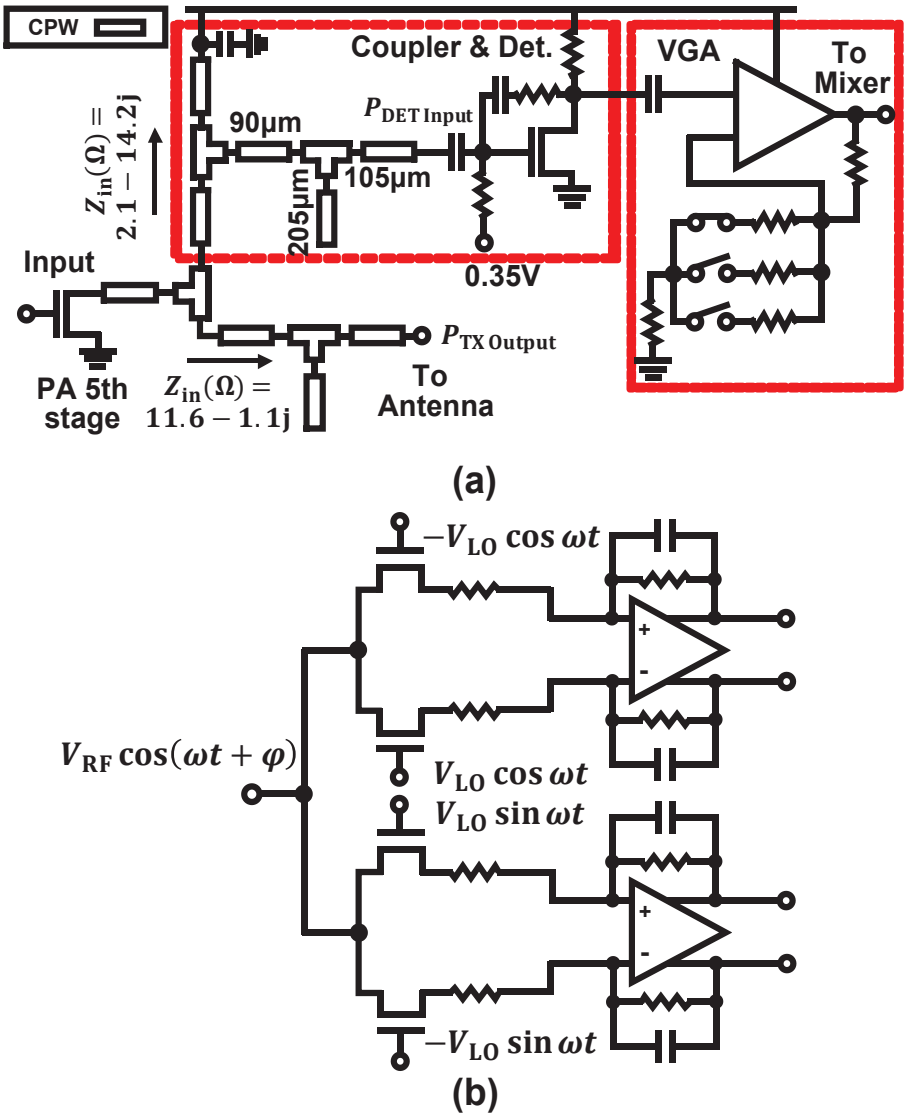


Figure 3.5: Circuit schematic of (a) the coupler, the detector and the VGA, (b) the quad-phase mixer and the low-pass filter.

in IEEE802.11ay. The LO generation in this work is realized by a quadrature injection-locked oscillator (QILO) with injection from a 20-GHz sub-sampling PLL [32]. The LO chain is capable of generating every required carrier frequencies including the channel bonding. To minimize the LOFT and I/Q imbalance of the transmitter, a calibration block mentioned in Section 3.1 is integrated with the transceiver. The transceiver system level design is shown in Fig. 3.4. Enough design margin is included in consideration of 64-QAM four-channel-bonding operation.

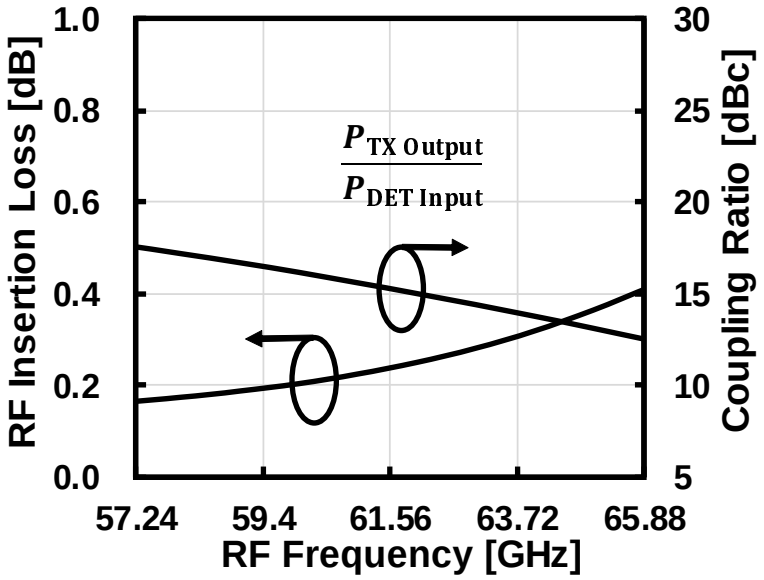


Figure 3.6: Simulated coupling ratio and RF path insertion loss of the proposed coupler.

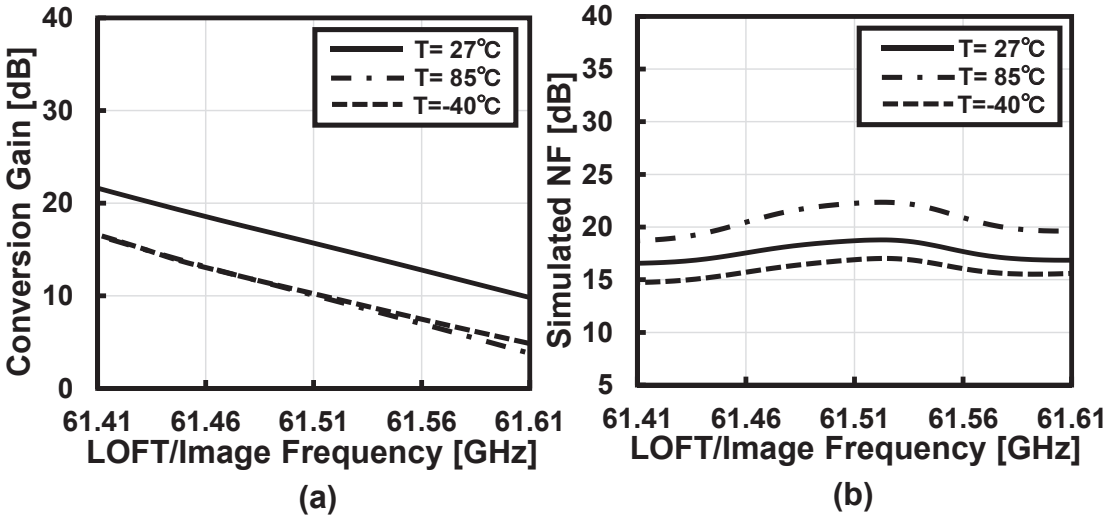


Figure 3.7: Simulated (a) conversion gain and (b) noise figure of the proposed calibration block against the input impairment frequency of the TX.

3.2.1 Calibration Block

Fig. 3.5(a) shows the circuit schematics for the coupler, detector and variable gain amplifier in the calibration path. Conventional couplers for detection usually utilize the quarter-wavelength coupled-line architecture [10, 42]. However, such couplers suffer from high

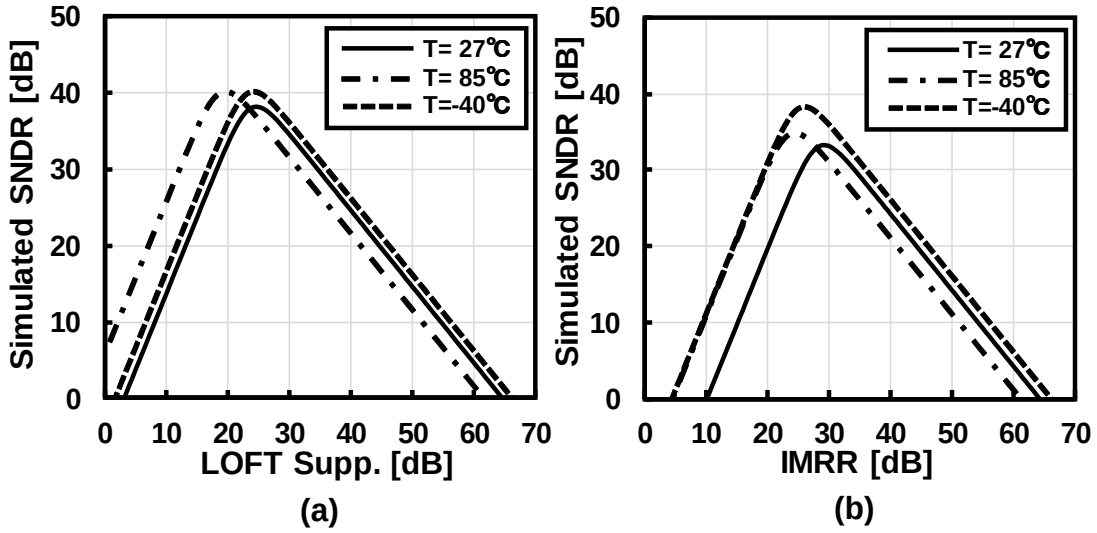


Figure 3.8: Simulated SNDR of the calibration path against (a) LOFT suppression and (b) IMRR.

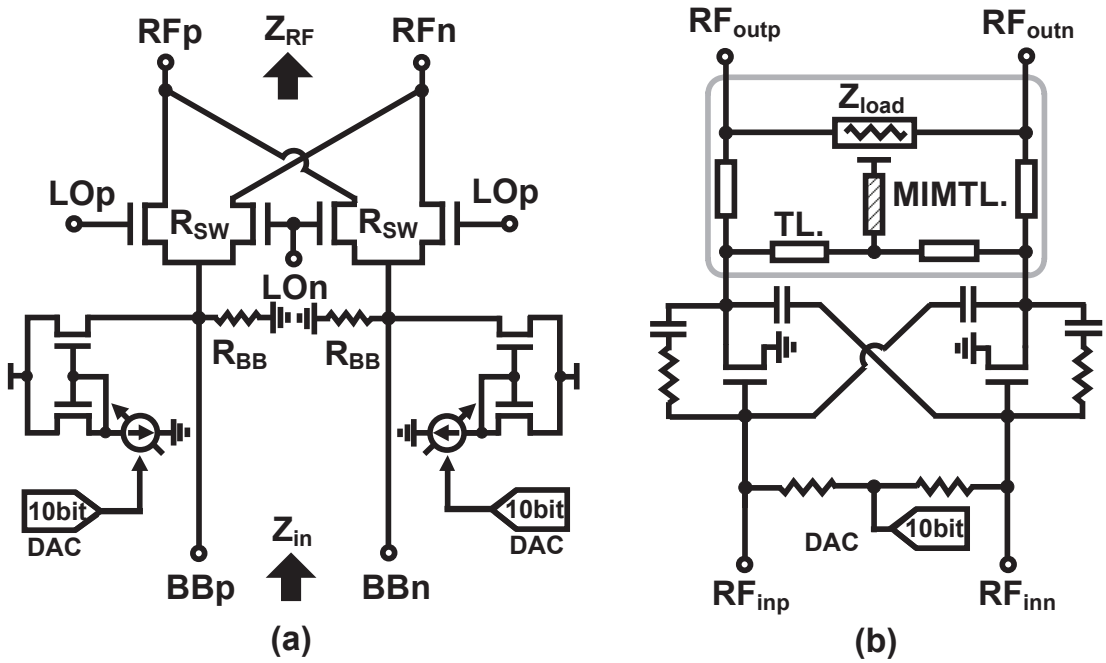


Figure 3.9: Circuit schematic of (a) the 60-GHz up-conversion mixer and (b) the 60-GHz variable-gain amplifier.

insertion-loss at RF path, which will significantly degrade the linearity performance of the TX. Additionally, large on-chip area will be consumed by the quarter-wavelength lines.

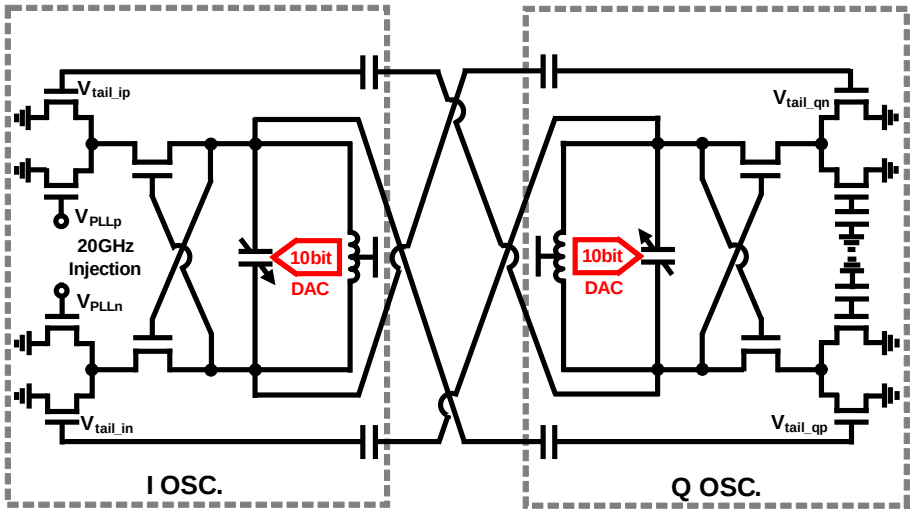


Figure 3.10: Circuit schematic of quadrature injection-locked oscillators (QILO).

In this work, an area-efficient coupler based on the transmission line (TL) is adopted. Instead of the lossy quarter-wavelength lines, the coupling in this work is realized by the shunt TL stub matching. The power is splitted at the branch point. After the following matching networks for the antenna side and the coupler side, the power of $P_{\mathrm{TX_Output}}$ and $P_{\mathrm{DET_Input}}$ will be delivered to the detector and the output of the TX, respectively. The simulated coupling ratio and the insertion loss for the PA are shown in Fig. 3.6. Within a frequency range of 57.24 to 65.88 GHz, the insertion loss for the TX is always less than 0.42 dB with a coupling ratio of larger than 17.5 dBc. The required area for this coupler is only 0.025 mm^2.

The detector circuit used in this work is based on a diode-connected transistor. A 0.35-V bias is chosen to achieve the highest second-order output. The VGA circuit is realized with a non-inverting amplifier. A DC block is inserted between the detector and the VGA to filter out the DC component generated by self-mixing. The signal output from the VGA will be sent to a mixer for down-conversion.

Fig. 3.5(b) shows the circuit schematic of the down-conversion mixer together with the first-order LPF. The 3dB-bandwidth of the LPF is designed to be 316 kHz, which only allows the DC component transferred to the ADC. Due to the random phase of the input signal, utilizing a single-phase LO for the down-conversion will lead to a time-variant DC level. As a result, a quad-phase down-conversion is adopted in this work to minimize the SNR degradation in the calibration path. If a mixer input signal of $V_{\mathrm{RF}}\cos(\omega t + \varphi)$ and a quad-phase LO are assumed, the detected signal strength can be derived from the I/Q

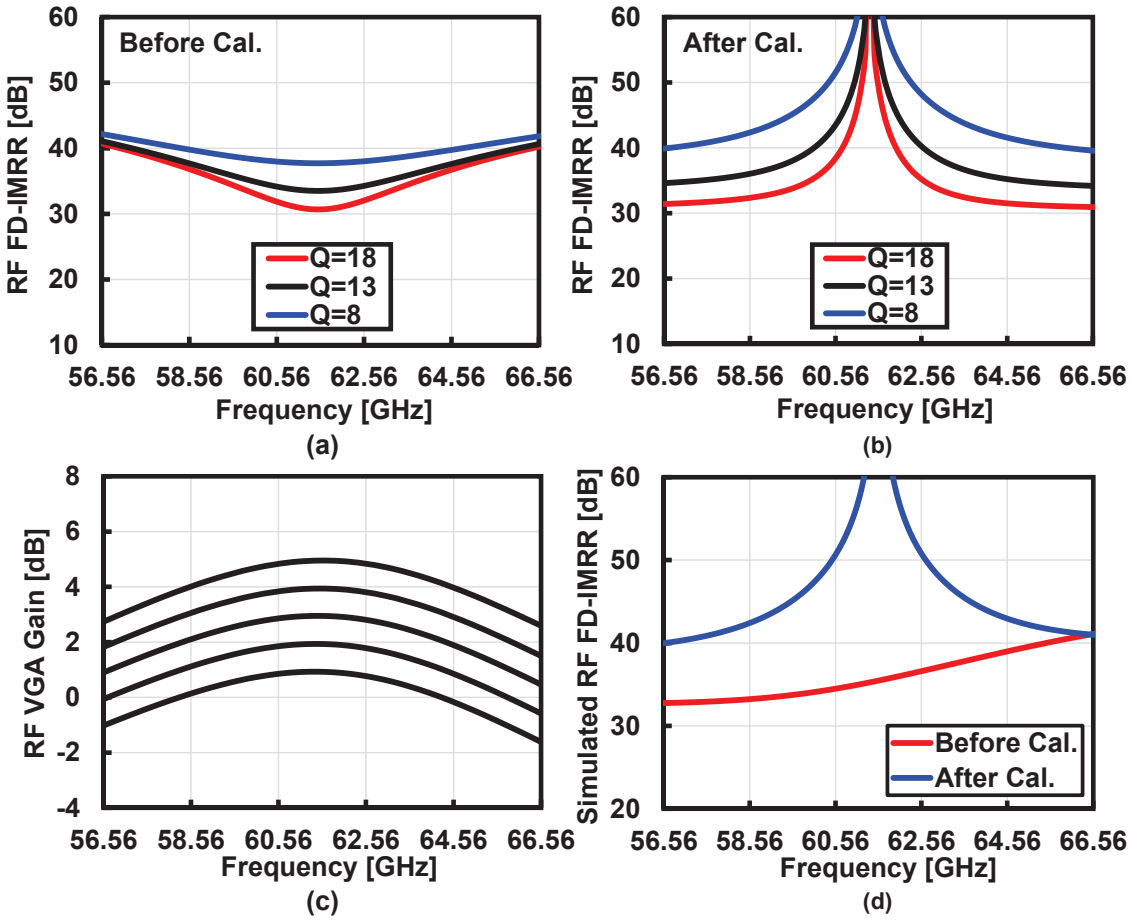


Figure 3.11: IMRR due to the RF domain frequency-dependent I/Q mismatch (a) before the proposed cal. and (b) after the proposed cal. The simulated (c) RF VGA gain and (d) RF FD-IMRR before and after the proposed calibration.

output voltages.

$$\begin{aligned} Signal\,Strength &= \sqrt{V_{\text{out\_I}}^2 + V_{\text{out\_Q}}^2} \\ &= 2V_{\text{LO}}V_{\text{RF}}\sqrt{\sin\varphi^2 + \cos\varphi^2} = 2V_{\text{LO}}V_{\text{RF}} \end{aligned} \tag{3.1}$$

It can be found from the above equation that the signal strength is no longer a function of the input phase. Quick and accurate detection can be realized.

Besides the constant magnitude detection, the calibration path still needs to achieve the required 50-dBc detection sensitivity. In this work, the calibration LOs (ω_{BB} or $2\omega_{\text{BB}}$) are generated from the 20-GHz PLL. The PLL output in this work is divided by ratios of 192 for the LOFT calibration and 96 for the IMRR calibration. As a result, when the

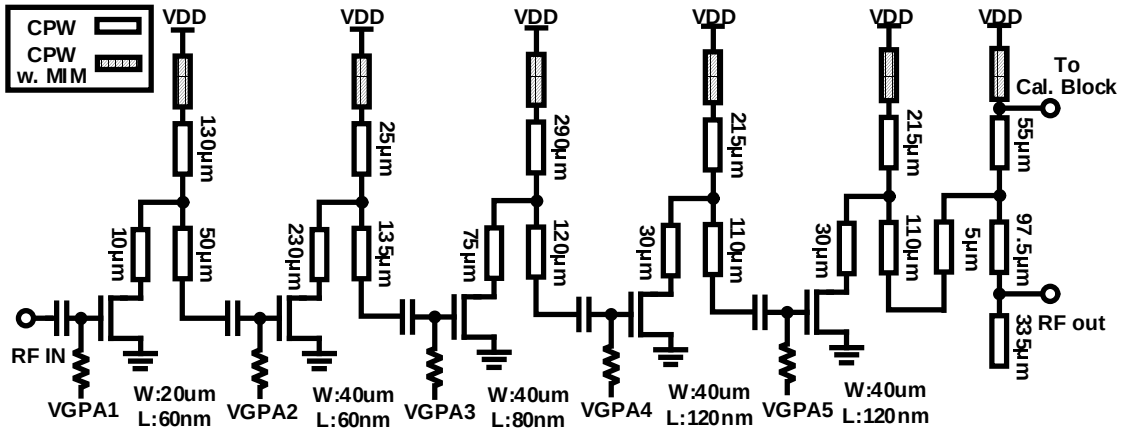


Figure 3.12: Circuit schematic of the 60-GHz 5-stage power amplifier.

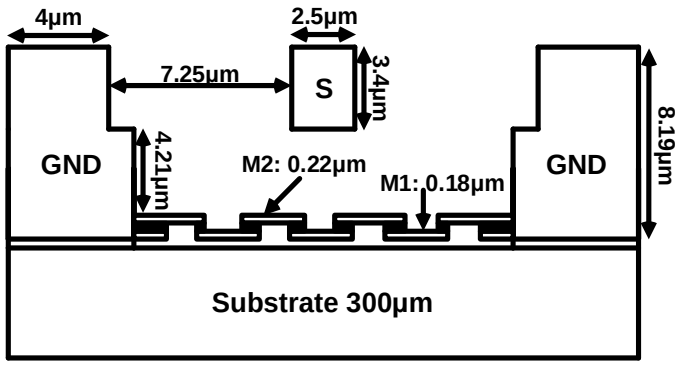


Figure 3.13: Cross-section view of the transmission line.

transmitter is operating at ch. 2.5 (LO frequency: 61.56 GHz, PLL output frequency: 20.52 GHz), the required baseband test-tone frequency will be 107 MHz. Fig. 3.7 shows the simulated conversion gain and noise figure of the calibration path against the input LOFT or image frequency. The TX RF output frequency is kept with 61.667 GHz considering the 107-MHz baseband test-tone. While, the TX output power is kept with 0 dBm. With three different temperature conditions (27 °C, 85 °C and -40 °C), the 61.56-GHz LOFT and the 61.453-GHz image result in a conversion gain variation of less than 5.5 dB and a noise figure variation of less than 4.1 dB.

Fig. 3.8 shows the simulated SNDR against the LOFT suppression and IMRR over different temperature conditions. The TX output power is still kept with 0 dBm. Usually an uncalibrated LOFT suppression or IMRR can reach 20 dB [10]. A 10-dB design margin is considered for the uncalibrated impairments. To improve the SNDR for a small LOFT suppression or IMRR, the gain of the calibration path can be further decreased. For a large

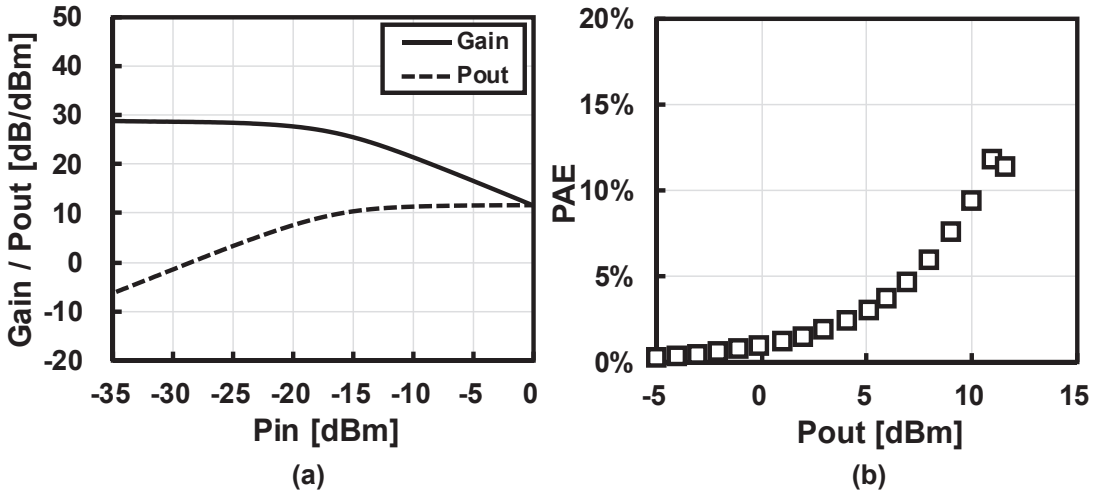


Figure 3.14: (a) Measured output power, gain and (b) corresponding PAE of the five-stage power amplifier.

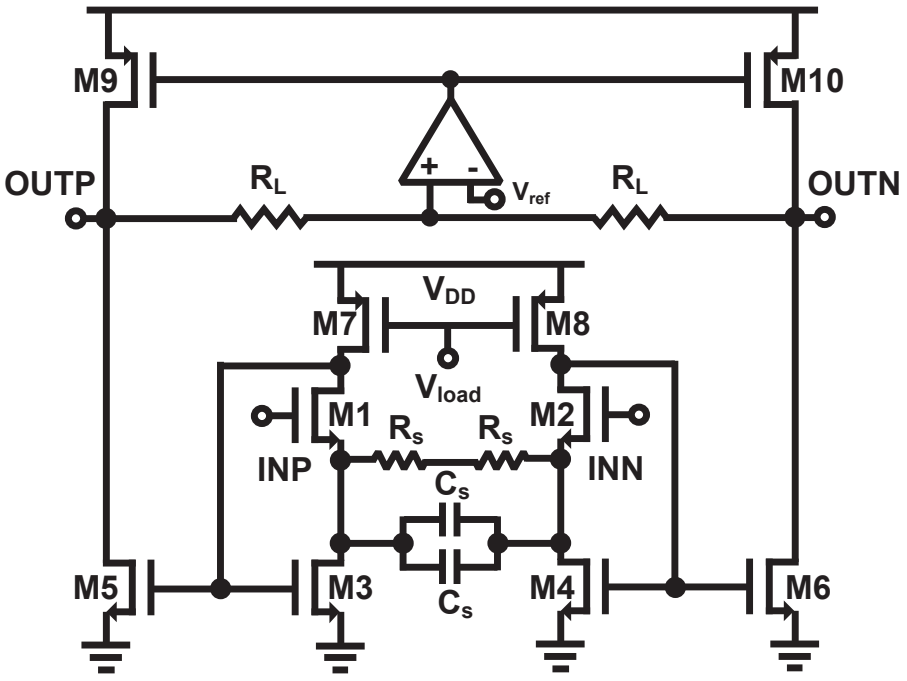


Figure 3.15: Circuit schematic of the baseband amplifier.

LOFT suppression or IMRR, the SNDR of the calibration path is limited by the noise floor. Regarding the required 50-dBc calibration sensitivity, more than 10-dB margin can be realized as shown in Fig. 3.8.

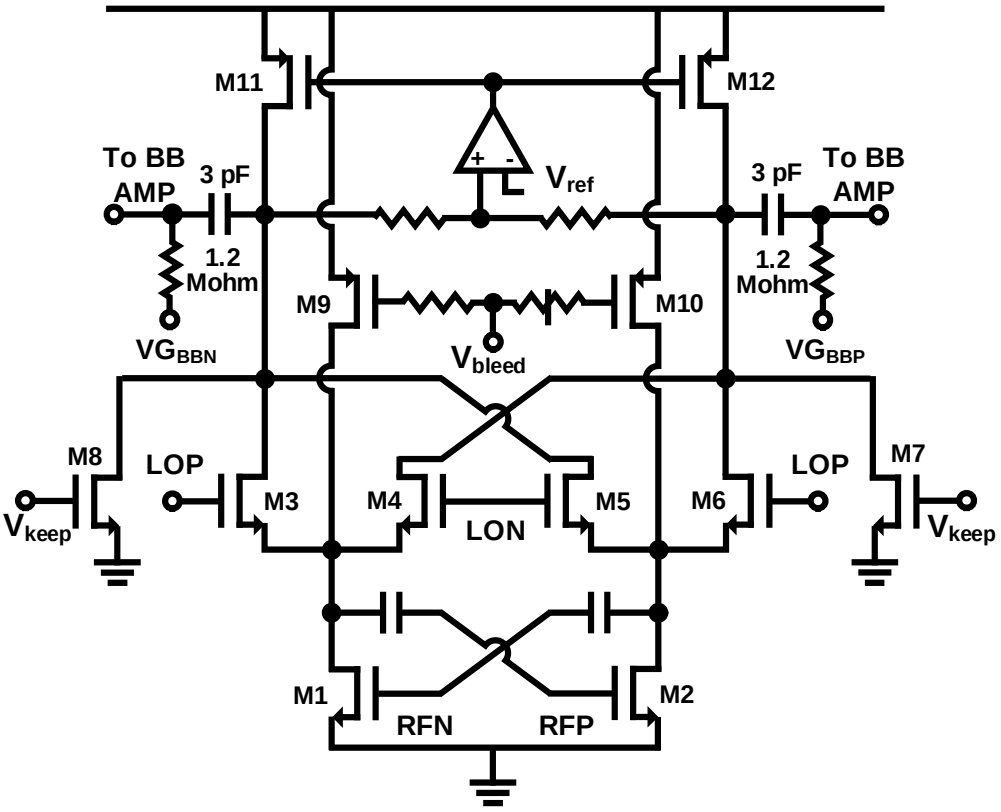


Figure 3.16: Circuit schematic of the fast-startup down-conversion mixer.

The DC offset of the calibration block will also degrade the calibration accuracy. Because the calibration system itself can be treated as a receiver, the DC offset at the calibration mixer output will directly offset the down-converted DC component. It is well-known that the DC offset for a receiver can be expressed as the following equation [43]:

$$V_{\text{offset\_total}} = V_{\text{self\_mixing}} + V_{\text{nonlinear}} + V_{\text{dynamic}} \tag{3.2}$$

where $V_{\text{self\_mixing}}$ represents the DC offset caused by the calibration LO self-mixing which is static and independent of the input. $V_{\text{nonlinear}}$ stands for the input-dependent DC component caused by the second-order nonlinearity of the calibration circuit. V_{dynamic} denotes the dynamic DC offset. Because of the huge frequency difference between the calibration LO and the 60-GHz RF signal, the dynamic DC offset caused by re-radiation can be ignored. Regarding $V_{\text{self\_mixing}}$, the DC offset from self-mixing can be removed by testing the ADC outputs $V'_{\text{out\_I}}$ and $V'_{\text{out\_Q}}$ without any RF input. The signal strength can be rewritten as:

$$Signal\,Strength' = \sqrt{(V_{\text{out\_I}} - V'_{\text{out\_I}})^2 + (V_{\text{out\_Q}} - V'_{\text{out\_Q}})^2} \tag{3.3}$$

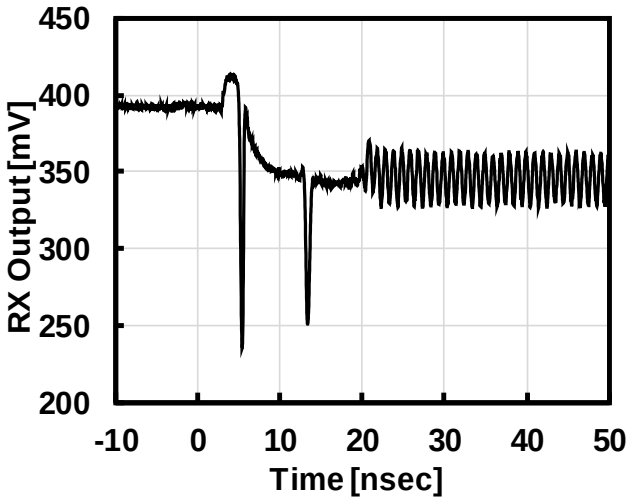


Figure 3.17: Measured output of the receiver.

The accuracy of *Signal Strength'* will rely on the effective number of bits (ENOB) of the ADC. With enough design margin (10 bit in this work), the $V_{\text{self\_mixing}}$ will not limit the final calibration accuracy. Furthermore, it is known that $V_{\text{nonlinear}}$ can be minimized by optimizing the IP2 [44]. The simulated IIP2 for the calibration path in a Monte Carlo simulation falls inside a range of 19.8 to 20.9 dBm regarding the nonlinearity and random mismatch. When the TX is operating at ch. 2.5 (LOFT frequency is 61.56GHz), a large LOFT of -25 dBm at the TX output will result in a -40-dBm input power for the calibration block. The corresponding DC component $V_{\text{nonlinear}}$ is estimated to be 0.23 mV. While for a small LOFT, the induced DC offset is negligible, which will not limit the calibration accuracy.

Additionally, the I/Q imbalance of the calibration circuit will cause potential degradation in the calibration accuracy. Moreover, the phase of the input signal φ_{in} will again influence the detected signal strength. Both 1-dB magnitude mismatch and 10-degree phase mismatch will cause a larger than 10% peak-to-peak ripple in the detected signal. The magnitude and phase imbalance of the calibration circuits can be suppressed by a frequency-divider-based LO generation and symmetric layout. The ripple can further be mitigated by an averaging function, so the calibration accuracy is not much degraded by the I/Q imbalance.

During the calibration period, the second harmonic of the detected LOFT generated by the calibration VGA will also fall into the same frequency with the detected image signal ($2\omega_{\text{BB}}$). As a result, the LOFT will be calibrated first to prohibit the IMRR calibration accuracy from degradation. At the same time, the calibrated LOFT will also be slightly

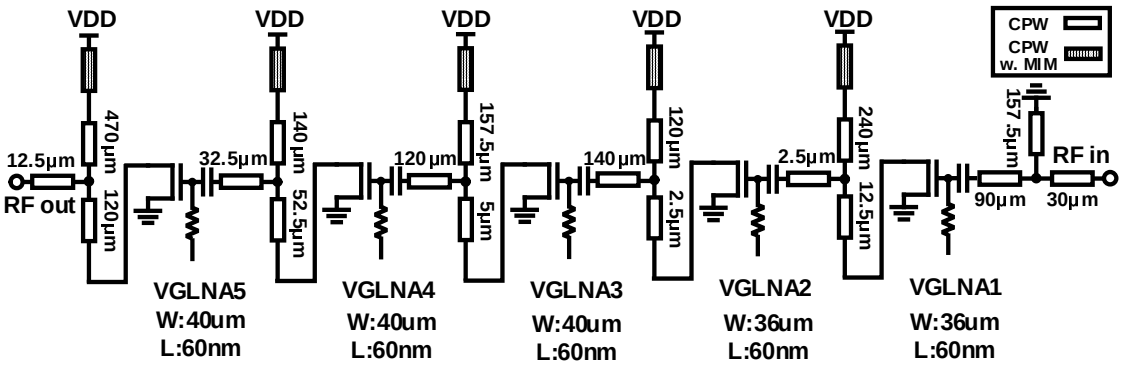


Figure 3.18: Circuit schematic of the 60-GHz 5-stage LNA.

influenced by the IMRR calibration due to the changed bias condition. Thus, an additional LOFT calibration is added at the end of the calibration procedure.

3.2.2 Transmitter

To meet the stringent transmitter EVM requirement from the IEEE 802.11ay, an improved linearity needs to be achieved within a flat frequency response. A mixer-first topology is adopted in the transmitter with the purpose of wide-band matching and low power consumption [13]. Fig. 3.9(a) shows the circuit schematic of the double-balanced up-conversion mixer. The LOFT cancellation in this work is realized by tuning the current sources at the baseband side [45]. Including the design margin, a 10-bit R-DAC is adopted for achieving a tuning resolution of less than 0.1-mV, which corresponds to a higher than 50-dB LOFT suppression.

As mentioned in Chapter 2, the I/Q imbalance in this work is compensated with a power-efficient RF domain calibration. Fig. 3.9(b) shows the capacitive-cross-coupling RF VGA. The I/Q magnitude mismatch is compensated by tuning the gate bias. Regarding the phase mismatch calibration, Fig. 3.10 shows the circuit schematic of the QILO. A 3-bit switching capacitor and a 10-bit-DAC-controlled varactor are designed to cover a frequency range from 57 to 66 GHz. To fullfil the required resolution for the I/Q phase calibration mentioned in Chapter 2, a sub-degree I/Q phase tuning is realized by tuning the free-run frequency of the I oscillator [32]. During the calibration period, the magnitude mismatch will be compensated first and afterward the phase mismatch will be calibrated by the RF gain-invariant phase tuning. The analysis mentioned in Chapter 2 assumed a perfect RF domain calibration. However, the mismatch between the I/Q calibration circuits will also induce additional RF domain IMRR degradation. The degradation from the QILO will be limited and frequency-independent due to its position at the LO path.

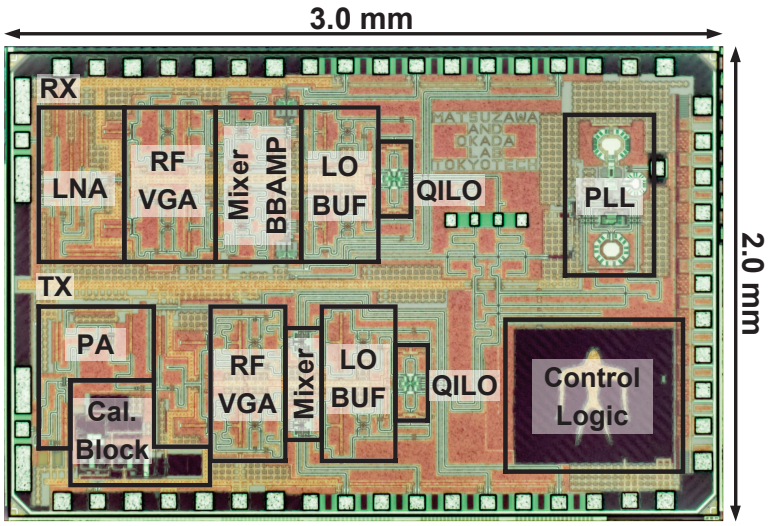


Figure 3.19: Die photo of the 60-GHz transceiver with calibration block.

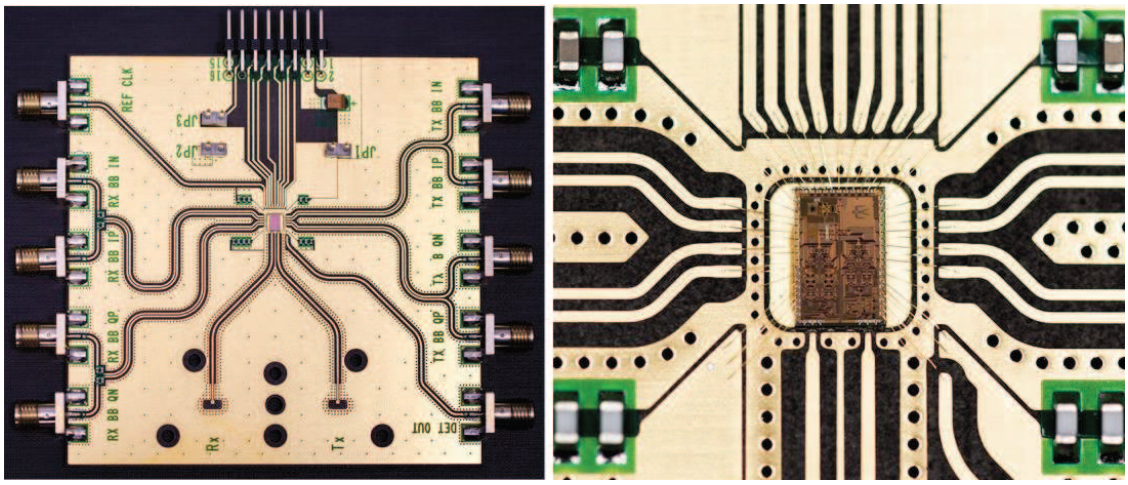


Figure 3.20: RF PCB for measurement.

While, the I/Q VGA will be the main contributor to the IMRR degradation due to its wide operational bandwidth. To analyze the influence from the RF VGA, the L-type matching network at the RF VGA output is modeled as a parallel RLC resonant circuit. When the feedback resistor is large enough, the I/Q imbalance due to the VGA can be presented with the following equations:

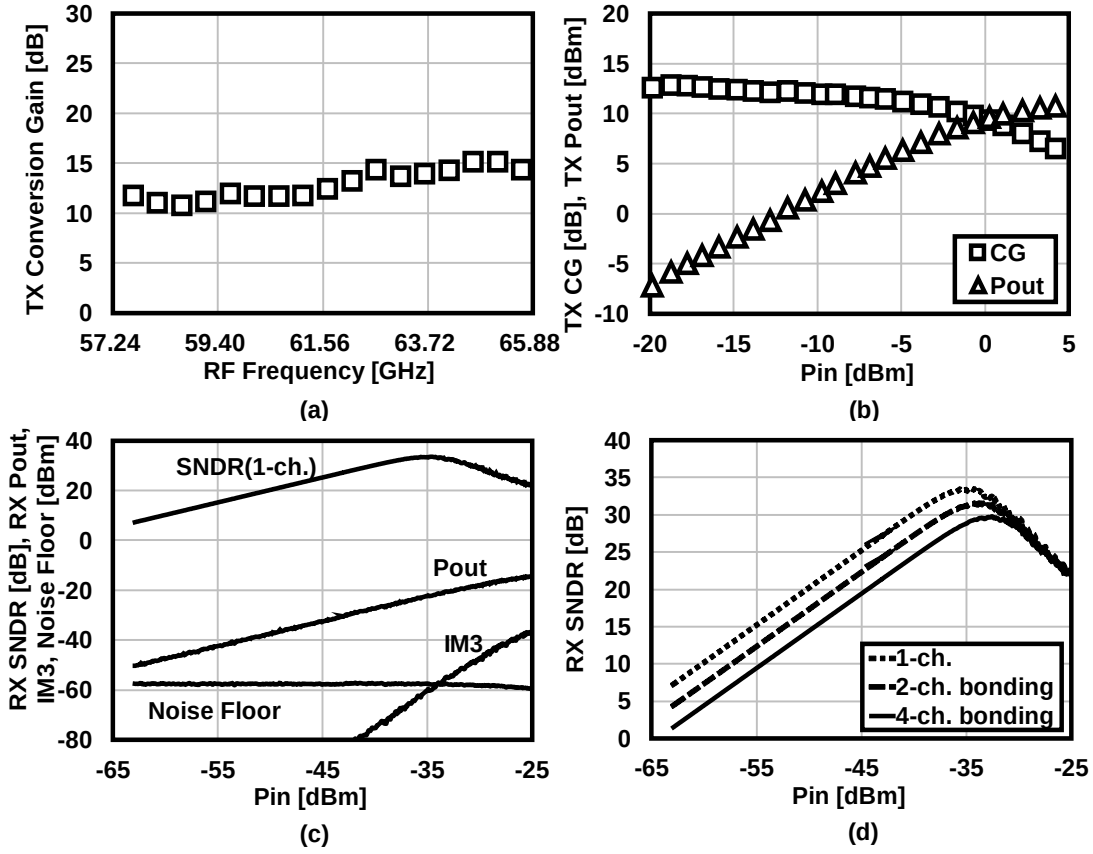


Figure 3.21: Measured characteristics of the TX: (a) TX conversion gain over frequency and (b) output power and conversion gain against input power. Measured characteristics of the RX: (c) RX SNDR, Pout, IM3, noise floor for 1-channel bandwidth and (d) RX SNDR for 2-channel and 4-channel bonding bandwidth.

Table 3.1: Core Area of Blocks

	Core Area [mm^2]
TX	1.07
RX	1.09
PLL	0.21
Cal. Block	0.19
Logic	0.36

$$\begin{aligned}\Delta A = \frac{MAG_{\mathrm{I}}}{MAG_{\mathrm{Q}}} &= \frac{\left|\dfrac{g_{\mathrm{m}}(L/C)}{R + j(\omega L - 1/\omega C)}\right|_{\mathrm{I}}}{\left|\dfrac{g_{\mathrm{m}}(L/C)}{R + j(\omega L - 1/\omega C)}\right|_{\mathrm{Q}}} \\ &= \sqrt{\frac{g_{\mathrm{m\_I}}^2\left(1 + Q^2\left(\dfrac{\omega}{\omega_{0\mathrm{Q}}} - \dfrac{\omega_{0\mathrm{Q}}}{\omega}\right)^2\right)}{g_{\mathrm{m\_Q}}^2\left(1 + Q^2\left(\dfrac{\omega}{\omega_{0\mathrm{I}}} - \dfrac{\omega_{0\mathrm{I}}}{\omega}\right)^2\right)}}\end{aligned} \tag{3.4}$$

Table 3.2: Power Consumption of Blocks

	Sub Blocks	**Power Consumption** [mW]
TX	PA	105.7
	I/Q RF VGA	12.1
	I/Q Mixer	2.0
	I/Q LO Buffer	16.6
	QILO	14.6
Cal. Block		3.1
RX	LNA	60.2
	I/Q RF VGA	20.5
	I/Q Mixer	6.4
	I/Q BB Amp	12.3
	I/Q LO Buffer	13.8
	QILO	10.3
PLL		15.0

$$\Delta\varphi = \arctan\left(Q\left(\frac{\omega_{0\mathrm{I}}}{\omega} - \frac{\omega}{\omega_{0\mathrm{I}}}\right)\right) - \arctan\left(Q\left(\frac{\omega_{0\mathrm{Q}}}{\omega} - \frac{\omega}{\omega_{0\mathrm{Q}}}\right)\right) \tag{3.5}$$

where ΔA and $\Delta\varphi$ are the I/Q magnitude and phase mismatch, while Q and ω_0 stand for the quality factor and the resonant frequency of the matching network. The equations find the IMRR degradation due to the transistor g_m mismatch does not rely on the frequency and can be easily removed. However, the resonant frequency difference caused by the mismatched transistor size and I/Q matching networks will cause a FD-IMRR after calibration. Fig. 3.11(a) and (b) show the influence of the RF FD-IMRR degradation due to the resonant frequency mismatch at channel 2.5. Severe FD-IMRR degradation against the increasing bandwidth after the calibration can be observed with an 100-MHz ω_0 mismatch (1.6%). Fig. 3.11 also implies that, RF FD-IMRR will be improved with a lower quality factor due to the suppressed in-band gain and phase mismatch. To minimize the degradation from the calibration circuit, the RF VGA in this work is designed based on the TL. The 50-ohm TL are utilized to realize a matching network with a reduced quality factor Q. Additionally, a symmetric layout of the TL matching network is also strong against the passive components mismatch between the I and Q path. Fig. 3.11(c) shows the simulated gain of the RF VGA with a 1-dB tuning step. A bandwidth of larger than 10 GHz is covered in this work. Furthermore, the RF-VGA is controlled by a 10-bit DAC. A less than 0.1-dB tuning step is achieved, which meets the resolution requirement from the I/Q magnitude imbalance calibration. The simulated IMRR before and after the proposed calibration is shown in Fig. 3.11(d). A transistor size mismatch of 5% is included in this simulation. After the calibration, larger than 40-dB IMRR can be maintained within

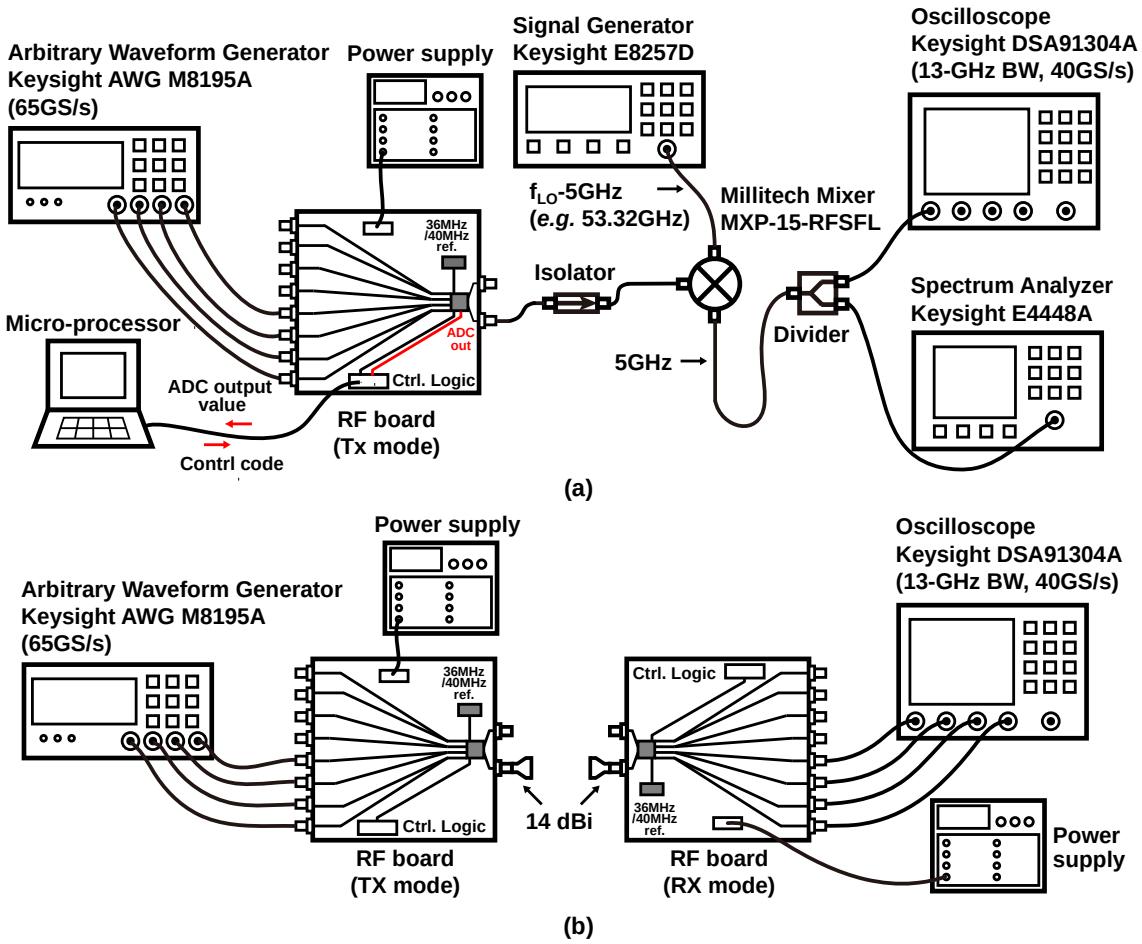


Figure 3.22: Equipment setup for (a) TX calibration and TX EVM measurement (b) TX-to-RX EVM measurement.

the whole 60-GHz band. Although the decreased Q results in a 5-dB maximum gain, the wide band matching still contributes to a flatter frequency response. The simulated transmitter-mode 3-dB bandwidth is from 54.8 GHz to 66.7 GHz.

Fig. 3.12 shows the TL-based five-stage common-source power amplifier. A cross-section view for the proposed TL is shown in Fig. 3.13. The top metal layer is selected for the signal line while the two interdigitated metal layers at the bottom are employed for shielding. Specific sizes of the TL are optimized for lower attenuation constant, which ensures an efficient and reliable matching performance. The VDD feed line for the power amplifier is realized by TL with shunt metal-insulator-metal (MIM) capacitor to ground. The feed line topology is carefully modeled with low impedance but high isolation to RF signal. Fig. 3.14 shows the measured results for the power amplifier at 61.56 GHz. The measured output P_{1dB} is 6.9 dBm and the saturated output power is 11.6 dBm. The

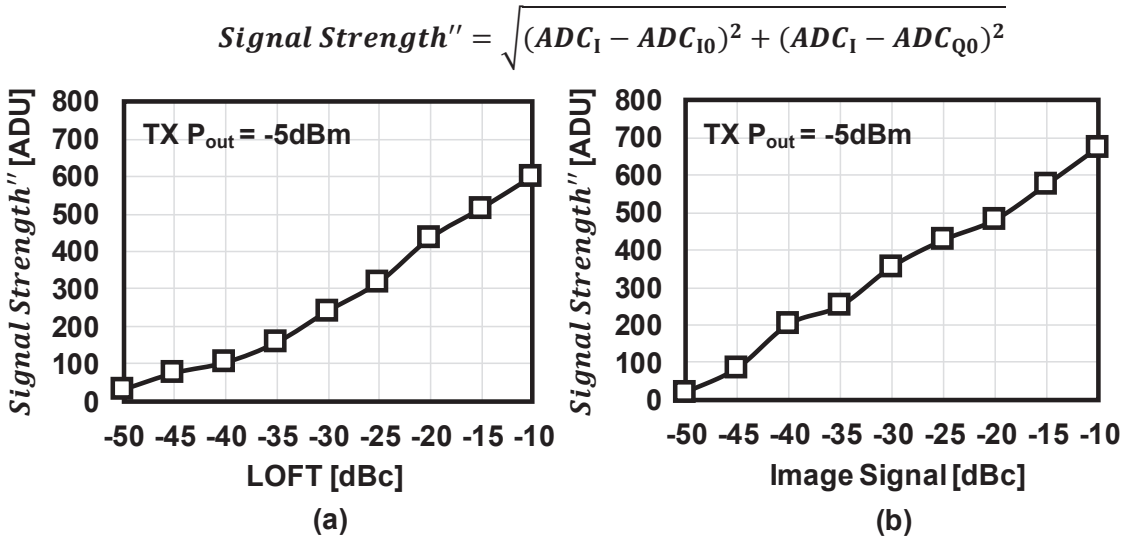


Figure 3.23: Measured (a) detected signal strength against the LOFT and (b) detected signal strength against the image signal.

corresponding power-added efficiency (PAE) at the P_{1dB} is 4.6%.

3.2.3 Receiver

As mentioned in Chapter 2, receivers targeting at the IEEE 802.11ay standard demand a careful design. The usage of the flipped-voltage-follower (FVF) [46] based amplifier at the baseband can achieve an improved linearity performance within a wide bandwidth [31]. Fig. 3.15 shows the single-stage I/Q baseband amplifier employed in this work. The frequency response is optimized and the power consumption is 12 mW. The simulated receiver-mode 3-dB RF bandwidth is from 55.9 GHz to 67.6 GHz.

To improve the SNDR of the receiver, a linearity-enhanced double-balanced active mixer based on the current-bleeding technique [47] is adopted in this work (Fig. 3.16). A reasonable power budget for the LO path can be realized with the current-mode switching. As shown in Fig. 3.16, a 3-pF capacitor and a 1.2-Mohm bias resistor are applied to maintain an AC coupling at the mixer output. However, an unreasonable settling time of larger than 3.5 μs will be required due to the charging time of the capacitor [31]. To support the low-latency requirement from the IEEE 802.11ay, two dummy transistors M7 and M8 are connected to the mixer output and kept on while the receiver is off. The small-size dummy transistors together with the common-mode feedback circuit will keep the output voltage unchanged with a power consumption of only 0.5 mW. Furthermore, the baseband amplifier is shut down with a VDD switch instead of any gate-bias tuning. Fig.

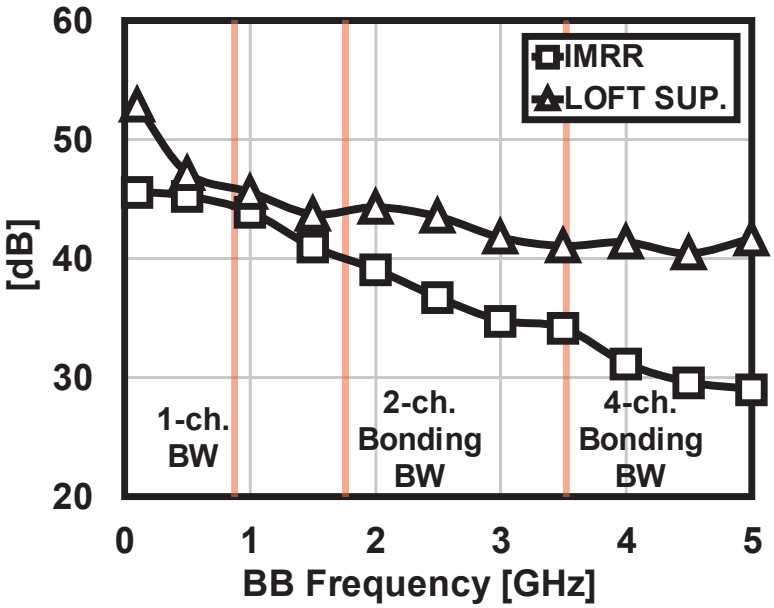


Figure 3.24: Measured LOFT suppression and IMRR over the baseband frequency.

3.17 shows the measured receiver output with a single-tone input (500-MHz at baseband). The receiver is switched on at 0 ns. The measured startup time for the receiver is less than 20 ns.

Regarding the increased input noise floor due to the bandwidth, a 5-stage TL-based LNA is employed in this work to suppress the noise. The circuit schematic is shown in Fig. 3.18. The input shunt-stab matching is shorted to ground for the purpose of electro-static discharge (ESD) protection. Two I/Q coupled-line baluns optimized by the electromagnetic (EM) simulation are inserted to transform the single-ended signal into differential.

3.3 Measurement Results

The 60-GHz transceiver with the calibration block is fabricated in a standard 65-nm C-MOS technology. Fig. 3.19 shows the die micrograph. The chip size is 3 mm x 2 mm with a core area of 2.81 mm^2. Core area for each block is summarized in the Table 3.1. The proposed on-chip calibration block occupies an area of less than 0.2 mm^2, which is area-efficient. Fig. 3.20 shows the 60-GHz RF PCB for measurement. The chip is silver-epoxy glued in the center of the PCB and connected to the 50-ohm transmission line with bonding wires. A bonding wire inductance of 0.5-nH is considered in the simulation. The

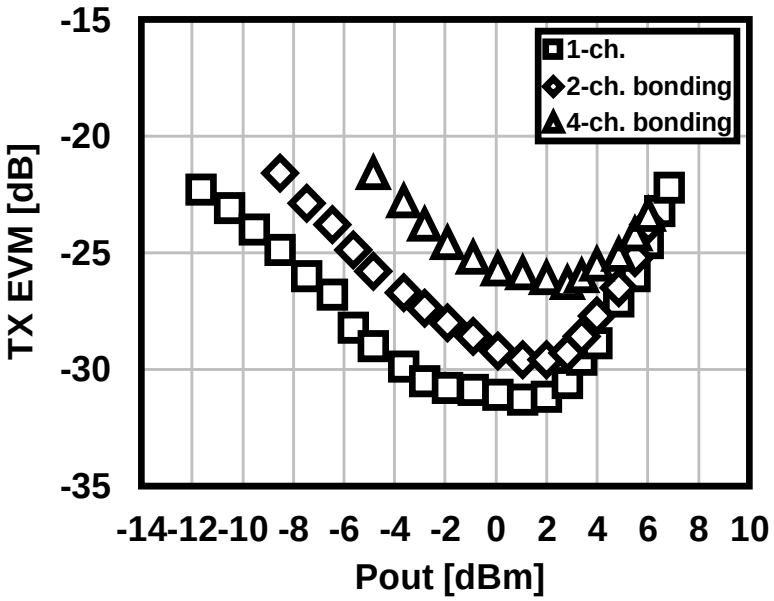


Figure 3.25: Measured TX EVM with 1-channel, 2-channel and 4-channel bonding bandwidth in 60 GHz band.

DC supply and the control signals for the on-chip logic are sent from the pin connectors. The insertion loss of the PCB is measured by comparing the saturated output power of a PCB in transmitter mode and a stand-alone PA. A PCB loss of 9.8 dB is observed at 61.56 GHz.

Fig. 3.21(a) shows the conversion gain of the TX excluding the PCB loss. The conversion gain is around 12.5 dB. To support the IEEE 802.11ay standard, the TX is required to cover the four channels defined in the 60-GHz band. The measured gain has a 4.5-dB variation over the entire 8.64-GHz bandwidth with a carrier frequency of 61.56 GHz (ch. 2.5). Fig. 3.21(b) shows the measured TX output power against the input power. The measured TX saturated output power is 10.8 dBm excluding the PCB loss. The measured output P_{1dB} for the TX is 6.5 dBm. Fig. 3.21(c) shows the measured output power, third-order intermodulation power (IM3) and output noise floor for the RX PCB. The LO frequency is 61.56 GHz while the input frequency is 61.66 GHz. The SNDR of the RX is calculated regarding the measured IM3 and noise floor with different bandwidth conditions (Fig. 3.21(d)). The calculated peak SNDRs are 33.5 dB, 31.6 dB, and 29.8 dB for 1-channel, 2-bonded channel, and 4-bonded channel, respectively. The measured phase noise at ch.2 is -93 dBc/Hz with a 1-MHz offset [32].

Fig. 3.22(a) shows the equipment setup for the TX EVM measurement. One PCB in transmitter mode with a 36-MHz onboard reference is used in this measurement. Fig.

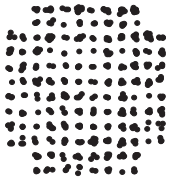
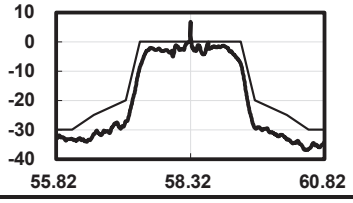
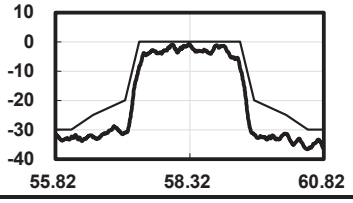
	Before cal.	After cal.
Carrier freq. BW.	58.32GHz 1.76GHz	58.32GHz 1.76GHz
Modulation	128QAM	128QAM
Data rate	-	12.32Gb/s
Constellation		
Spectrum		
TX EVM	-19.5dB	-28.7dB
TX-to-RX EVM	-	-27.2dB

Figure 3.26: Measured TX and TRX performance at channel 1 before and after the calibration in SC mode.

3.22(b) shows the measurement setup for TX-to-RX EVM. Two PCBs with two 14-dBi horn antennas are used in this measurement. One operates in transmitter mode and the other operates in receiver mode. During the measurement, the TX and RX are tested in SC mode. For both TX and TX-to-RX measurement, the baseband signal is generated by an arbitrary waveform generator (Keysight AWG M8195A). Modulated baseband signals with the symbol rate of 1.76 GSymol/s for a 1-ch. bandwidth, 3.52 GSymbol/s for a 2-bonded channel and 7.04 GSymbol/s for a 4-bonded channel are generated. The corresponding roll-off factor is 0.25. The TX output spectrum is observed with a down-conversion mixer and a spectrum analyzer (Keysight E4448A). An oscilloscope (DSA91394A) with an adaptive equalizer is used for the EVM measurement.

The TX calibration performance is also evaluated with the setup shown in Fig. 3.22(a). A single-tone baseband signal of 107 MHz is generated from the AWG for the calibration. The LO frequency is 61.56 GHz. In this condition, frequencies of the corresponding RF signal, LOFT and image signal are 61.453 GHz, 61.56 GHz and 61.667 GHz, respectively. During the calibration period, the output codes of the calibration ADCs will be sent to a

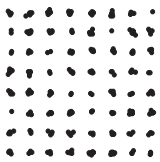
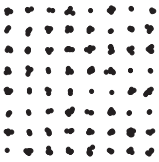
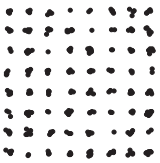
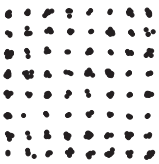
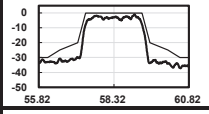
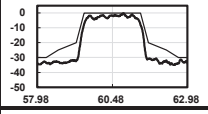
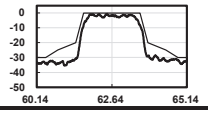
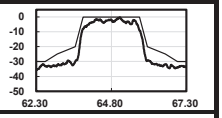
Channel/ Carrier freq.	ch.1 58.32GHz	ch.2 60.48GHz	ch.3 62.64GHz	ch.4 64.80GHz
Modulation	64QAM			
Data rate	10.56Gb/s	10.56Gb/s	10.56Gb/s	10.56Gb/s
Constellation				
Spectrum				
TX EVM	-30.3dB	-30.0dB	-29.3dB	-28.4dB
TX-to-RX EVM	-28.2dB	-27.0dB	-25.2dB	-27.1dB
Distance	0.15m	0.15m	0.14m	0.14m

Figure 3.27: Measured performance in 64-QAM within the channels defined in IEEE 802.11ad.

microprocessor and a gradient descent algorithm is applied to search for the best bias value. Finally, the feedback control code will be sent back to the chip for calibration. Fig. 3.23 shows the measured $Signal\,Strength''$ calculated from the output codes of the I/Q ADCs. The ADC_{I}, ADC_{Q} and ADC_{I0}, ADC_{Q0} in the equation stand for the output codes with and without RF input for the calibration block, respectively. The TX output power is fixed with -5 dBm in this measurement. As shown in the figure, The LOFT and the image signal level less than -50 dBc can still be detected by the proposed circuit. The calibrated LOFT suppression and IMRR over the channel-bonding conditions are measured and shown in Fig. 3.24. The LOFT suppression is always higher than 40 dB within the 4-bonded channel. The IMRR of TX is better than 44.5 dB, 40.0 dB, and 34.2 dB for 1 channel, 2-bonded channel, and 4-bonded channel, respectively. The influence of FD-IMRR after an RF domain calibration can be obviously observed from this result. One important reason for the observed FD-IMRR is because of the frequency-dependent mismatch caused by the RF PCB and the baseband cables. Fig. 3.25 demonstrates the TX 64-QAM EVM after calibration against the average output power. In the left region

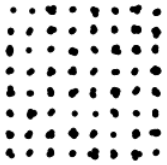
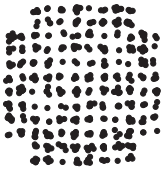
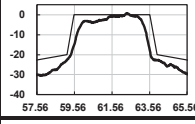
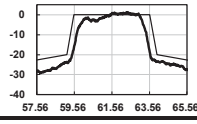
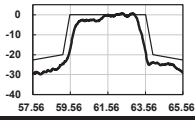
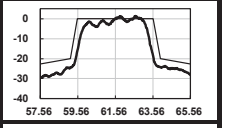
Carrier freq. BW.	61.56GHz 2-ch. bonding	61.56GHz 2-ch. bonding	61.56GHz 2-ch. bonding	61.56GHz 2-ch. bonding
Modulation	QPSK	16QAM	64QAM	128QAM
Data rate	7.04Gb/s	14.08Gb/s	21.12Gb/s	24.64Gb/s
Constellation				
Spectrum				
TX EVM	-29.7dB	-29.5dB	-29.8dB	-27.1dB
TX-to-RX EVM	-26.6dB	-27.3dB	-27.5dB	-26.1dB
Distance	1.06m	0.40m	0.10m	0.03m

Figure 3.28: Summarization of 2-channel bonding performance at ch.2.5 defined in IEEE 802.11ay.

of the traces, The EVMs are dominated by the output noise floor. While, in the right region, the EVMs are limited by the IM3. Thanks to the high-accuracy calibration, the minimum EVMs of the TX in 64-QAM are 31.3 dB, 29.8 dB, and 26.3 dB for 1 channel, 2-bonded channel, and 4-bonded channel, respectively. The peak EVM for the 4-ch. bonding condition is degraded in the figure, which is due to the increased bandwidth. By optimizing the transmitter-path NF, the peak EVM can be improved.

A similar calibration is performed at ch.1 (carrier frequency: 58.32 GHz). Fig. 3.26 compares the spectrum and constellation in 128-QAM before and after the calibration. Large LOFT at 58.32 GHz can be observed from the spectrum before calibration, which cannot satisfy the spectrum emission mask requirement. After the calibration, the LOFT and the image signal are suppressed. A TX EVM improvement of 9.2 dB is achieved. The RX IMRR calibration in this work is performed by adjusting the RX I/Q VGA and QILO. The corresponding TX-to-RX EVM after the calibration within a 2.16-GHz (1-channel) bandwidth is -26.0 dB in 128-QAM, which satisfies the requirement for a BER of less than 10^{-3}. A data rate of 12.32 Gb/s in 128-QAM is realized by the transceiver.

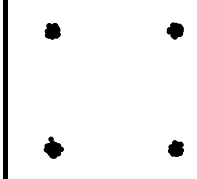
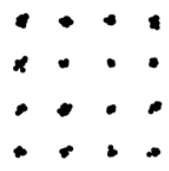
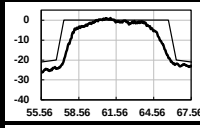
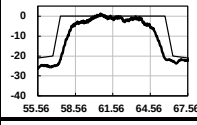
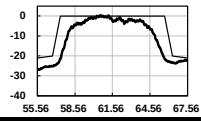
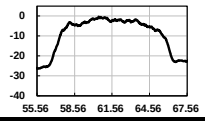
Carrier freq. BW.	61.56GHz 4-ch. bonding	61.56GHz 4-ch. bonding	61.56GHz 4-ch. bonding	61.56GHz 10.44GHz
Modulation	QPSK	16QAM	64QAM	64QAM
Data rate	14.08Gb/s	28.16Gb/s	42.24Gb/s	50.10Gb/s
Constellation				
Spectrum				
Pout	8.3dBm	8.3dBm	7.7dBm	-
TX EVM	-26.3dB	-26.3dB	-26.3dB	-24.0dB
TX-to-RX EVM	-24.5dB	-24.6dB	-24.3dB	-23.2dB
Distance	0.54m	0.24m	0.04m	0.04m

Figure 3.29: Summarization of 4-channel bonding performance at ch.2.5 defined in IEEE 802.11ay.

The IEEE 802.11ay standard demands the coexistence with the existing IEEE 802.11ad standard. As a result, channels defined in IEEE 802.11ad (ch.1 to ch.4) are supposed to be supported by the proposed transceiver. Fig. 3.27 summarizes the measured spectrum, constellation, TX EVM and TX-to-RX EVM in 64-QAM for each channel. The EVMs are measured in SC mode. The measured peak TX EVMs in 64-QAM are better than -28.4 dB. Furthermore, the TX output spectrums satisfy the required spectrum emission mask. The measured peak TX-to-RX EVMs in 64-QAM are -28.2 dB, -27.0 dB, -25.2 dB and -27.1 dB for ch.1, ch.2, ch.3 and ch.4, respectively. The maximum communication distance is defined by the required TX-to-RX SNRs for a BER of 10^{-3}, which are -9.8 dB for QPSK, -16.5 dB for 16-QAM, -22.5 dB for 64-QAM and -25.5 dB for 128-QAM. Data link of 10.56 Gb/s in 64-QAM is maintained from ch.1 to ch.4 with further than 0.14-m communication distance. A 2.5-m communication distance is achieved at ch.1 in QPSK.

Fig. 3.28 and Fig. 3.29 demonstrate the summarized channel bonding performance

at ch.2.5. Within a 2-channel bonding bandwidth, the TX after calibration achieves TX EVMs of -29.7 dB, -29.5 dB, -29.8 dB and -27.1 dB in QPSK, 16-QAM, 64-QAM and 128-QAM, respectively. The maximum data-rate realized with a 2-bonded channel is 24.64 Gb/s in 128-QAM. The corresponding TX-to-RX EVM is -26.1 dB. The measured maximum distances with a 2-bonded channel are 1.06 m for QPSK, 0.40 m for 16-QAM, 0.10 m for 64-QAM and 0.03 m for 128-QAM. Regarding a 4-channel bonding condition, the transceiver in this work supports data-links of 14.08 Gb/s in QPSK, 28.16 Gb/s in 16-QAM and 42.24 Gb/s in 64-QAM. The corresponding TX-to-RX EVMs are -24.5 dB in QPSK, -24.6 dB in 16-QAM and -24.3 dB in 64-QAM. For both 2-ch. bonding and 4-ch. bonding conditions, the output spectrums satisfy the spectrum emission masks from the IEEE 802.11ay. The non-flatness of the spectrum is mainly from the 5-stage PA and the measurement equipment. The measured maximum data-rate is 50.1 Gb/s in 64-QAM with an RF bandwidth of 10.44 GHz. The corresponding TX EVM and TX-to-RX EVM are -24.0 dB and -23.2 dB, respectively. A communication distance of 0.04 m is achieved in this condition.

Table 3.2 shows the power consumption breakdown of the transceiver. The analog and digital supply voltages are 1 V in this work. The proposed calibration block consumes 3.1 mW during the calibration period. The power consumption of the transceiver in TX mode is 169 mW including the PLL and the calibration block. The measured RX mode power consumption is 139 mW with the PLL.

Table 3.3 compares this work with the state-of-the-art 60 GHz CMOS transceiver frontends. This work presents the first 60-GHz transceiver achieving 4-channel bonding in 64-QAM with a single-element transceiver. An equivalent data-rate of 42.24 Gb/s is realized with a low power consumption. Furthermore, this work is the first-reported transceiver achieving 128-QAM in the 60 GHz band. Data-rate of 24.64 Gb/s in 128-QAM is available with 2-channel bonding.

3.4 Conclusion

This chapter presents a 60-GHz CMOS transceiver designed for the IEEE 802.11ay standard. A calibration block for LOFT and I/Q imbalance featuring high-accuracy and low-power is implemented with the transceiver. The RF building blocks are optimized for high SNDR and flat gain response. The proposed transceiver supports the channels defined in the existing IEEE 802.11ad standard together with the bonded channels defined in the IEEE 802.11ay standard. This work reports the first 128-QAM 60-GHz transceiver. Additionally, a 4-channel bonding data-rate of 42.24 Gb/s in 64-QAM is also available. A maximum data-rate of 50.1 Gb/s in 64-QAM is realized, which is the highest

data-rate achieved by using the 60-GHz band. Compared with the conventional 60-GHz transceivers realizing 4-ch. bonding in 64-QAM, the proposed work realizes an area-efficient and power-efficient design with the single-element transceiver implementation. Short-range ultra-high-speed data communication for the next generation WLAN could be achieved.

Table 3.3: Performance Comparison of 60-GHz Transceivers

	Data rate/ Modulation	TX-to-RX EVM	Pout/ant. path	Integration	Power Consumption
[10]	2.5Gb/s QPSK	-22.0dB 1 ch. (TX only)	2.0dBm at TX EVM=-22.0dB	90nm, direct conversion, TX, RX, LO, antenna, analog BB, dig. BB.	TX: 347mW RX: 274mW
[11]	4.6Gb/s 16QAM	-19.5dB 1 ch.	-4.0dBm* at TX EVM=-21.0dB	40nm, 16-array heterodyne, TX, RX, LO, analog BB, dig. BB.	TX: 1190mW RX: 960mW 16x16 array
[12]	4.6Gb/s 16QAM	-20.5dB 1 ch.	-2.0dBm at TX-to-RX EVM =-22.0dB	28nm/40nm, 144-array, heterodyne, TX, RX, LO, analog BB, dig. BB	TX: 8400mW RX: 6600mW 144-element
[13]	28.16Gb/s 16QAM 4-ch. bonding	-26.3dB 1 ch.	8.5dBm at TX EVM=-21.0dB	65nm, direct conversion, TX, RX, LO.	TX: 251mW RX: 220mW
[14]	27.8Gb/s 16QAM	-18.0dB	N.A.	28nm, digital polar TX, direct conversion RX, TX, RX, LO, w/o PLL.	TX: 210mW RX: 110mW
[15]	21.12Gb/s +21.12Gb/s 2ch. bonding	-24.0dB (LB) -23.0dB (HB)	7.0dBm at TX EVM=-22.0dB	65nm, direct conversion, 2TX, 2RX, 2LO.	TX: 544mW RX: 432mW
[27]	7Gb/s 16QAM	-20.4dB 1 ch.	6dBm* at TX EVM=-23dB	28nm, 4-element, direct conversion, TX, RX, LO.	TX: 670mW RX: 431mW 4-element
This Work	12.32Gb/s 128QAM 1 ch.	-27.2dB 1 ch.	7.3dBm at TX EVM=-22.0dB	65nm, direct conversion, TX, RX, LO.	TX: 169mW RX: 139mW
	24.64Gb/s 128QAM 2-ch. bonding	-26.1dB 2-ch. bonding			
	42.24Gb/s 64QAM 4-ch. bonding	-24.3dB 4-ch. bonding			
	50.10Gb/s 64QAM 10.44GHz BW.	-23.2dB 10.44 BW.			

* estimated from the material.

Chapter 4

Area-Efficient Bi-Directional Transceiver

As mentioned in Chapter 2, the millimeter-wave spectrum suffers from an enlarged FSPL. As a result, beamforming technique is usually utilized for extending the communication distance. Considering the middle-range scenarios like streaming 8K UHD movies at smart home, large-sized transceiver array will be required. An increased number of antennas and element-transceivers will be necessary for supporting such a phased-array system. Moreover, the MIMO technique utilizing the spacial multiplexing is also essential for the future IEEE 802.11ad/ay. Additional antennas and element-transceivers will also be induced from the MIMO configuration. Regarding both of the situations mentioned above, the system size, weight along with the manufacturing cost will be greatly increased. Design considerations will be mandatory for a compact system size and a reduced system cost.

Chapter 3 introduces a CMOS IEEE 802.11 ad/ay transceiver with LOFT and I/Q imbalance calibration. The data rate in a short-range communication could be significantly improved with suppressed power and area consumptions. However, when further implement the transceiver presented in Chapter 3 to the array applications, the separated transmitter and receiver antennas will significantly increase the system size and weight. [48] introduces a two-element transceiver chip supporting the dual-polarized MIMO operation. A maximum data rate of 27.8 Gb/s is achieved by adding up two simultaneous data-streams through the H and V polarizations of the dual-polarized antennas, respectively. Although a TRX switch is adopted in this work for antenna sharing, the separated circuit chains designed for the transmitter and the receiver still occupy a redundant area. The manufacturing cost will be in turn increased. To reduce the manufacturing cost along with the system size and weight, the bi-directional technique could be applied for the

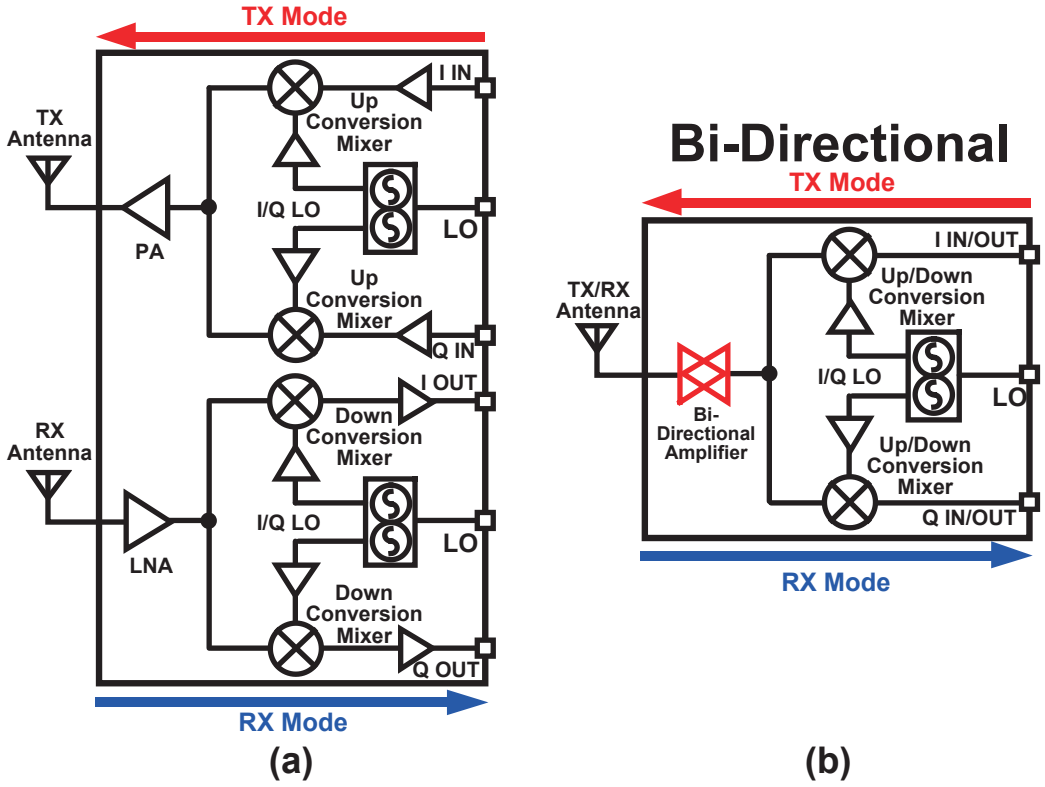


Figure 4.1: Block diagrams of (a) conventional 60-GHz direction-conversion transceiver and (b) bi-directional transceiver.

IEEE 802.11ay MIMO systems [49–52]. Usually, the bi-directional transceivers utilize a bi-directional amplifier to entirely share the mixer and the LO distribution between the transmitter and the receiver modes. As a result, the required on-chip area for a single-element transceiver could be decreased to almost half theoretically.

In this chapter, a CMOS two-element transceiver chip designed based on a bi-directional architecture will be introduced. The proposed gain-boosted bi-directional amplifier further allows the sharing of interstage passive components. With the help of the designed PA-LNA, the required area for a single-element transceiver in this work is 3 mm^2 including the pads. The proposed bi-directional transceiver in TX-mode achieves an EVM of -26 dB with -4.2-dBm output power. The measured RX-mode NF is 4.8 dB at 62.56 GHz. The maximum raw data rate realized by this work is 28.16 Gb/s in 16-QAM with a four-bonded channel. A two-channel-bonding data rate of 21.12 Gb/s in 64-QAM is also achieved. As a result, this work provides a high performance solution with minimized system size and manufacturing cost for the next generation WLAN.

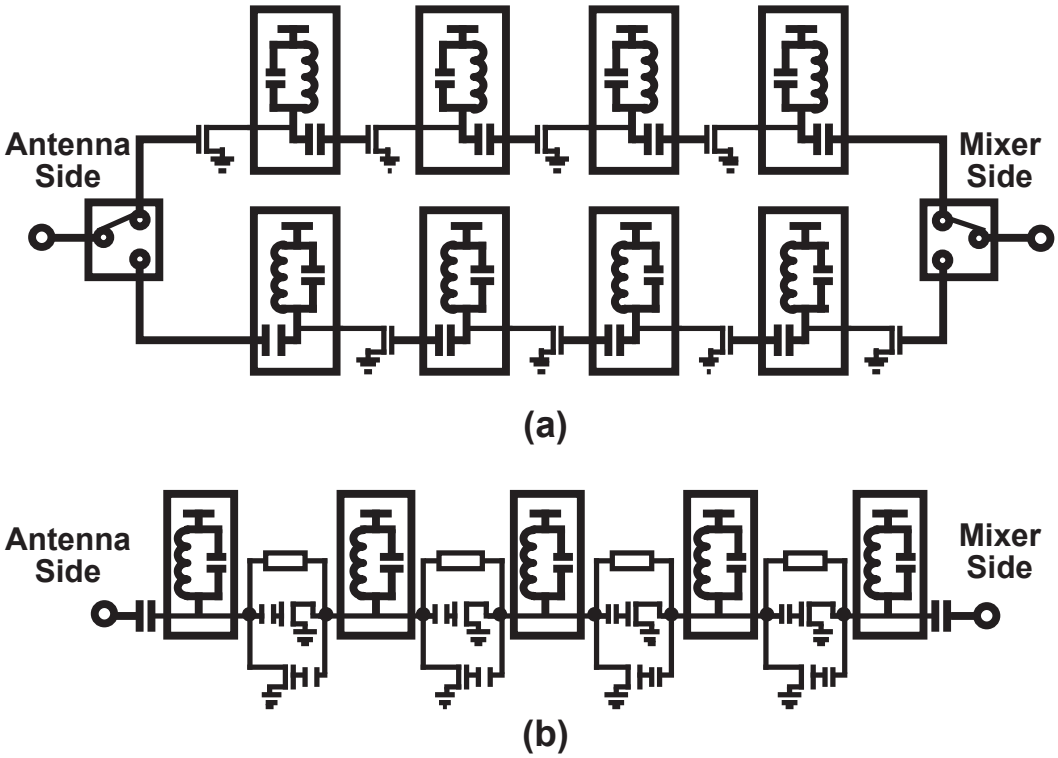


Figure 4.2: Circuit schematics of (c) conventional bi-directional amplifier and (d) proposed bi-directional amplifier.

4.1 Proposed Bi-Directional Architecture

To decrease the manufacturing cost and system size, an area-efficient design will be strongly demanded by the IEEE 802.11ay transceivers. Fig. 4.1 (a) shows the block diagram of a 60-GHz conventional direct-conversion transceiver [30]. The manufacturing cost along with the physical size of the system will be significantly increased due to the increased number of antennas and the enlarged chip area. For middle range communication scenarios like streaming the 8K UHD movies, the beamforming technique is usually applied for extending the communication range. The required size and cost will become even larger for an IEEE 802.11ay phased-array transceiver.

To suppress the manufacturing cost and the system size, the bi-directional technique could be utilized. Fig. 4.1 (b) shows the block diagram of a direct-conversion transceiver based on the bi-directional architecture. The key component for such a transceiver is the bi-directional amplifier whose operating direction could be reconfigured by digital control signals. Fig. 4.2 (a) shows the conventional bi-directional amplifier [53]. By utilizing two

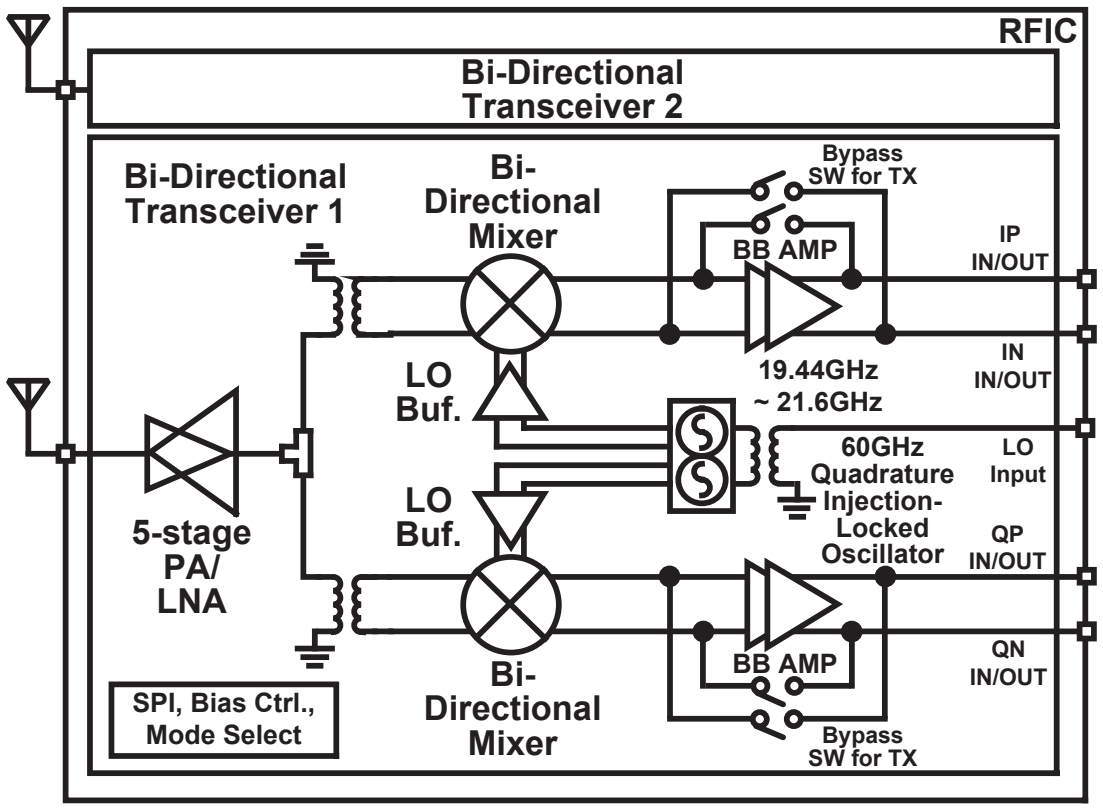


Figure 4.3: Block diagram of proposed bi-directional transceiver.

single-pole double-throw (SPDT) switches at the antenna side and the mixer side, respectively, the operating mode of the amplifier could be switched between the PA mode and the LNA mode. As a result, the antenna, up- and down-conversion mixers, and the LO generation could be completely shared between the TX and RX modes. Ideally, the on-chip area for the transceivers could be reduced to half with the help of the bi-directional technique. However, the area reduction achieved by a conventional bi-directional transceiver is much less than half due to the unshared interstage passive components of the conventional bi-directional amplifier. Considering the phased-array transceiver implementation where the mixer and the LO distribution only occupy a limited proportion of the total area consumption, the manufacturing cost of the conventional design will be increased significantly.

To further minimize the required area, Fig. 4.2 (b) shows the proposed bi-directional amplifier. In the proposed work, the transistors for TX and RX modes in each of the amplifier stages are connected. By controlling the gate bias, the bi-directional operation could be supported, and the passive components could be shared. However, additional

TX	Bi-Directional Mixer	PA	Board Loss	Total
Power Gain [dB]	-17.00	28.00	-9.80	
Cumulative Gain [dB]	-17.00	11.00	1.20	1.20
NF [dB]	17.00	9.00	9.80	
Cumulative NF [dB]	17.00	26.00	26.01	26.01
OIP3 [dBm]	2.00	7.80	100.00	
Cumulative OIP3 [dBm]	2.00	7.77	-2.03	-2.03

RX	Board Loss	LNA	Bi-Directional Mixer + BB Amp	Total
Power Gain [dB]	-9.80	20.00	-3.00	
Cumulative Gain [dB]	-9.80	10.20	7.20	24.08
NF [dB]	9.80	6.00	18.00	
Cumulative NF [dB]	9.80	15.80	16.43	14.77
OIP3 [dBm]	100.00	7.00	2.00	
Cumulative OIP3 [dBm]	100.00	7.00	-0.12	4.91

Figure 4.4: Level diagram design of the 60-GHz bi-directional transceiver.

insertion loss will arise due to the matching networks sharing. Considering the system requirements, such kind of RF-path gain degradation is usually not acceptable for a noisy millimeter-wave transceiver. Thus, the gain boosting technique [54–56] is utilized in the proposed design for compensating the RF-path conversion gain in both TX and RX modes. A minimized on-chip area along with an optimized system performance could be supported for the IEEE 802.11ay MIMO and beamforming systems.

As mentioned in Chapter 2, To maintain enough EVM for complex modulation schemes, the IEEE 802.11ay transceivers still need to address various design challenges. The enlarged channel bandwidth due to the channel-bonding not only results in a higher noise level but also demands a wider operating bandwidth for the RF frontend. Considering the modulation schemes such as 16-QAM or 64-QAM, careful design considerations regarding the system linearity and noise floor will be necessary for achieving an optimized EVM [31, 57]. Besides, as mentioned in Chapter 3, the direct-conversion transceivers suffer from the in-band LO leakage and image. The calibration circuits with high accuracy for compensating the I/Q imbalance and canceling the LO leakage are still essential [30, 45].

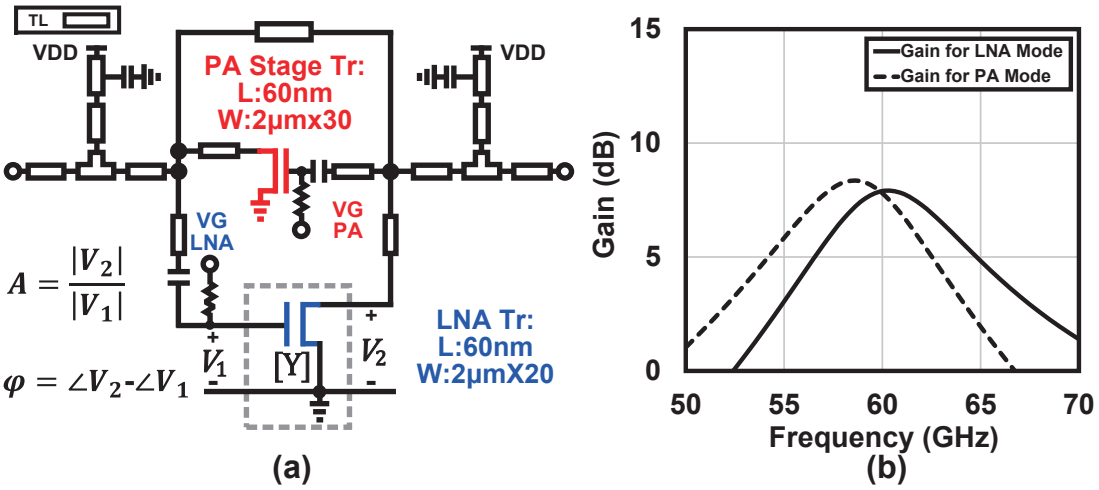


Figure 4.5: (a) Circuit schematic of single-stage bi-directional amplifier and (b) simulated gain in PA and LNA modes.

4.2 Circuit Implementation

Fig. 4.3 shows the block diagram of the proposed bi-directional transceiver chip. Direct-conversion topology is utilized in this work to reduce the system complexity. Entirely two transceiver elements are integrated into the same chip, which is capable of supporting the MIMO or beamforming configuration. Each of the element-transceivers consists of the PA-LNA, the I/Q bi-directional mixer, the QILO, the I/Q baseband amplifier for RX mode, and the bypass switches for TX mode. With the help of the 5-stage PA-LNA based on the proposed bi-directional technique, the I/Q mixers along with the I/Q LO generation could be entirely shared between the TX and RX modes. The required on-chip area for a single-element transceiver is reduced to half. Fig. 4.4 shows the level diagram design for the proposed 60-GHz bi-directional design. The system performance of the transceiver needs to be taken good care of regarding both the TX mode and RX mode. Complex modulation schemes such as 64-QAM and wide operation bandwidth are also considered in the system level design.

4.2.1 PA-LNA

Regarding the potentially degraded system noise and linearity performance, sharing the interstage matching for a multi-stage amplifier requires gain compensation. To increase the gain of a millimeter-wave amplifier, unilateralization technique has been widely utilized [58]. However, the theoretically gain achieved by the unilateralization technique is limited at high-frequency [56]. As a result, the gain of PA and LNA transistors in

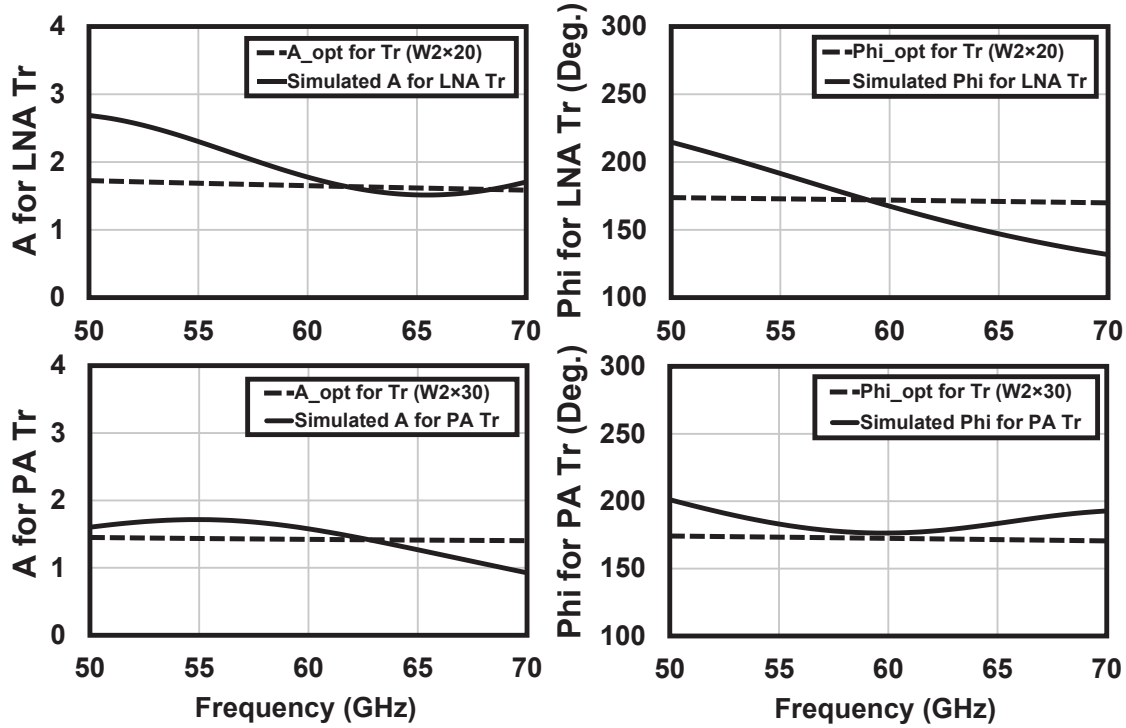


Figure 4.6: Simulated (a) A and (b) φ of PA and LNA transistors.

this work are boosted to the maximum achievable power gain [54]. Fig. 4.5 (a) shows the circuit schematic for a single-stage bi-directional amplifier. The PA- and LNA-mode transistors with different sizes are connected for sharing the interstage matching as mentioned in Section 4.1. The mode selection is realized by switching the gate bias VGTX and VGRX. To realize the maximum achievable gain, the A and φ defined in the figure for the single-stage amplifier after matching should satisfy the following requirements [54, 55].

$$A = A_{\text{opt}} = \frac{|Y_{12} + Y_{21}{}^{*}|}{2G_{22}} \tag{4.1}$$

$$\varphi = \varphi_{\text{opt}} = (2k+1)\pi - \angle(Y_{12} + Y_{21}{}^{*}) \tag{4.2}$$

where Y_{12} and Y_{21} are the 2-port Y parameters for the transistor in common-source connection. G_{22} in the equation is the real part of Y_{22} and k is an arbitrary integer. After adjusting the feedback TL along with the matching networks, Fig. 4.6 shows the simulated A and φ of the single-stage bi-directional amplifier and the calculated A_{opt} and φ_{opt} over frequency. Within the frequency range of 57.24 to 65.88 GHz, the simulated A and φ fit the calculated A_{opt} and φ_{opt} very well for both PA and LNA transistors, which ensures an optimized gain. Fig. 4.5 (b) shows the simulated gain for the single-stage bi-directional

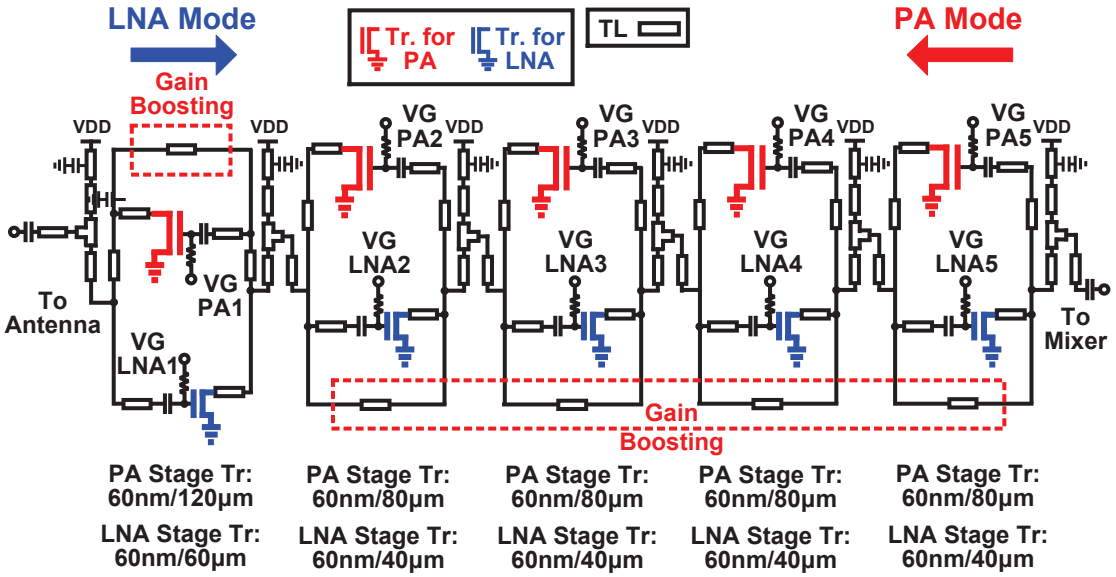


Figure 4.7: Circuit schematic of proposed five-stage PA-LNA.

amplifier. The achieved peak gains are 8.3 dB and 7.9 dB including the additional insertion loss due to the matching sharing for the PA mode and LNA mode, respectively.

Totally five of the proposed amplifier stages are utilized for the PA-LNA in this work. Fig. 4.7 shows the circuit schematic. The interstage matching networks are designed based on the area-efficient TLs. The characteristics of the TL are optimized with electromagnetic simulations. An accurate matching condition along with the minimized on-chip area could be realized. The antenna in this work is shared between the TX and RX modes for reducing the system size and weight. Fig. 4.8 shows the antenna sharing. To further minimize the required area, this work utilizes a TL-based antenna sharing network. The simulated insertion losses are 0.5 dB for the PA mode and 1.2 dB for the LNA mode at 60 GHz. One potential issue for the proposed antenna sharing network is the voltage swing generated by the PA transistor at the gate of the LNA transistor. The linearity of the PA will be degraded due to the triode-region resistance of the LNA transistor. As a result, the LNA-transistor gate-voltage swing during the PA mode are minimized during the design. In the simulation, the swing is always less than 240 mV at the PA operation point. To further improve the performance, a negative voltage bias could be applied for the LNA transistors during the PA mode.

Fig. 4.9 shows the measured characteristics of the PA-LNA. The proposed PA-LNA achieves around 15-dB gain in both PA and LNA modes. Within the frequency range of 57.24 to 65.88 GHz, the measured return losses of the antenna and mixer ports are always better than -9 dB in both PA and LNA modes. Fig. 4.10 shows the measured PA-mode

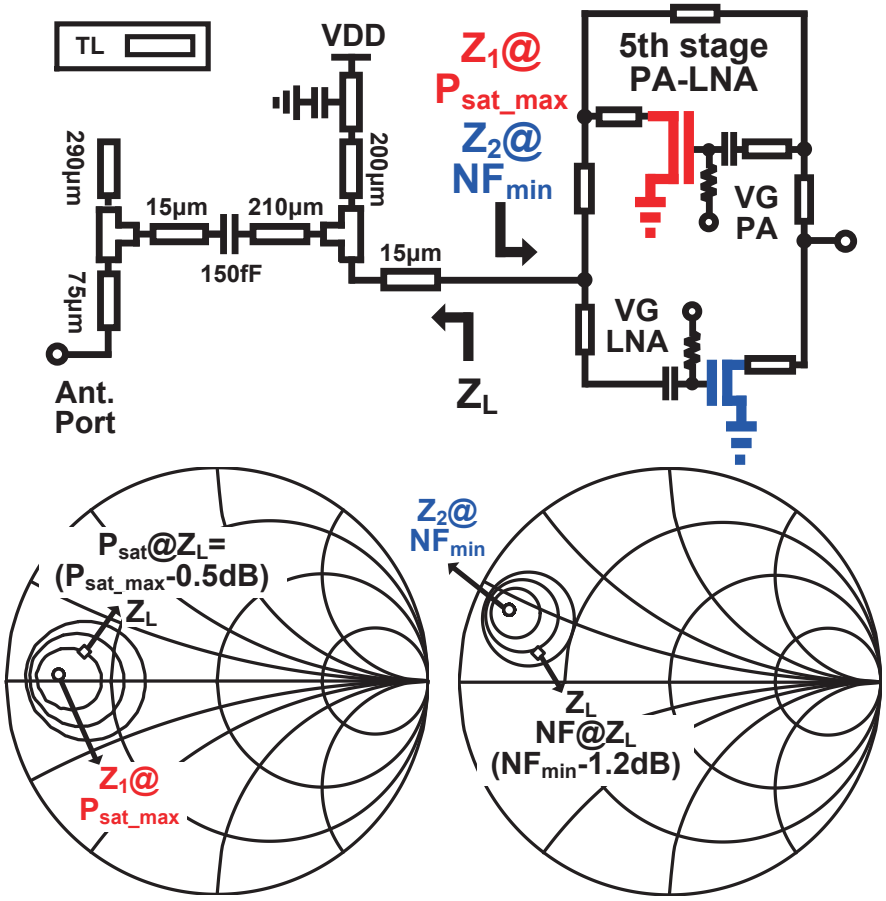


Figure 4.8: Antenna sharing for PA-LNA.

linearity and the LNA-mode NF. The measured NF in LNA mode is 4.2 dB at 61.56 GHz, while the measured saturated output power is 0 dBm in PA mode.

4.2.2 Bi-Directional Mixer and Baseband Amplifier

In addition to the PA-LNA, the area is further saved with an I/Q bi-directional mixer. This work utilizes a passive double-balanced mixer for both up- and down-conversion. The I/Q LO generation could be shared between the TX and RX modes with the help of the passive mixer.

Usually, the transmitters and receivers require different conversion gain levels. To increase the strength of the received signal, a higher conversion gain is demanded by the receiving chain. As a result, the I/Q baseband amplifiers are adopted in this work. The flipped-voltage-follower (FVF) topology baseband amplifier is usually utilized to achieve a high linearity within a wide bandwidth [31]. Fig. 4.11 shows the circuit schematic

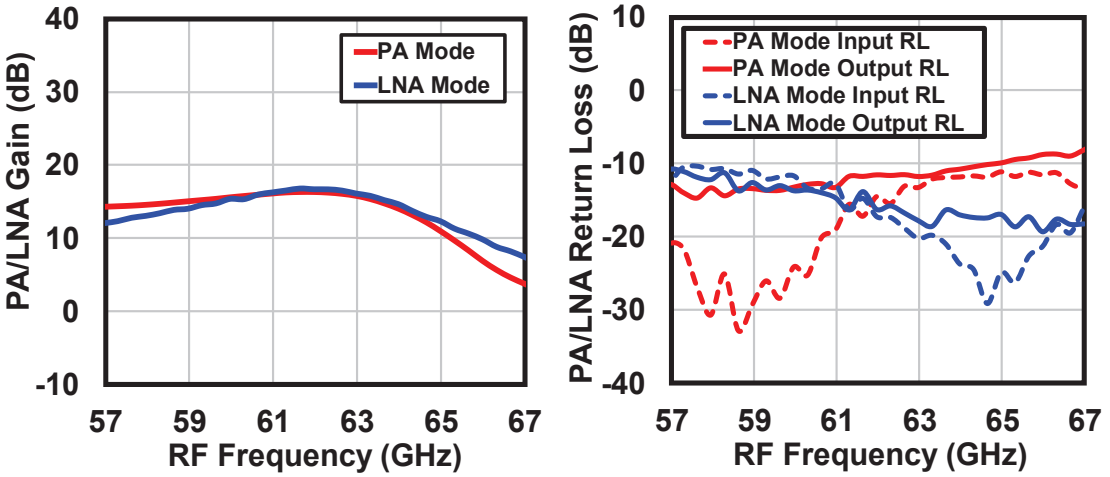


Figure 4.9: Measured (a) gain and (b) return loss of bi-directional amplifier.

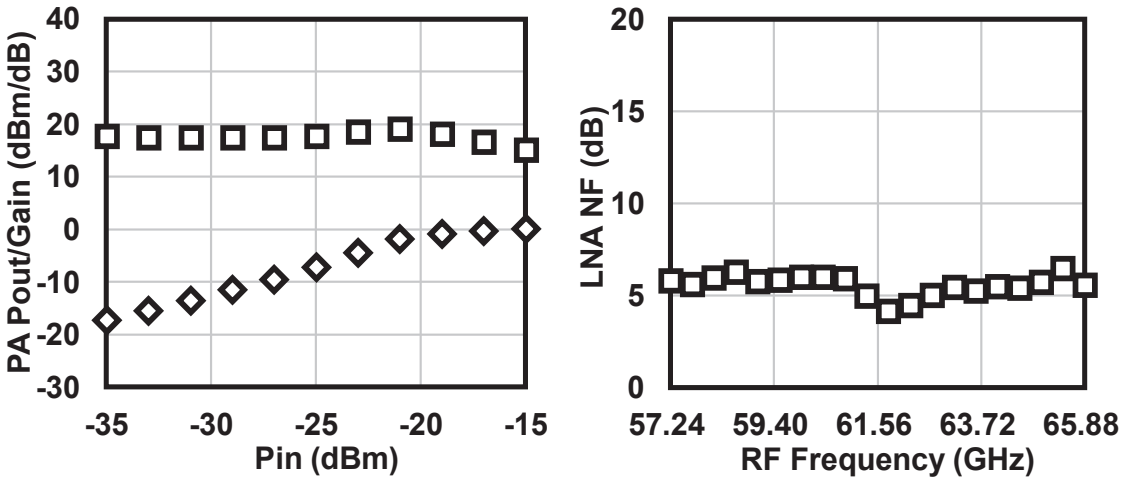


Figure 4.10: Measured (a) PA-mode output power and (b) LNA-mode noise figure of bi-directional amplifier.

of the amplifier unit, which consists of two amplifier stages. The first stage is a FVF amplifier with capacitor C_s for gain peaking. The second stage is usually in common-source topology [15, 31, 57]. However, the operating conditions for M3 and M7 will not be entirely the same due to the different drain-node voltages. The linearity of such an amplifier will be degraded. Additionally, because the voltage gain of the unit amplifier is determined by the mirror ratio of M3 (M4) and M7 (M8), and the impedance ratio between the output node and the source node of M1 (M2), the achievable gain will be limited by the r_{ds} of the common-source transistors. To improve the linearity and gain

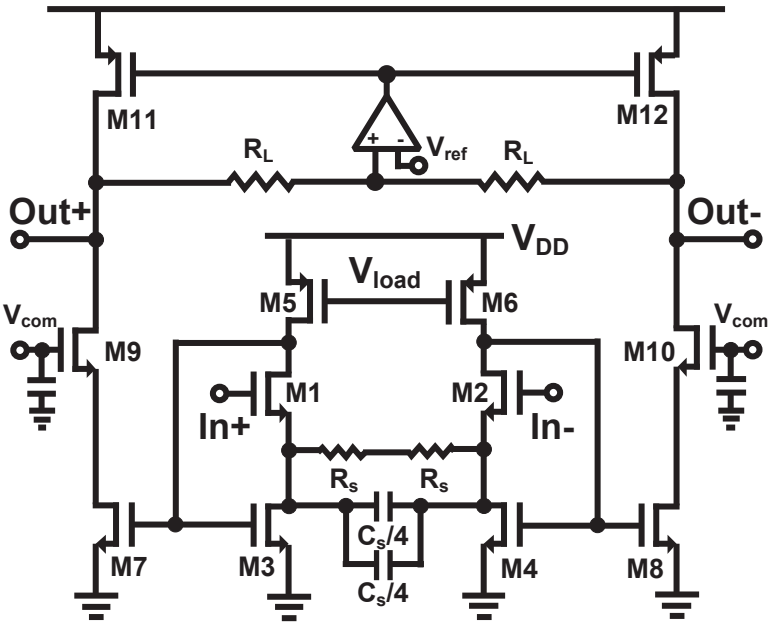


Figure 4.11: Circuit schematic for first stage of baseband amplifier.

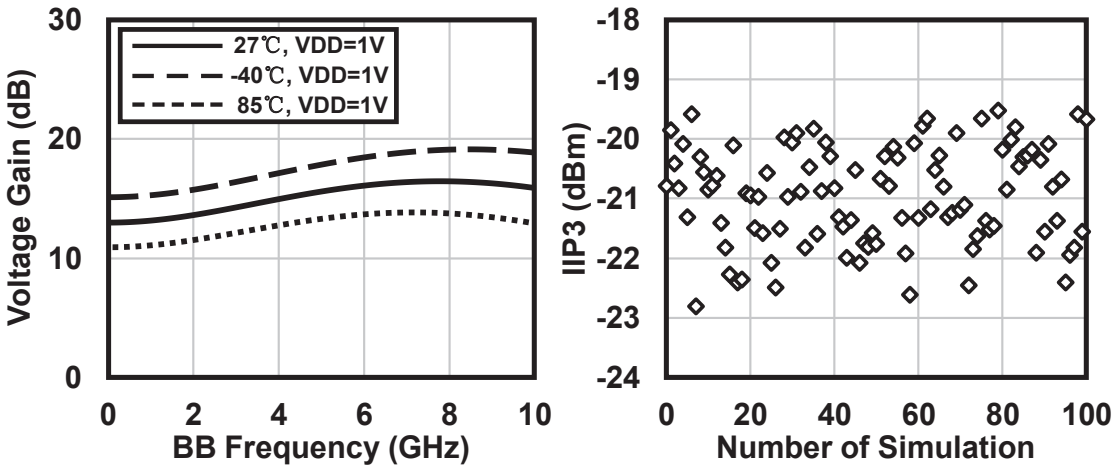


Figure 4.12: Simulated (a) voltage gain and (b) IIP3 of the baseband amplifier.

performance, this work adopts cascode topology for the second stage. When $g_{m9}r_{ds9} \gg 1$, the voltage gains of the second stage and the whole amplifier unit could be expressed with the following equations.

$$A_{V,2nd} \approx g_{m7} \cdot [(r_{ds7} \cdot r_{ds9} \cdot g_{m9}) /\!/ r_{ds11} /\!/ R_L] \tag{4.3}$$

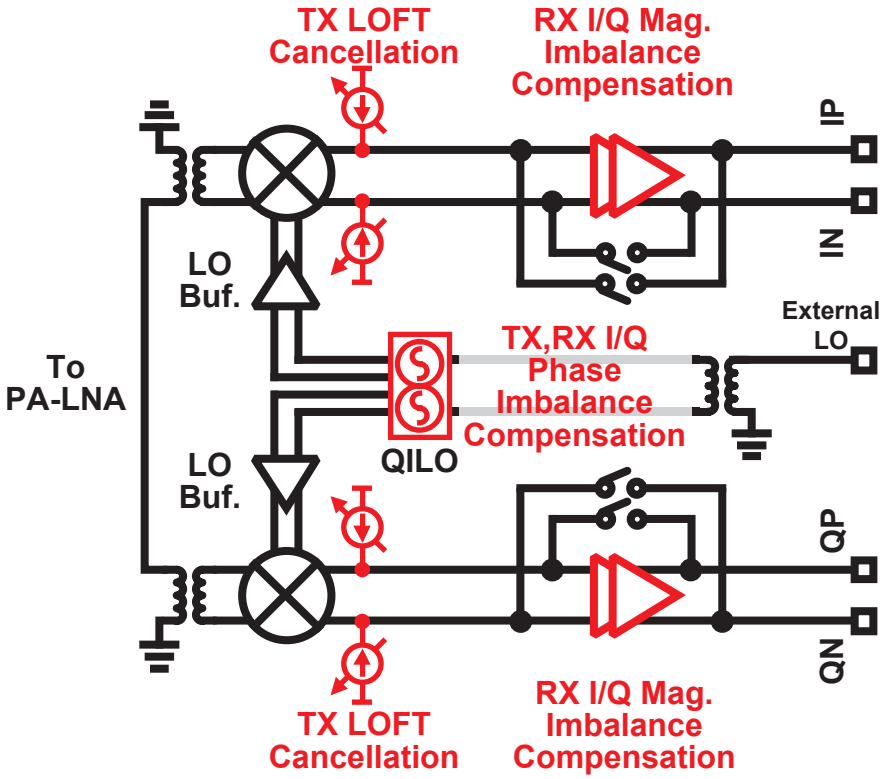


Figure 4.13: LO leakage and image cancellation.

$$A_{\mathrm{V,total}} \approx \frac{g_{\mathrm{m7}}}{g_{\mathrm{m3}}} \cdot \frac{(r_{\mathrm{ds7}} \cdot r_{\mathrm{ds9}} \cdot g_{\mathrm{m9}}) \,/\!/\, r_{\mathrm{ds11}} \,/\!/\, R_{\mathrm{L}}}{r_{\mathrm{ds3}} \,/\!/\, R_{\mathrm{S}} \,/\!/\, (1/j\omega C_s)} \tag{4.4}$$

Thanks to the cascode topology, the linearity could be improved by the replica biasing from M1 (M2) to M9 (M10). A larger R_{L} could also be selected for a higher gain. In this work, two of the amplifier units are used for the baseband amplifier. Fig. 4.12 (a) shows the simulated voltage gain with three different temperature conditions. The baseband amplifier achieves around 13-dB gain at 27°C. The gain variation due to the temperature is around 5 dB. Fig. 4.12 (b) shows the simulated IIP3 of the amplifier at 1 GHz in the Monte Carlo simulation. Regarding the random mismatch from the circuit, the simulated IIP3 falls in a range of -22.8 to -19.5 dBm. An improved gain performance along with optimized linearity is realized by the baseband amplifier. To support the bi-directional operation, switches are also implemented for bypassing the baseband amplifier in TX mode.

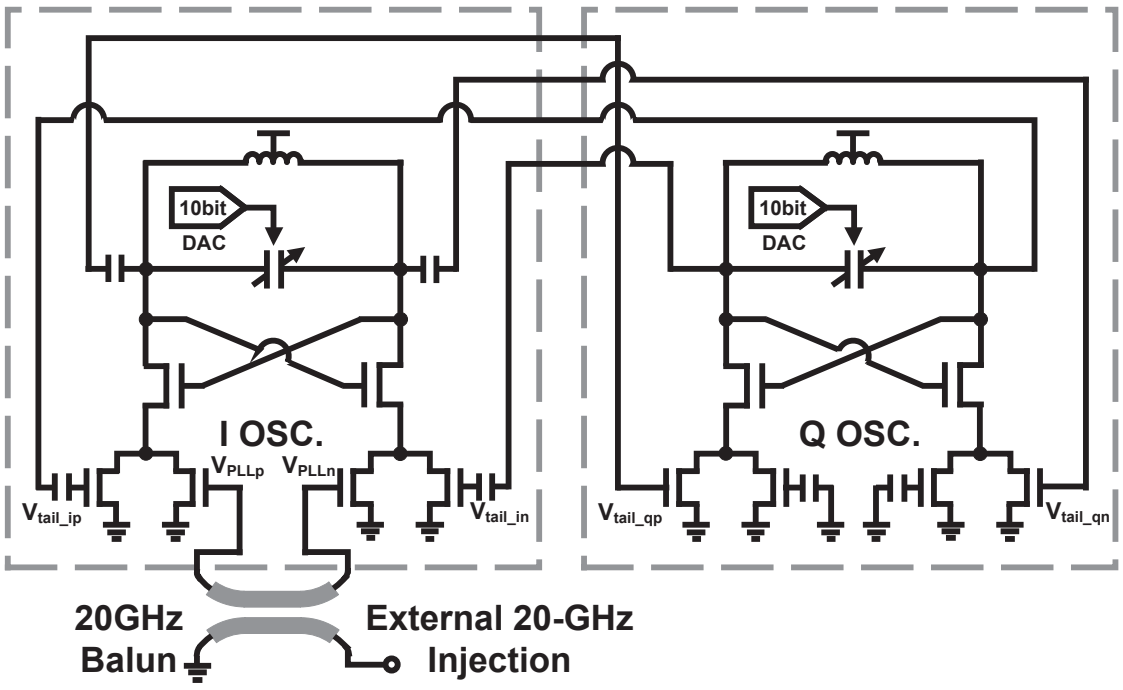


Figure 4.14: Circuit schematic of quadrature injection-locked oscillator with balun.

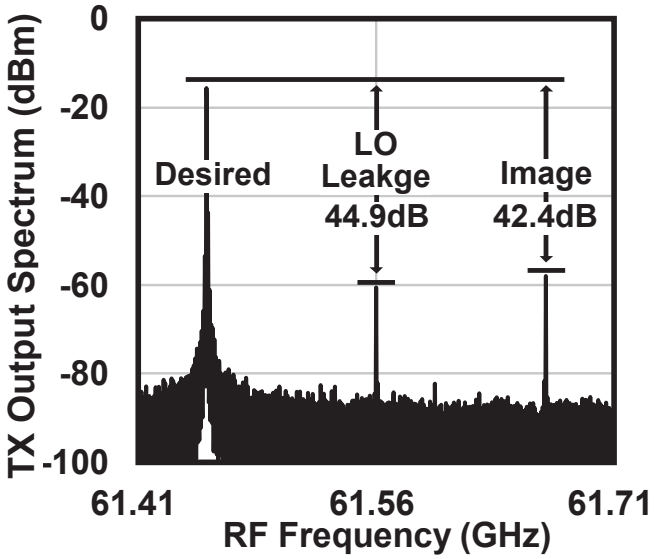


Figure 4.15: Measured TX-mode output spectrum before and after LO leakage and image cancellation.

4.2.3 LO Leakage and I/Q Imbalance Cancellation

As mentioned in Section 4.1, the LO leakage and the I/Q imbalance for a direct-conversion transceiver will limit the EVM performance. To suppress the LO leakage and compensate

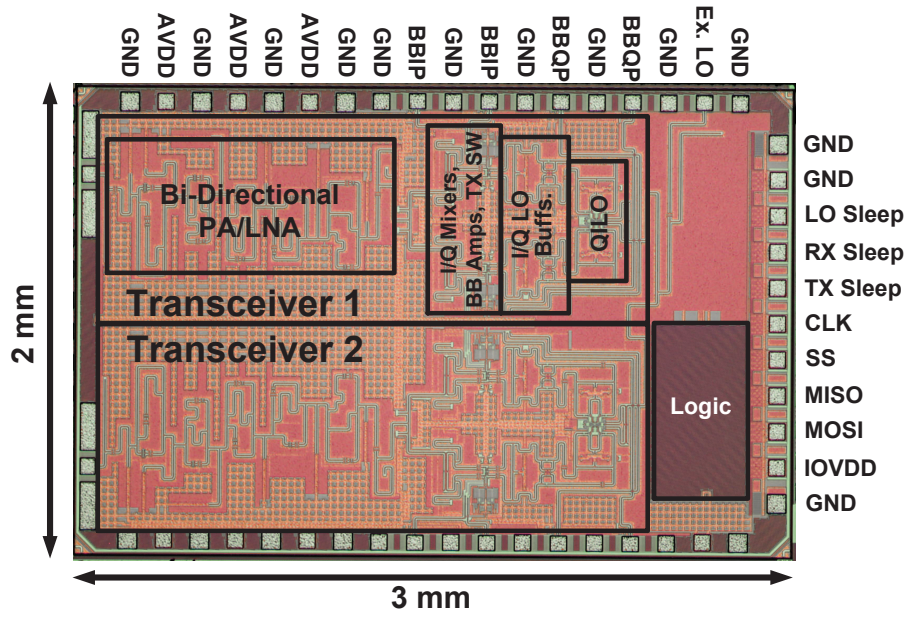


Figure 4.16: Die micrograph of proposed bi-directional transceiver chip.

the I/Q imbalance, an RF-domain calibration method similar to the proposal in Chapter 3 is utilized in this work [57]. Fig. 4.13 shows the block diagram for explaining the calibration. To cancel the LO leakage caused by the dc offset, two current sources controlled by 10-bit DACs are attached to the passive mixer [45]. A tuning step of less than 0.1 mV is realized. Regarding the I/Q imbalance, the RX-mode magnitude mismatch is calibrated by adjusting the I/Q baseband amplifiers while the TX-mode mismatch is compensated by tuning the I/Q baseband input power.

Fig. 4.14 shows the circuit schematic of the QILO for I/Q LO generation. The QILO in this work is designed to cover all the required LO frequencies from IEEE 802.11ay including the channel-bonding. The single-ended 20-GHz injection signal is generated from the external and transformed into differential by a 20-GHz on-chip coupled-line balun. With injection only to the I oscillator, the QILO in this work is capable of compensating the phase mismatch between I path and Q path. By controlling the free-run frequency of the I oscillator, a sub-degree phase tuning is realized [32].

Fig. 4.15 shows the measured TX-mode output spectrum of the proposed bi-directional transceiver. The frequencies of the LO and the baseband input signal are 61.56 GHz and 100 MHz, respectively. Larger than 40-dB suppression ratio could be achieved for both the LO leakage and the image signal.

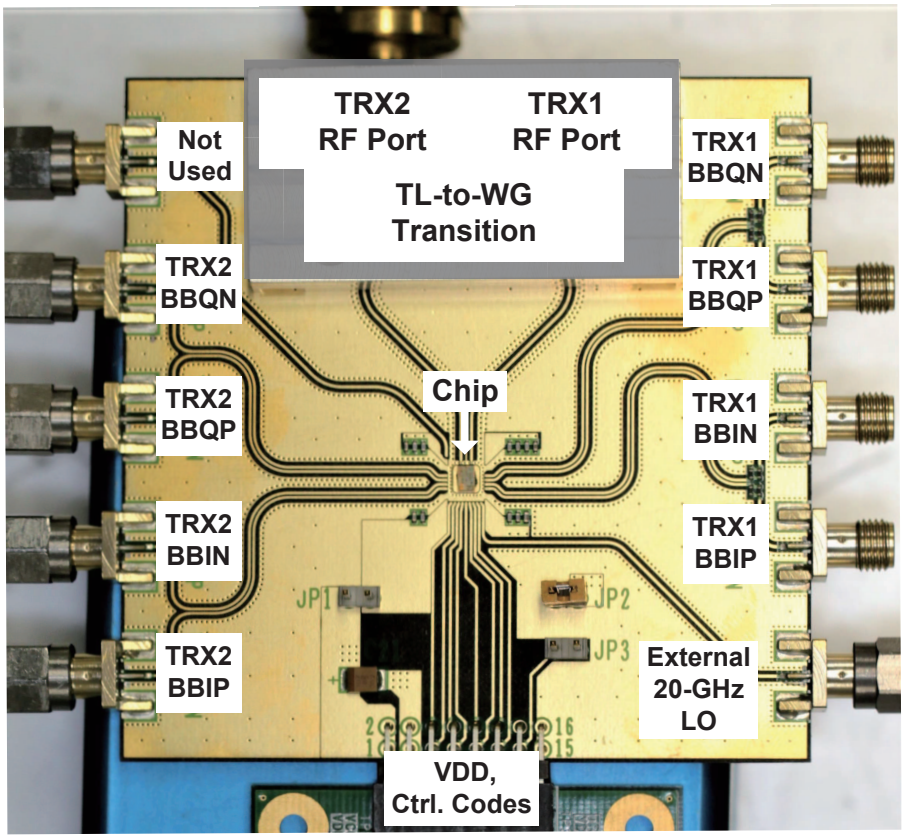


Figure 4.17: Photograph of RF PCB.

Table 4.1: Core Area of Blocks

Building Blocks	**Core Area** [mm^2]
PA-LNA	0.44
Bi-Directional Mixer	0.03
Baseband Amplifier	0.02
LO Buffer	0.07
QILO	0.12
Logic	0.29

4.3 Measurement Results

The proposed two-element bi-directional transceiver chip is fabricated in a standard 65-nm CMOS process featuring low manufacturing cost. The die micrograph and the pad assignment of the proposed chip are shown in Fig. 4.16. The chip size is 3 mm× 2 mm. Each of the element-transceivers occupies an area of 3 mm^2. Because the wire-bonding

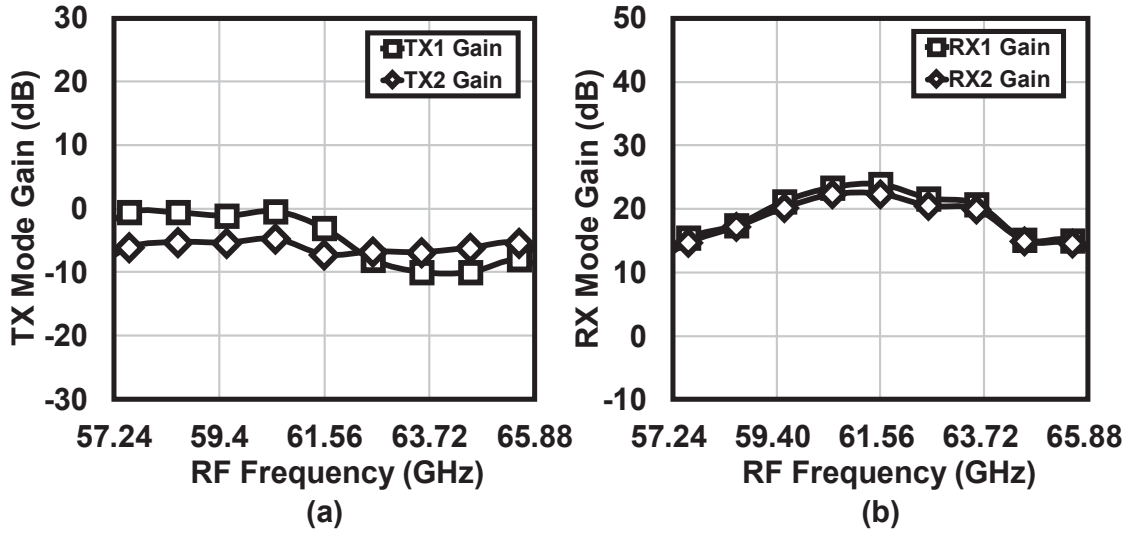


Figure 4.18: Measured characteristics of transceiver: (a) TX-mode gain, (b) RX-mode gain.

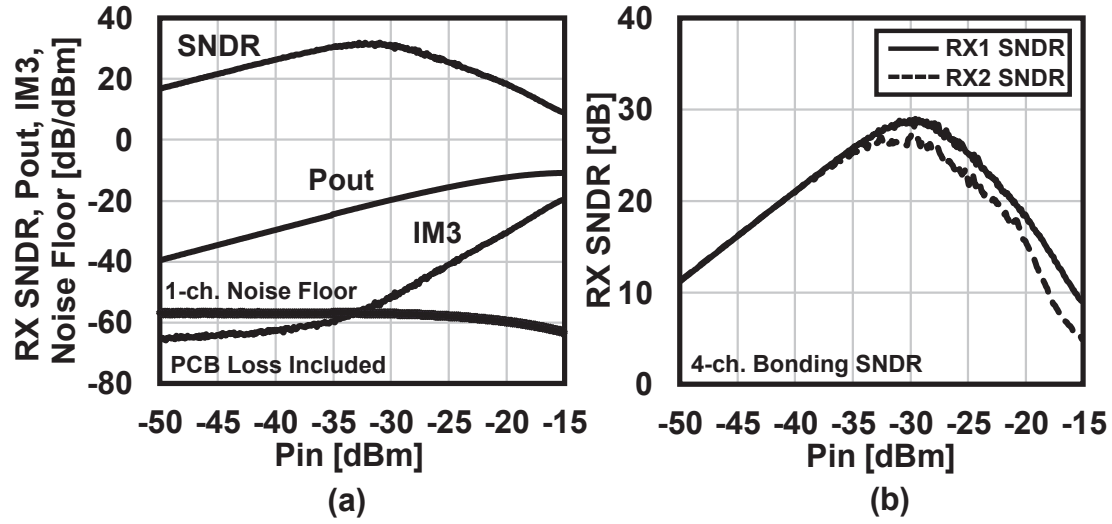


Figure 4.19: (a) Measured RX-mode output power, IM3 and noise floor for TRX element 1 and (b) corresponding SNDRs for RXRX-mode SNDR.

package is adopted in this work, the area consumption for each element-transceiver is mainly decided by the number and the placement of the RF and DC pads. By applying the flip-chip package, the required area could be further reduced. Table 4.1 summarizes the area consumptions for each transceiver building blocks. Thanks to the proposed bi-directional technique, the TL-based 5-stage PA-LNA consumes 0.44 mm^2. The reported

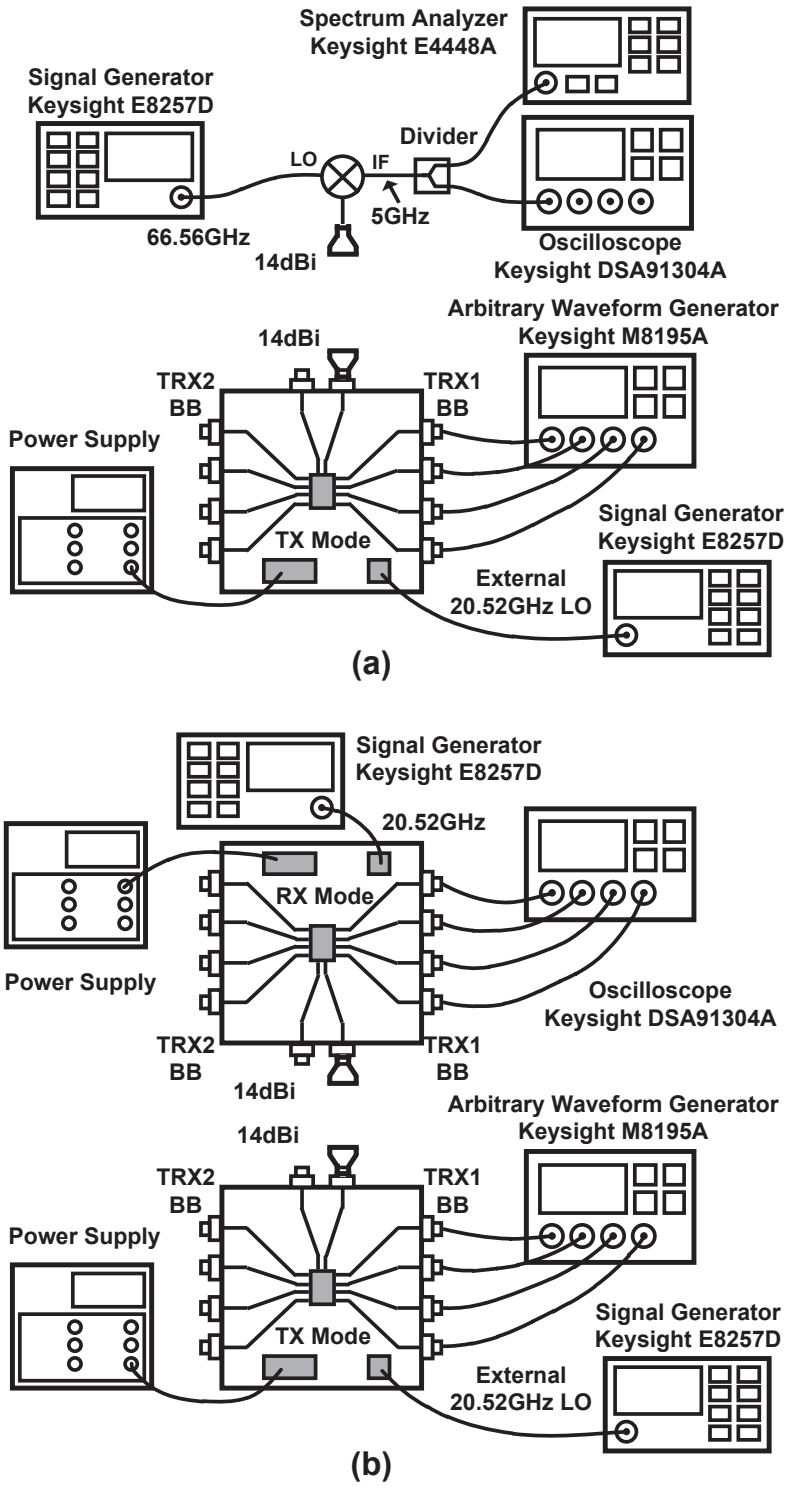


Figure 4.20: Equipment setups for (a) TX spectrum, constellation, and EVM measurement and (b) TX-to-RX constellation and EVM measurement.

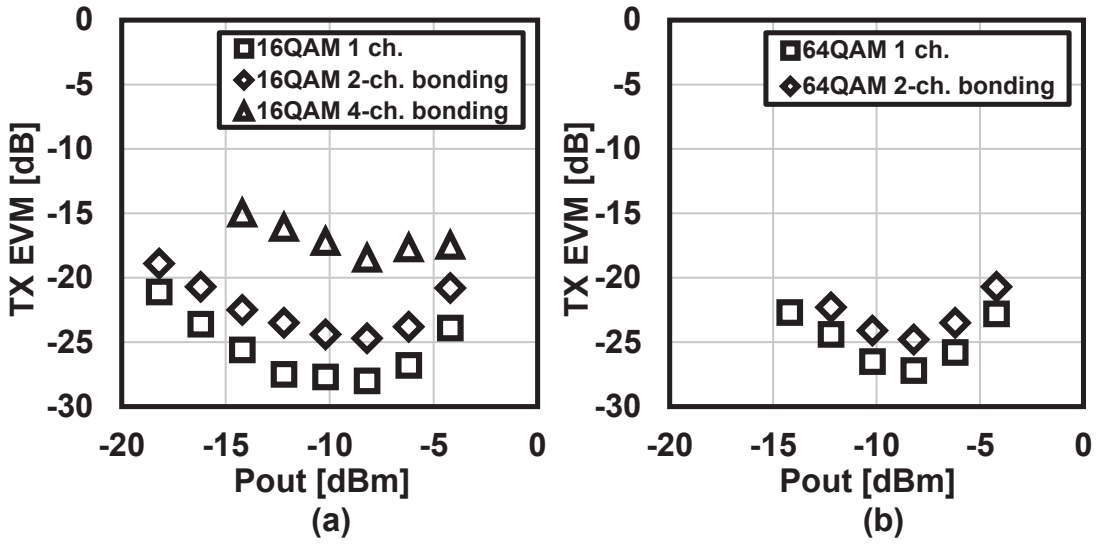


Figure 4.21: Measured TX-mode EVMs for TRX element 1 (a) in 16-QAM and (b) in 64-QAM.

size can be minimized even further by folding the transmission lines during the layout. At the same time, the required area for the I/Q mixers and the I/Q LO generation circuits are reduced to half because of the bi-directional operation.

To evaluate the performance of the proposed bi-directional transceivers, the fabricated chips are implemented into RF printed circuit boards (PCBs). Fig. 4.17 shows the photograph of the RF PCB. One of the transceiver chips is wire-bonded to the PCB at the center. The I/Q baseband input/output signals of TRX element 1 and 2 are distributed to the right and left edges of the PCB, respectively. The RF ports of the TRX elements are connected to the TL-to-waveguide transitions with TLs. The required power supplies and SPI control signals are sent from the pin connectors at the bottom of the photo. The insertion loss of RF PCB is evaluated by comparing the saturated output powers of the TX-mode PCB measurement and the on-wafer PA measurement. The measured PCB loss at 60 GHz is 8.5 dB.

Fig. 4.18 shows the measured characteristics of the proposed transceiver in TX and RX modes. Fig. 4.18 (a) and (b) shows the measured TX-mode and RX-mode gains at channel 2.5 (the center frequency is 61.56 GHz), respectively. Within the frequency range of 57.24 to 65.88 GHz, TRX element 1 and TRX element 2 both achieve around -5-dB conversion gain in TX mode and around 20-dB conversion gain in RX mode. Furthermore, the RX-mode output power, IM3, and noise floor are measured for the TRX elements including the PCB loss at 61.66 GHz. The measured RX-mode NF is 4.8 dB at

Table 4.2: Power Consumption Summary

	Building Blocks	**Power Consumption** [mW]
TX Mode	PA	69.7
	Mixer	3.1
	LO Buffer	10.4
	QILO	22.1
RX Mode	LNA	67.3
	Mixer	0.2
	Baseband Amp.	20.2
	LO Buffer	10.8
	QILO	29.9

62.56 GHz. Within the 60-GHz band, the NF is less than 6 dB. Fig. 4.19 (a) shows the RX-mode measurement results for TRX element 1. Based on the measurement results, the calculated RX-mode SNDRs for TRX element 1 and TRX element 2 are demonstrated in Fig. 4.19 (b) with a four-channel-bonding bandwidth. The achieved maximum SNDRs are 29.0 dB for TRX element 1 and 27.2 dB for TRX element 2.

The proposed bi-directional transceiver is evaluated with SC mode modulated signals. Fig. 4.20 (a) shows the equipment setup for TX-mode constellation, spectrum, and EVM measurement. One RF PCB operating in TX mode and a 14-dBi horn antenna are utilized. The SC-mode baseband modulated signals with symbol rates of 1.76 GSymbol/s for one channel, 3.52 Gsymbol/s for two-bonded channels, and 7.04 Gsymbol/s for four-bonded channels are generated from the arbitrary waveform generator (Keysight M8195A). After the RF PCB, the output signals are received by another 14-dBi horn antenna and down-converted by a mixer. The spectrum is analyzed by a spectrum analyzer (Keysight E4448A) and the constellation and EVM are evaluated by an oscilloscope (Keysight DSA91394A). Regarding the TX-to-RX measurement, one TX-mode PCB and one RX-mode PCB are utilized. With two horn antennas, the TX-to-RX EVM and communication distance are measured. The maximum communication distances in this work are defined by the required TX-to-RX SNRs for a bit error rate of 10^{-3} regarding different modulation schemes, which are -9.8 dB for QPSK, -16.5 dB for 16-QAM, and -22.5 dB for 64-QAM.

The TX-mode EVMs of TRX element 1 are measured with different modulation schemes. The RF center frequency for this measurement is 61.56 GHz. Fig. 4.21(a) shows the 16-QAM EVMs against the output power with different channel bandwidths. Minimum TX-mode EVMs of -28.0 dB for one-channel, -24.7 dB for a two-bonded channel, and -18.5 dB for a four-bonded channel are achieved by the proposed transceiver.

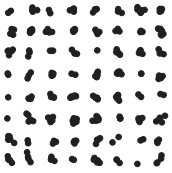
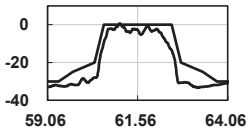
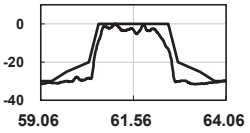
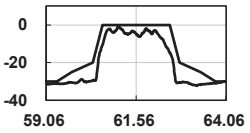
Carrier freq. BW.	61.56GHz (1-ch.)	61.56GHz (1-ch.)	61.56GHz (1-ch.)
Modulation	QPSK	16QAM	64QAM
Data rate	3.52Gb/s	7.04Gb/s	10.56Gb/s
Constellation			
Spectrum			
TX EVM	-29.2dB	-28.0dB	-27.3dB
TX-to-RX EVM	-24.8dB	-24.3dB	-24.0dB
Distance	0.61m	0.12m	0.07m

Figure 4.22: Measured spectra, constellations, TX EVMs, and TX-to-RX EVMs with one-channel bandwidth.

The measured 64-QAM EVMs are shown in Fig. 4.21 (b). The proposed transceiver realizes TX-mode EVMs of -27.2 dB and -24.8 dB for one-channel and two-channel-bonding bandwidths, respectively.

Fig. 4.22 summarizes the performance of the proposed bi-directional transceiver with one-channel bandwidth. SC-mode data communications in QPSK, 16-QAM, and 64-QAM can be supported. The measured maximum communication distances are 0.61 m in QPSK, 0.12 m in 16-QAM, and 0.07 m in 64-QAM. The TX-mode output spectra satisfy the spectrum emission mask defined in IEEE 802.11ad/ay. The corresponding TX-to-RX EVMs for QPSK, 16-QAM, and 64-QAM are -24.8 dB, -24.3 dB, and -24.0 dB, respectively. In this work, the maximum data rate realized in 64-QAM is 21.12 Gb/s, which is measured with a two-channel-bonding bandwidth. Fig. 4.23 shows the measured performance with a two-bonded channel. The achieved TX-to-RX EVMs are -22.7 dB for QPSK, -22.2 dB for 16-QAM, and -22.5 dB for 64-QAM. The four-channel-bonding performance is demonstrated in Fig. 4.24. Four-channel-bonding data rates of 28.16 Gb/s and 14.08 Gb/s are realized by the proposed transceiver in 16-QAM and QPSK, respectively. The TX-mode EVMs and TX-to-RX EVMs are -19.3 dB and -17.7 dB for QPSK, -18.5 dB and -17.6 dB for 16-QAM. The measured two-channel-bonding and

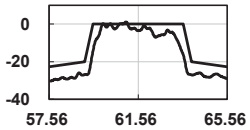
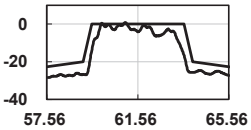
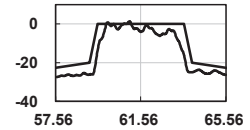
Carrier freq. BW.	61.56GHz (2-ch. bonding)	61.56GHz (2-ch. bonding)	61.56GHz (2-ch. bonding)
Modulation	QPSK	16QAM	64QAM
Data rate	7.04Gb/s	14.08Gb/s	21.12Gb/s
Constellation			
Spectrum			
TX EVM	-26.5dB	-24.7dB	-24.5dB
TX-to-RX EVM	-22.7dB	-22.2dB	-22.5dB
Distance	0.29m	0.10m	0.02m

Figure 4.23: Measured spectra, constellations, TX EVMs, and TX-to-RX EVMs with two-channel-bonding bandwidth.

four-channel-bonding spectra also satisfy the channel-bonding spectrum emission masks defined in IEEE 802.11ay.

Table 4.2 shows the power consumption summary. The analog and digital VDDs in this work are both 1 V. Including the I/Q LO generation, the TX-mode power consumption is 105 mW while the RX-mode power consumption is 128 mW. Table 4.3 compares this work with the state-of-the-art 60-GHz transceivers. Thanks to the proposed area-efficient bi-directional technique, the proposed two-element transceiver chip consumes 6-mm^2 area. The required area for a single-element transceiver is 3 mm^2. A maximum raw data rate of 28.16 Gb/s per element-transceiver is realized in 16-QAM. The proposed chip could be configured for IEEE 802.11ay MIMO communication. Concerning the required ultra-high data-rate and the numerous number of transceiver elements, the proposed chip could significantly suppress the manufacturing cost of the frontend while maintaining the high-speed data communication.

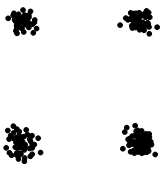
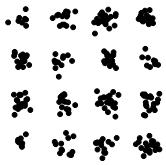
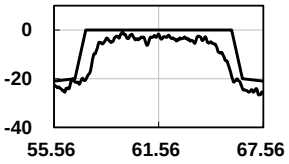
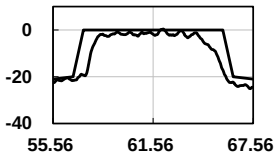
Carrier freq. BW.	61.56GHz (4-ch. bonding)	61.56GHz (4-ch. bonding)
Modulation	QPSK	16QAM
Data rate	14.08Gb/s	28.16Gb/s
Constellation		
Spectrum		
TX Pout	-8.2dBm	-8.2dBm
TX EVM	-19.3dB	-18.5dB
TX-to-RX EVM	-17.7dB	-17.6dB
Distance	0.16m	0.01m

Figure 4.24: Measured spectra, constellations, TX EVMs, and TX-to-RX EVMs with four-channel-bonding bandwidth.

4.4 Conclusion

This Chapter introduces a 60-GHz CMOS bi-directional transceiver designed for IEEE 802.11ay. The bi-directional amplifier proposed in this paper allows the sharing of the interstage passive components, which further reduces the required on-chip area. A two-element transceiver chip consumes 6 mm^2 area including the pads. The proposed transceiver is evaluated with SC-mode modulated signals. The realized maximum data rate in 64-QAM is 21.12 Gb/s with a two-channel-bonding bandwidth. The maximum data rate achieved by this work is 28.16 Gb/s in 16-QAM with four-channel-bonding bandwidth. Reduced manufacturing cost along with high-speed data communication could be supported for the next generation WALN.

Table 4.3: Performance Comparison of 60-GHz Transceivers

	Data rate	**TX Pout /ant. path**	**RX NF**	**Area**	**Integration**	**Power Consumption**
[10]	2.5Gb/s QPSK	2.0dBm at TX EVM =-22.0dB	7.1dB	13.5mm^2 RFIC only	90nm, direct conversion, TX, RX, LO, analog BB (RFIC only)	TX: 347mW RX: 274mW RFIC only
[49]	N.A.	N.A.	<9.0dB*	29.0mm^2 32×element	90nm, 32-element, heterodyne, TX(IF), RX(IF), LO	TX: 1200mW RX: 850mW 32×ele.
[15]	21.12Gb/s per TRX 64QAM	7.0dBm at TX EVM =-22.0dB	N.A.	17.6mm^2 2×element	65nm, direct conversion, 2TX, 2RX, 2LO.	TX: 544mW RX: 432mW 2×ele.
[27]	7Gb/s 16QAM	6dBm* at TX EVM =-23dB	4.8dB*	7.9mm^2 4×element	28nm, 4-element, direct conversion, TX, RX, LO.	TX: 670mW RX: 431mW 4×ele.
[57]	42.24Gb/s 64QAM	7.3dBm at TX EVM =-22.0dB	N.A.	6mm^2	65nm, direct conversion, TX, RX, LO.	TX: 169mW RX: 139mW
[59]	4.6Gb/s 16QAM	-2.0dBm at TX EVM =-22.0dB	6.5dB	21.9mm^2 RFIC only 12×element	40nm, 12-element, heterodyne, TX(IF), RX(IF), LO (RFIC only)	TX: 8400mW RX: 6600mW 144×ele.
[48]	27.8Gb/s 16QAM	N.A.	7.0dB	4.3mm^2 RFIC only 2×element	28nm, digital polar TX, direct conversion RX, TX, RX, LO, w/o PLL.	TX: 210mW RX: 110mW
This Work	21.12Gb/s per TRX 64QAM 28.16Gb/s per TRX 16QAM	-4.2dBm at TX EVM =-26.0dB	4.8dB	6.0mm^2 2×element	65nm, direct conversion, TX, RX, LO.	TX: 210mW RX: 256mW 2×ele.

* estimated from the material.

Chapter 5

LO Phase Shifting Phased-Array Transceiver

60-GHz CMOS transceivers have been introduced in Chapter 3 and Chapter 4 for the next generation WLAN system. Area-efficient solutions with significantly improved data rate have been provided. Similar to the WLAN system, mobile communication network also requires an improvement in the data access speed. This chapter will introduce a CMOS implementation of the 28-GHz phased-array transceiver designed for 5G NR.

As mentioned in Chapter 1, the next generation mobile network 5G NR will also utilize the millimeter-wave spectrum to boost the data rate. Among the FR2 defined in 5G, band n257, which is from 26.5 to 29.5 GHz, could be available in most parts of the world. Extremely high speed wireless communication experience could be provided. Different from the transceivers designed for the under-6-GHz band, the silicon-based millimeter-wave phased-array transceivers demand a larger array size. Accurate beam control is required for providing stabilized data communication and avoiding interference [2, 60]. An improved phase tuning resolution along with suppressed gain and phase errors will be required. During the past few years, radio-frequency (RF), local-oscillator (LO) and baseband phase shifting architectures are utilized in millimeter-wave phased-array transceivers. Fig. 5.1 shows a comparison between different phase shifting architecture. The RF phase shifting architecture, which shares the mixer and LO distribution, can reduce area and power consumptions [2–9]. However, the RF phase shifters suffer from gain variation during phase tuning, which is usually more than 0.5 dB [61–64]. A gain-compensated phase map will be required to be maintained regarding the varying RF path gain. Baseband phase shifting architecture can realize very predictable and high-resolution phase tuning with the baseband analog circuits [23]. However, due to the large fractional bandwidth for the baseband phase shifters, gain and phase mismatches will

	RF phase shifting	LO phase shifting	BB phase shifting
On-chip area	Compact	Large	Large
Power consumption	Low	High	High
Phase Shifting Resolution	Limited	Fine	Fine
Gain Variation	Large	Low	Large
Blocker tolerance	Strong	Weak	Weak

Figure 5.1: Comparison of phase shifting architecture.

arise along the frequency between the transceiver elements. Additionally, the quadrature LO distribution not only consumes power and area but also degrades the I/Q imbalance of the transceiver.

By saturating the mixer with enough LO voltage swing, LO phase shifting architecture can realize fine phase tuning with greatly improved gain and phase errors [65–67]. Although the LO distribution consumes additional area and power, the induced area and power consumptions could be suppressed by the power-efficient design and the LO sharing between the transmitter and receiver.

In this chapter, a 28-GHz phased-array transceiver chip based on the LO phase shifting architecture is introduced. The proposed transceiver chip is fabricated in a 65-nm CMOS process featuring low manufacturing cost. The proposed LO phase shifter achieves a measured RF gain variation of less than 0.2 dB and an RMS phase error of 0.3°. The eight-element transceiver modules in this work are capable of scanning the beam from −50° to +50°. Accurate beam control with suppressed sidelobe level is realized during the beam scan. At a distance of 5 m, the proposed module demonstrates the first 512-QAM constellation in the 28 GHz band. A data link of 6.4 Gb/s in 256-QAM is maintained within a scan angle of −50° to +50°.

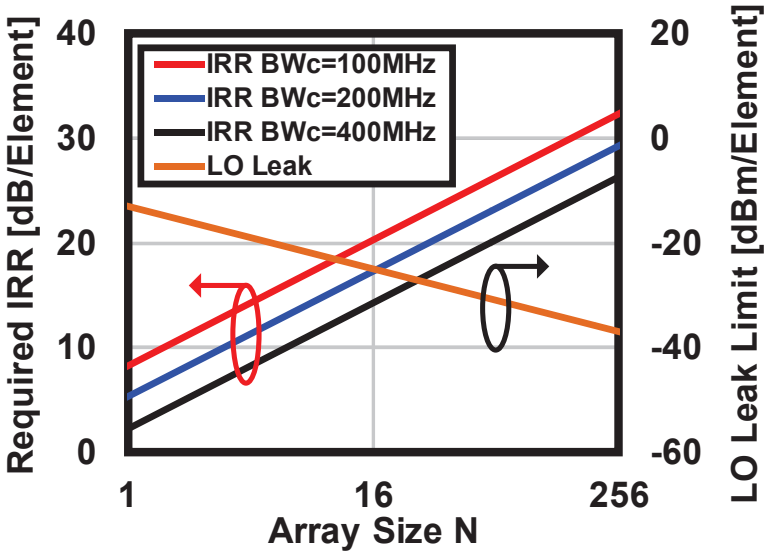


Figure 5.2: Calculated LO leakage limitation and the required IRR against the array size N.

5.1 Considerations on the LO Phase Shifting Architecture

An optimized EVM performance over a long communication distance is supposed to be maintained by the future 5G millimeter-wave phased-array transceivers. High-speed, low-latency, and stabilized data links with suppressed sidelobe and spurious levels are required over all beam scan angles. As mentioned in Chapter 3, due to the enlarged bandwidth, careful considerations on the noise figure (NF), linearity are always essential for millimeter-wave transceiver design. On the other hand, due to the enlarged array size, an improved phase shifting resolution along with suppressed phase and gain errors will be strongly demanded. To improve the phase tuning resolution, design considerations are required for the phase-shifting architecture, magnitude and phase errors, power consumption and area. Adding additional least significant bit (LSB) to the passive RF phase shifters [63, 68] could improve the resolution, but the circuit for the LSB will induce extra insertion loss and area cost. The gain error performance will also be degraded during phase shifting. RF active vector summing phase shifters [64, 69] can solve these problems to some degree. However, a compensated phase map is required for cancelling the gain and phase errors caused by the I/Q generation. As a result, to support accurate beam control with suppressed sidelobe level, the RF gain-invariant LO phase shifting architecture is adopted in this work. The sidelobe regrowth caused by the gain variation during

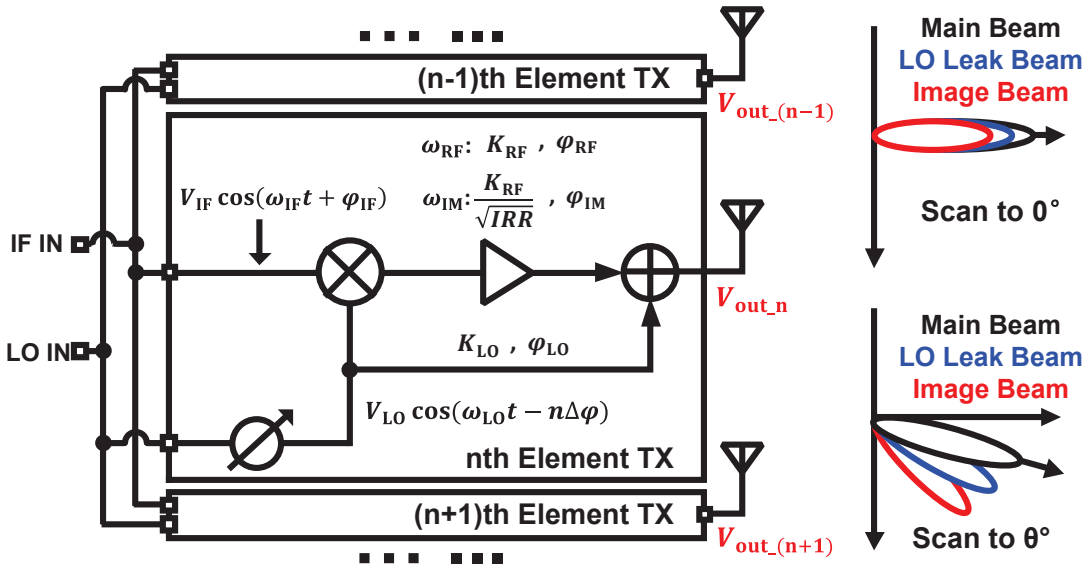


Figure 5.3: Analysis model for LO leakage and image signal.

phase tuning can be significantly suppressed. When compared with the RF phase shifters, the LO phase shifters only need to cover a limited frequency range. A much-improved phase tuning step with sufficiently small phase error could be achieved by LO phase shifting architecture. At the same time, because the LO phase shifters are located in the LO path, gain variation of the LO phase shifters during phase tuning will not influence the RF path SNDR. As a result, an optimized transceiver SNDR along with stabilized data communication can be realized during beam steering.

However, when utilize the LO phase shifting in combination with the heterodyne architecture, the LO leakage and the image signal will potentially generate spurious over the air. As a result, a stringent level for spurious radiation is regulated by the 5G NR standard for FR2 [70, 71]. The BS transmitter spurious emission limit defined in 5G NR for FR2 is less than $P_{\text{spur\_TRP}}$=-13 dBm/MHz [72]. Regarding the BS type 2-O requirement, the maximum radiated LO leakage power per element can be found through dividing $P_{\text{spur\_TRP}}$ by N, where N is the array size. When consider a 256-element array, the corresponding $P_{\text{LO\_leak}}$ should be kept under -37.1 dBm. Concerning the image rejection ratio (IRR), a similar equation can be derived:

$$IRR > \frac{P_{\text{out}}}{P_{\text{spur\_TRP}} \cdot BW_{\text{t}}} \cdot N \tag{5.1}$$

where P_{out} denotes the radiated power of the transmitter and BW_{t} is the maximum transmission bandwidth in megahertz for a corresponding BW_{c}. Fig. 5.2 shows the LO leakage

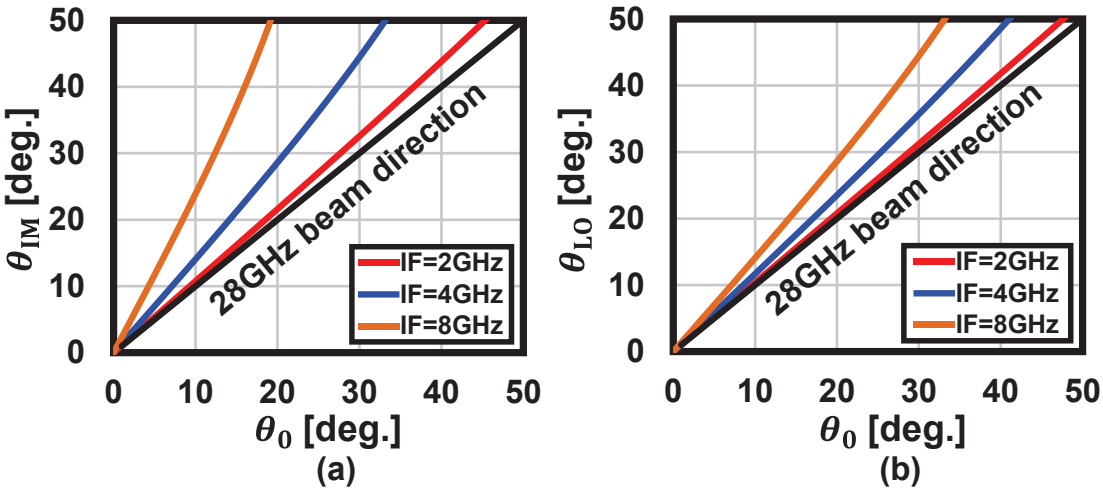


Figure 5.4: Calculated (a) image beam direction θ_{IM} and (b) LO leakage beam direction θ_{LO} against RF beam direction θ_0 with different intermediate frequencies (IFs).

limitation and the required IRR for a single-element transmitter against the array size. For a BW_c of 100 MHz together with a P_{out} of 15 dBm, the IRR should be larger than 32.3 dBc for a 256-element array.

Even when the total radiated LO leakage and image power meet the spurious emission limits, careful design is still required for the image and LO leakage radiation patterns. For phased-array transceivers based on the LO phase shifting, all RF frequency components are shifted with the same phase. Thus, beam squinting will occur in the image and LO leakage beams. Fig. 5.3 shows the analysis model for the image and LO leakage patterns. When the linear array with N isotropic radiators in the figure scans the beam to θ_0, the beam patterns $F_{IM}(\theta)$ and $F_{LO}(\theta)$ for the image signal and the LO leakage, respectively, can be calculated by summing over the transmitter elements. For simplicity, the ωt terms are omitted in the following equations [73]:

$$F_{IM}(\theta) = \frac{K_{RF}V_{IF}V_{LO}}{2\sqrt{IRR}} \frac{\sin\left[0.5Nd(k_{IM}\sin\theta - k_{RF}\sin\theta_0)\right]}{N\sin 0.5d(k_{IM}\sin\theta - k_{RF}\sin\theta_0)} \tag{5.2}$$

$$F_{LO}(\theta) = K_{LO}V_{LO} \frac{\sin[0.5Nd(k_{LO}\sin\theta - k_{RF}\sin\theta_0)]}{N\sin 0.5d(k_{LO}\sin\theta - k_{RF}\sin\theta_0)} \tag{5.3}$$

In the equation, k_{RF}, k_{IM} and k_{LO} denote the propagation constants for the RF signal, the image signal and the LO leakage, respectively, while d represents the spacing between elements. Different from the RF beam direction θ_0, the image and LO leakage beam

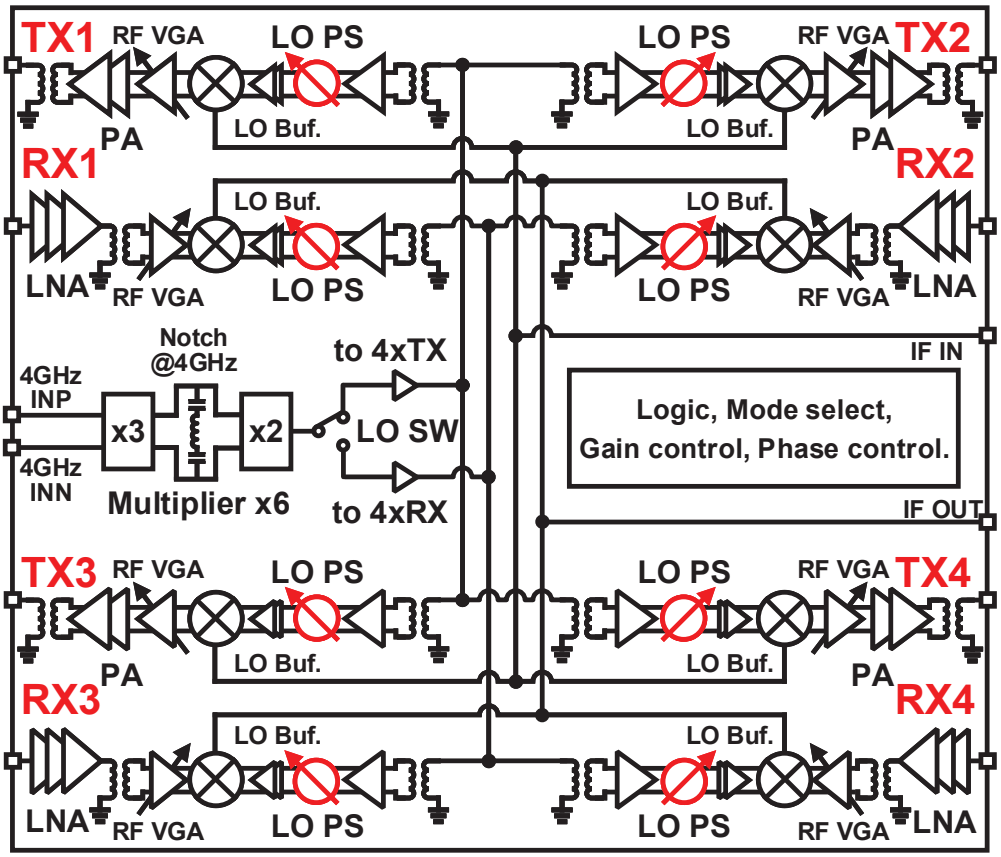


Figure 5.5: System block diagram of the proposed phased-array transceiver.

directions θ_{IM} and θ_{LO} are given as follows:

$$\sin\theta_{\mathrm{IM}} = \frac{\omega_{\mathrm{RF}}}{\omega_{\mathrm{IM}}}\sin\theta_0 \qquad \sin\theta_{\mathrm{LO}} = \frac{\omega_{\mathrm{RF}}}{\omega_{\mathrm{LO}}}\sin\theta_0 \tag{5.4}$$

The analysis above shows that the image and LO leakage also benefit from the array factor. When the RF beam is steered to θ_0 ($\theta_0 \neq 0°$), the image and LO leakage beams can point in completely different directions due to beam squinting. In consideration of a 256-element array, the radiated image and LO leakage will cause potential interference. As a result, an IF range of 2.5 to 5.5 GHz and an LO range of 23.4 to 24.6 GHz are selected in this work not only due to the frequency generation plan but also because of the directions of LO leakage and image beams. The image and LO leakage in the transmitter is also well-suppressed without any lossy notch filters, which contributes to a power- and area-efficient design.

TX	Divider	Mixer	RF Buffer	PA	Board loss	Total
Power Gain [dB]	-7.00	-10.00	8.00	20.00	-3.00	
Cumulative Gain [dB]	-7.00	-17.00	-9.00	11.00	8.00	8.00
NF [dB]	7.00	10.00	9.00	8.50	3.00	
Cumulative NF [dB]	7.00	17.00	26.00	26.50	26.50	26.50
OIP3 [dBm]	100.00	3.00	15.00	24.50	100.00	
Cumulative OIP3 [dBm]	100.00	3.00	9.54	23.32	20.32	20.32

RX	Board Loss	LNA	RF Buffer	Mixer	Combiner	Total
Power Gain [dB]	-3.00	20.00	8.00	-10.00	5.00	
Cumulative Gain [dB]	-3.00	17.00	25.00	15.00	20.00	20.00
NF [dB]	3.00	4.30	8.50	10.00	0.00	
Cumulative NF [dB]	3.00	7.30	7.40	7.42	7.42	7.42
OIP3 [dBm]	100.00	2.00	12.00	5.00	100.00	
Cumulative OIP3 [dBm]	100.00	2.00	7.88	-2.89	2.11	2.11

Figure 5.6: Level diagram design of the transceiver.

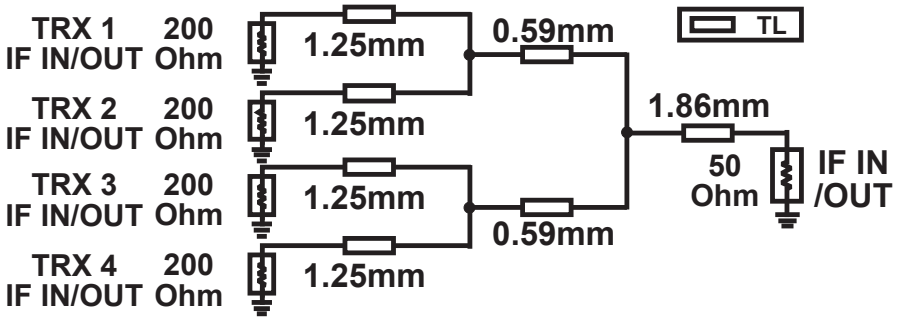


Figure 5.7: Transmission line branching network for IF combining and splitting.

5.2 Circuit Implementation

Fig. 5.5 shows the block diagram of the proposed four-element phased-array transceiver. A superheterodyne architecture is adopted in this work to remove the in-band LO leakage and image. The element-transmitter in this work consists of a two-stage PA, a one-stage RF VGA, and an up-conversion mixer, while the element-receiver includes a three-stage LNA, a one-stage RF VGA, and a down-conversion mixer. Fig. 5.6 shows the level diagram of the phased-array transceiver chip. The linearity of the transmitter is optimized regarding the input branching network. Complex modulation scheme could be supported by the proposed chip. Fig. 5.7 shows the branching network for combining/splitting the 4-GHz IF signal. The branching network is designed using the 50-ohm TLs. The simulated splitting loss is 7.5 dB at 4 GHz, including the splitting ratio and distribution loss. The

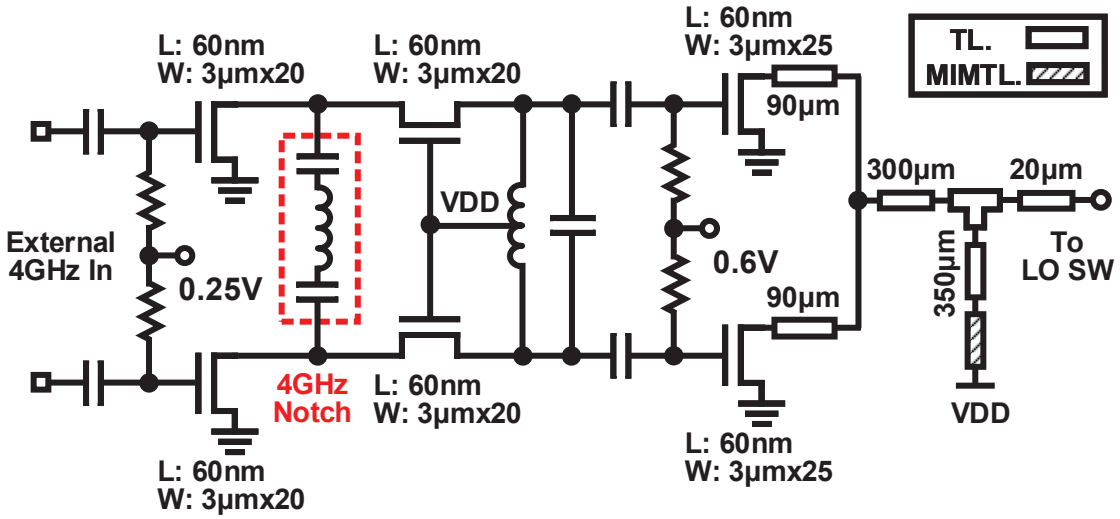


Figure 5.8: Circuit schematic of multiplier.

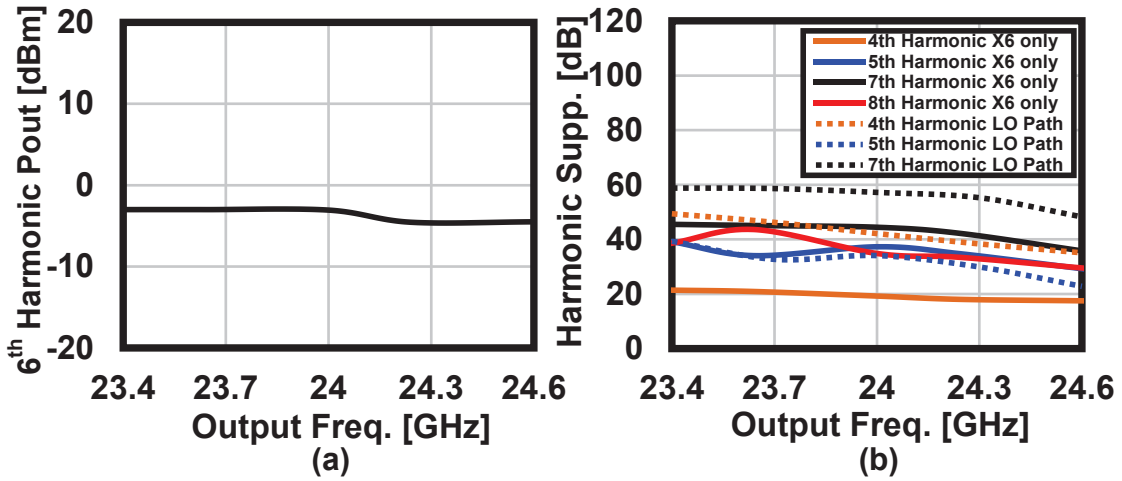


Figure 5.9: Measured (a) 6th-order harmonic output power and (b) harmonic suppression for multiplier.

required 24-GHz LO is generated by multiplying the external 4-GHz signal by six. An amplifier-based LO switch is utilized to redirect the 24-GHz LO to the transmitter array or to the receiver array. The LO distribution in this work is realized in a single-ended formation. The single-ended LO is transformed into a differential before the transceiver elements. The coupling between the LO and the IF distributions can induce gain and phase mismatch among the transceiver elements, so the crossing component for the distribution is carefully designed. The measured coupling ratios are less than -45 dB at 24 GHz and

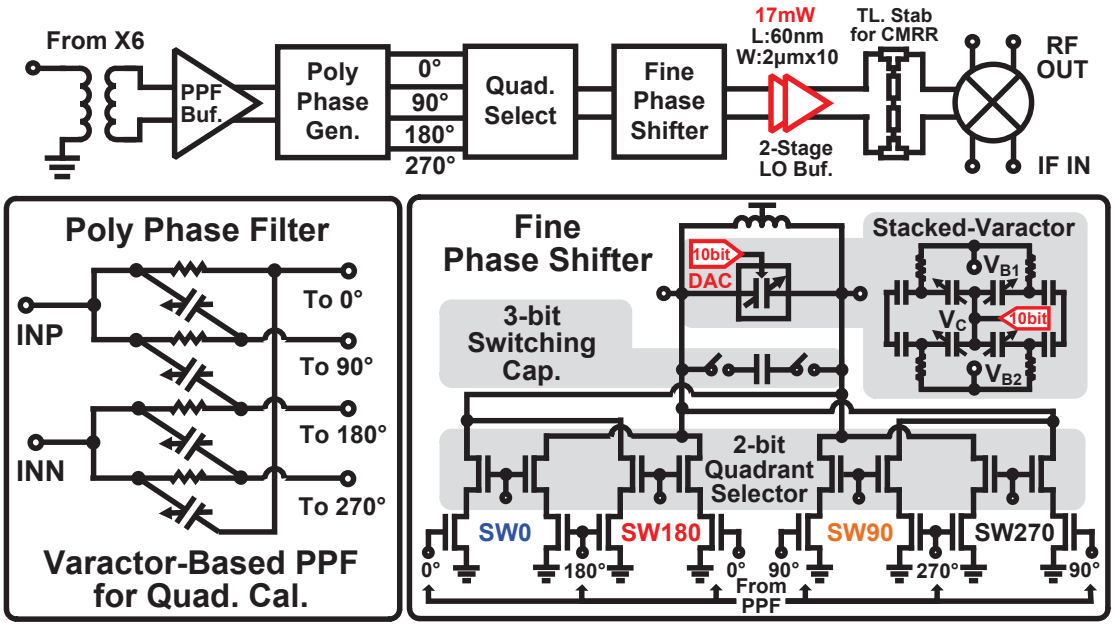


Figure 5.10: Block diagram of the LO for each element-transceiver and circuit schematic of the proposed LO phase shifter.

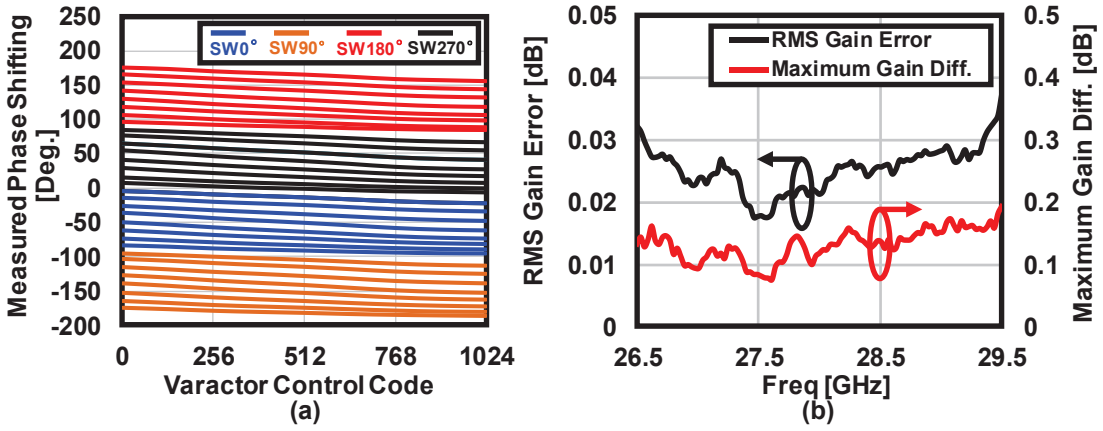


Figure 5.11: Measured (a) phase shift at 28 GHz and (b) RF path gain variation and corresponding RMS gain error for the LO phase shifter.

less than -60 dB at 4 GHz. An LO phase shifter designed for the optimized gain and phase errors is utilized to maintain the required phase shifting. A logic block for digital control is also integrated into the chip for controlling the bias and switches. The transceiver chip can be changed between transmitter and receiver modes by the logic controller. Additionally, functions like gain control, poly-phase filter (PPF) quad-phase calibration, and fine phase

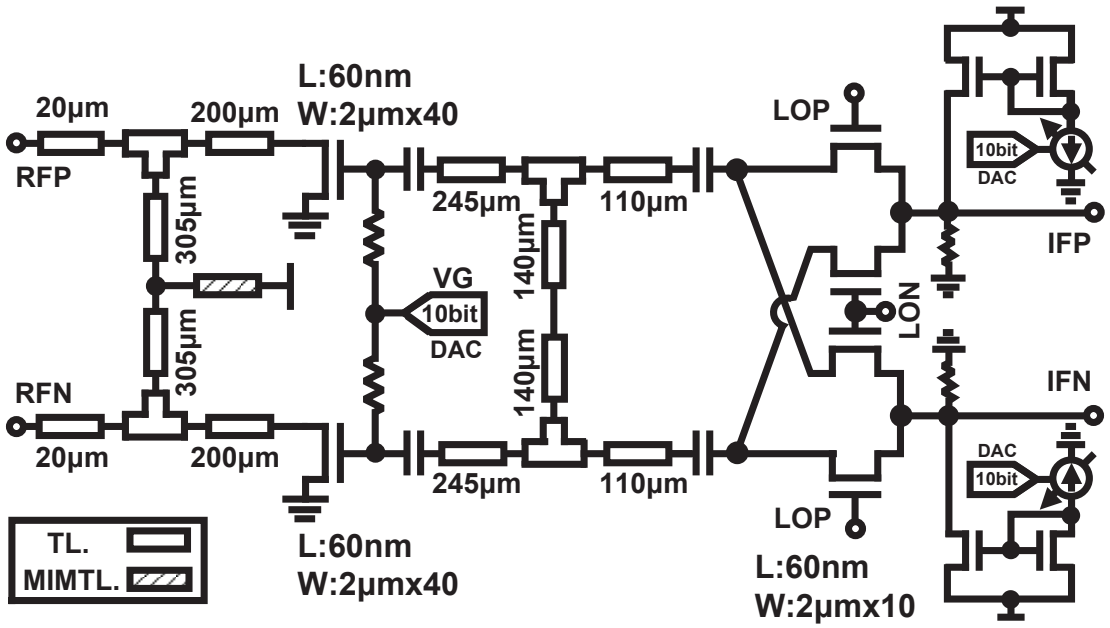


Figure 5.12: Circuit schematic of up-conversion mixer and RF VGA.

tuning are realized with an external microprocessor through the digital control block.

5.2.1 LO

Fig. 5.8 shows the circuit schematic of the multiplier. This work utilizes a frequency tripler and doubler to realize the required six-fold multiplication. Because the 7th harmonic of the multiplier falls inside the operational bandwidth, harmonic suppression of the multiplier is optimized in consideration of improving the EVM and decreasing the spurious emissions. The proposed tripler has a differential topology [74]. Thus, the even-order harmonics, which fall close to the desired 3rd-order output, are suppressed. To further prohibit the strong external 4-GHz signal from entering the doubler, an LC notch filter designed at the fundamental frequency is inserted. The doubler in this work also adopts differential topology. The differential outputs are combined together for suppressing the odd-order components. The output matching networks are designed based on the 50-ohm TLs. The TLs with shunt MIM capacitors to ground are utilized for the power supply. The gate bias of the doubler is optimized for a higher 2nd-order harmonic [75]. Fig. 5.9 (a) demonstrates the measured saturated power of the desired 6th-order output for a stand-alone multiplier. Within the frequency range of 23.4 to 24.6 GHz, the saturated output power is around -3 dBm. The measured harmonic suppressions are shown in Fig. 5.9 (b). The 5th, 7th, and 8th harmonic suppressions for the multiplier are larger

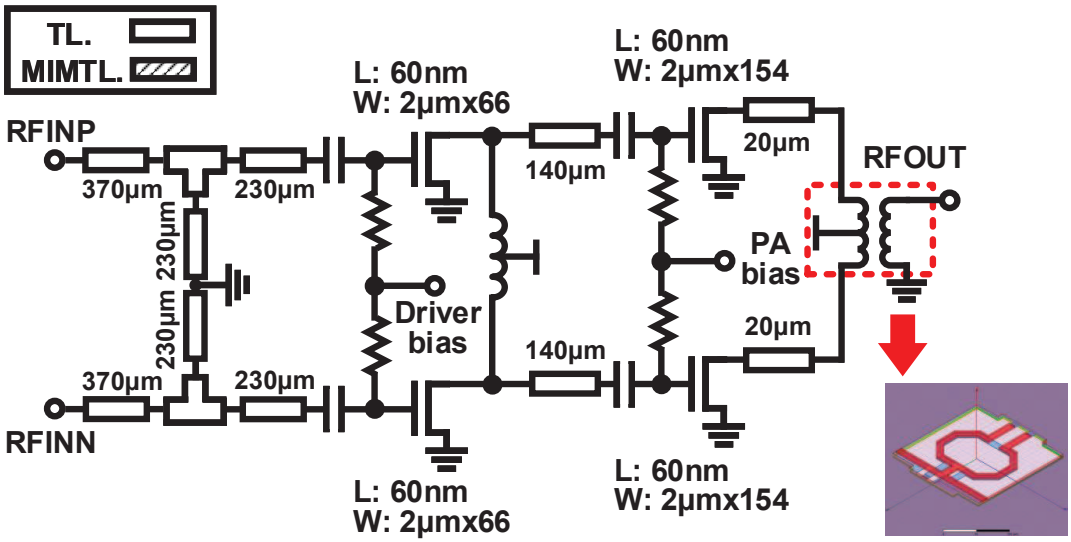


Figure 5.13: Circuit schematic of differential power amplifier.

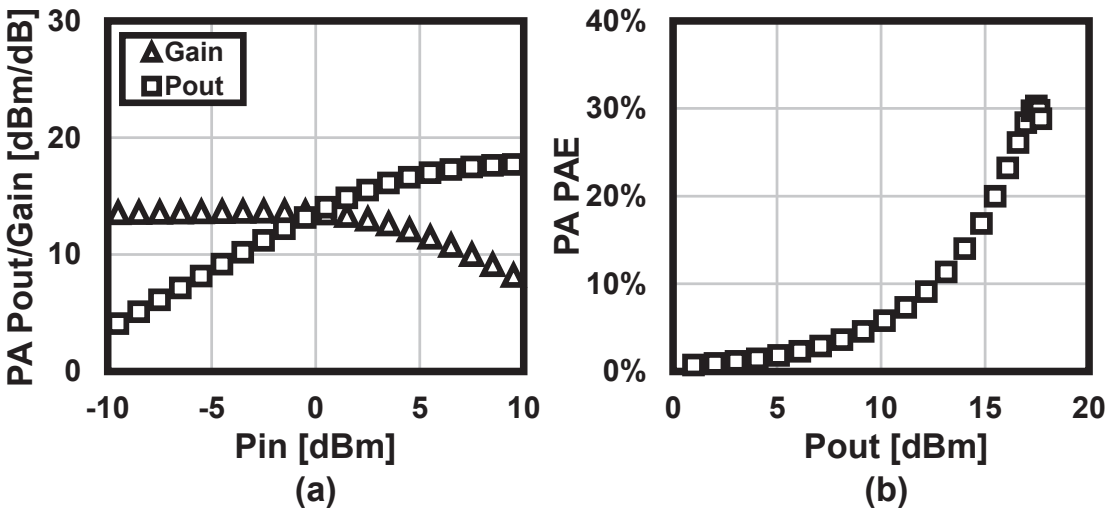


Figure 5.14: Measured (a) output power and gain and (b) power-added efficiency of power amplifier.

than 30 dB, while the 4th harmonic suppression is around 20 dB. The measured harmonic suppressions for the complete LO path, including the multiplier, the LO switch, and the phase shifter, are also shown in the same figure. The 4th, 5th and 7th order harmonic suppressions at 24-GHz LO frequency are larger than 30 dB.

The proposed LO phase shifter designed for each transceiver element is shown in Fig. 5.10. To realize a fine phase shifting step, the 24-GHz LO is first sent for the quad-

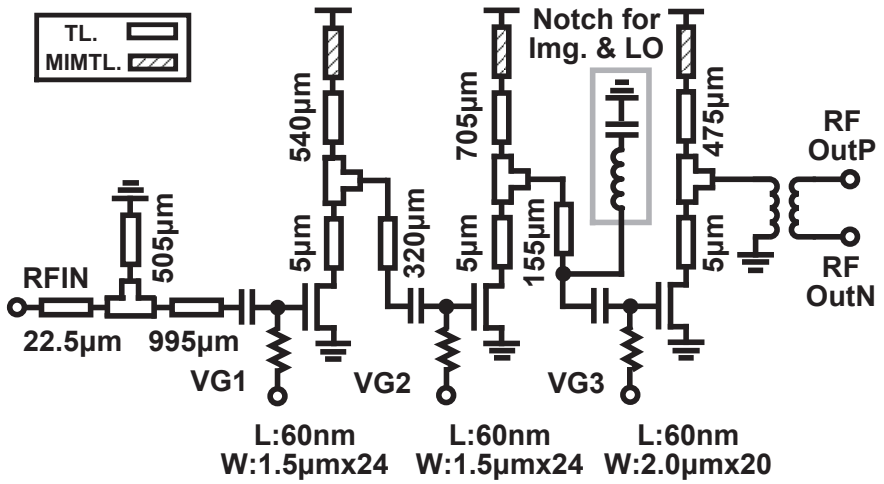


Figure 5.15: Circuit schematic of LNA.

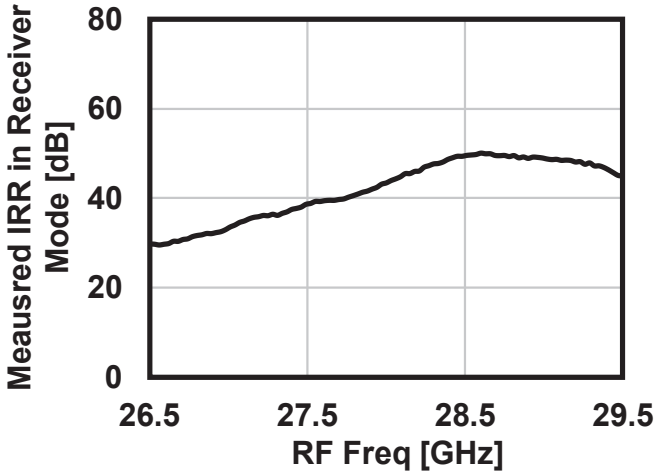


Figure 5.16: Measured receiver-mode IRR against input RF frequency.

phase generation. Afterward, the generated quad-phase LOs are selected by a quadrant selector and finally shifted by a fine phase shifting stage. As a result, the fine phase shifter in this work only needs to cover 90°. Thus, a linear and high-resolution phase tuning can be achieved. For the quad-phase generation, a constant-magnitude PPF is adopted in this work [76]. Varactors controlled by the 10-bit DACs are utilized in the PPF. The quadrature phase mismatch after fabrication can be compensated by tuning the varactor. A tuning range larger than 20° is maintained at the LO frequency of 24 GHz. With default bias setting, a PPF phase mismatch of 5.1° is measured at 24 GHz. After

Table 5.1: Core Area of Blocks

Blocks	**Core Area** [mm^2]
PA	0.18
RF Buf. & Mixer	0.16
LO Phase Shifter & Buf.	0.25
LNA	0.24
Multiplier	0.3
LO SW &Buf.	0.27
Logic	0.64

tuning the varactor, the phase mismatch is reduced to less than 0.1°. The imbalance of the quad-phase outputs can also be influenced by the input common-mode signal and the load impedance variation. Thus, a differential buffer with enhanced common-mode rejection is inserted before the PPF to suppress the common-mode generated by the on-chip balun. Concerning the load impedance variation during the fine phase tuning, the quadrant selector in this work adopts a cascode switching array topology to provide the required isolation between the PPF and fine tuning stage. The load impedance variation is suppressed during the phase shifting.

The circuit schematic of the fine phase shifter is also shown in Fig. 5.10. To cover a 90° tuning range, an LC tank is utilized in this work. Considering an LO frequency of ω_{LO} and tank quality factor of Q, the magnitude and phase responses can be expressed using the following equations:

$$\begin{aligned} A &= \sqrt{1 + Q^2\left(\frac{\omega_{\mathrm{LO}}}{\omega_0} - \frac{\omega_0}{\omega_{\mathrm{LO}}}\right)^2} \\ \varphi &= \arctan\left(Q\left(\frac{\omega_0}{\omega_{\mathrm{LO}}} - \frac{\omega_{\mathrm{LO}}}{\omega_0}\right)\right) \end{aligned} \tag{5.5}$$

where ω_0 denotes the resonant frequency for the LC tank. To maintain a phase shift from $-45°$ to $+45°$, the capacitance tuning range of C_1 to C_2 is required to be covered, where C_1 and C_2 are defined by:

$$C_1 = \frac{2Q^2}{L\omega_{\mathrm{LO}}^2\left(2Q^2 + \sqrt{1+4Q^2} + 1\right)} \tag{5.6}$$

$$C_2 = \frac{2Q^2}{L\omega_{\mathrm{LO}}^2\left(2Q^2 - \sqrt{1+4Q^2} + 1\right)} \tag{5.7}$$

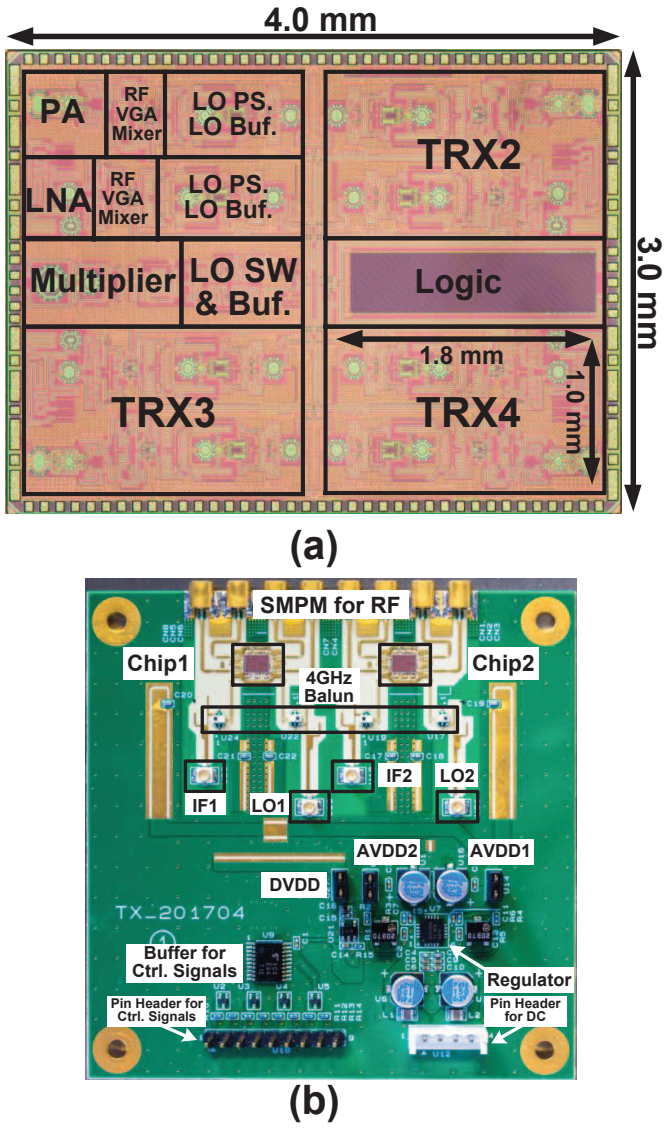


Figure 5.17: (a) Die micrograph of four-element phased-array transceiver chip and (b) photograph of transmitter-mode RF PCB.

The Q for the tank is reduced to extend the capacitance tuning range. High-resolution phase tuning is realized with a 3-bit capacitor bank together with a 10-bit DAC-controlled varactor. The stacked varactor in this work is designed to achieve a wider phase coverage along with linear phase tuning. The measured raw gain variation of the phase shifter is 2.7 dB at 24 GHz.

After the LO phase shifter, a two-stage differential LO buffer is inserted. A small transistor size of $0.06\mu\text{m}/2\mu\text{m} \times 10$ is selected for saturating the LO driving power with reduced power consumption. The two-stage LO buffer only consumes 17 mW when mea-

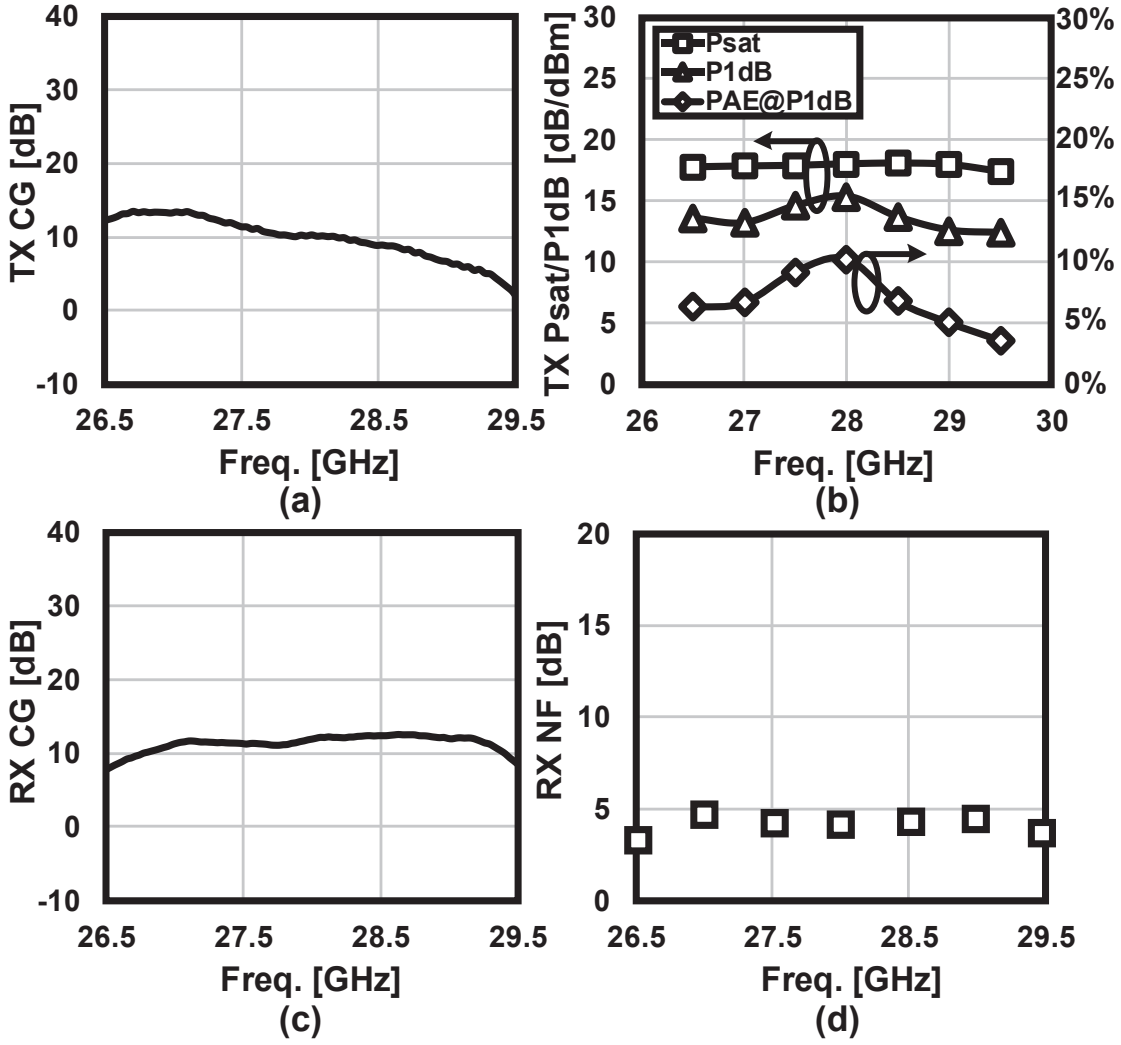


Figure 5.18: Measured transceiver characteristics: (a) transmitter-mode conversion gain, (b) transmitter-mode linearity and PAE, (c) receiver-mode conversion gain and (d) receiver-mode noise figure.

sured. Furthermore, to suppress the LO leakage due to the imbalanced differential LO, a shunt-shorted TL stub for common-mode rejection is inserted before the mixer.

Fig. 5.11 (a) shows the measured phase shift for the proposed LO phase shifter. A 360° tuning range and a tuning step of less than 0.04° are achieved by the proposed circuit. Thanks to isolation from the quadrant selector, the phase control code for the fine stage could be shared within the four quadrants. The measured RMS phase error is only 0.3° due to the code sharing. The measured RF gain variation is shown in the Fig. 5.11 (b). With the help of the power-efficient LO buffers, the measured RF gain variation is less than 0.2 dB within a frequency range of 26.5 to 29.5 GHz. The calculated RMS gain

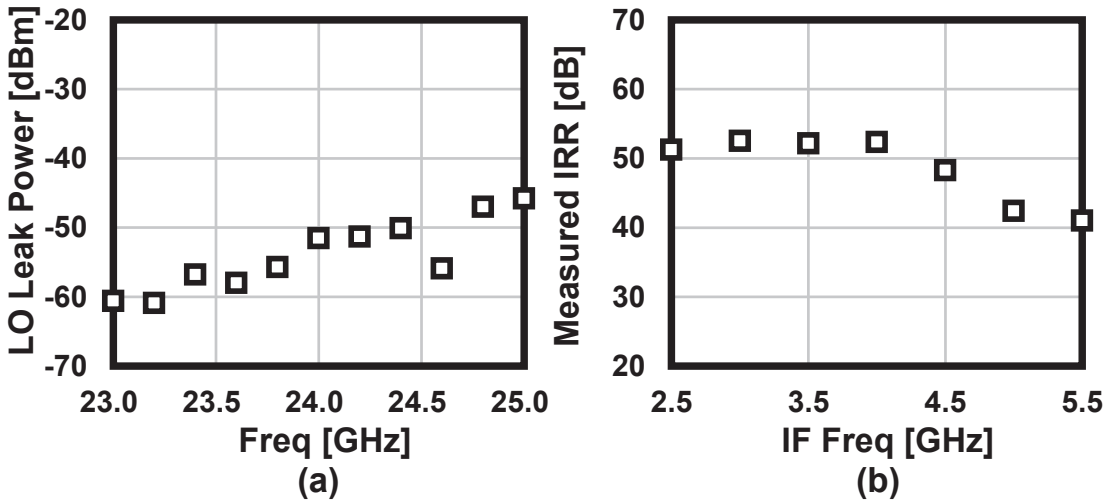


Figure 5.19: Measured transmitter-mode (a) LO leakage and (b) IRR.

error is less than 0.04 dB. Thus, an RF gain-invariant, quasi-continuous phase tuning is realized with a sufficiently small phase error, allowing the proposed LO phase shifter to accurately control beam.

The required calibration also benefits from the proposed LO phase shifter. Because of the gain-invariant phase tuning, accurate calibration could be maintained with a simple procedure. Additionally, by choosing part of the control codes, the phase shifter can be easily configured into a coarse phase shifting mode if accurate calibration is not required. The calibration time could be further shortened depending on the required calibration accuracy.

5.2.2 Transmitter

The transmitter proposed in this work adopts a differential topology. Fig. 5.12 shows the up-conversion mixer along with the RF VGA. A double-balanced passive mixer is used to suppress the LO leakage through both the IF and RF sides. To save power, the transistor size in the mixer is optimized for a large LO swing. Two current sources are attached to the IF input for adjusting the DC offset [13, 30]. A designed tuning resolution of 0.1 mV is realized by the 10-bit DACs. To calibrate the magnitude mismatch between different elements, a DAC-controlled TL-based RF VGA is used to realize a less-than-0.1-dB gain tuning resolution along with a 10-dB tuning range. The phase variation of the VGA can be easily compensated by gain-invariant phase tuning.

Regarding the 5G CMOS PA design, larger output power with higher power-added

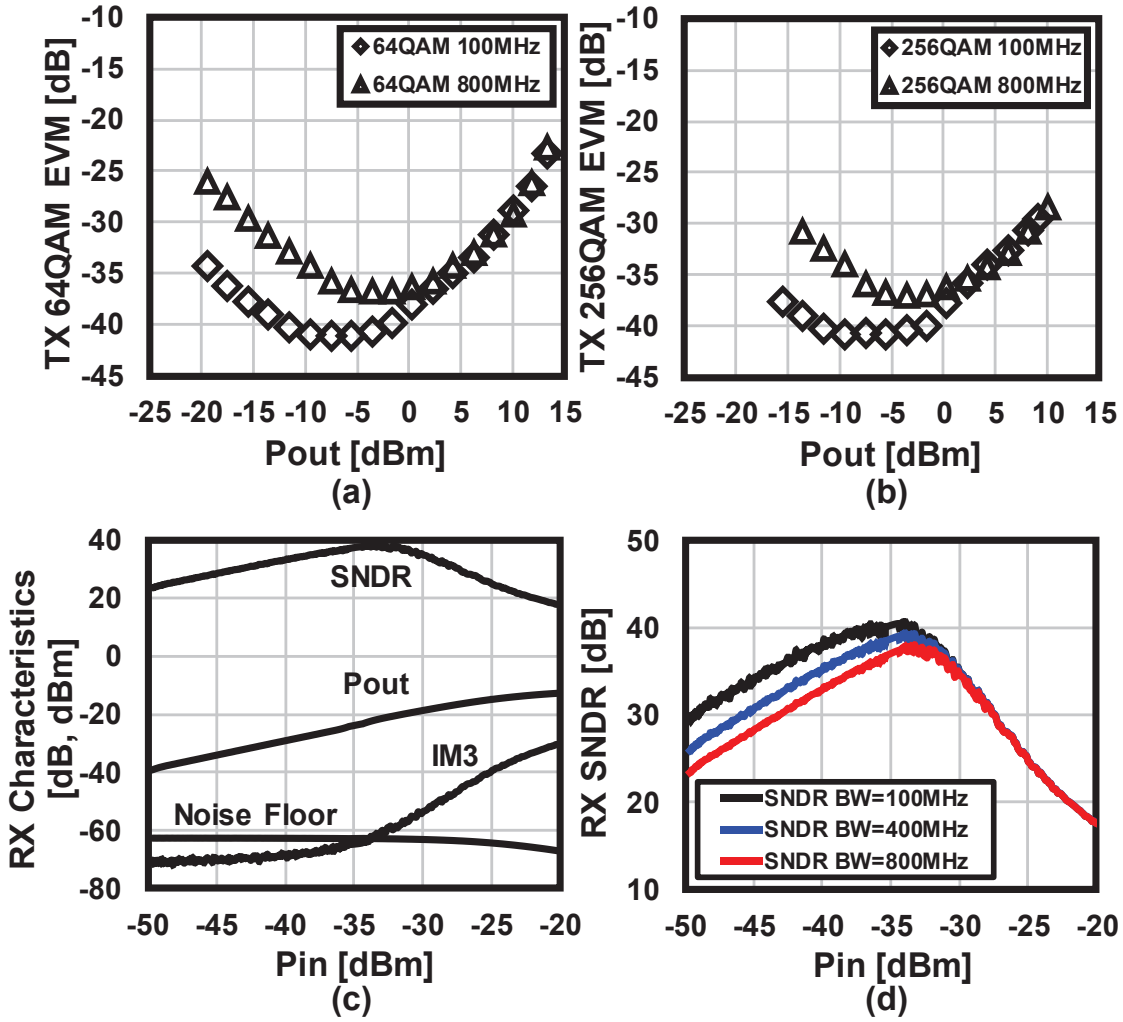


Figure 5.20: Measured (a) TX EVM in 64-QAM; (b) TX EVM in 256-QAM; (c) RX output power, IM3, noise floor, and SNDR at 28 GHz and (d) RX SNDRs with different input signal bandwidths.

efficiency (PAE) is always desirable. To achieve larger power delivery, the PA in this work also adopts differential topology. Fig. 5.13 shows the circuit schematic of the proposed two-stage PA. The input of the driver stage is designed based on the reliable and compact TL matching. Both the driver and final stages are designed based on the common-source (CS) topology. At the output, a balun optimized with low insertion loss is utilized to combine the differential signals to single-ended. The 3D model for the balun together with the DC supply line is also shown in the figure. The simulated insertion loss of the balun is 0.6 dB at 28 GHz. Fig. 5.14 shows the on-wafer measurement result for the stand-alone PA. The measured gain at 28 GHz is 13.5 dB. The achieved saturated output

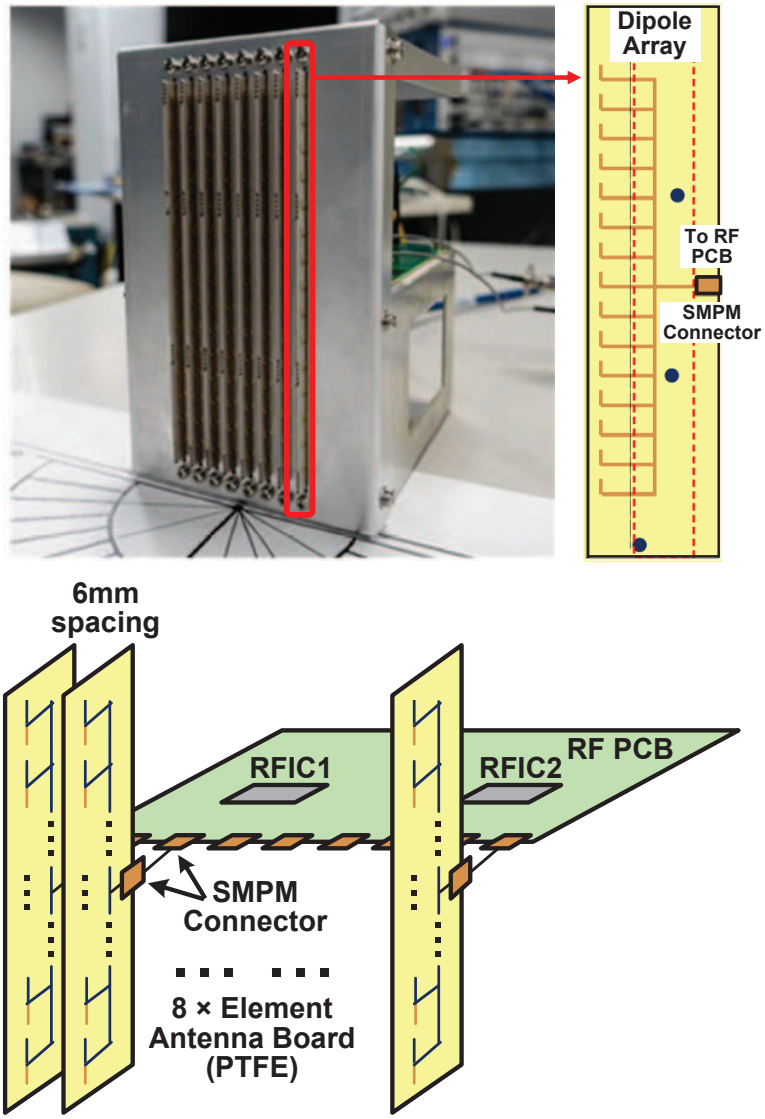


Figure 5.21: Photograph and schematics of eight-element transceiver module and dipole-array antenna.

power is 17.7 dBm with an output P_{1dB} of 16.1 dBm. Fig. 5.14 (b) demonstrates the corresponding PAE against the output power. The peak PAE realized by this work is 30.6% at a 17.5-dBm output. The measured PAE at P_{1dB} is 23.2%.

5.2.3 Receiver

A 28-GHz receiver demands optimizations with respect to noise figure and linearity. As a result, a three-stage CS LNA with an optimized NF is utilized in this work. Fig. 5.15

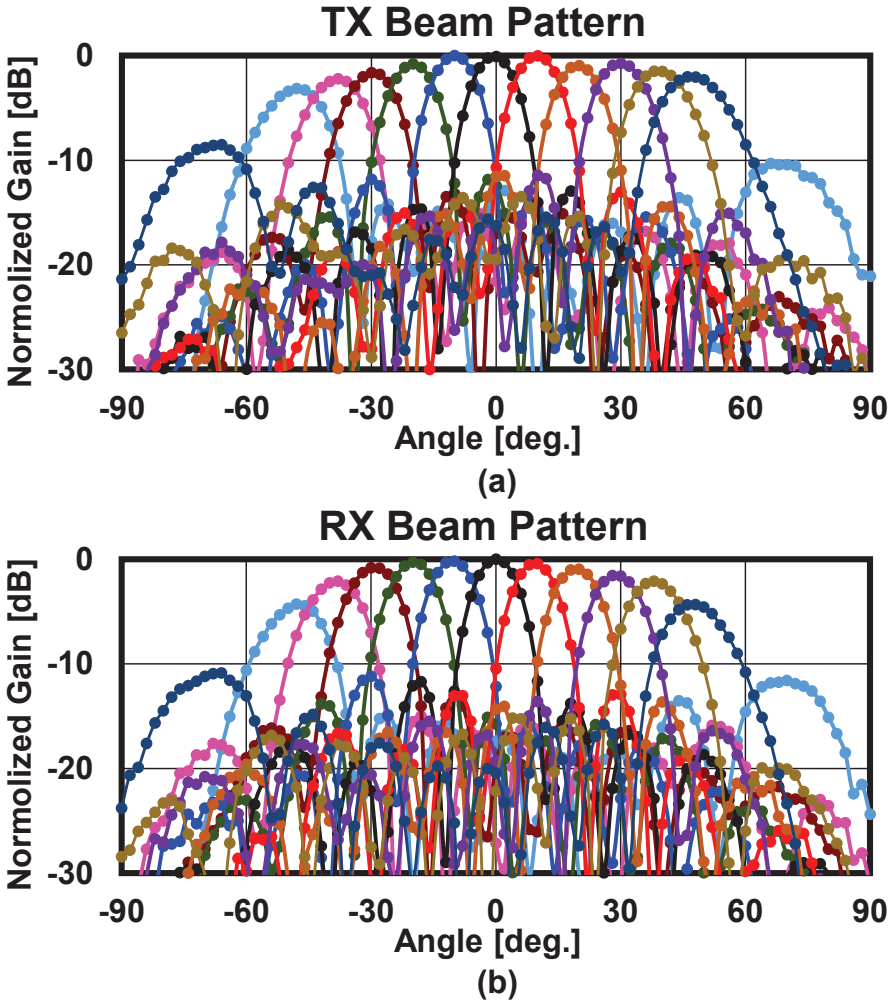


Figure 5.22: Measured beam patterns for eight-element transceiver module: (a) TX mode and (b) RX mode.

shows the circuit schematic of the LNA. The single-ended LNA is designed based on TL matching. At the RF input, a shunt stub shorted to ground is applied for electrostatic discharge protection. Regarding the potentially received out-of-band interferences, such as the LO leakage and image mentioned in Section 5.1, an LC notch designed at the image and LO frequency is inserted at the third stage. Fig. 5.16 shows the measured IRR for the receiver against the input RF frequency. The measurement is carried out with a fixed LO frequency of 24 GHz. Within the 5G NR band n257, the measured IRR is always higher than 30 dB. The rejection at the 24-GHz LO frequency is higher than 22 dB. Additionally, the single-ended output of the LNA is further transformed into differential output by a 28-GHz balun. A differential RF VGA is inserted to suppress the balun mismatch and provide the variable gain.

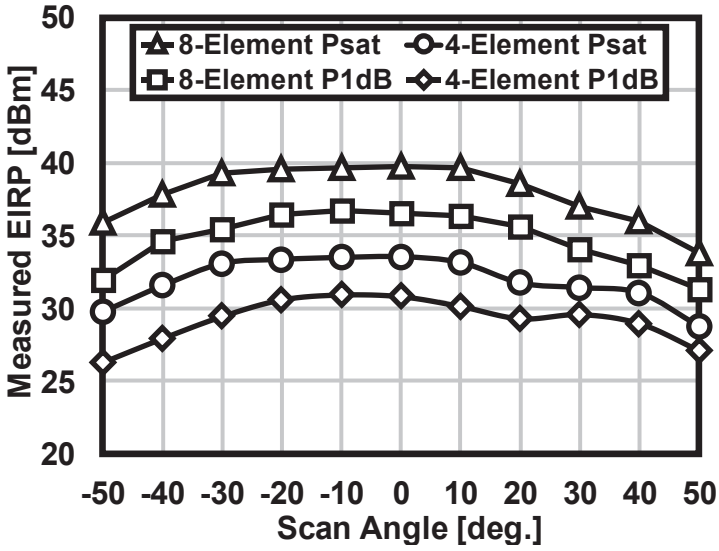


Figure 5.23: Measured EIRPs for (a) four-element and (b) eight-element phased-array transceiver modules.

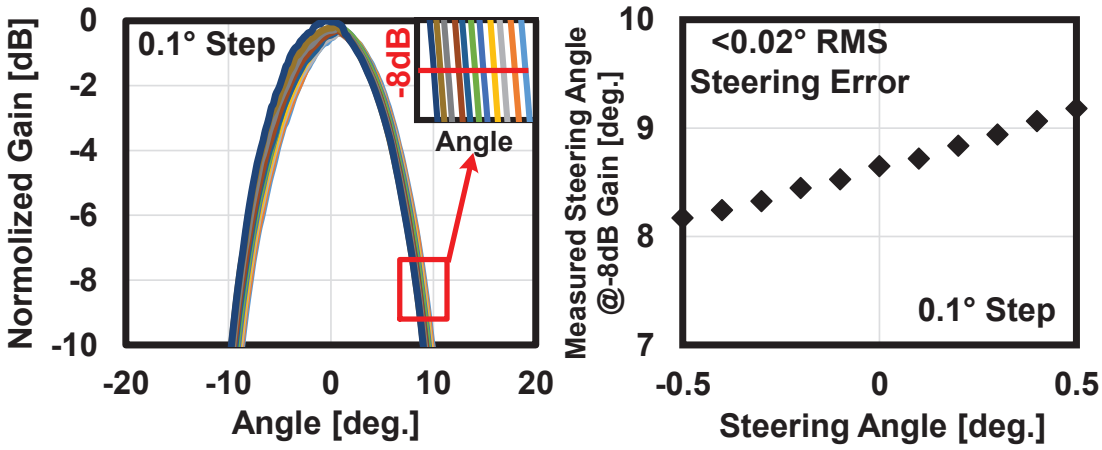


Figure 5.24: Measured beam-steering performance of proposed eight-element phased-array transceiver.

The down-conversion mixer in LO phase shifting phased-array transceivers are exposed to spatial blockers. Careful design considerations will be required both in system and building block levels. In this work, a passive double-balanced mixer with an optimized IIP3 is utilized for down-conversion. A simulated IIP3 of 15dBm is achieved for the mixer, which will not limit the blocker-tolerance of system. Facing a strong spatial blocker, the receiving performance can be improved by decreasing the gain of the LNA and RF VGA.

Table 5.2: Power Consumption of Blocks

	Sub Blocks	**Power Consumption** [mW]
TX	PA	179.8
	RF Buf.	31.6
	Mixer	0.6
RX	LNA	30.6
	RF Buf.	19.5
	Mixer	0.7
LO	Multiplier	37.1
	LO Switch & Buf.	28.0
	PPF Buf.	44.4
	LO Phase Shifter	10.3
	2-Stage LO Buf.	16.6

5.3 Measurement Results

The proposed 28-GHz four-element phased-array transceiver is fabricated in a standard 65-nm CMOS process. Fig. 5.17 (a) shows a die micrograph of the chip. The chip size is 3 mm × 4 mm. Table 5.1 denotes the core area breakdown of the key building blocks. A single-element transceiver occupies an on-chip area of 1.85 mm^2. To evaluate the characteristics of the proposed transceiver array, RF printed circuit boards (PCBs) are designed for the transmitter and receiver arrays separately. Fig. 5.17 (b) shows the PCB for the transmitter array. Two chips are wire-bonded to the PCB. The transmitter outputs from the chips are connected to 50-ohm transmission lines and further distributed symmetrically to SMPM connectors. This work assumes a 0.5-nH bond wire inductance. Matching networks for compensating the inductance are inserted on both the chip and the PCB. The insertion loss of the PCB is measured by comparing the saturated transmitter-mode output power of the on-wafer measurement and the PCB measurement. A PCB loss of 6.04 dB is observed at 28 GHz including the bond wire and the SMPM connectors. The measured magnitude and phase mismatches between channels are less than 2.9 dB and 9.2°, respectively. During the over-the-air (OTA) measurement, the mismatches are compensated by tuning the RF VGA and LO phase shifter. For evaluating the receiver array, a similar PCB is also implemented.

Fig. 5.18 shows the measured characteristics of a single-element transmitter and receiver. Within the frequency range of 26.5 to 29.5 GHz, the measured transmitter-mode conversion gain is around 10 dB. Fig. 5.18 (b) shows the measured on-wafer output power and the PAE at P_{1dB} of the transmitter. The proposed transmitter achieves a saturated

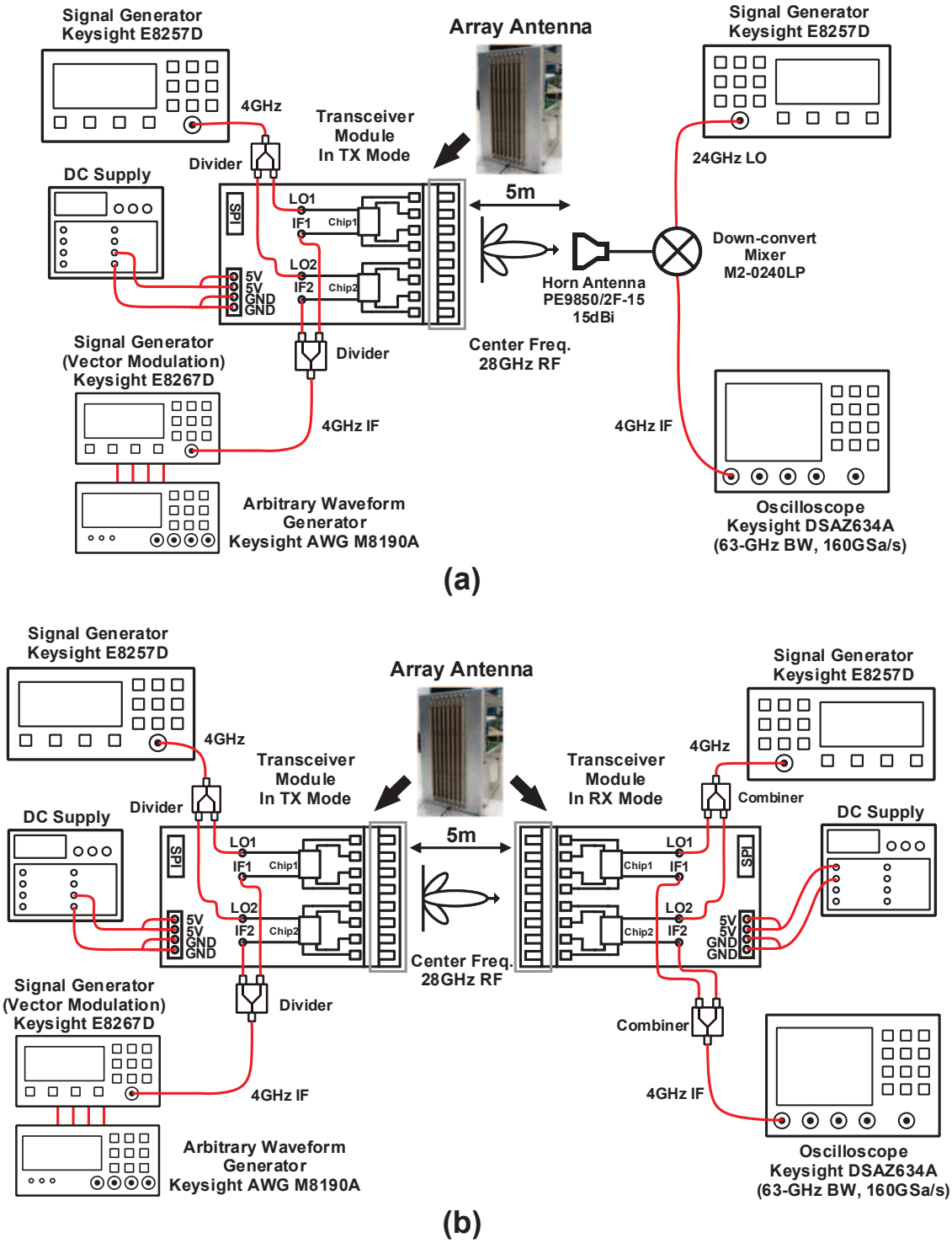
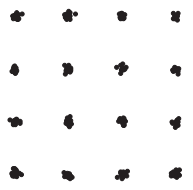
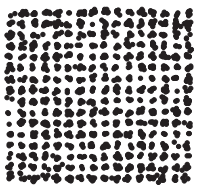
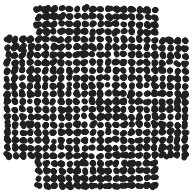


Figure 5.25: Equipment setup for the 5-m over-the-air (OTA) measurement.

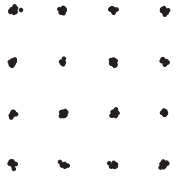
5m OTA Measurement	Modulation	QPSK	16QAM	64QAM
	Symbol rate	2.5GS/s	2.5GS/s	2.5GS/s
	Bandwidth*	3.1GHz*	3.1GHz*	3.1GHz*
	Data rate	5Gb/s	10Gb/s	15Gb/s
	Beam direction	0°	0°	0°
	Constellation**			
	TX EVM (RMS)**	-28.8dB (3.6%)	-28.7dB (3.7%)	-27.9dB (4.0%)
	TX-to-RX EVM (RMS)***	-25.5dB (5.3%)	-25.1dB (5.6%)	-25.2dB (5.5%)

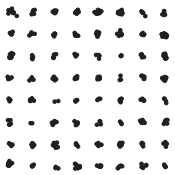
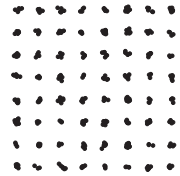
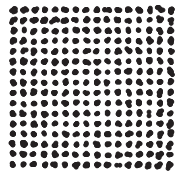
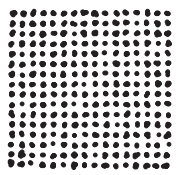
5m OTA Measurement	Modulation	256QAM	512QAM
	Symbol rate	1.6GS/s	0.8GS/s
	Bandwidth*	2.0GHz*	1.0GHz*
	Data rate	12.8Gb/s	7.2Gb/s
	Beam direction	0°	0°
	Constellation**		
	TX EVM (RMS)**	-30.9dB (2.9%)	-35.0dB (1.8%)
	TX-to-RX EVM (RMS)***	-29.3dB (3.4%)	-32.7dB (2.3%)

*The roll-off factor is 0.25.
**Constellation, and TX EVM are measured with an external downconverter.
***TX-to-RX EVM(RMS) is measured through TX and RX, which is equivalent to –SNR(MER).

Figure 5.26: Summarized constellation, TX EVM, and TX-to-RX EVM for eight-element phased-array transceiver module in 5-m OTA measurement.

output power of 18.0 dBm along with an output P_{1dB} of 15.7 dBm at 28 GHz. The measured 28-GHz PAE is 10.3% at P_{1dB}. Fig. 5.18 (c) shows the measured conversion gain against the frequency for the receiver. The flat frequency response of the receiver optimizes the EVM performance. The measured NF for the receiver in this work is less than 5 dB from 26.5 to 29.5 GHz. At 28 GHz, the achieved NF is 4.1 dB. Fig. 5.19 (a) demonstrates the measured LO leakage power against the frequency for the transmitter. A less than -50 dBm leakage power can be observed at 24 GHz. Regarding the image rejection, the measured IRR is larger than 40 dBc from 2.5 to 5.5 GHz IF. Spurious emissions are

5m OTA Measurement	Modulation	QPSK	QPSK	16QAM	16QAM
	Symbol rate	2GS/s	2GS/s	2GS/s	2GS/s
	Bandwidth*	2.5GHz	2.5GHz	2.5GHz	2.5GHz
	Data rate	4.0Gb/s	4.0Gb/s	8.0Gb/s	8.0Gb/s
	Beam direction	20°	50°	20°	50°
	Constellation**				
	TX EVM (RMS)**	-31.6dB (2.6%)	-31.4dB (2.7%)	-31.4dB (2.7%)	-31.1dB (2.8%)
	TX-to-RX EVM (RMS)***	-29.6dB (3.3%)	-28.4dB (3.8%)	-29.0dB (3.5%)	-28.2dB (3.9%)

5m OTA Measurement	Modulation	64QAM	64QAM	256QAM	256QAM
	Symbol rate	2GS/s	2GS/s	800MS/s	800MS/s
	Bandwidth*	2.5GHz	2.5GHz	1.0GHz	1.0GHz
	Data rate	12.0Gb/s	12.0Gb/s	6.4Gb/s	6.4Gb/s
	Beam direction	20°	50°	20°	50°
	Constellation**				
	TX EVM (RMS)**	-31.3dB (2.7%)	-30.9dB (2.9%)	-36.3dB (1.5%)	-35.9dB (1.6%)
	TX-to-RX EVM (RMS)***	-29.2dB (3.5%)	-27.8dB (4.1%)	-33.4dB (2.1%)	-30.7dB (2.9%)

*The roll-off factor is 0.25.
**Constellation, and TX EVM are measured with an external downconverter.
***TX-to-RX EVM(RMS) is measured through TX and RX, which is equivalent to –SNR(MER).

Figure 5.27: Measured beam scan performance of eight-element phased-array transceiver module in 5-m OTA measurement.

suppressed by this work.

Fig. 5.20 (a) shows the measured SC mode EVM in 64-QAM for the transmitter. The peak EVM in 64-QAM is -41.1 dB for a 100-MHz bandwidth and -36.7 dB for a 800-MHz bandwidth. Concerning the required -26-dB transmitter EVM in 64-QAM for a less-than-10^{-3} TX-to-RX bit error rate [31], the proposed transmitter achieves a 11.7-dBm output power. Fig. 5.20 (b) demonstrates the measured EVM in 256-QAM. The peak EVMs in 256-QAM are -37.1 dB and -40.8 dB for the 100-MHz and 800-MHz bandwidths, respectively. An output power of 6.1 dBm in 256-QAM is achieved at the -32.9-dB EVM. Still, a larger-than-1-dB margin is left at the output power mentioned above for the required -31.5-dB transmitter EVM in 256-QAM. For the single-element receiver, the output power, IM_3, and the output noise floor are measured at 28 GHz and

shown in Fig.5.20 (c). The calculated SNDR of the receiver with different bandwidth is shown in Fig. 5.20 (d). The maximum SNDRs are 40.8 dB, 39.3 dB and 38.1 dB for bandwidths of 100 MHz, 400 MHz, and 800 MHz, respectively.

The transmitter and receiver PCBs are further implemented into eight-element transmitter and receiver modules. Fig. 5.21 shows a photograph of the transmitter module. A total of eight antenna elements are connected to the PCB through the SMPM connectors with a 6-mm spacing. The 15-element dipole-array antennas are utilized for the element-antenna in this work [77, 78]. A cosecant-squared shaping beam in elevation is achieved by the dipole-array. The measured element-antenna gain at 0° in elevation is 11.9 dBi.

The beam patterns of the eight-element transceiver modules are evaluated with an additional standard gain horn antenna. The normalized beam patterns in the azimuth plane are demonstrated in Fig. 5.22 with beam scan angles from −50° to +50°. Thanks to the sufficiently small amplitude and phase errors, the measured sidelobe levels are always lower than -9 dBc for the TX mode and -11 dBc for the RX mode. The achieved peak-to-null ratios at 0° scan are higher than 29 dB and 23 dB for the TX and RX modes, respectively. The measured EIRPs against the beam scan angle for the transmitter module are shown in Fig. 5.23. The achieved saturated EIRP is 39.8 dBm for eight-element transmitter and 33.6 dBm for four-element transmitter at 0° scan. The observed 6-dB difference in EIRP matches with the theory. The measured EIRPs at P_{1dB} are 36.5 dBm and 30.8 dBm for eight-element and four-element transmitters, respectively.

The beam-steering performance is also measured. Fine varactor tuning of the phase shifter, which covers 30°, is utilized in this measurement. The proposed transmitter module is capable of steering the beam with a 0.1° resolution from −50° to +50° in azimuth plane with the help of the very-fine phase shifting resolution. The normalized beam patterns for the beam-steering is shown in Fig. 5.24. The RMS steering error is calculated from the angles at a normalized gain of -8 dB. With the help of the gain-invariant and quasi-continuous phase tuning, the proposed transceiver module demonstrates an RMS steering error of less than 0.02° from −0.5° to +0.5°.

During the OTA measurement, the performance of the eight-element phased-array transceiver is also evaluated with the SC-mode modulated signal. Fig. 5.25 demonstrates the equipment setups for the TX and TX-to-RX constellation measurements. One transmitter module is used for the TX measurement. The modulated signals in QPSK, 16-QAM, 64-QAM, and 256-QAM with a 4-GHz frequency offset are generated by an arbitrary waveform generator (AWG). The radiated signal within a beam angle of −50° to +50° is received by a standard gain horn antenna at a 5-m distance. An external down-converter is utilized to down-convert the received signal to low frequency. The EVM and constellation are evaluated with an oscilloscope. For the TX-to-RX measurement, one

Table 5.3: Performance Comparison of 28-GHz Phased-Array Transceivers

	This work		Qualcomm [5]	IBM [2]	UCSD [8]	
Process	65nm CMOS		28nm CMOS	0.13μm SiGe	0.18μm SiGe	
P1dB/path	15.7dBm		12.0dBm***	14.0dBm***	10.5dBm***	
Psat/path	18.0dBm		14.0dBm***	16.4dBm***	12.5dBm***	
RX NF	4.1dB		4.4-4.7dB***	3.7dB***	4.6dB***	
TX Gain/path @28GHz	10dB		15dB*	32dB	17dB*	
RX Gain/path @28GHz	12dB		15dB*	34dB	17dB*	
Integration/chip	4xTRX		24xTRX	32xTRX	4xBeam Former	
PDC/path	TX: 299mW @11dBm/path RX:148mW		TX: 119mW @11dBm/path RX: 42mW	TX: 319mW @16dBm/path RX: 206mW	TX: 200mW @11dBm/path RX: 130mW	
Chip Area	12mm^2		29mm^2	166mm^2	12mm^2	
PS Architecture	LO PS		RF PS	RF PS	RF PS	
RMS Gain Error	< 0.04dB		N/A	Gain var. < 1.5dB	< 0.8dB	
RMS Phase Error	0.3°		N/A	<0.8°	<6°	
Phase Res./Step	2+3+10 bit/0.3° ****		3 bit/45°	41 Seg./4.9°	6 bit/6° ****	
Module Array Size	8×1		4×1	8×8	8×4	
Antenna Integration	Antenna on PCB		Antenna on PCB	Antenna in Package	Antenna on PCB	
EIRP@Psat	39.8dBm		35.0dBm/pol.	54.0dBm/pol.	45.0dBm	
Polarization	Single-Pol.		Dual-Pol.	Dual-Pol.	Single-Pol.	
Dimensions of Beam Scanning	Azimuth only		Azimuth +Elevation	Azimuth +Elevation	Azimuth +Elevation	
Beam Steering Resolution	0.1°		N/A	1.4°	1°	
Distance	5.0m		N/A	N/A	5.0m	
Constellation	64 QAM	512 QAM	64QAM	256QAM*	16 QAM	256 QAM
Max Symbol Rate	2.5GS/s	0.8GS/s	0.4GS/s (TX only)*	N/A	1.5GS/s	0.25GS/s
Max Data Rate	15Gb/s	7.2Gb/s	N/A	3.5Gb/s*	6Gb/s	2Gb/s
TX-to-RX EVM (800MS/s)	1.7%**	2.3%**	TX EVM=0.9% (100MS/s)	N/A	6.1%*	2.1% (250MS/s)

* Estimated from the material. ** Referred to the RMS magnitude of the constellation.
*** TRX switch included. **** Step limited by phase error.

transmitter module and one receiver module are utilized. The TX-to-RX EVMs are also tested at a 5-m distance. The beam directions for both modules are set to 0°, 20°, and 50°. The summarized TX constellation, TX EVM, and TX-to-RX EVM at 0° are shown in Fig. 5.26. Within a 5-m distance, the proposed eight-element module achieves maximum data rates of 5 Gb/s in QPSK, 10 Gb/s in 16-QAM, 15 Gb/s in 64-QAM, 12.8 Gb/s in 256-QAM, and 7.2 Gb/s in 512-QAM. The corresponding TX EVM and TX-to-RX EVMs are, respectively, -28.8 dB and -25.5 dB for QPSK, -28.7 dB and -25.1 dB for 16-QAM, -27.9 dB and -25.2 dB for 64-QAM, -30.9 dB and -29.3 dB for 256-QAM, and -35.0 dB and -32.7 dB for 512-QAM. All of the measured EVMs meet the requirements for a bit error rate of 10^{-3}. The beam scan performance summary of the eight-element module is demonstrated in Fig. 5.27. At a 5-m distance, data streams of 2 GSymbol/s in QPSK, 16-QAM, and 64-QAM and 800 MSymbol/s in 256-QAM are supported by the proposed module within ±50°. Data rates of 4 Gb/s in QPSK, 8 Gb/s in 16-QAM, 12 Gb/s in 64-QAM, and 6.4 Gb/s in 256-QAM are realized.

Table 5.2 shows the power consumption breakdown for the proposed phased-array transceiver. The measured power consumption in transmitter mode for the whole chip is 1.2 W at an output power of 11 dBm per path. In receiver mode, the power consumption is 0.59 W. Table 5.3 compares this work with some state-of-the-art 28-GHz phased-array transceivers. The proposed LO phase shifting transceiver chip achieves measured RMS gain and phase errors of less than 0.04 dB and 0.3°, respectively. Excellent transmitter linearity and receiver NF characteristics are also maintained with moderate power consumption. Regarding the 5-m OTA measurement, the proposed eight-element module reports the constellations up to 512-QAM. The achieved data rates in 256-QAM and 512-QAM are 12.8 Gb/s and 7.2 Gb/s, respectively. A maximum data rate of 15 Gb/s in 64-QAM is realized by the module.

5.4 Conclusion

In this paper, a CMOS 28-GHz four-element phased-array transceiver designed for 5G NR is implemented. The proposed transceiver based on the LO phase shifting architecture achieves an RF gain-invariant and continuous phase tuning. The measured RMS gain and phase errors are less than 0.04 dB and 0.3°, respectively. Accurate beam control with suppressed sidelobe and spurious radiations can be supported by this work. The eight-element transceiver modules developed in this work are capable of scanning the beam from −50° to +50°. During the 5-m OTA measurement, the proposed eight-element modules report the first 512-QAM constellation in the 28-GHz band. A data rate of 15 Gb/s in 64-QAM is realized by the modules. In addition, within a beam scan angle of

±50°, the developed modules support 6.4-Gb/s data rate in 256-QAM. Stabilized and high-data-rate communications could be achieved within all beam scan angles.

Chapter 6

Neutralized Bi-Directional Phased-Array Transceiver

To cover enough communication distance, as mentioned in Chapter 2, the millimeter-wave phased-array transceivers designed for the 5G NR requires a large array size. In consideration of the beamforming and MIMO configuration, the system size, weight along with the manufacturing cost will be increased due to the required numerous number of antennas and element-transceivers. As a result, reducing the physical size and cost will be essential for a 5G MIMO system.

To reduce the physical size of the MIMO system, dual-polarized MIMO technique could be applied. DP-MIMO system utilizes the cross-pol. isolation of the dual-pol. antennas for MIMO communication. As shown in Fig. 6.1, two data streams named horizontal-stream and vertical-stream are transmitted simultaneously from the TX array to the RX array. Due to shared aperture between the H and V streams, the required antenna number could be reduced to half for a 2X2 MIMO configuration. A compact system size along with a small system weight could be realized. Fig. 6.2 shows a link budget example for a 500-m data communication. The modulation scheme is 64-QAM. Array sizes of 256 and 4 are selected for the TX side and the RX side, respectively. Although the communication distance could be covered with 4 dB margin, the required numerous number of element-transceivers still occupy huge on-chip area which increases the manufacturing cost.

To further decrease the manufacturing cost due to the chip area, the bi-directional technique could be also be utilized for the 28 GHz phased-array transceivers. Fig. 6.3 (a) shows the circuit schematic of a conventional bi-directional beamformer. For a larger power delivery, usually differential topology is widely adopted by 5G millimeter-wave transceivers. Similar to the bi-directional amplifier mentioned in the previous chapter, to

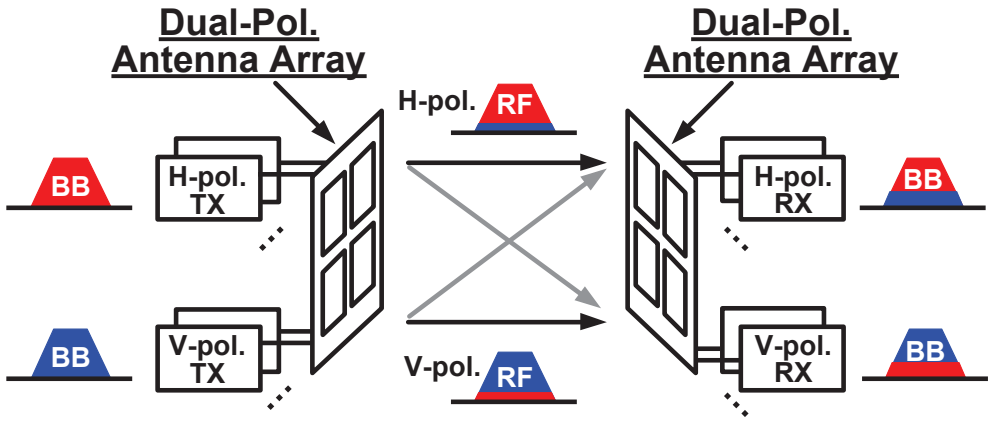


Figure 6.1: Dual-polarized MIMO.

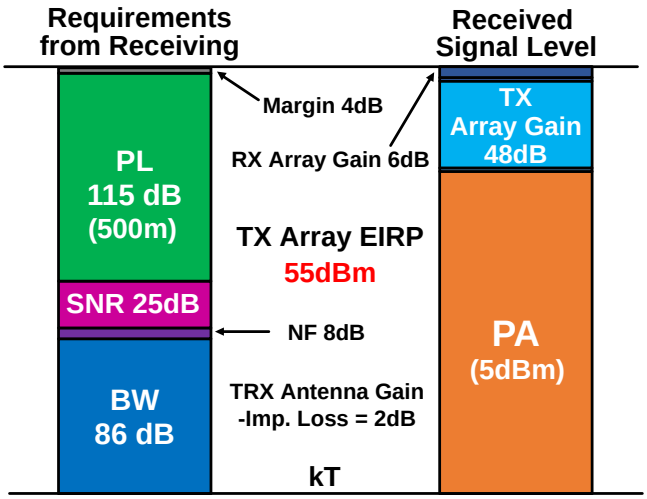


Figure 6.2: Link budget for MIMO communication.

support the bi-directional operation, two TRX switches are utilized at the ends of two amplifier chains. As a result, bi-directional operation could be supported and the passive phase shifter could be shared. However the unshared inter-stage passive components of the conventional design still occupies huge on-chip area. To address this issue, Fig. 6.3 (b) shows the proposed full differential bi-directional beamformer. In this work, a neutralized bi-directional core which allows the sharing of the inter-stage matching is utilized. The additional IL caused by the matching sharing could be compensated by the proposed core in both TX mode and RX mode. Regarding the different requirements from the PA and LNA, an unbalanced neutralized core is proposed. Finally, usually the passive phase shifters are utilized in the conventional design for supporting the bi-directional operation.

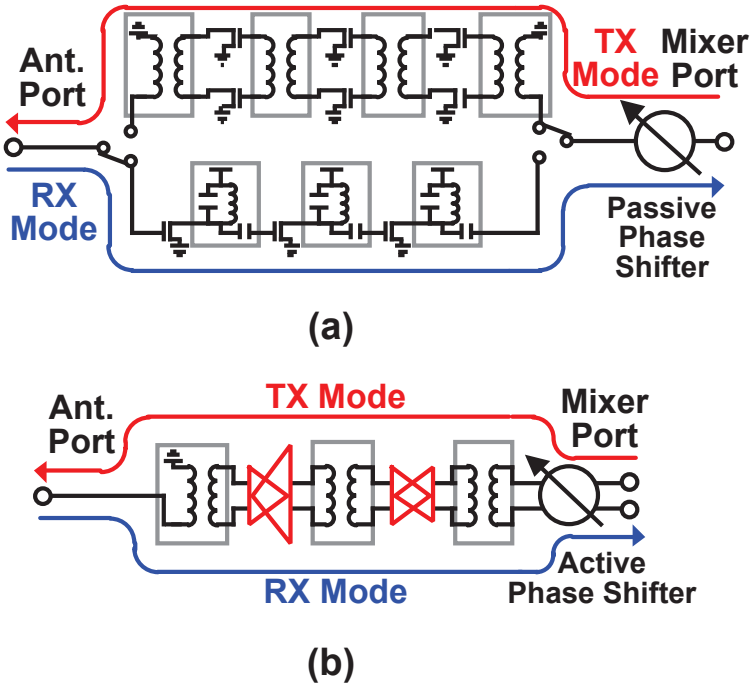


Figure 6.3: (a) Conventional bi-directional beamformer and (b) proposed full-differential bi-directional beamformer.

However such phase shifters require gain compensation, which increase the power and area consumptions. As a result, in this work an active bi-directional vector-summing phase shifter is proposed. An improved phase tuning resolution could be realized with a compact on-chip area. The detailed circuits for the proposed bi-directional chip will be introduced in the following section.

6.1 Circuit Implementation

Fig. 6.4 shows the system block diagram. Totally 8 element beamformers are integrated in the same chip. To maintain the DP-MIMO configuration, 4 of the beam formers are for the H polarization and the other 4 elements are for the vertical polarization. In consideration of the large-sized phased-array and MIMO configuration in 5G NR, bi-directional technique is utilized in this work for minimizing the on-chip area. The proposed array beamformer is capable of operating in TX and RX modes with the same bi-directional circuit chain. A single-element beamformer consists of 2-stage PA-LNA, RF buffer, phase shifter, and isolation buffer. The 28-GHz signal is distributed by a T-

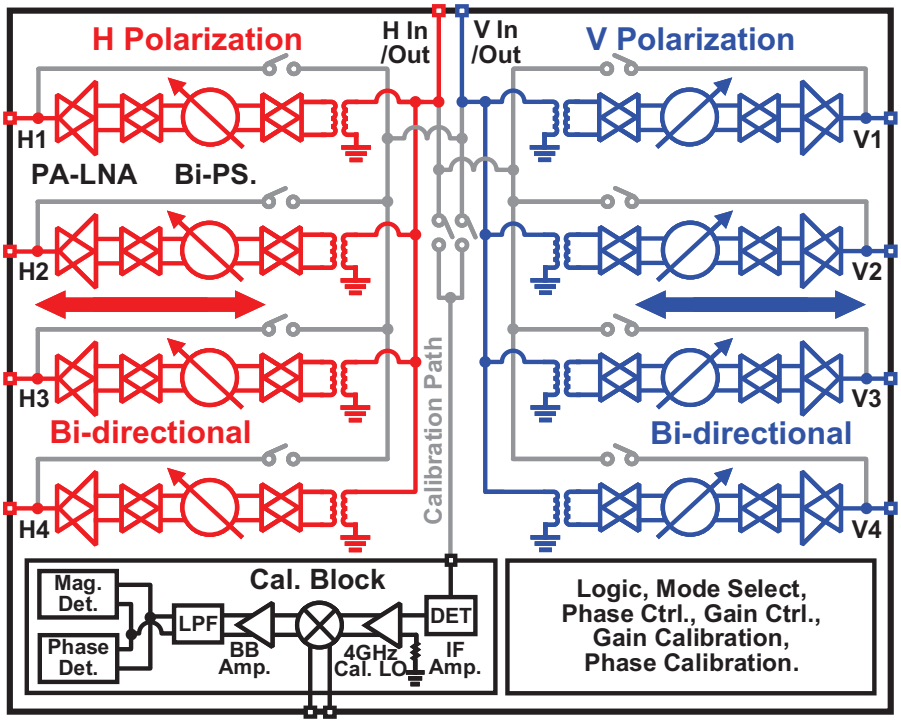


Figure 6.4: Block diagram of the proposed bi-directional beamformer chip.

TX	Divider	BIPS w Buffer	RF Buffer	PA	Board loss	Total
Power Gain [dB]	-10.00	2.00	8.00	10.00	-3.00	
Cumulative Gain [dB]	-10.00	-8.00	0.00	10.00	7.00	7.00
NF [dB]	10.00	13.00	8.50	8.00	3.00	
Cumulative NF [dB]	10.00	23.00	23.76	23.86	23.86	23.86
OIP3 [dBm]	100.00	7.00	14.00	23.40	100.00	
Cumulative OIP3 [dBm]	100.00	7.00	11.46	19.31	16.31	16.31

RX	Board Loss	LNA	RF Buffer	BIPS w Buffer	Combiner	Total
Power Gain [dB]	-3.00	10.00	8.00	2.00	8.00	
Cumulative Gain [dB]	-3.00	7.00	15.00	17.00	25.00	25.00
NF [dB]	3.00	6.00	8.50	13.00	0.00	
Cumulative NF [dB]	3.00	9.00	9.62	9.89	9.89	9.89
OIP3 [dBm]	100.00	12.00	12.00	4.40	100.00	
Cumulative OIP3 [dBm]	100.00	12.00	11.36	3.88	11.88	11.88

Figure 6.5: Level diagram design of the proposed beamformer chip.

junction divider/combiner to each element in single-ended. After the distribution, an isolation buffer is inserted for suppressing the influence of impedance variation caused by the phase tuning. Thus, independent phase tuning between each element can be realized. For minimizing the magnitude and phase errors between elements, a calibration circuit is integrated into the chip. The calibration paths are shared between H and V. The

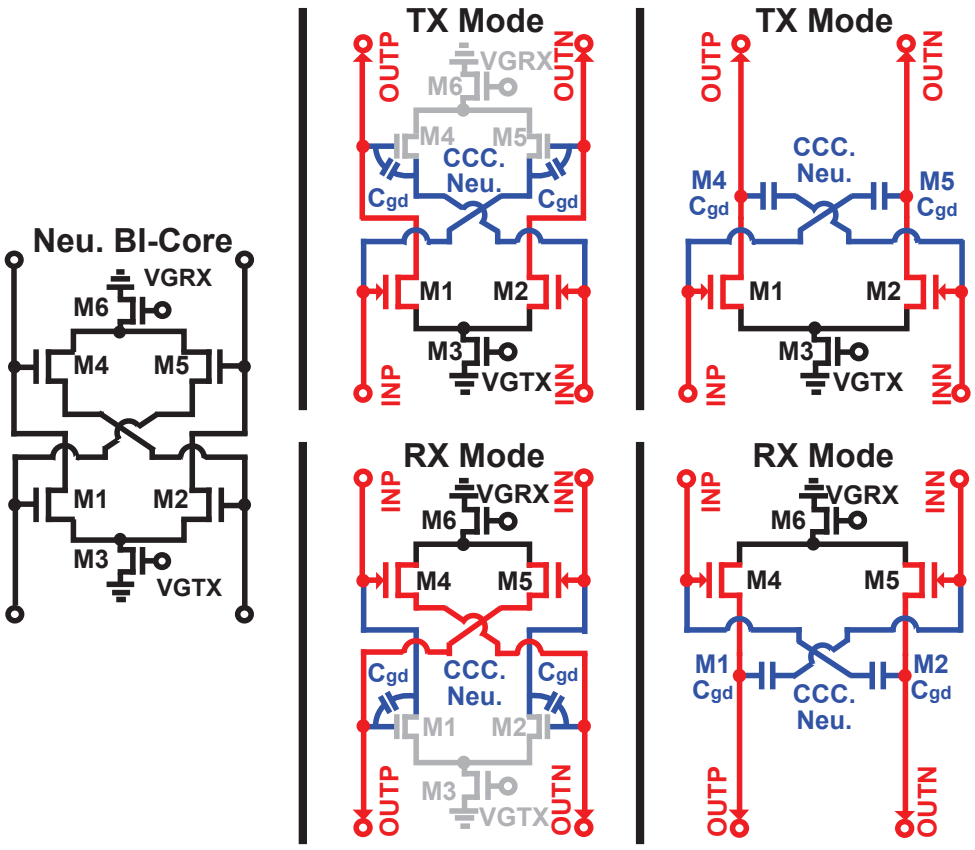


Figure 6.6: Circuit schematic of the proposed neutralized bi-directional core.

simulated cross-pol. isolation is higher than 39 dB at 28 GHz. The beamformer chip can be configured into H/V TX/RX calibration modes by the calibration select switches using quarter-wave-length TL. The redirected 28-GHz signal is down-converted to a low frequency, and then the magnitude and phase detection is performed. Fig. 6.5 shows the system design of the phased-array beamformer chip. The linearity of the TX-mode beamformer and the NF of the RX-mode beamformer are well optimized.

6.1.1 Neutralized Bi-Directional Core

In this work, the bi-directional amplifiers are designed based on the proposed neutralized bi-directional core. Compared with the conventional switch-based bi-directional approach, the proposed bi-directional amplifier completely shares the inter-stage matching networks between the TX and the RX. Thus, the required on-chip area is further minimized. Fig. 6.6 presents the circuit schematic of the proposed neutralized bi-directional core, which consists of two transistor pairs in cross-coupling connection. Transistors M1

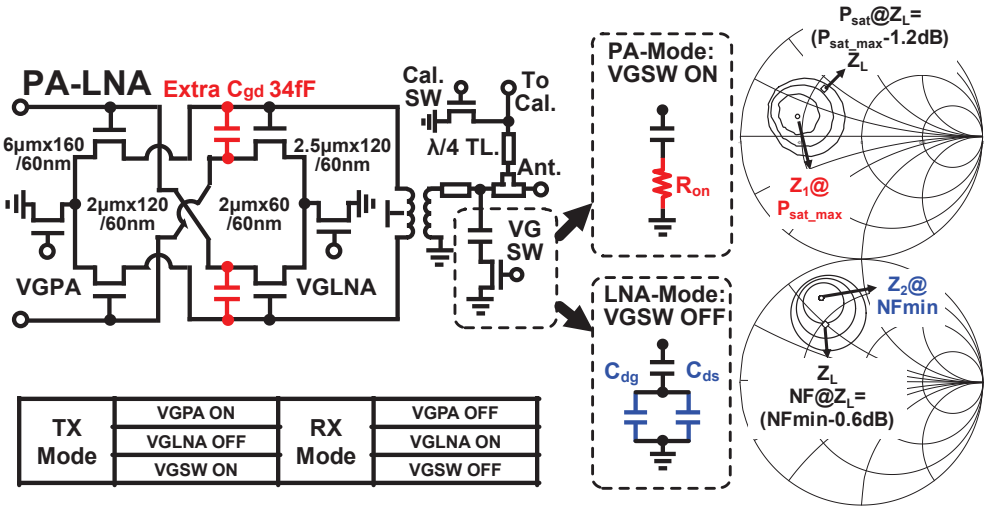


Figure 6.7: Circuit schematic of the proposed PA-LNA.

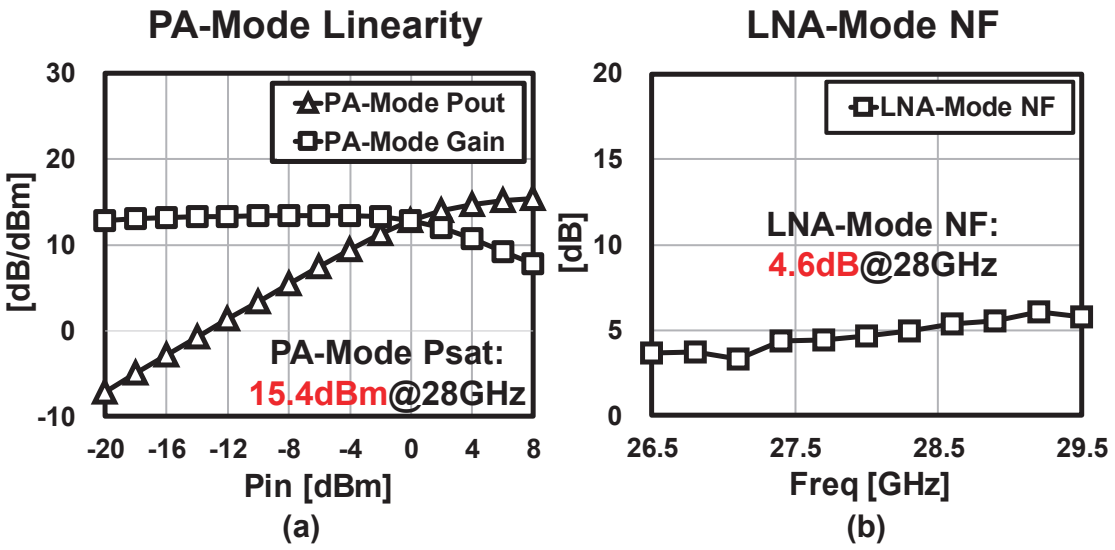


Figure 6.8: Measured on-wafer performance of PA-LNA: (a) measured PA-mode output power and (b) LNA-mode NF.

and M2 are utilized for the TX mode, while M4 and M5 are utilized for the RX mode. The mode selection is realized by switching the tail bias (M3, M6). If the same transistor size is selected for M1-2 and M4-5, the Cgd of M1 and M2 will be neutralized by M4 and M5 in TX mode, while the Cgd of M4 and M5 will be neutralized by M1 and M2 in RX mode. The higher gain characteristics and the enhanced reverse isolation are realized by the proposed bi-directional amplifier, which contributes to low-noise and

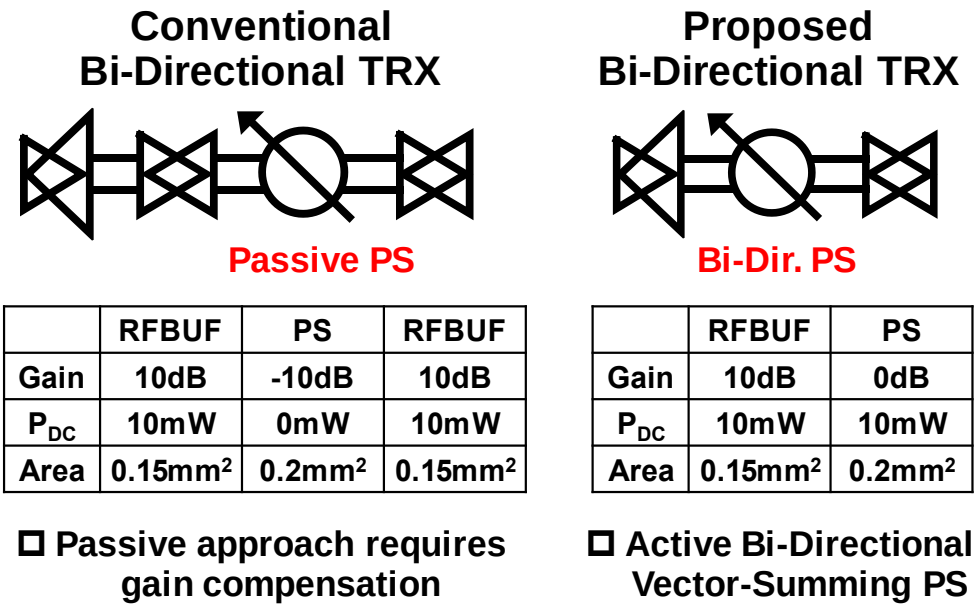


Figure 6.9: System estimation for the conventional passive bi-directional phase shifter and the proposed active vector-summing phase shifter.

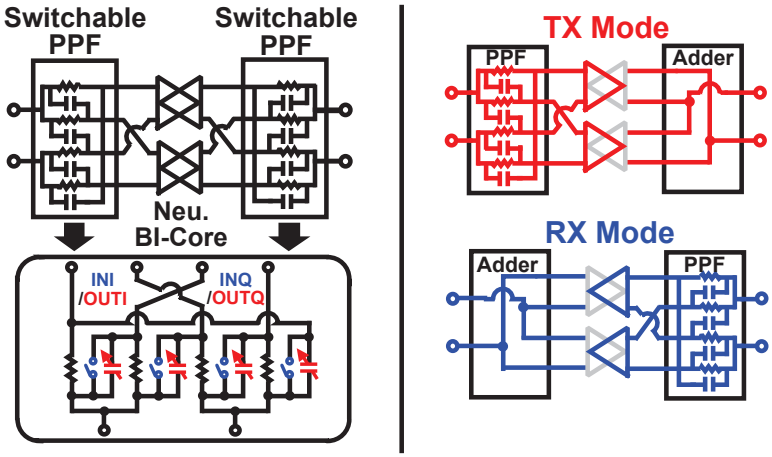


Figure 6.10: Circuit schematic of the proposed active bi-directional phase shifter.

high-stability operation as well as an improved phase tuning isolation. By switching the tail bias, the operation mode could be switched between the TX mode and the RX mode for a TDD system. While, regarding the FDD implementation, the proposed neutralized bi-directional core could not be utilized. When both of the tail bias for TX transistor pair and RX transistor pair are turned on, cancellation of the input signal will occur.

Fig. 6.7 demonstrates the circuit schematic of the proposed PA-LNA. Due to the

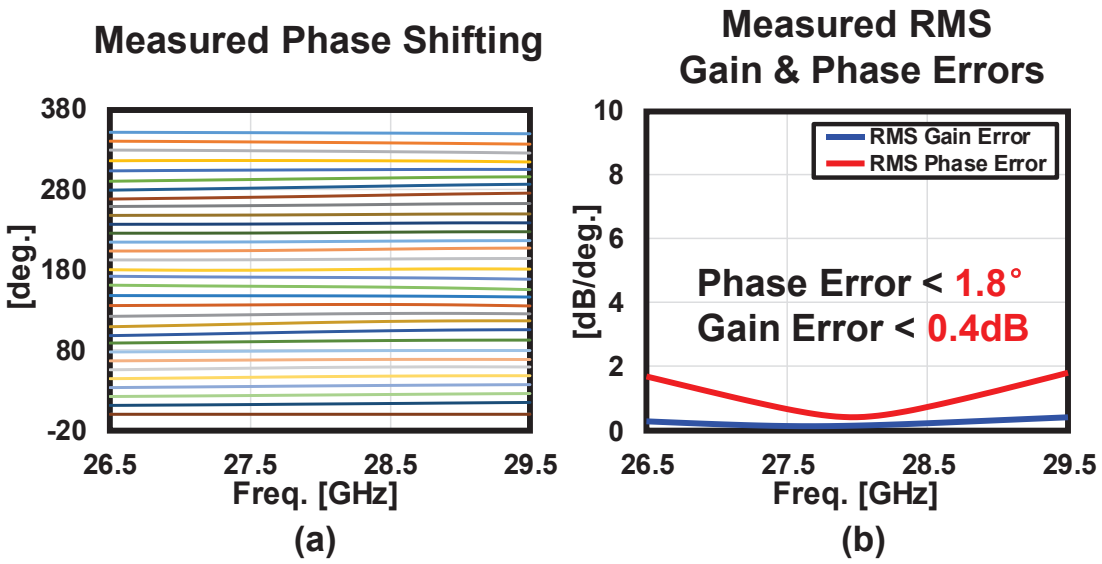


Figure 6.11: (a) Measured phase shifting and (b) RMS phase and gain errors of the proposed bi-directional phase shifter.

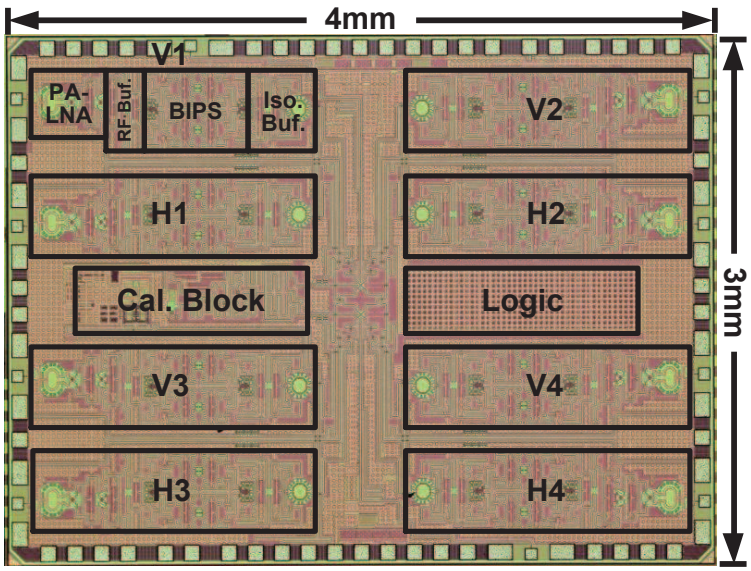


Figure 6.12: Die micrograph of the proposed chip.

different transistor size requirements for PA and LNA, an unbalanced bi-directional amplifier architecture is proposed. Extra capacitors Cgd are attached to the LNA transistor to compensate the additional Cgd from the PA transistor. As a result, neutralization can be realized in both operation modes. The PA and LNA share the antenna node in a switch-

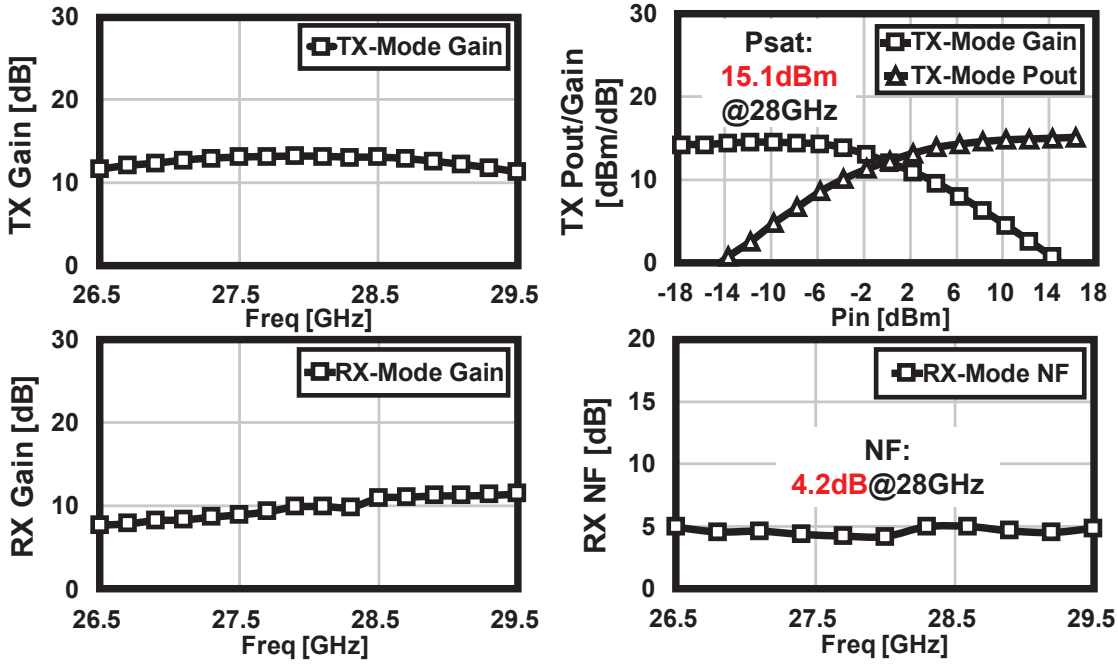


Figure 6.13: Measured on-wafer characteristics of the single-path beamformer.

less manner. A large capacitor in series with a small switching transistor is attached to the antenna node. By switching the transistor, the output matching network can be adapted to the required impedance for PA and LNA. The measured on-wafer characteristics of a standalone PA-LNA is shown in Fig. 6.8. Fig. 6.8 (a) shows the measured output power of the PA. A saturated output power of 15.4 dBm is achieved at 28 GHz. The corresponding P1dB is 13 dBm. For the LNA-mode, the measured NF is 4.6 dB at 28 GHz. Within the frequency range of 26.5 GHz to 29.5 GHz, the measured NF is always less than 6 dB.

6.1.2 Bi-Directional Phase Shifter

As mentioned in the previous section, the phase shifters in a bi-directional transceiver also requires design considerations. Not only the bi-directional operation but also a minimized system area and power consumptions are required to be achieved. Usually, the passive phase shifters are utilized for supporting bi-directional operation. However, the insertion loss of the passive solutions require compensation at the RF path. Fig. 6.9 shows the system estimation with conventional passive bi-directional phase shifter. Although the passive phase shifter consumes 0 power consumption, to realize enough RF path gain, additional RF buffer will be required for gain compensation. To address this issue, this work adopt an active bi-directional vector summing phase shifter. An improved gain

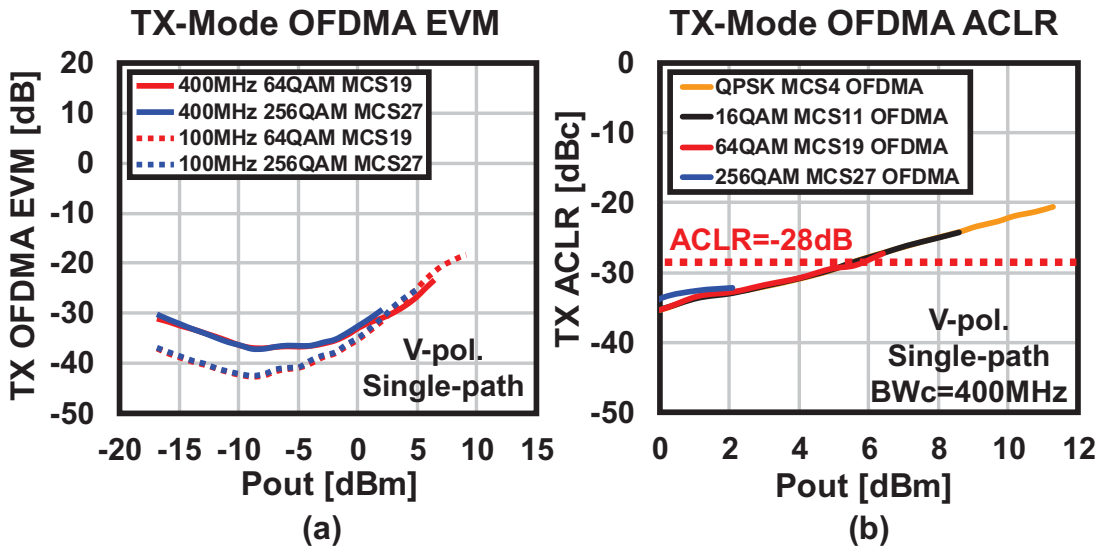


Figure 6.14: Measured (a) OFDM-mode EVM and (b) the corresponding ACLR of the TX-mode beamformer.

characteristic could be supported by the proposed phase shifter. An area-efficient system could be achieved by removing the RF buffer for gain compensation. Fig. 6.10 shows circuit schematic of the phase shifter. Two switchable poly-phase filters are utilized in the proposed phase shifter. They can be configured into the normal PPF mode or the adder mode. In both TX and RX modes, one of the switchable PPF is configured into PPF mode, while the other one is configured into adder mode. The VGAs in such a phase shifter are also based on the proposed neutralized bi-directional core. As a result, the vector summing could be realized in both TX and RX modes. The bi-directional operation could be supported with an improved gain performance. Fig 6.11 shows the measured phase shifting for a 5-bit phase map. 360° could be covered in both TX and RX modes. Within the frequency range of 26.5 GHz to 29.5 GHz, the measured RMS phase error is always less than 1.8° and the measured RMS gain error is always less than 0.4 dB.

6.2 Measurement Results

The proposed bi-directional phased-array beamformer chip is fabricated in a standard 65 nm CMOS process. The manufacturing cost is also minimized by using CMOS process when considering massive production. Fig. 6.12 shows the die micrograph of the beamformer. The chip size is 4 mm x 3 mm. Thanks to the area-efficient bi-directional architecture, the proposed beamformer in this work only occupies an active area of 0.58

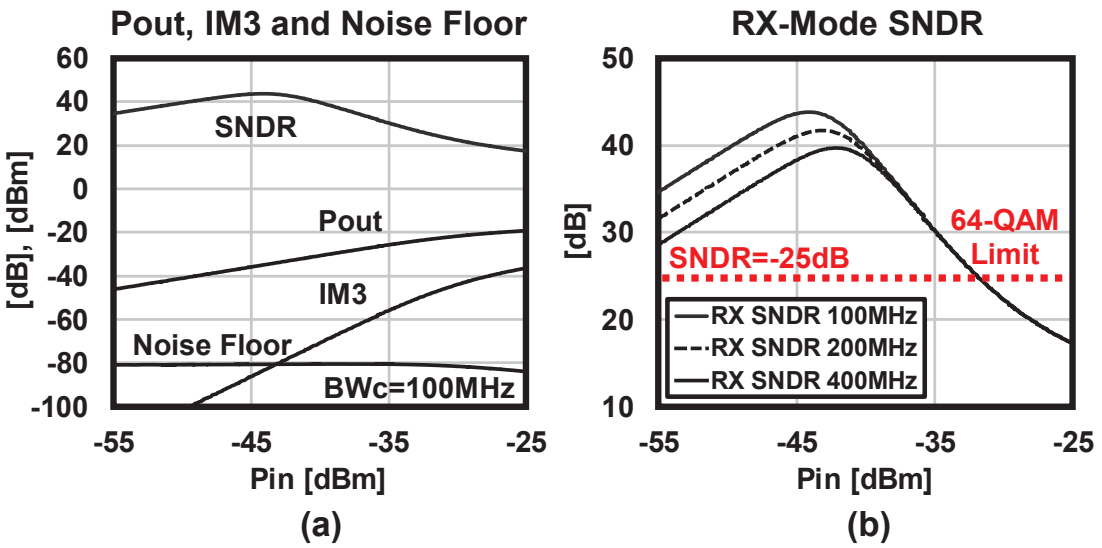


Figure 6.15: Measured (a) output power, IM3, output noise floor and (b) the corresponding SNDRs of the RX-mode beamformer.

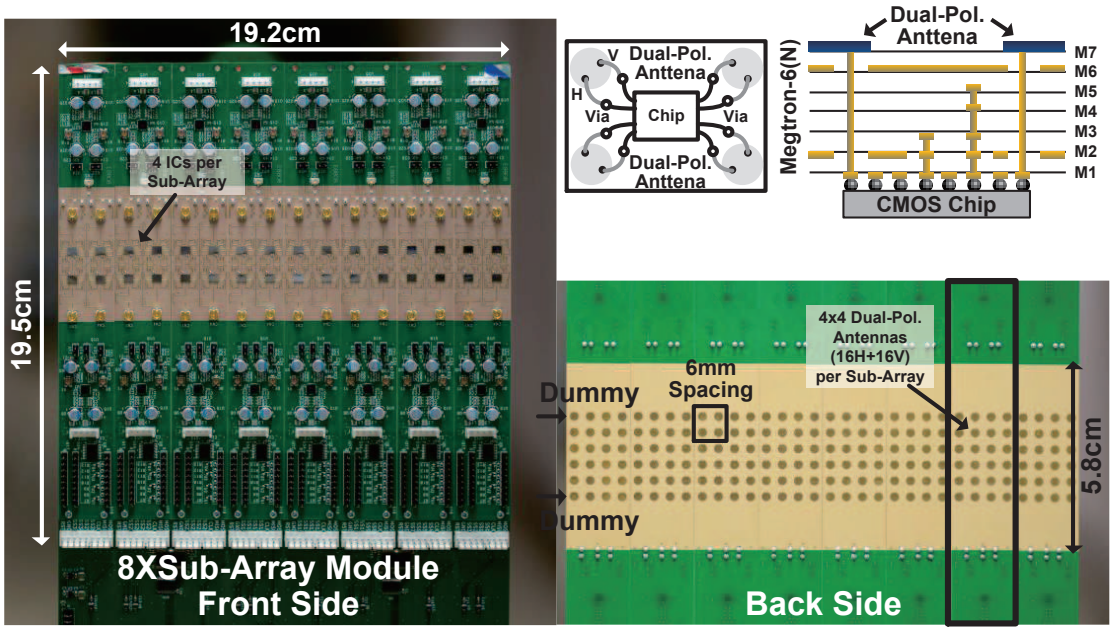


Figure 6.16: Photograph of the transceiver module.

mm^2.

Fig. 6.13 shows the measured on-wafer characteristics for a single-path beamformer. The left hand side summarizes the measured gain characteristics for the beamformer in

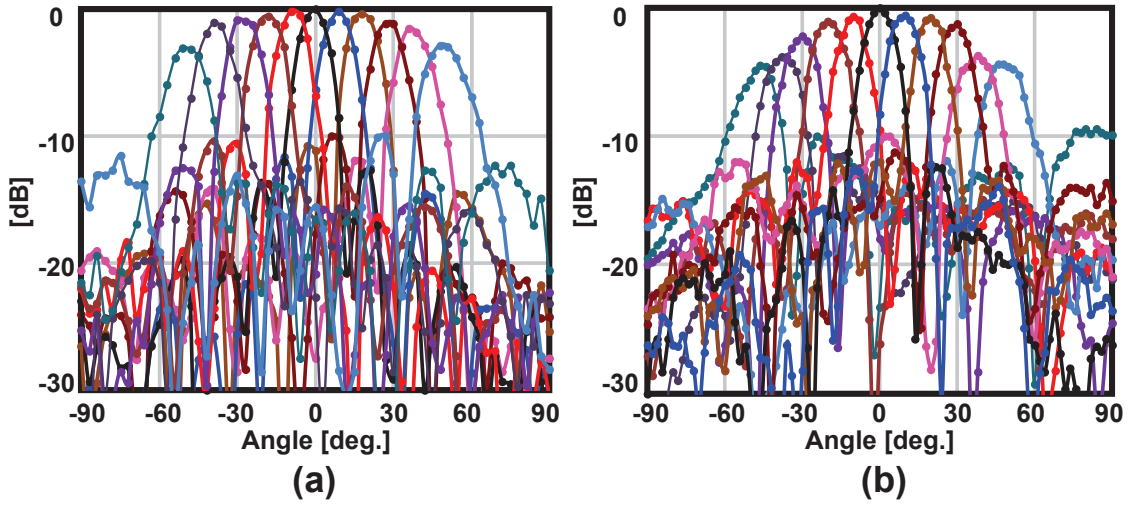


Figure 6.17: Measured beam patterns of two sub-array modules in azimuth plane for (a) V polarization and (b) H polarization.

TX and RX modes. Within the frequency range of 26.5 GHz to 29.5 GHz, the beamformer achieves around 14-dB gain in TX mode and 10-dB gain in RX mode including the insertion loss of the divider/combiner. The right hand side shows the measured linearity for TX mode and NF for RX mode. The achieved Psat and P1dB in TX mode are 15.1 dBm and 11.3 dBm at 28 GHz. Regarding the RX, a NF of 4.2 dB is achieved at 28 GHz. The measured NF is always less than 5 dB from 26.5 GHz to 29.5 GHz.

The proposed TX-mode beamformer in this work is also evaluated with the 5G NR down-link packets. Fig 6.14 (a) summarizes the measured EVM regarding different modulation schemes and different bandwidths. The proposed TX-mode beamformer achieves the 64-QAM (MCS19) and 256-QAM (MCS27) EVMs of -25.1 dB and -32.5 dB at the output power of 5.6 dBm and 0.1 dBm, respectively. The 5G NR standard also set the adjacent channel leakage ratio limitation for the transmitter, which is -28 dB for the 28 GHz band. The measured ACLR performance for the TX mode beamformer regarding different modulation schemes are summarized in Fig 6.14 (b). The bandwidth for this measurement is kept with 400 MHz. From the measurement results, for modulation schemes like 64-QAM and 256-QAM, the maximum output power is mainly decided by the EVM limitation. While for modulation schemes of QPSK or 16-QAM, the maximum output power is limited by the ACLR. In this work, the corresponding ACLRs are -28.9dBc in 64-QAM and -33.6dBc in 256-QAM at the output power of 5.6 dBm and 0.1 dBm, respectively.

The RX-mode output power, IM3 and noise floor are also measured at 28 GHz. The results are shown in Fig 6.15 (a). The RX-mode SNDRs are calculated regarding different

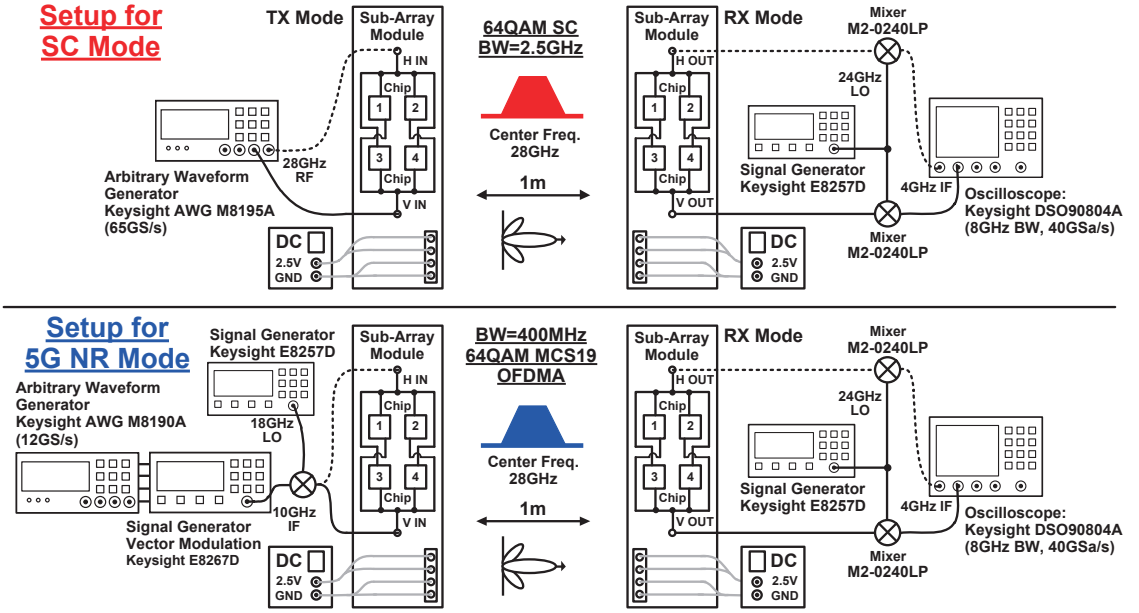


Figure 6.18: Measurement setup for the OTA measurement.

channel bandwidths. The achieved peak SNDRs are 43.8 dB for 100 MHz, 41.8 dB for 200 MHz and 39.7 dB for 400 MHz. Regarding a large RX input, the SNDR can be further improved by decreasing the gain level of the LNA or RF buffer.

To further evaluate the over-the-air performance of the phased-array beamformer, the fabricated chips are implemented into phased-array transceiver module. Fig 6.16 shows the photograph of the proposed module. The left side shows the front side of the transceiver module and the right hand shows the backside. The proposed phased-array transceiver module in this work totally consists of 8 sub-array modules. For each of the sub-array modules, totally 4 of the chips are implemented to the front side in a flip chip manner. In the backside, a 4x4 dual-polarized antenna array is implemented with a 6-mm spacing. Each antenna element has H and V ports for dual-polarized excitation. The H and V ports of each chip are connected to a 2x2 antenna array through the vias. Multiple 4x4 sub-array module modules in this work can be combined side by side to make a larger array such as 32x4.

Fig. 6.17 shows the measured azimuth-plane beam pattern using two sub-array modules. Fig. 6.17 (a) shows the beam pattern for V polarization and Fig. 6.17 (b) shows the pattern for H polarization. The proposed module is capable of scanning the beam from $-50°$ to $+50°$. At $0°$ scan, the measured saturated EIRP for V pol. is 45.6 dBm.

The sub-array modules are also evaluated with the modulated signals. The equipment setup for the OTA measurement is shown in Fig. 6.18. Totally two sub-array modules

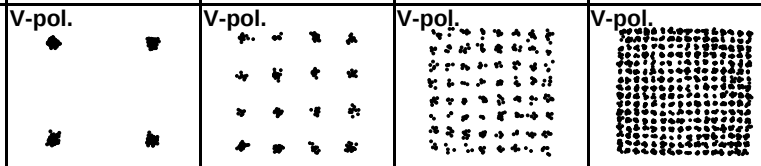
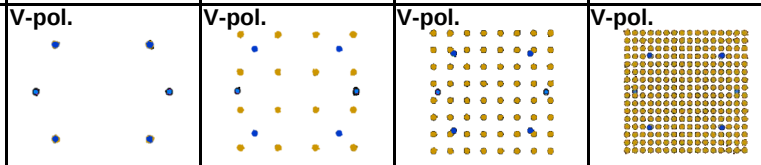
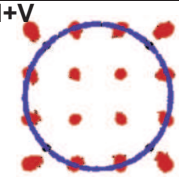
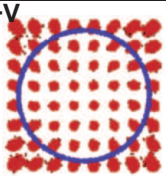
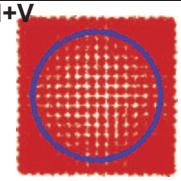
Single-Carrier Mode	Modulation	QPSK	16QAM	64QAM	256QAM
	Symbol rate	3GSymbol/s	3GSymbol/s	2.5GSymbol/s	0.8GSymbol/s
	Data rate	6Gb/s	12Gb/s	15Gb/s	6.4Gb/s
	Constellation				
	TX Output Power	8.0dBm	8.0dBm	7.8dBm	0.6dBm
	TX EVM (RMS)	-25.3dB	-24.2dB	-24.2dB	-29.7dB
	TX-to-RX EVM (RMS)	-22.5dB	-22.1dB	-22.6dB	-29.1dB
OFDMA Mode	Modulation	QPSK	16QAM	64QAM	256QAM
	MCS	5G NR MCS 4	5G NR MCS 10	5G NR MCS19	5G NR MCS27
	BW_c	400MHz	400MHz	400MHz	400MHz
	Constellation				
	TX Output Power	-6.9dBm	-7.0dBm	-7.9dBm	-7.9dBm
	TX EVM (RMS)	-37.5dB (1.3%)	-37.3dB (1.4%)	-37.0dB (1.4%)	-36.8dB (1.4%)
	TX-to-RX EVM (RMS)	-35.1dB (1.8%)	-34.8dB (1.8%)	-34.6dB (1.9%)	-34.4dB (1.9%)

Figure 6.19: Measured SC mode and OFDM mode constellations and EVMs.

are utilized in this measurement. One is operating in TX mode while the other is operating in RX mode. For SC mode measurement, the modulated RF signal for the input side is generated from the arbitrary waveform generator (Keysight AWG M8195A) with a frequency offset of 28 GHz. With a 1-meter communication distance, the transmitted signal is received by the RX-mode sub-array module. The received signal is further down-converted to 4 GHz and evaluated with an oscilloscope (Keysight DSO90804A). Regarding the OFDM mode measurement, the input RF signal is generated by an AWG (Keysight AWG M8190A) along with a signal generator (Keysight E8267D). With a maximum channel bandwidth of 400 MHz, the beamformed signal is transmitted to the RX array. Similar to the SC mode measurement, the down-converted signal is evaluated by the oscilloscope.

Fig. 6.19 shows the measured constellations and EVMs. The upper side shows the SC mode results. The sub-array module in this work achieves maximum raw data rates of 6 Gb/s in QPSK, 12 Gb/s in 16-QAM, 15 Gb/s in 64-QAM and 6.4 Gb/s in 256-QAM. The realized TX EVMs and TX-to-RX EVMs are -25.3 dB and -22.5 dB for QPSK, -24.2

BW=100MHz	Modulation	16QAM	64QAM	256QAM
	MCS	MCS 10	MCS 19	MCS 27
	TX-to-RX Constellation for DP-MIMO *	H+V 	H+V 	H+V 
	TX-to-RX EVM (RMS) for DP-MIMO	-31.4dB (2.7%)	-31.2dB (2.8%)	-31.1dB (2.8%)

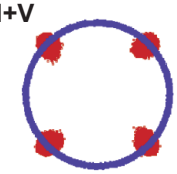
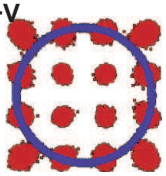
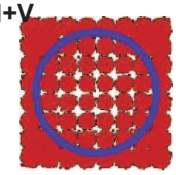
BW=400MHz	Modulation	QPSK	16QAM	64QAM
	MCS	MCS 4	MCS 10	MCS 19
	TX-to-RX Constellation for DP-MIMO *	H+V 	H+V 	H+V 
	TX-to-RX EVM (RMS) for DP-MIMO	-26.7dB (4.6%)	-26.2dB (4.9%)	-26.2dB (4.9%)

Figure 6.20: Measured constellations and EVMs for DP-MIMO communication.

dB and -22.1 dB for 16-QAM, -24.2 dB and -22.6 dB for 64-QAM, -29.7 dB and -29.1 dB for 256-QAM. Regarding the OFDM mode measurement, the results are summarized in the lower side. With 400-MHz channel bandwidth, modulation schemes of QPSK, 16-QAM, 64-QAM and 256-QAM could be supported by this work. the achieved TX EVMs and TX-to-RX EVMs are -37.5 dB and -35.1 dB for QPSK, -37.3 dB and -34.8 dB for 16-QAM, -37.0 dB and -34.6 dB for 64-QAM, -36.8 dB and -34.4 dB for 256-QAM.

A 2X2 DP-MIMO measurement is also carried on in this work. Fig. 6.20 summarizes the results regarding different channel bandwidths. In this measurement, two 5G NR uplink signals are transmitted from the transmitter side to the receiver side simultaneously. The measured constellations are shown for H and V streams together. This work supports a DP-MIMO communication of up to 256-QAM for 100 MHz bandwidth and up to 64-QAM for 400 MHz bandwidth. The achieved TX-to-RX EVMs are -31.4 dB for 16-QAM, -31.2 dB for 64-QAM and -31.1 dB for 256-QAM with 100-MHz channel bandwidth and -26.7 dB for QPSK, 26.2 dB for 16-QAM and 26.2 dB for 64-QAM with 400-MHz channel bandwidth.

6.3 Conclusion

This chapter presents a 28-GHz 4H+4V bi-directional beamformer chip supporting DP-MIMO in 65 nm CMOS. The proposed neutralized bi-directional amplifier significantly reduces the required on-chip area. A bi-directional vector summing phase shifter is also introduced. The measured RMS phase and gain errors are 0.4° and 0.2 dB at 28 GHz, respectively. The array module achieves a saturated EIRP of 45.6 dBm/pol. at 0° scan when 32H+32V array. In a 1-m OTA measurement, a 4x4 sub-array module supports single-carrier data-rates of 15 Gb/s and 6.4 Gb/s per polarization in 64-QAM and 256-QAM, respectively. The measured 400-MHz OFDMA TX-to-RX EVM for the 4x4 sub-array module at 0° scan is -34.4 dB in 256-QAM. 2x2 DP-MIMO communication with a 400-MHz 5G NR channel bandwidth is also achieved with a 64-QAM EVM of 4.9% for the 4x4 sub-array module. Thanks to the proposed bi-directional architecture, the required on-chip area for a single-element beamformer is less than 0.6 mm^2. High-data-rate, reduced manufacturing cost and compact system size could be achieved by this work.

Chapter 7

Conclusion and Future Work

7.1 Conclusion

This thesis presented novelly proposed building block circuits and transceiver architectures for the next generation wireless communication networks. The data rate could be significantly boosted and the required chip area could be reduced to almost half for the next-generation millimeter-wave phased-array transceivers. Facing the design challenges in the millimeter-wave phased-array transceivers, this thesis provide detailed design requirements and systematic design methodology.

Both system-level and circuit-level key technologies are introduced for improving the wireless data rate of the transceivers. An accuracy-improved automatic calibration method is proposed for suppressing the EVM of millimeter-wave direct-conversion transceivers. The calibrated TX LOFT suppression and IMRR are both higher than 45 dB. The TX EVM is improved from -19.5 dB to -28.7 dB before and after the proposed calibration. The corresponding TX-to-RX data rate could be boosted from 3.52 Gb/s to 12.32 Gb/s. 50.1 Gb/s in 64-QAM is achieved by this work in 60-GHz band.

At the same time, for suppressing the manufacturing cost of the millimeter-wave phased-array transceivers with enlarged array size, the bi-directional architecture is introduced in this work. The improved gain characteristics and the optimized reverse isolation realized by the proposed neutralized bi-directional circuitry contributes to a low-noise and high-stability system performance. The proposed transceiver demonstrates 15-Gb/s data rate. A 2×2 DP-MIMO communication is also supported by this work for minimizing the system size. With the proposed technique, the required core area for a single element transceiver is reduced from 1.3 mm^2 to less than 0.65 mm^2.

To summarize, this thesis introduces novel techniques for improving system EVM and minimizing chip area. High-data-rate, low-manufacturing-cost, bi-directional millimeter-

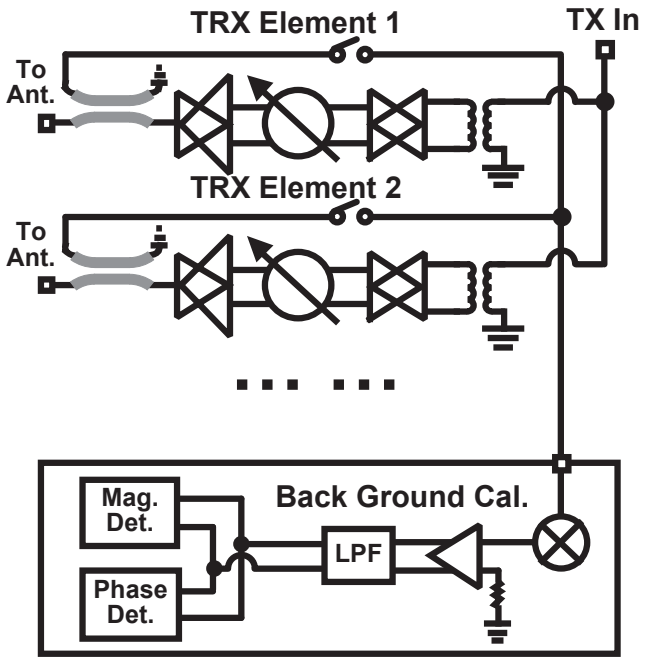


Figure 7.1: Background phase and magnitude calibrations.

wave phased-array transceivers could be realized for both the next-generation WLAN and the next-generation mobile networks.

7.2 Future Work

This thesis presents the potential of the millimeter-wave spectrum for achieving ultra-high wireless throughput. Plentiful frequency resource in millimeter-wave band could be utilized for supporting the next-generation wireless communication. High-data-rate, area-efficient and compact transceiver solutions have been proposed and implemented. Regarding the future extensions of this thesis, the future works and directions in both system-level and circuit-level will be described in this section.

7.2.1 Background Calibration

As mentioned in Chapter 2, long-ranged communication using the millimeter-wave spectrum requires enlarged EIRPs. If without careful control on the gain and phase errors over element-transceivers, the regrowth of sidelobe will generate potential blockers in the space. Although foreground calibration circuits for compensating the errors could be

utilized at the initialization, the errors caused by the temperature over time will still influence the sidelobe performance. Moreover, the required calibration time also tradeoff the low-latency requirements.

To address this issue, background calibration could be introduced for suppressing the errors due to the temperature and reducing the time for initialization. Fig. 7.1 shows the block diagram for explaining the background calibration. By including the calibration switchable paths with 10-dB couplers, the foreground calibration could be moved to background. Because the 10-dB coupler is located at the end of every element-transceiver, enough attentions should be paid for the insertion loss of the coupler. Degradations should be avoided against the output power and the PAE of the PA. At the same time, the coupler characteristics should be co-designed with the SNDR of the calibration network. Margins should be left for maintaining enough detection accuracy. Finally, methods for reducing the calibration time will also be strongly demanded.

7.2.2 Gain-Imbalance Improved Bi-Directional Phase Shifters

Phase shifters are the key component for beamforming. The characteristics of phase shifters will direct influence the gain and phase errors during the beam steering. This thesis introduced a bi-directional active phase shifter for minimizing the area and improving the RF path gain. While, the gain error performance for the proposed phase shifter will be degraded by the unideal switchable PPF. Fig. 7.2 shows the equivalent circuit schematic of the adder-mode switchable PPF. The output voltage swing V_{out} could be derived regarding the input voltages ΔV_{I} and ΔV_{Q}:

$$V_{\text{out}} = -\frac{Z_{\text{L}}(R_{\text{PPF}} - R_{\text{ON}})}{R_{\text{PPF}}R_{\text{ON}} + Z_{\text{L}}R_{\text{PPF}} + Z_{\text{L}}R_{\text{ON}}}\Delta V_{\text{I}} + \frac{Z_{\text{L}}(R_{\text{PPF}} + R_{\text{ON}})}{R_{\text{PPF}}R_{\text{ON}} + Z_{\text{L}}R_{\text{PPF}} + Z_{\text{L}}R_{\text{ON}}}\Delta V_{\text{Q}} \tag{7.1}$$

R_{PPF} in the equation represents the resistance for PPF while R_{ON} is the parasitic resistance of the transistor switches. Ideally, R_{ON} equals to zero and the proposed switchable PPF functions as an ideal adder. However, when R_{ON} not equals to zero, gain imbalance will be induced to the input voltages from I and Q VGAs, which could be expressed with the following equation:

$$\text{GainVar.} = 20\log\frac{R_{\text{PPF}} + R_{\text{ON}}}{R_{\text{PPF}} - R_{\text{ON}}}(\text{dB}) \tag{7.2}$$

As a result, additional compensation for the phase codes between I and Q VGAs is utilized in this work, which is complicated. To address this issue, architectures of bi-directional active phase shifters are required to be introduced for suppressing the gain

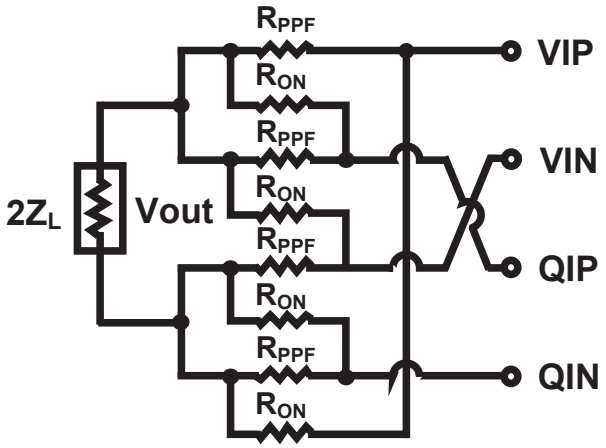


Figure 7.2: Circuit schematic for the adder-mode switchable PPF.

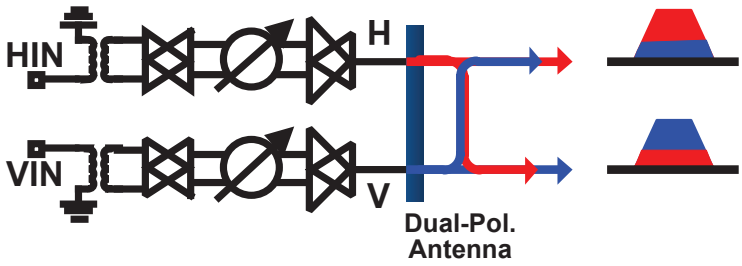


Figure 7.3: Degradation of cross-pol. isolation

imbalance.

7.2.3 Cross-Pol. Isolation Enhancement for DP-MIMO

As mentioned in the Chapter 6, the dual-polarized MIMO could be introduced for an improved data rate and a minimized system size. The cross-pol. isolation between the horizontal-stream and the vertical-stream is utilized for MIMO communication. However, as shown in Fig. 7.3, factors such as PCB implementation, placement of the transmitter and the receiver, and the dual-polarized antenna itself can easily degrade the isolation between the two streams. Enhancement of the cross-pol. isolation regarding any kind of degradation will be strongly demanded.

Cancellation methods at the digital domain could be utilized for compensating the leakage between H and V streams. However, huge power consumption will be introduced to the system. Thus, high-accuracy and low-power analog domain cancellation is more preferable and worth considerations.

7.2.4 Blocker Tolerance

Block tolerance is one of the most important design aspects for the wireless transceivers. Strong in-band blockers will cause desensitization to the receiver front-end and in turn degrades the system SNDR. Even more degradation could be induced due to the unideal LO and the reciprocal-mixing.

Different with the transceivers operating at low frequency, the millimeter-wave transceivers nowadays suffer less from the blockers due to the limited number of millimeter-wave applications. However, regarding the fast growth of the connected wireless devices mentioned in Chapter 1, the blocker tolerance becomes more and more important during the millimeter-wave transceivers design progress, especially for the long-ranged communication with extremely large EIRP. To improve the blocker-tolerance, methods like blocker cancellation and null-steering could be introduced for the millimeter-wave phased-array transceivers.

7.2.5 Process

Compared with the 65nm bulk CMOS process utilized in this work, other process technologies such as compound semiconductors could also be potential candidates for realizing the next-generation millimeter-wave phased-array transceivers. Compound semiconductors such as gallium arsenide (GaAs) are capable of providing higher maximum oscillation frequency and higher power efficiency when compared with bulk CMOS. Low power consumption and high power efficiency design could be achievable with such process technologies. Similarly, CMOS SOI process improves the system performance by isolating the devices from the lossy silicon substrate, which is also a good choice for implementing the system. While for the process mentioned above, additional consideration will be strongly demanded regarding the increased manufacturing costs.

Additionally, advanced technology node in CMOS process could further improve the integration level for a millimeter-wave phased-array system. The system could benefit from implementing the RF front-end along with the digital baseband in the same chip.

Bibliography

[1] [Online]. Available: https://www.cisco.com/c/en/us/solutions/collateral/service-provider/visual-networking-index-vni/white-paper-c11-738429.html.

[2] B. Sadhu, *et al.*, "A 28-GHz 32-Element TRX Phased-Array IC With Concurrent Dual-Polarized Operation and Orthogonal Phase and Gain Control for 5G Communications," *IEEE Journal of Solid-State Circuits*, vol. 52, no. 12, pp. 3373–3391, Dec. 2017.

[3] H. Kim, *et al.*, "A 28GHz CMOS Direct Conversion Transceiver With Packaged Antenna Arrays for 5G Cellular System," *IEEE Journal of Solid-State Circuits*, vol. 53, no. 5, pp. 1245–1259, May 2018.

[4] Y. Yeh, *et al.*, "A 28-GHz Phased-Array Transceiver With Series-Fed Dual-Vector Distributed Beamforming," *IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, pp. 65–68, June 2017.

[5] J. D. Dunworth, *et al.*, "A 28GHz Bulk-CMOS Dual-Polarization Phased-Array Transceiver With 24 Channels for 5G User and Basestation Equipment," *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, pp. 70–72, Feb. 2018.

[6] S. Mondal, *et al.*, "A 25-30 GHz Fully-Connected Hybrid Beamforming Receiver for MIMO Communication," *IEEE Journal of Solid-State Circuits*, vol. 53, no. 5, pp. 1275–1287, May 2018.

[7] M. Huang, *et al.*, "A 23-to-30GHz Hybrid Beamforming MIMO Receiver Array With Closed-Loop Multistage Front-End Beamformers for Full-FoV Dynamic and Autonomous Unknown Signal Tracking and Blocker Rejection," *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, pp. 68–70, Feb. 2018.

[8] K. Kibaroglu, *et al.*, "A Low-Cost Scalable 32-Element 28-GHz Phased Array Transceiver for 5G Communication Links Based on a 2×2Beamformer Flip-Chip

Unit Cell," *IEEE Journal of Solid-State Circuits*, vol. 53, no. 5, pp. 1260–1274, May 2018.

[9] K. Kibaroglu, *et al.*, "A 64-Element 28-GHz Phased-Array Transceiver With 52-dBm EIRP and 8-12-Gb/s 5G Link at 300 Meters Without Any Calibration," *IEEE Transactions on Microwave Theory and Techniques*, vol. 66, no. 12, pp. 5796–5811, Dec. 2018.

[10] N. Saito, *et al.*, "A Fully Integrated 60-GHz CMOS Transceiver Chipset Based on WiGig/IEEE 802.11ad With Built-in Self Calibration for Mobile Usage," *IEEE Journal of Solid-State Circuits*, vol. 48, no. 12, pp. 3146–3159, Dec. 2013.

[11] M. Boers, *et al.*, "A 16TX/16RX 60GHz 802.11ad Chipset With Single Coaxial Interface and Polarization Diversity," *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, pp. 344–345, Feb. 2014.

[12] T. Sowlati, *et al.*, "A 60GHz 144-Element Phased-Array Transceiver With 51dBm Maximum EIRP and ±60° Beam Steering for Backhaul Application," *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, pp. 66–68, Feb. 2018.

[13] K. Okada, *et al.*, "A 64-QAM 60GHz CMOS Transceiver With 4-channel Bonding," *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, pp. 346–347, Feb. 2014.

[14] S. Daneshgar, *et al.*, "A 27.8Gb/s 11.5pJ/b 60GHz Transceiver in 28nm CMOS With Polarization MIMO," *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, pp. 166–168, Feb. 2018.

[15] R. Wu, *et al.*, "A 42Gb/s 60GHz CMOS Transceiver for IEEE 802.11ay," *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, pp. 248–249, Feb. 2016.

[16] T. Mitomo, *et al.*, "A 2-Gb/s Throughput CMOS Transceiver Chipset With In-Package Antenna for 60-GHz Short-Range Wireless Communication," *IEEE Journal of Solid-State Circuits*, vol. 47, no. 12, pp. 3160–3171, Dec. 2012.

[17] S. Saigusa, *et al.*, "A Fully Integrated Single-Chip 60GHz CMOS Transceiver With Scalable Power Consumption for Proximity Wireless Communication," *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, pp. 348–349, Feb. 2014.

[18] J. Lee, *et al.*, "A Low-Power Low-Cost Fully-Integrated 60-GHz Transceiver System With OOK Modulation and On-Board Antenna Assembly," *IEEE Journal of Solid-State Circuits*, vol. 45, no. 2, pp. 264–275, Feb. 2010.

[19] M. Tabesh, *et al.*, "A 65 nm CMOS 4-Element Sub-34 mW/Element 60 GHz Phased-Array Transceiver," *IEEE Journal of Solid-State Circuits*, vol. 46, no. 12, pp. 3018–3032, Dec. 2011.

[20] L. Kong, *et al.*, "A 50mW-TX 65mW-RX 60GHz 4-Element Phased-Array Transceiver with Integrated Antennas in 65nm CMOS," *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, pp. 234–235, Feb. 2013.

[21] S. Emami, *et al.*, "A 60GHz CMOS Phased-Array Transceiver Pair for Multi-Gb/s Wireless Communications," *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, pp. 164–166, Feb. 2011.

[22] A. Siligaris, *et al.*, "A 65-nm CMOS Fully Integrated Transceiver Module for 60-GHz Wireless HD Applications," *IEEE Journal of Solid-State Circuits*, vol. 46, no. 12, pp. 3005–3017, Dec. 2011.

[23] V. Vidojkovic, *et al.*, "A Low-Power Radio Chipset in 40 nm LP CMOS With Beamforming for 60 GHz High-Data-Rate Wireless Communication," *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, pp. 236–237, Feb. 2013.

[24] Y. Wang, *et al.*, "A 100mW 3.0 Gb/s Spectrum Efficient 60 GHz Bi-Phase OOK CMOS Transceiver," *IEEE Symposium on VLSI Circuits*, pp. C298–C299, June 2017.

[25] [Online]. Available: https://www.fcc.gov/document/part-15-rules-unlicensed-operation-57-64-ghz-band.

[26] [Online]. Available: http://www.itrs2.net/itrs-reports.html.

[27] G. Mangraviti, *et al.*, "A 4-Antenna-Path Beamforming Transceiver for 60GHz Multi-Gb/s Communication in 28nm CMOS," *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, pp. 246–247, Jan. 2016.

[28] K. Okada, *et al.*, "A 60-GHz 16QAM/8PSK/QPSK/BPSK Direct-Conversion Transceiver for IEEE802.15.3c," *IEEE Journal of Solid-State Circuits*, vol. 46, no. 12, pp. 2988–3004, Dec. 2011.

[29] K. Okada, *et al.*, "Full Four-Channel 6.3-Gb/s 60-GHz CMOS Transceiver With Low-Power Analog and Digital Baseband Circuitry," *IEEE Journal of Solid-State Circuits*, vol. 48, no. 1, pp. 46–65, Jan. 2013.

[30] J. Pang, *et al.*, "A 128-QAM 60GHz CMOS Transceiver for IEEE802.11ay with Calibration of LO Feedthrough and I/Q Imbalance," *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, pp. 424–425, Feb. 2017.

[31] R. Wu, *et al.*, "64-QAM 60-GHz CMOS Transceivers for IEEE 802.11ad/ay," *IEEE Journal of Solid-State Circuits*, vol. 52, no. 11, pp. 2871–2891, Nov. 2017.

[32] T. Siriburanon, *et al.*, "A Low-Power Low-Noise Mm-Wave Subsampling PLL Using Dual-Step-Mixing ILFD and Tail-Coupling Quadrature Injection-Locked Oscillator for IEEE 802.11ad," *IEEE Journal of Solid-State Circuits*, vol. 51, no. 5, pp. 1246–1260, May 2016.

[33] T. Kanar, *et al.*, "A 2-15-GHz Accurate Built-in-Self-Test System for Wideband Phased Arrays Using Self-Correcting Eight-State I/Q Mixers," *IEEE Journal of Solid-State Circuits*, vol. 64, no. 12, pp. 4250–4261, Dec. 2016.

[34] G. Hueber, *et al.*, "Smart Front-End Signal Processing for Advanced Wireless Receivers," *IEEE Journal of Selected Topics in Signal Processing*, vol. 3, no. 3, pp. 472–487, June 2009.

[35] L. Anttila, *et al.*, "Efficient Mitigation of Frequency-Selective I/Q Imbalance in OFDM Receivers," *IEEE Vehicular Technology Conference*, pp. 1–5, Sep. 2008.

[36] Y. Zhou, *et al.*, "Impact of LPF Mismatch on I/Q Imbalance in Direct Conversion Receivers," *IEEE Transactions on Wireless Communications*, vol. 10, no. 6, pp. 1702–1708, June 2011.

[37] A. Rezola, *et al.*, "Built-in-Self-Calibration for I/Q Imbalance in Wideband Millimeter-Wave Gigabit Transmitters," *IEEE Transactions on Microwave Theory and Techniques*, vol. 65, no. 11, pp. 4758–4769, Nov. 2017.

[38] FCC, "Code of Federal Regulations CFR title 47, part 30 Upper Microwave Flexible Use Service, Section 30.202," 2018.

[39] S. Shakib, *et al.*, "A Wideband 28GHz Power Amplifier Supporting 8x100MHz Carrier Aggregation for 5G in 40nm CMOS," *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, pp. 44–45, Feb. 2017.

[40] Y. Zhang, *et al.*, "A High-Efficiency Linear Power Amplifier for 28GHz Mobile Communications in 40nm CMOS," *IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, pp. 33–36, June 2017.

[41] V. H. C. Chen, *et al.*, "A 69.5mW 20GS/s 6b Time-Interleaved ADC with Embedded Time-to-Digital Calibration in 32nm CMOS SOI," *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, pp. 380–381, Feb. 2014.

[42] M. J. Chiang, *et al.*, "Artificial-Synthesized Edge-Coupled Transmission Lines for Compact CMOS Directional Coupler Designs," *IEEE Transactions on Microwave Theory and Techniques*, vol. 57, no. 12, pp. 3410–3417, Dec. 2009.

[43] R. Svitek, *et al.*, "DC Offsets in Direct-Conversion Receivers: Characterization and Implications," *IEEE Microwave Magazine*, vol. 6, no. 3, pp. 76–86, Sep. 2005.

[44] K. Dufrene, *et al.*, "Digital Adaptive IIP2 Calibration Scheme for CMOS Downconversion Mixers," *IEEE Journal of Solid-State Circuits*, vol. 43, no. 11, pp. 2434–2445, Nov. 2008.

[45] C. P. Lee, *et al.*, "A Highly Linear Direct-Conversion Transmit Mixer Transconductance Stage With Local Oscillation Feedthrough and I/Q Imbalance Cancellation Scheme," *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, pp. 1450–1459, Feb. 2006.

[46] R. G. Carvajal, *et al.*, "The Flipped Voltage Follower: A Useful Cell for Low-Voltage Low-Power Circuit Design," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 52, no. 7, pp. 1276–1291, July 2005.

[47] S. G. Lee, *et al.*, "Current-Reuse Bleeding Mixer," *Electronics Letters*, vol. 36, no. 8, pp. 696–697, Apr. 2000.

[48] K. Dasgupta, *et al.*, "A 60-GHz Transceiver and Baseband With Polarization MIMO in 28-nm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 53, no. 12, pp. 3613–3627, Dec. 2018.

[49] E. Cohen, *et al.*, "A CMOS Bidirectional 32-Element Phased-Array Transceiver at 60 GHz With LTCC Antenna," *IEEE Transactions on Microwave Theory and Techniques*, vol. 61, no. 3, pp. 1359–1375, Mar. 2013.

[50] E. Cohen, *et al.*, "A Bidirectional TX/RX Four Element Phased-Array at 60GHz With RF-IF Conversion Block in 90nm CMOS Process," *IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, pp. 207–210, June 2009.

[51] U. Kodak, *et al.*, "Bi-Directional Flip-Chip 28 GHz Phased-Array Core-Chip in 45nm CMOS SOI for High-Efficiency High-Linearity 5G Systems," *IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, pp. 61–64, June 2017.

[52] J. Pang, *et al.*, "A 28GHz CMOS Phased-Array Beamformer Utilizing Neutralized Bi-Directional Technique Supporting Dual-Polarized MIMO for 5G NR," *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2019.

[53] E. Cohen, *et al.*, "A Bidirectional TX/RX Four-Element Phased Array at 60 GHz With RF-IF Conversion Block in 90-nm CMOS Process," *IEEE Transactions on Microwave Theory and Techniques*, vol. 58, no. 5, pp. 1438–1446, May 2010.

[54] O. Momeni and E. Afshari, "A High Gain 107 GHz Amplifier in 130 nm CMOS," *IEEE Custom Integrated Circuits Conference (CICC)*, pp. 1–4, Sep. 2011.

[55] H. Bameri and O. Momeni, "A High-Gain mm-Wave Amplifier Design: An Analytical Approach to Power Gain Boosting," *IEEE Journal of Solid-State Circuits*, vol. 52, no. 2, pp. 357–370, Feb. 2017.

[56] O. Momeni, "A 260GHz Amplifier With 9.2dB Gain and -3.9dBm Saturated Power in 65nm CMOS," *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, pp. 140–141, Feb. 2013.

[57] J. Pang, *et al.*, "A 50.1-Gb/s 60-GHz CMOS Transceiver for IEEE 802.11ay With Calibration of LO Feedthrough and I/Q Imbalance," *IEEE Journal of Solid-State Circuits*, pp. 1–16, 2019.

[58] W. L. Chan and J. R. Long, "A 58-65 GHz Neutralized CMOS Power Amplifier With PAE Above 10% at 1-V Supply," *IEEE Journal of Solid-State Circuits*, vol. 45, no. 3, pp. 554–564, Mar. 2010.

[59] T. Sowlati, *et al.*, "A 60-GHz 144-Element Phased-Array Transceiver for Backhaul Application," *IEEE Journal of Solid-State Circuits*, vol. 53, no. 12, pp. 3640–3659, Dec. 2018.

[60] M. Giordani, *et al.*, "A Tutorial on Beam Management for 3GPP NR at mmWave Frequencies," *IEEE Communications Surveys Tutorials*, pp. 1–1, 2018.

[61] M. Elkholy, *et al.*, "Low-Loss Highly Linear Integrated Passive Phase Shifters for 5G Front Ends on Bulk CMOS," *IEEE Transactions on Microwave Theory and Techniques*, vol. 66, no. 10, pp. 4563–4575, Oct. 2018.

[62] J. Dunworth, *et al.*, "28GHz Phased Array Transceiver in 28nm Bulk CMOS for 5G Prototype User Equipment and Base Stations," *IEEE/MTT-S International Microwave Symposium*, pp. 1330–1333, June 2018.

[63] C. F. Campbell, *et al.*, "A Compact 5-Bit Phase-Shifter MMIC for K-band Satellite Communication Systems," *IEEE Transactions on Microwave Theory and Techniques*, vol. 48, no. 12, pp. 2652–2656, Dec. 2000.

[64] K. Koh, *et al.*, "0.13-μm CMOS Phase Shifters for X-, Ku-, and K-Band Phased Arrays," *IEEE Journal of Solid-State Circuits*, vol. 42, no. 11, pp. 2535–2546, Nov. 2007.

[65] J. Pang, *et al.*, "A 28GHz CMOS Phased-Array Transceiver Featuring Gain Invariance Based on LO Phase Shifting Architecture With 0.1-Degree Beam-Steering Resolution for 5G New Radio," *IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, pp. 56–59, June 2018.

[66] N. Ebrahimi, *et al.*, "A 71-86-GHz Phased Array Transceiver Using Wideband Injection-Locked Oscillator Phase Shifters," *IEEE Transactions on Microwave Theory and Techniques*, vol. 65, no. 2, pp. 346–361, Feb. 2017.

[67] L. Wu, *et al.*, "A 4-Path 42.8-to-49.5 GHz LO Generation With Automatic Phase Tuning for 60 GHz Phased-Array Receivers," *IEEE Journal of Solid-State Circuits*, vol. 48, no. 10, pp. 2309–2322, Oct. 2013.

[68] G. Shin, *et al.*, "Low Insertion Loss, Compact 4-bit Phase Shifter in 65 nm CMOS for 5G Applications," *IEEE Microwave and Wireless Components Letters*, vol. 26, no. 1, pp. 37–39, Jan. 2016.

[69] M. Tsai, *et al.*, "60GHz Passive and Active RF-Path Phase Shifters in Silicon," *IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, pp. 223–226, June 2009.

[70] C. Hemmi, *et al.*, "Pattern Characteristics of Harmonic and Intermodulation Products in Broadband Active Transmit Arrays," *IEEE Transactions on Antennas and Propagation*, vol. 50, no. 6, pp. 858–865, June 2002.

[71] T. Kaho, *et al.*, "Carrier Power to Intermodulation-Distortion Power-Ratio-Increasing Technique in Active Phased-Array Antenna Systems," *IEEE Transactions on Microwave Theory and Techniques*, vol. 50, no. 12, pp. 2987–2994, Dec. 2002.

[72] 3GPP, "Technical Specification 38.104 (V15.2.0) Base Station (BS) Radio Transmission and Reception," June 2018.

[73] M. Skolnik, "Radar Handbook, Third Edition." McGraw-Hill Professional, 2008.

[74] N. Mazor, *et al.*, "Analysis and Design of An X-Band-to-W-Band CMOS Active Multiplier with Improved Harmonic Rejection," *IEEE Transactions on Microwave Theory and Techniques*, vol. 61, no. 5, pp. 1924–1933, May 2013.

[75] K. Yamamoto, "A 1.8-V Operation 5-GHz-Band CMOS Frequency Doubler Using Current-Reuse Circuit Design Technique," *IEEE Journal of Solid-State Circuits*, vol. 40, no. 6, pp. 1288–1295, June 2005.

[76] J. Kaukovuori, *et al.*, "Analysis and Design of Passive Polyphase Filters," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 55, no. 10, pp. 3023–3037, Nov. 2008.

[77] T. Kuwabara, *et al.*, "A 28 GHz 480 Elements Digital AAS Using GaN HEMT Amplifiers With 68 dBm EIRP for 5G Long-Range Base Station Applications," *IEEE Compound Semiconductor Integrated Circuit Symposium (CSICS)*, pp. 1–4, Oct. 2017.

[78] K. Kunihiro, "Multi-Beam Phased Arrays for 5G Systems," *IEEE Int. Solid-State Circuits Conf. (ISSCC) Forum4: Circuit and System Techniques for mm-Wave Multi-Antenna Systems*, Feb. 2018.

Appendix A

Publication List

A.1 Journal Paper

- **Jian Pang**, Shotaro Maki, Seitarou Kawai, Noriaki Nagashima, Yuuki Seo, Masato Dome, Hisashi Kato, Makihiko Katsuragi, Kento Kimura, Satoshi Kondo, Yuki Terashima, Hanli Liu, Teerachot Siriburanon, Aravind Tharayil Narayanan, Nurul Fajri, Tohru Kaneko, Toru Yoshioka, Bangan Liu, Yun Wang, Rui Wu, Ning Li, Korkut Kaan Tokgoz, Masaya Miyahara, Atsushi Shirane, Kenichi Okada, "A 50.1Gb/s 60-GHz CMOS Transceiver for IEEE 802.11ay with Calibration of LO Feed-Through and I/Q Imbalance," *IEEE Journal of Solid-State Circuits (JSSC)*, Vol. 54, No. 5, pp. 1375-1390, May 2019.

- **Jian Pang**, Rui Wu, Yun Wang, Masato Dome, Hisashi Kato, Hongye Huang, Aravind Tharayil Narayanan, Hanli Liu, Bangan Liu, Takeshi Nakamura, Takuya Fujimura, Masaru Kawabuchi, Ryo Kubozoe, Tsuyoshi Miura, Daiki Matsumoto, Zheng Li, Naoki Oshima, Keiichi Motoi, Shinichi Hori, Kazuaki Kunihiro, Tomoya Kaneko, Atsushi Shirane, Kenichi Okada, "A 28GHz CMOS Phased-Array Transceiver Based on LO Phase Shifting Architecture with Gain Invariant Phase Tuning for 5G New Radio," *IEEE Journal of Solid-State Circuits (JSSC)*, Vol. 54, No. 5, pp. 1228-1242, May 2019.

A.2 International Conferences and Workshops

- **Jian Pang**, Shotaro Maki, Seitarou Kawai, Noriaki Nagashima, Yuuki Seo, Masato Dome, Hisashi Kato, Makihiko Katsuragi, Kento Kimura, Satoshi Kondo, Yuki Terashima, Hanli Liu, Teerachot Siriburanon, Aravind Tharayil Narayanan,

Nurul Fajiri, Tohru Kaneko, Toru Yoshioka, Bangan Liu, Yun Wang, Rui Wu, Ning Li, Korkut Kaan Tokgoz, Masaya Miyahara, Kenichi Okada, Akira Matsuzawa, "A 128-QAM 60GHz Transceiver for IEEE802.11ay with Calibration of LO Feedthrough and I/Q Imbalance," *IEEE International Solid-State Circuits Conference (ISSCC)*, San Francisco, CA, pp.424-425, Feb. 2017.

- **Jian Pang**, Zheng Li, Ryo Kubozoe, Xueting Luo, Rui Wu, Yun Wang, Dongwon You, Ashbir Aviat Fadila, Rattanan Saengchan, Takeshi Nakamura, Joshua Alvin, Daiki Matsumoto, Aravind Tharayil Narayanan, Bangan Liu, Hanli Liu, Zheng Sun, Hongye Huang, Korkut Kaan Tokgoz, Naoki Oshima, Keiichi Motoi, Shinichi Hori, Kazuaki Kunihiro, Tomoya Kaneko, Atsushi Shirane, Kenichi Okada, "A 28GHz CMOS Phased-Array Beamformer Utilizing Neutralized Bi-Directional Technique Supporting Dual-Polarized MIMO for 5G NR," *IEEE International Solid-State Circuits Conference (ISSCC)*, San Francisco, CA, pp.344-345, Feb. 2019.

- **Jian Pang**, Rui Wu, Yun Wang, Masato Dome, Hisashi Kato, Hongye Huang, Aravind Tharayil Narayanan, Hanli Liu, Bangan Liu, Takeshi Nakamura, Takuya Fujimura, Masaru Kawabuchi, Ryo Kubozoe, Tsuyoshi Miura, Daiki Matsumoto, Naoki Oshima, Keiichi Motoi, Shinichi Hori, Kazuaki Kunihiro, Tomoya Kaneko, and Kenichi Okada, "A 28GHz CMOS Phased-Array Transceiver Featuring Gain Invariance Based on LO Phase Shifting Architecture with 0.1-Degree Beam-Steering Resolution for 5G New Radio," *2018 IEEE Radio Frequency Integrated Circuits Symposium, Philadelphia (RFIC)*, Philadelphia, PA, pp.56-59, Jun. 2018.

- **Jian Pang**, Korkut Kaan Tokgoz, Shotaro Maki, Zheng Li, Xueting Luo, Ibrahim Abdo, Seitarou Kawai, Hanli Liu, Bangan Liu, Makihiko Katsuragi, Kento Kimura, Atsushi Shirane, Kenichi Okada, "A 28.16-Gb/s Area-Efficient 60GHz CMOS Bi-Directional Transceiver for IEEE 802.11ay," *IEEE Asian Solid-State Circuits Conference (A-SSCC)*, Tainan, Taiwan, pp.77-78, Nov. 2018.

- **Jian Pang**, Ryo Kubozoe, Zheng Li, Masaru Kawabuchi, Kenichi Okada, "A 28GHz CMOS Phase Shifter Supporting 11.2Gb/s in 256QAM with an RMS Gain Error of 0.13dB for 5G Mobile Network," *IEEE MTT-S European Microwave Conference (EuMC)*, Madrid, Spain, pp.807-810, Sep. 2018.

A.3 Domestic Conferences and Workshops

- **Jian Pang**, Shotaro Maki, Seitarou Kawai, Noriaki Nagashima, Yuuki Seo, Makihiko Katsuragi, Kento Kimura, Satoshi Kondo, Hanli Liu, Teerachot Siriburanon, Tohru Kaneko, Masaya Miyahara, Kenichi Okada, Akira Matsuzawa, "A 128-QAM 60GHz CMOS Transceiver for IEEE802.11ay with Calibration of LO Feedthrough and I/Q Imbalance," *LSI and System Workshop*, Tokyo, May 2017.

- **Jian Pang**, Shotaro Maki, Seitarou Kawai, Noriaki Nagashima, Yuuki Seo, Masato Dome, Hisashi Kato, Makihiko Katsuragi, Kento Kimura, Satoshi Kondo, Yuki Terashima, Hanli Liu, Teerachot Siriburanon, Aravind Tharayil Narayanan, Nurul Fajiri, Tohru Kaneko, Toru Yoshioka, Bangan Liu, Yun Wang, Rui Wu, Ning Li, Korkut Kaan Tokgoz, Masaya Miyahara, Kenichi Okada, Akira Matsuzawa, "A 128-QAM 60GHz Transceiver for IEEE802.11ay with Calibration of LO Feedthrough and I/Q Imbalance," *IEEE SSCS Japan Chapter ISSCC Reporting Meeting*, Osaka, Mar. 2017 (Invited talk).

- **Jian Pang**, Zheng Li, Ryo Kubozoe, Xueting Luo, Rui Wu, Yun Wang, Dongwon You, Ashbir Aviat Fadila, Rattanan Saengchan, Takeshi Nakamura, Joshua Alvin, Daiki Matsumoto, Aravind Tharayil Narayanan, Bangan Liu, Hanli Liu, Zheng Sun, Hongye Huang, Korkut Kaan Tokgoz, Naoki Oshima, Keiichi Motoi, Shinichi Hori, Kazuaki Kunihiro, Tomoya Kaneko, Atsushi Shirane, Kenichi Okada, "A 28GHz CMOS Phased-Array Beamformer Utilizing Neutralized Bi-Directional Technique Supporting Dual-Polarized MIMO for 5G NR," *IEEE SSCS Japan Chapter ISSCC Reporting Meeting*, Osaka, Mar. 2019 (Invited talk).

- **Jian Pang**, Zheng Li, Ryo Kubozoe, Xueting Luo, Rui Wu, Yun Wang, Dongwon You, Ashbir Aviat Fadila, Rattanan Saengchan, Takeshi Nakamura, Joshua Alvin, Daiki Matsumoto, Aravind Tharayil Narayanan, Bangan Liu, Junjun Qiu, Hanli Liu, Zheng Sun, Hongye Huang, Atsushi Shirane, Kenichi Okada, "A 28GHz CMOS Bi-Directional Phased-Array Beamformer for 5G NR Supporting Dual-Polarized MIMO," *Integrated Circuits and Devices Workshop*, Ishigaki Island, Mar. 2019.

- **Jian Pang**, Shotaro Maki, Seitarou Kawai, Noriaki Nagashima, Yuuki Seo, Makihiko Katsuragi, Kento Kimura, Satoshi Kondo, Hanli Liu, Teerachot Siriburanon, Kenichi Okada and Akira Matsuzawa, "A 128-QAM 60GHz CMOS Transceiver for IEEE802.11ay with Calibration of LO Feedthrough and I/Q Imbalance," *Integrated Circuits and Devices Workshop*, Okayama, Mar. 2017.

- **Jian Pang**, Hisashi Kato, Atsushi Shirane, Kenichi Okada, "A High-Resolution LO Phase Shifter with RF Gain-Invariant Phase Tuning for 5G New Radio," *IEICE Society Conference*, Kanazawa, C-12-20, Sep. 2018.

- **Jian Pang**, Masato Dome, Kenichi Okada, Akira Matsuzawa, "An Area-Efficient Low-Loss TRX Switching Technique," *IEICE Society Conference*, Sapporo, C-12-4, Sep. 2016.

A.4 Co-author

A.4.1 Journal Paper

- Rui Wu, Ryo Minami, Yuuki Tsukui, Seitaro Kawai, Yuuki Seo, Shinji Sato, Kento Kimura, Satoshi Kondo, Tomohiro Ueno, Nurul Fajri, Shoutarou Maki, Noriaki Nagashima, Yasuaki Takeuchi, Tatsuya Yamaguchi, Ahmed Musa, Korkut Kaan Tokgoz, Teerachot Siriburanon, Bangan Liu, Yun Wang, **Jian Pang**, Ning Li, Masaya Miyahara, Kenichi Okada, Akira Matsuzawa, "64-QAM 60-GHz CMOS Transceivers for IEEE 802.11ad/ay," *IEEE Journal of Solid-State Circuits (JSSC)*, Vol. 52, pp. 2871-2891, Nov. 2017.

- Yun Wang, Bangan Liu, Rui Wu, Hanli Liu, Aravind Tharayil Narayanan, **Jian Pang**, Ning Li, Toru Yoshioka, Yuki Terashima, Haosheng Zhang, Dexian Tang, Makihiko Katsuragi, Daeyoung Lee, Sungtae Choi, Kenichi Okada, Akira Matsuzawa, "A 60-GHz 3.0 Gb/s Spectrum Efficient BPOOK Transceiver for Low-power Short-range Wireless in 65-nm CMOS," *IEEE Journal of Solid-State Circuits (JSSC)*, 2019.

- Bangan Liu, Yun Wang, **Jian Pang**, Haosheng Zhang, Dongsheng Yang, Aravind Tharayil Narayanan, DaeYoung Lee, SungTae Choi, Rui Wu, Kenichi Okada, and Akira Matsuzawa, "A low-power pulse-shaped duobinary ASK modulator for IEEE 802.11ad compliant 60GHz transmitter in 65nm CMOS," *IEICE Transactions on Electronics*, Vol. E101-C, No. 2, pp.126-134, Feb. 2018.

A.4.2 Conferences

- Korkut Kaan Tokgoz, Shotaro Maki, Seitaro Kawai, Noriaki Nagashima, Jun Emmei, Masato Dome, Hisashi Kato, **Jian Pang**, Yoichi Kawano, Toshihide Suzuki, Taisuke Iwai, Yuuki Seo, Kimsrun Lim, Shinji Sato, Li Ning, Kengo

Nakata, Kenichi Okada, Akira Matsuzawa, "A 56Gb/s W-Band CMOS Wireless Transceiver," *IEEE International Solid-State Circuits Conference (ISSCC)*, San Francisco, CA, pp. 242-243, Feb. 2016.

- Korkut Kaan Tokgoz, Shotaro Maki, **Jian Pang**, Noriaki Nagashima, Ibrahim Abdo, Seitaro Kawai, Takuya Fujimura, Yoichi Kawano, Toshihide Suzuki, Taisuke Iwai, Kenichi Okada, and Akira Matsuzawa, "A 120Gb/s 16QAM CMOS Millimeter-Wave Wireless Transceiver," *IEEE International Solid-State Circuits Conference (ISSCC)*, San Francisco, CA, pp. 168-169, Feb. 2018.

- Hanli Liu, Zheng Sun, Hongye Huang, Wei Deng, Teerachot Siriburanon, **Jian Pang**, Yun Wang, Rui Wu, Toruki Someya, Atsushi Shirane, Kenichi Okada, "A 265μW Fractional-N Digital PLL with Seamless Automatic Switching Subsampling/Sampling Feedback Path and Duty-Cycled Frequency-Locked Loop in 65nm CMOS," *IEEE International Solid-State Circuits Conference (ISSCC)*, San Francisco, CA, Feb. 2019.

- Yun Wang, Bangan Liu, Hanli Liu, Aravind Tharayil Narayanan, **Jian Pang**, Ning Li, Toru Yoshioka, Yuki Terashima, Haosheng Zhang, Dexian Tang, Makihiko Katsuragi, Daeyoung Lee, Sungtae Choi, Rui Wu, Kenichi Okada, and Akira Matsuzawa, "A 100mW 3.0Gb/s spectrum efficient 60GHz bi-phase OOK CMOS transceiver," *IEEE Symposium on VLSI Circuits (VLSI Circuits)*, Kyoto, pp. 298-299, June 2017.

- Bangan Liu, Huy Cu Ngo, Kengo Nakata, Wei Deng, Yuncheng Zhang, Junjun Qiu, Toru Yoshioka, Jun Emmei, Haosheng Zhang, **Jian Pang**, Aravind Tharayil Narayanan, Dongsheng Yang, Hanli Liu, Kenichi Okada, and Akira Matsuzawa, "A 1.2 ps-Jitter Fully-Synthesizable Fully-Calibrated Fractional-N Injection-Locked PLL Using True Arbitrary Nonlinearity Calibration Technique," *IEEE Custom Integrated Circuits Conference (CICC)*, San Diego, CA, Apr. 2018.

- Bangan Liu, Yuncheng Zhang, Junjun Qiu, Wei Deng, Zule Xu, Haosheng Zhang, Jian Pang, Yun Wang, Rui Wu, Teruki Someya, Atsushi Shirane, and Kenichi Okada, "An HDL-described Fully-synthesizable Sub-GHz IoT Transceiver with Ring Oscillator based Frequency Synthesizer and Digital Background EVM Calibration," *IEEE Custom Integrated Circuits Conference (CICC)*, Austin, TX, Apr. 2019.

- Yun Wang, Rui Wu, **Jian Pang**, Dongwon You, Ashbir Aviat Fadila, Rattanan Saengchan, Xi Fu, Daiki Matsumoto, Takeshi Nakamura, Ryo Kubozoe, Masaru

Kawabuchi, Bangan Liu, Haosheng Zhang, Junjun Qiu, Hanli Liu, Naoki Oshima, Keiichi Motoi, Shinichi Hori, Kazuaki Kunihiro, Tomoya Kaneko, Atsushi Shirane and Kenichi Okada, "A 39GHz Phased-Array CMOS Transceiver with Built-in Calibration for Large-Array 5G NR," *IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, Boston, MA, Jun. 2019.

- Rui Wu, **Jian Pang**, Yuuki Seo, Kento Kimura, Seitarou Kawai, Shinji Sato, Satoshi Kondo, Tomohiro Ueno, Nurul Fajri, Yasuaki Takeuchi, Tatsuya Yamaguchi, Ahmed Musa, Masaya Miyahara, Kenichi Okada, Akira Matsuzawa, "An LO-Buffer-Less 60-GHz CMOS Transmitter with Oscillator Pulling Mitigation," *IEEE Asian Solid-State Circuits Conference (A-SSCC)*, Toyama, Japan, pp. 109-112, Nov. 2016.

- Ning Li, Takeshi Inoue, Takuichi Hirano, **Jian Pang**, Rui Wu, Kenichi Okada, Hitoshi Sakane, and Akira Matsuzawa, "Substrate Noise Isolation Improvement by Helium-3 Ion Irradiation Technique in a Triple-well CMOS Process," *IEEE European Solid-State Device Conference (ESSDERC)*, Graz, Austria, Sep. 2015.

- Rui Wu, Ryo Minami, Yuuki Tsukui, Seitaro Kawai, Yuuki Seo, Shinji Sato, Kento Kimura, Satoshi Kondo, Tomohiro Ueno, Nurul Fajri, Shoutarou Maki, Noriaki Nagashima, Yasuaki Takeuchi, Tatsuya Yamaguchi, Ahmed Musa, Korkut Kaan Tokgoz, Teerachot Siriburanon, Bangan Liu, Yun Wang, **Jian Pang**, Ning Li, Masaya Miyahara, Kenichi Okada, Akira Matsuzawa, "Ultra-high-data-rate 60-GHz CMOS transceiver for future radio access network," *IEEE International Conference on ASIC (ASICON)*, Guiyang, China, Oct. 2017.

- Masato Dome, **Jian Pang**, Hisashi Kato, Kenichi Okada, Akira Matsuzawa, "Consideration of Diode Linearizer for 60 GHz CMOS Power Amplifier," *IEICE Society Conference*, C-12-1, Sep. 2016.

- Ryo Kubozoe, **Jian Pang**, Zheng Li, Masaru Kawabuchi, Atsushi Shirane and Kenichi Okada, "A 28GHz gain-invariant vector summing phase shifter in CMOS technology," *IEICE Society Conference*, C-12-19, Sep. 2018.

- Takeshi Nakamura, **Jian Pang**, Atsushi Shirane and Kenichi Okada, "Improvement on Phase Tuning Interference in 28GHz Phased-Array Transmitter," *IEICE Society Conference*, C-12-18, Sep. 2018.