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Article / Book Information

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種別(和文)	論文要旨
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論 文 要 旨

THESIS SUMMARY

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学生氏名： Student's Name	Pang Jian	指導教員（主）： Academic Supervisor(main)	岡田　健一　教授
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要旨（英文 800 語程度）
Thesis Summary（approx.800 English Words ）

The exponential growth of data traffic demands an improved data access speed in the next-generation wireless communication networks. Regarding the limited spectrum resource at the under-10-GHz band, the millimeter-wave spectrum with wide available bandwidth are ready for realizing high-speed data communication. However, designing high-data-rate millimeter-wave transceivers with suppressed power and manufacturing costs is extremely challenging considering the enlarged channel bandwidth and the increased free-space-path-loss. Thus, area-efficient millimeter-wave transceivers with optimized error vector magnitude performance are strongly demanded. This thesis presents high-performance and compact-sized millimeter-wave transceiver solutions to the next-generation local area and mobile communication networks. The proposed calibration technique helps to improve the EVM performance, while the proposed bi-directional architecture minimize the required on-chip area to almost half.

During the past few years, millimeter-wave transceivers implemented in CMOS process have been deeply researched due to the high integration level and the reduced manufacturing cost. The direct-conversion architecture is also attractive due to the minimized number of building blocks. However, the LO feed through and I/Q imbalance in such transceiver architecture will potentially limit the overall EVM. Therefore, this thesis introduces an automatic calibration method for improving the EVM performance of millimeter-wave transceivers. With the proposed compact, low-power and high-accuracy calibration circuits, the calibrated TX LOFT suppression and IMRR are both higher than 45 dB. The TX EVM is improved from -19.5 dB to -28.7 dB before and after the proposed calibration. A maximum single-carrier mode data-rate of 50.1 Gb/s is realized by the calibrated transceiver in 64-QAM. Also, a 128-QAM data rate of 24.64 Gb/s is achieved with a TX-to-RX EVM of -26.1 dB. Compared with the conventional frequency-interleaving architecture and the polarized MIMO solution, the single-element transceiver implementation presented in this thesis benefits from the lower power and manufacturing costs, while maintaining an ultra-high data rate.

To further suppress the chip area considering the MIMO configuration and the beamforming implementation, this thesis also presents a CMOS two-element transceiver chip. Thanks to the bi-directional architecture, The required transceiver die area could be minimized to almost half for a decreased manufacturing cost. The proposed gain-boosted bi-directional amplifier further allows the sharing of interstage passive components. With the help of the designed PA-LNA, the required area for a single-element transceiver in this work is 3 mm^2 including the pads. The maximum raw data rate realized by this work is 28.16 Gb/s in 16-QAM. High-data-rate solution with minimized system size and manufacturing cost is provided for the next-generation WLAN.

Wireless communication capacity improvements for the next-generation mobile communication network is also significant. This thesis introduces a four-element CMOS phased-array transceiver chip. Accurate beam control with improved steering resolution and suppressed EIRP degradation is achieved by the LO phase shifting architecture. The eight-element transceiver module in this work is capable of scanning the beam from -50° to +50°. At a distance of 5 m, the proposed module demonstrates a maximum data rate of 15 Gb/s in 64-QAM. A data link of 6.4 Gb/s in 256-QAM is maintained within a scan angle of -50° to +50°. High-speed and stabilized data communications could be provided within all beam scan angles.

The millimeter-wave phased-array and MIMO systems for mobile communication suffer severely from the enlarged array size. The system size, weight along with the manufacturing cost are significantly increased. Thus, this thesis presents a CMOS 4H+4V bi-directional beamformer chip supporting DP-MIMO. The proposed neutralized bi-directional amplifier significantly reduces the required on-chip area. An active bi-directional vector-summing phase shifter is also introduced for improving the phase shifting resolution and suppressing the

power and area consumptions. In a 1-m OTA measurement, a 4×4 sub-array module supports single-carrier data-rates of 15 Gb/s and 6.4 Gb/s per polarization in 64-QAM and 256-QAM, respectively. 2×2 DP-MIMO communication with a 400-MHz channel bandwidth is also achieved with a 64-QAM EVM of 4.9%. Thanks to the proposed bi-directional architecture, the required on-chip area for a single-element beamformer is less than 0.6 mm^2. Reduced manufacturing cost and compact system size could be maintained with high data rate.

To summarize, this thesis introduces novel techniques for improving system EVM and minimizing chip area. High-data-rate, low-manufacturing-cost, bi-directional millimeter-wave phased-array transceivers could be realized for both the next-generation WLAN and the next-generation mobile networks.