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論 文 要 旨

THESIS SUMMARY

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要旨（英文 800 語程度）
Thesis Summary（approx.800 English Words ）

The scaling of CMOS technology allows faster circuits, small chip areas, and low power consumption for many systems. Some clock generators output signals around to 100GHz. However, not every system requires a high frequency clock as high as the frequencies required in RF circuits. For examples, relatively low frequency clock generators with low phase noise are generally required for analog-to-digital converters (ADCs) and digital-to-analog converters (DACs). Conventional clock generators generally require relatively large area and power consumption to provide low frequency clock with desired phase noise performance in fine CMOS process.

This thesis presents study on a phase-locked loop (PLL) using an injection-locked ring oscillator to provide relatively low frequency clock with small chip area, low power consumption, and good phase noise performance. The proposed PLL is a combinational system of a conventional charge-pump PLL and an injection-locked oscillator and takes advantage of their respective merits. That is, the conventional charge-pump PLL (CPPLL) maintains the stable lock state and an injection-locked oscillator provides good phase noise. This configuration leads two challenges; one is unstable lock state due to the confliction between phase realignments by the PLL and a pulse injection, and the other is to ensure the stable lock of the injection-locked oscillator under PVT (Process-Voltage-Temperature) variations. The first challenge can be solved by separating the CPPLL and the loop of the injection-locked oscillator while sharing the control voltage of the oscillators. The second can be solved by a lock controller and careful design of the oscillators.

The proposed PLL composes of a CPPLL and an injection-locked oscillator identical to the oscillator of the CPPLL, which are controlled by a lock controller. Prior to designing the oscillator, this thesis derives an ideal lock range model for an injection-locked ring oscillator under direct injection method to clarify stable lock state and to provide insight and guideline for designers. The injection-locked oscillator is designed based on the derived lock range and its type is a 3-stage differential ring oscillator which can avoid latch-up or down of an even-stage oscillator due to unexpected external disturbance and then secure stable oscillation. In order to reduce the oscillator gain, the current source of the oscillator is divided into 3-kinds of current sources: an offset frequency providing the lower limit of the output frequency to allow settling time of the coarse tuning to be shortened, current source for coarse tuning controlled by 5 bits, and current source for fine tuning connected to the output of the loop filter. Two identical oscillators share the same

control voltage generated by the CPPLL to have small difference between their oscillation frequencies. The oscillators are designed to have the frequency difference small enough in order to maintain stable lock of the injection-locked oscillator under PVT variations. For verification, various and numerous simulations were performed.

The operation of the proposed PLL has basically three stages which are coarse tuning stage, fine tuning stage, and normal operation stage. At first, the proposed PLL tries to lock the coarse tuning at the coarse tuning stage. As soon as the coarse tuning is locked, the fine tuning stage starts to determine whether the oscillator operates at the desired frequency. After the fine tuning is locked, the injection signal is inputted to the injection-locked oscillator and then the proposed PLL operates at normal operation stage. These operations of the proposed PLL are controlled by the lock controller which is composed of two 7/10-bit counters, a 5-bit up/down counter and detector, a D flip-flop, an initial voltage, and an internal clock generator (CLK). A basic operation of the lock controller is to compare the two input signals to determine which one has higher or lower frequency using 7/10-bit counters and to decide whether the oscillator is locked. And the lock controller controls the operating stages of the proposed PLL using lock alarms, LOCKC and LOCKF. In frequency comparison in the lock controller using counters, the number of bits in the counters are carefully chosen considering meta-stable range, which is a frequency range unable to make a proper decision due to the difference between the delay times of the input signals and is described in detail in this thesis.

The proposed PLL is fabricated in a 90nm CMOS process and occupies an area of 0.242mm^2. The proposed PLL has the high injection ratio of 20 and is tolerable to −5.8% ～ 5.0% variation of the supply voltage, which corresponds to tolerance to temperature variation of 96.4 °C. In-band noises of the proposed PLL at offset frequencies of 10kHz and 100kHz are −108.2dBc/Hz and −114.6dBc/Hz, respectively. The power consumption is 2.8mW.

Moreover, this thesis presents the metastable range detection method to achieve a balance of frequency coverage of the PLL. Also, the compensation technique to voltage and temperature variation in PLLs with hybrid control is introduced to enhance the tolerance to the PVT variations.