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論文 / 著書情報
Article / Book Information

題目(和文)	
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著者(和文)	ZhangHaosheng
Author(English)	Haosheng Zhang
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Category(English)	Doctoral Thesis
種別(和文)	論文要旨
Type(English)	Summary

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（博士課程）
Doctoral Program

論 文 要 旨

THESIS SUMMARY

系・コース： Department of, Graduate major in	電気電子 系 電気電子 コース	申請学位（専攻分野）： Academic Degree Requested	博士 (Philosophy) Doctor of
学生氏名： Student's Name	Zhang Haosheng	指導教員（主）： Academic Supervisor(main)	岡田　健一
		指導教員（副）： Academic Supervisor(sub)	

要旨（英文 800 語程度）
Thesis Summary（approx.800 English Words ）

This dissertation presents one chip-scale ultralow-power atomic clock (ULPAC) in the microwave frequency region. Highly stable frequency standard is essential for high-performance networks such as smart power grids, accurate and robust navigation, self-clocked long-time data logging, scientific metrology, and sensing applications. Widely deployed electro-mechanical oscillators such as the quartz crystal and micro-electromechanical systems resonators suffer from large frequency shifts due to the high sensitivity of the resonance frequency to external or internal factors. The typical long-term stability of such electro-mechanical oscillators is well below the parts-per-billion level (10^{-9}).

For decades, atomic oscillators have been the sole choice in applications requiring ultra-high precision clocks. The superior frequency stability of atomic clocks can be attributed to the fact that the frequency is determined by the transition of energy levels of atoms. However, adopting the conventional atomic clocks for portable and mobile applications, such as the low-earth-orbit small satellite constellations, presents numerous challenges due to the requirements for compact and power-efficient implementation for probing the atomic resonance and preserving the coherence of atoms.

The demonstration of the ULPAC prototype provides one compact, transportable and low-cost frequency standard with atomic grade frequency stability performance, which will enhance or enable various portable and mobile applications. One new suspended compact quantum package architecture along with a fully integrated frequency probing and locking loop implemented in CMOS technology results in a small form-factor package and ultralow-power consumption. Meanwhile, the short-term frequency stability is maintained by low noise circuit design. In addition, dedicated low-noise magnetic field, optimization of the operation condition of the vertical-cavity surface-emitting laser (VCSEL) and temperature control loops are incorporated for isolating and mitigating the internal and external factors affecting the long-term frequency stability. The output frequency of a crystal oscillator is continuously compensated and stabilized by locking to the peak of a coherent population trapping signal, thereby inheriting the superior frequency stability of the atomic clock. The proposed ULPAC system achieves a frequency stability of 2.2×10^{-12} at an averaging time of 10^5 s, while consuming 59.9 mW. The frequency probing and locking circuits implemented in a standard 65-nm CMOS process node occupy an area of 2.55 mm^2. The prototype of this atomic clock occupies a volume of 15 cm^3.

This thesis introduces the implementation details of frequency probing and locking loop together with other control loops. Besides, system-level modeling and analysis are provided for performance optimization and evaluating the atomic clock performance. Chapter 1 gives explains why the atomic clock could demonstrate a superior frequency stability performance as compared with other types of resonators such as electromechanical oscillators. Regarding the implementation complexity and field deployments, the research motivation and perspective of chip-scale ultralow-power atomic clock are introduced with a summary of the state-of-arts of chip-scale atomic clock or chip-scale molecular clock. Chapter 2 of this thesis starts with an introduction to the physical principle of ULPAC. It explains the concept of coherent population trapping (CPT). The superiority of the CPT approach for realizing a compact atomic clock is illustrated with a comparison of electromagnetically induced transparency method. The ULPAC based on the CPT principle could largely reduce the power consumption of laser and remove the volume limit for the atomic cell. Chapter 3 gives the implementation details of ULPAC regarding the quantum physical package, frequency probing and locking loop as well as other control loops like the magnetic, temperature loops. The architecture of the quantum physical package including the VCSEL layout and the detailed circuit design including simulation results are given in this chapter. Chapter 4 includes the evaluations and characterizations of the ULPAC performance. One thorough frequency stability analysis is carried out for diagnosing the short-term noise contributor and major frequency shift. The other performance metrics like power consumption, temperature-dependent variations and mechanical shock tests are also disclosed. Chapter

5 focuses on the low power circuit design techniques for next-generation 20 mW ULPAC. The RF circuits typical dominate the power consumption of one electronic system. One novel power-efficient CMOS oscillator with low phase noise performance is first introduced, which is referred to as pulse-VCO. The pulse-VCO inherits the high power efficiency of the conventional class-C VCO, while removes the design trade-off between the robust start-up and power efficiency of class-C VCO. Then one ultralow-power injection-locked phase-locked loop (PLL) is introduced. Phase noise is dramatically improved by the low-noise RC phase generator and loop-bandwidth optimization. Together with the only 0.2 mW power consumption class-D VCO, the injection-locked PLL achieves a record figure of merit of -271 dB. Chapter 6 introduces promising potential quantum technologies that can be adopted in the future to improve frequency stability performance, like Raman-Ramsey excitation and optical transition. Conclusions are also included in this final chapter.

備考 ： 論文要旨は、和文 2000 字と英文 300 語を 1 部ずつ提出するか、もしくは英文 800 語を 1 部提出してください。
Note : Thesis Summary should be submitted in either a copy of 2000 Japanese Characters and 300 Words (English) or 1copy of 800 Words (English).

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