論文 / 著書情報
Article / Book Information

題目(和文)	SiC MOSFET用の希土類ゲート絶縁膜に関する研究
Title(English)	A Study on Rare Earth Gate Dielectrics for SiC MOSFET
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論 文 要 旨

THESIS SUMMARY

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要旨（英文 800 語程度）
Thesis Summary（approx.800 English Words ）

Silicon carbide (SiC) is a promising candidate for high efficiency power device application. However, SiC metal-oxide-semiconductor field-effect transistor (MOSFET) using thermally grown silicon dioxide (SiO_2) as gate dielectrics suffer from degraded mobility as well as the reliability issues in threshold voltage (V_{th}). Various process technologies have been proposed to recover the degraded mobility so far. However, the negative shift in the V_{th} was enhanced by these processes. Insertion of rare earth oxide gate dielectrics has been reported to achieve both high mobility as well as high V_{th} at the same time. As the basic mechanism is not fully understood, further research on rare earth oxide gate dielectrics for SiC power devices is mandatory.

As the thermally grown interface structure seems to be origin of the degradation in mobility and the negative shift in the V_{th}, complete inhibition of the surface SiC oxidation or different surface SiC oxidizing process might be used to solve the problem. Therefore, in this study, as rare earth materials, yttrium-silicate (Y-silicate) and cerium oxide (CeO_x) dielectrics for SiC metal-oxide-semiconductor (MOS) capacitors and MOS field-effect transistors (MOSFET) have been investigated based on physical and electrical analyses. Coating with Y-silicate is known to protect the SiC surface from oxidation, thus preserving the initial surface after gate stack formation. On the other hand, CeO_x is known to oxidize the surface by means of radical oxygen species, expecting different type of interface structure.

A thermal stability of the Y-silicate interface layer with a thickness of 0.6 nm has been confirmed at 1000^{o}C annealing. A lower interface state density (D_{it}) is lower, and a higher peak mobility of 19 cm^2/Vs with a high V_{th} of 4.2 V has been obtained compared to a deposited-SiO_2 with the same process. Although limited improvements were obtained, initial surface treatment might further enhance the properties.

On the other hand, CeO_x interface layer has showed its thermal stability up to 1100^{o}C process temperature. A high peak mobility of 54 cm^2/Vs with a V_{th} of 2.3 V has been obtained with the CeO_x interface layer, both higher than high-temperature NO-processed MOSFETs. Although there exists hysteresis in the gate voltage swing, the interface formation by means of CeO_x layer might be the key to forming the interface structure.

By stacking the rare earth gate dielectrics, namely CeO_x/Y-silicate or Y-silicate/CeO_x, a slight degraded mobility compared to CeO_x interface layer was obtained. However, the V_{th}

showed a higher value, keeping the role of both gate dielectrics.

In conclusion, the effect of rare earth oxide interface layers for gate dielectric on SiC to the mobility and the V_{th} has been experimentally investigated. Suppression of the surface SiC oxidation by Y-silicate layer leads to the suppression of the negative shift in V_{th} with slight mobility recovery. CeO_x interface layer improves the mobility over 50 cm^2/Vs with suppression of negative V_{th} shift. The obtained results give insights and guideline to the interface formation structure for SiC MOSFET processes.