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Device-Simulation-Based Study of Space Heavy Ions Effects on Semiconductor Material Electronic Devices

by

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≪Device-Simulation-Based Study of Space Heavy Ions Effects on Semiconductor Material Electronic Devices≫

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Chapter 1:

General Introduction

1.1 Semiconductor Material Electronic Devices in spacecraft

Japan aerospace exploration agency (JAXA) has developed and launched so many kinds of spacecraft such as earth observation satellites, Global Positioning System (GPS) satellites, scientific satellite and rockets etc. Such spacecrafts are composed by so many kinds of Electrical, Electronic, and Electromechanical (EEE) parts. According to the example of earth observation space satellite "Daich"[(1-1)], it is said that percentage of EEE parts cost in total developing cost is more than 10 %. It is not too much to say that most important part in development of spacecraft is related to EEE parts. Generally, there are three device types in EEE parts. Passive parts such as resistors, capacitors, inductors and crystal oscillator etc. are included to electrical devices. Active parts such as diodes, transistors, memory devices and micro processing units (MPU) etc. are included to electronic devices. And printed circuit board, mechanical switch, mechanical relays, connectors and cables etc. are included to electromechanical devices. Although these types of parts are also used for the ground applications such as automotive, airplane and medical etc., basically, spacecrafts are also composed by same type parts. One of the big differences between EEE parts for ground and for space is that the EEE parts for space cannot be repaired or replaced in the case of malfunction. Therefore, EEE parts for space are needed to evaluate its quality, reliability, lifetime and failure rate, etc. in advance. In particular, semiconductor electronic devices such as MPU, memory, diode, transistor, etc. are significantly important devices which define spacecraft performance as the central core device. On the other hands, these electronic devices should be taken care specially because it is well known that these electronic devices are strongly influenced by space radiation.

1.2 Space radiation

EEE parts for spacecraft should tolerate a harsh environment comparing with ground environment. For example, EEE parts should function in the harsh thermal environment, in vacuum environment and tolerate mechanical shock and vibration when the launch of spacecraft. In addition, most significant difference between ground and space is harsh radiation environment. Almost space radiation can not reach to ground due to be prevented by double barriers which are earth magnetic field and atmosphere. Fig. 1-1 shows an image of radiations are protected by earth atmosphere[1-2]. Therefore, EEE parts for ground application almost do not need to take care about radiation effects. On the other hands, EEE parts for space applications including electronic devices are exposed strong radiation in orbit. There are mainly three types of space radiations around the earth, Galactic cosmic rays (GCR), Solar cosmic rays (SCR) and charged particles captured by Van-Allen radiation belt. Each types of radiations have various energy and penetrating power and abundance ratio of these radiations are depends on the altitude of space satellites. Detail of regarding to space radiation is explained in chapter 2.

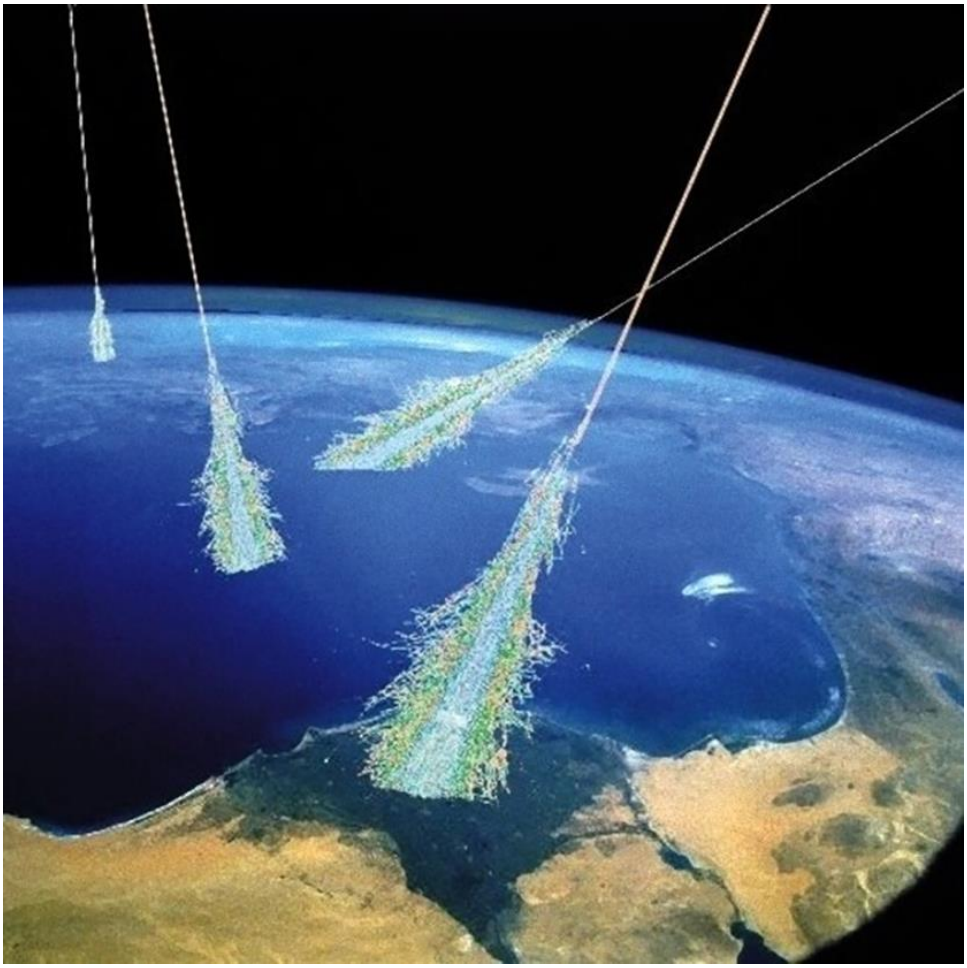

Fig. 1-1. An image of attenuation of space radiations by earth atmosphere [1-2].

1.3 Technology load-map of electronic devices for ground use and for space use

In the case of electronic devices for ground, it is said that the electronic devices evolving depends on the “Moore's law”. This was proposed by Gordon Moore who was co-founder of Intel corporation in over 50 years ago. He said “The number of transistors incorporated in a chip will approximately double every 24 months”. Surprisingly, technology load-map of electronic devices for ground use follows Moore’s law as he had presented at this time, as shown in Fig. 1-2[1-3]. Transistors in electronic devices for ground use

become smaller and higher integration following the Moore's law day by day.

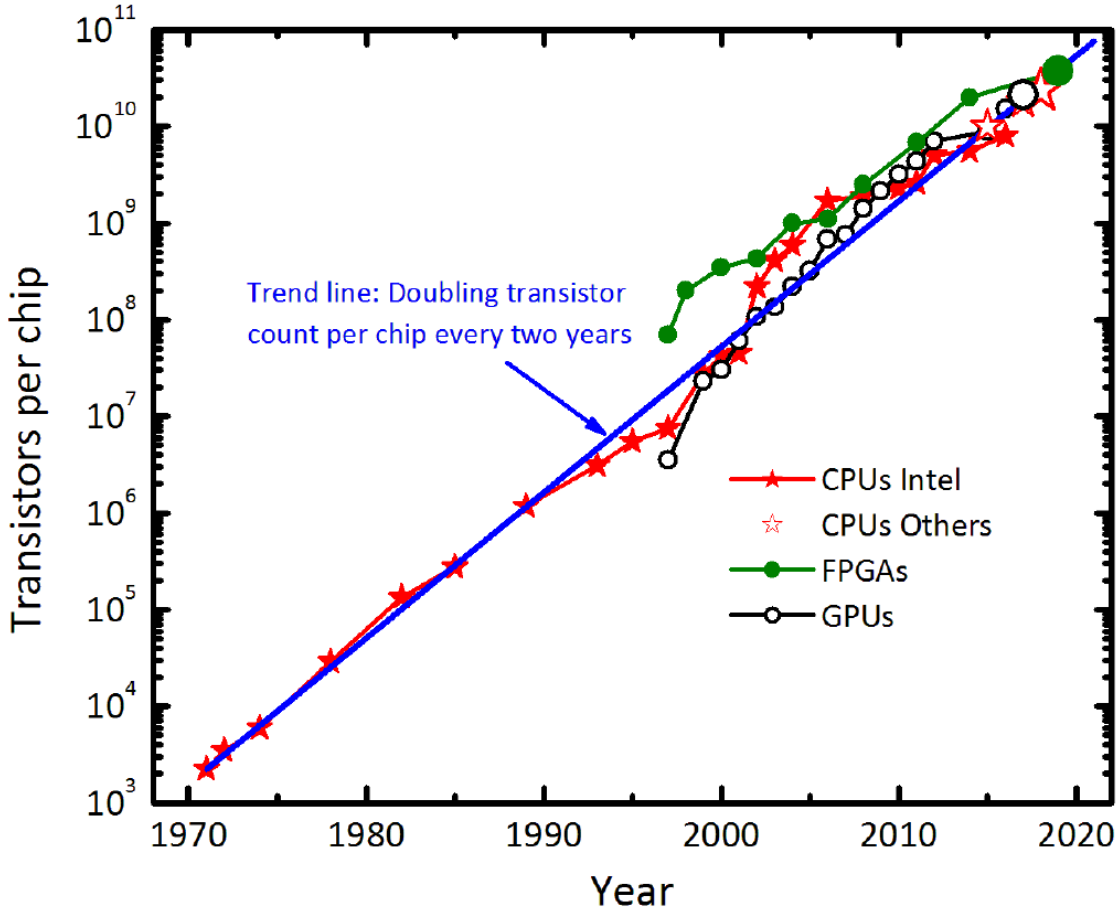

Fig. 1-2. Moore's law: The number of transistors on integrated circuit chips[1-3].

Technology load-map of electronic devices for space use is also following Moore's law, basically. However, it is said that technology load-map of electronic devices for space use is delayed two generations from the technology load-map of electronic devices for ground use. This is because radiation sensitivity is strongly depending on transistor size. Namely, it is indicated that significantly difficult to develop the electronic devices which have a radiation tolerant with cutting edge transistors.

1.4 Differences between the electronic devices for ground use and for space use

Main differences of features between electronic devices for ground use and for space use are listed in Table 1-1.

Table 1-1 Main differences of features between electronic devices for ground use and for space use.

	Electronic devices for space use	Electronic devices for ground use
Operating temperature limits	-55～125℃	0～70℃ (-40～110℃)
Radiation tolerance & vacuum environment	considered	not considered
Mechanical shock & vibration	◎	△
Packages	Metal or ceramic hermetic sealing	Plastic

Because of the satellite temperature in orbit becomes over 100 degrees on dayside and becomes approximately minus 50 degrees on nightside in orbit, electronic devices for space use should have the thermal tolerant to operate in the harsh thermal environment in orbit. In addition, there is not thermal pass to the air because of vacuum environment in orbit. Therefore, thermal design of electronic devices for space use is very severe compare with electronic devices for ground use. Regarding to the mechanical shock and vibration, a part of electronic devices for ground use, e.g. car applications, are considered about the mechanical shock and vibration same as electronic

devices for space use. About the packages of electronic devices, there are big differences between ground use and space use. Generally, the packages of electronic devices for ground use are made by plastic for the purpose of miniaturization and weight saving. In contrast, packages of electronic devices for space use are metal or ceramic package for the purpose of shield of radiations and to add the robustness. In addition, one of the reasons why plastic package cannot be used for electronic devices for space use is outgas issues which is released from organic materials. This outgas have the potential of inducing malfunction in space satellites due to corrosion or degrading sensor performance[(1-4), (1-5)]. A picture of appearance both of memory electronic devices for space use and for ground use are shown in Fig. 1-3. Of course, radiation tolerance and vacuum environment are completely considered on electronic devices for space use. In particular, regarding to the radiation tolerance, electronic devices for space use are taken care by not only using thick packages as mentioned above, but also applied radiation tolerant techniques to the circuits on inner chip itself.

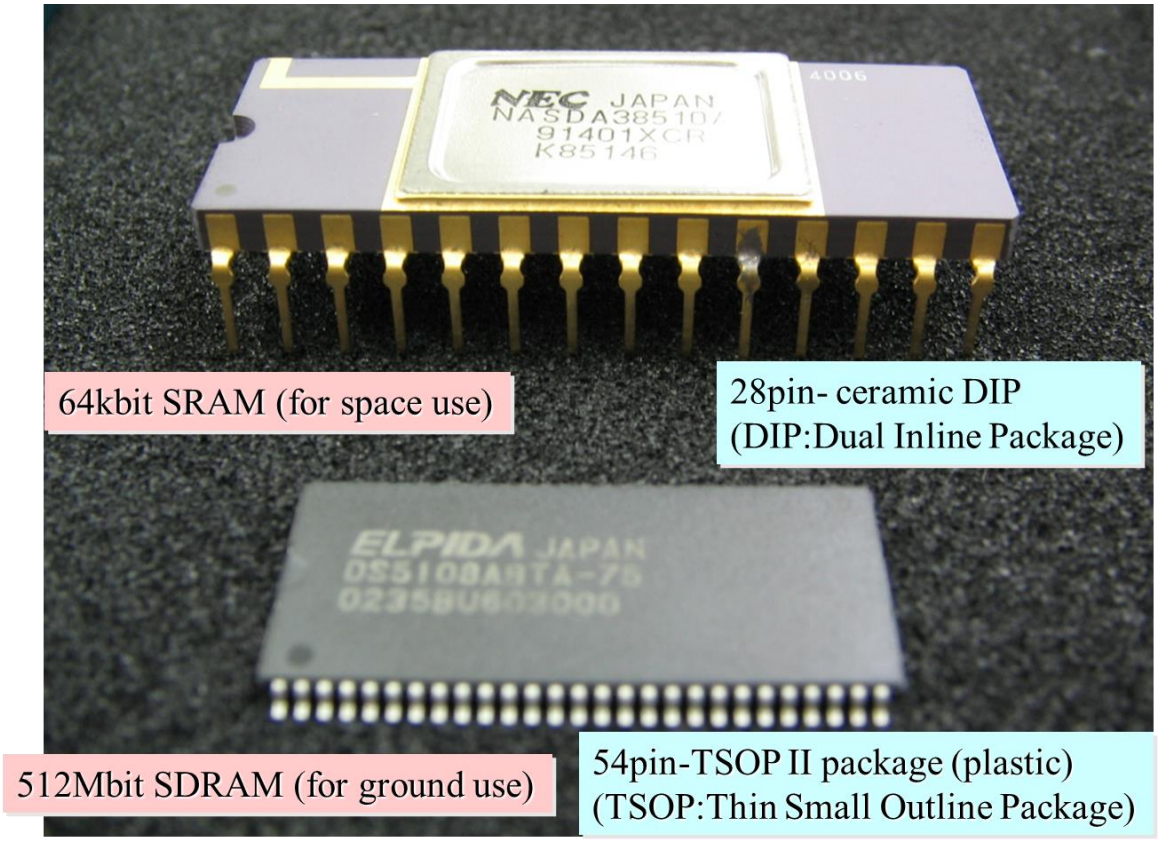

Fig. 1-3. Comparison electronic device packages for ground use with for space use.

1.5 Space satellite malfunctions in orbit

In the long history of space exploration, so many malfunctions of satellites in orbit have been experienced. According to the study of H. C. Koons, et al., it was said that over 80% of malfunctions were related to the space radiation[1-6]. One of the reason of malfunctions due to space radiation is electrostatic discharge. Satellite body, cables or solar cells are gradually taken a charge by huge number of electrons in orbit, and some destructions are occurred due to these charge discharge. This type of malfunction was experienced in Japanese space satellite “ADEOS-2”. Electric power transmission cable from solar cells were damaged by electrostatic discharge, and finally, this satellite was loss of control[1-7]. The other hands, satellite anomalies due to the radiation effect on semiconductor material electronic devices were also serious issues. Table 1-2 shows the satellite anomalies related to solar activity such as solar flare in autumn 2003[1-8]. In worst case scenario, the satellite was total loss due to radiation effect as shown in Table 1-2. In recent years, such catastrophic anomalies due to radiation effect in orbit become rare because radiation tolerant techniques and ground test are developed. Therefore, it is significantly important to establish the radiation tolerant techniques and estimation method of radiation effect for semiconductor material electronic devices.

Table 1-2. Satellite anomalies due to solar activities in autumn 2003[1-8].

Date	Satellite	Event
23 Oct	Genesis	Enters safe mode. Operations resumed on 3 Nov
24 Oct	**Midori**	**Safe mode, power dropped, telemetry lost - total loss**
24 Oct	Stardust	Enters safe mode because of read errors. Recovered
24 Oct	Chandra	Observations halted because of high radiation levels. Restarted 25 Oct
24 Oct	GOES 9, 10	High bit error rates
24 Oct	GOES 12	Magnetic torquers disabled
25 Oct	RHESSI	Spontaneous reset of CPU
26 Oct - 5 Nov	SMART-1	Several auto-shutdowns of electric propulsion
26 Oct	INTEGRAL	One instrument goes into safe mode because of increased radiation
26 Oct	Chandra	Observations halted again autonomously. Later resumed
27 Oct	NOAA 17	AMSU-A1 lost scanner. Possibly power supply failure
27 Oct	GOES 8	X-ray sensor turned itself off. Could not be recovered
28 Oct	SIRTF	Science experiments turned off for 4 days due to high proton fluxes
28 Oct	Chandra	Observations halted autonomously. Resumed on 1 Nov
28 Oct	DMSP F16	SSIES sensor lost data. Recovered
28 Oct	RHESSI	Spontaneous reset of CPU
28 Oct	Mars Odyssey	MARIE instrument has temperature red alarm and is powered off. Not yet recovered
28 Oct	Microwave Anisotropy Probe	Star tracker reset and backup tracker autonomously turned on. Prime tracker recovered
28 Oct	**Kodama**	Temporary safe mode, triggered by increased noise received by Earth sensor. Recovered 7 Nov 2003
29 Oct	AQUA, Landsat, TERRA, TOMS, TRMM	All instruments turned off or safed. Orbital maintenance of TRMM had to be increased
29 Oct	CHIPS	Computer went offline, contact lost for 18 hrs. Spacecraft went tumbling; recovered successfully later. Offline for a total of 27 hrs
29 Oct	X-ray Timing Explorer	Proportional Counter Assembly (PCA) experiences high voltages. All Sky Monitor autonomously shuts off
29 Oct	RHESSI	Spontaneous reset of CPU
29 Oct	Mars Odyssey	Memory error. Corrected with a cold reboot on 31 Oct
30 Oct	DMSP F16	Microwave sounder lost oscillator; switched to redundant system. Primary sounder recovered 4 Nov
30 Oct	X-ray Timing Explorer	Both instruments recovered, but PCA shuts down again. Recovery delayed
28-30 Oct	(Inmarsat)	Two Inmarsat satellites experienced speed increases in momentum wheels requiring firing of thrusters, and one had outage when its CPU tripped out
28-30 Oct	FedSat	Despite triaxial stabilisation, satellite starts wobbling; has Single Event Upset
28-30 Oct	ICESat	GPS resets. Turning on of the UARS/HALOE instrument delayed
28-30 Oct	SOHO	CDS instrument commanded into safe mode for 3 days
28-30 Oct	ACE	Plasma observations lost
28-30 Oct	WIND	Plasma observations lost
28-30 Oct	GOES	Electron sensors saturated
28-30 Oct	MER 1, MER 2	Enter Sun idle mode after excessive star tracker events. Stable, waiting for recovery
28-30 Oct	GALEX	Two ultraviolet experiments turned off because of high voltages caused by excess charge
28-30 Oct	POLAR	Despun platform went out of lock three times. Recovered automatically each time
28-30 Oct	Cluster	Some of the four spacecraft had processor resets. Recovered.
2 Nov	Chandra	Observations halted again autonomously due to radiation
3 Nov	DMSP F16	SSIES sensor lost data. Recovered.
6 Nov	POLAR	TIDE instrument reset itself . High voltage supplies were disabled. Recovered

1.6 Objective of the present work

1.6.1 Objective and motivation of the present work

As introduced on the session 1.5, so many space satellites lost its functions on-orbit due to the radiation effect. Radiation effect is significant serious issue for the semiconductor material electronic devices. The case of satellite function lost in orbit have become rare because people have become well understand to radiation effects for semiconductor material devices. However, due to the recent semiconductor material electronic devices become higher integration and smaller size as following Moore's law, new radiation effects which have never identified are appeared. Among them, it is said that one of the most serious problem for semiconductor material logic circuit is "charge sharing phenomenon". This is because in the case of charge sharing occur in the high integrated circuit, the countermeasures which was said to effective techniques for the radiation in conventional become to be invalidated. The mechanism of charge sharing phenomenon is explained in chapter 3. Therefore, it is significantly important to estimate the effect of charge sharing for designing the radiation tolerant semiconductor material logic circuit in present or future. There are some experimental researches[(1-9), (1-10)] and simulation-based researches[(1-11)-(1-15)] regarding to the charge sharing and charge sharing-induced Multi Cell Upset (MCU), which is the Single Event Upset (SEU) occurrence in more than two memory cells due to single charged ion incidence. In contrast to the most of past studies which use mix-mode simulation, i.e. the combination of device simulation and circuit simulation, the simulation method developed in this study can estimate the charge sharing area by using commonly available device simulator only. The simulation method in this study can be reflected the effect of parasitic

capacitor or resistor in memory circuit has been reflected to the simulation result. In addition, the electric field in whole of memory circuit which related to the total amount of charge collection on the transistor has also been reflected to the simulation result. Also, there are no reports which compare the estimation result of the charge sharing area led from radiation irradiation test of memory circuit with that of device simulation by using the same size transistors. Therefore, this study is intended to provide the quantitative estimation of charge sharing area induced by heavy ion by using the device-simulation-based method established in this work. The charge sharing area on a 65 nm bulk CMOS memory circuit is quantitatively calculated by only using device simulator with proposed device simulation model. Three-dimensional (3D) device simulation model which based on the simple memory circuit with 65 nm process size transistor is prepared. The charge sharing area on actual memory circuit with the same size transistors is also investigated using heavy ion accelerator. Obtained charge sharing areas from both approaches are compared with each other and the validity of device-simulation-based estimation method is confirmed. In addition, charge sharing tolerant memory circuits are suggested based on the results from established simulation method.

The objectives of the present work are classified in the following two items;

1. Establishment of the estimation method for charge sharing phenomenon by using the device simulator.
2. Suggestion of charge sharing tolerant memory logic circuit based on the above simulation method.

1.6.2 Outlines of the thesis content

In Chapter 1 “General Introduction”, the background and objective of this work are indicated. Types of EEE parts for spacecraft are introduced. And differences of characteristics between electronic devices for ground use and for space use are explained. Electronic devices for space use have been also become high integrated following the Moore’s law same as electronic devices for ground use. Space radiation effects has been serious issues in such high integrated electronic devices for space use. Therefore, it is significantly important to establish the estimation method of radiation effects and the radiation tolerant techniques.

Chapter 2 “Radiation Environment in Orbit” introduces the radiation environment in actual orbit which is the electronic devices for space use are exposed. Radiation types which the electronic devices are exposed are different depends on the satellite orbit. Characteristics of radiation environment depending on the satellite orbit are explained in this chapter.

Chapter 3 “Radiation Effects on a Semiconductor Material Devices” indicate the various radiation effects on semiconductor material electronic devices. Detail mechanisms of SEU and charge sharing phenomenon which are this study focused on are explained in Chapter 3.

Chapter 4 “Charge Sharing Induced SEU Simulation by Using the Device Simulator” introduce the device simulation method simulation model for estimation of charge sharing phenomenon and SEU which induced by this phenomenon. Estimation results by using this model and method are also indicated in this chapter.

In Chapter 5 “Experimental Verification of the Device Simulation Model Validity”, validity of the estimation method which introduced in chapter 4 is discussed by comparing the result between devices simulation and charged

heavy ion irradiation test for test memory circuit.

Charge sharing tolerant memory circuit which considered by using the estimation method in this study are proposed in Chapter 6 “Considering of Charge Sharing Tolerant Memory Circuit Based on the device simulation result”.

Chapter 7 “General Conclusion” summarize the results described in chapter 4 through 6 and conclusion of this thesis.

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Chapter 2:

Radiation Environment in Orbit

2.1 Introduction

Electronic devices which are used on ground such as for car applications, medical equipment, industrials and also toys are not considered its radiation tolerant because there is not strong radiation environment under the earth atmospheres. This is because charged particles such as electrons or protons which come to the earth are captured by geomagnetism that is called Van-Allen radiation belt (Fig. 2-1)[2-1]. Other hands, electronic devices for space application must be considered its radiation tolerant. This is because there is too strong radiation environment in space incomparable with on ground radiation environment. In addition, electronic devices which are composed to spacecraft cannot be repaired or replaced after they are launched. Therefore, it is significant important to understand the radiation environment in space correctly to develop or evaluate radiation tolerant devices. A person who develops spacecraft must estimate the probability of radiation malfunctions and the total dose correctly based on the radiation environment which is different for each orbital altitude. In this chapter, the detail of radiation environment in space and its relationship to orbital altitude were indicated.

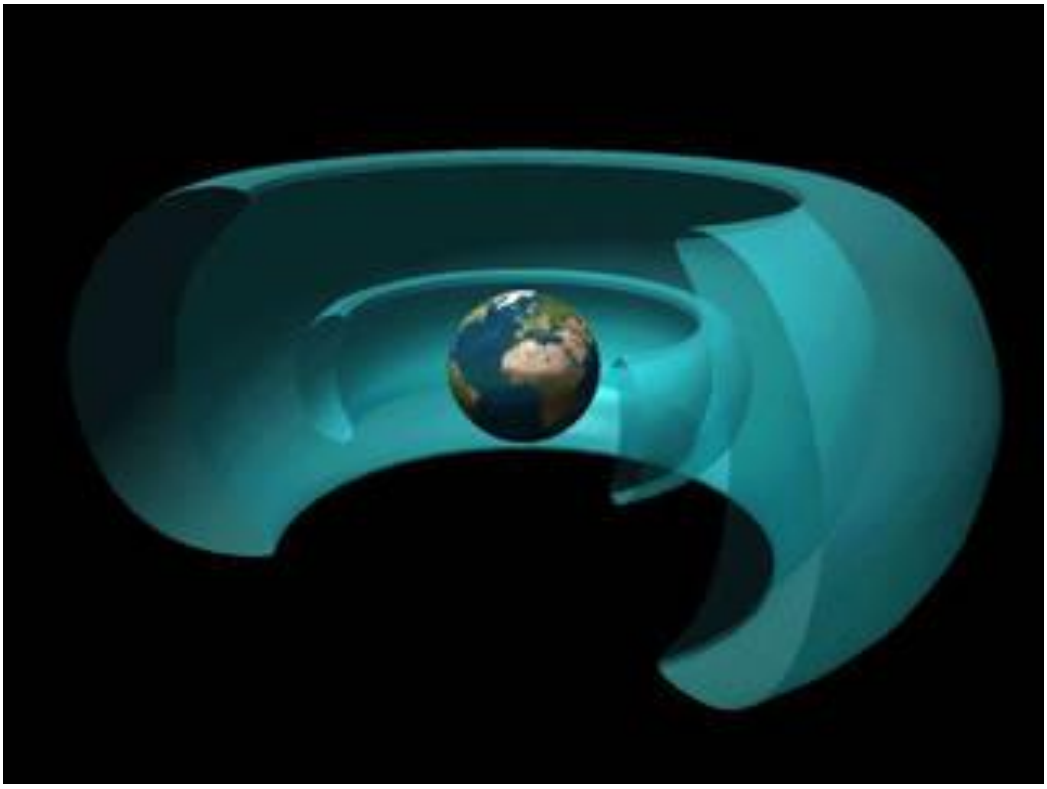

Fig. 2-1. Van-Allen radiation belt[2-1].

2.2 Radiation environment around the earth orbit

As shown in Fig. 2-2, there are three types of radiation around the earth orbit. Galactic cosmic rays (GCR), Solar cosmic rays (SCR) and Van-Allen radiation belt[(2-2)].

It is said that the origin of GCR may be supernova. 98% of GCR is consist of the protons or the heavy ions which heavier than the proton ion, others are consist of electrons or positrons. Element distribution of GCR is indicated in Fig. 2-3[(2-3)]. Almost all of ions in GCR are lighter than Fe ion. And the number of ions which are heavier than Fe less than five digit compare with the number of Fe ions. Element distribution of GCR has a dependence on solar cycle, it increases in the case of solar minimum.

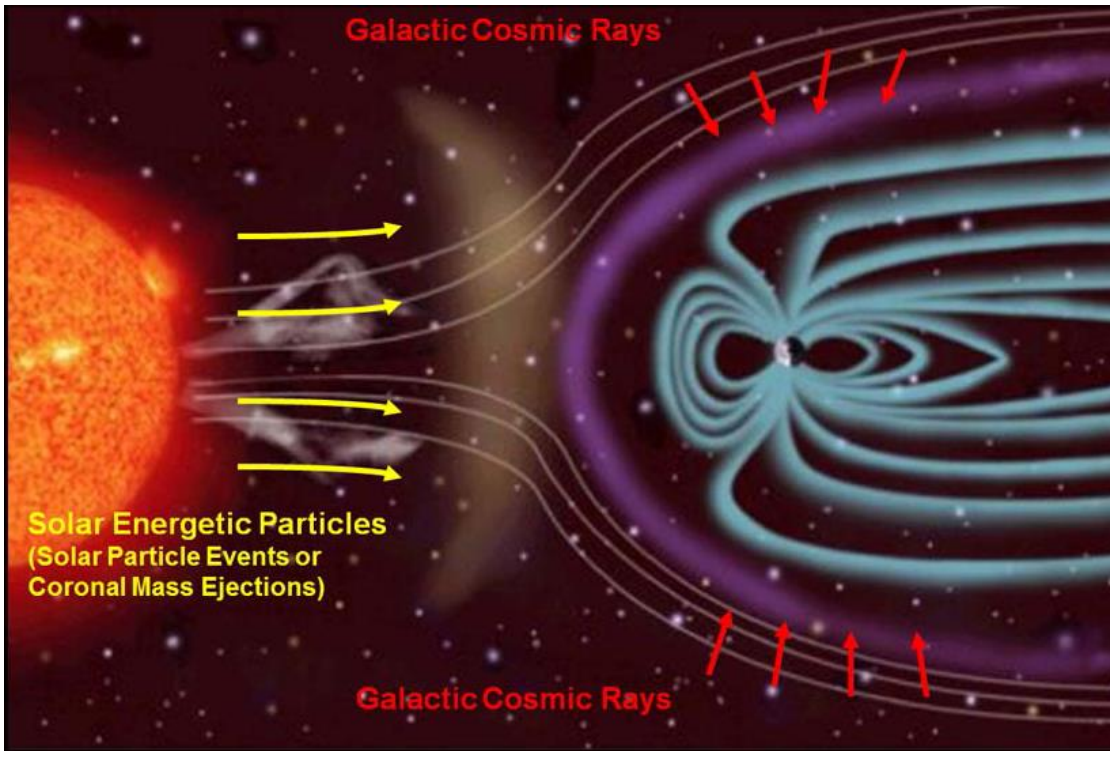

Fig. 2-2. Radiation environment around the earth[(2-2)].

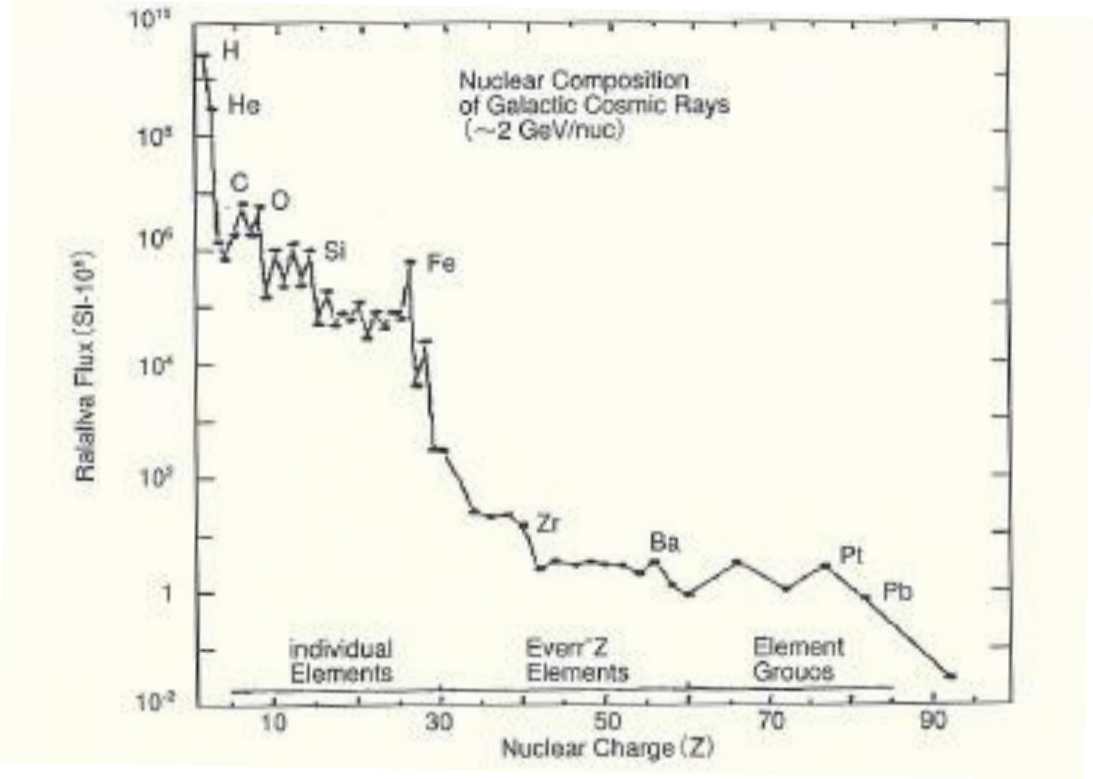

Fig. 2-3. Element distribution of GCR[2-3].

SCR are consist of the high energy charged particles which come from solar flare. 80 to 90% of SCR is high energy protons, and generally, its occurrence cannot be expected in advance. SCR occurrence also has a dependence on solar cycle, the probability of the occurrence increases in the case of solar maximum. One solar cycle is commonly 11 years, so solar maximum and solar minimum frequently repeat by this cycle.

It was identified by Van Allen[2-4], Sekiko Yoda and McIlwein[2-5], [2-6] that there are high energy radiation particles which captured in the geomagnetic in the near earth orbit. It is called Van Allen radiation belt, and the shape is double donuts as shown in Fig. 2-1. Because each layer of Van Allen radiation belt has a polarity, protons are captured in inside layer and electrons are captured in outside layer, mainly. Although low earth orbit spacecrafts such as International Space Station (ISS) (its altitude is less than 600 km) go around more inside than inner belt of Van Allen radiation belt, it needs to take care about the South Atlantic Anomaly (SAA). The area of SAA is indicated in Fig. 2-4 [2-7]. There are much more protons than other area because the edge of inner belt of Van Allen radiation belt get into more low altitude due to tilt of rotation axis of the earth. Actually, so many bit errors were observed in this area on the memory of demonstration component in the small demonstration satellite 1 (SDS-1) which was developed and launched by JAXA. Fig. 2-5 indicates the coordinate of observed error bits, and it shows that the observed error bits are concentrated in SAA and Polar region.

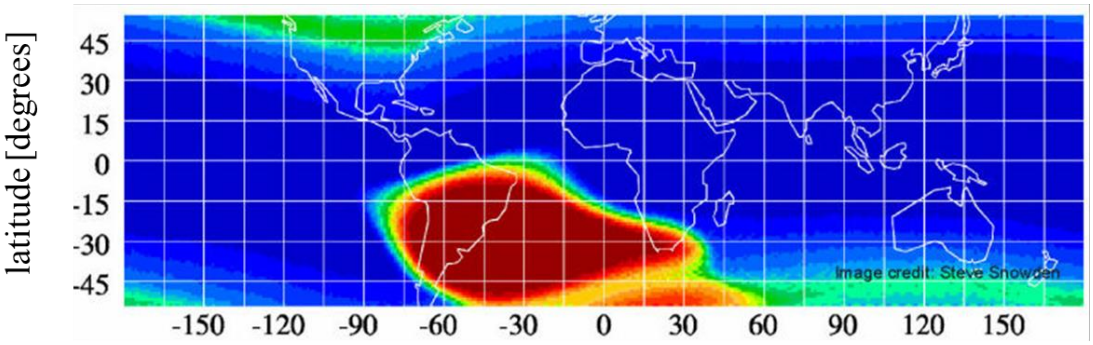

Fig. 2-4. South Atlantic Anomaly (SAA)[2-7].

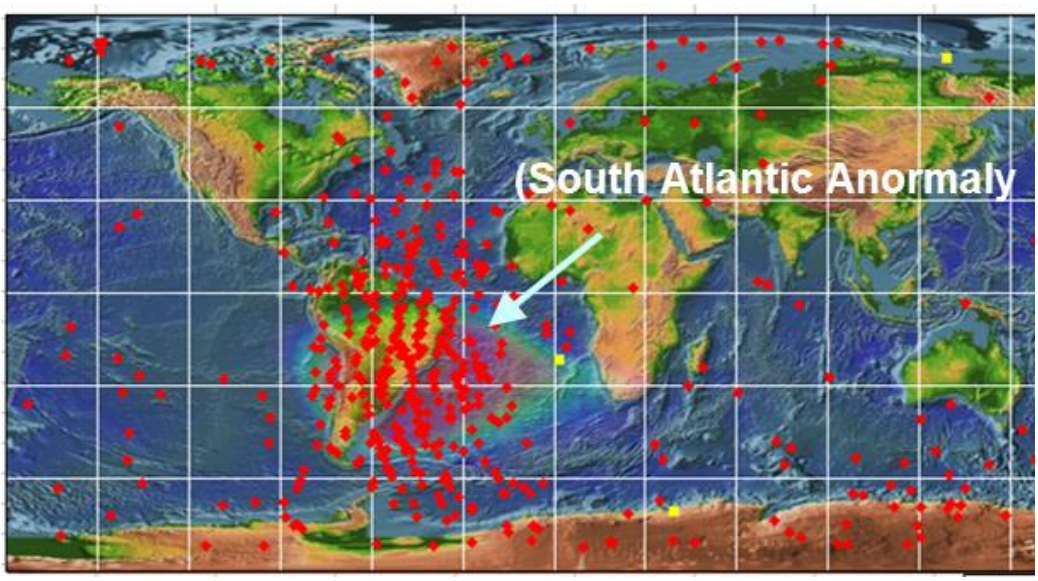

Fig. 2-5. Coordinate of error bit observed on SDS-1 satellite.

2.3 Type of radiation which should be take care on each satellite altitude

As mentioned in the term 2.2, electronic devices which are composed to the space craft should consider the types of radiation on the satellite altitude. Types of satellite orbit are illustrated in Fig.2-6. Satellite orbit which altitude is less than 2,000 km calls low earth orbit (LEO). The earth observation satellites and ISS mainly use this orbit. The orbit which altitude is 35,786 km calls geostationary orbit (GEO). GPS satellites or geostationary meteorological satellites mainly use this orbit. And the orbit between LEO and GEO calls medium earth orbit (MEO). Almost of satellites avoids this orbit due to its strong radiation environment. Geostationary transfer orbit (GTO) is the orbit that is used by satellites to enter GEO. Radiation types which should be considered on each orbit are listed below.

- LEO: Protons captured to inner belt of Van Allen radiation belt.
  LEO satellites which altitude less than 1,000 km should consider the SAA, in particular.
- GEO: Heavy ions form GCR and protons from SCR.
  GEO satellites are exposed so many high energy protons in the case of solar flare occurrence.
- MEO: Depends on its altitude, satellites are exposed protons captured to inner belt or electrons captured to outer belt of Van Allen radiation belt.
- GTO: Satellites are exposed protons and electrons captured to both Van Allen radiation belt during transition.
  After that, the satellites are exposed same radiation condition as GEO.

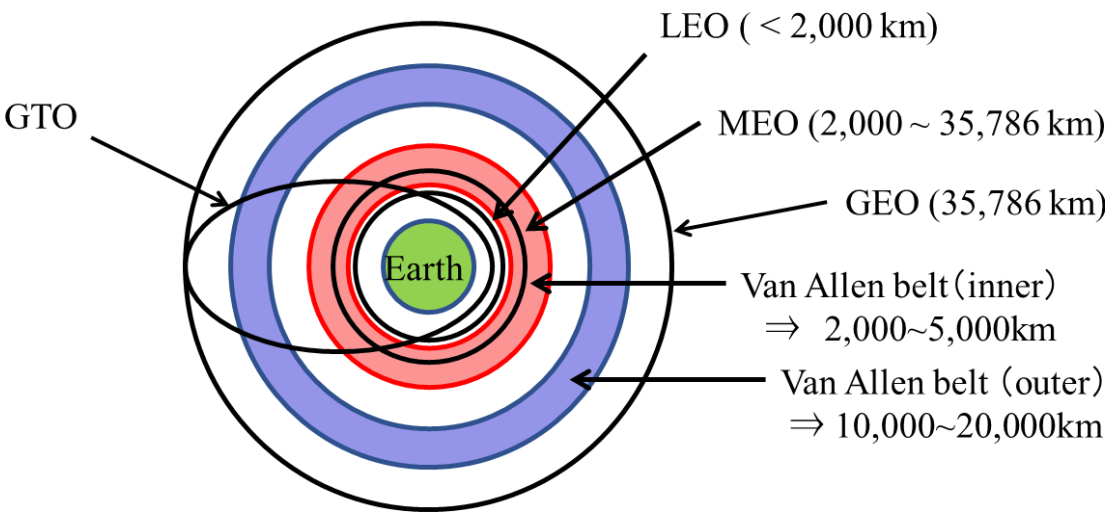

Fig. 2-6. An image of satellite orbit.

2.4 Conclusion

Different to on-ground environment, there is strong radiation environment on orbit around the earth. The radiation environment around the earth and its relationship to the satellite altitude was explained in this chapter. Mainly three types of radiation which have different origin exist around the earth. It is significantly important that electronic devices which are applied to the space satellites should be evaluated its radiation tolerance considering to the radiation environment (kinds of ion particles and its energy) depends on the satellite altitude. In addition, based on considering the satellite mission lifetime, the electronic device robustness which need for succeed the target mission can be expected in advance.

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Chapter 3:

Radiation Effects on Semiconductor Material Electronic Devices

3.1 Introduction

So many kinds of electronic devices are composed to the components on spacecraft such as resistors, capacitors, fuses and inductors. In particular, semiconductor devices are most important parts among them. Semiconductor devices which are represented to micro-processing unit (MPU), application specific integrated circuit (ASIC) and field-programmable gate array (FPGA) have a role of brain of the spacecraft. However, such semiconductor devices are influenced most serious impact due to radiation incident. There are many types of radiation effects which depends on the device types such as the soft-error or the destructive mode in worst case. According to the study of H. C. Koons, et al., distribution of the causes of satellites' anomalies at the age of 1999 are indicated in Fig. 3-1[3-1]. At that time, percentages of anomalies due to radiation effects on semiconductor electronic devices were accounted for over 30% (Single Event Upsets (SEUs) and radiation damage in Fig. 3-1) of all satellites' anomalies. Because of such serious issues for the electronic parts, several types of radiation tolerant techniques had been studied continuously. The influences of radiation and its mechanisms on semiconductor material devices and the radiation tolerant techniques which were studied in the past are explained in this chapter.

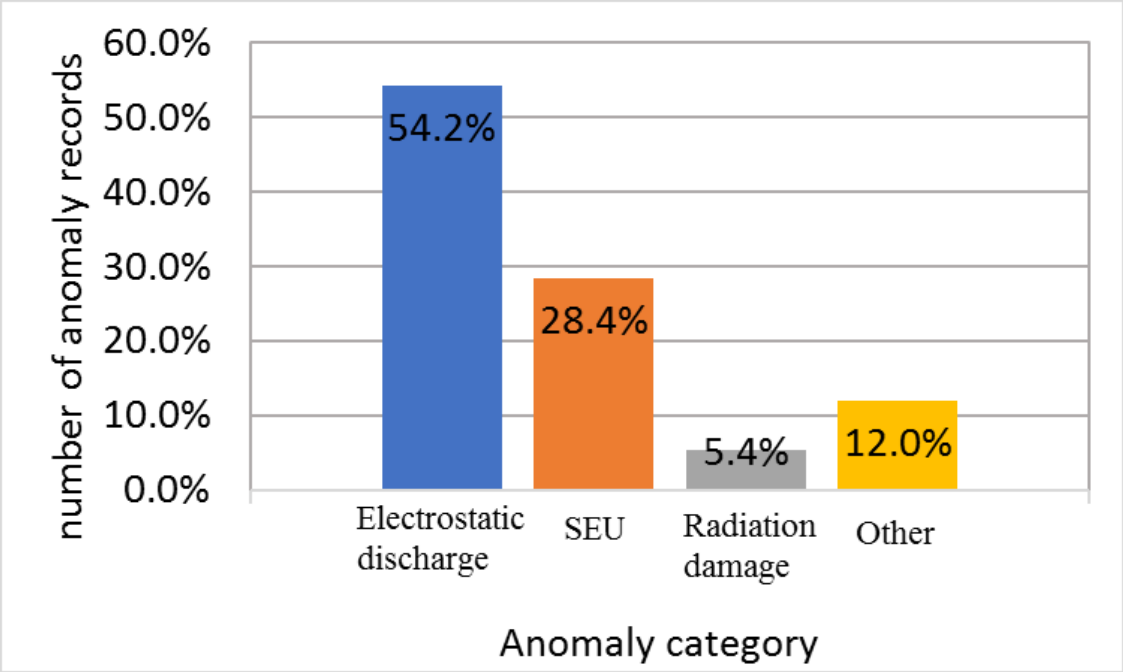

Fig. 3-1. Distributions of the causes of satellites' anomalies on 1999[3-1].

3.2 Radiation effects on the semiconductor material electronic devices

Generally, it is said that radiation effects on the semiconductor material devices are categorized into two types of fundamental damages. One is the lattice displacement damage, and the other is the ionizing effect. The detail mechanism of these radiation effects are explained in this section.

3.2.1 Lattice displacement damage in the semiconductor electronic devices

Electronic devices or optical devices such as CCD, light emitting diode, photo coupler etc., are exposed many kinds of radiation particles in orbit. When these particles penetrate inside of semiconductor device, the phenomena of ionization or of flick off the atom are occurred. As a result, the semiconductor devices are damaged temporarily or permanently. Most of kinetic energy of incident particle is used to ionizing the material and caused to various ionizing effects (which is explained in next session). On the other hands, remaining energy is used to flick off atoms from crystal lattice and then permanent lattice defects are created. This phenomenon is called lattice displacement damage which is one of the reasons for performance degradation of electronic devices. Lattice displacement damage in the semiconductor devices in orbit is mainly caused by proton ions which exist in large amounts in the space radiation environment. In recent years, the demands for using in orbit the CCDs or light emitting diodes which are sensitive to the performance degradations due to lattice displacement damage are increasing day by day. Therefore, this is one of important phenomena which should be understood its impact for the space use devices.

As explained above, most of kinetic energy of the charged particle which

penetrate to the inside of semiconductor devices is used to ionizing the material. However, less than 0.1% energy is used to flick off the atom from crystal lattice and to create lattice defect. Incident charged particle collision to the semiconductor atomic nucleus and generate the primary knock-on atom (PKA). In the case of PKA received enough energy, PKA continue to collide and to flick off the other atom until PKA energy is under the energy to trigger of displacement. In many cases, vacancy-interstitial pair don't become the stable defect due to recombination. However, a part of the vacancy which don't recombine moves between the crystal lattice, and forms the stable defect with dopant of impurity atom as shown in fig. 3-2. Many kinds of degradation effects are led to various devices due to forming the defect level. Degradation effects are different due to the kinds of device, and the sensitivity to the lattice displacement damage is also different depends on the kinds of devices. Lattice displacement damage effects on the various devices are shown in table 3-1.

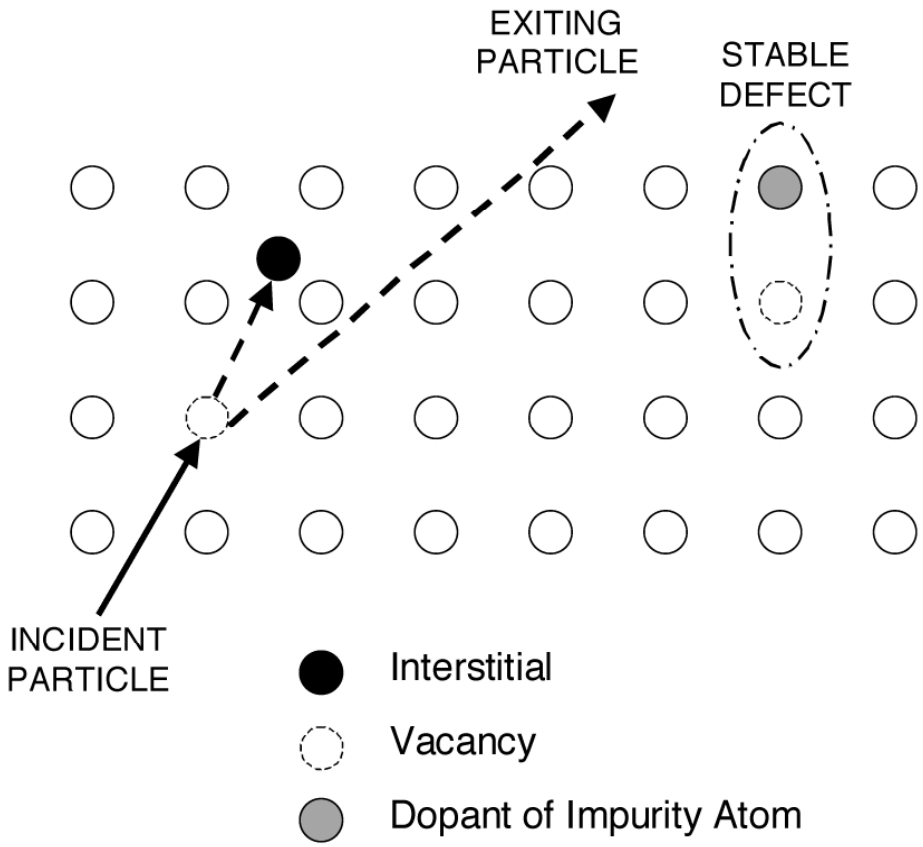

Fig. 3-2. A mechanism of lattice displacement damage generation[3-2].

Table. 3-1 Lattice displacement damage effects on the various devices

Category	Device	Lattice displacement damage effect	Sensitivity
Sensor Light-receiving element	CCD	・Degrade of Charge Transfer Efficiency（CTE） ・Increase of dark current ・Increase the number of hot pixel ・Increase of bright column ・Random Telegraph Noise	・Sensitive
	・Photo diode ・Photo transistor	・Decrease of light-current ・Increase of dark current ・Degrade of response speed ・Decrease of current gain(h_{FE}) on the photo transistor	・Sensitivity depends on the usage ・MSM photo diode is not sensitive ・Photo transistor is sensitive
Light emitting element	・LED ・Laser diode	・Decrease of light output ・Increase of current threshold (laser diode)	・Low sensitivity
Photo coupler	・Photo coupler	・Degrade of Current Transfer Ratio (CTR)	・Sensitivity depends on the usage ・Photo coupler with photo diode have most tolerant ・Photo coupler with photo transistor is a little sensitive than above one
Bipolar	・Bipolar transistor ・Liner IC	・Decrease of current gain(h_{FE})	・Sensitive on the low current condition

3.2.2 Ionizing effects in the semiconductor electronic devices

As described above, the major action of charged particles' incident to semiconductor materials is electron-hole pair generation (ionization). Amount of ionization depends on the charged particle energy and on the absorbed energy to the material (absorbed dose). Generally, the energy which is gave from charged particles to material is represented to Linear Energy Transfer (LET). LET means the amount of the kinetic energy loss per unit length, so the unit of LET is MeV/(mg/cm^2). Mainly, there are two types of phenomena in the ionizing effects. One is the "Total Ionizing Dose effect (TID)" which is the phenomenon of electronic device performance degradation depending on the amount of radiation dose. The other is the "Single Event Effect (SEE)" which is the phenomenon leading to the device hard error or soft error. This phenomenon is not related to the total amount of radiation dose but related to the position of charged particle incidence.

3.2.2.1 Total ionizing dose effect

In the case of radiation induced ionizing in the semiconductor, vacancy recombine to the free electron immediately in usual. However, in the isolator such as SiO_2 in MOSFET device, vacancy don't recombine easily because there are almost not free electrons. In addition, electrons and vacancy (holes) are led to electric field and move to opposite direction each other due to the reverse polarity. Electrons move to gate electrode with few picoseconds due to its high mobility[(3-3), (3-4)]. Meanwhile, holes move to the interface of isolator slowly. Although some holes are vanished due to recombine with electron during to move, other holes reach to interface of isolator and are captured by isolator interface defect. As a result, holes form "captured

positive charge" and it degrade device original performance, gradually. TID leads to degrade regarding to power consumption and operation speed of electronic devices, mainly. Since degradation level due to TID depends on the total amount of dose, this can be prevented by some kinds of shields such as thick metal package.

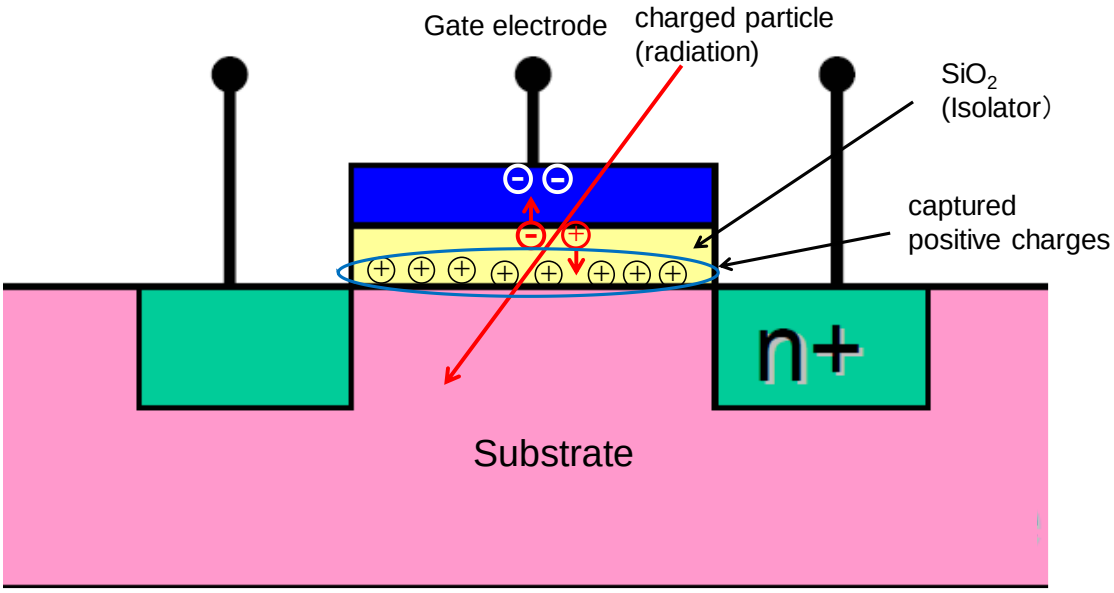

Fig. 3-3. A mechanism of Total Ionizing dose effect in MOSFET.

3.2.2.2 Single event effects

Single event effects (SEE) are induced by the ionization due to one charged particle incident. There are many kinds of failure or error due to SEE which is different to each device. This phenomenon strongly depends on the position of charged particle incident into semiconductor devices. For example, in the case of charged particle incident between materials which have high electric field, increase of leak current or burning out of the electronic devices is occurred due to current pass generated by radiation induced ionization in worst case. In the case of logic circuit, if the charged particle incident to the p-n junction of transistor or neighborhood, generated charge is collected immediately, and it induces error output. This gathering process is mainly separated to drift mechanism due to the electronic field and to diffusion mechanism due to the carrier density gradients in semiconductor material. Total amount of charge which is collected to the transistor is specified approximately by the combination of initial generated charge due to charged particle incident, charge mobility defined from drift-diffusion and recombination speed. There are many types and mechanisms of SEE which depends on the kinds of electronic devices. Because the effective countermeasure is different per types of SEE, it is significantly important to understand the mechanism of SEE. Although new types of SEE have been identified on the latest electronic devices due to their complexity, the major of SEE and device types affected by SEE are listed below.

Table. 3-2 Major types of SEE and device types affected by SEE

SEE	Impacted device types
Single Event Upset (SEU)	Memory, Microprocessor, AD/DA converter
Single Event Transient (SET)	Analog IC, Logic circuit, AD/DA converter, High speed photo-coupler, Microprocessor, High speed access memory etc.
Single Event Latch-up (SEL)	Circuit based on CMOS process
Single Event Burn-out (SEB)	Power MOSFET, NPN bipolar transistor
Single Event Gate rupture (SEGR)	Power MOSFET

(1) Single Event Upset (SEU)

SEU is the phenomenon which induces the soft error in memory, microprocessor and AD/DA convertor etc. The mechanism of SEU is very simple as shown in Fig. 3-4.

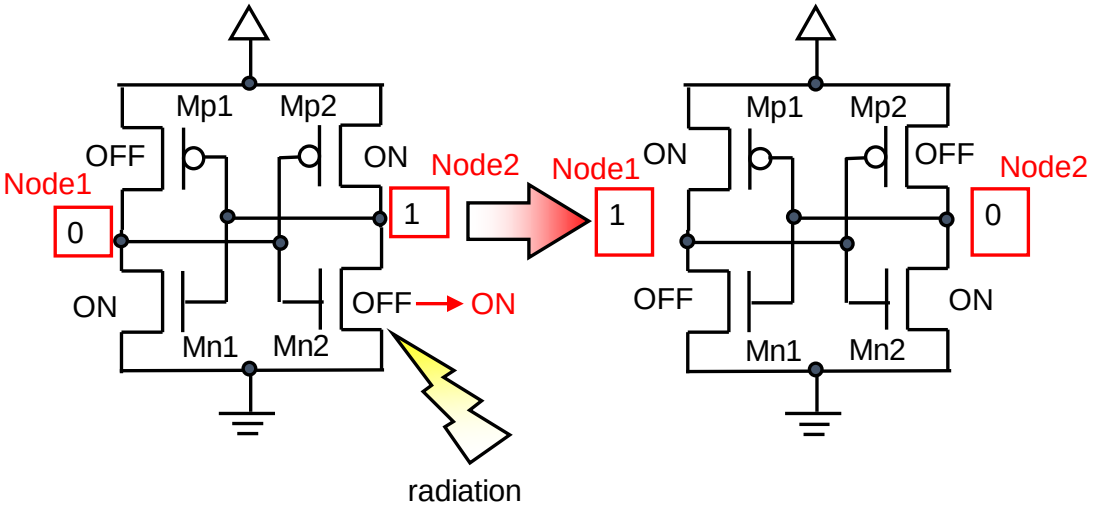

Fig. 3-4. A mechanism of SEU in the latch memory circuit.

Charge generated by the ionization due to charged particle incident is collected to the memory node through the off-state transistor and induces to flip the memory state in each memory node. In the case of charged particle incident to the drain in the off-state transistor, large amount of charge is collected to the drain because charge collection is particularly large on the reverse biasing p-n junction. Collected charge which is over the critical charge (Q_c) that means of minimum charge to induce single event phenomenon flips electrical potential of Node1 and Node2. Q_c differs by transistor parameter such as structure, size, impurity concentration and supply voltage. Total amount of collected charge depends on the number of initial generated charge which is induced by the ionization due to charged particle incident and this initial generated charge depends on the energy of charged particle and the kinds of it.

To prevent the error due to SEU, several circuit techniques are studied in the past. The dual interlocked storage cell (DICE)[3-5), (3-6)] (Fig.3-5) circuit and triple modular redundancy (TMR)[3-7)] (Fig.3-6) circuit are well-known as techniques which improving SEU tolerance. These circuits techniques are based on the concept of “redundant”, i.e. SEU is never occurred even if charge was collected on single transistor because one memory state was maintained by multiple transistors.

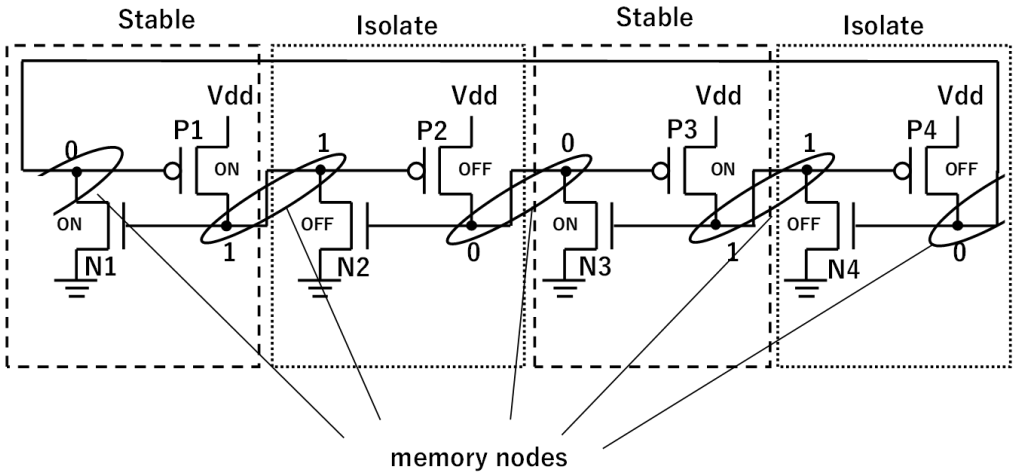

Fig. 3-5 Schematic diagram of dual interlocked storage cell (DICE).

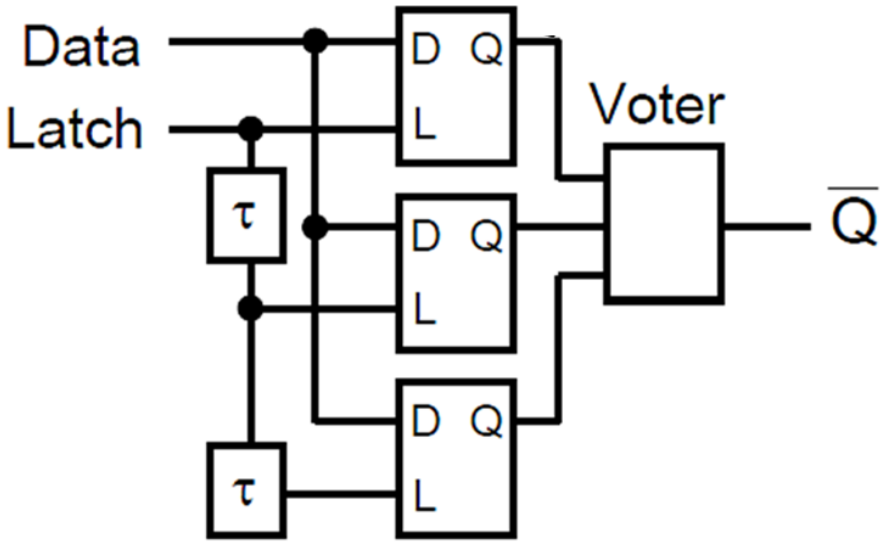

Fig. 3-6 Block diagram of triple modular redundancy (TMR).

In the recent years, transistor size becomes extremely small due to the demands for high integration. As a result of this, Q_c becomes small and the distance between neighbor transistors has been becoming significantly narrow in recent integrated circuits. Therefore, SEU is easy to occur in such electric devices and new issues regarding to SEU are appeared. One of the issues is the multiple cell upset (MCU). MCU means that multiple memory cells are flipped simultaneously by single charged particle incident. And, the reason why MCU is occurred is that radiation induced charges are collected to multiple transistors simultaneously due to the distance between transistors are becoming narrow. This phenomenon calls “charge sharing phenomenon”. A conceptual diagram of charge sharing is shown in Fig.3-7. Similar issues are occurred on the redundancy circuits. This means that SEU tolerant by redundancy becomes not effective enough due to multiple transistors are flipped simultaneously. This is one of the serious issues in recent integrated circuits.

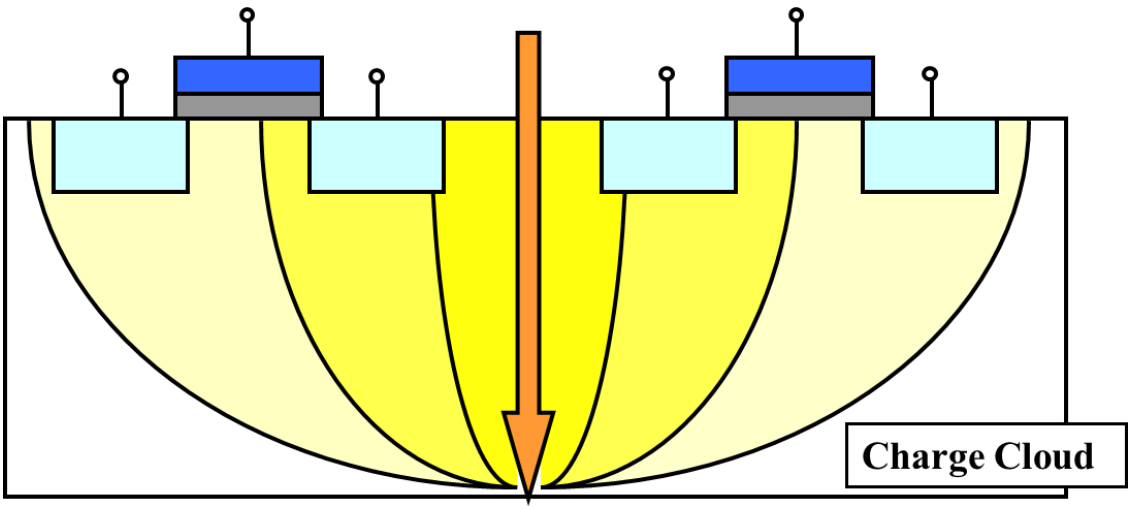

Fig. 3-7 A conceptual diagram of charge sharing.

(2) Single Event Transient (SET)

In the case of charged particle penetrate to transistors and generated charge is collected to transistors, the collected charge appears as pulse noise on the output. This pulse noise which is induced by charged particle is called “Single Event Transient (SET)”. SET which has certain amplitude is often recognized real output signal to the next stage circuit and induces the serious malfunction on many kinds of logic circuits. The amplitude and width of SET depends on the energy of charged particle. The example of the differences of SET pulses depends on LET is shown in Fig.3-8.

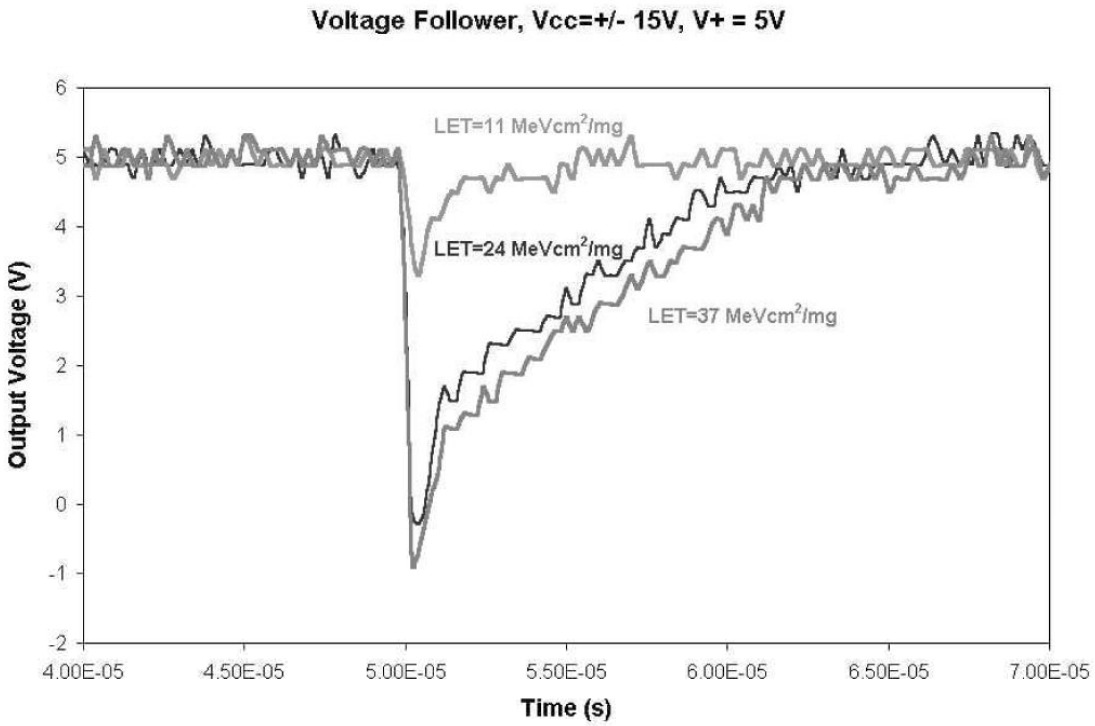

Fig. 3-8 The example of the differences of SET pulses depends on LET[3-8].

(3) Single Event Latch-up (SEL)

SEL is the one of destructive phenomenon due to the charged particle. In the devices which are composed with CMOS process, parasitic transistors are turned on in a moment due to injection of radiation induced charges. As a result, current pass is created between supply voltage and ground, and large current continue to flow. Eventually, electrode meltdown and serious loss of functions in the electric devices are occurred. Effective countermeasure of SEL is to add the circuit which have the function of large current flow detection and power reset function.

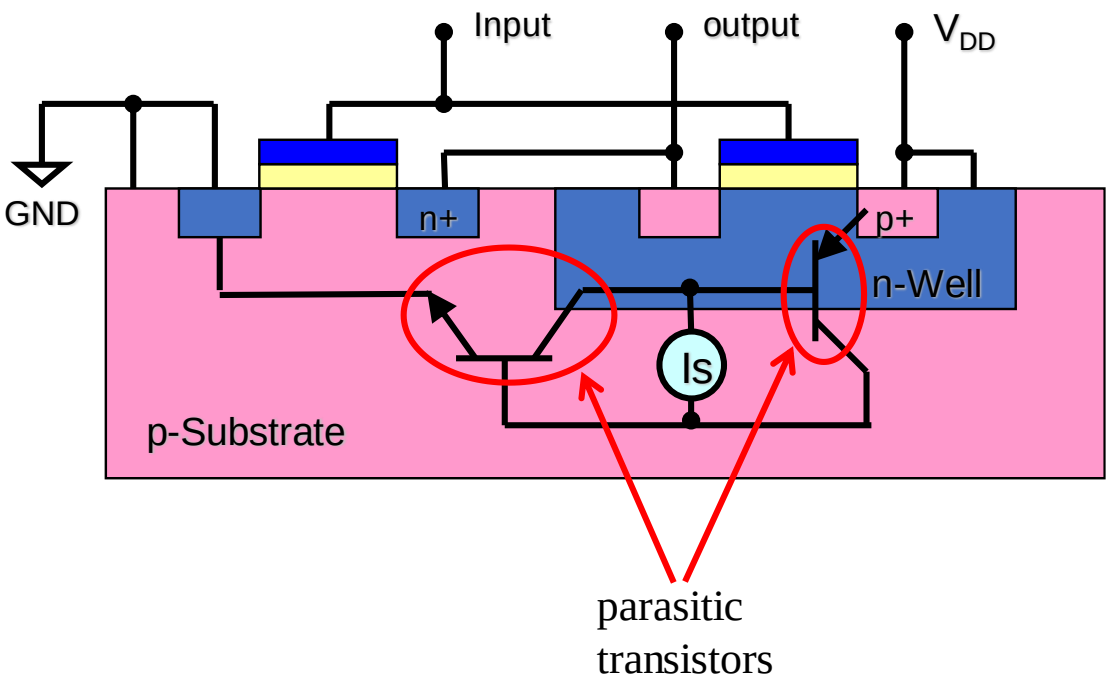

Fig. 3-9 Mechanism of Single Event Latch-up.

(4) Single Event Burn-out (SEB)

SEB is also destructive phenomenon which occur in the power MOSFET mainly. Fig. 3-10 shows cross section and equivalent circuit of power MOSFET. As shown in Fig. 3-10, power MOSFET includes parasitic bipolar transistor. Charged particle incident lead to turn-on this parasitic bipolar transistor and large current flow in a moment. As a result, power MOSFET is burned out and loss of function because power MOSFET is applied high voltage to operate, generally. SEB also occur in bipolar transistor devices which have vertical structure same as power MOSFET.

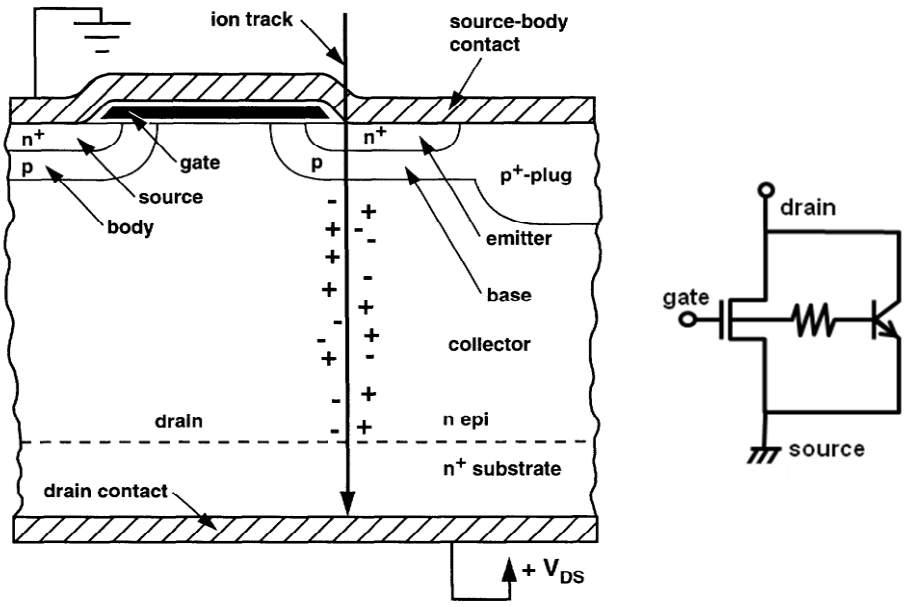

Fig. 3-10 Cross section and equivalent circuit of power MOSFET[3-9].

(5) Single Event Gate Rupture (SEGR)

Differ from the other SEE, SEGR is destructive phenomenon on the gate oxide in the power MOSFET. The ionizing charges which are induced by the charged particle incident in the vicinity of gate oxide move to the interface of gate oxide due to be led by electric field. As a result, electric field intensity becomes stronger on the gate oxide and dielectric destruction is occurred.

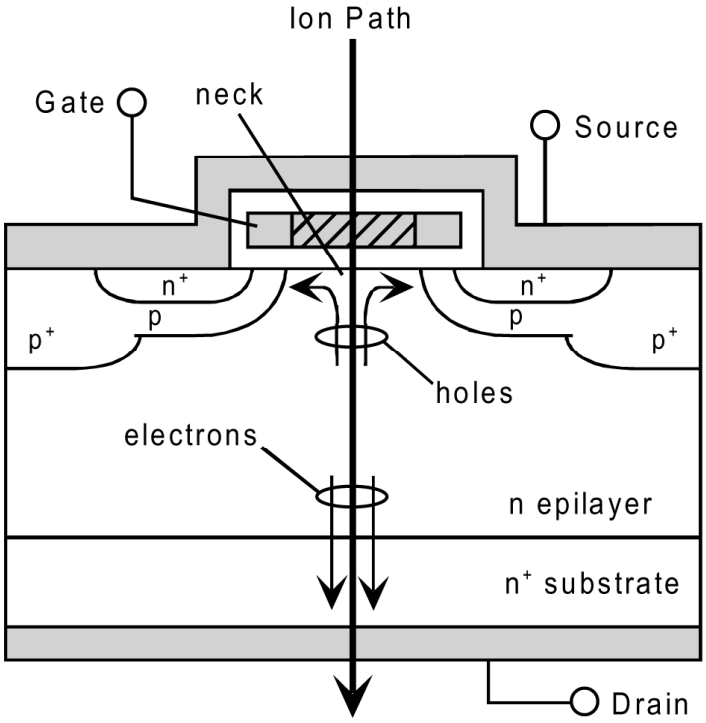

Fig. 3-11 Mechanism of Single event gate rupture (SEGR)[3-10].

3.3 Conclusion

In this chapter, types and mechanisms of radiation effects on the semiconductor material devices were explained in detail. There are various radiation effects depend on the device types or operation conditions. Lattice displacement damage and TID effect makes performance degradation on the electronic devices. These effects can be taken measures by any shields because they are related to the total amount of irradiated charged particles. On the other hands, SEE is related to the position of charged particle incident. Therefore, this cannot be taken measures by shields, simply. Regarding to the SEE, it is significantly important to understand its mechanisms to take appropriate countermeasures. Particularly, regarding to the SEU, conventional countermeasures are becoming not effective enough on the recent high integrated electronic devices due to the charge sharing phenomenon.

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Chapter 4:

Charge Sharing Induced SEU Simulation by Using the Device Simulator

4.1 Introduction

In the case of the electronic devices are need to be investigate radiation tolerant before space use, radiation irradiation test must be performed in general. However, radiation irradiation test is not easy to perform. There are few radiation irradiation facilities in domestic and abroad because very large-scale accelerator equipment is needed to radiation irradiation facility. In addition, the facility machine time is very limited because there are too many users who want to use the radiation facility to perform radiation test. Other reason why radiation test is not easy to perform is its high cost for preparing the test sample and test equipment. One of the good ideas to clear up these issues is using the simulation method. Due to the simulation can be performed in virtual at all, limited machine time of radiation irradiation facility and high cost for preparation of radiation irradiation test can be ignored. Regarding to SEU which becomes serious issue in resent high integrated electronic circuit, the estimation methods by using computer simulation were studied and developed in the past. P. E. Dodd performed SEU simulation by using the mixed mode simulation which is the combined simulation of device simulation and circuit simulation[4-1]. Charge collection due to the charge sharing on 130 nm CMOS technology was simulated by 2-dimension (2D) device simulation in the study of Oluwole A. Amusan et al[4-2]. There are many studies regarding to SEU, MCU or charge sharing other than these such as different transistor size simulation and 3D device simulation etc[4-3]-[4-7]. As described in the chapter 1, the objective of this work is to establish the estimation method for the behavior of charge sharing and SEU occurrence simultaneously by using device simulator only. In addition, the validity of the simulation method in this work is evaluated through the comparison of radiation irradiation test result of same transistor

size memory device. Comparison result is indicated in the chapter 5.

4.2 Hyper Environment for Exploration of Semiconductor Simulation (HyENEXSS)

HyENEXSS is the three-dimensional (3D) technology computer aided design (TCAD) simulator originally developed by Semiconductor Leading Edge Technologies Inc. (Selete) [4-8]. HyENEXSS is composed by some software as 3D process simulator (HySyPros), 3D device simulator (Hyper Device-Level Electrical Operation Simulator: HyDeLEOS) Graphic software (SGraph) etc. 3D device simulator HyDeLEOS is used in this work. Device simulator solves the semiconductor basic equation regarding to input information of device structure and boundary condition, and outputs electronic characteristics such as electrode current. In particular, the method how to solve the Poisson's equation, electron current continuity equation and hole current continuity equation simultaneously is called “Drift-Diffusion model (DD model)” in this simulator. Basic equations included in the HyDeLEOS are listed in table 4-1. Note that the meanings of the symbols in basic equations are listed in table 4-2. HyDeLEOS outputs the electronic characteristics by using the combination of DD model based on these basic equations, carrier mobility model and carrier generation/recombination model.

Table 4-1. Basic equations in the HyDeLEOS

Name	Equation
Poisson's equation	$\mathrm{div}(\varepsilon grad\psi) = -q(N_D - N_A + p - n) - \rho_{fix} - \rho_n - \rho_p$
electron current continuity equation	$\frac{\partial n}{\partial t} - div\left(\frac{J_n}{q}\right) = U$
hole current continuity equation	$\frac{\partial p}{\partial t} - div\left(\frac{J_p}{q}\right) = U$
heat conduction equation	$\rho c\frac{\partial T_L}{\partial t} - div(\kappa_L grad T_L) = Q_L$

Table 4-2. Meanings of symbols in basic equations

Symbol	meaning	Unit
ψ	Electric potential	V
q	Positive charges (= 1.6×10^{-19})	C
ε	permittivity	F/cm
N_D	Density of donner	cm^{-3}
N_A	Density of accepter	cm^{-3}
n, p	Density of electrons and holes	cm^{-3}
ρ_{fix}	Fixed charges	C
ρ_n	Charges of electron-mediated trap level	C
ρ_p	Charges of hole-mediated trap level	C
J_n,J_p	Current density of electrons and holes	A/cm^2
U	Carrier generation/recombination term	cm^{-3}/s
T_L	Lattice temperature	K
κ_L	Thermal conductivity of lattice	W/cmK
Q_L	Exothermic term	W/cm^3

To run the device simulation on the HyDeLEOS simulator, user should prepare the structure file and calculation condition file. Physical structure parameters such as gate length, thickness of gate oxide and size of substrate etc., impurities concentration parameter, position of electrode and “mesh” parameter are included in the structure file. Mesh is designated the boundary to solve the basic equations. Although more detail simulation can be performed with the finer mesh size, it needs too much time for calculation. The convergence condition of equations, designation of physical model and input bias conditions are included in the calculation condition file. Before preparing the structure file, users are recommended to draw the design drawing draft because the structure file must be written by text. An example of design drawing draft for 2D device simulation is shown in Fig. 4-1. And the structure file example which is based on the Fig. 4-1 is shown in Fig. 4-2, the calculation file example is shown in Fig. 4-3.

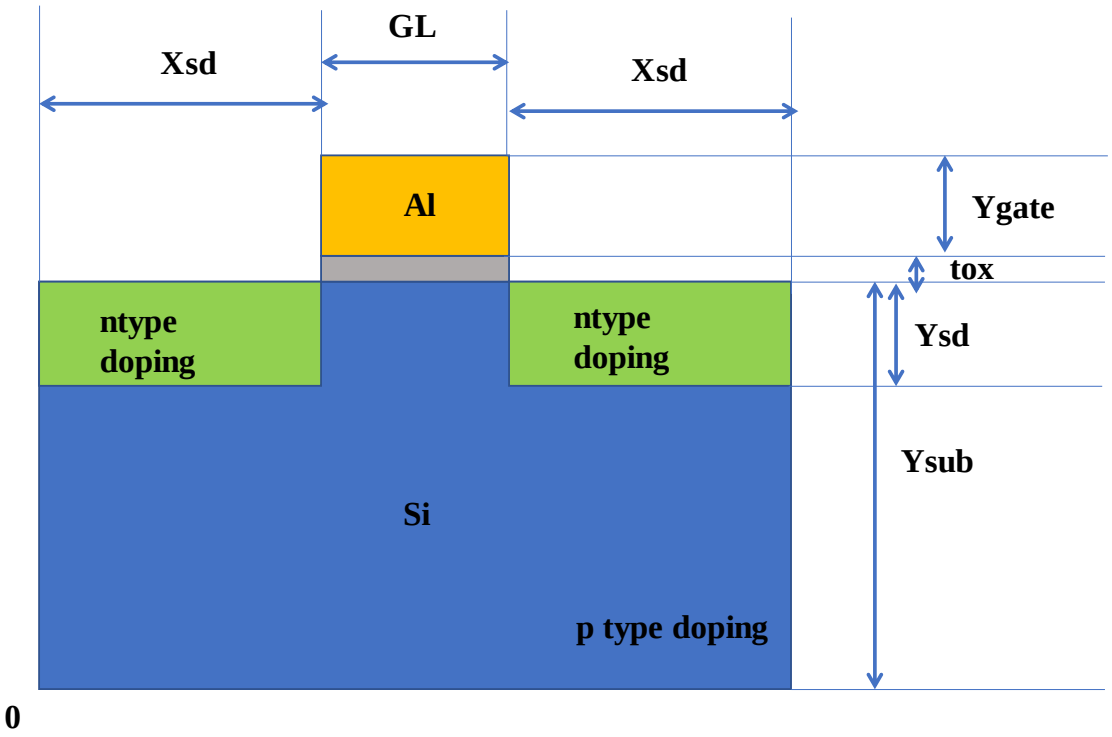


Fig. 4-1. An example of design drawing draft for HyDeLEOS simulation.

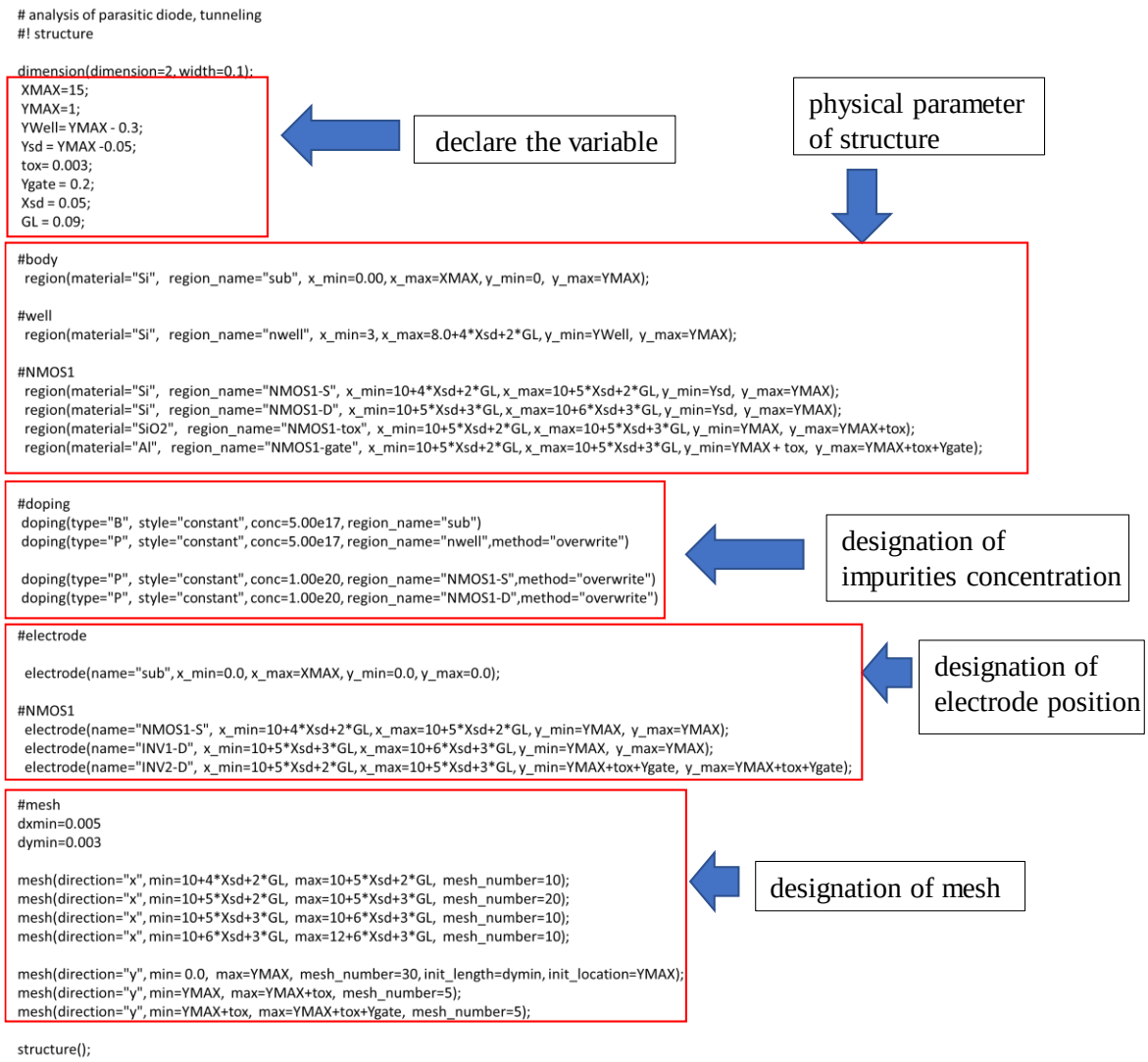


Fig. 4-2. The example of structure file for HyDeLEOS simulation.

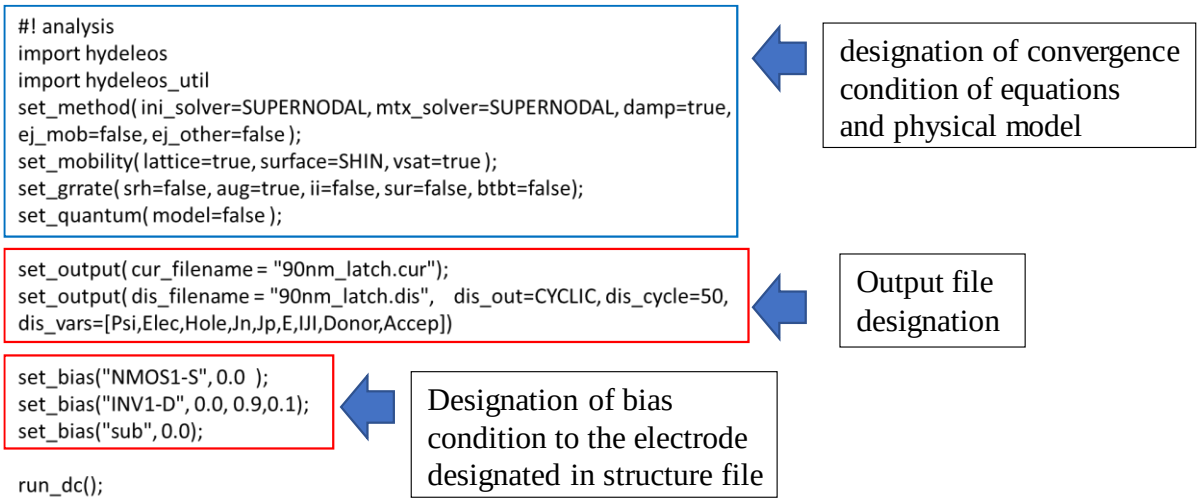


Fig. 4-3. The example of calculation condition file for HyDeLEOS simulation.

4.3 Device simulation model for charge sharing induced SEU simulation

HyDeLEOS has a function of charge injection to a certain position and time. HyDeLEOS can also simulate the behavior of injected charges by using DD model, carrier mobility model and carrier generation/recombination model. Therefore, this simulator is useful for simulating charge generation and charge collection behavior in the case of charged particle incident to the semiconductor devices. In this work, to directly simulate the SEU due to the charge collection on the circuit, a simple memory circuit model was built on the 3D device simulator. Fig. 4-4 shows the schematic diagram of memory circuit. Stored data within memory circuit is kept as the electric potential of Node1 and Node2. Electrodes of transistors (P1, P2, N1 and N2) were connected virtually on device simulator. Design drawing draft of the 3D device simulation model same as Fig. 4-1 is illustrated in Fig. 4-5.

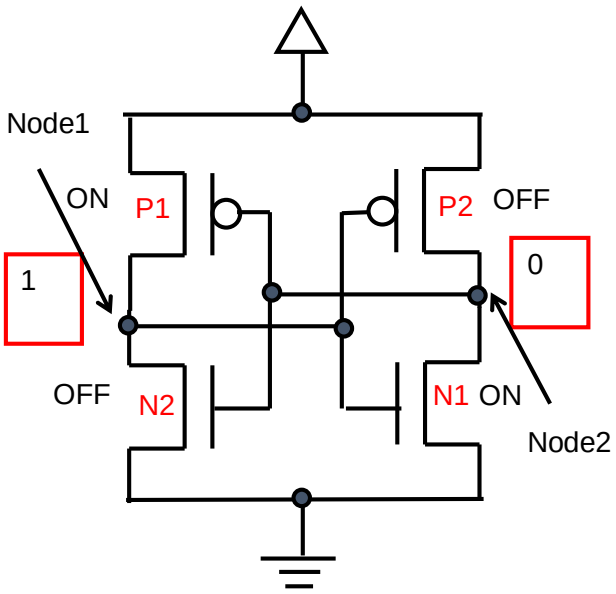


Fig. 4-4. The schematic diagram of memory cell for device simulation.

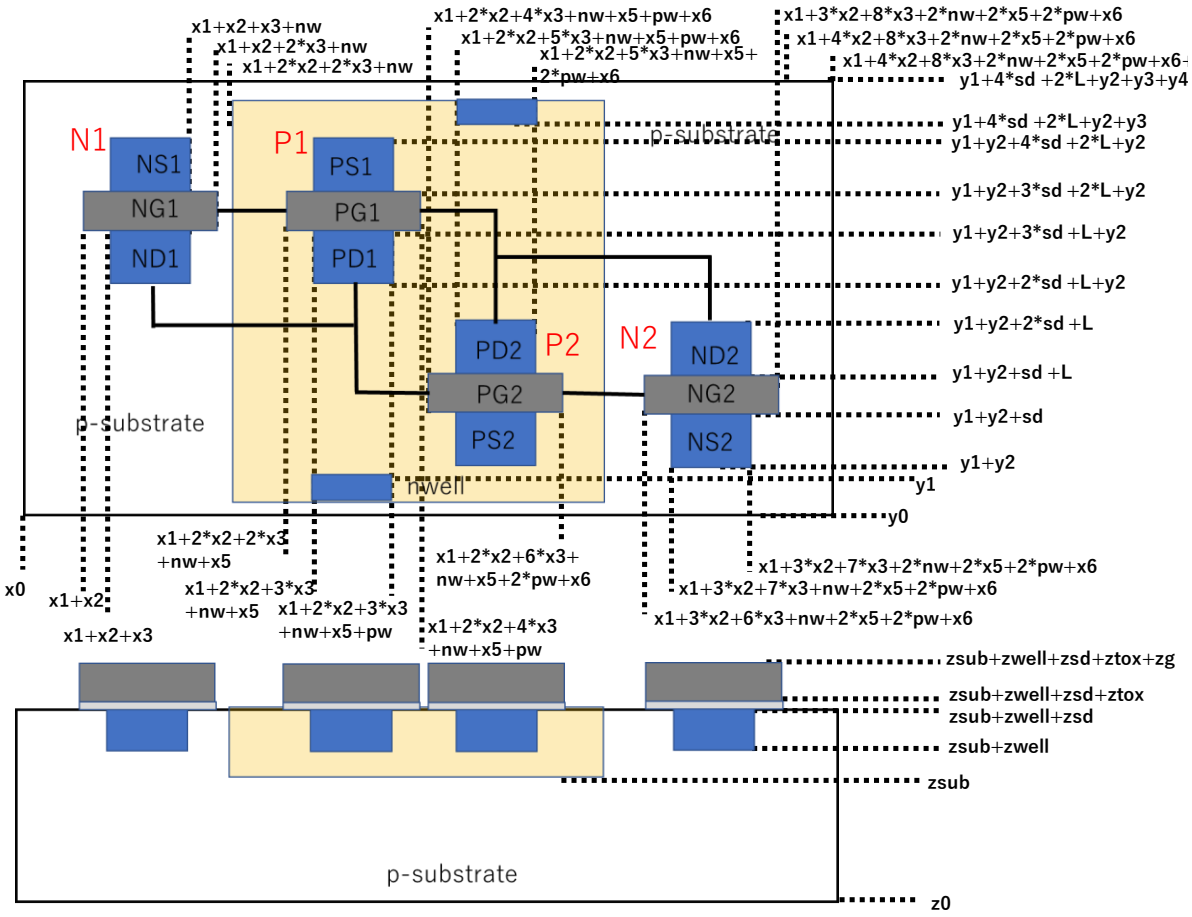


Fig. 4-5. The design drawing draft of the 3D device simulation model.

N-type MOSFET and p-type MOSFET in the device simulation model were designed as Fig. 4-6, 4-7. Both transistors gate lengths were designed as 65 nm, gate widths were designed as 100 nm and SiO_2 gate oxide thickness is designated as 2nm. In n-type MOSFET, boron was doped to the substrate as p-type impurity with 3×10^{18} cm^{-3} concentration, and phosphorus was doped to the n-type diffusion regions with 1×10^{20} cm^{-3} concentration. Regarding to p-type MOSFET, phosphorus was doped to the n-well as n-type impurity with 7×10^{18} cm^{-3} concentration, and boron was doped to the p-type diffusion regions with 1×10^{20} cm^{-3} concentration.

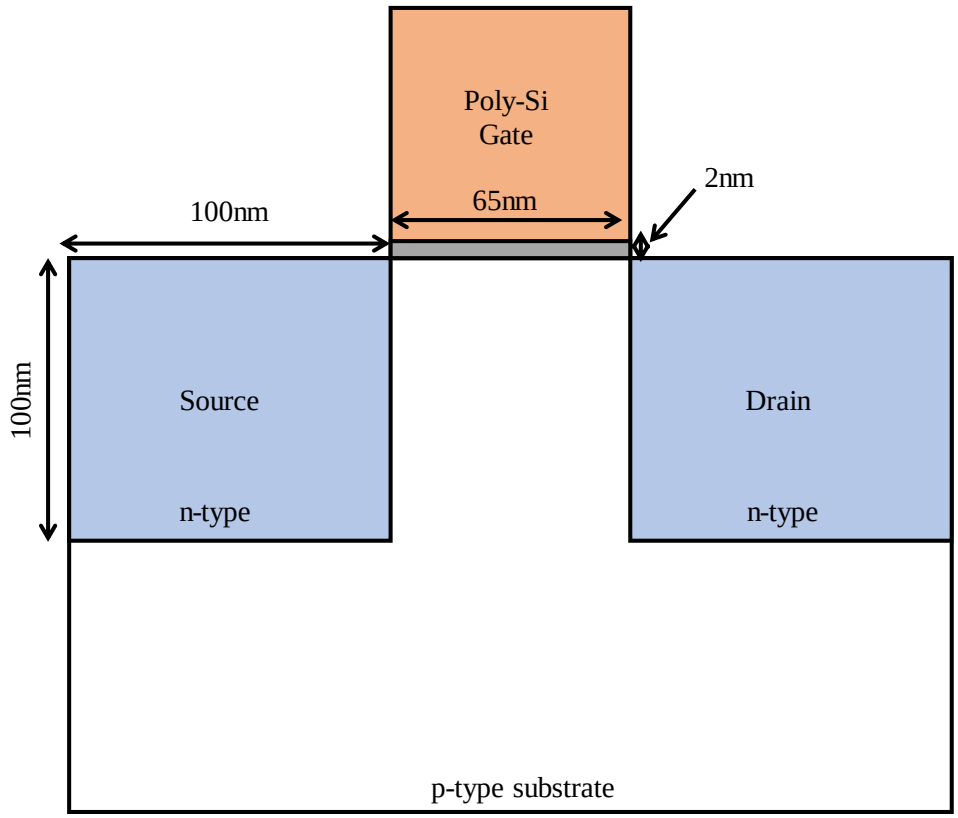


Fig. 4-6. The design drawing draft of the n-type MOSFET model.

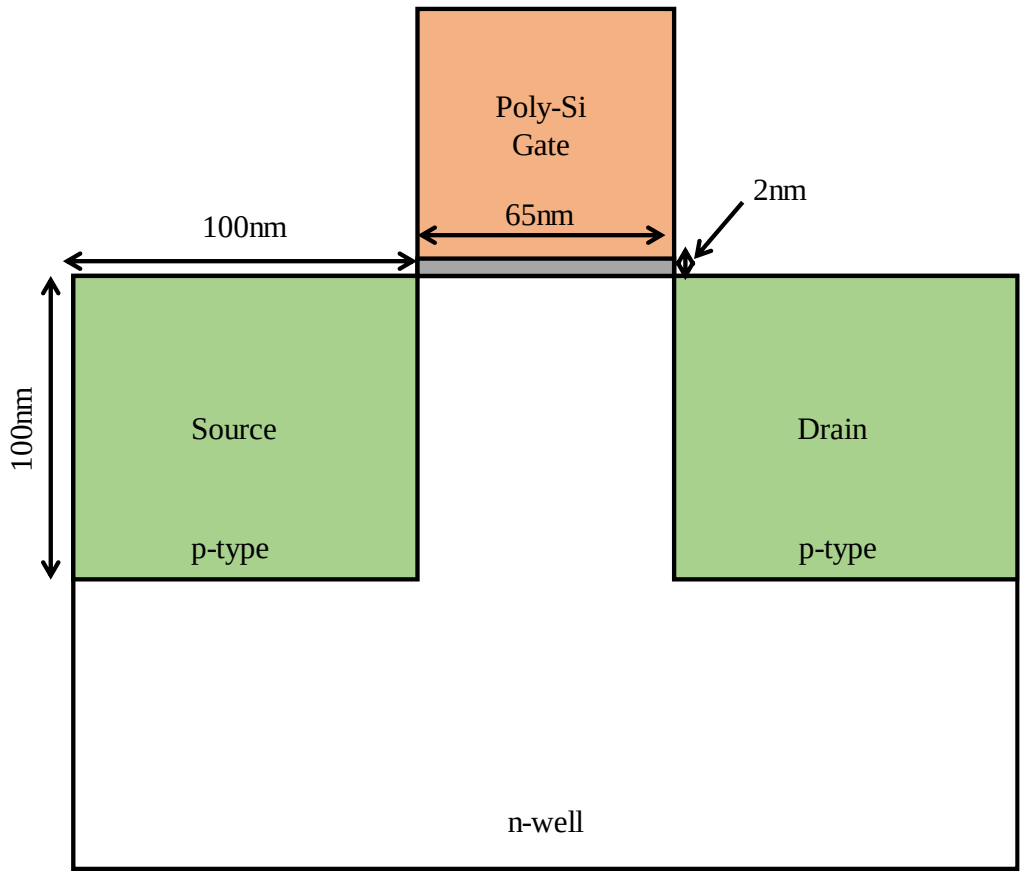


Fig. 4-7. The design drawing draft of the p-type MOSFET model.

The structure file was described based on these design drawing draft and memory circuit model was drawn on device simulator indicated as Fig 4-8. Whole simulation area was designated as 4 × 5 × 15 μm which includes target memory cell.

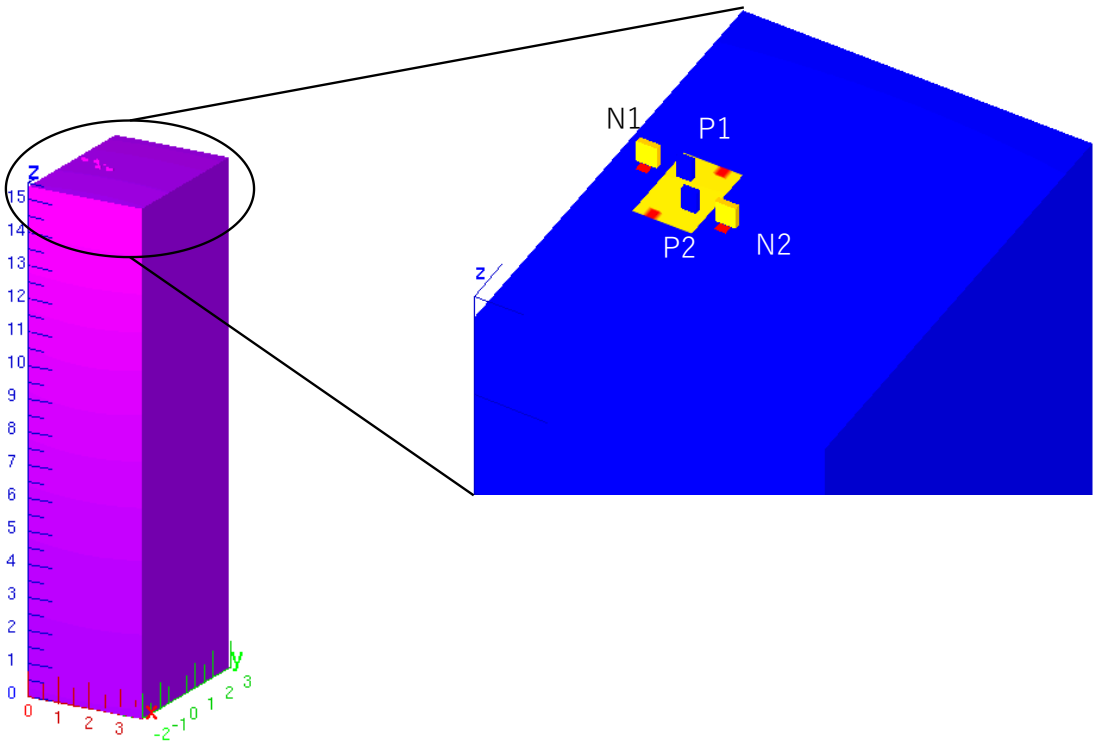


Fig. 4-8. The device simulation model which was drawn on device simulator.

4.4 Radiation induced charge injection and collection behavior simulation on device simulator

By using the device simulation model which is indicated in Fig 4-8, memory circuit function and radiation induced charge collection behavior can be simulated, simultaneously, namely, SEU due to the charge sharing can be simulated on device simulator. As shown in Fig.4-9, to simulate the behavior of radiation induced charge collection to the transistor of memory cell, charges which are assumed the ionization due to charged particle incident is injected to the position of certain distance far from N2 transistor. To make comparative verification with radiation irradiation test result, a total amount of injected charges was set to same as the charges which are generated in the case of charged Xe ion incidence to the semiconductor. Other reason why Xe ion is selected is that the Xe ion has the LET as 68.8 MeV/(mg/cm^2) in silicon. As Fig. 2-3 on chapter 2 shows, the radiation environment regarding to the GCR on orbit, heavy ions exist on orbit is mostly the ions lighter than Fe and its LET is lower than Xe ion. Namely, this verification by Xe ion can be treated as worst case testing and this worst case conditions is selected so that the robust circuit for charge sharing phenomenon can be designed even if in this worst case conditions. Note that, the encounter probability with the Xe ion in orbit is said only once in a hundred years. The total amount of injected charges (N) is led from the formula (4-1) which depend on the LET of charged particle.

$$N = \frac{LET \times \rho \times d}{E} \qquad (4-1)$$

ρ : density of silicon (mg/cm^3)

d : the distance of heavy ion penetration in silicon (cm)

E : energy to create one electron-hole pair in silicon (eV)

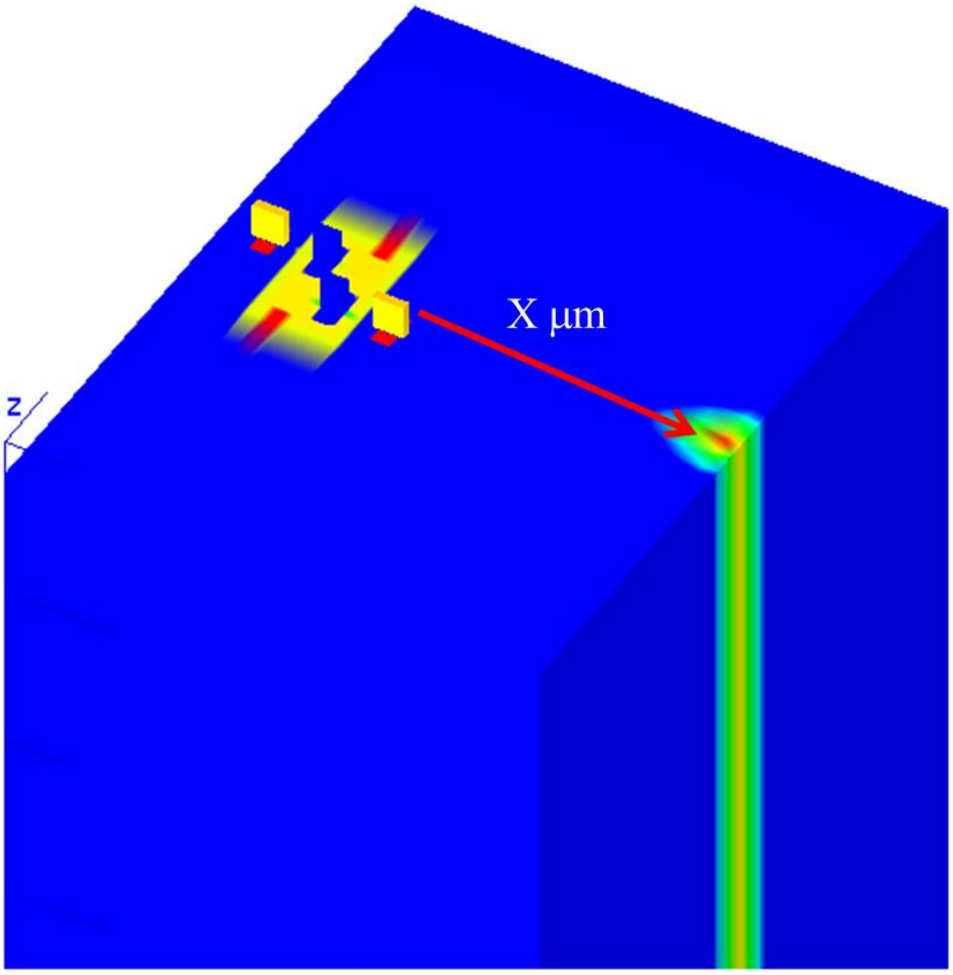


Fig. 4-9. The simulation image of charge generation on the device simulator.

Transient analysis on device simulator was performed from 0 nsec to 10 nsec with 1×10^{-13} sec minimum division. Charges which were assumed the ionization due to charged particle incident were injected to certain position at the time of 5.0 nsec from simulation start time. At first, to validate whether the device simulation model can simulate the memory function and SEU occurrence simultaneously, device simulation was performed with the conditions that charges inject to the drain of N2 transistor directly. Simulation result is shown in Fig. 4-10.

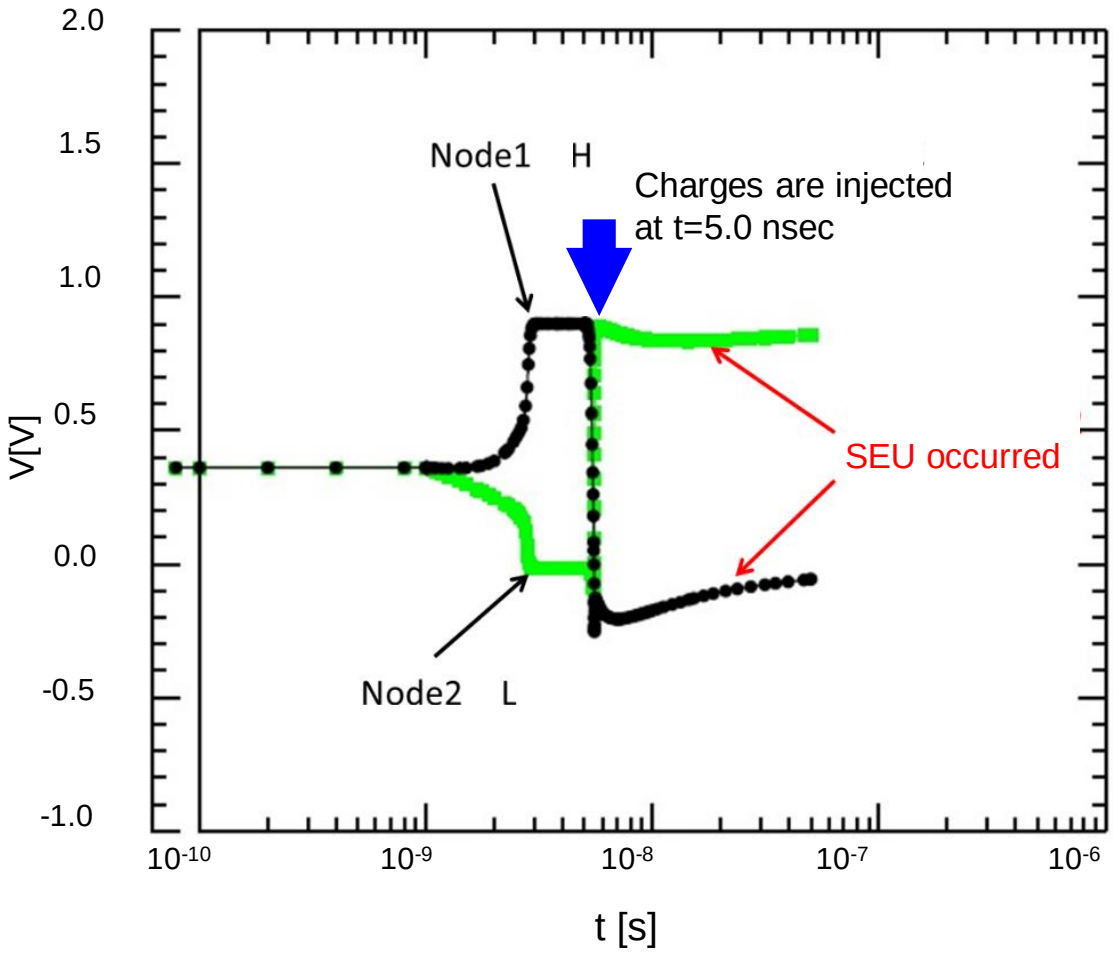
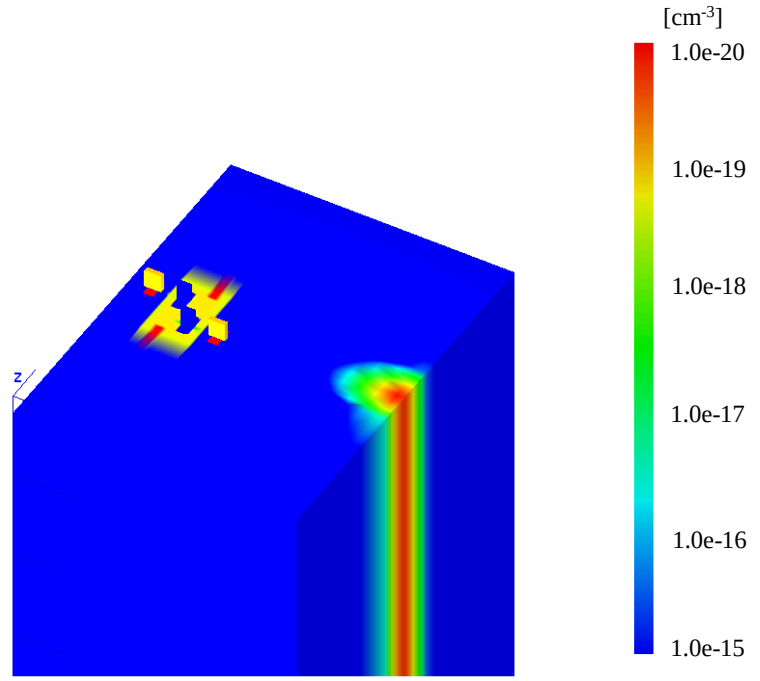


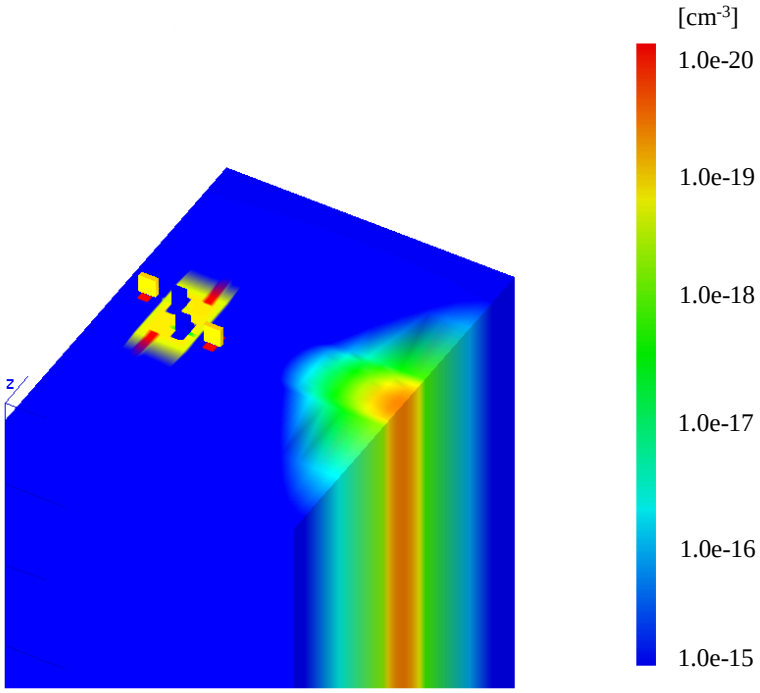
Fig. 4-10. Device simulation result with the conditions which charges injecting to the N2 transistor drain.

In Fig. 4-10, electric potential of Node1 is indicated as black plots and electric potential of Node2 is indicated as green plots. Electric potentials of Node1 and Node2 are fixed to “H” and “L” as soon as simulation starting. Charges which were assumed the ionization due to the radiation irradiation were injected at the time of 5.0 nsec from simulation start. Each electric potential was flipped after the charge injection, namely, SEU occurrence was observed in the memory circuit on the device simulator. Injected charges to the N2 transistor drain are collected to N2 transistor immediately, and N2 transistor off-state is switched to on-state due to this charge collection. As a result, electric potential of Node1 is changed from “H” to “L” and this change induces the change of Node2 electric potential from “L” to “H”. According to the simulation result which is indicated in Fig. 4-10, it is confirmed that the device simulation model in this work can simulate the memory function and SEU occurrence, simultaneously.

Next, the device simulation with the conditions of charges injected to the certain distance from N2 drain is performed. Injected charges spread in a circle and the spread speed depends on the drift-diffusion of charges and electric field of the transistors. A behavior of injected charges spread which depends on the elapsed time is shown in Fig. 4-11 (a) to (f). And the color gradation in Fig. 4-11 indicates electron density of simulation field.

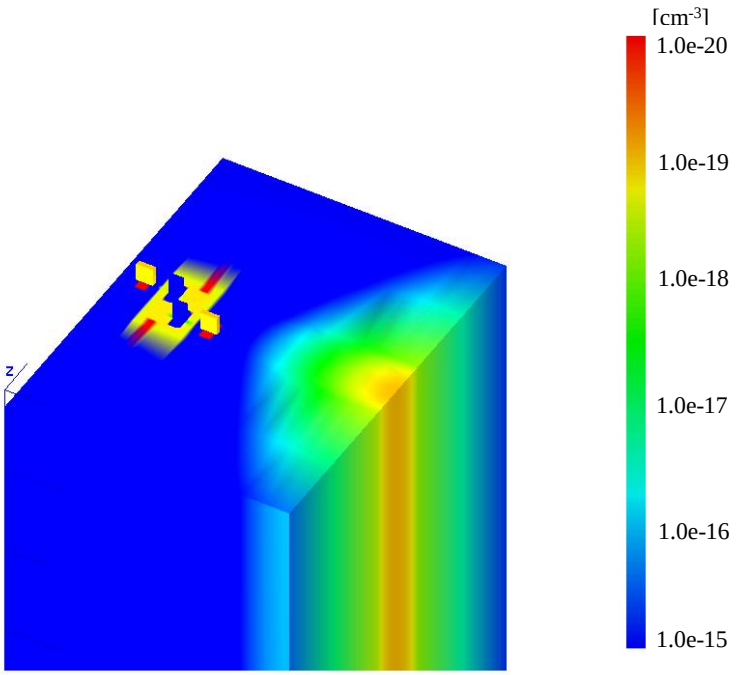


(a) t = 5.01 nsec

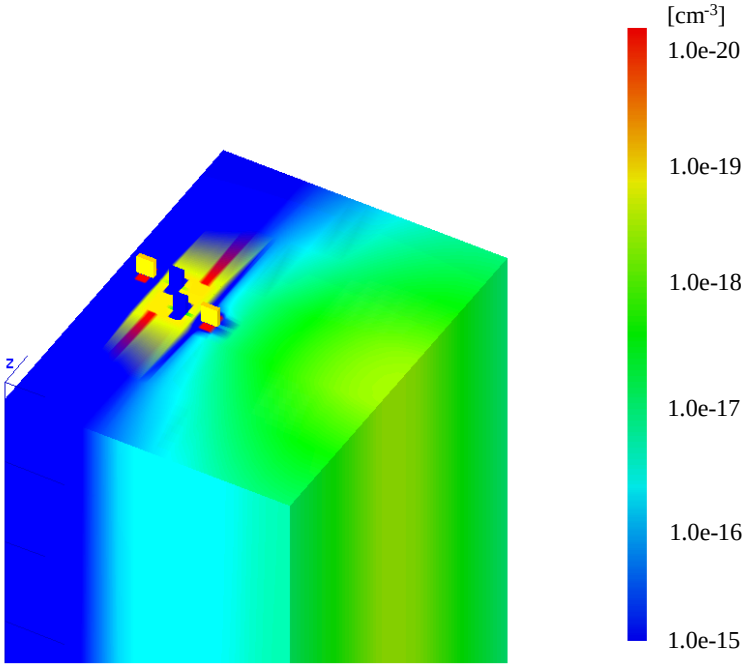


(b) t = 5.05 nsec

Fig. 4-11. A behavior of injected charges spread which depends on the elapsed time.

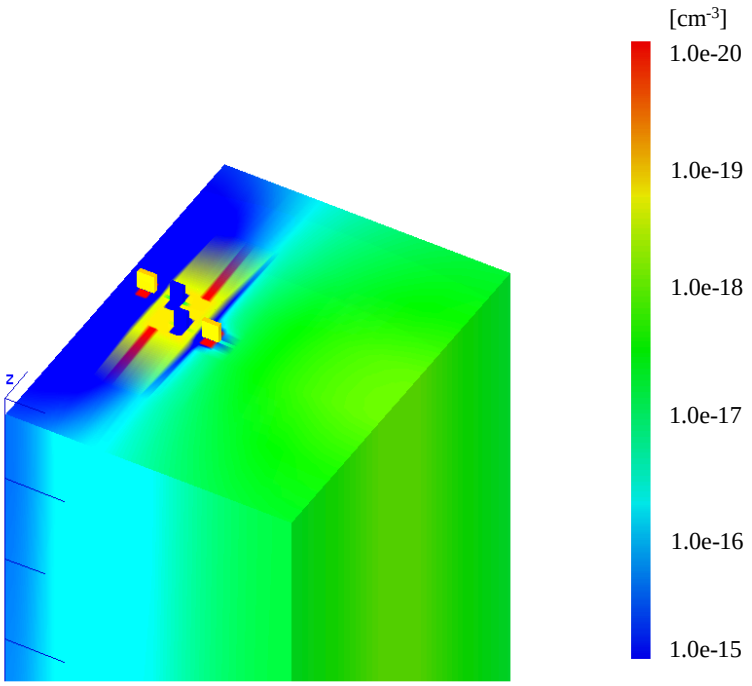


(c) t = 5.1 nsec

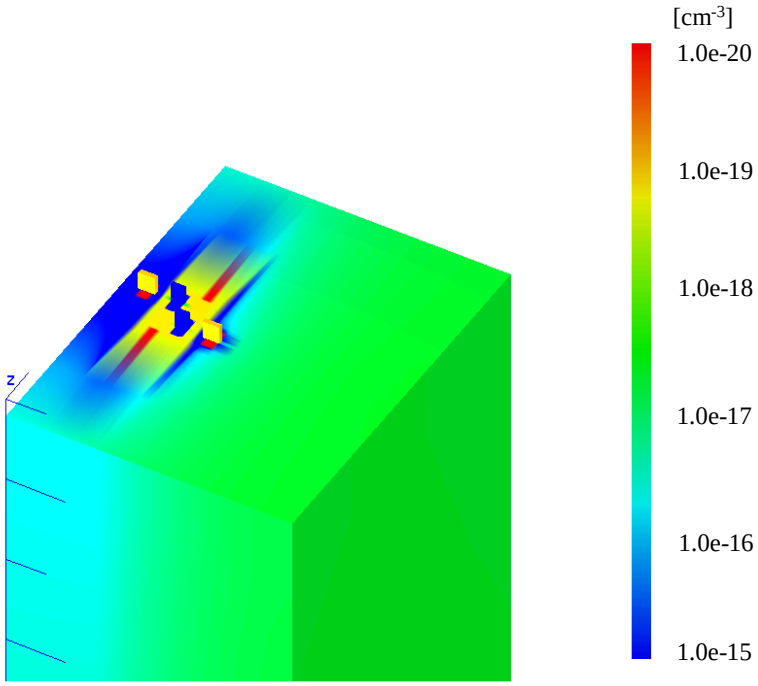


(d) t = 5.5 nsec

Fig. 4-11. A behavior of injected charges spread which depends on the elapsed time.



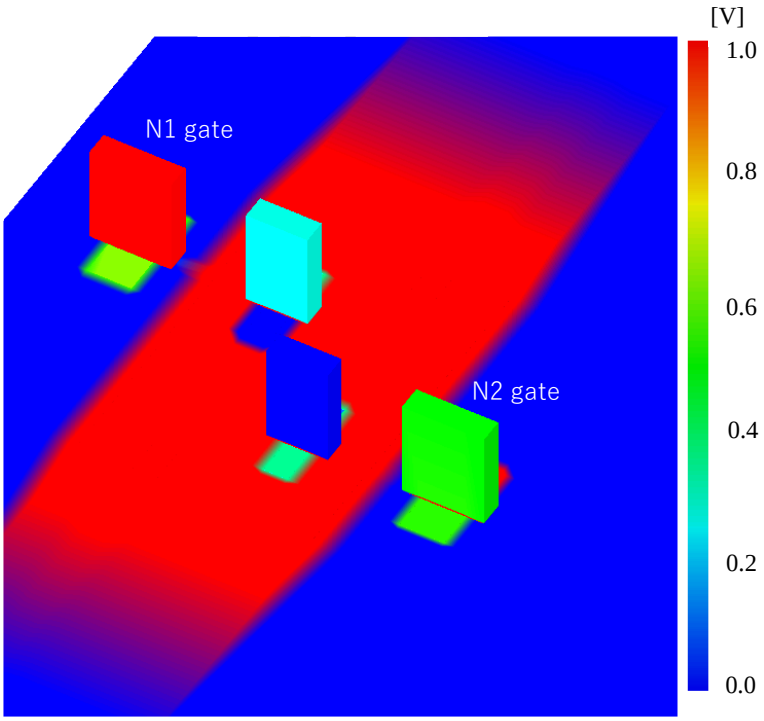
(e) t = 6.0 nsec



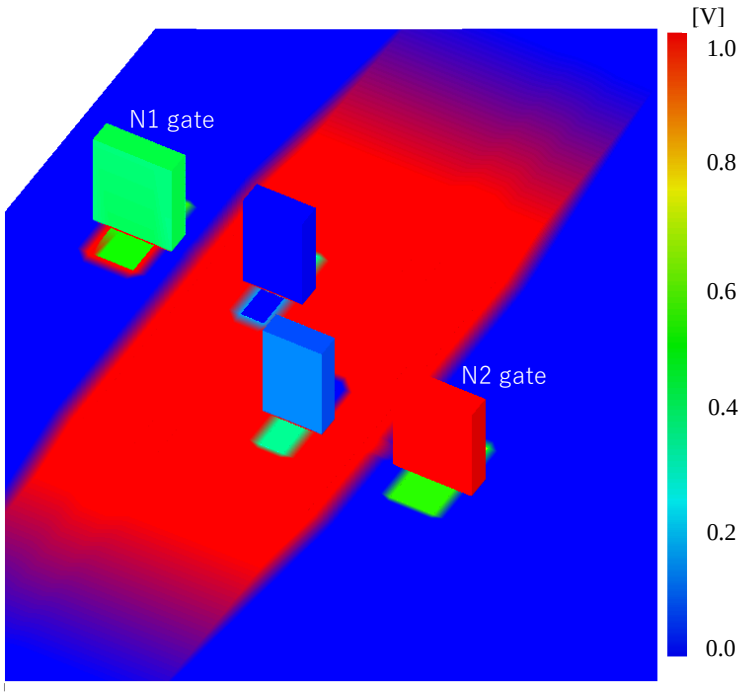
(f) t = 10.0 nsec

Fig. 4-11. A behavior of injected charges spread which depends on the elapsed time.

Simulation results of electric potential in two different cases of charge injection position are illustrated in Fig. 4-12 (a) to (d). And the color gradation in Fig. 4-12 indicates electric potential of simulation field. One condition is to inject charges to 2.2 μm distance from N2 transistor, the other is to inject charges to 2.6 μm distance from N2 transistor. As shown in Fig. 4-12 (a) and (b), focusing on the electric potential both of N1 and N2 transistor gates, it can be seen that a relationship of electric potential is flipped in the condition of charges injection to 2.2 μm distance from N2 transistor. On the other hand, as shown in Fig. 4-12 (c) and (d), a relationship of electric potential is not flipped in the condition of charges injection to 2.6 μm distance from N2 transistor. This is also indicated that the device simulation model in this work can estimate the SEU occur due to collection of the injected charges at a distant position from memory cell by the transistor of memory cell. Namely, SEU due to charge sharing can be simulated by using this device simulation model on device simulator.

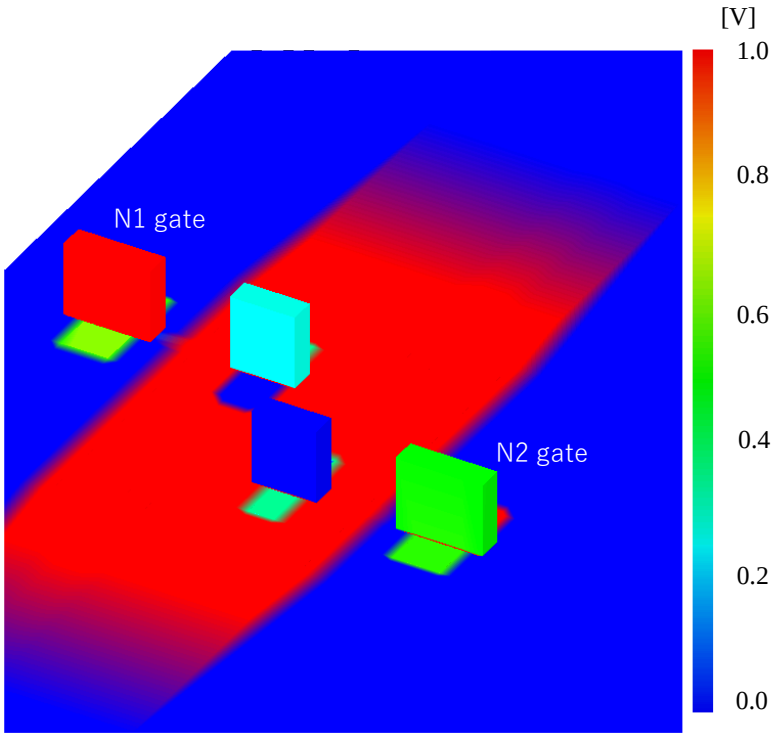


(a) Electric potential with 2.2 μm distance condition at the time of 5.001 nsec.

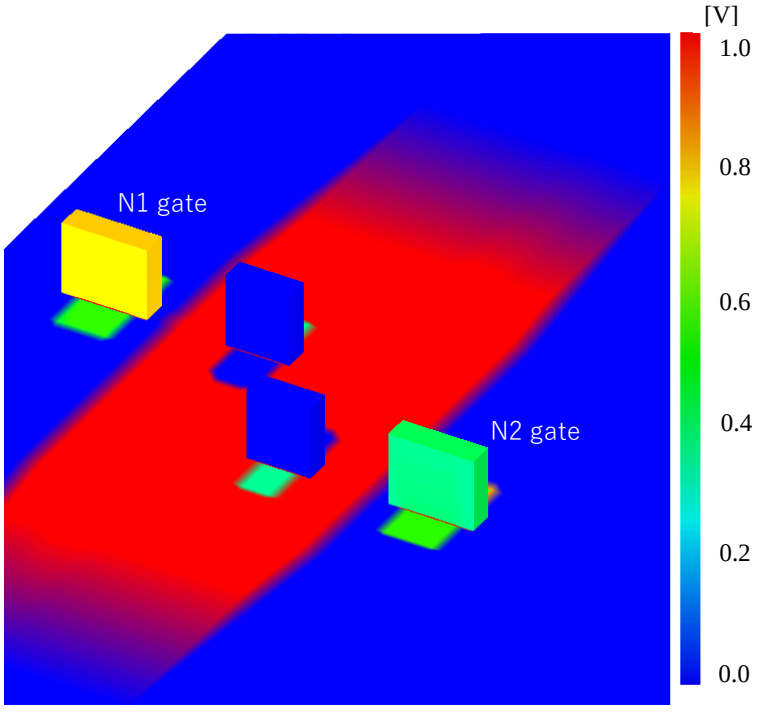


(b) Electric potential with 2.2 μm distance condition at the time of 6.0 nsec.

Fig. 4-12. Simulated electric potential on each condition.



(c) Electric potential with 2.6 μm distance condition at the time of 5.001 nsec.



(d) Electric potential with 2.6 μm distance condition at the time of 6.0 nsec.

Fig. 4-12. Simulated electric potential on each condition.

Time dependent voltage transition of each memory nodes which have different position of charge injection are shown in Fig. 4-13. Simulation results of five different position of charge injection are drawn on same graph. According to the simulation results, it is clearly indicated in the case that charges is injected at the position 2.3 μm or less far from N2 transistor, electric potential of each memory node are flipped. Hence, transistors which exist in the range of 2.3 μm from the center of charged particle incident have the potential to collect the enough charges to flip the electric potential of memory. Namely, SEU due to charge sharing should be occurred in the case of transistors in the memory device are allocated within a radius of 2.3 μm circle.

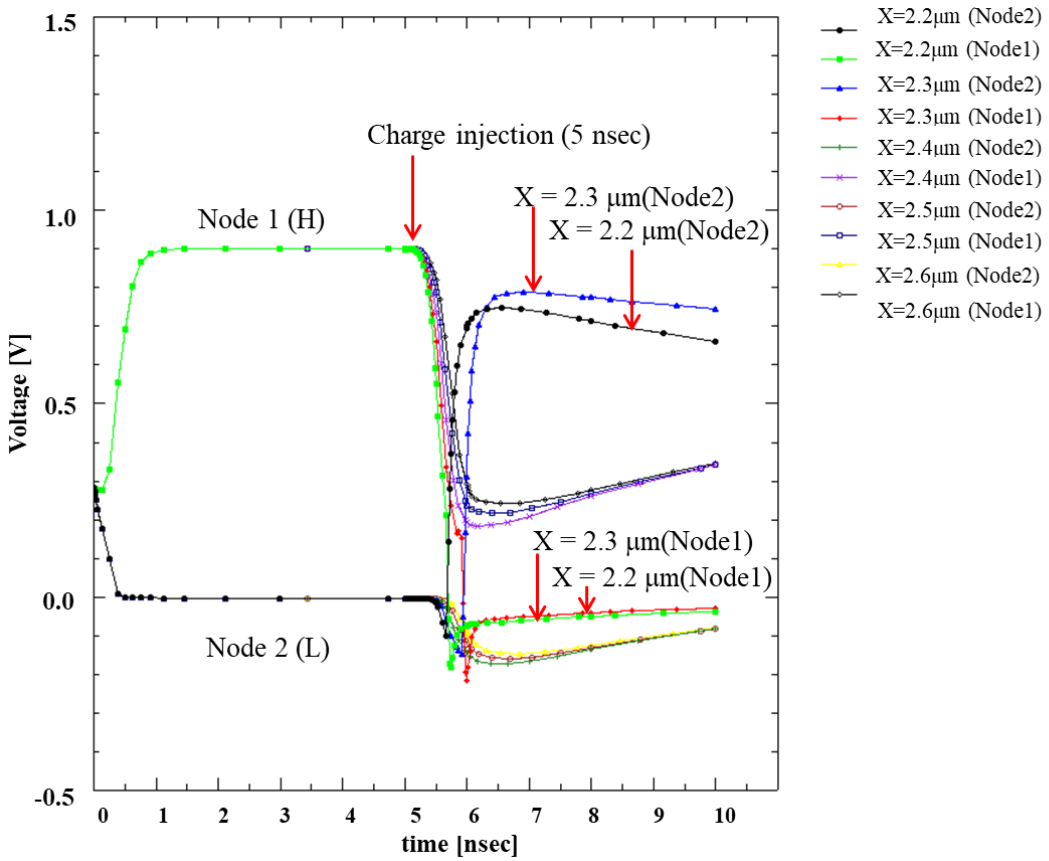


Fig. 4-13. Voltage transition of each memory node as a function of the elapsed time after simulation start with various position of charge injection.

In addition, to investigate the dependence of charge sharing area to the total number of charge injection, the same simulation with various number of charge injection are performed. Assumed charged heavy ions are Kr (LET=40.3 [MeV/(mg/cm^2)]), Ar (LET=15.8 [MeV/(mg/cm^2)]) and Ne (LET=6.6 [MeV/(mg/cm^2)]) which are available heavy ions to radiation irradiation test in the accelerator facility used to experiment of this work. Total number of injected charges which depends on the LET in each heavy ion are calculated by formula (4-1). Figure 4-14 plots the maximum distance between the position of charge injection and off-state transistor in various number of charge injection when SEU was observed. Fitted curve which was calculated by using the formula (4-2) which based on Weibull distribution[4-9] is drawn in same graph.

$$X = 4.85\left(1 - \exp\left(-\left(\frac{N - 0.2}{171.8}\right)^{0.48}\right)\right) \qquad (4-2)$$

It seems that there is trend of saturation in large number of injected charges conditions. This is because a part of injected charges which move long distance are disappeared due to recombination.

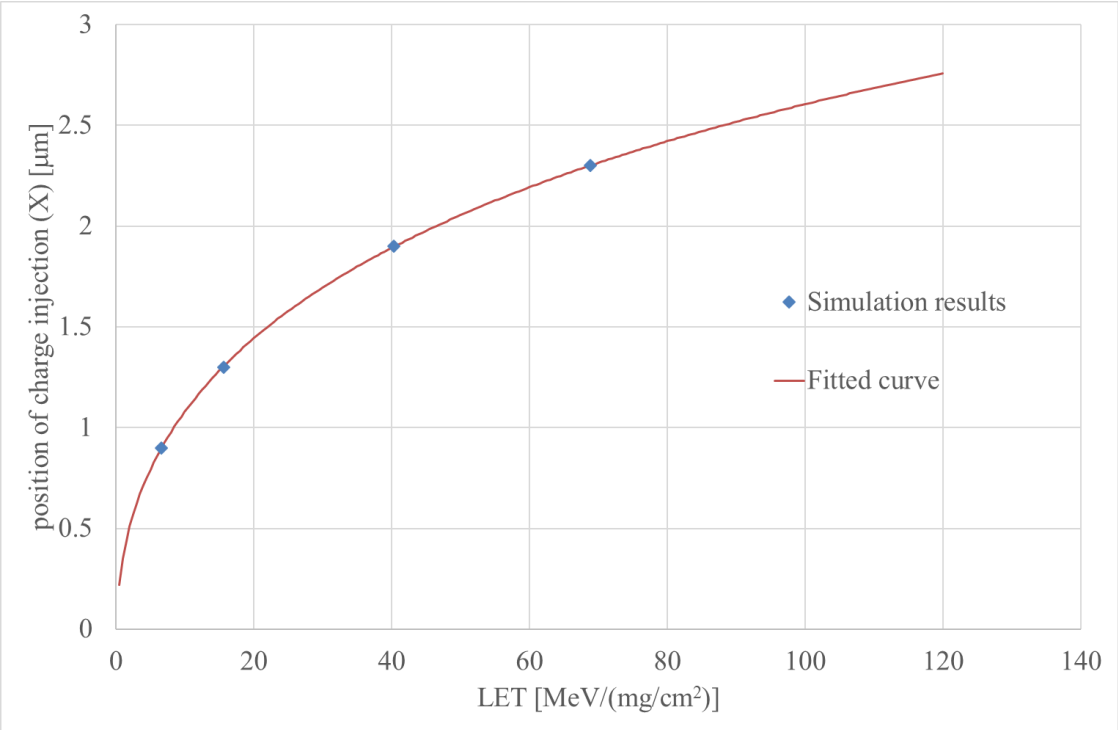


Fig. 4-14. The maximum distance between the position of charge injection and off-state transistor in various number of charge injection when SEU is observed.

4.5 Conclusion

In this chapter, device simulation model which purpose is simulate the SEU due to the charge sharing was indicated. HyDELEOS device simulator which are composed into the TCAD composite software HyENEXSS is convenient to the simulation of this purpose because this simulator has the function of charge behavior simulation based on the DD model, carrier mobility model and carrier generation/recombination model. Device simulation model which was created on the device simulator was indicated and it was confirmed that this model can simulate the behavior of injected charges and memory circuit function, simultaneously. Namely, it was indicated that this simulation model can simulate the SEU occurrence due to the charge sharing phenomenon. As a simulation result, it was identified that transistors which exist in the range of 2.3 μm from the center of charged particle incident had the potential to collect the enough charges to flip the electric potential of memory. In other words, SEU due to the charge sharing should be occurred in the case of transistors in the memory device are allocated within a radius of 2.3 μm circle. Validity of this simulation results are evaluated by comparing with the results of radiation irradiation test on chapter 5.

In addition, on the developed device-simulation-based method, charge sharing area can be estimated easily by changing total amount of injected charges when another kind of heavy ions are assumed. Also, this device-simulation-based method has a potential of extendibility to different types of memory circuits and memory circuit with different process size transistors by adapting the circuit structure model to device simulator. Regarding to this extendibility, further comparisons in various conditions of simulation results and experimental results are needed.

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3-7.
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Chapter 5:

Experimental Verification of the Device Simulation Model Validity

5.1 Introduction

Generally, when anyone want to know the radiation tolerant of semiconductor electronic device, irradiation tests of charged heavy ions are performed by using the facility with a large accelerator. Although the estimation method in this work can simulate the radiation tolerant without irradiation tests of charged heavy ions, experimental validation of validity of the simulation model of course should be performed by irradiation tests of charged heavy ions. Hence, a memory circuit test sample fabricated with 65 nm bulk CMOS process was prepared and performed to the irradiation test of a charged heavy ion. This test sample was fabricated with the same structure parameter as device simulation model, e.g. transistor gate length, gate oxide thickness, supply voltage etc. In this chapter, outline about the procedure of irradiation tests of charged heavy ions and test facility are explained at first. Then the procedure about the irradiation test of a charged heavy ion to memory circuit sample and test results are indicated. To the next, the result of validity evaluation by comparing the experimental result with the simulation result are indicated.

5.2 Outline about irradiation tests of charged heavy ions and test facility

There are two main purposes to perform the irradiation tests of charged heavy ions.

(1) Estimation of the probability of SEE occurrence in orbit.
(2) Identifying the radiation sensitive volume of electronic circuit.

In particular, electronic devices in the field of space must be evaluated the radiation tolerance of them because they are exposed to strong radiation in space. Therefore, there are many specification documents, handbooks and guidelines regarding to the irradiation tests of charged heavy ions[5-1), (5-2), (5-3)]. Procedures and preparations of irradiation tests of charged heavy ions are different depending on the types of electronic devices and the kinds of target single events. In this session, outline about the procedure and the preparations regarding to SEU test of the memory circuit experiment which was related to this work and outline about test facility were explained.

5.2.1 Outline of procedure and preparations of SEU test

Before performing the SEU test, relationship of charged heavy ion range and thickness between the interface and device layer of the test sample should be grasped. LET which is meaning of the energy loss during a charged heavy ion penetrates the unit length material is not constant in the route of charged heavy ion penetration. Fig. 5-1 indicate an example of the LET as a function of the silicon thickness. As shown in Fig. 5-1, plots of the relationship of LET and charged particle penetration lengths were drawn as the curve which was called “Bragg Curve”. LET become maximum just before stopping, this peak call “Bragg Peak”. Generally, sudden change of LET is the source of error for the irradiation test of charged heavy ion. Therefore, it is important that the thicknesses of each layer of test device should be grasped and charged heavy ion should be selected which has the characteristic of constant LET during the sensitive device layer in the route of charged heavy ion penetration. And, the range of charged heavy ion in the material can be calculated by using the Stopping and Range of Ions in Matter (SRIM) software[5-4)].

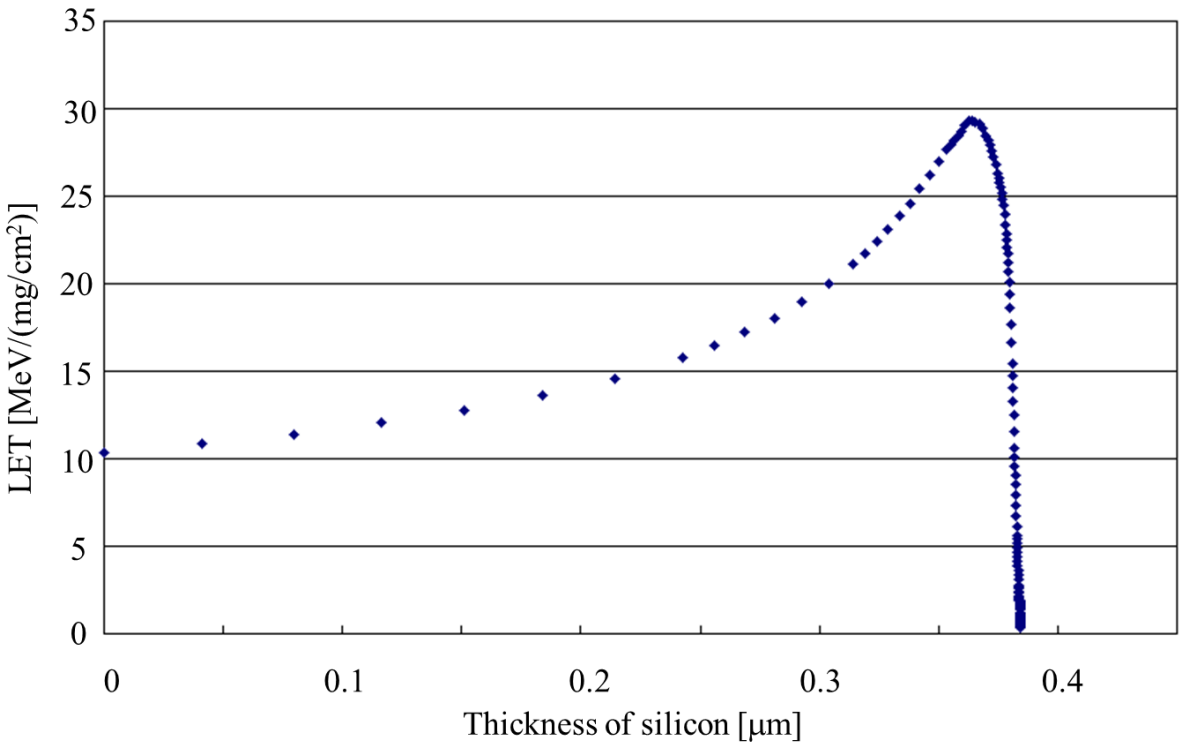


Fig. 5-1. An example of the LET depending on the silicon thickness.

For the purpose of grasping each layer thickness of test device, cross-sectional analysis of test device should be performed. An example of the cross-sectional analysis pictures is shown in Fig. 5-2. According to a result of cross-sectional analysis in Fig. 5-2, thickness between surface of silicon chip and transistor layer is 13.5 μm. As shown in the example of Fig. 5-2, there is the test device which has the passivation overcoating. In the case of the thickness between surface of silicon chip and transistor layer is too thick to compare with the range of charged heavy ion, the passivation overcoat can be removed by using solvent (e.g. fuming nitric acid etc.).

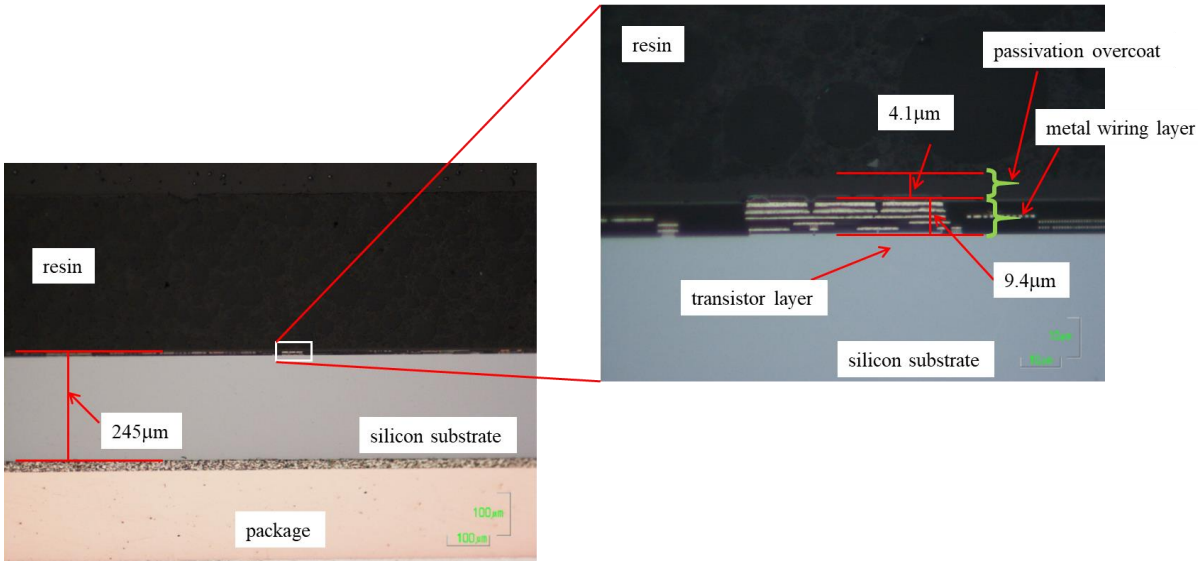


Fig. 5-2. An example of cross-sectional analysis pictures.

Range of charged heavy ion generated by accelerator is short in general. Therefore, the top of package of test electronic device should be removed physically or chemically. In the case of test electronic device package is made of plastic, silicon chip surface can be exposed by using solvent. In the case of test electronic device package is made of ceramic, silicon chip surface can be exposed by removing lid of package physically.

For the SEE test, test equipment and operation program need to be prepared according to a purpose. Test equipment and operation program of SEU test for the memory circuit which is the target of this work are simple relatively. Regarding to the SEU test for the memory circuit, static condition test is suitable. Operation program of static condition test writes “0” or “1” to all memory bit. And then charged heavy ions are irradiated, after that, the program reads the value of all memory bit and compares read values with the written values. As a result of comparison, the program judges SEU occurred in the memory bit which different between written value and read value, and the program logs the memory bit address and number of SEU. Note that, the memory bit address means the numbers assigned to each memory bit to identify the physical location of memory bit. Cross section of SEU sensitive volume in one bit memory cell is calculated by (5-1) formula. The operating flow of the program for SEU test is indicated in Fig. 5-3.

$$\sigma = \frac{N}{\Phi \times bit} \qquad (5-1)$$

σ: Cross section of SEU sensitive volume per one bit [cm^2/bit],
N: Number of SEU, Φ: Total fluence [particles/cm^2] (Total number of irradiated charged heavy ions per cm^2.), bit: Total number of bits in the test memory device

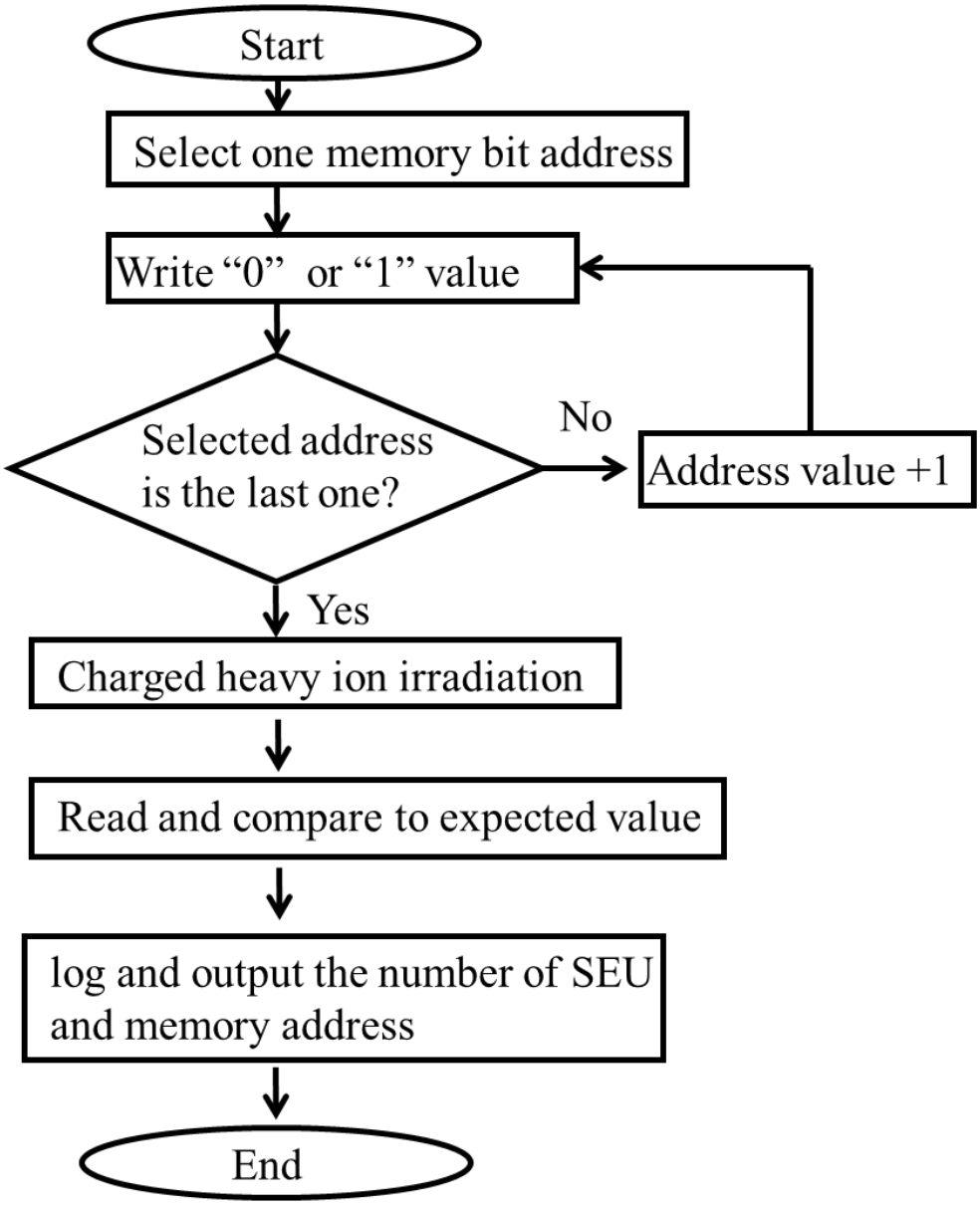


Fig. 5-3. The flow of program operation for the SEU test.

5.2.2 Outline about irradiation test facility of charged heavy ion

There are not many choices of the accelerator facilities which can provide charged heavy ions for the irradiation test, in domestic particularly. The reasons are that a large-scale accelerator and high cost for the maintenance are needed. The accelerator facility which is used in this work is Takasaki Ion Accelerators for Advanced Radiation Application (TIARA) facility in the National Institutes for Quantum and Radiological Science and Technology (QST). This facility has the ability of accelerate the cocktail ion beam. The cocktail ion beam which means multi ions are accelerated at the same time can be switch the kinds of irradiate charged heavy ions quickly, therefore, this facility is convenient for electronic device radiation test. The cocktail ion beam includes five kinds of charged heavy ions which characteristics are listed in Table 5-1.

Table 5-1 Characteristics of ions in the cocktail ion beam at TIARA facility

Ion Species	Energy [MeV]	LET [Mev/(mg/cm^2)]	Range in Si [μm]
N	53.2	3.4	49.2
Ne	69.7	6.6	39.0
Ar	137.0	15.8	36.1
Kr	289.0	40.3	37.3
Xe	394	68.8	34.6

JAXA have dedicated single event test vacuum chamber and ion beam line in TIARA. The appearance of the facility is shown in Fig. 5-4. Focused ion beam is transported from accelerator and collide Au scattering foil. Focused ion beam is scattered due to elastic collision with Au, and then ion beam is defocused to pipe size of ion beam line (5cm diameter).

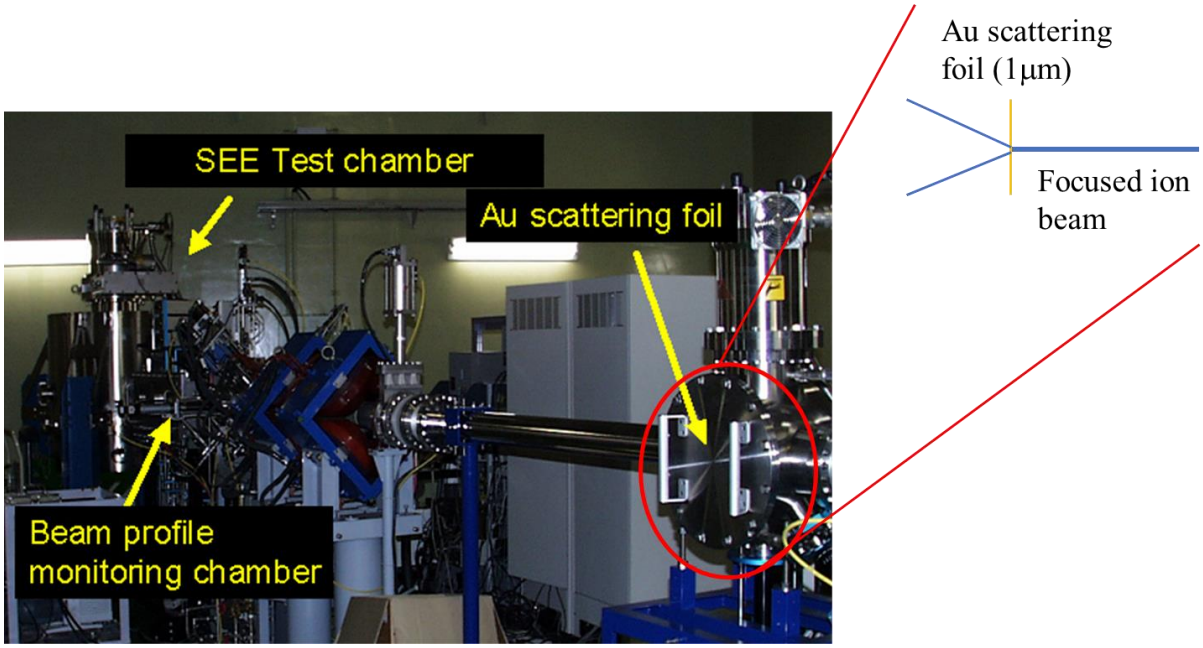


Fig. 5-4. The appearance of single event test chamber in TIARA.

Defocused ion beam is transported to the beam profile monitoring chamber and is measured its profiles, e.g. flux and uniformity in-plane. Fig. 5-5 shows the internal of the beam profile monitoring chamber. There are five scintillation counters and the each counter count the ion beam flux. Beam uniformity in-plane can be calculated by using the counts of each scintillation counter. For the purpose of obtain the constant flux in the charged heavy ion irradiation area, beam uniformity is adjusted over 90% by using the electromagnet which is in upstream of beam line. When the irradiation test of charged heavy ion is started, the center scintillation counter is moved to out of irradiation field by remote control. During the irradiation test of charged heavy ion, ion beam flux is monitored by four corner scintillation counters.

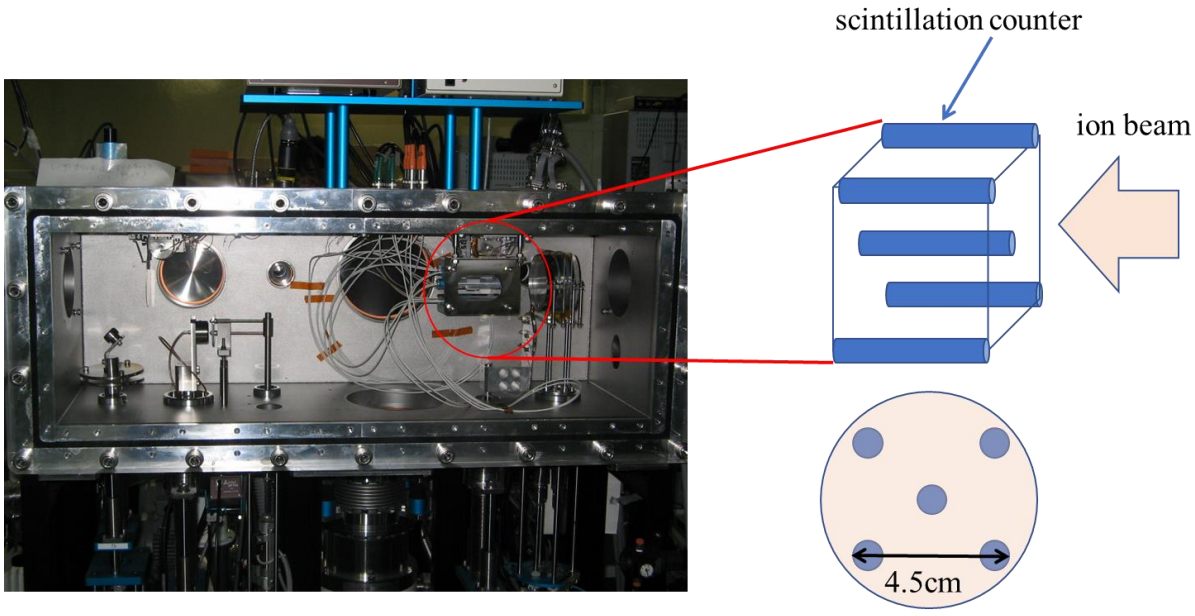


Fig. 5-5. The internal of the beam profile monitoring chamber.

After ion beam profile is measured in the beam profile monitoring chamber, charged heavy ions are transported to the SEE test chamber and irradiated to the device under test (DUT). The SEE test chamber has the four-axis goniometer stage, therefore, the irradiation test of charged heavy ion with optional angle can be performed by moving the DUT to optional angle. The internal of the SEE test chamber is shown in Fig. 5-6. Note that, irradiation test of charged heavy ion in TIARA is performed under vacuum conditions because the energy and range of charged heavy ion are decreased by atoms which are included in the air. For that reason, the SEE test chamber equips with the vacuum pumps.

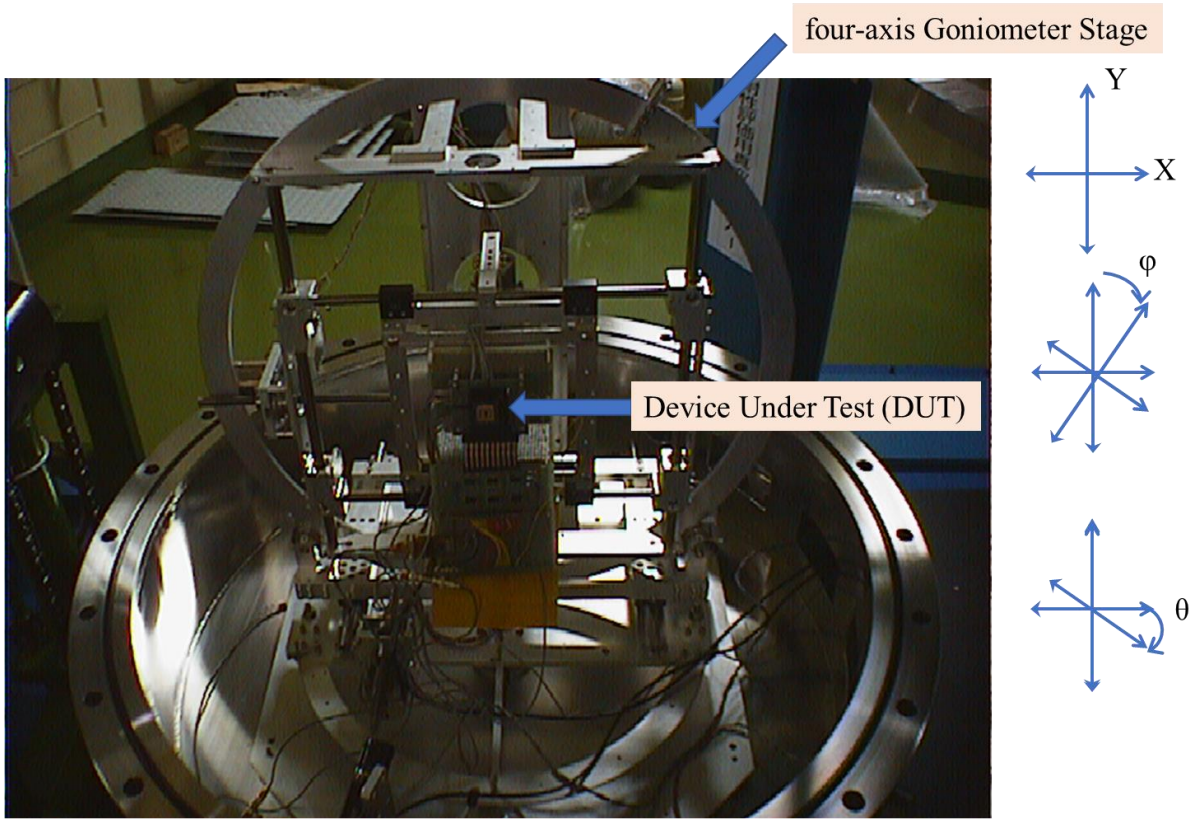


Fig. 5-6. The internal of the SEE test chamber.

5.3 Irradiation test of charged heavy ion

The irradiation test of charged heavy ion was performed for the purpose of validating the result of charge sharing device simulation in this work. The experiment conditions and experimental results are explained in this session.

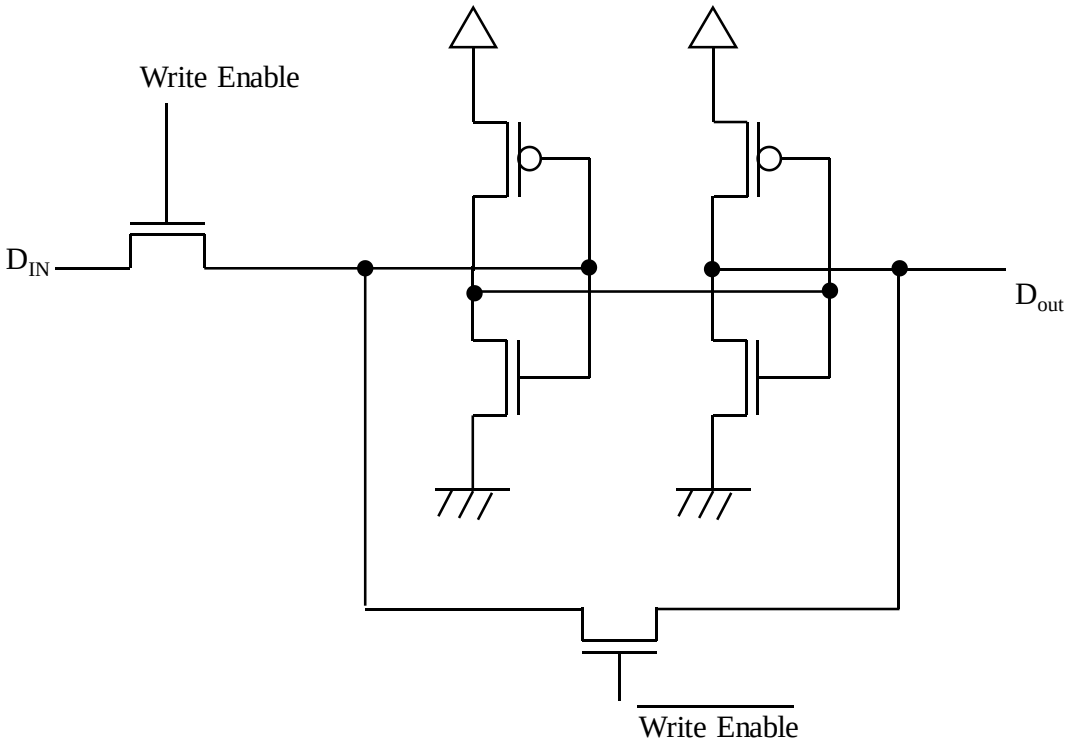
5.3.1 Test conditions of the ion irradiation test of charged heavy ion

The irradiation test of charged heavy ion for validation was performed by using TIARA facility. Test sample was fabricated with 65 nm bulk CMOS process of Taiwan Semiconductor Manufacturing Co., Ltd. (TSMC). Test sample includes 8 kbit simple latch memory standard cells is indicated in Fig. 5-7, so that the test results of this memory circuit can be used for validation because the structure is same as it of memory circuit of device simulation model. Test program of latch memory cells is followed to the flow of Fig. 5-3. Test conditions are shown below.

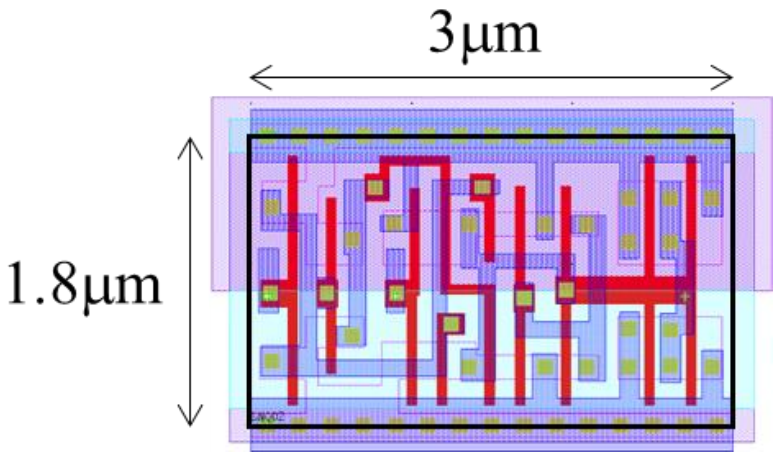
- Supply voltage: 0.9V (minimum)
- Test temperature: 25˚C (room temperature)
- Irradiated charged heavy ions: Xe (same as device simulation conditions)
- Total fluence: 1.0×10^6 [particles/cm^2]
- Flux: approximately 1.0×10^4 [particles/cm^2/sec]

SEU tends to be occurred easily in the case of lower supply voltage. Therefore, supply voltage was set to minimum condition as worst case

evaluation. Generally, total fluence is set to more than 1.0×10^7 [particles/cm^2] in SEU test because charged heavy ions need to be incident to almost all transistors to identify the sensitive volume. This fluence means that one charged heavy ion incident to every 0.1 μm^2. In this work, total fluence was set to 1.0×10^6 [particles/cm^2] for the purpose of identify the multi cell upset (MCU) due to the charge sharing phenomenon.



(a) Schematic diagram of latch memory.



(b) Layout of one-bit latch memory cell.

Fig. 5-7. The simple latch memory circuit in the test sample.

5.3.2 Test results of irradiation test of charged heavy ion

Test program of SEU test for the latch memory output the error number and error address information followed to the flow of Fig. 5-3. For the purpose of estimation for SEU due to the charge sharing phenomenon, the error address information was used. Error address can be converted to physical position of error latch memory cell. In this experiment, total fluence is set to 1.0×10^6 [particles/cm^2], therefore, probability of adjacent latch memory cells upset at the same time due to two charged heavy ions penetration is low. Namely, if there are the error addresses of two or more latch memory cells which are allocated adjacent, it can be identified MCU occurrence due to charge sharing phenomenon. Fig. 5-8 shows the error addresses log which was output by the test program. One address includes four bits of memory cells and 0 to F number is represented by these bits in hexadecimal. In this experiment, “1” value is written in all memory bits, therefore expected value to read is “F”. After charged heavy ions were irradiated, read values were compared with write values and error addresses and error bits were identified. Physical allocated positions of error bits were converted by using the combination of error addresses and error bits information. Physical error bits are mapped as shown in Fig. 5-9. There are eight blocks in all layout area and one block includes 1 kbit latch memory circuit. Enlarged error bits map of each memory block are also indicated in Fig. 5-10.

Address	Write value	Read value	Error bit
00E	F	E	1
026	F	B	4
034	F	7	8
04A	F	E	1
055	F	D	2
066	F	B	4
073	F	E	1
074	F	7	8
081	F	D	2
085	F	B	4
086	F	E	1
088	F	7	8
08A	F	D	2
08D	F	7	8
0B0	F	7	8
0B6	F	7	8
0E5	F	E	1
0E6	F	E	1
0E9	F	B	4
0EB	F	6	9
0EF	F	D	2
0F0	F	7	8
0F1	F	E	1
0F6	F	7	8
115	F	7	8
134	F	E	1
182	F	7	8
189	F	7	8
18F	F	D	2
1BE	F	A	5
1C2	F	7	8

Address	Write value	Read value	Error bit
1CB	F	B	4
1CF	F	D	2
1FE	F	A	5
20A	F	D	2
223	F	B	4
22B	F	D	2
235	F	E	1
238	F	E	1
23D	F	B	4
24A	F	D	2
24F	F	7	8
259	F	7	8
25F	F	D	2
263	F	B	4
278	F	E	1
279	F	B	4
287	F	B	4
2C7	F	B	4
2E6	F	D	2
303	F	7	8
309	F	7	8
30B	F	E	1
318	F	7	8
31C	F	7	8
330	F	E	1
34A	F	E	1
34D	F	7	8
358	F	7	8
370	F	D	2
384	F	7	8
396	F	D	2

Address	Write value	Read value	Error bit
39A	F	7	8
3D6	F	D	2
3DA	F	D	2
3EA	F	D	2
404	F	E	1
41D	F	B	4
421	F	E	1
422	F	7	8
424	F	D	2
42F	F	B	4
444	F	E	1
460	F	E	1
463	F	E	1
464	F	B	4
467	F	B	4
46C	F	D	2
46F	F	B	4
47D	F	B	4
48F	F	7	8
495	F	3	C
4CA	F	B	4
4CC	F	B	4
4D5	F	7	8
4DC	F	E	1
536	F	7	8
5AF	F	E	1
5C3	F	D	2
5D2	F	7	8
60C	F	E	1
612	F	E	1

Address	Write value	Read value	Error bit
641	F	B	4
65C	F	7	8
660	F	E	1
687	F	7	8
68E	F	7	8
696	F	E	1
6D6	F	E	1
6E3	F	D	2
6E7	F	E	1
6F0	F	B	4
70D	F	7	8
74D	F	7	8
74E	F	B	4
76E	F	D	2
793	F	E	1
7C0	F	B	4
7C7	F	D	2
7CF	F	E	1
7D3	F	E	1
7DA	F	7	8
7D3	F	E	1
7DA	F	7	8

Fig. 5-8. The error addresses log which was output by the test program.

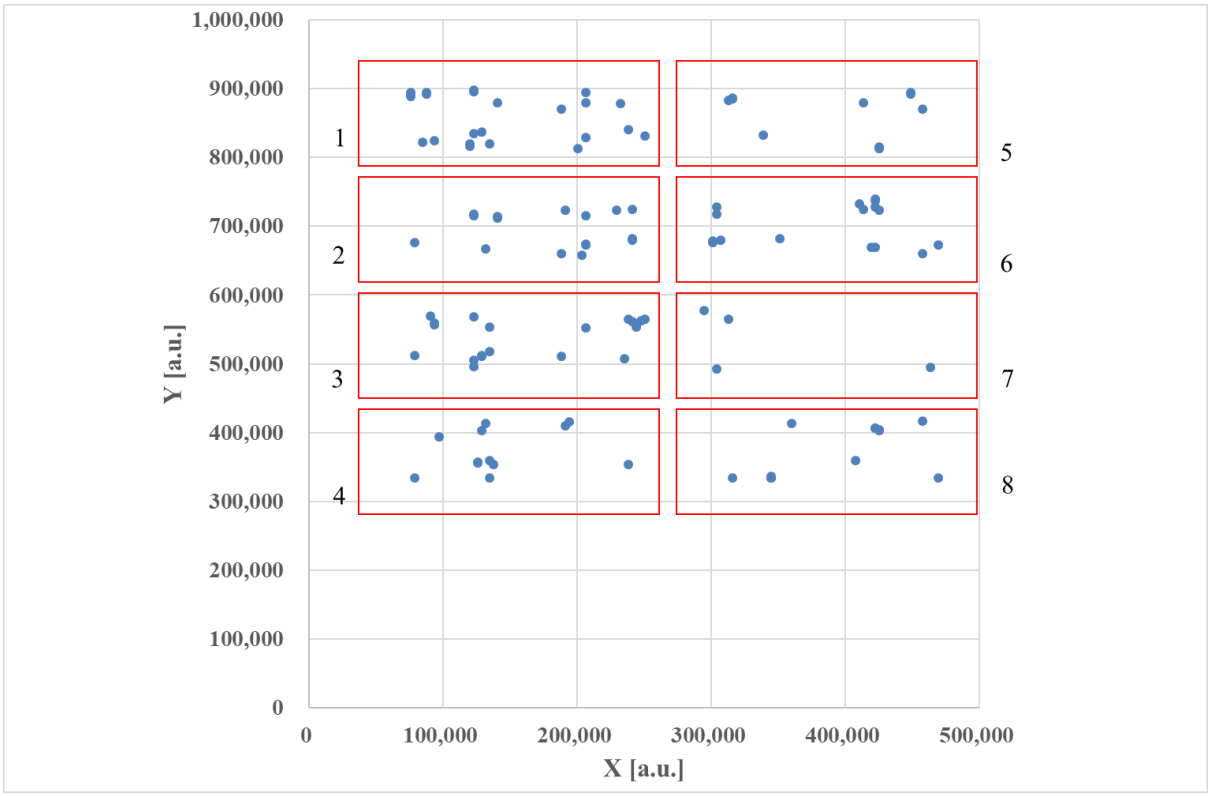
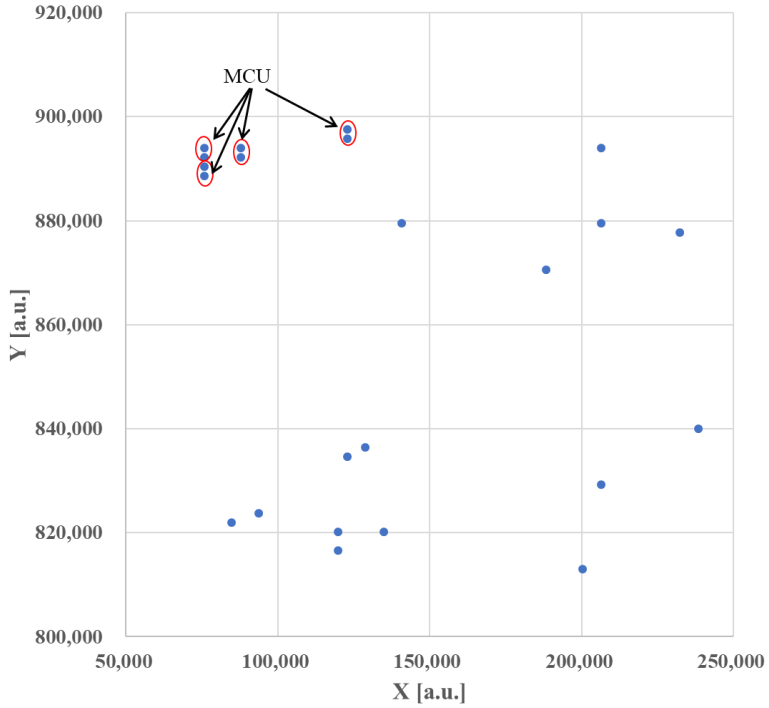
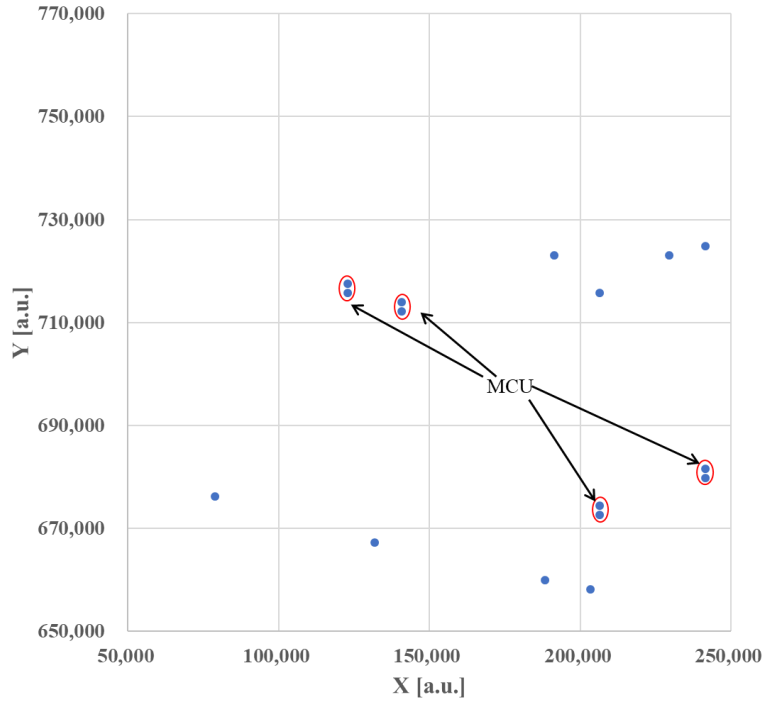


Fig. 5-9. Physical error bits map of the 8 kbit latch memory.

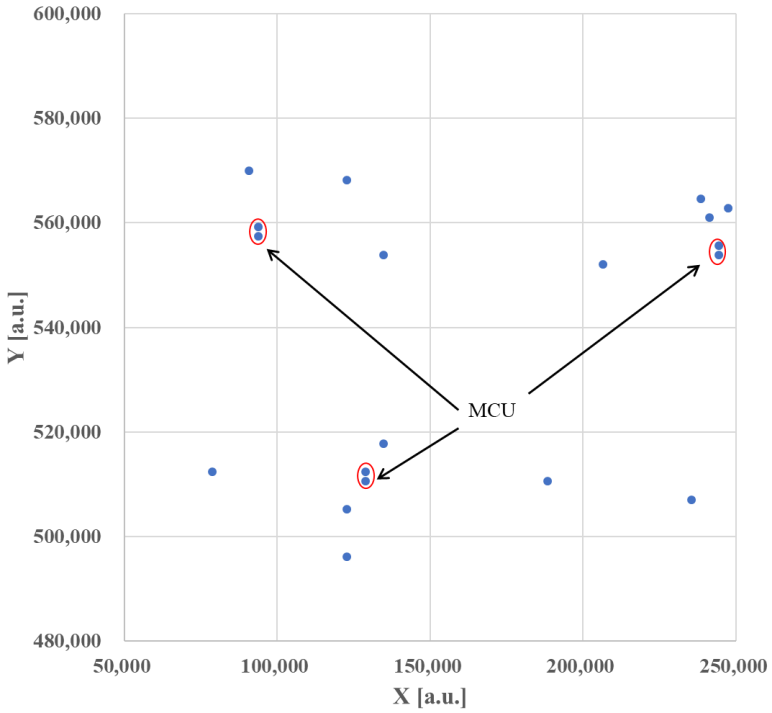


(a) Enlarged physical error bits map of block number 1.

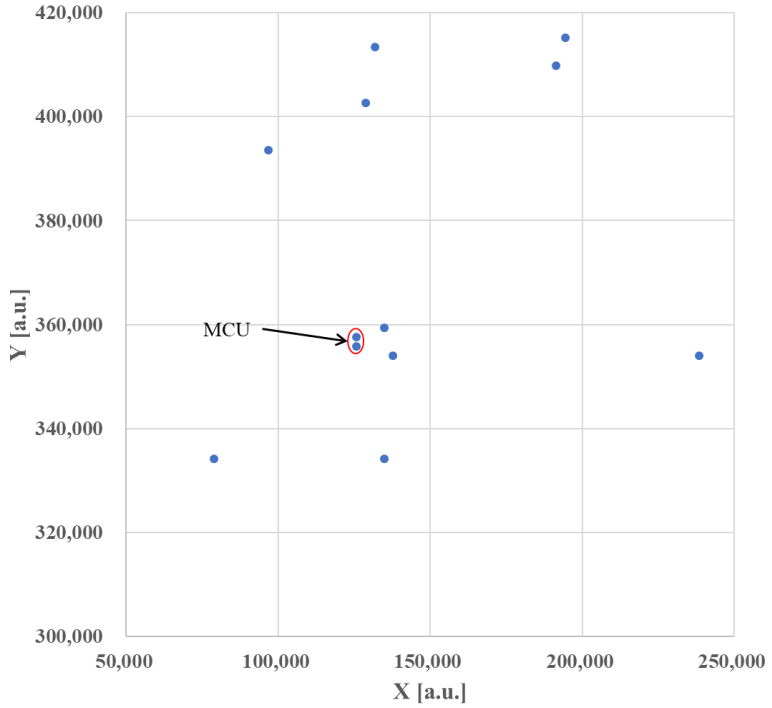


(b) Enlarged physical error bits map of block number 2.

Fig. 5-10. Enlarged Physical error bits map.

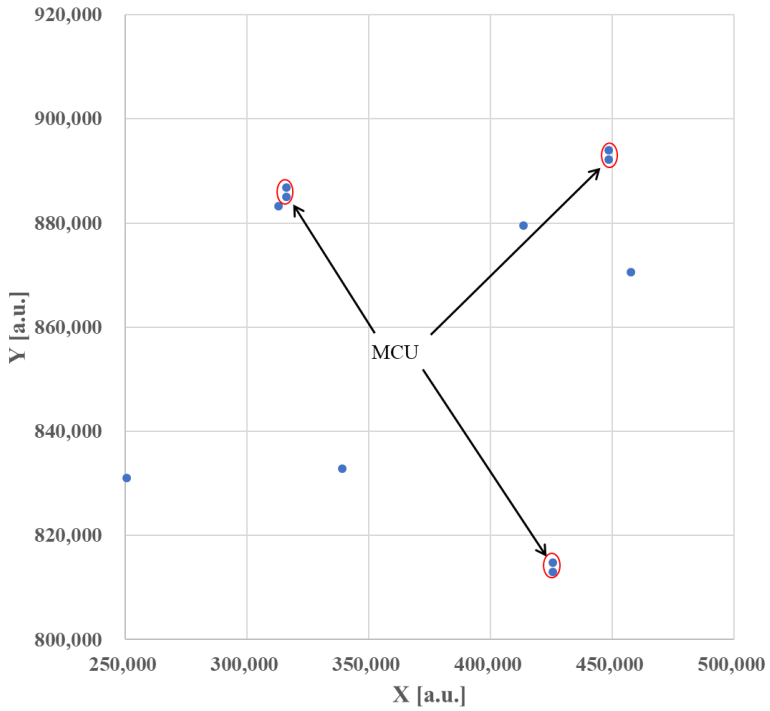


(c) Enlarged physical error bits map of block number 3.

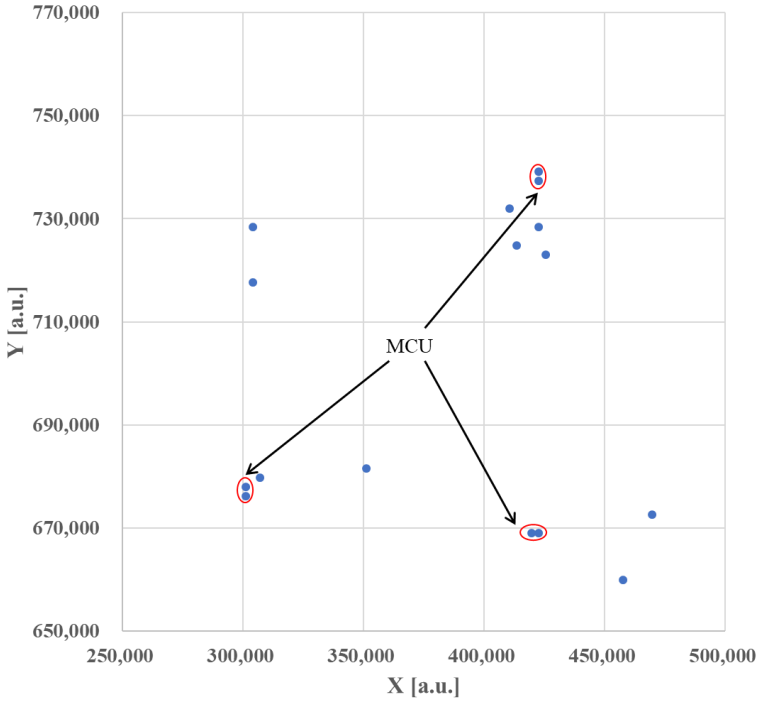


(d) Enlarged physical error bits map of block number 4.

Fig. 5-10. Enlarged Physical error bits map.

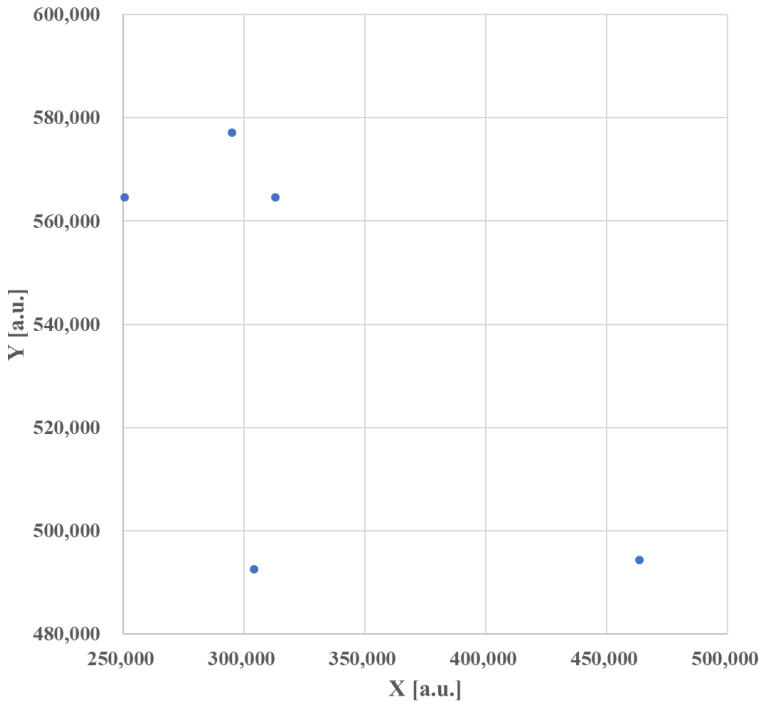


(e) Enlarged physical error bits map of block number 5.

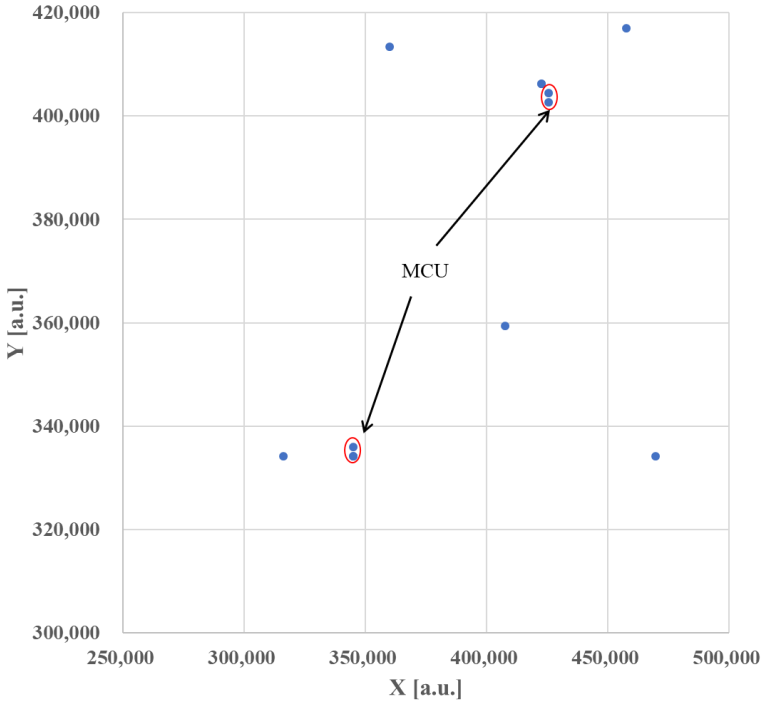


(f) Enlarged physical error bits map of block number 6.

Fig. 5-10. Enlarged Physical error bits map.



(g) Enlarged physical error bits map of block number 7.



(h) Enlarged physical error bits map of block number 8.

Fig. 5-10. Enlarged Physical error bits map.

In Fig. 10 (a) to (h), MCUs are represented by red circle. As a result of physical mapping, maximum number of bits included in one MCU is two. Note that, although there is four bits vertical string in Fig. 10 (a), this is considered to be a combination of two MCUs. Because, one reason is lateral neighbor latch memory bits are allocated with same distance as vertical one. The other reason is charged heavy ion incident vector is vertical to the chip surface. Therefore, it can be determined that the four bits vertical string is a combination of two MCUs. According to the mapping result, maximum number of bits included in one MCU is two. And the layout area of one latch memory bit is 1.8 μm × 3.0 μm as shown in Fig. 5-7 (b). Therefore, charge sharing affected area can be estimated as less than 10.8 μm^2 (3.6 × 3.0 μm or 1.8 × 6.0 μm), as shown in the image of Fig. 5-11.

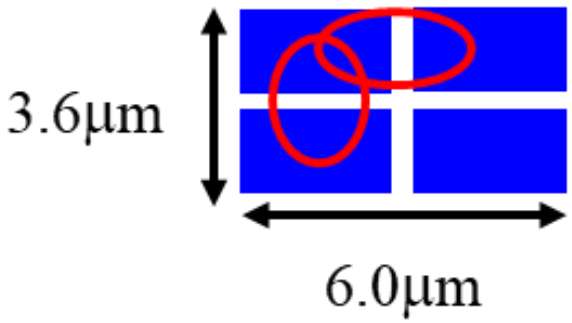
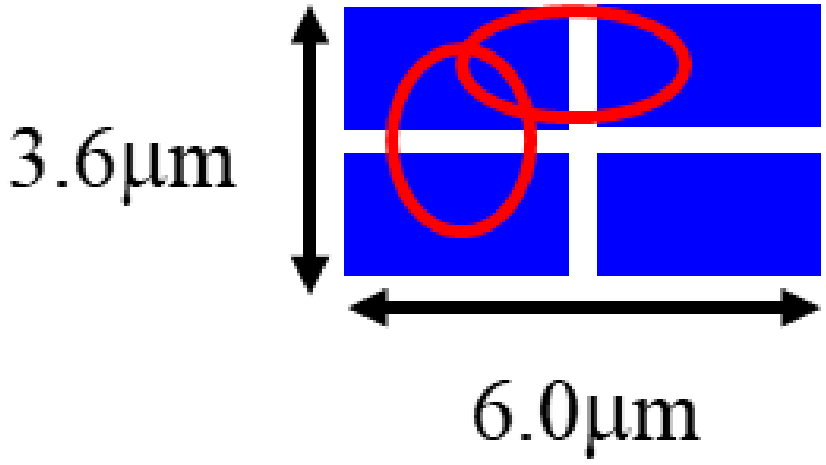


Fig. 5-11. A conceptual diagram of estimated charge sharing affected area.

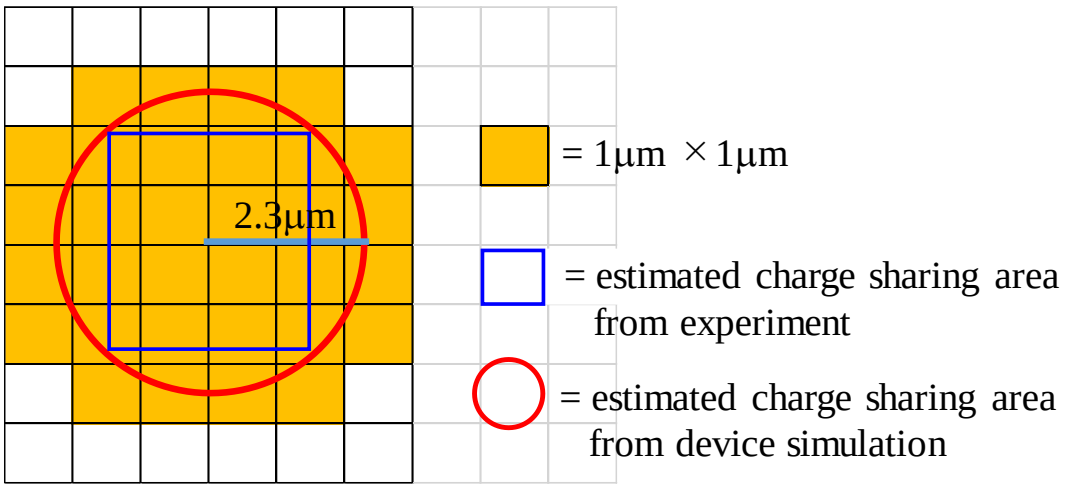
5.4 Validity verification of device simulation result

5.4.1 Comparison of device simulation result and charged heavy ion irradiation test result

According to the analysis result from irradiation test of charged heavy ion, charge sharing affected area can be estimated less than 10.8 μm^2 in the case of this tested sample. On the other hands, according to the device simulation results which were indicated in chapter 4, transistors which exist in the range of 2.3 μm from the center of charged particle incident have the potential to collect the enough charges to flip the electric potential of the memory circuit. Namely, charge sharing affected area can be estimated as 16.6 μm^2 which means the area of 2.3 μm radius circle. Comparison of estimated charge sharing area from irradiation test of charged heavy ion and from device simulation are shown in Fig. 5-12. The charge sharing area estimated from experiment result is indicated as blue square and the charge sharing area estimated from device simulation result is indicated as red circle in Fig. 5-12 (b). According to the comparison between the estimation results from experiment and it from device simulation, although there is a little difference, it can be confirmed that approximately consistent result is obtained.



(a) The estimated charge sharing area from the experiment.

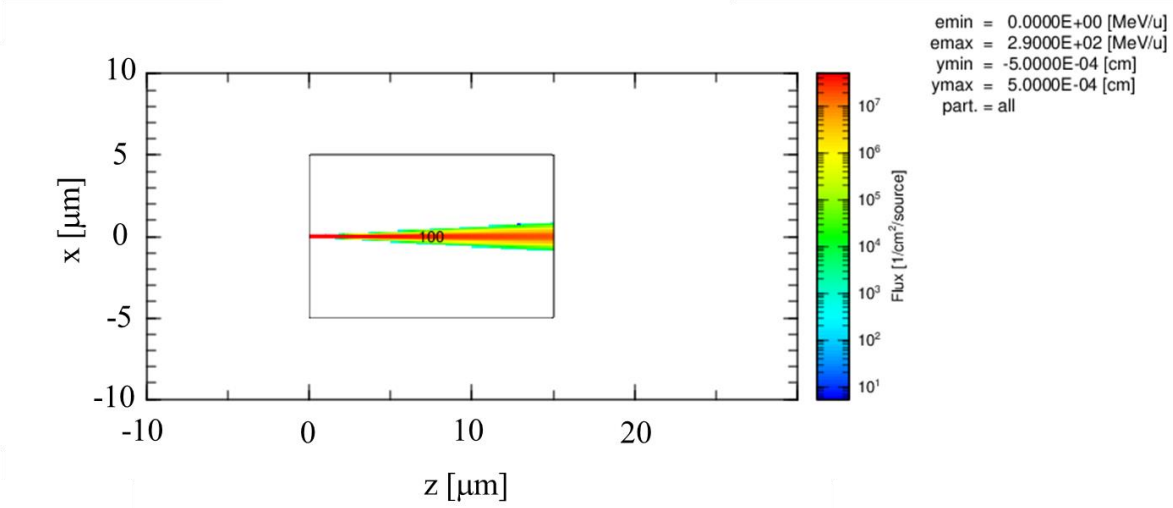


(b) The estimated charge sharing area from the device simulation.

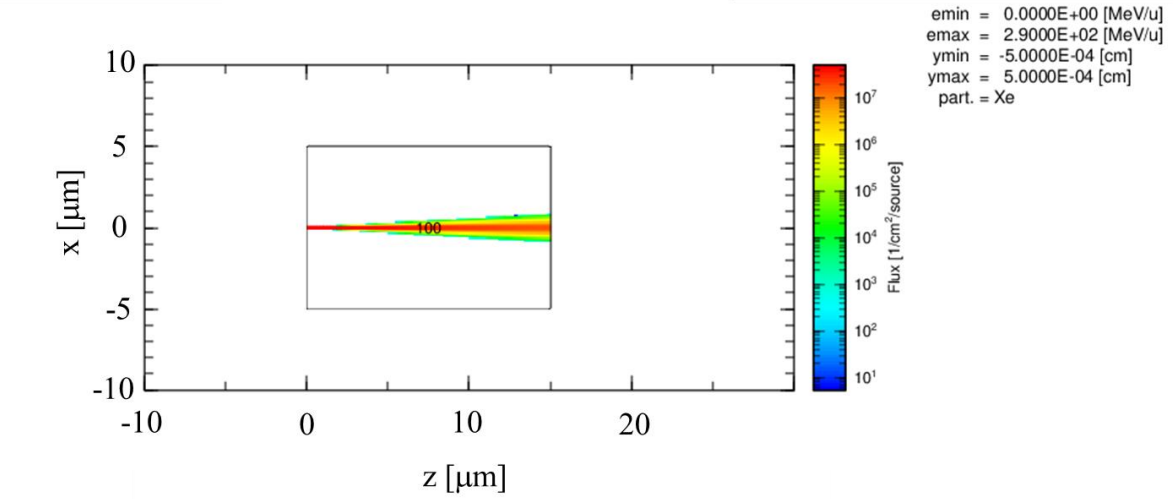
Fig. 5-12. The comparison of estimated charge sharing area from charged heavy ion irradiation test and from device simulation.

5.4.2 Impact of nuclear reaction for the error between simulation result and experimental result

There is 5.8 μm^2 differ between the estimation result of charge sharing affected area from experiment and it from device simulation. It is assumed that one of the reasons for this difference is the nuclear reaction. Although device simulation did not include effects of nuclear reaction, elastic scattering and silicon recoils might be occurred due to the collision of charged heavy ions and silicon atoms in actual irradiation test. To validate the effect of nuclear reaction for the error between simulation result and experimental result, Particle and Heavy Ion Transport code System (PHITS) simulator[5-5] which based on the Monte Carlo simulation method was used. This simulator has a function of simulating the transportation of charged heavy ions and a function of simulating the generation of the primary knock on atoms (PKA), secondary protons and secondary neutrons etc. from nuclear reaction. The simulation was performed with the condition of Xe heavy ions accelerated with 3.4 MeV/u energy transported to the 10 μm × 10 μm × 15 μm Si rectangular. The accelerated energy was set to same as the energy of Xe heavy ion which used to the experiment in TIARA facility. The total number of transported Xe ions in PHITS simulation was set to 1×10^6 particles. This is also same as the total number of Xe ions which were irradiated test sample in TIARA facility. Simulation result is shown in Fig. 5-13.

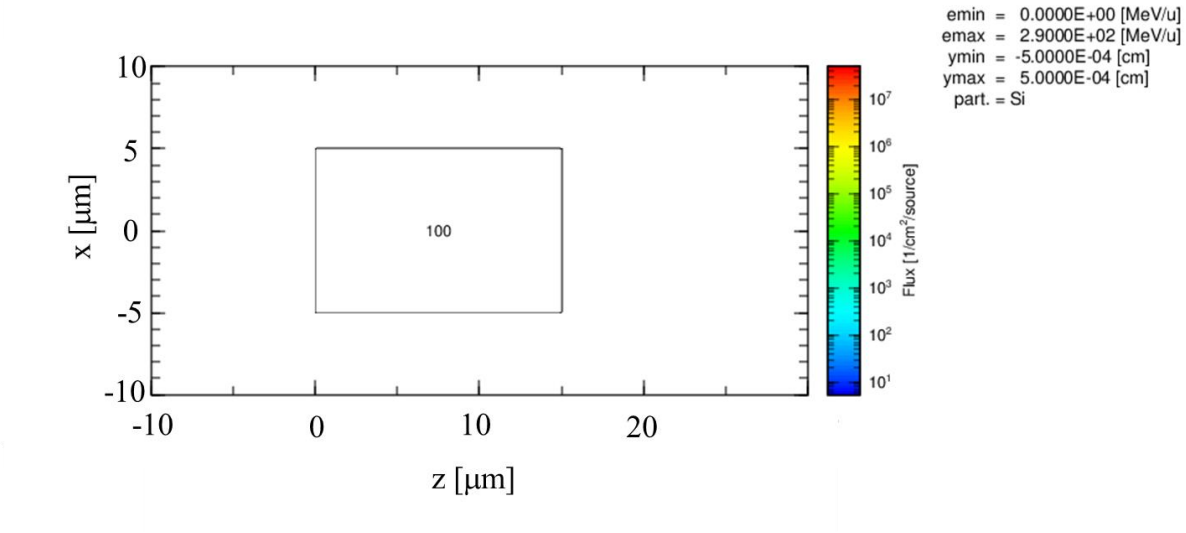


(a) The trajectory of all ions in Xe ion transportation simulation.

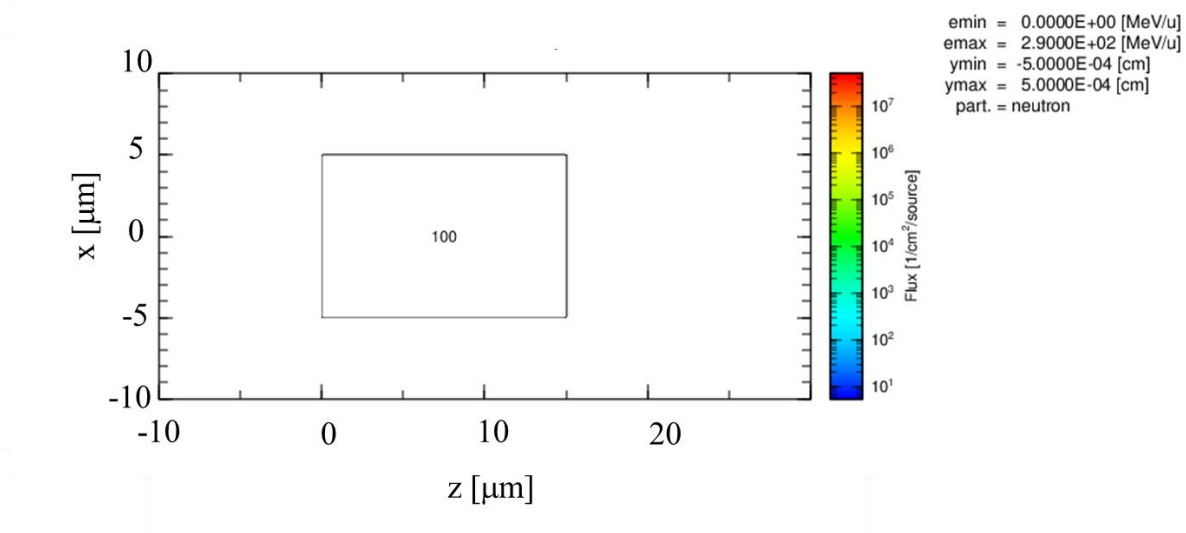


(b) The trajectory of Xe ions in Xe ions transportation simulation.

Fig. 5-13. The track of Xe ions transportation from PHITS simulation.

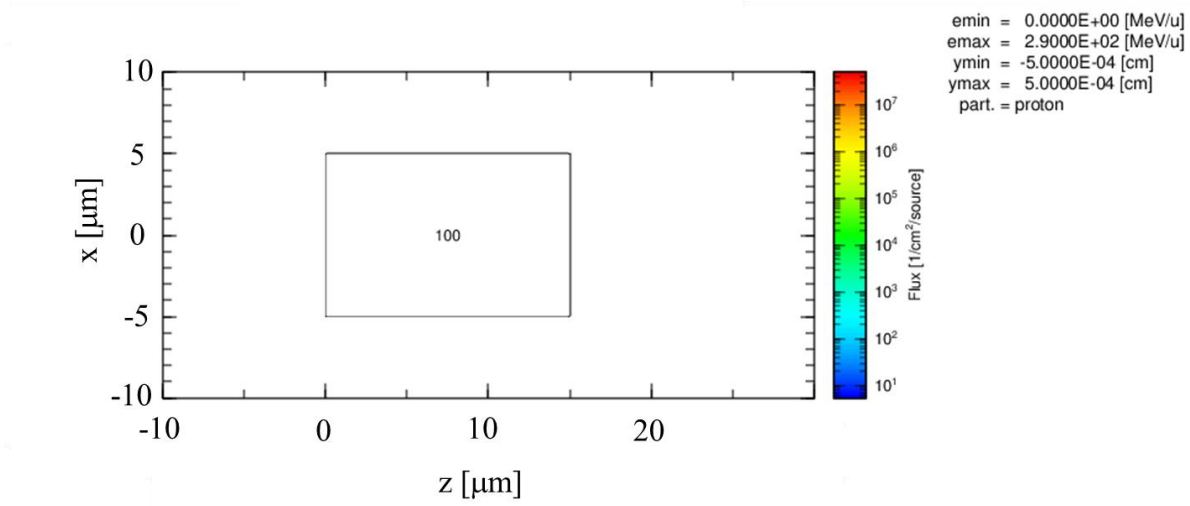


(c) The trajectory of Si ions as PKA in Xe ions transportation simulation.



(d) The trajectory of secondary neutrons in Xe ions transportation simulation.

Fig. 5-13. The track of Xe ions transportation from PHITS simulation.



(e) The trajectory of secondary protons in Xe ions transportation simulation.

Fig. 5-13. The track of Xe ions transportation from PHITS simulation.

Simulation results indicate that secondary particles and Si particles as PKA were not generated in this simulation condition. This is because accelerate energy of Xe ions was not enough to generate the secondary particles and PKA. Namely, it is assumed that the secondary particles and PKA were not generated in this total number of Xe ion transportation conditions due to low probability of secondary particles and PKA generation. Therefore, it is assumed that secondary particles and PKA were not generated in actual irradiation test of charged heavy ion in TIARA facility. As shown in Fig. 5-13 (b) trajectory of Xe ions become a little wide near the right side boundary of simulation area. Although a Xe atom is much heavier than a Si atom, it is assumed that a part of trajectory of Xe ion made curve due to elastic scattering. This elastic scattering has the potential to induce the error between simulation result and experimental result, but it is assumed that the impact is limited because transistors of memory circuit cannot collect

charges generated in deep position of substrate[5-6].

5.4.3 Consideration of other elements which have the potential of impact for the error between simulation result and experimental result

In addition to the reason of estimated charge sharing area error explained in session 5.4.2, it is assumed that causes of the error are the reasons explained in next. First of all, memory circuit type was different between the device simulation and the experiment, strictly speaking. Device simulation model in this work was simple SRAM type memory circuit. On the other hands, test sample which was performed irradiation test of charged heavy ion was latch type memory circuit. Although there is only the little different between the schematic diagram of each memory circuit, it is assumed that there are differences about parasitic element, electric field conditions around the transistor and critical charge Q_c. And the transistor model of device simulation included many assumes. Strictly speaking, it is assumed that concentration of impurity in the substrate, well and diffusion layer was different, and its distribution was also different to the real device. These differences have an impact to the threshold voltage of transistor, and therefore it leads to the difference of Q_c of memory circuit. The error between estimated charge sharing area from experiment and from device simulation was led from combination of the reasons above. It should be noted that, in the case of device simulation model which is more similar as the circuit in the experimented sample is used, it has been confirmed that more realistic result was obtained[5-7]. However, device simulation which using such a complex structure needs long time for calculation. There is a trade-off between precision and simulation time.

5.5 Conclusion

In this chapter, experiment of charged heavy ion irradiation for the latch memory and the validity evaluation of device simulation results was indicated. The irradiation test of charged heavy ion was performed by using Xe ions in TIARA facility. Addresses information of SEU error observed memory cell which were output by test program, and layout area information of one-bit memory cell were used to identify the MCUs. According to the results of the irradiation test of charged heavy ion, maximum number of bits which were included in one MCU were two. The layout area of one-bit memory cell is 1.8 μm × 3.0 μm, therefore, it was identified that the charge sharing area from the irradiation test of charged heavy ion was 10.8 μm^2 (3.6 × 3.0 μm or 1.8 × 6.0 μm). On the other hands, the charge sharing area estimated from device simulation result was 16.6 μm^2. Although there is a little error between the both of estimated charged sharing area due to nuclear reactions or due to many assumes included in device simulation, it could be confirmed that approximately consistent result was obtained.

References

(5-1) ECSS Basic Specification No. 25100, Single Event Effects Test Method and Guidelines

(5-2) ASTM F 1192, Standard Guide for the Measurement of Single Event Phenomena (SEP) Induced by Heavy Ion Irradiation of Semiconductor Devices

(5-3) EIA/JESD57, Test Procedures for Measurement of Single-Event Effects in Semiconductor Devices from Heavy Ion Irradiation

(5-4) The Stopping and Range of Ions in Matter (SRIM) http://www.srim.org

(5-5) K. Niita, N. Matsuda, Y. Iwamoto, H. Iwase, T. Sato, H. Nakashima, Y. Sakamoto, and L. Sihver, PHITS: Particle and Heavy Ion Transport Code System, Version 2.23, JAEA-Data/Code 2010-022 2010. [Online]. Available: http://phits.jaea.go.jp/index.html

(5-6) Amusan, Oluwole A., et al. "Charge collection and charge sharing in a 130 nm CMOS technology." IEEE Transactions on nuclear science 53.6 (2006): 3253-3258.

(5-7) Akifumi Maru, Akifumi Matsuda, Satoshi Kuboyama and Mamoru Yoshimoto, “Simulation-Based Understanding of "Charge-Sharing Phenomenon" induced by Heavy-Ion incident on a 65nm Bulk CMOS Memory Circuit”, The Institute of Electronics, Information and Communication Engineers (IEICE) Transaction on Electronics, Vol.E105-C, No.1, Jan. 2022 (in press)

Chapter 6:

Suggestion of Charge Sharing Tolerant Memory Circuit Based on the Device Simulation Result

6.1 Introduction

According to the results of chapter 4 and 5, estimation method of charge sharing phenomenon by using the device simulation was indicated and was validated its validity. It is a very big advantage that charge sharing phenomenon can be approximately estimated in advance without the irradiation test of charged heavy ion. Because the irradiation test of charged heavy ion needs so high cost and time, e.g. cost of test device fabrication or cost of accelerator machine time. In addition, one of the big advantages of this method is to create more options for charge sharing induced single event upset tolerant circuit. For example, this method convenient for designing of memories which are applied error correction code (ECC) algorithm[(6-1), (6-2)] and memories composed with redundancy circuit. In this chapter, some examples of charge sharing tolerant memory circuit based on the device simulation results are indicated.

6.2 Charge sharing tolerant memory circuit

Generally, memorized data in the memory cells are read from multi memory cells at one time and read values are treated as “Word” which means a strings of “0” or “1” value. Memory cells which compose to one word are not need to be allocated in order as shown in Fig. 6-1. An example of read “Word” in the memory circuit is shown in Fig. 6-2. The example is one of most simple ECC algorithm. When one-Word data is read, a parity bit is read at the same time. In the case of Fig. 6-2, the parity bit indicates the total number of “1” data which is included in one-Word is odd number or even number. Namely, if one-bit value included in Word is wrong due to SEU, parity bit value is contradictory with the Word value. Operating system detects such contradictions and invalidate these read results. The advantage of this algorithm is recovering the one-bit error without any additional countermeasure circuit to the memory cell itself. However, this algorithm cannot detect the error in Word in the case of there are over two error bits.

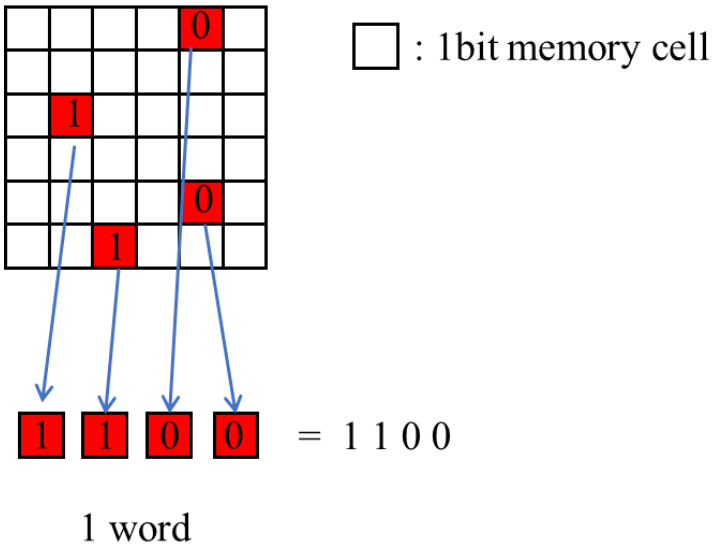


Fig. 6-1. An example of read “Word” in the memory circuit.

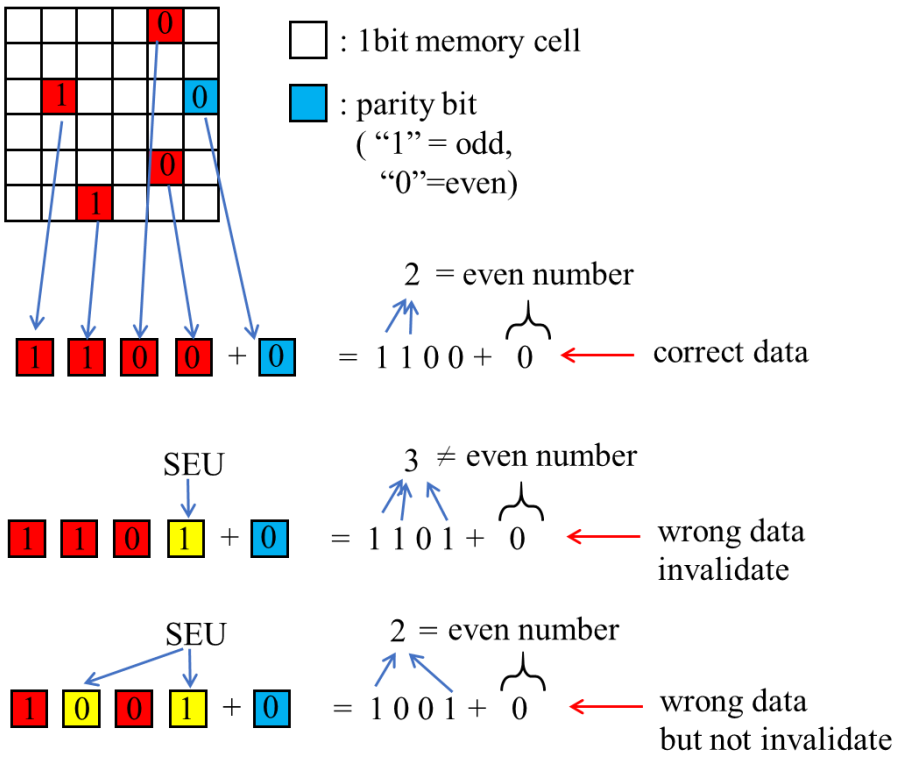


Fig. 6-2. An example of simple ECC algorithm.

As shown in Fig. 6-2, this ECC algorithm tolerates only one error included in one-Word when memorized data is read. Other most of ECC algorithm also cannot tolerate multi errors included in one-Word. As explained in chapter 3, multi cell upset due to charge sharing phenomenon becomes a serious problem in recent years. Because distance between neighbor transistors becomes narrow and critical charge Qc becomes small due to high integration and transistor size decreasing. In such a high integrated memory circuit, ECC algorithm as the countermeasure of SEU does not have enough effect due to charge sharing phenomenon. A solution of this issue is very simple. Just separating with certain distance each memory bit cells which compose one Word and a parity bit. To decide the distance between each memory bit cell, the simulation method which is provided in this work is very useful. According to the estimation result from charge sharing simulation, the affected area of charge sharing is in the circle of 2.3 μm radius. Therefore, each memory bit cells should be separated with 2.3 μm distance as shown in Fig. 6-3. Since space between these memory bit cells can be filled with memory bit cell which compose to other Words, there is almost no area penalty. There is the penalty of time related to re-read operation or rollback operation when SEU is detected.

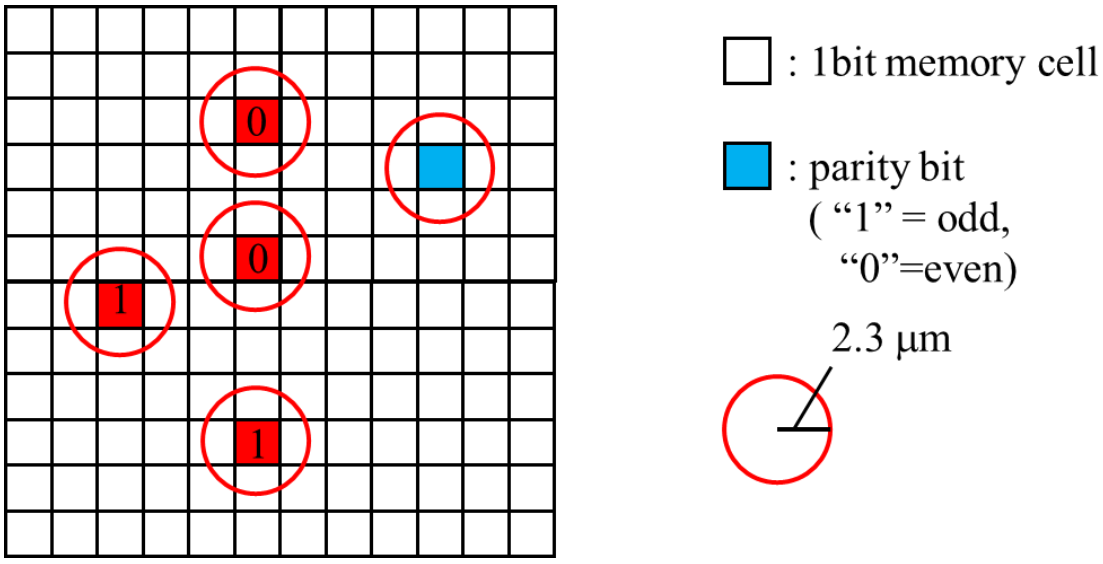


Fig. 6-3. A charge sharing tolerant memory layout.

This layout technique by using the results of the device simulation also can be used for redundancy memory circuits. For example, triple modular redundancy circuit (TMR)[6-3] is composed with three memories and one majority circuit. In the case of this circuit, three memories should be separated with appropriate distance each other to avoid SEU in more than two memories. Although this type of technique has the area penalty, there is no penalty regarding to time related to re-read operation because read data do not need to be invalidated due to majority circuit function.

Cautionary points of ECC and TMR techniques for SEU error are data refresh rate. SEU induced error memory bit cells can be detected only after these memory bits reading. Namely, a total number of SEU induced error memory bit cells are increased continuously due to many radiation penetrations, in actual orbit, and eventually, more than two error bits are inserted to one-Word or to TMR circuit. Memory circuit which applied to ECC or TMR techniques with a charge sharing estimation method should be used like a cache memory which is the kind of high frequent read and refresh memory.

Penalty of layout area to avoid the charge sharing phenomenon can be canceled when the wide band gap semiconductor materials other than Si are used to the substrate. This is because the total amount of generated charges decreases when charged heavy ions incident to the substrate of wide band gap semiconductor materials. Fig. 6-4 indicates radiation ionization energy as a function of the band gap width of semiconductor materials. As shown in Fig. 6-4, according to the study of Claude A. Klein, radiation energy which need to generate one electron-hole pair depends on the band gap energy of semiconductor materials[6-4]. For example, in the case of SiC material, generated charges due to charged heavy ion incident decrease approximately half comparing with Si material substrate. Also, in the case of substrate of diamond material, generated charges decrease one approximately fifth

comparing with Si material substrate.

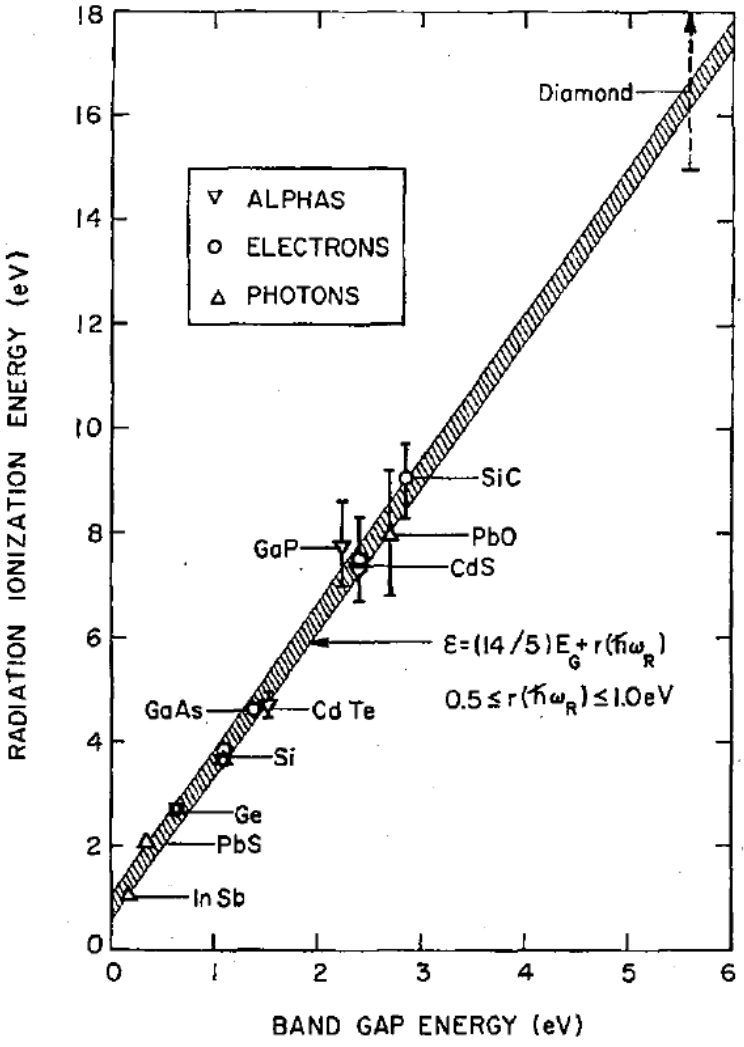


Fig. 6-4. Radiation ionization energy as a function of the band gap width of semiconductor materials[6-4].

6.3 Conclusion

In this chapter, memory circuits based on ECC and TMR techniques were suggested as an example of composing the charge sharing tolerant memory circuit by using the estimation method in this work. To prevent that more than two SEU induced error memory bit cells are existing in one-Word or TMR memory circuit, this device-simulation-based method is very convenient to decide the distance between memory bit cells each other. In addition, there is an advantage that significantly high cost for fabricating the test sample or for radiation irradiation test itself is not need due to this method is simulation base. The radiation tolerant memories can be composed by applying these countermeasure techniques and using this memory to high frequent read or refresh memory such a cache memory. The area penalty to avoid charge sharing phenomenon can be canceled by applying the substrate of wide band gap semiconductor materials.

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Chapter 7:

General Conclusion

Electronic devices for space application are demanded to have radiation tolerance because there is so strong radiation environment in orbit comparing with the ground environment. In recent years, due to the demands for high integration and high performance of electronic devices, radiation tolerance of electronic devices become more serious. The reasons are that the distance between transistors each other becomes narrow and the critical charge Q_c becomes small in such high integrated electronic devices. Charge sharing phenomenon is significantly serious problem in such high integrated memory devices because conventional countermeasures for the radiation have not enough effect to this phenomenon. In this thesis, the estimation method for charge sharing phenomenon by using the device simulator HyDeLEOS was proposed and its efficiency and validity had been validated. The objectives of the present work are classified in the following two items;

1. Establishment of the estimation method for charge sharing phenomenon by using the device simulator.
2. Suggestion of charge sharing tolerant memory logic circuit based on the above simulation method.

In chapter 3, mechanisms of radiation effects on the semiconductor material devices were explained. The lattice displace ment damage and the ionizing effect are the two main radiation effects on semiconductor material devices. And the mechanism of charge sharing phenomenon which is related to the ionizing effect and impacts to the SEU tolerance of memory circuit was also explained.

In chapter 4, the calculation schemes and the procedure of device simulator HyDeLEOS were indicated. The device simulation model which is composed with simple SRAM type memory circuit for the estimation of charge sharing phenomenon was composed on HyDeLEOS simulator and

the results of device simulation were indicated. This simulation model can simulate the injected charge drift-diffusion which simulates charge sharing and memorized value flip which simulates SEU, simultaneously. According to the device simulation results, the affected area of the charge sharing was estimated within the 2.3 μm radius circle.

Validity of device simulation model has been validated by comparing with the result of the irradiation test of charged heavy ion result in chapter 5. Test memory circuit sample was fabricated with 65 nm bulk CMOS process which was same transistor process size of device simulation model and the irradiation test of charged heavy ion was performed with it. The irradiation test conditions of charged heavy ion were set to almost same as device simulation conditions. By using the output of the error bits addresses from the test program, the affected area of the charge sharing was estimated as the area of two times of one memory bit cell layout area (1.8 μm × 3.0 μm × 2). On the other hands, the estimated charge sharing area from the result of the device simulation was 16.6 μm^2. Although there is the error between the both of estimated charged sharing areas due to nuclear reactions or due to many assumes included in the device simulation, it could be confirmed that approximately consistent result was obtained.

In chapter 6, the memory circuits based on ECC and TMR techniques were suggested as examples of composing the charge sharing tolerant memory circuits by using the estimation method in this work. Charge sharing tolerant can add to ECC technique by separating memory bit cells included in one-Word each other with appropriate distance which is decided by the estimation method of charge sharing affected area in this work. Also, redundancy circuit like a TMR circuit can be added charge sharing tolerant by separating memory bit cells which connected to majority circuit each other with appropriate distance. Charge sharing tolerant memory circuit can be composed as high frequent read and refresh memory device by applying the

combination of these techniques and the estimation method of the device-simulation-based charge sharing affected area. The area penalty to avoid charge sharing phenomena can be canceled by applying the substrate of wide band gap semiconductor materials.

Therefore, in this thesis, the validity of the device-simulation-based estimation method for charge sharing phenomenon has been validated and charge sharing tolerant memory circuit based on this estimation method has been indicated. In future work, the upgrade of the estimation method will be planned with the addition of the function regarding to radiation penetration with angle.

List of Publications

1. Original articles for this thesis

≪Chapter 5≫

1) **Akifumi Maru**, Hiroyuki. Shindou, Tsukasa. Ebihaara, Akiko. Makihara, Toshio. Hirao, Satoshi. Kuboyama, “DICE based Flip-Flop with SET Pulse Discriminator on a 90 nm bulk CMOS process”, IEEE Trans. Nucl. Sci., Vol. 57, No.6, 3602-3608 (2010).
2) **Akifumi Maru**, Hiroyuki. Shindou, Koichi Suzuki, “Preliminary Evaluation of the 6 MV Tandem Accelerator at The University of Tsukuba for Single Event Testing”, Transactions of the Japan Society for aeronautical and Space Sciences, Aerospace Technology Japan, Vol. 16, Issue 2, pp. 161-164 (2018)

≪Chapter 4 and 5≫

3) **Akifumi Maru**, Akifumi Matsuda, Satoshi Kuboyama and Mamoru Yoshimoto, “Simulation-Based Understanding of "Charge-Sharing Phenomenon" induced by Heavy-Ion incident on a 65nm Bulk CMOS Memory Circuit”, The Institute of Electronics, Information and Communication Engineers (IEICE) Transaction on Electronics, Vol.E105-C, No.1, Jan. 2022 (in press)

Other related articles

1) Satoshi Kuboyama, **Akifumi Maru**, Naomi Ikeda, Toshio Hirao, Takashi Tamura, “Characterization of Microdose Damage Caused by Single

Heavy Ion Observed in Trench Type Power MOSFETs", IEEE Trans. Nucl. Sci., Vol. 57, No.6, 3257-3261 (2010).

2) Satoshi Kuboyama, **Akifumi Maru**, Hiroyuki Shindou, Naomi Ikeda, Toshio Hirao, Hiroshi Abe, Takashi Tamura, "Single-Event Damages Caused by Heavy Ions observed in AlGaN/GaN HEMTs", IEEE Trans. Nucl. Sci., Vol. 58, No.6, 2734-2738 (2011).

3) Akiko Makihara, Tamotsu Yokose, Yoshihisa Tsuchiya, Yoshio Miyazaki, Hiroshi Abe, Hiroyuki Shindou, Tsukasa Ebihara, **Akifumi Maru**, Koichi Morikawa, Satoshi Kuboyama, Takashi Tamura, "Applicability of redundant pairs of SOI transistors for analog circuits and their applications to phase-locked loop circuits" IEEE Trans. Nucl. Sci., Vol. 60, No.1, 230-235 (2013).

2. Presentation list

1) **A. Maru**, H. Shindou, T. Ebihaara, A. Makihara, T. Hirao, S. Kuboyama, "DICE based Flip-Flop with SET Pulse Discriminator on a 90 nm bulk CMOS process", Nuclear and Space Radiation Effects Conference (NSREC), 2009.

2) **Akifumi Maru**, Akifumi Matsuda, and Mamoru Yoshimoto "A Study of Single Event Mitigation Techniques for Nano-Scale Semiconductor Devices", The 65th JSAP Spring Meeting, 2018.

3) **Akifumi Maru**, Akifumi Matsuda, and Mamoru Yoshimoto "A Study on Single Event Mitigation Techniques for Nano-Scale Semiconductor Devices (2)", The 79th JSAP Autumn Meeting, 2018.

4) **Akifumi Maru**, Hiroyuki Shindou, and Koichi Suzuki "Preliminary Evaluation of 6 MV Tandem Accelerator in Tsukuba University for Single Event Testing", 31st ISTS, 26th ISSFD & 8th NSAT in Matsuyama, Ehime, (2017).

5) **Akifumi Maru**, Hiroyuki Shindou, and Koichi Suzuki “Scandalization activity of single event test methods for electronic devices for space use.” [Translated from Japanese.], The 29th REAJ Autumn Symposium, 2016.

3. Award

1) Award for excellence, Reliability Engineering Association of Japan, 2016

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