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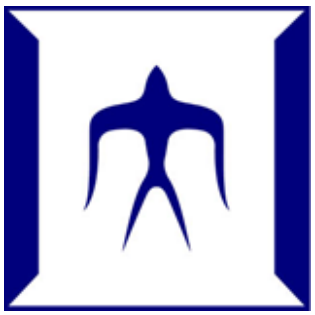

A Study of 300GHz-Band CMOS Phased-Array Transceiver System for High Data Rate Wireless Communication

by

Ibrahim Imad Ibrahim Abdo

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in the

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of

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To my family,

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Abstract

This dissertation presents a study of 300GHz-band CMOS transceiver and phased-array systems that are based on subharmonic mixing. 300GHz-band is one of the main candidates for the next generation of wireless communication systems (6G). This thesis covers the design details of the transceiver RF front-end including the mixers, LO chain components, and the PCB implementation for the phased-array system. Using the CMOS process to build 300GHz-band transceivers is an attractive option considering the low cost and the compatibility with the digital integrated circuits. However, the main obstacle resides in the low maximum oscillation frequency ($f_{\max}$) of the CMOS transistors which barely exceeds 300GHz for small transistor sizes. As a result, the implementation of reliable power amplifiers (PAs) and low noise amplifiers (LNAs) is quite difficult and still not demonstrated well in the literature. Most of the recent works eliminate the RF amplifiers and adopt the mixer-last transmitter (TX), mixer-first receiver (RX) architecture instead. The design using the mentioned architecture is still challenging considering that the linearity and noise requirements of the mixers are very critical. In addition, the free space path loss of the 300GHz-band is approximately 20dB higher than the loss of the currently popular 5G bands around 30GHz, making it more difficult to achieve the required signal-to-noise-ratio (SNR) for a long-distance high-data-rate wireless link. Overcoming the SNR degradation may cause a drastic increase in the area and the power consumption, so careful design and implementation techniques are necessary. Two 300GHz-band transceiver systems are discussed in this thesis; a low-power transceiver with a single-mixing-path, and a phased-array transceiver with output power improvement and image rejection techniques. The low-power transceiver utilizes a subharmonic mixer with novel circuit techniques to provide suitable system performance and to meet the link budget requirements. The subharmonic mixer is chosen in this work to reduce the LO frequency and the design complexity. Other parts such as the LO chain components are also designed using special circuit techniques to reduce the overall power consumption. The transceiver proposed in this thesis achieves a 34Gb/s maximum data rate over a 1cm distance while consuming 0.41W from a 1V supply. Compound semiconductor (InP) PAs and LNAs are added to the system to study the "hybrid-transceiver" option, and as a result, the max-

imum data rate is improved to 56Gb/s with higher order modulations such as 64QAM becoming usable as well. The phased-array transceiver utilizes the subharmonic mixer with a bi-directional architecture. The TX mode is based on the outphasing technique to improve the average output power, and the RX mode adopts the Hartley architecture to cancel any undesired image signals. Thanks to the bi-directional operation, the TX and the RX share the antenna, and that makes it easier to implement a phased-array due to the small chip size. The measured beam range of the implemented array is from -18° to 18°. The maximum data rate of the TX mode is 52Gb/s and the maximum data rate of the RX mode is 36Gb/s. Apart from the systems mentioned above, the thesis also explores frequency multiplication techniques at mm-wave frequencies due to their critical role in sub-THz systems in general. The introduced systems are implemented in 65nm CMOS technology and the effectiveness of the proposed techniques was verified in clean-room and over-the-air measurements.

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Chapter 1

Introduction

We have been experiencing a massive evolution of the wireless communication technologies in the last 20 years due to the exponential growth of data consumption worldwide [1]. Every year, the communication technologies are becoming a more essential part of our lives as social media, e-commerce, live-streaming, and video download applications are seeing a rapid growth in the recent years. Being connected became much more vital after the global spread of COVID-19 as remote education and work was the only way to keep productive during quarantine. The start of 5G infrastructure deployment in the last couple of years is another sign that we are entering a new era of communications where being connected all the time is the norm. Mainly, Frequencies below 6GHz were used for communication systems due to the small path-loss and the relatively low-loss implementation options. However, these frequencies are crowded with many applications and the achievable data rate is quite limited. The 5G regulated by the 3rd Generation Partnership Project (3GPP) utilizes higher frequencies in the millimeter wave (mm-wave) bands to provide higher data rate links at the expense of shorter communication range. Phased-arrays are also essential for the operation of the 5G transceivers to overcome the increase of the path-loss. 5G systems are expected to reach data rates as high as 10Gb/s with low latency. Furthermore, 5G is targeted to be a technology that supports future industry and society, for use cases demanding particular requirements and high performance. The 5G technology will be set to a constant evolution in the next years to deal with the wide range of applications. In the recent years, a lot of efforts were made to implement high performance millimeter-wave transceivers for 5G and for the 60GHz standards as well [2–6].

Ten years from now, the next generation of wireless communications, which is going to be potentially called “6G”, is anticipated to be introduced. After achieving many use cases and solutions for social issues by 5G, the fusion of several use cases and the needs

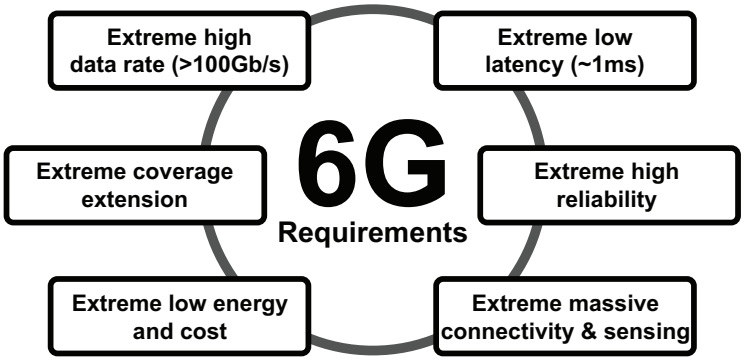


Figure 1.1: 6G technology requirements.

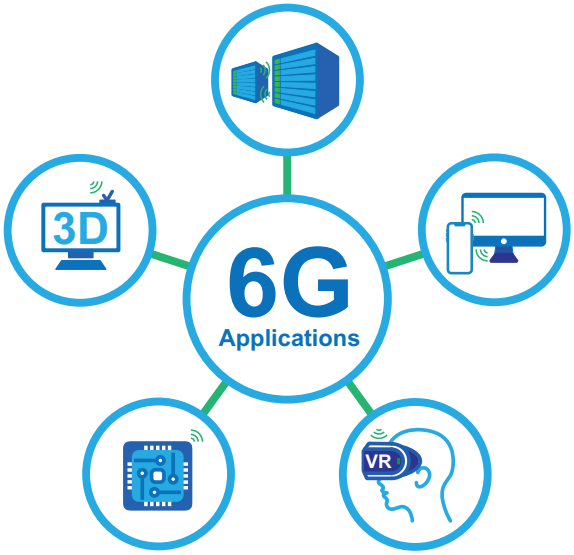


Figure 1.2: 6G technology possible applications

for new use cases will appear. However, the combination of requirements of the new use cases cannot be covered by the 5G performance. Fig.1.1 shows the requirements that will be aimed for in the 6G technology [7]. More diverse and new requirements that are not fulfilled by the 5G and its evolution are considered with new use cases expected to appear after the deployment of 5G. Extremely higher data rates (>100Gb/s), low latency, wide coverage, low cost and energy, high reliability, and massive connectivity are the main requirements considered in the current vision for 6G.

Some of the applications that represent new use cases for 6G are shown in Fig.1.2. Using extremely high data rate wireless communication can provide solutions to the current bottlenecks [8]. In addition, light field and holographic displays demand hundreds of Gb/s communication speeds that cannot be satisfied by the 5G technology [9]. Uncom-

pressed video streaming and massive sensor networks are also among the applications that are still out of reach for the current technologies.

One of the driving factors of the emerging of 6G is that the 5G millimeter-wave frequency bands (e.g. 28GHz and 39GHz) do not have enough bandwidth to accommodate the speed and capacity requirements of the 6G use cases. Hence, higher frequency bands are being considered, especially in the sub-THz (0.1-1THz) region. High data rates were demonstrated using transceivers operating around 100GHz [10–15], but the lack of standardization and the existing regulations and applications make it difficult to realize the same data rates when actual deployment is considered. On the other hand, one of the most appealing candidates to be utilized in 6G is the 300GHz-band which roughly covers the frequencies from 250GHz to 320GHz. The 300GHz-band has three main characteristics that make it a very desirable choice for some 6G applications: (i) the available bandwidth is very wide with much less crowdedness compared to the lower frequency bands, (ii) electronic devices can still operate at this band with acceptable performance compared to the higher frequencies, and finally (iii) the short wavelength at 300GHz-band which enables miniature antenna implementation with an order of several hundred μm. The 300GHz phased-array technology that is introduced in the following chapters is expected to be one of the key enabling technologies for 6G as it makes it possible to satisfy the data rate and latency requirements. Other 6G enabling technologies also include non-Terrestrial Networks for wide coverage, wireless power transfer for low energy solutions and massive connectivity, and new network topologies.

In this thesis, the design of a future 6G 300GHz-band wireless transceiver system is studied. Leveraging the advantages of the 300GHz-band requires special design considerations to overcome its big challenges such as the high path loss (around 20dB more than the 5G bands), the high component losses, the limited performance of the main system components, and other challenges that will be mentioned later in this thesis.

1.1 Standards and Regulations for 300GHz-band

As the 300GHz-band is starting to attract attention recently, efforts have been made to standardize this band. The Institute of Electrical and Electronics Engineers (IEEE) introduced IEEE Std. 802.15.3d–2017 which is an amendment of the IEEE Std. 802.15.3d–2016 to define a wireless PHY layer that operates at 100Gb/s [16]. The standard covers the frequencies between 252.72GHz and 321.84GHz. 69 channels with 8 supported bandwidths from 2.16GHz and up to 69.12GHz which is quite massive and should easily fulfill the requirements of 6G new use cases. The standard channels are shown in Fig.1.3.

According to the decisions at the World Radio Conference 2019 (WRC-2019), the

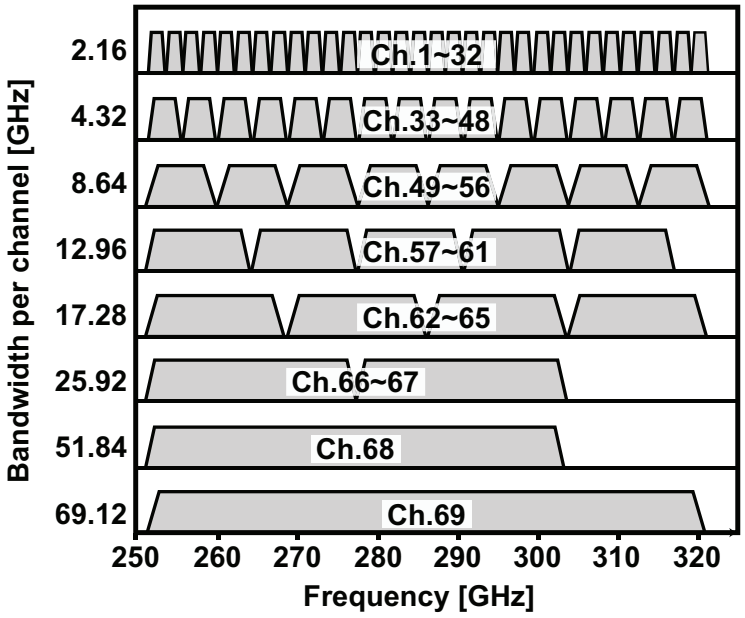


Figure 1.3: IEEE Std. 802.15.3 channel plan.

mentioned standard bands can be used for THz communications, but the radio astronomy and satellite services must be protected [17]. The bands 275-296GHz, 306-313GHz, 318-333GHz, and 356-450GHz have no specific conditions to protect Earth exploration and satellite service applications [18, 19], so a very wide bandwidth is still available to use without potential interference concerns.

The standards and regulations of the 300GHz-band may keep getting updated in the coming years based on the interference analysis and the new challenges to appear before the deployment.

1.2 300GHz-band CMOS Transceivers

Many works have utilized the 300GHz-band to achieve high data rates up to 120Gb/s using compound semiconductors or SiGe as in [20–33]. The high $f_{\max}$ makes it possible to design power amplifiers (PA) and low noise amplifiers (LNA) with high gain and good linearity resulting in an excellent EVM performance. However, the compound semiconductor process-based systems are costly, very difficult to integrate, and large-scale digital circuits are not feasible in most cases, reducing the system's overall feasibility. The CMOS process is still more desirable as the main system process due to its low cost, excellent area efficiency, and high integration ability. Implementing the whole transceiver system using CMOS process means that both the RF front-end, the A/D and D/A inter-

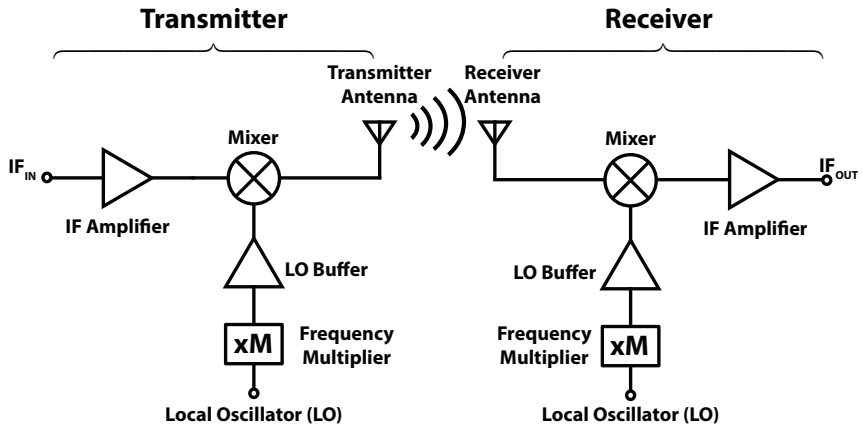


Figure 1.4: Generic architecture for the 300GHz-band transceiver.

faces, the control/calibration circuits, and the processing circuits can be all integrated on one chip. System-on-chip (SoC) which is very common in mobile devices can also be realized by the full-CMOS implementation. However, there are many design difficulties that must be faced to make the operation of the transceiver acceptable. One large drawback of the CMOS process is its low $f_{\max}$ which does not normally exceed 300GHz. As a result, the RF-side amplifiers (PA and LNA) are not feasible so far, causing the dominance of the mixer-last (frequency-converter-last) TX, mixer-first RX architecture in the recent works [34–47]. For transceiver systems with amplifiers, lower frequencies were used as in [10, 48–50]. The mixer-last TX mixer-first RX architecture suffers from the limited linearity, high noise figure, and LOFT radiation from both the TX and the RX (LO emission). Fig.1.4 shows the general architecture of a heterodyne 300GHz-band mixer-last TX mixer-first RX transceiver. Besides the challenging mixer design, the LO generation circuit design is also very critical considering the very high operation frequency. The CMOS-based transceivers usually utilize LO frequencies in the D-band (110–170GHz) to realize LO buffering with decent driving power to be applied to the mixer. Several up-conversion steps and/or subharmonic mixing are the main techniques used to reduce the LO frequency. Consequently, frequency multiplier design in the D-band is very crucial to achieve the required performance of the LO chain. Additionally, circuit-level and architecture-level novel techniques are essential for the wireless link to be realized.

1.3 Overview of This Thesis

The main aim of this thesis is to study the 300GHz-band transceiver implemented using CMOS process and to develop techniques for achieving wireless communication while

keeping the power consumption to an acceptable value. PCB implementation for simple transceivers and phased-array transceivers is also considered.

This thesis is organized as follows: Chapter 2 introduces the main concepts and challenges that face the design of 300GHz-band CMOS circuits and transceivers. In this chapter, the most important challenges and requirements of the transceiver systems are discussed. The CMOS transistor limitations at high frequencies, LO chain and mixer requirements are explored. Beamforming importance and realization conditions are alos explained in this chapter.

Chapter 3 presents several frequency multiplier topologies for F-band and D-band LO signal generation with high output power, low power consumption, and harmonic suppression. Both single-ended and differential solutions are considered.

Chapter 4 presents a 300GHz-band CMOS transceiver system based on subharmonic mixing architecture. The system presented in this chapter achieves 300GHz wireless communication while consuming lower DC power than the recent designs. A subharmonic mixer with high conversion gain and acceptable linearity is presented in this chapter. A hybrid transceiver architecture that includes both CMOS up-/down-conversion circuitry and InP amplification circuitry is also presented in this chapter to study the alternative solutions for high performance 300GHz links.

Chapter 5 presents a 300GHz-band CMOS bi-directional phased-array transceiver system that provides critical features for millimeter-wave links such as beamforming. Output power improvement and image rejection techniques which are included in the system are also explained in this chapter. This chapter also explores the possible phased-array architectures for 300GHz-band systems and explains the details of the stacked antenna solution.

Finally, the conclusions and future directions of this research are presented in chapter 6.

Chapter 2

300GHz-Band CMOS Phased-Array Design Challenges

As discussed in the previous chapter, realizing a 300GHz-band wireless link using the CMOS process is very challenging and requires taking many factors into consideration. This chapter explains in detail the main obstacles and challenges that face the implementation of a practical 300GHz-band CMOS transceiver system with an acceptable power consumption and manufacturing cost.

2.1 $f_{\max}$ of the CMOS Transistor

One of the most important parameters used to evaluate the transistor performance at millimeter-wave and sub-THz frequencies is the maximum oscillation frequency ($f_{\max}$). $f_{\max}$ is the frequency at which the maximum available gain becomes 1 and is the maximum frequency the transistor can oscillate at. Beyond that frequency, it is not possible to achieve any gain from the transistor. To determine the value of $f_{\max}$ for a transistor using the S-parameters, the maximum available gain ($G_{a(max)}$ or MAG) is calculated first. MAG is the theoretical gain achieved when the input and the output impedances of the transistor are perfectly matched. It can be calculated as:

$$G_{a(max)} = \frac{|S_{21}|}{|S_{12}|}\left(K - \sqrt{K^2-1}\right) \tag{2.1}$$

where S_{ij} are the s-parameters of the transistor, and K is the stability factor which is calculated as follows:

$$K = \frac{1-|S_{11}|^2-|S_{22}|^2+|D|^2}{2|S_{12}S_{21}|} \tag{2.2}$$

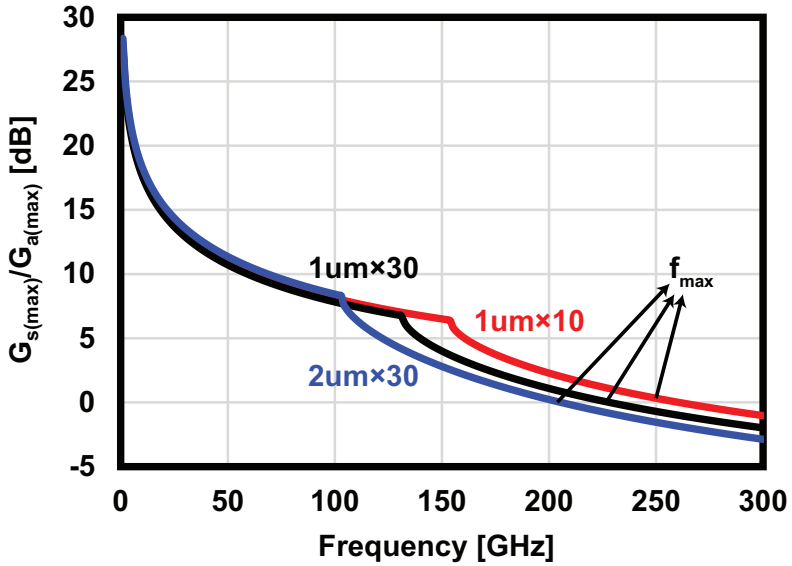


Figure 2.1: Simulated maximum available/stable gain for several transistor sizes in 65nm CMOS process.

given that

$$D = S_{11}S_{22} - S_{12}S_{21} \tag{2.3}$$

This definition of MAG is only applicable when the device is stable unconditionally ($K > 1$), which is the case at higher frequencies. When the device is conditionally stable ($K < 1$), the maximum stable gain (MSG) is used and it is defined as:

$$G_{s(max)} = \frac{|S_{21}|}{|S_{12}|} \tag{2.4}$$

Fig.2.1 shows the simulated MAG/MSG for several transistor sizes in CMOS 65nm process. The frequency at which the MAG becomes 1 (0dB) is the f_{max}. Beyond that frequency, it is not possible to achieve any gain from the transistor. It can be observed that the f_{max} is less than 300GHz making it extremely difficult to implement a reliable amplifier circuit.

The f_{max} is also closely related to the parasitics of the transistor and its interconnects. The following formula clarifies the effect of the main parasitics on the f_{max} [51, 52]:

$$f_{max} = \frac{f_T}{2\sqrt{R_g g_m C_{gd} / \left(C_{gs} + C_{gd}\right) + \left(R_g + r_{ch} + R_s\right) g_{ds}}} \tag{2.5}$$

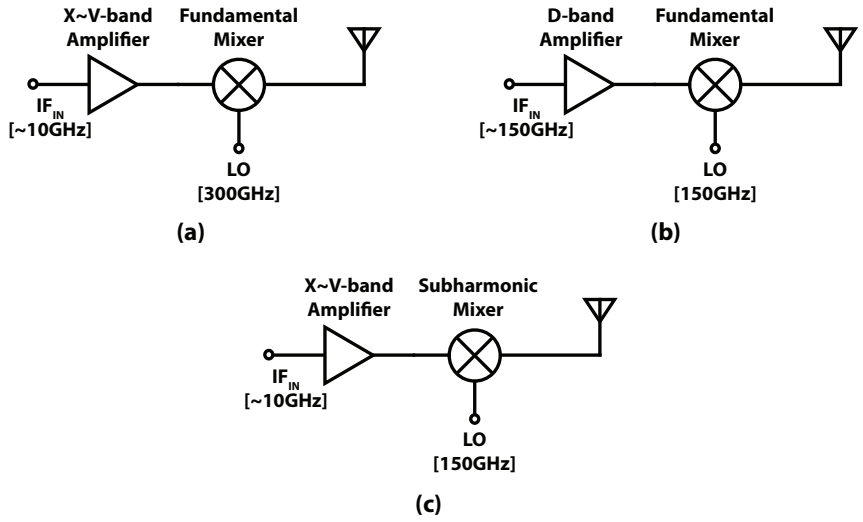


Figure 2.2: Possible 300GHz-band system architecture options for different LO frequencies. (a) Simple fundamental mixing. (b) Both LO and IF are in the D-band. (c) Subharmonic mixing.

where $f_T = g_m/2\pi(C_{gs}+C_{gd})$ is the cut-off frequency, R_g and R_s are the gate resistance and the source resistance, respectively. r_{ch} is the equivalent non-quasi static resistance, g_{ds} is the drain-source conductance, C_{gd} is the gate-drain capacitance, and C_{gs} is the gate-source capacitance.

It is clear from (2.5) that the f_{max} degrades as the parasitic resistance and capacitance increase. The gate resistance has the largest effect, so careful optimization of the gate connection can be one way to improve the overall frequency characteristics of the transistor. Also, (2.5) explains the reason behind the better performance of the smallest transistor in Fig.2.1 at high frequency compared to the larger ones. As a result, even when amplification is realized around 300GHz using CMOS transistors by applying suitable optimization to the transistor size and layout, the achieved output power will be low due to the small transistor size as in [53, 54] for example.

Taking the points mentioned above into consideration, the work in this thesis adopts the mixer-last TX mixer-first RX architecture to overcome the f_{max} limitations. However, f_{max} and gain improvement techniques are applied to the LO buffering circuits which operate between 100GHz and 150GHz as will be explained in the later chapters.

2.2 LO Generation

As mentioned in Chapter 1, the LO signal generation chain of 300GHz-band systems is a very critical part, and it decides how well the mixer operates by providing the suitable driving power and the suppression of the undesired harmonics. The frequency of the LO signal is decided depending on the system overall architecture, but because the RF frequency is extremely high, it is quite difficult to reduce the LO frequency to less than 100GHz. Fig2.2 illustrates several system architecture options that have been demonstrated in the literature (showing only the transmitter part). The simple fundamental mixing option in Fig2.2(a) is the most challenging to implement due to the high LO frequency as the <100GHz IF signal is supposed to be directly up-converted to a much higher frequency band. This option is rarely used due to the complex and power consuming LO generation circuit required to provide a suitable driving power using CMOS. The second option in Fig2.2(b) assumes an IF signal up-converted first to the D-band before getting up-converted again by the RF mixer. This option requires much lower LO frequency, and hence, a much simpler and less power consuming LO chain circuitry. The main issue in this option is the high IF signal frequencies in the D-band which are also required to occupy a very wide bandwidth as well. Implementing a reliable wideband CMOS amplifier that operates with suitable linearity characteristics at such frequencies is not straight forward, and the amplifier may cause the overall system linearity to degrade due to the poor CMOS gain performance in the D-band. Instead of increasing the IF frequency to such high frequencies, subharmonic mixing can be used as illustrated in Fig.2.2(c). The LO signal frequency is kept at around half the RF frequency in the D-band, and the IF frequency is set somewhere below 100GHz. This enables wideband IF amplification with decent linearity while utilizing a high power LO chain that consumes acceptable DC power.

The architecture in Fig.2.2(c) is adopted in all systems presented in this thesis due to its compatibility with the CMOS process. However, a subharmonic mixer with good linearity and high conversion gain is required to make the transceiver system feasible as will be shown in the later chapters.

Another issue that is related to the LO chain of 300GHz-band systems is the appearance of undesired harmonics at the output. Due to the frequency multiplication, many undesired harmonics appear at the output of the LO chain. These harmonics may up-convert undesired signals to the RF band, and they may cause serious linearity issues to the RF mixer. A detailed discussion about the requirements and the design techniques of the frequency multipliers is introduced in the next chapter.

2.3 Error Vector Magnitude

Bit Error Rate (BER) is one of the most common indicators to evaluate the communication system performance. It is the ratio between the number of bit errors and the total number of transmitted bits during a time interval. For wireless communication to take place, a BER of 10^{-3} is considered acceptable. The BER is directly related to two other parameters that can be calculated directly from circuit component characteristics; signal-to-noise ratio (SNR) and error vector magnitude (EVM). Both of these parameters are closely related to each other as well, and the following equation estimates the that relation as calculated in [55]:

$$SNR \approx \frac{1}{EVM^2} \tag{2.6}$$

Fig.2.3 plots the relation between BER and SNR for several modulation schemes. As can be expected, higher SNR values are required for higher-order modulation schemes to achieve the required BER as the number of levels increases. A 9.8dB SNR (around -9.8dB EVM) is required to achieve QPSK wireless communication, while a 16.5dB (around -16.5dB EVM) SNR is required to achieve 16-QAM link and so forth.

In the real case, there are many additional factors that increase the EVM and degrade the overall BER. The distortion caused by the non-linearity of the devices must be added to the equation by replacing the SNR by signal-to-noise and distortion ratio (SNDR), where the distortion is usually dominated by the third-order inter-modulation components (IM3). Additional EVM degradation factors including carrier phase noise (φ^2_{RMS}), image signals or I/Q mismatch, LO feedthrough (LOFT) if in-band, and the gain flatness (GF) of the RF band. The equation (2.6) becomes as follows [5]:

$$EVM_{tot} \approx \sqrt{\frac{1}{SNDR^2} + \varphi^2_{\text{RMS}} + EVM^2_{\text{image}} + EVM^2_{\text{LOFT}} + EVM^2_{\text{GF}}} \tag{2.7}$$

Achieving the EVM requirements for the 300GHz-band transceivers is much more difficult compared to the commonly used lower frequency bands as the target bandwidth is much wider, the path loss is much higher, and the device performance is quite limited. That explains the critical role of the RF mixers in the 300GHz-band CMOS mixer-last TX mixer-first RX systems, as the mixer characteristics define the overall EVM of the system. Here, both the output signal power and the noise figure of the mixer have direct effect on the system SNDR due to the absence of RF amplification.

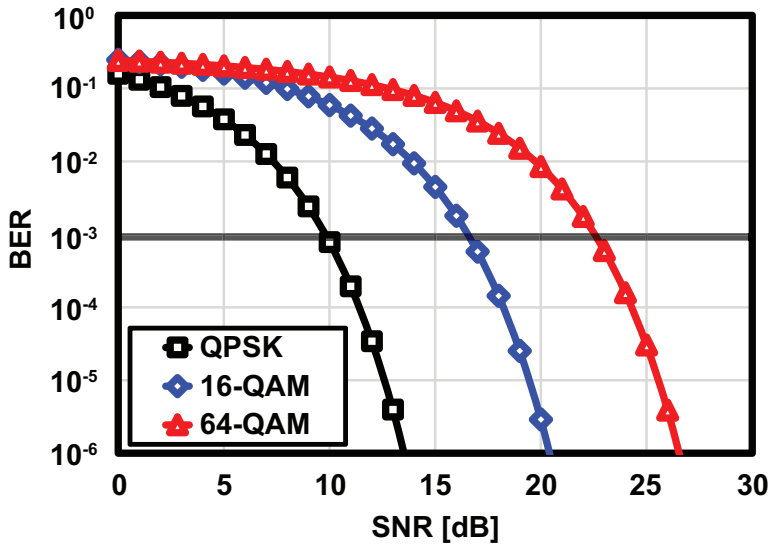


Figure 2.3: Calculated BER against SNR for several modulation schemes

2.4 FSPL and Beamforming

The transmitted signal in any wireless system experiences a drop in its power level before reaching the receiver input due to the propagation nature of electromagnetic waves and the finite antenna size. This loss is commonly referred to as free-space-path-loss (FSPL) and is defined as follows:

$$\text{FSPL(dB)} = 20\log\left(\frac{4\pi df}{c}\right) \tag{2.8}$$

where d is the communication distance between the transmitter and the receiver, f is the signal frequency, and c is the speed of light. It is observed in (2.8) that increasing the frequency from the commonly used 3GHz frequency to 300GHz increases the FSPL by a huge 40dB (or 10000 times as can be expected from the inverse-square law). Antennas with high directivity such as horn antennas and lens antennas are commonly used to solve the large FSPL issue in 300GHz-band systems. However, such implementation causes the link to be realized only when the RX is placed within the radiation angle of the horn/lens antenna which is usually very narrow especially when the antenna gain gets higher. Any change of the RX radial position will highly degrade the communication performance.

To solve this issue effectively, many millimeter-wave systems adopt the phased-array implementation where many transceivers and their antennas (printed antennas in most cases) are placed as an array with certain pitch, and the phase of each transceiver (element) is controlled so that the total radiation direction shifts to the desired angle. This way, both

TX and RX radial positions can be changed within the range of the array which is much wider than the beam width of a high-gain horn antenna. Although the antenna gain of printed antennas is smaller than that of horn and lens antennas, the array gain itself gets higher as the number of elements increases. The following equation shows the calculation process of the link budget considering all parameters (all in dB):

$$P_{\mathrm{OUT(TX)}} + G_{\mathrm{TX}} + G_{\mathrm{RX}} - FSPL - NoiseFloor > SNR_{\mathrm{req}} \tag{2.9}$$

where $P_{\mathrm{OUT(TX)}}$ is the output power of the TX, G_{TX} and G_{RX} are the antenna gain values of TX and RX, respectively (array gain if phased-array), *NoiseFloor* is the noise floor at the input of the receiver, and SNR_{req} is the required SNR for the target link.

Implementing the phased-array system at 300GHz-band has a big obstacle compared to the phased-array systems of lower millimeter-wave frequencies due to the very short wavelength. This issue is discussed in details in the next section.

2.5 Challenges for 300GHz-band Phased-Array

The phased-array implementation is essential for 300GHz-band systems to overcome the high FSPL issue while providing some flexibility to the system so that additional applications and use cases become feasible for 6G technology in the future. However, the phased-array design at this band has many critical issues that are not considered dominant at lower frequencies. The first issue resides in the large losses that the passive structures have on- and off-chip due to the short wavelength of the target band. That means that antenna implementation and its connection to the transceiver circuit needs much more attention compared to the other bands. Another issue that is related to the physical structure of the array, especially the antenna spacing, is the very short antenna pitch required to achieve acceptable beam steering range. Other issues also include the area and cost limitations, and the power consumption. In this section, some more details about the mentioned issues are introduced, with a brief explanation of the strategies this thesis proposes to face them.

2.5.1 Antenna Implementation and Connection

The short wavelength at 300GHz (around 1mm) reduces the size of the antenna considerably. This can be an advantage when wireless sensor networks or medical applications are targeted considering the size limitations in these cases. As the antenna size is in the millimeter order, it can be implemented even on-chip alongside the transceiver circuit.

However, the on-chip antenna characteristics rely heavily on the chip dielectric material characteristics, especially the relative permittivity (ε_r) and the resistivity. The low resistivity of the silicon substrate for example causes large losses and a huge degradation in the radiation efficiency [56].

The on-PCB antenna is a better option when the antenna performance is prioritized. There are many PCB material choices with much better characteristics for antenna implementation. Low permittivity and higher resistivity can be obtained by using the suitable material regardless of the chip materials. The main drawback of the on-PCB antenna is that a lossy structure is required to connect the transceiver chip to the PCB antenna. Wire bonding is a very poor option at 300GHz considering its length which is too long compared to the wavelength, resulting in a large inductance that causes serious degradation to the RF signal. The flip chip process is another option that shows a much better compatibility with the higher frequencies due to the small size of the connecting bump. The distance between the chip and the PCB after implementation can be as short as 20μm. On the other hand, the flip chip process is more complicated and costly compared to the wire bonding, and smaller bumps should be used at high frequency causing more complication and high cost.

2.5.2 Antenna Placement and Spacing

The placement of antennas in phased-array systems must be considered thoroughly to avoid the degradation in the beam shape and the steering range. The spacing between antenna elements directly affect the angle range as can be calculated using the following equation:

$$\Delta\Phi = \frac{2\pi d \sin\theta}{\lambda} \tag{2.10}$$

where $\Delta\Phi$ is the phase shift between elements, d is the distance between elements, and θ is the beam angle. The beam angle range calculated results for three different antenna pitches (0.5λ, λ, and 2λ) are shown in Fig.2.4. It can be observed that a long pitch causes the steering range to be narrower, and 0.5λ is the maximum pitch that covers the whole range. A 2λ pitch means that the steering range does not exceed 30° as well.

In the conventional millimeter-wave phased-array systems, the arrays consisting of broadside antennas like metal patches are more common as the antennas are aligned in a two-dimensional fashion with a $\lambda/2$ pitch. For frequencies around 28GHz (5G standard band) this structure is not so difficult to realize as the wavelength is in the centimeter order as can be seen in Fig.2.5(a). However, when it comes to the 300GHz-band, the wavelength is much shorter, and the required pitch becomes shorter as well. Considering a 1–2mm wide chip, antennas need to be placed so far from chip to obtain the $\lambda/2$ pitch as

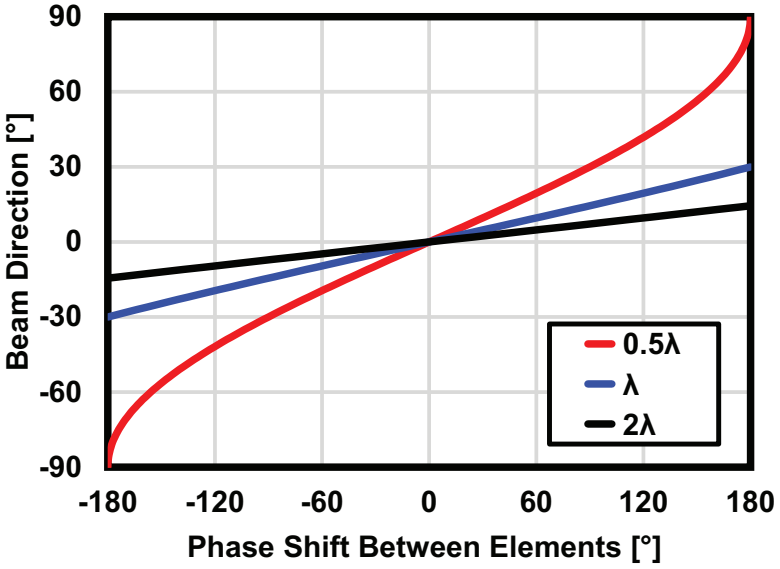


Figure 2.4: Beam steering range for different antenna pitch lengths.

illustrated in Fig.2.5(b). The long distance between the chip and the antenna means that long lossy transmission lines are required on-PCB, causing huge losses to the RF signal.

On-chip arrays as in [57–61] make it possible to build a suitable structure with a suitable antenna pitch, but the chip area is huge and the antenna gain is limited due to the large silicon substrate loss as discussed in the previous section.

By knowing that the thickness of the CMOS chip with the PCB is still less than λ even at the 300GHz-band. A stacked antenna alignment can be adopted instead of the horizontally adjacent configuration as illustrated in Fig.2.5(c). The end-fire antennas are used here, and the antenna pitch in the stack can be $\lambda/2$ without using long lossy connecting transmission lines.

2.5.3 Power Consumption

The use of multiple transceiver circuits to build the phased-array system causes the overall power consumption to increase considerably. Hence, the power consumption of every chip must be minimized by improving the efficiency of the frequency conversion circuits.

2.5.4 Manufacturing Cost

The manufacturing cost is another critical factor that must be considered in the phased-array system design. The chip area is surely one of the main cost deciders, but the off-chip connections are also very crucial at 300GHz. High-cost materials with good high

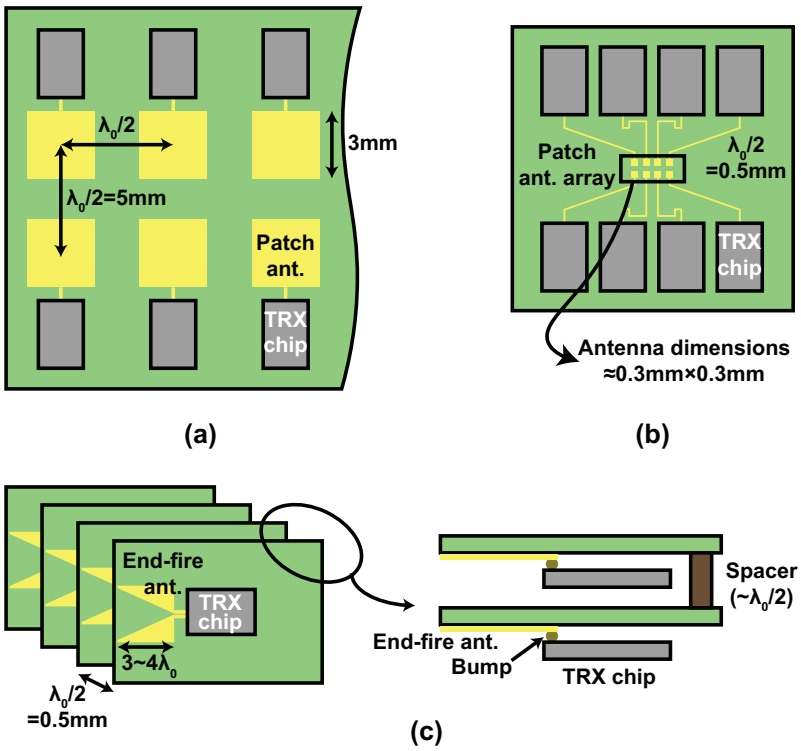


Figure 2.5: Phased-array implementation issue at 300GHz-band. (a) 28GHz phased-array structure. (b) Using the same structure for 300GHz. (c) Proposed stacked architecture.

frequency characteristics are required instead of the conventional cheap ones. Flip chip and module implementation also cause the cost of manufacturing to go up.

Another big choice to make for phased-arrays is whether to implement several transceivers on the same chip or to implement each transceiver on a chip. The first option reduces the off-chip components and losses, but higher chip fabrication cost is expected as the yield by necessity gets lower on bigger chips [62]. Such dilemmas and their solutions will shape the way sub-THz phased-array transceivers develop in the future.

Chapter 3

Frequency Multipliers for LO Generation [1]

The LO signal generation circuitry is one of the most challenging parts of the 300GHz-band systems as its operating frequency is in the sub-THz region, and the required output power is relatively high to drive the mixer properly. The low-efficiency LO buffers operating at the sub-THz frequencies consume large DC power as a result. So, if the previous frequency multiplier stage provides suitable signal power with sufficient undesired harmonic suppression, the number of LO buffering stages can be reduced lowering the overall system power consumption.

Simple circuit architecture is usually preferred at the sub-THz frequencies to reduce the losses and the required area as transmission lines are heavily used. So, relatively simple, high-power/conversion-gain characteristics, and fundamental/harmonic suppression are the main targets for sub-THz frequency multiplier design. In this chapter, several frequency multipliers operating mainly at the F-band (90-140GHz) frequencies with improved output power and harmonic rejection characteristics are introduced. The area is minimized by adopting very simple structures and effective rejection techniques.

3.1 Frequency Multiplier Topologies

Many works focused on providing superior frequency multiplier circuits at W-, F- and D-band as in [64–72]. The choice of the suitable frequency multiplier topology to be used

[1] This chapter is based on "F-band Frequency Multipliers with Fundamental and Harmonic Rejection for Improved Conversion Gain and Output Power" [63], by the same author, which appeared in the IEICE Transactions on Electronics, © 2021 IEICE. The material in this paper was presented in part at the IEICE Transactions on Electronics [63], and some of the figures of this paper are reused from [63] under the permission of the IEICE.

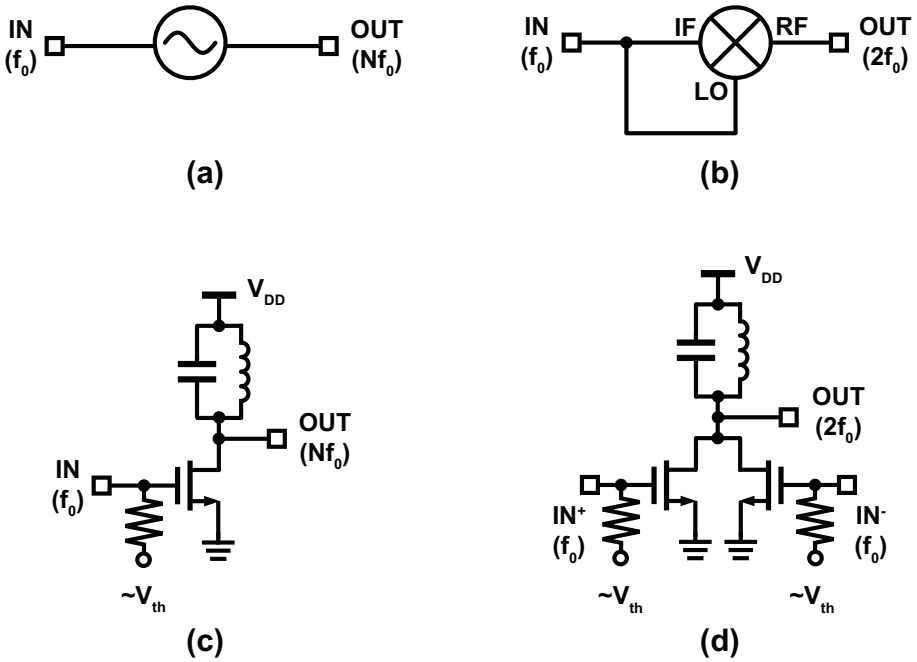


Figure 3.1: Conventional frequency multiplier topologies: (a) Injection-lock-based, (b) Mixer-based, (c) Device nonlinearity-based, and (d) Push-push-based.

in the 300GHz-band CMOS transceiver system usually depends on the simplicity and the feasibility at frequencies around the f_{max}. The main common frequency multiplier topologies can be divided into four as illustrated in Fig. 3.1 [73]. The injection-based topology [64] can provide the desired output with relatively low input power, but they have limited performance when operating at a frequency far from the center frequency. Mixer-based multipliers have a wider operation bandwidth, but they have high input requirements to operate properly [72]. Device/Line Nonlinearity-based multipliers [65, 68] are very common for high frequencies due to their simplicity and compatibility with the transmission line-based design. However, their conversion gain is limited and the undesired harmonics still appear at the output due to the wideband characteristics of the matching circuits at such frequencies. Push-push-based frequency doublers are also very common for sub-THz systems [66, 67, 69–71], but balun mismatches at the input side cause leakage of the fundamental signal to the output and degrades the output power.

In the following sections of this chapter, F-band device nonlinearity-based frequency triplers with fundamental and second harmonic cancellation techniques and a push-push-based frequency doubler with balun mismatch compensation techniques are introduced.

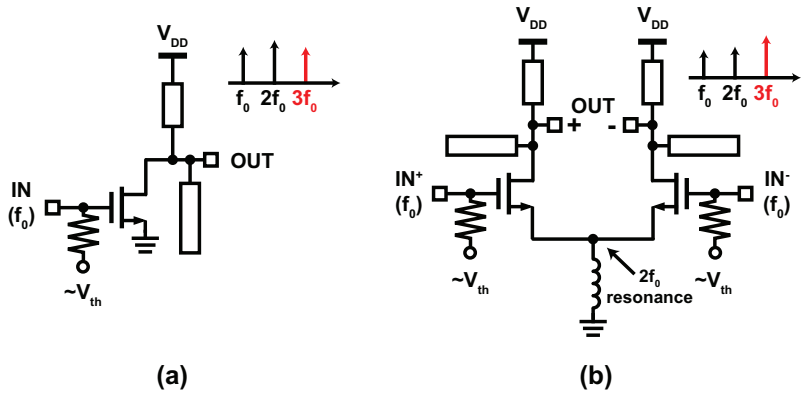


Figure 3.2: Conventional device nonlinearity-based frequency triplers: (a) Single-ended, (b) Differential with second harmonic resonance at the tail node.

3.2 Millimeter-Wave Frequency Triplers

One of the main design considerations of the frequency multiplier design is the ability to reject undesired harmonics so that they do not appear at the output. The device-nonlinearity-based frequency multipliers normally operate at higher input power values to get higher conversion gain. So, suppressing the fundamental frequency and the undesired harmonics is very important to avoid the saturation of the circuit by the undesired components. As a result, the desired frequency signal will dominate the output and its power will improve. For the frequency tripler circuit, the most common technique to reject the fundamental signal is by utilizing the bandpass characteristics of the output matching network. However, the wideband nature of the transmission-line-based matching networks causes the rejection to be insufficient. Placing open quarter-wave stubs at the output to reject the fundamental component is not effective for triplers because the third harmonic will face a small impedance similar to that at the fundamental frequency as the electrical length there is $3\lambda/4$. Using the quarter-wave stub at the second harmonic frequency also degrades the third harmonic output power due to the wideband characteristics of the stub. The conventional architecture is illustrated in Fig. 3.2,(a). One of the solutions is to use the differential architecture to automatically cancel the second harmonic which has even characteristics as shown in Fig. 3.2,(b). By adding a tail inductance, the output can be improved as well [34]. However, the fundamental rejection still depends on the matching network characteristics. It is also common to have single-ended buffering stages when it comes to the operation close to $f_{\max}$ due to the design flexibility and layout simplicity.

This section presents two novel tripler circuits for improved output power and harmonic rejection; (i) a single-ended tripler circuit with a passive feedback network, and (ii) a differential tripler with filtering stubs and balun mismatch compensation.

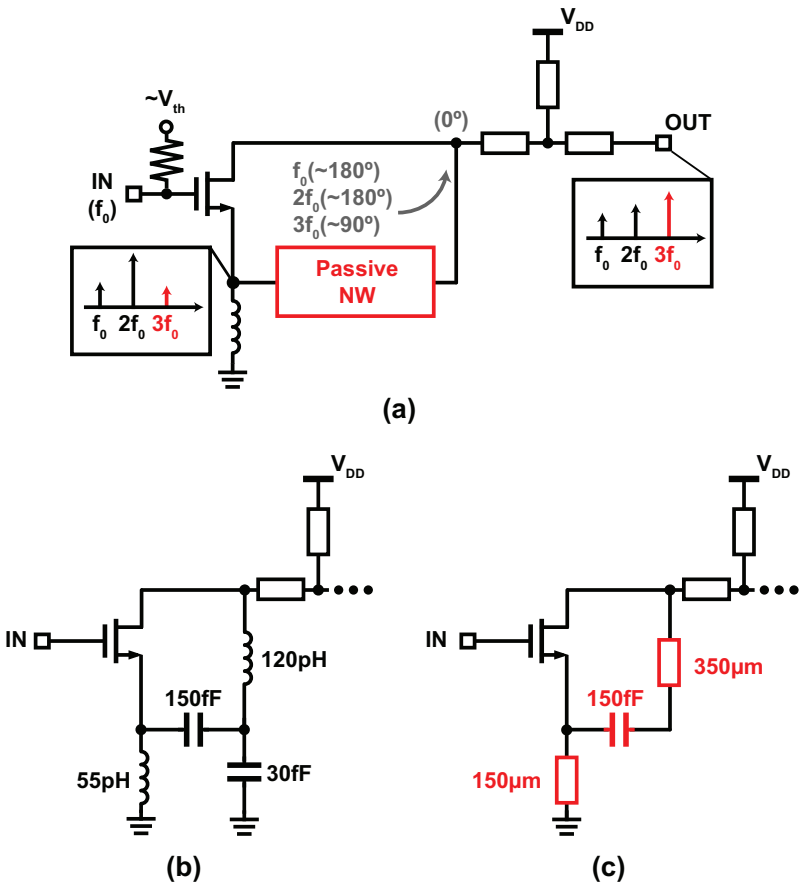


Figure 3.3: Proposed fundamental and second harmonic rejection technique. (a) The feedback network operation. (b) The circuit built using lumped components. (c) The proposed circuit.

3.2.1 Proposed Single-Ended Tripler

In this work, a tripler circuit with a passive feedback network is proposed to improve the performance as shown in Fig. 3.3,(a). The inductor that is connected to the source resonates at the second harmonic to generate the cancellation signals, and the passive network passes these components to the output with the suitable phase shifts. The phase difference between the drain current and the feedback current at the undesired fundamental and second harmonic frequencies must be around 180° to provide the cancellation, while a phase difference of less than 90° between the drain and the feedback currents is required at the desired third harmonic to avoid any cancellation as:

$$|I_{out3}| = \sqrt{|I_{d3}|^2 + |I_{f3}|^2 + 2|I_{d3}||I_{f3}|\cos(\theta)} \tag{3.1}$$

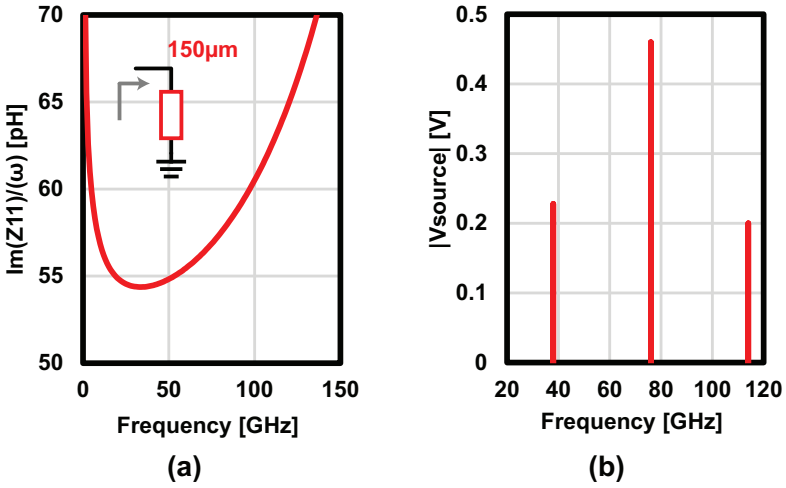


Figure 3.4: (a) The inductance of the tail transmission line. (b) The voltage magnitude at the source for all the harmonics. (f_0=38GHz, P_{IN}=10dBm)

where I_{out3}, I_{d3}, and I_{f3} are the output, drain, and feedback currents at the third harmonic, respectively. θ is the phase differency between the drain and the feedback currrents. For $|\theta| \leq 90°$, it is guaranteed that the output current is larger than the drain current. The passive network is also designed to have a very low impedance at the fundamental frequency to increase the suppression, and a very high impedance at the desired third harmonic to avoid any degradation.

The circuit can be designed using lumped elements as shown in Fig. 3.3,(b). However, using the inductors at high frequencies may cause some design difficulties regarding their modeling and layout limitations. Hence, in this work, we use the transmission lines to provide the suitable inductance and phase shifts as illustrated in Fig. 3.3,(c).

To calculate the source transmission line length, the input impedance formula is used:

$$Z_{\text{in}}(l) = Z_0 \frac{Z_{\text{L}} + j(Z_0 \tan(\frac{2\pi}{\lambda} l))}{Z_0 + jZ_{\text{L}} \tan(\frac{2\pi}{\lambda} l)} \tag{3.2}$$

where $Z_{in}(l)$ is the input impedance of the line with the transmission line length l, Z_0 is the characteristic impedance of the transmission line (50 Ω), λ is the electrical wavelength, and ω is the angular frequency. For a $Z_L = 0$, the transmission line length to provide the suitable inductance is around 150μm. The simulated inductance is shown in Fig. 3.4(a). The voltage components at the transistor source are shown in Fig. 3.4(b) with the second harmonic voltage having the largest magnitude. The calculated value provides the best second harmonic rejection as the simulation results show in Fig. 3.5. The sensitivity of

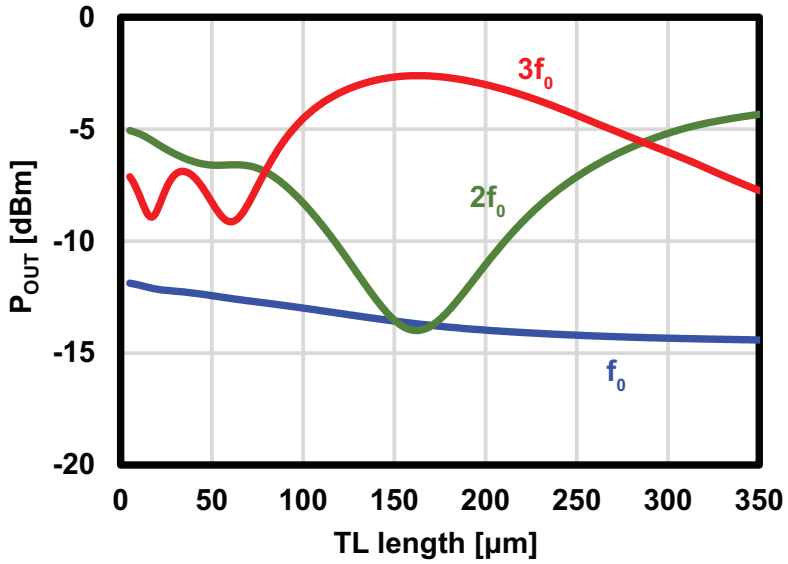


Figure 3.5: Simulated output power of the frequency tripler for different tail transmission line lengths. (f_0=38GHz, P_{IN}=10dBm)

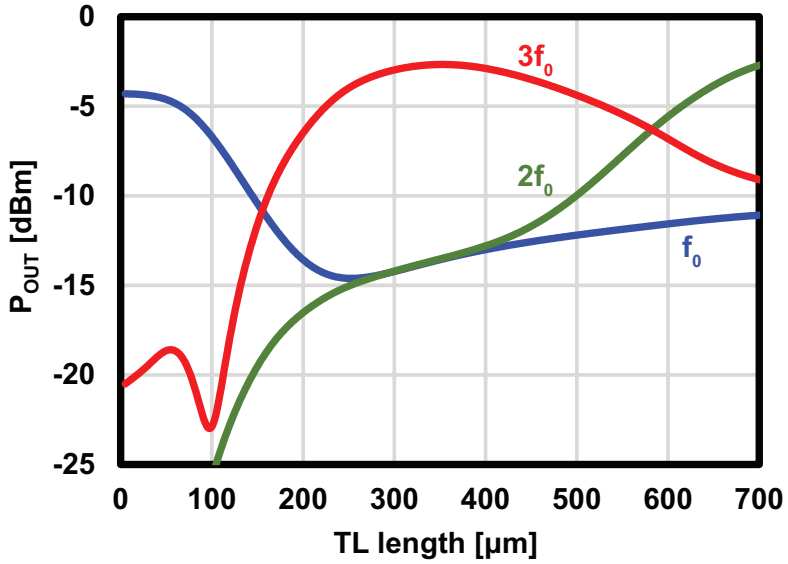


Figure 3.6: Simulated output power of the frequency tripler for different feedback transmission line lengths. (f_0=38GHz, P_{IN}=10dBm)

the operation against the feedback line variation is also investigated in Fig. 3.6 and the performance is reliable even for large line length error. Adding the transmission line to the source slightly degrades the small-signal output power of the tripler, but the improvement

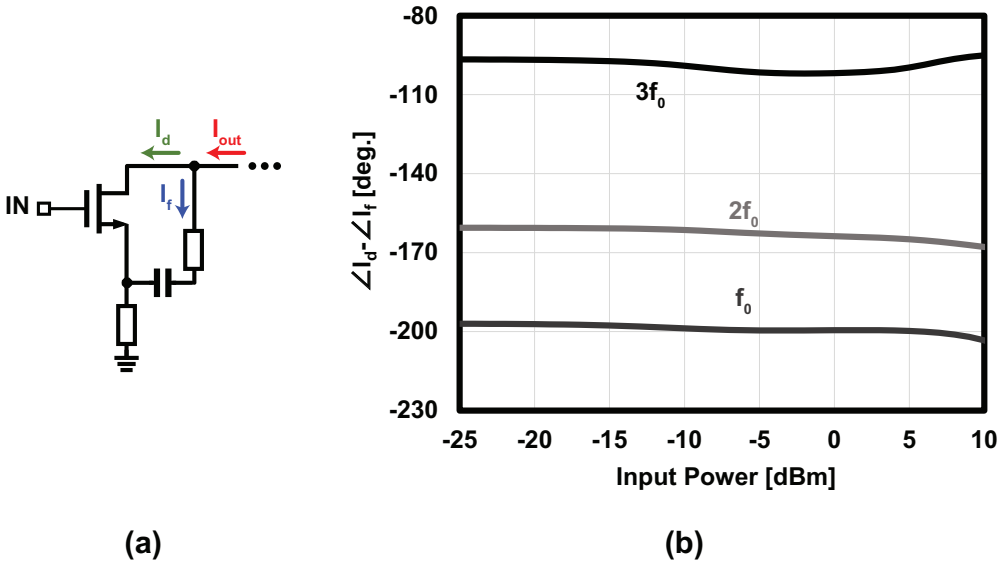


Figure 3.7: Frequency tripler simulated operation: (a) The simulated currents, (b) The simulated phase difference between the drain and the feedback currents. (f_0=38GHz, P_{IN}=10dBm)

caused by the fundamental and second harmonic rejection has a larger effect for higher input power situations.

The operation of the tripler is further investigated in Fig. 3.7. The currents of the branches shown in Fig. 3.7(a) are simulated to evaluate the feedback performance. The simulated phase difference between the drain current and the feedback network current is near 180°, as shown in Fig. 3.7(b), and the difference is close to 90° in the third harmonic signal case. The output current is considerably smaller than the original drain current at the fundamental and the second harmonic frequencies as can be observed in Fig. 3.8(a) and (b). The output current at the fundamental frequency seems large at the output, but it can be easily suppressed further by the matching network as the desired frequency is much higher. The desired third harmonic signal amplitude has a slight increase due to the 90° phase difference (Fig. 3.8(c)).

The detailed schematic of the proposed tripler is illustrated in Fig. 3.9. Input and output matching circuits are implemented using short stubs. The micrograph of the chip which was fabricated using 65nm CMOS is shown in Fig. 3.10. The simple, single-ended circuit structure made the area as small as 0.29mm^2 with a much smaller active area.

The measurement setup used to characterize the proposed tripler is illustrated in Fig. 3.11. The input signal is generated using a 67GHz signal generator that covers the whole target band, and the output is detected using VDI Erickson Power Meter. A WR-8 waveguide

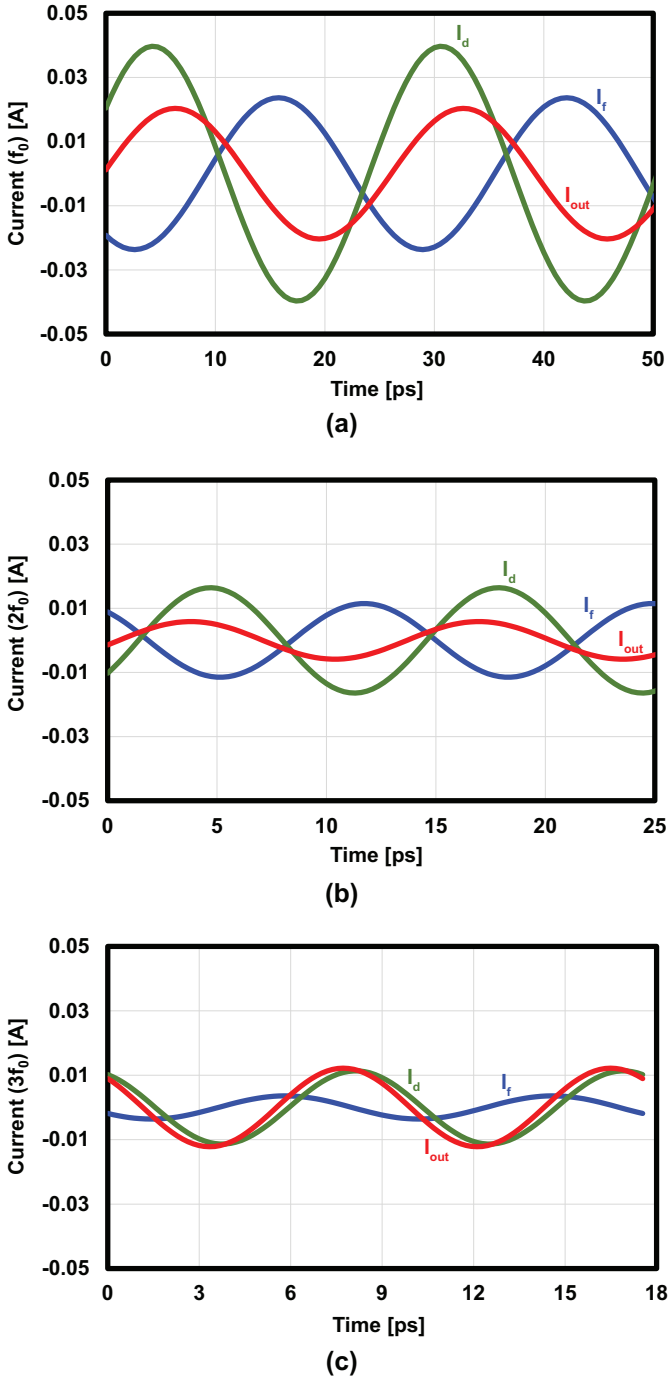


Figure 3.8: Frequency tripler simulated operation: (a) Current waveforms of fundamental signals, (b) second harmonic signals, and (c) third harmonic signals (f_0=38GHz, P_{IN}=10dBm)

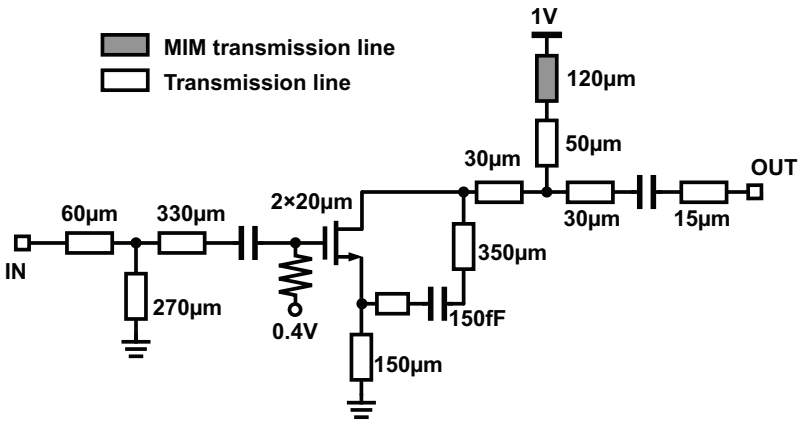


Figure 3.9: Proposed frequency tripler circuit schematic.

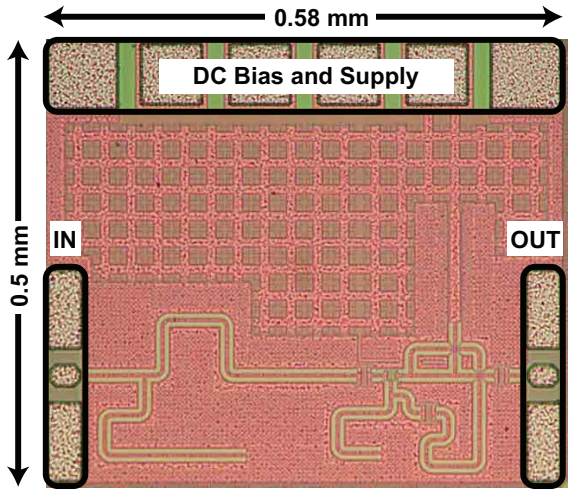


Figure 3.10: Frequency tripler micrograph. (© 2021 IEICE)

probe is used to connect the circuit output pad to the power sensor. The simulated and measured output power values of the proposed tripler are shown in Fig. 3.12. Around -2.9dBm output power is achieved with a bandwidth of around 27GHz. The measured fundamental signal rejection ratio (HRR1) is shown in Fig. 3.13(a). More than 10dB rejection is achieved around the center frequency similar to the second harmonic rejection ratio (HRR2) shown in Fig. 3.13(b).

The measured power in/out characteristics at 38GHz input frequency (114GHz output frequency) are shown in Fig. 3.14. The maximum conversion gain is around -13.5dB. The simulation results show good agreement with the measured results as can be seen in the graphs. Table 3.1 compares the performance of both proposed tripler and doubler circuits with the state-of-the-art CMOS frequency multipliers that operate at frequencies around

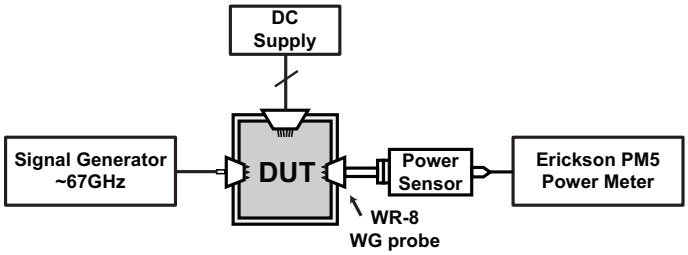


Figure 3.11: Measurement setup.

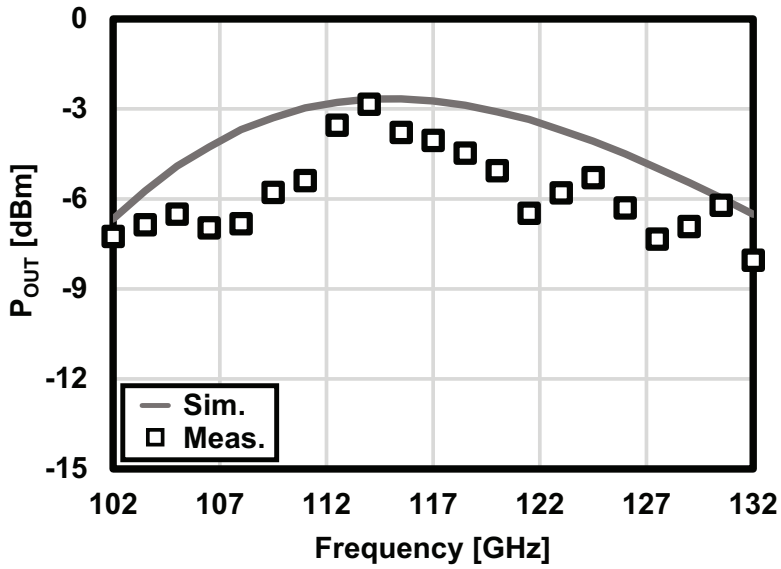


Figure 3.12: Tripler measured and simulated output power. (input power = 10dBm)

100GHz. The tripler achieves competitive performance with a very simple single-ended device non-linearity-based architecture thanks to the harmonic cancellation techniques, reducing the required area and DC power. Injection-locking-based designs as in [64] may show superior performance, but they require tuning due to the PVT variation as they are oscillator-based, not to mention the inclusion of buffers.

Table 3.1: Tripler Performance Comparison

	This Work	**[64]**	**[65]**
Process	65nm CMOS	40nm CMOS	130nm CMOS
Frequency [GHz]	103-130	115-129	92-104
Mult. Factor	×3	×3	×3
Topology	Device NL[$]	ILFT[#]	NLTL[%]
Max. CG [dB]	−13.5	N/A	−12.2
Max. P_{OUT} [dBm]	−2.9	3	−1.5
HRR1[*] [dB]	3.7-12.3	> 38	N/A
HRR2[**] [dB]	8.6-15.4	> 20	N/A
P_{DC} [mW]	< 28	53.2	135
Area [mm^2]	0.29	0.36	1.12

[*] Fundamental rejection ratio. [**] Second harmonic rejection ratio.
[$] Device non-linearity [#] Injection-locking frequency tripler.
[%] Non-linear transmission line.

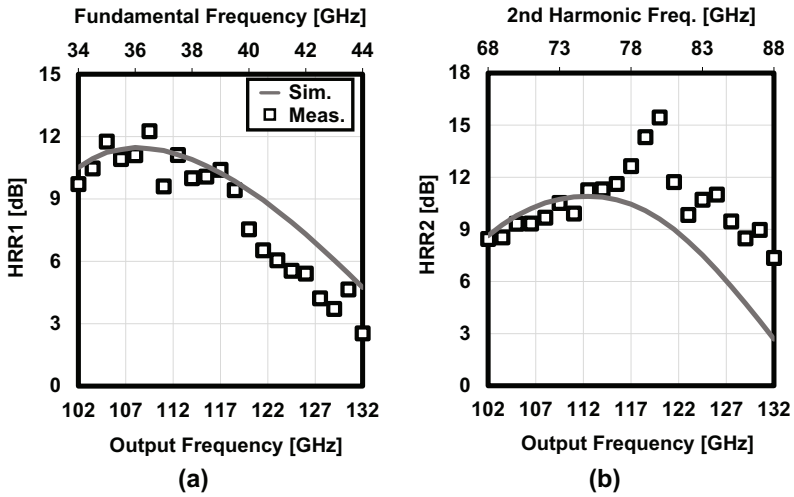


Figure 3.13: Tripler measured and simulated fundamental rejection ratio. (input power = 10dBm)

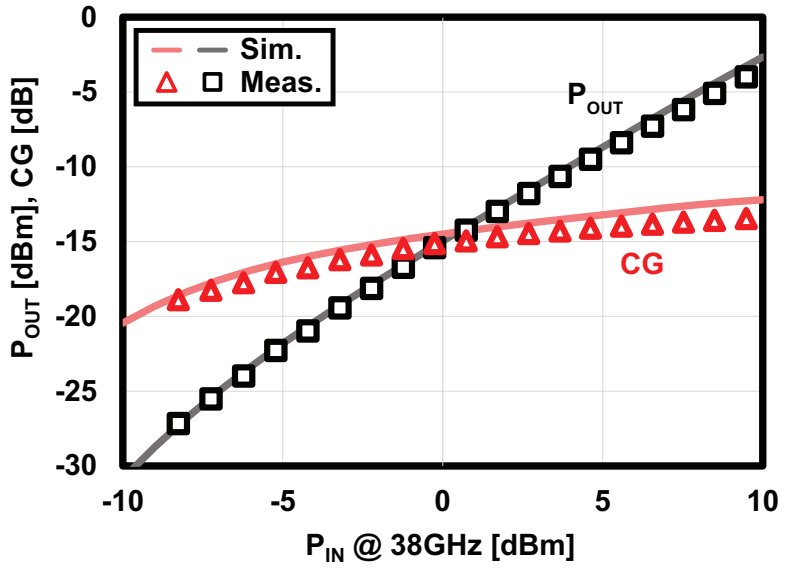


Figure 3.14: Tripler measured and simulated output power and Conversion gain.

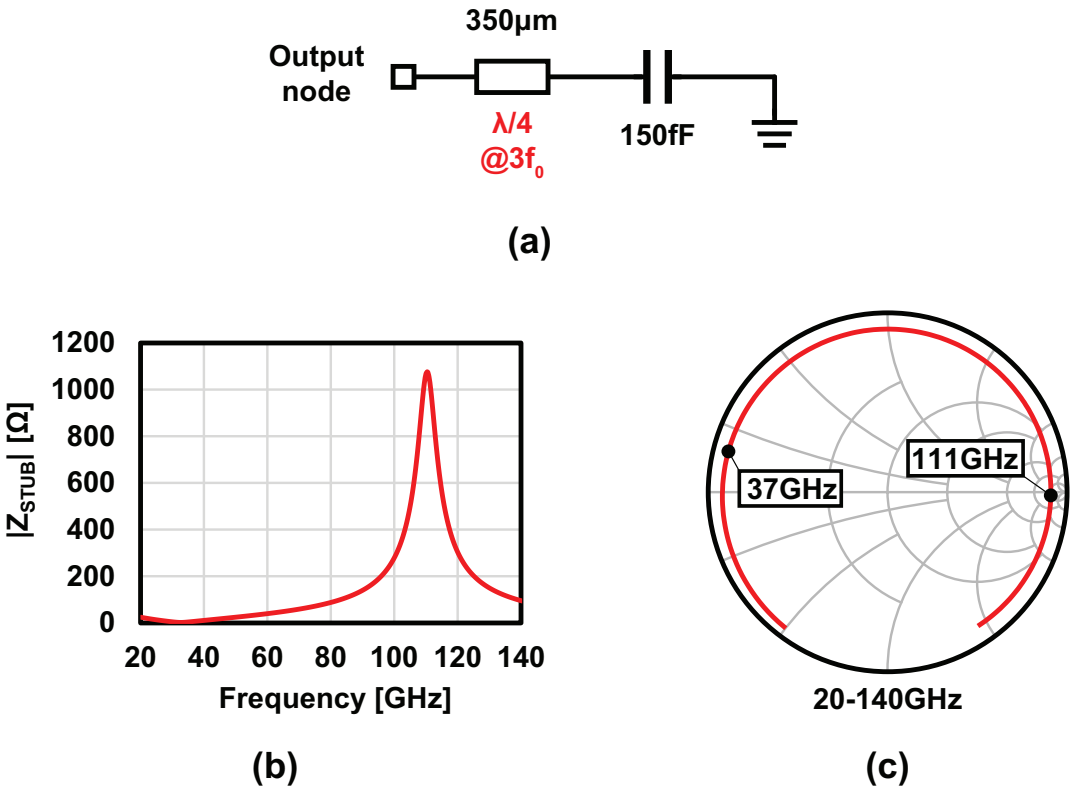


Figure 3.15: Fundamental rejection stub (a) schematic (b) simulated stub impedance, (c) smith chart.

3.2.2 Proposed Differential Tripler

As mentioned earlier in this section, the differential architecture automatically cancels the second harmonic at the tripler output due to the odd symmetry. However, the perfect symmetry is not possible in practical situations as balun and device mismatches cause the second harmonic common mode signal power to increase. The fundamental signal which is usually suppressed using stubs may still have high power at the output due to the non-ideal characteristics of the stubs. In this subsection, fundamental and second harmonic suppression techniques that utilize the differential properties are introduced.

First, a fundamental frequency rejection stub illustrated in Fig. 3.15(a) is introduced. a quarter-wave stub at the third harmonic frequency is loaded with a purely capacitive reactance. The input impedance of the stub is calculated as in the following equation:

$$Z_{\text{in}}(l) = Z_0 \frac{j(Z_0 \tan(\frac{2\pi}{\lambda} l) - \frac{1}{\omega C})}{Z_0 + j\frac{1}{\omega C}\tan(\frac{2\pi}{\lambda} l)} \tag{3.3}$$

where $Z_{\text{in}}(l)$ is the input impedance of the stub with the transmission line length l, Z_0 is the

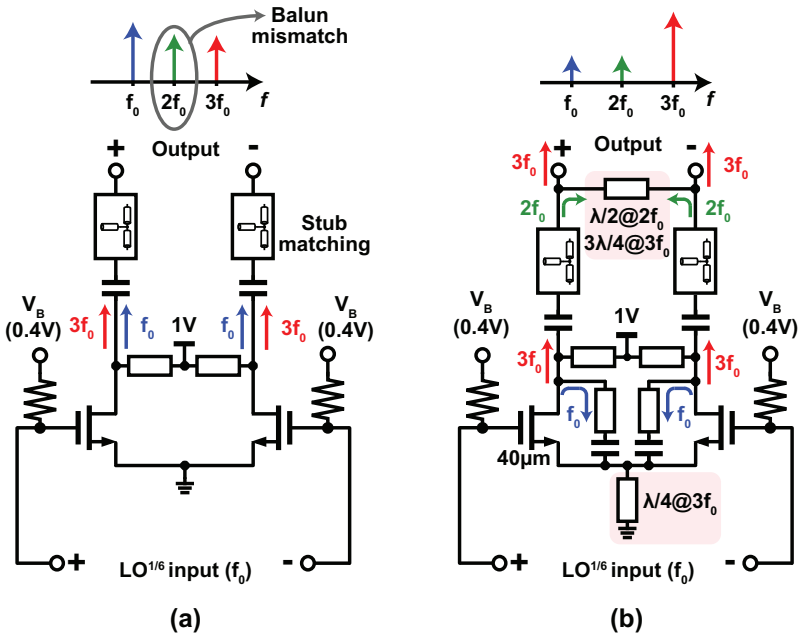


Figure 3.16: Tripler circuit (input signal frequency = f_0 = 38–39GHz): (a) Conventional differential tripler. (b) Proposed tripler circuit.

characteristic impedance of the transmission line (50 Ω), λ is the electrical wavelength, ω is the angular frequency, and C is the load capacitance. The capacitance value is optimized so that the stub looks as a short circuit at the fundamental frequency, while having a large impedance at the third harmonic to avoid any losses. Since the load is purely capacitive (ideally), the stub will act as an open or short when the imaginary part is equal to zero. Hence,

$$C = \frac{1}{Z_0 \omega \tan(\frac{2\pi}{\lambda} l)} \tag{3.4}$$

The optimal calculated C value using (3.4) is around 150fF.

Fig. 3.15(b) shows the simulated impedance of the stub. High impedance is achieved at the desired frequency (111GHz) while a very small impedance can be observed around the fundamental frequency similar to an open quarter-wave stub. The smith chart is also shown in Fig. 3.15(c).

The explained fundamental rejection stub is applied to the differential tripler architecture as shown in Fig.3.16(a) and (b). A virtual ground appears between the two stubs connected to both differential ends. The stubs are also connected to the sources of the transistors which are connected to a tail transmission line with the length of $\lambda/4$ at the third harmonic of the input frequency to prevent the loss of the desired signal. The fundamental frequency component flows through the stub and gets canceled due to the low

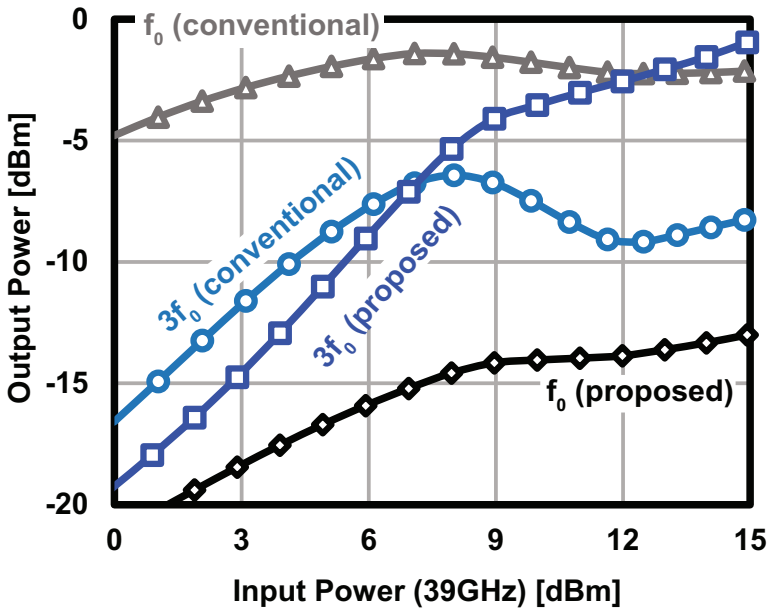


Figure 3.17: Proposed tripler simulated output power and the comparison with the conventional architecture.

impedance path. The fundamental component is reduced by about 20dB by this method and the output power of the desired third harmonic signal increases for high input power values as simulation results show in Fig.3.17. This increase is because of the dominance of the third harmonic signal at the output compared to the fundamental-dominated case of the conventional architecture. The common mode second harmonic signal appears at the output due to the balun mismatch and the nature of the even harmonics, causing undesired effects on the tripler linearity and on the succeeding stages. In order to reduce second harmonic degradation, a $\lambda/2$-length transmission line (at the second harmonic frequency) is added to connect the differential ends. The line acts as two open stubs for common mode signal with the length of $\lambda/4$, but it acts as two shorted stubs with the length of $3\lambda/8$ at the desired third harmonic, and it is used as a part of the matching network. As a result, the second harmonic signal is canceled completely without affecting the desired output signal by adding this compensating line. The simulated improvement of second harmonic rejection by adding the line is shown in Fig.3.18. The differential tripler consumes a 40mW power from a 1V supply when driven by a 7dBm input signal.

The frequency tripler introduced in this subsection is one of the important building blocks used to implement the system presented in the following chapter. Due to its good output power and harmonic rejection characteristics, the number of LO buffers is reduced

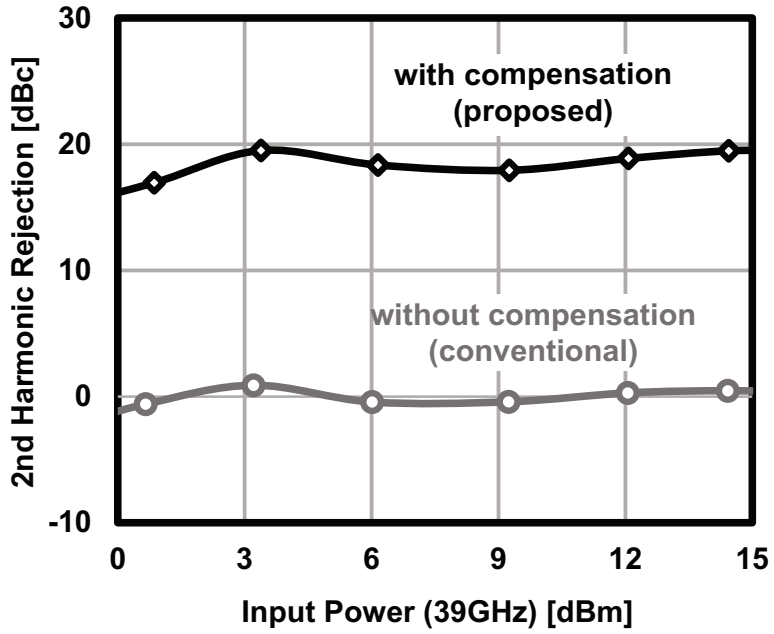


Figure 3.18: Proposed tripler simulated 2nd harmonic rejection and the comparison with the conventional architecture.

and the overall power consumption of the transceiver system is successfully reduced.

3.3 Push-Push Doubler

The push-push frequency doubler is a very common topology for millimeter-wave frequency doublers due to its high output power and automatic rejection of the fundamental signal. Fig. 3.19 shows the basic schematic and operation principle of the push-push doubler. Two transistors are connected by the drains and sources, while the input signal is applied differentially to their gates. The bias voltage for both transistors is set to be around the threshold voltage of the transistor. As each transistor conducts for half a cycle, the resulting output current has twice the frequency of that of the input voltage. The differential fundamental signal leaked power signals cancel each other at the output.

However, balun mismatches can cause the fundamental signal leakage to appear at the output again, and it causes the output power of the doubler to be degraded as well. To avoid the balun mismatch issues and to improve the output power at the desired frequencies, the circuit shown in Fig. 3.20 is introduced in this work. Two transmission lines connecting the differential ends at the input and the output are added to the circuit. Both lines are half-wavelength at the fundamental frequency. These lines will work as

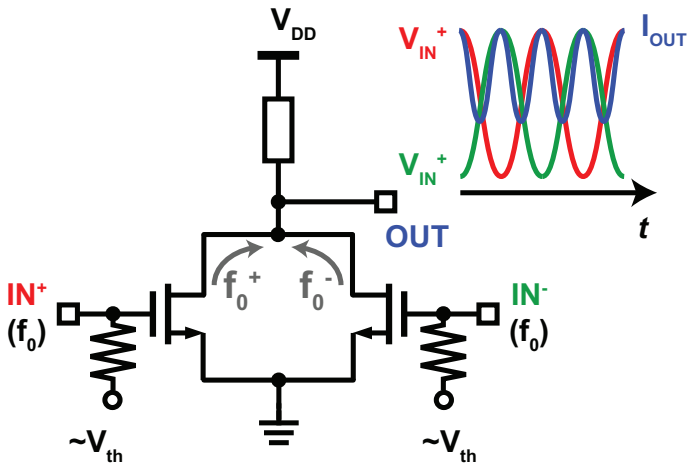


Figure 3.19: Conventional push-push frequency doubler and its operation.

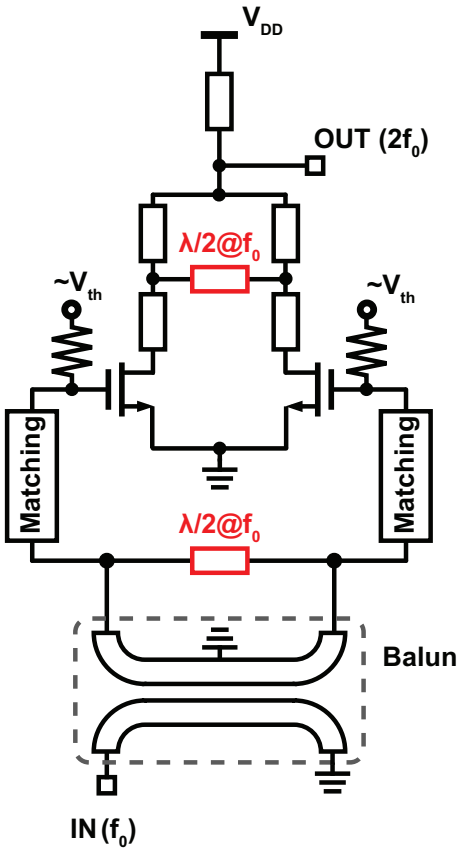


Figure 3.20: Proposed modified push-push frequency doubler.

quarter-wave short stubs at the differential mode of the fundamental frequency having a minimum effect on the desired differential mode. The matching conditions can be im-

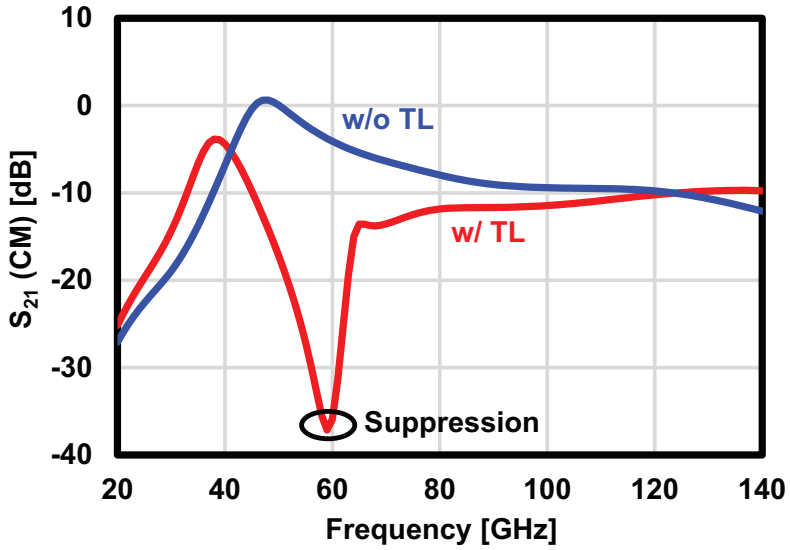


Figure 3.21: The effect of the balun mismatch compensation line on the common mode signal.

proved by connecting series transmission lines to the drain of each transistor. The main improvement obtained by adding the two half-wavelength lines can be observed at the common-mode of the fundamental frequency as shown in Fig. 3.21. Each line works as two open quarter-wavelength stubs at common-mode connected to both ends. Hence, the fundamental common-mode component will be effectively shorted and suppressed at the input and the output. The simulated S_{21} shows that a common-mode suppression of more than 30dB can be achieved by the introduced technique, reducing the effect of the balun mismatch to the minimum.

The complete schematic of the push-push doubler including the matching networks is shown in Fig. 3.22. Additional open stubs are added to improve the matching at the output. The chip was also fabricated in 65nm CMOS technology and the micrograph is shown in Fig. 3.23. The total area is around $0.38mm^2$.

The Doubler was measured using the same setup used for tripler which is previously shown in section 3 (Fig. 3.11). The measured output power as shown in Fig. 3.24 is around 1.1dBm. The improvement at the center frequency compared to the conventional structure is around 3dB. However, the bandwidth of operation is much narrower due to the dependency on the line electrical length. This disadvantage limits the usage of the doubler to LO generation circuits for fixed LO frequency. The fundamental rejection ratio shown in Fig. 3.25 is also improved considerably compared to the conventional case. The power in/out measured characteristics are shown in Fig. 3.26. The conversion gain can exceed

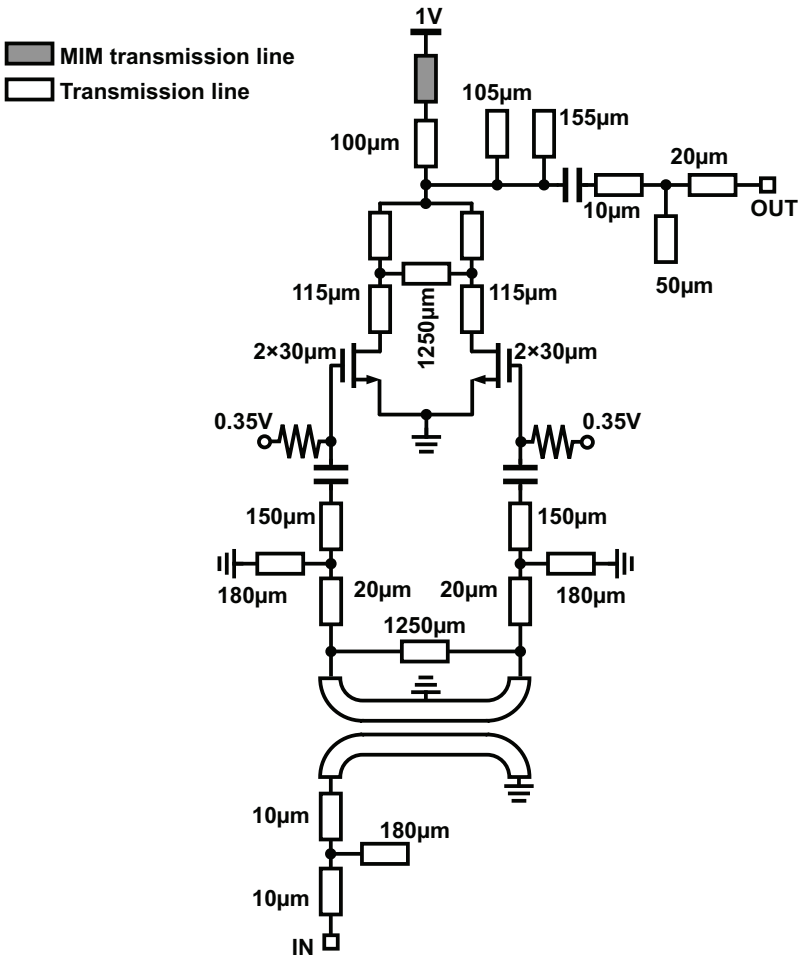


Figure 3.22: Proposed push-push frequency doubler detailed schematic.

0dB at the optimal input power condition including the balun losses.

Table 2 compares the performance of proposed doubler circuits with the state-of-the-art CMOS frequency doublers that operate at frequencies around 100GHz. The doubler achieves high conversion gain including the balun losses without the need to apply any amplification.

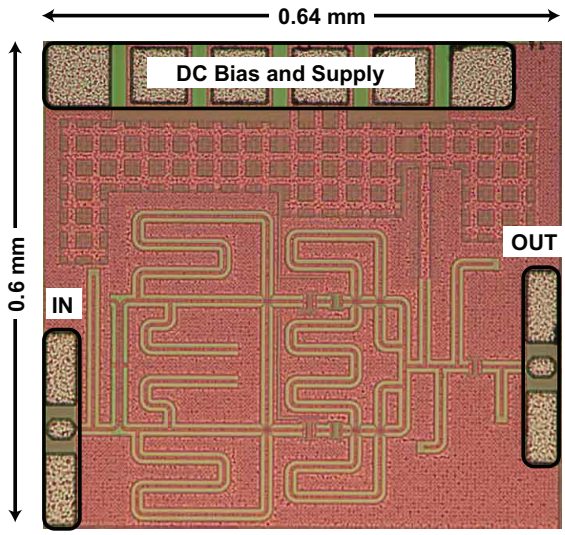


Figure 3.23: Proposed push-push frequency doubler micrograph. (© 2021 IEICE)

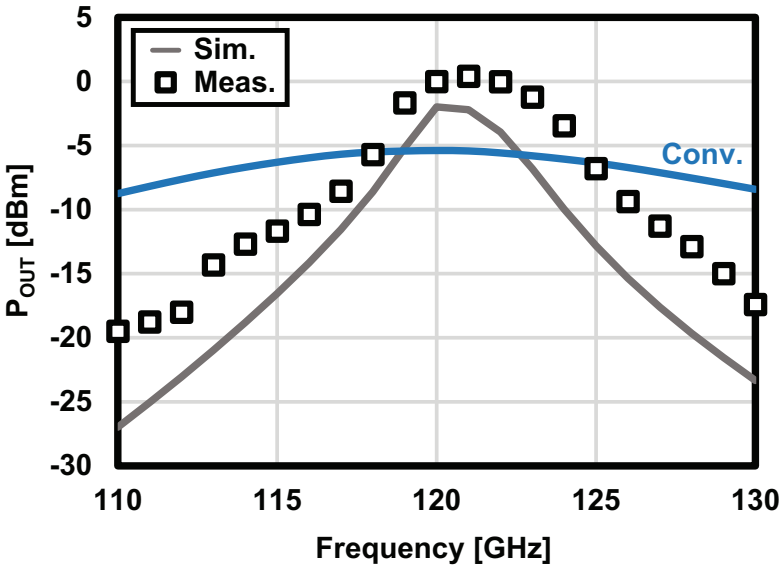


Figure 3.24: Push-push frequency doubler measured and simulated output power.

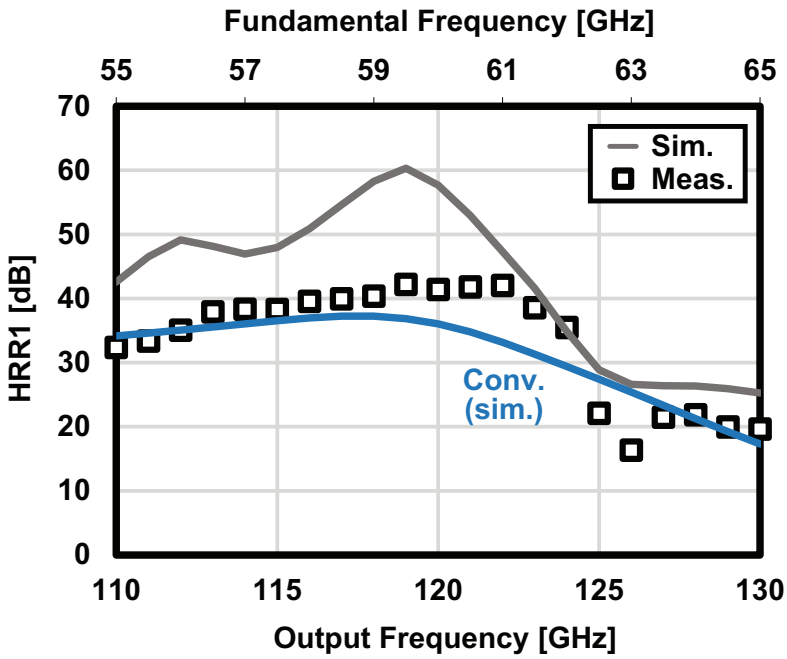


Figure 3.25: Push-push frequency doubler measured and simulated fundamental rejection ratio.

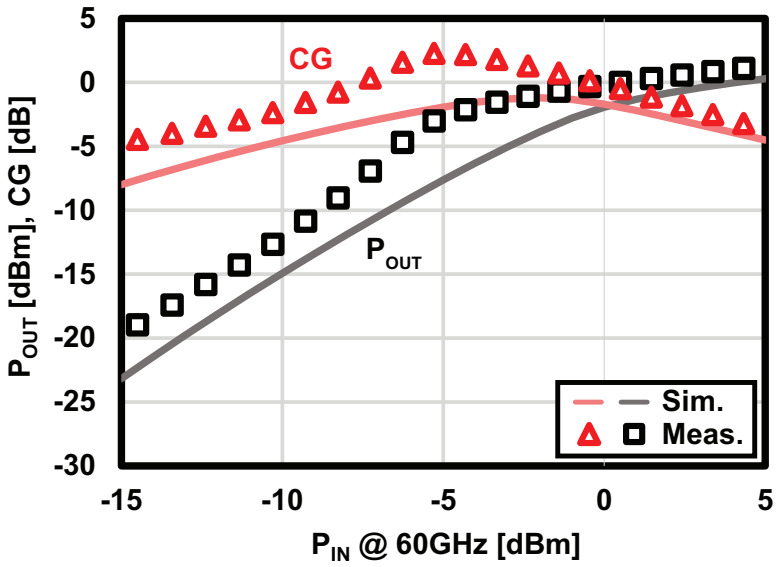


Figure 3.26: Push-push frequency doubler measured and simulated output power and Conversion gain.

Table 3.2: Doubler Performance Comparison

	This Work	**[66]**	**[67]**	**[70]**
Process	65nm CMOS	65nm CMOS	65nm CMOS	65nm CMOS
Frequency [GHz]	118-124	84-103	95-150	73-88
Mult. Factor	×2	×2	×2	×2
Max. CG [dB]	2.3	1.94	−8	0.8
Max. P_{OUT} [dBm]	1.1	6.94	3	−3.2
HRR1 [dB]	34.8-42.2	N/A	30-42.4	> 19
HRR1 + P_{OUT} [dB]	35.9	N/A	33	15.8
P_{DC} [mW]	< 32	< 82.8	< 22.8	14
Area [mm^2]	0.38	0.25	0.24	0.22

Chapter 4

Subharmonic-Mixer-Based 300GHz-Band Transceiver

To achieve reliable wireless communication at 300GHz-band using CMOS transceivers, the mixer-last TX mixer-first RX is the most suitable option so far as explained in Chapter 1. As a result, the mixer performance becomes the most dominant when the system SNDR calculations take place. Most of the recent CMOS 300GHz-band systems are built around unconventional mixing (frequency conversion) circuitry to meet the linearity and noise requirements of the link budget [34, 35, 37–40, 45]. In addition, subharmonic mixing which enables reasonable frequency plan for IF and LO as explained in section 2.2 is preferable for simpler, smaller, and low-power transceiver chip. However, novel design techniques are required to fit a subharmonic mixer into the system including conversion gain improvement, linearity enhancement, and harmonic suppression techniques.

This chapter presents a subharmonic-mixer-based 300GHz-band transceiver that achieves wideband wireless communication without consuming large area and high DC power. In addition, the design details of the subharmonic mixer and its advantages over the conventional ones are discussed.[1] [2]

[1]The sections 4.1, 4.2, and 4.3 are based on "A 300GHz Wireless Transceiver in 65nm CMOS for IEEE802.15.3d Using Push-Push Subharmonic Mixer" [42], by the same author, which appeared in the Proceedings of IEEE/MTT-S International Microwave Symposium (IMS), © 2020 IEEE.

[2]The sections 4.4 and 4.5 are based on "64QAM wireless link with 300GHz InP-CMOS hybrid transceiver" [74], by the same author, which appeared in the IEICE Electronics Express, © 2021 IEICE. The material in this paper was presented in part at the IEICE Electronics Express [74], and some of the figures of this paper are reused from [74] under the permission of the IEICE.

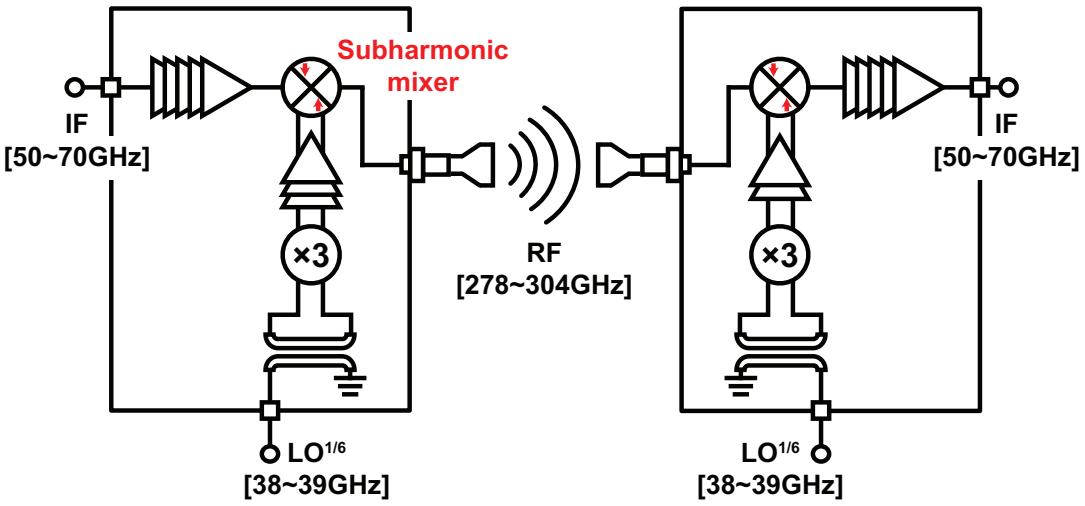


Figure 4.1: Proposed transceiver block diagram.

4.1 Proposed Transceiver Architecture

The proposed transceiver architecture is shown in Fig. 4.1. The mixer-last TX mixer-first RX topology is adopted with the IF frequency bandwidth covering most of the V-band. The high IF frequency reduces the required LO input frequency of the mixer to less than 120GHz. To satisfy the requirements of high-order modulations, high-linearity and low-conversion-loss subharmonic mixer circuit is proposed.

In addition to the proposed mixer, the transceiver consists of IF amplifiers (around 23dB gain), LO fundamental blocking tripler with balun mismatch cancellation and neutralized differential buffers. The fundamental blocking tripler input signal (38 to 39GHz) is tripled to generate the required differential $LO^{1/2}$ input of the subharmonic mixer. Fundamental and second-harmonic rejection techniques are proposed to suppress the undesired frequency components at the output of the tripler reducing the required number of high frequency buffering stages to only two in the RX and three in the TX. The mixer converts the IF signal (50-70GHz) using the second harmonic of the $LO^{1/2}$ signal to the RF frequency (278-304GHz) and vice versa. The operating RF frequency band covers several IEEE Std. 802.15.3d channels as shown in Fig. 4.2.

The main design point in this system is to achieve good mixer linearity and conversion gain while providing suitable IF and LO signals with low DC power consumption.

4.2 Circuit Implementation

In this section, the circuit design details of each block are explained.

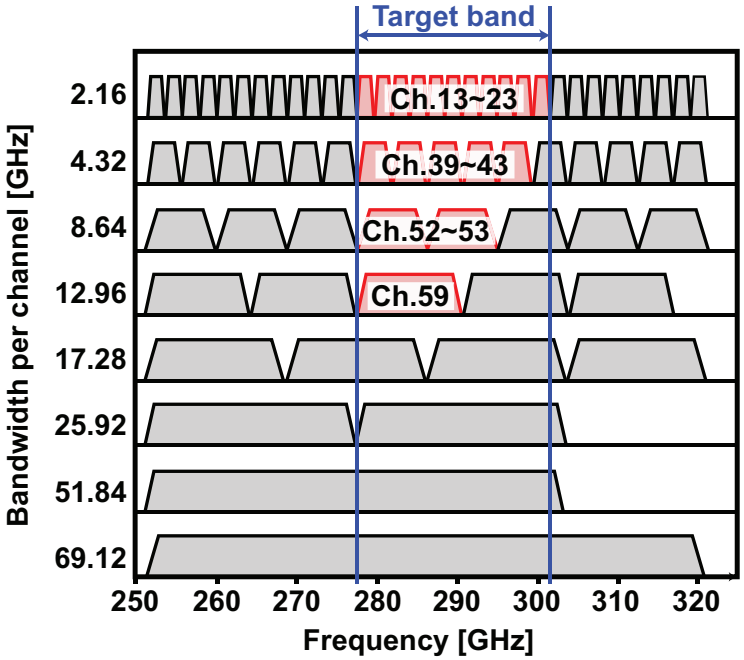


Figure 4.2: Target frequency band and the covered IEEE Std. 802.15.3d channels.

4.2.1 Push-Push Subharmonic Mixer

Many of the recent works on millimeter-wave CMOS transceivers in the literature utilize simple passive mixers especially for up-conversion to provide good conversion gain, linearity, and bandwidth while avoiding the design complexity and the power consumption issues of the active types [2, 3, 5, 6, 10]. It also gets more difficult to achieve good linearity at high frequencies with the active mixers.

Apart from the fundamental mixing operation, there are two main issues that make it difficult to use the conventional simple single transistor mixer or the double-balanced mixer at frequencies that exceed 200GHz. The first issue is that getting good conversion gain and output power requires high LO power to drive the mixer. However, the CMOS amplifiers cannot simply provide several dBm at 240GHz for example [35, 39]. The other issue is that the effect of gate parasitics will be huge, causing the conversion gain and the output power to degrade. These two issues were faced by introducing multiplier-based mixers where both the LO and the IF signals are applied to the same input port [38, 40]. The output power of these mixers is high enough to achieve reliable communication at the 300GHz-band, but the IF frequency is too high, the scond harmonic components are in-band, and the operation is uni-directional, so the antenna sharing without lossy RF switches is not possible.

Reducing both the IF and LO frequency to the bands that are suitable for CMOS am-

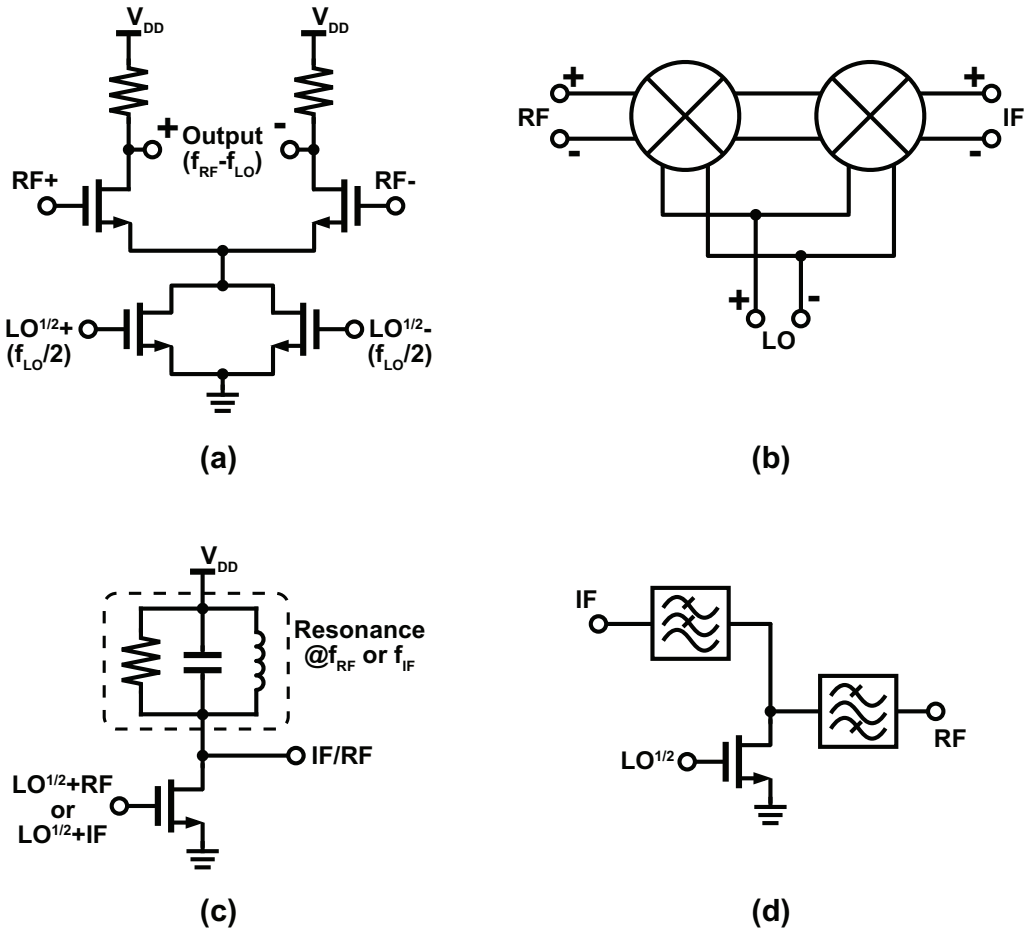


Figure 4.3: Conventional CMOS subharmonic mixer circuits. (a) Push-push LO doubling, (b) 2-stage mixing, (c) transconductance mixer, and (d) resistive mixer.

plification is possible using subharmonic mixing as discussed in section 2.2. Conventional subharmonic mixers that are implementable using CMOS are illustrated in Fig. 4.3. The push-push doubler which is commonly used in millimeter-wave design can be placed in the mixer as shown in Fig.4.3(a). However, the active nature of this mixer limits the linearity due to the cascode structure, so higher supply voltages are usually used as in [75–77]. 2-stage mixing is another way to achieve the subharmonic operation, where two cascading mixers with the same LO frequency up-/down-convert the signal twice as shown in Fig. 4.3(b). Since active mixer implementation with cascoded transistors is required to avoid large cascading losses [78, 79], the same linearity issue can be expected. Transconductance mixers shown in Fig.4.3(c) utilize the third order non-linearity of the transistor to extract the subharmonic mixing components at the output using matching or an LC tank. Both LO and IF are applied to the mixer gate which means that the bi-directional operation is not possible. Many undesired harmonics also appear at the output affecting

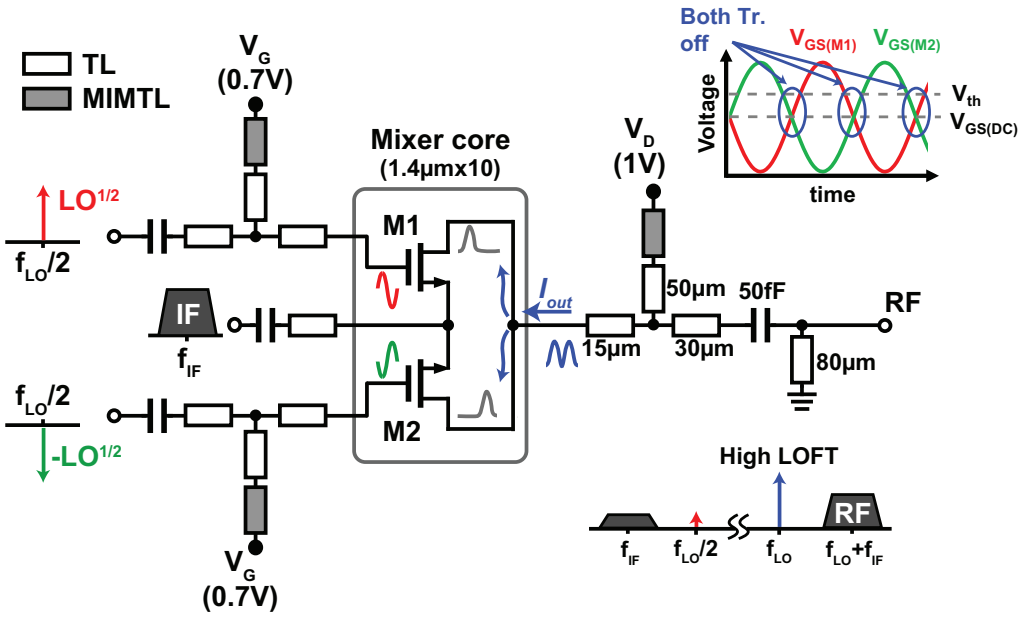


Figure 4.4: Schematic and operation of the push-push subharmonic mixer.

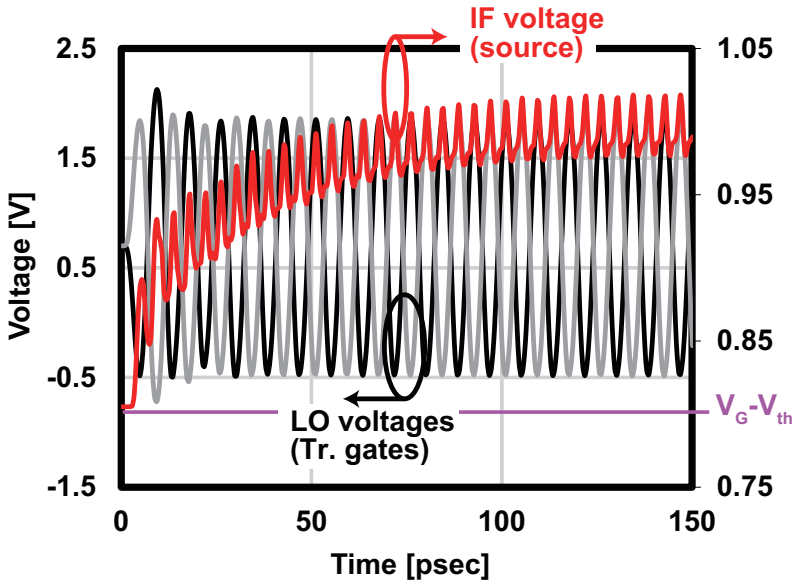


Figure 4.5: Transient simulation of the source voltage.

the linearity [37, 80, 81]. Fig.4.3(d) shows the resistive mixer typical architecture. the LO is "injected" to the gate of the transistor, and the IF/RF signals are filtered at the output with the required non-linearity order. The linearity of this architecture is better than the mentioned three subharmonic mixers, and the operation is completely passive. However, wideband matching with high isolation is required to achieve the desired performance [82, 83].

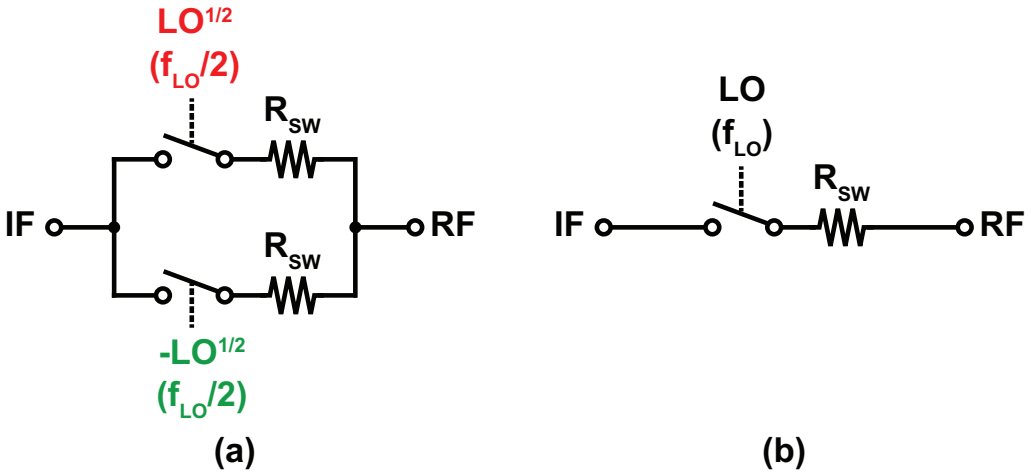


Figure 4.6: (a) Switching operation of the proposed mixer and (b) the equivalent circuit with second harmonic switching.

In this work, we introduce a passive subharmonic mixer with good conversion gain, wide bandwidth, and acceptable linearity that supports bi-directional operation to enable antenna sharing between the TX and the RX.

The introduced subharmonic mixer has the push-push frequency multiplier as a starting design point, The push-push doubler has two transistors with connected drains and sources, but the input is applied differentially to their gates. The output current has twice the frequency of the input LO signal. A DC blocking capacitor is added to the source node and the IF signal is applied to the sources through that capacitor as shown in Fig. 4.4. The V_{GS} is set to a value that is slightly smaller than the threshold voltage of the transistor. The source voltage is controlled by applying the desired voltage to the drain, as the high-cycle of the LO signal passes the current to charge the DC blocking capacitor to the drain voltage level. Fig. 4.5 shows the source voltage increase due to the high-cycles of the LO signal. Having the V_{GS} lower than the threshold will create some off periods in the current of the mixer (Fig. 4.6(a)), and that will result in a switching operation close to that of the fundamental mixer, but at twice the frequency of LO (Fig. 4.6(b)). Higher conversion gain can be expected from this mixer compared to the other subharmonic ones, but the usage of the source node limits the size of the transistors and the output power as a result. The IF and the LO ports in this mixer are separated enabling the desired bi-directional operation.

By increasing both the gate and the source voltage levels, the depletion region inside the CMOS transistor expands as the drain and the source voltage values are higher than the voltage of the grounded transistor body as illustrated in Fig. 4.7. That will affect the

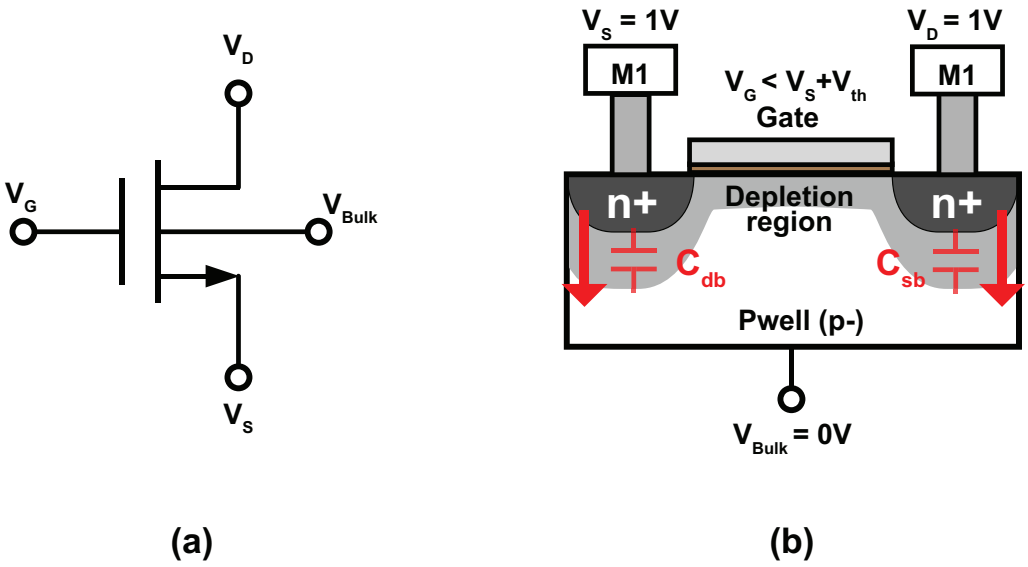


Figure 4.7: Proposed mixer biasing technique

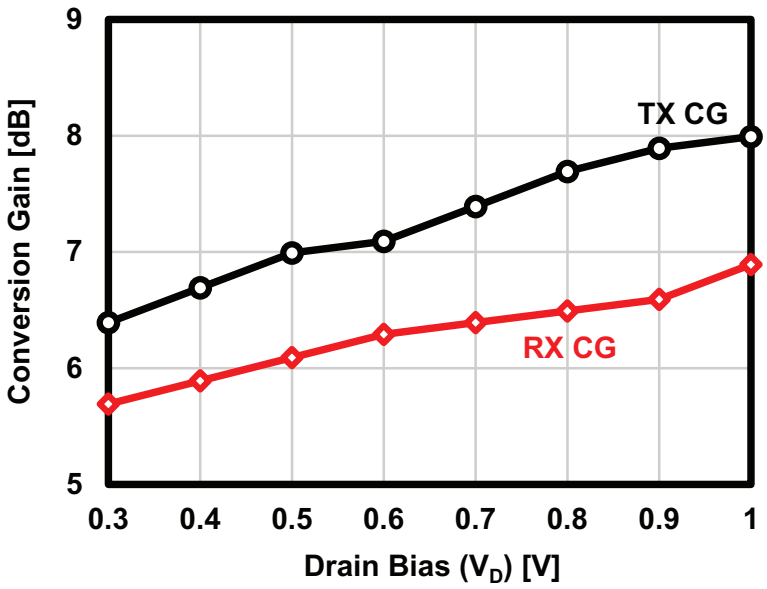


Figure 4.8: Measured conversion gain improvement due to the reduced junction capacitance.

capacitance of the reverse-biased source-bulk P/N junctions defined as:

$$C_{\mathrm{SB}} = \frac{WL_{\mathrm{diff}}C_{\mathrm{J}}}{\left(1+\frac{V_{\mathrm{SB}}}{\phi_{\mathrm{j}}}\right)^{m_{\mathrm{j}}}} \tag{4.1}$$

where WL_{diff} is the diffusion area, ϕ_{j} is the built-in junction potential, and V_{SB} is the

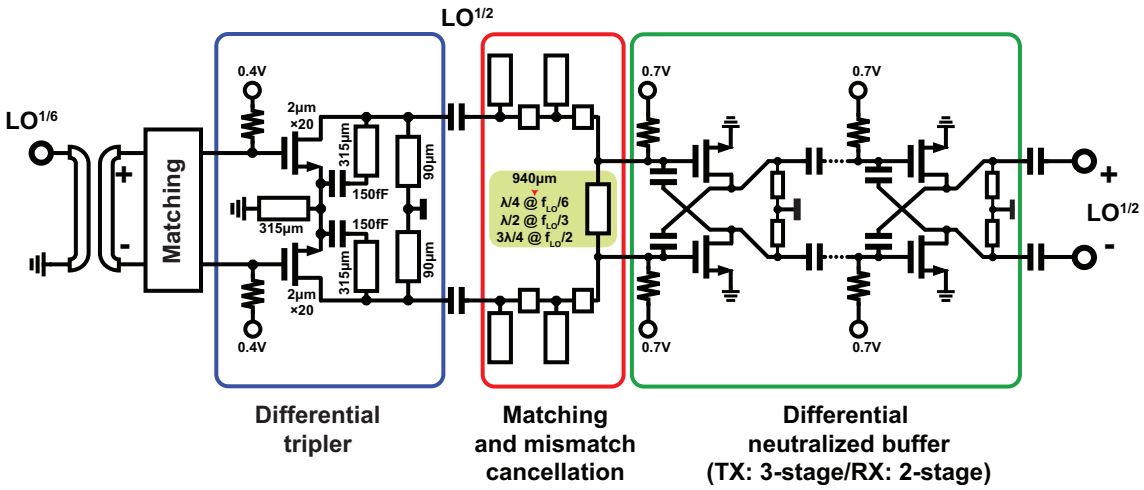


Figure 4.9: LO chain circuit schematic.

source-to-bulk voltage and

$$C_{\mathrm{J}} = \sqrt{\frac{\varepsilon_{\mathrm{Si}} q N_{\mathrm{b}}}{2\phi_{\mathrm{j}}}} \tag{4.2}$$

here, $\varepsilon_{\mathrm{Si}}$ is the dielectric constant of silicon, q is the electronic charge constant, and N_{b} is the bulk dopant concentration. The same equation can be used to calculate the drain-bulk capacitance and the P-well related junction capacitance as well.

It is quite clear from (4.1) that increasing the source/drain voltage while keeping the bulk grounded reduces the junction capacitance. The conversion gain improves accordingly as shown in the measurement results in Fig. 4.8.

By increasing the source-bulk voltage, the threshold voltage of the transistor changes due to the body effect according to the following equation:

$$V_{\mathrm{th}} = V_{\mathrm{th0}} + \gamma\left(\sqrt{V_{\mathrm{SB}} + 2\varphi_{\mathrm{F}}} - \sqrt{2\varphi_{\mathrm{F}}}\right) \tag{4.3}$$

where V_{th} is the threshold voltage, V_{th0} is the threshold at zero-bias, γ is the body effect parameter, V_{SB} is the source-body voltage and φ_{F} is the surface potential. The threshold change is compensated by optimizing the gate bias voltage.

4.2.2 LO Chain

The LO chain consists of the differential frequency tripler with fundamental and second harmonic suppression explained in the Sub-section 3.2.2, and differential neutralized amplifiers. Thanks to the high output power and the good harmonic suppression of the

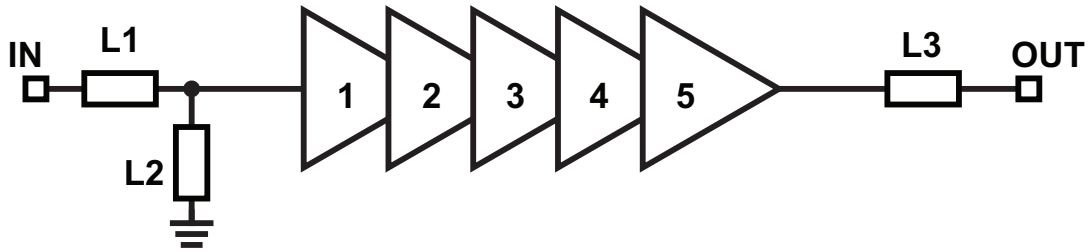


Figure 4.10: 5-stage IF amplifier.

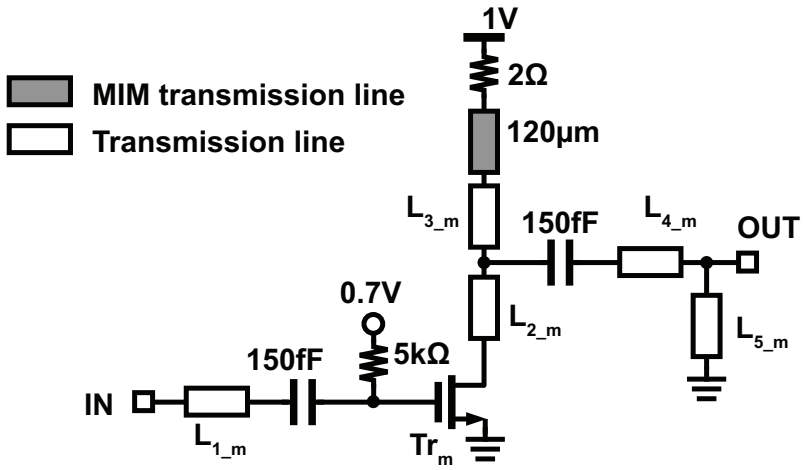


Figure 4.11: V-band IF amplifier single-stage schematic.

proposed tripler, the number of differential LO buffers is limited to 3 in the TX and 2 in the RX. As a result, the power consumption and the chip area are kept small compared to the prior works. Fig.4.9 shows the detailed schematic of the LO chain.

Table 4.1: TX IF amplifier detailed parameters

1st stage		2nd stage		3rd stage		4th stage		5th stage	
Tr_1	40um	Tr_2	40um	Tr_3	40um	Tr_4	80um	Tr_5	80um
L_{1_1}	100um	L_{1_2}	25um	L_{1_3}	130um	L_{1_4}	80um	L_{1_5}	30um
L_{2_1}	375um	L_{2_2}	320um	L_{2_3}	120um	L_{2_4}	10um	L_{2_5}	10um
L_{3_1}	320um	L_{3_2}	365um	L_{3_3}	180um	L_{3_4}	400um	L_{3_5}	450um
L_{4_1}	115um	L_{4_2}	120um	L_{4_3}	50um	L_{4_4}	40um	L_{4_5}	10um
L_{5_1}	150um	L_{5_2}	190um	L_{5_3}	130um	L_{5_4}	240um	L_{5_5}	190um

Table 4.2: RX IF amplifier detailed parameters

1st stage		2nd stage		3rd stage		4th stage		5th stage	
Tr_1	2x20um	Tr_2	2x20um	Tr_3	2x20um	Tr_4	2x20um	Tr_5	2x20um
L_{1_1}	200um	L_{1_2}	45um	L_{1_3}	205um	L_{1_4}	160um	L_{1_5}	180um
L_{2_1}	180um	L_{2_2}	345um	L_{2_3}	275um	L_{2_4}	70um	L_{2_5}	165um
L_{3_1}	350um	L_{3_2}	245um	L_{3_3}	95um	L_{3_4}	260um	L_{3_5}	320um
L_{4_1}	10um	L_{4_2}	105um	L_{4_3}	80um	L_{4_4}	380um	L_{4_5}	10um
L_{5_1}	315um	L_{5_2}	140um	L_{5_3}	230um	L_{5_4}	360um	L_{5_5}	380um

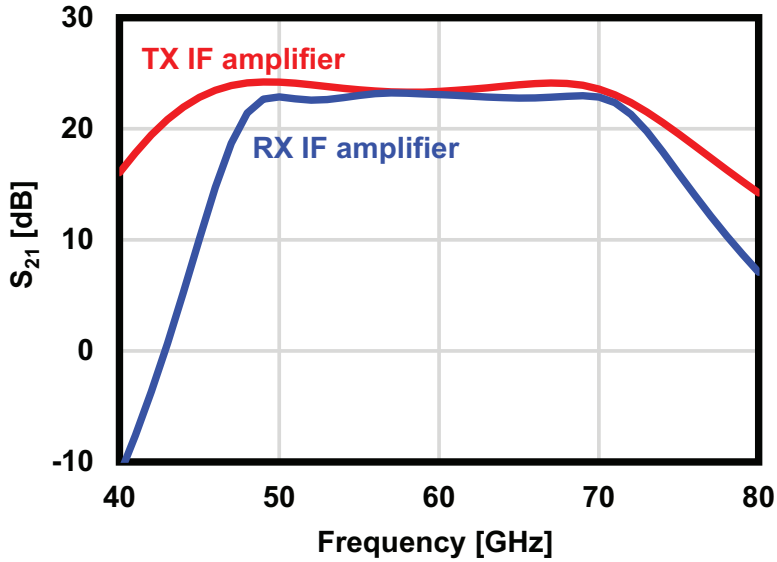


Figure 4.12: Simulated IF amplifiers gain characteristics.

4.2.3 IF Amplifiers

Both TX and RX IF amplifiers are designed to cover a large part of the V-band. Staggered tuning technique is used to cover the wide frequency range from 50GHz to 70GHz. The TX IF amplifier is designed to achieve high linearity so that it can drive the mixer properly without degrading the system SNDR, and the RX IF amplifier is designed to achieve low noise figure to minimize the amplifier effect on the system overall noise performance. Transmission lines are used to implement the loads and the matching networks. The amplifier schematic is shown in Fig. 4.10. Each stage is a common-source amplifier with a 2Ω resistor that connects the drain network to the supply voltage to improve the stability of the amplifier. The inter-stage matching is realized by adding a short stub between every

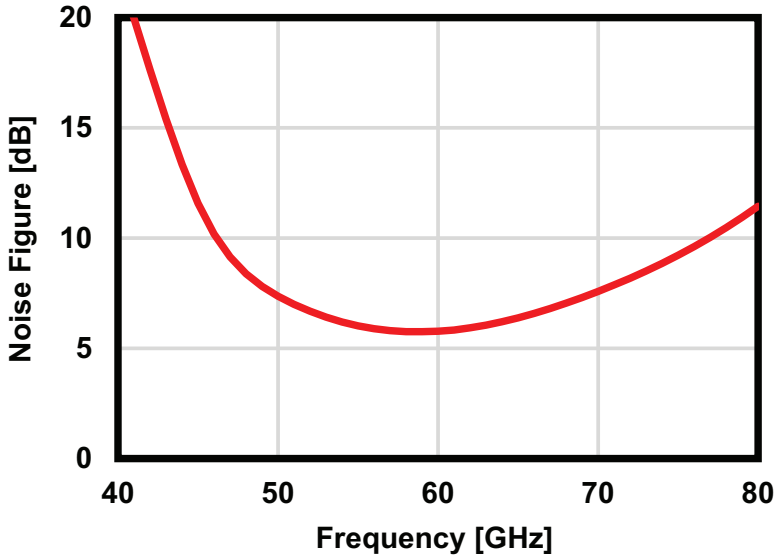


Figure 4.13: Simulated RX IF amplifier noise figure.

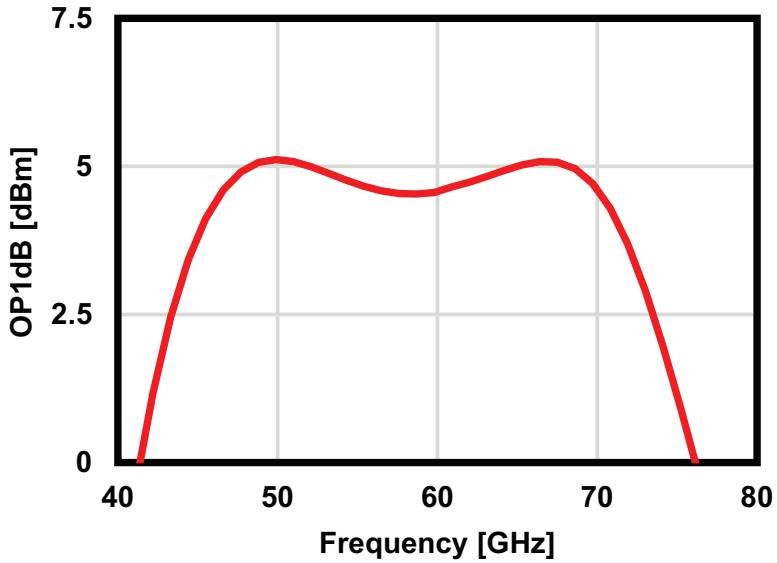


Figure 4.14: Simulated TX IF amplifier OP1dB.

two stages. The transistor sizes and the transmission line lengths for the TX IF amplifier are listed in table 4.1, and the values of these parameters for the RX IF amplifier are listed in table 4.2. The staggered tuning is implemented by optimizing the transistor sizes, the load transmission line lengths, and the inter-stage matching frequencies. More than 20dB gain and a bandwidth of more than 20GHz are achieved for both TX and RX IF amplifier

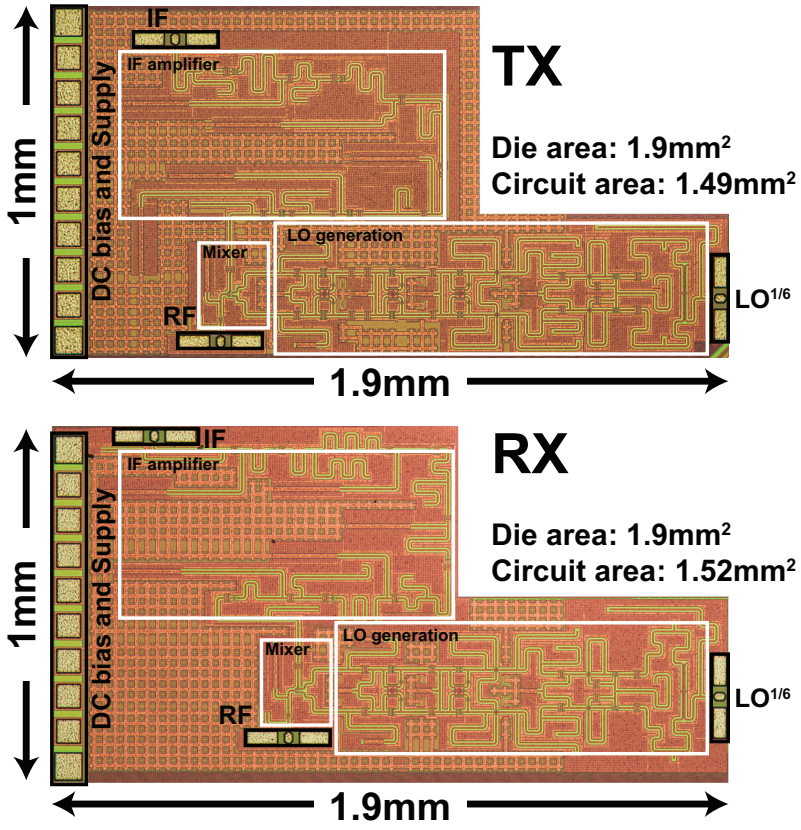


Figure 4.15: CMOS TX and RX chip photos. (© 2020 IEEE)

cases as shown in Fig. 4.12 with the TX one achieving higher gain and bandwidth due to the larger transistor sizes. Such high gain is essential to overcome any external losses coming from PCB implementation and measurement equipment. The noise figure of the RX IF amplifier is around 6dB at the band of interest as the simulation results show in Fig. 4.13. The simulated OP1dB of the TX IF amplifier is shown in Fig 4.14, and around 5dBm is achieved at most of the target frequencies.

4.3 Measurement Results of the CMOS Transceiver

The proposed transceiver was fabricated using 65nm CMOS technology. Fig. 4.15 shows the die photos of TX and RX. The chip size of both TX and RX is 1.9mm^2. Fig. 4.16 shows the measured conversion gain of TX (9dB) and RX (6dB), excluding PCB loss. The de-embedded RX mixer conversion gain is around -16.5dB. Fig. 4.17 shows the input/output power characteristics of the TX. The OP1dB of the TX mixer is around -16dBm.

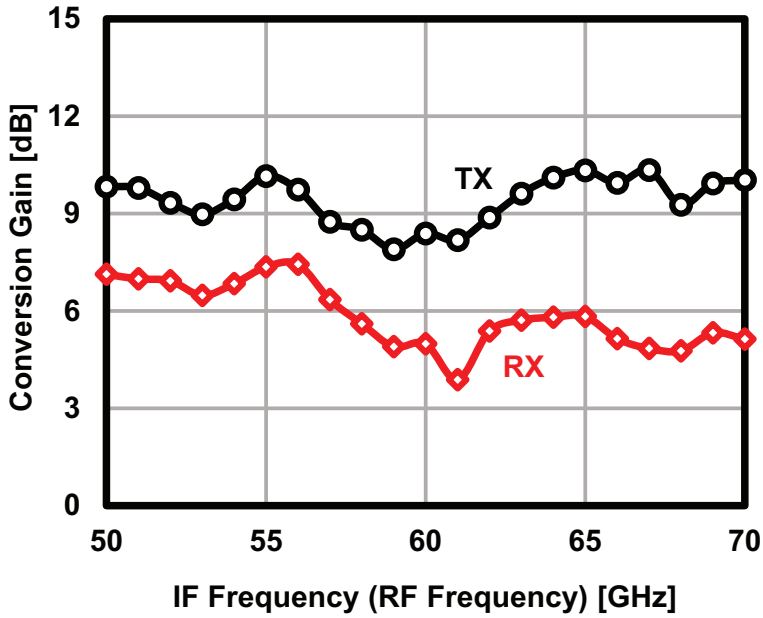


Figure 4.16: Measured TX and RX conversion gain values.

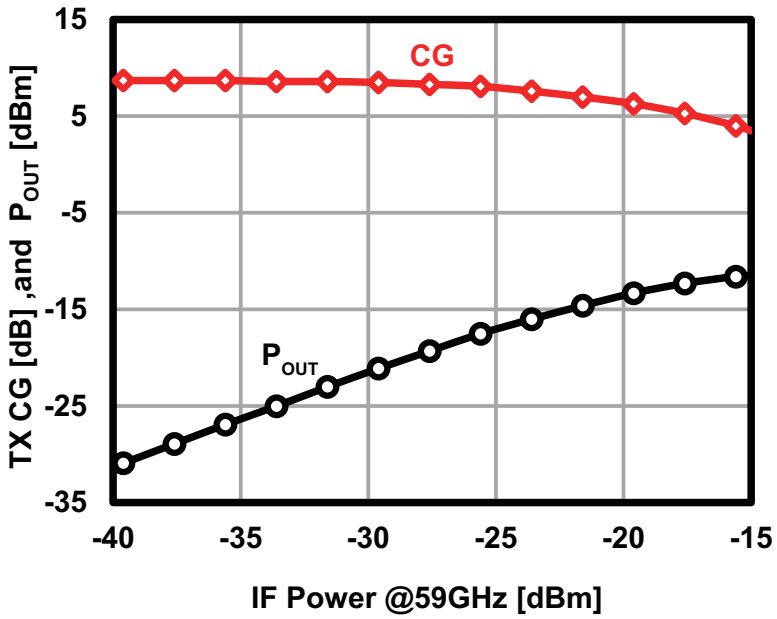


Figure 4.17: Measured TX input/output power characteristics.

A PCB was implemented to evaluate the OTA performance of the transceiver. The PCB photo is shown in Fig. 4.18. IF and LO signals are applied to the PCB using

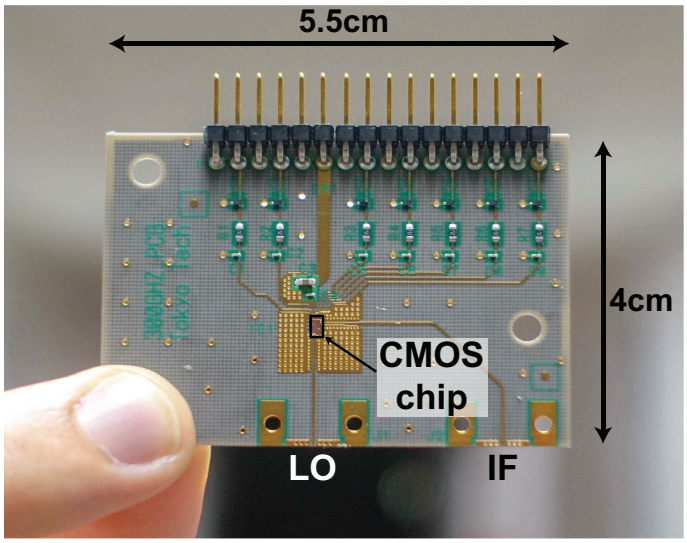


Figure 4.18: PCB for OTA evaluation. (© 2020 IEEE)

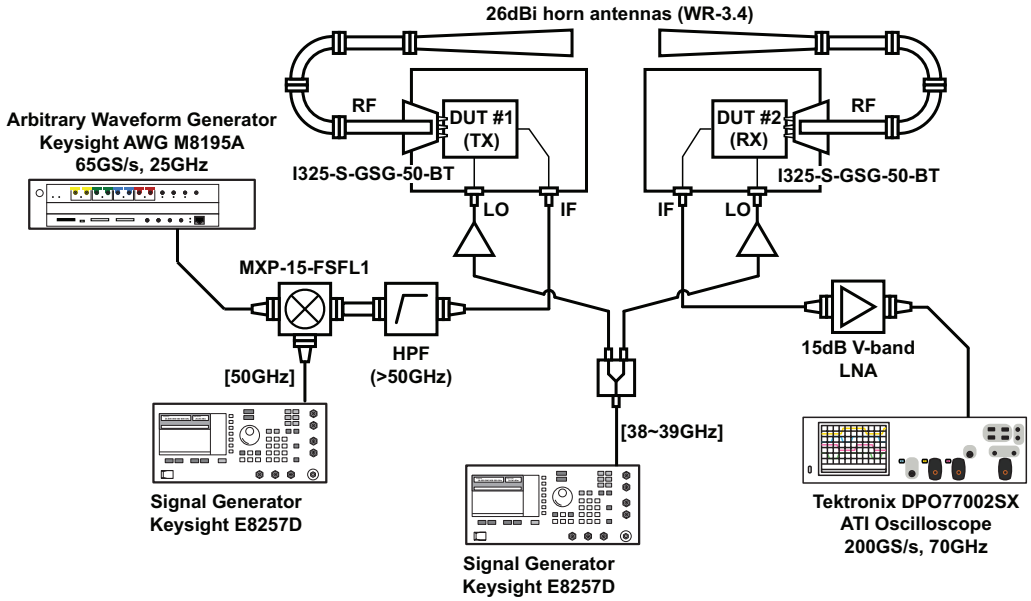


Figure 4.19: CMOS transceiver measurement setup.

end launch V-band connectors. The chip is connected to the PCB using wire bonding except for the RF inputs and outputs due to the huge loss of the bonding wires at 300GHz considering the short wavelength.

The OTA measurement environment of the complete TRX system is illustrated in Fig. 4.19 with the PCB and setup photos shown in Fig. 4.20. 26dBi horn antennas are attached to the TX and RX using waveguide probes that are landed on each chip. The IF sig-

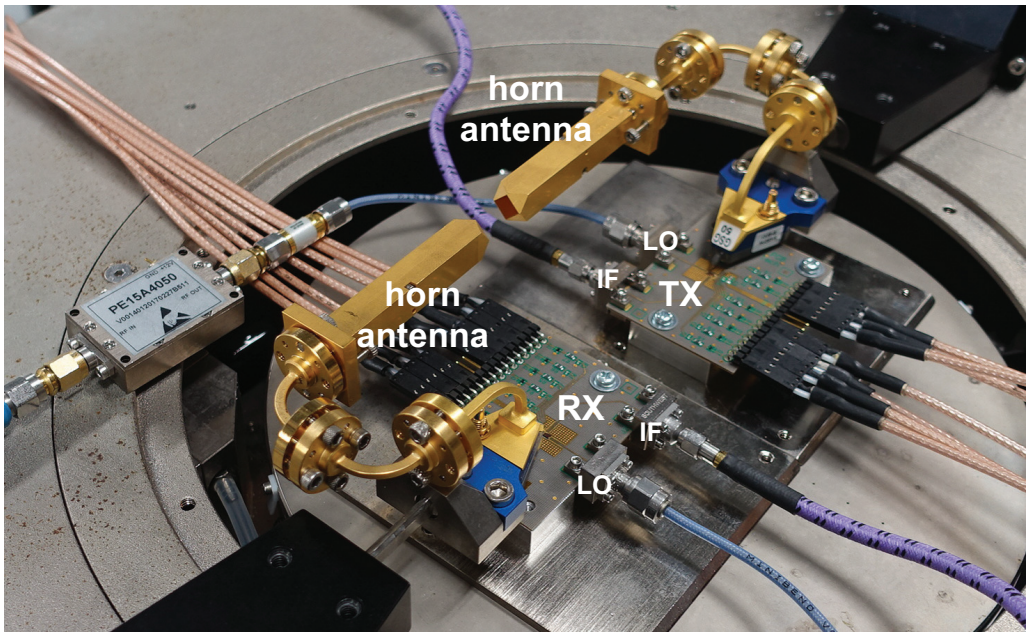


Figure 4.20: CMOS transceiver measurement setup photo. (© 2020 IEEE)

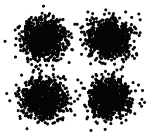
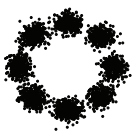
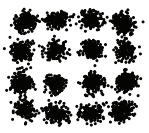
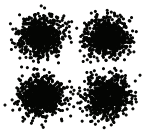
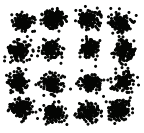
Distance [cm]	1			4	
Center Frequency [GHz]	288			288	
Bandwidth [GHz]	20.86	12.27	7.36	18.4	3.68
Symbol rate [Gbaud]	17	10	6	15	3
Modulation	QPSK	8PSK	16QAM	QPSK	16QAM
TX-to-RX Constellation					
TX-to-RX EVM	-10.12	-14.83	-16.72	-10.21	-16.91
Data rate [Gb/s]	34	30	24	30	12

Figure 4.21: Performance summary for maximum data rate conditions.

nal is generated externally using the Keysight arbitrary wave generator (AWG) M8195A and up-converted using an external V-band mixer. To suppress the LO leak and the image signal of the external mixer, a high pass filter (HPF) is directly connected to the mixer output. The LO signals of both TX and RX are generated from the same signal generator and divided by a power splitter. To compensate for the large PCB loss at the LO frequency, external LO buffers are added to the setup. The output signal of the RX is amplified using an external V-band amplifier to compensate for the wire bonding losses, and the output is observed using the Tektronix DPO77002SX oscilloscope. The mentioned oscilloscope has a 70GHz analog bandwidth that eliminates the need to down-convert the RX output

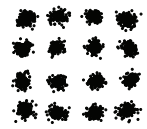
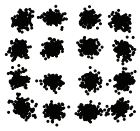
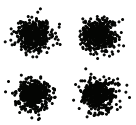
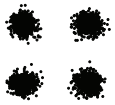
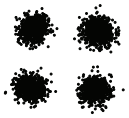
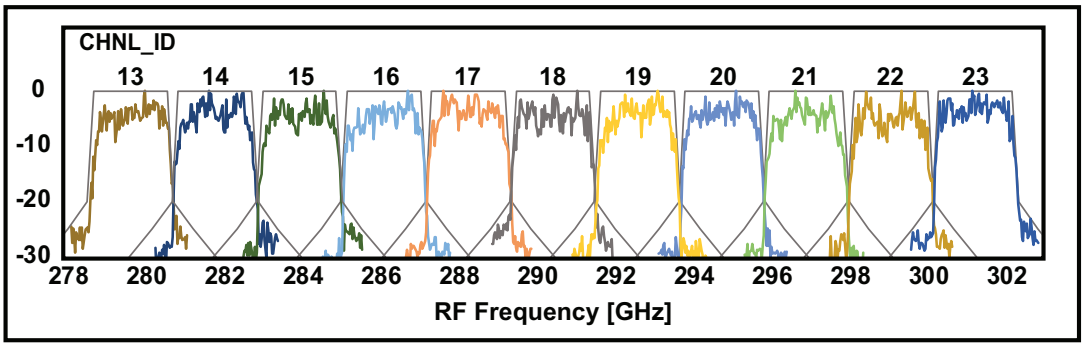
CHNL_ID	17	41	43	52	59
Center Frequency [GHz]	288.36	289.44	298.08	282.96	285.12
Bandwidth [GHz]	2.16	4.32	4.32	8.64	12.96
Symbol rate [Gbaud]	1.76	3.52	3.52	7.04	10.56
Modulation	16QAM	16QAM	QPSK	QPSK	QPSK
TX-to-RX Constellation					
TX-to-RX EVM	-19.57	-17.81	-11.98	-15.05	-13.04
Data rate [Gb/s]	7.04	14.08	7.04	14.08	21.12

Figure 4.22: Performance summary for IEEE Std. 802.15.3d channels.



***CHNL_ID is the channel ID as defined by IEEE Std. 802.15.3d.**
****Roll-off factor of all the measurements is 0.25 as specified by the standard.**

Figure 4.23: Measured spectrum of IEEE Std. 802.15.3d channels having CHNL_ ID 13 to 23.

externally.

The measured constellations and the main performance parameters considering maximum data rate conditions are listed in Fig 4.21. 34Gb/s is the maximum achievable data rate using QPSK with a 17Gbaud symbol rate over 1cm distance. 8PSK and 16QAM are also achieved for lower symbol rates. The TRX data rate was also measured over a 4cm distance separating the horn antennas ends, and 30Gb/s is achieved using QPSK. In addition, the communication using IEEE Std. 802.15.3d was tested for the channels (13–23, 39–43, 52–53, 59). Measured constellations and performance parameters are shown in Fig. 4.22 for sample channels (17, 41, 43, 52, 59) at 1cm distance. The Measured spectrum of channels (13–23) covering the whole TRX bandwidth is shown in Fig. 4.23 as well. Fig. 4.24 and Fig. 4.25 show the relation between the EVM and the baud rate for 1cm and 4cm links, respectively. The power consumption of TX and RX is 0.27mW and 0.14mW, respectively. Table 4.3 and Table 4.4 show the power breakdown of the

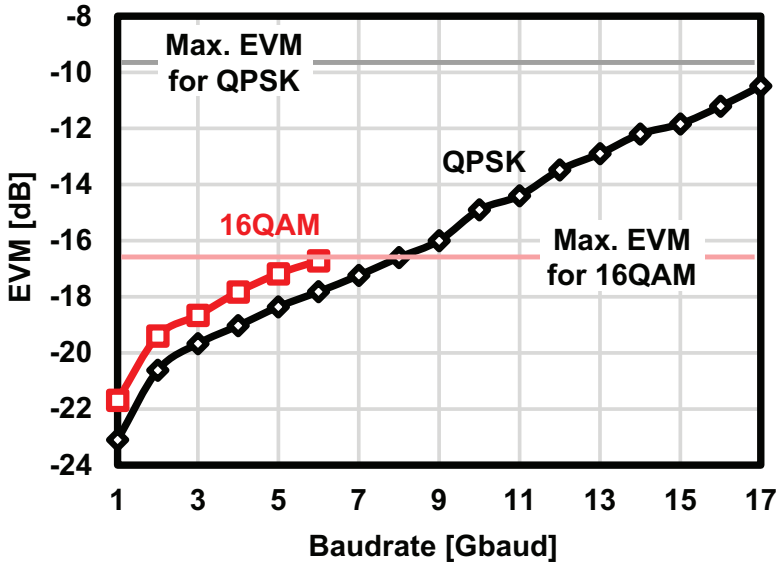


Figure 4.24: Measured EVM versus baud rate for 1cm distance.

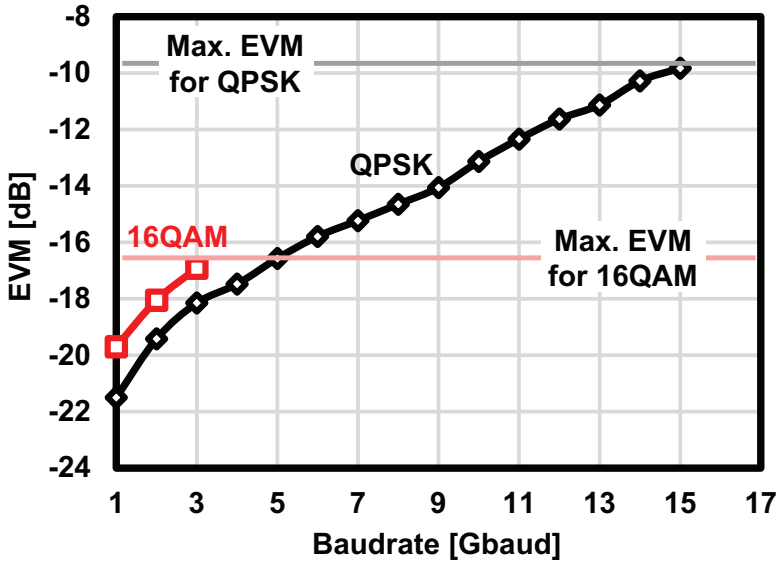


Figure 4.25: Measured EVM versus baud rate for 4cm distance.

transceiver. The performance of the proposed TRX is compared with other >200GHz transceivers in Table 4.5.

Table 4.3: Power consumption of transmitter blocks

Transmitter	
5-stage IF amplifier	104mW
Frequency tripler	40mW
3-stage LO buffer	135mW
Total TX	279mW (measured=272mW)

Table 4.4: Power consumption of receiver blocks

Receiver	
5-stage IF amplifier	40mW
Frequency tripler	40mW
2-stage LO buffer	50mW
Total RX	130mW (measured=135mW)

Table 4.5: CMOS transceiver performance comparison

	[31]	**[20]**	**[38, 39]**	**[40]**	**[34, 35]**	**This work [42]**
Process	130nm SiGe	80nm InP-HEMT	40nm CMOS	40nm CMOS	65nm CMOS	65nm CMOS
RF frequency [GHz]	220–255	278–302	290*	252–279	240*	**278–304**
Evaluated schemes	16QAM	16QAM 64QAM	QPSK 16QAM 32QAM	QPSK 16QAM	QPSK	QPSK 16QAM
Max. baud rate [Gbaud]	23.75	30	14	20	8	17
Max. data rate [Gb/s]	95	120	32	80	16	34
RX mixer CG [dB]	8&	–	-19	–	–	**-16.5**
Standard-based	No	No	No	No	IEEE Std. 802.15.3d	IEEE Std. 802.15.3d
P_{DC} [W]	1.41	TX:4.5$ RX:4.5$	TX:1.4 RX:0.65	TX:0.89 RX:0.9	TX:0.22 RX:0.26	TX:**0.27** RX:**0.14**
Area [mm^2]	TX:N/A RX:N/A	TX:2.44 RX:2.44	TX:5.19 RX:3.15	TRX: 11	TX:2 RX:2	TX:**1.9** RX:**1.9**

* Center frequency. & Including BB amplifier gain. $ Without LO multiplier.

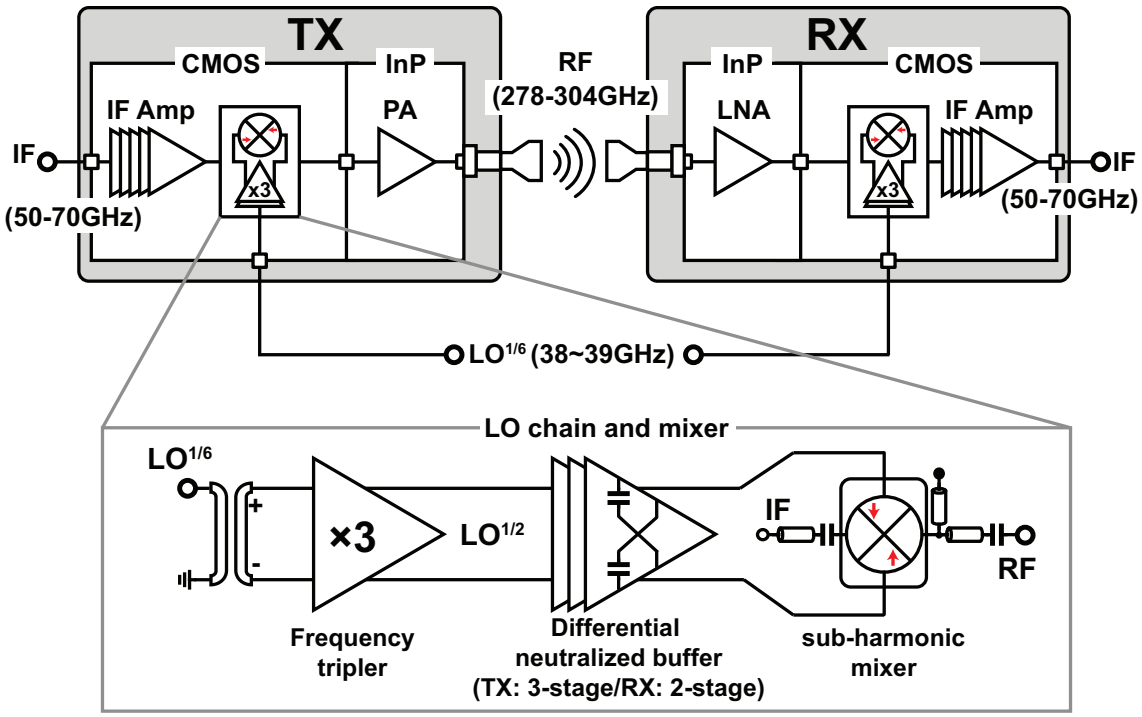


Figure 4.26: Block diagram of the hybrid transceiver with the simplified schematic of the CMOS part.

4.4 InP-CMOS Hybrid Transceiver

As discussed in the earlier sections, the CMOS mixer-last transmitter, mixer-first receiver system has very severe mixer linearity requirements, causing the overall system complexity to increase in order to get a reliable high data rate link.

Many works have demonstrated 300GHz-band links with high data rates up to 120Gb/s using compound semiconductors as in [20–27, 84, 85] as the high $f_{\max}$ makes it possible to design PAs and LNAs with high gain and good linearity resulting in an excellent EVM performance. However, the compound semiconductor process-based systems are costly, very difficult to integrate, and large-scale digital circuits are not feasible in most cases reducing the system's overall feasibility.

In this section, a hybrid transceiver that has the CMOS part which improves the integration between the transceiver front-end and the baseband circuitry, and the InP-HEMT part that provides the gain, linearity, and noise figure improvement at the transmitter output and the receiver input. In other words, a CMOS transceiver is used to up- and down-convert the IF signal to and from 300GHz, and InP-HEMT amplifiers are placed as PA and LNA. One of the biggest challenges facing the hybrid system is the difficulty of the OTA link evaluation before implementation. The direct implementation of the CMOS-

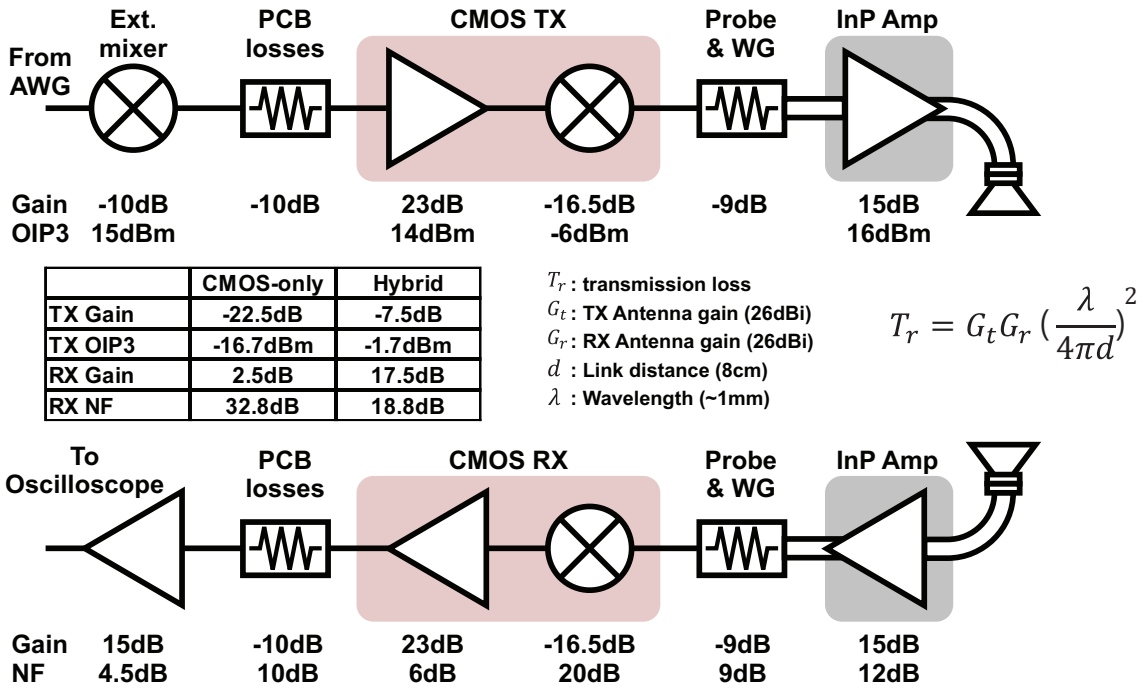


Figure 4.27: Detailed performance parameters used to calculate the SNDR of the hybrid transceiver.

InP connection on a board or in a module for link evaluation is not a practical choice at 300GHz-band due to the limited acceptable connection methods that can be used to avoid having huge losses. To tackle this issue, a measurement setup similar to the one used in the previous section is adopted for OTA measurement.

The transceiver system used to evaluate the wireless link is shown in Fig. 4.26. The RF frequency band from 278GHz to 304GHz is covered by up-converting the 50–70GHz IF band using a tripled LO signal that can be tuned between 38–39GHz. The subharmonic mixer utilizes the second harmonic of the 114–117GHz LO input. The CMOS part consists of the mentioned subharmonic mixer, V-band IF amplifier, tripler, and LO buffers as explained in Section 4.1. The InP-HEMT amplifiers are designed using power combining to improve the overall linearity [86]. The amplifiers are also implemented into waveguide modules with minimized connection losses.

The improvement on the SNDR by adding the InP-HEMT amplifiers to the CMOS system is shown in Fig. 4.27. An 8cm distance is considered in this calculation with 26dBi antenna gain for both transmitter and receiver antennas. A 5Gbaud symbol rate is used to evaluate the SNDR here using the following equation:

$$SNDR = \frac{P_{\mathrm{RX(OUT)}}}{N_{\mathrm{RX}} + IM3} \tag{4.4}$$

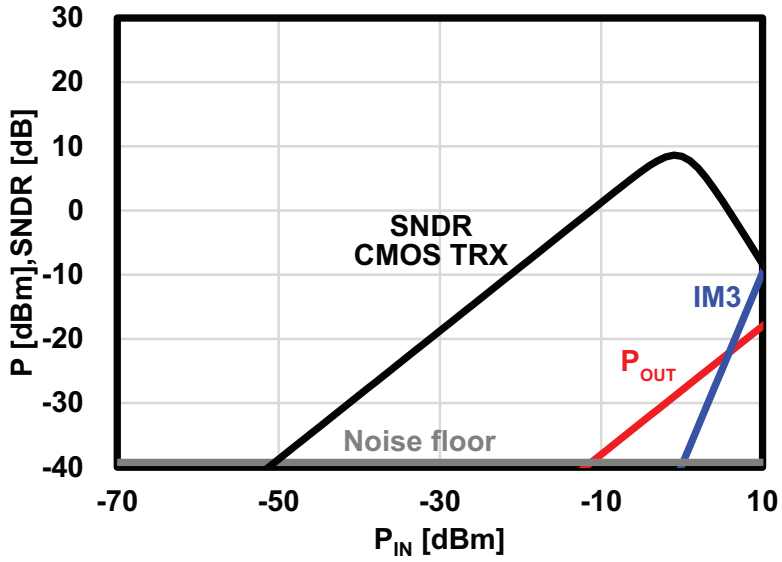


Figure 4.28: Calculated SNDR of the CMOS-only TRX (symbol rate = 5Gbaud).

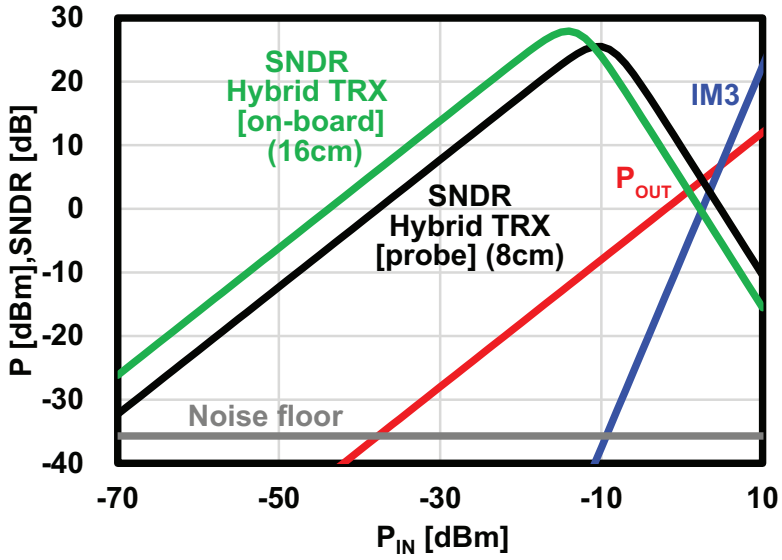


Figure 4.29: Calculated SNDR of the hybrid transceiver (symbol rate = 5Gbaud).

where $P_{\mathrm{RX(OUT)}}$ is the signal output power of the receiver, and N_{RX} is the noise floor at the receiver output. The parameters of each component are estimated using simulations and de-embedded measurement results. From this calculation, it can be observed that the 15dB InP amplifier gain increases the transmitter output power, and hence, the power at the receiver antenna. The receiver gain is increased by the amplifier gain and

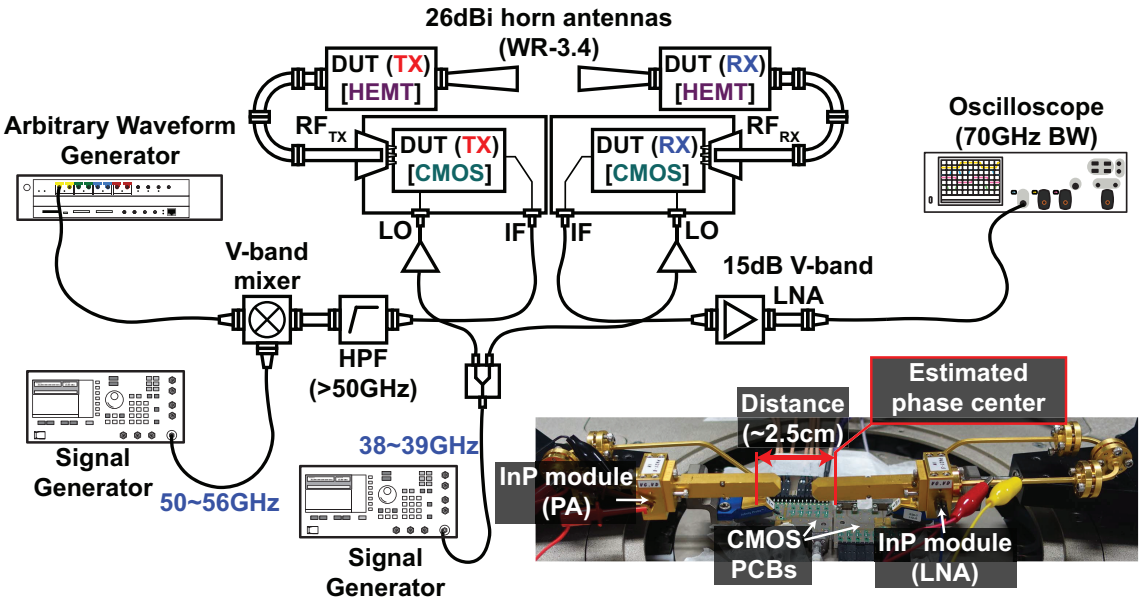


Figure 4.30: Hybrid transceiver measurement setup. (© 2021 IEICE)

its noise figure gets reduced to an estimated value of 18.8dB compared to the 32.8dB of the CMOS-only receiver (including the external losses such as antenna-CMOS connection). The total TX-to-RX calculated SNDR improves from 8.6dB to 25.5dB at a 5Gbaud symbol rate enabling 64QAM communication by adding the InP amplifiers to the system as shown in Fig. 4.28 and Fig. 4.29. Assuming that a 2dB connection is realized for on-board implementation, the estimated SNDR improves to 27.9dB over twice the distance as shown in Fig. 4.29. This estimation indicates that a low-loss connection is crucial for hybrid transceivers.

4.5 Measurement Results of the Hybrid Transceiver

The measurement setup used to evaluate the 300GHz wireless link is shown in Fig. 4.30. The data is generated using an arbitrary waveform generator and up-converted externally to the V-band. The 300GHz output signal is applied to the waveguide InP-HEMT amplifier module through a waveguide probe. Waveguide bends are used to align the antennas on the probe station. The 26dBi waveguide horn antennas are directly connected to the amplifier modules. The receiver V-band output is directly evaluated by a 70GHz oscilloscope after the external amplification which is used to compensate for the CMOS-to-PCB connection loss. The horn antennas are 5.6cm long, so the distance between the phase centers is estimated using the horn-to-horn measured propagation loss.

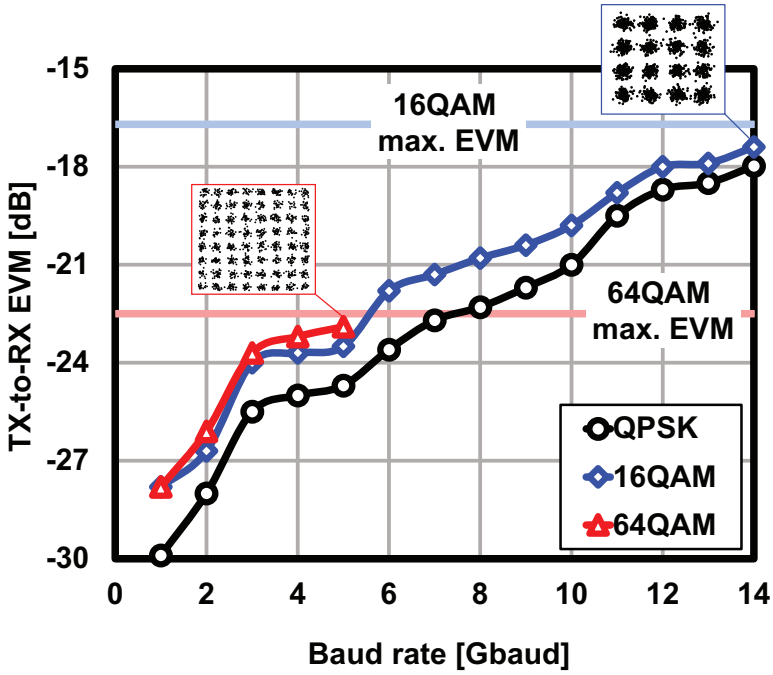


Figure 4.31: Hybrid transceiver measured EVM vs baud rate.

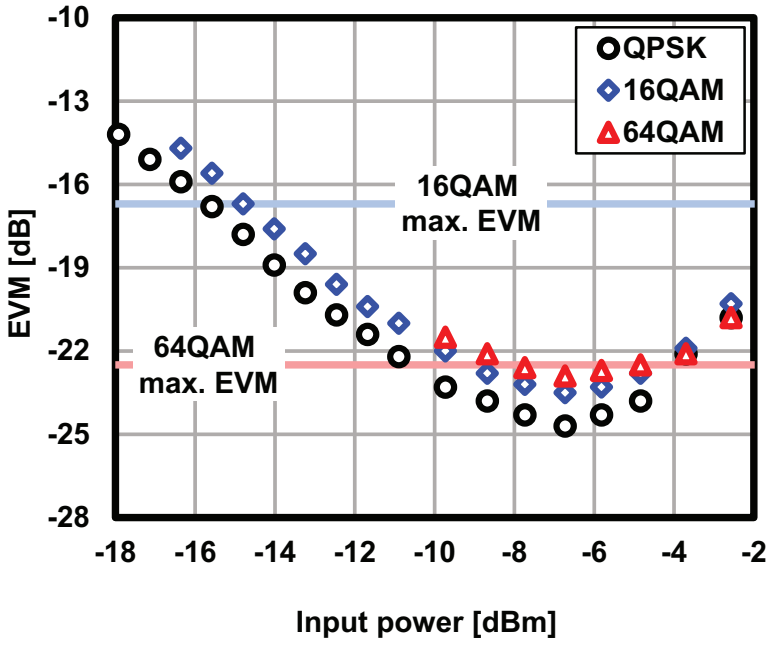


Figure 4.32: Hybrid transceiver measured EVM vs input power.

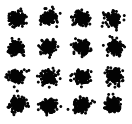
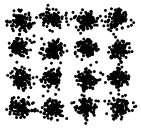
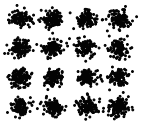
CHNL_ID	20	42	53	59	--
Center Frequency [GHz]	294.84	293.76	291.6	285.12	290
Bandwidth [GHz]	2.16	4.32	8.64	12.96	17.5
Symbol rate [Gbaud]	1.76	3.52	7.04	10.56	14
Modulation	64QAM	64QAM	16QAM	16QAM	16QAM
TX-to-RX Constellation					
TX-to-RX EVM [dB]	-25.14	-22.59	-19.71	-16.76	-16.72
Data rate [Gb/s]	10.56	21.12	28.16	42.24	56

Figure 4.33: Hybrid transceiver performance summary. (© 2021 IEICE)

Table 4.6: Hybrid transceiver performance comparison

	[31]	[20]	[38, 39]	[40]	[42]	This Work
Process	130nm SiGe	80nm InP-HEMT	40nm CMOS	40nm CMOS	65nm CMOS	65nm CMOS 80nm InP-HEMT
RF frequency [GHz]	220–255	278–302	290*	252–279	278–304	278–304
Evaluated schemes	16QAM	16QAM 64QAM	QPSK 16QAM 32QAM	QPSK 16QAM	QPSK 16QAM	16QAM **64QAM**
Max. data rate (16QAM) [Gb/s]	95	120	32	80	24	56
Max. data rate (64QAM) [Gb/s]	–	100	–	–	–	**30**
Communication distance [cm][&]	100	3.9	1.5	4.8	1	2.5
P_{DC} [W]	1.41	TX:4.5[$] RX:4.5[$]	TX:1.4 RX:0.65	TX:0.89 RX:0.9	TX:0.27 RX:0.14	TX:1.73 RX:1.61
Energy-per-bit [pJ/b]	14.8	75	64.1	22.4	17.1	59.6
Area [mm^2]	TX:N/A RX:N/A	TX:2.44 RX:2.44	TX:5.19 RX:3.15	TRX: 11	TX:1.9 RX:1.9	TX:3.8 RX:3.8

* Center frequency. & Normalized to 26dBi antenna gain. $ Without LO multiplier.

Fig. 4.31 shows the measured EVM for several baud rates with an estimated distance of 2.5cm. 16QAM is achieved for baud rates up to 14Gbaud resulting in a maximum data rate of 56Gb/s. 64QAM is also achieved at a maximum baud rate of 5Gbaud (30Gb/s). The measured 5Gbaud EVM with swept input power over the same distance is shown in

Fig. 4.32. Fig. 4.33 summarizes the measured performance for the main IEEE 802.15.3d standard channels and the maximum data rate condition. 64QAM modulation is usable in several channels such as ch. 20 and ch. 42. The maximum data rate achieved using a standardized channel is 42.24Gb/s (ch. 59).

4.6 Conclusion

Subharmonic mixing provides more suitable design options for CMOS sub-THz transceivers due to the reduced LO and IF frequency bands. The proposed passive subharmonic mixers achieves good conversion gain (-16.5dB) and acceptable linearity without consuming DC power. The proposed biasing technique reduces the transistor parasitic capacitance and improves the conversion gain. 34Gb/s link is achieved over 1cm distance using the proposed subharmonic-mixer-based transceiver with relatively low power consumption.

To improve the transceiver characteristics and the system SNDR, InP PA and LNA are added to the CMOS system. The InP-CMOS Hybrid transceiver achieves relatively high data rates while keeping most of the system components in the CMOS chip. The achieved SNDR is also high enough to realize 64QAM communication. The demonstration in this chapter shows that the digital-friendly CMOS process can be combined with the high-speed compound semiconductors to leverage the pros of the sub-THz band. Using the CMOS process makes it possible to integrate more complicated circuits as in SoCs where powerful processing circuitry can be directly connected to the transceiver on the same chip.

Chapter 5

Bi-Directional 300GHz-Band Phased-Array Transceiver

The subharmonic mixer introduced in Chapter 4 enabled a low power wireless link with acceptable performance. However, the output power is limited due to the severe linearity requirements of the mixer. The recent works introduced many solutions to improve the output power of CMOS transmitters around 300GHz-band. Using frequency multiplication to up-convert a 100GHz signal provides higher TX power due to the ability to operate the multiplier at its saturated output power, but the usable modulation schemes are limited and the operation is uni-directional, not to mention the expanded spectrum [34, 45]. Another way to use frequency multiplication is to apply both LO and IF signals to the input of the multiplier [38, 40], and the desired mixing components are filtered at the output. The TX output power here is slightly lower than that of the simple multiplier-last TX, but higher-order modulation schemes are feasible due to the linear relation between the desired signal power and the input power. The main issues of this architecture are the in-band undesired harmonics and the uni-directional operation.

In this work, the subharmonic mixer introduced in the previous chapter is used to utilize a lower LO frequency and to enable the bi-directional operation. The outphasing technique is used to solve the limited linearity issue of the mixer.

In the recent implementations of 300GHz-band CMOS transceivers [34, 35, 37–40], the TX and RX parts are designed separately mainly because the multiplier-based mixers are uni-directional and cannot be shared between TX and RX as illustrated in Fig. 5.1(a). Hence, a lossy antenna switch is required to share the antenna. However, separate antennas are usually used for TX and RX to avoid the switch losses. In addition, horn and lens antennas are used in most of the recent implementations due to their high gain characteristics, but that limits the radiation to be pointed only towards a certain direction, making

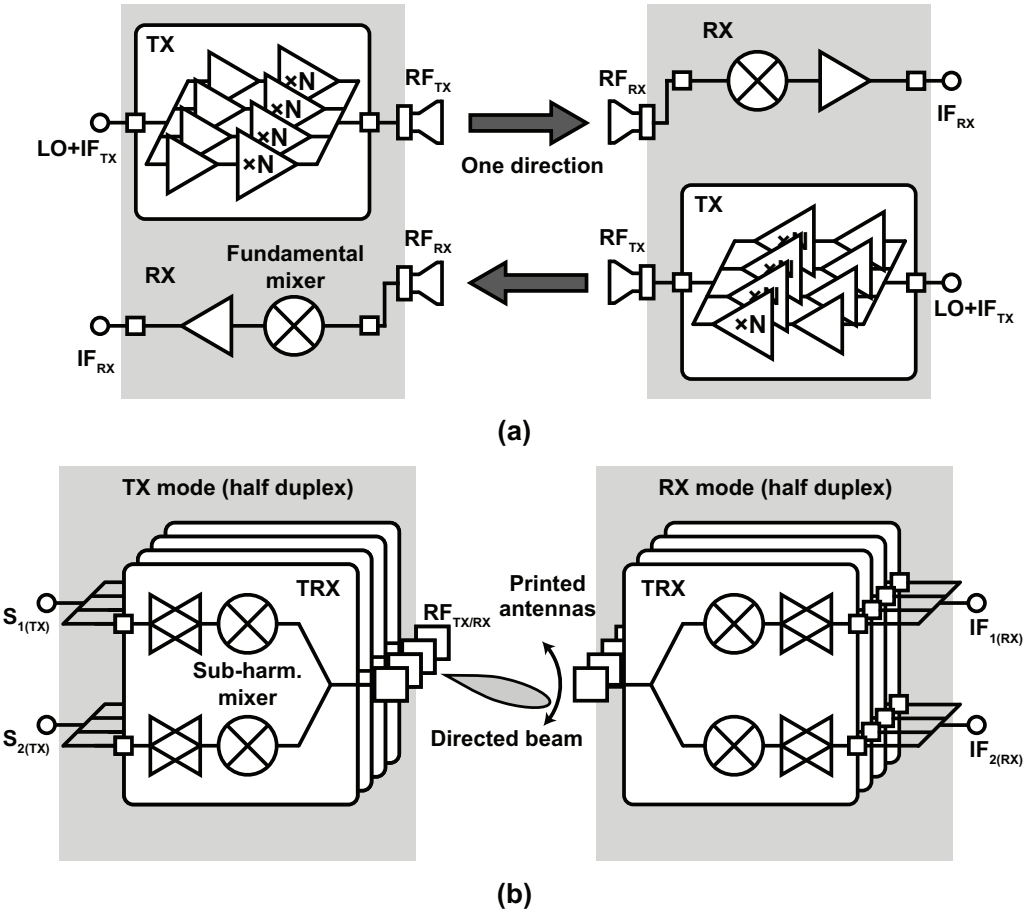


Figure 5.1: (a) Conventional sub-THz transceiver (b) Proposed transceiver with bi-directional architecture and beamforming.

it necessary to physically rotate the TX whenever that RX position changes, and vice versa. In this work, we adopt a bi-directional mixer architecture that makes it possible to share all the circuit components and antennas, reducing by that the area on- and off-chip as shown in Fig. 5.1(b). The reduced area by sharing the components and the antennas enables the system to be implemented as a phased-array to provide higher output power and beamforming as well.

This Chapter describes the design details and measurements of a phased-array bi-directional 300GHz-band TRX that utilizes outphasing with LOFT cancellation as its transmitting mode, and the Hartley architecture for its receiving mode [44]. For the cases where the image is canceled out using a matching circuitry or the antenna bandpass characteristics, the LOFT cancellation mode can also be applied to the receiving mode to eliminate the LO emission.

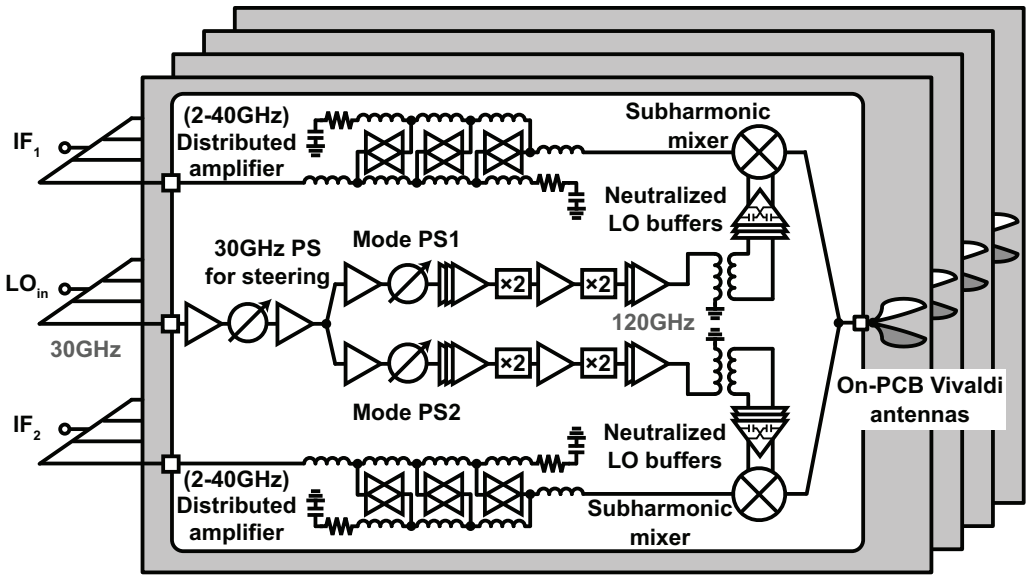


Figure 5.2: Bi-directional 300GHz-band phased-array transceiver architecture.

5.1 Phased-Array Transceiver Architecture

Fig 5.2 shows the block diagram of the 300GHz-band CMOS TRX system. It consists of two bi-directional subharmonic mixers, two bi-directional IF distributed amplifiers, three phase shifters in the LO chain to control the beam direction and the operation mode, frequency doublers, and LO buffers. All the circuit components are shared between the TX and RX. LO cancellation can be done in both transmitter and receiver modes, but image cancellation is also possible in the receiver mode by applying a 90° phase shift externally. The LO frequency is 240GHz (30GHz input LO) and the IF signal is centered around 16GHz. The antennas are printed on PCBs and the connection with CMOS is designed using the flip-chip process to implement a 4-element phased-array. The operation of the TX mode and the RX mode are explained in this section.

5.1.1 Outphasing Transmitter with LOFT Cancellation

The outphasing technique is usually applied to power amplifier systems to improve their efficiency by driving the amplifier at higher output power levels [87–89]. It was also used with frequency multipliers to provide higher efficiency as in [45]. In our design, we adopt the outphasing architecture using the passive subharmonic mixer to improve the average output power of the TX at 300GHz-band. The outphasing technique is one of the most suitable options to leverage the mixer saturated power to the maximum, as applying the constant envelope signal to the mixer means that the mixer can be driven at

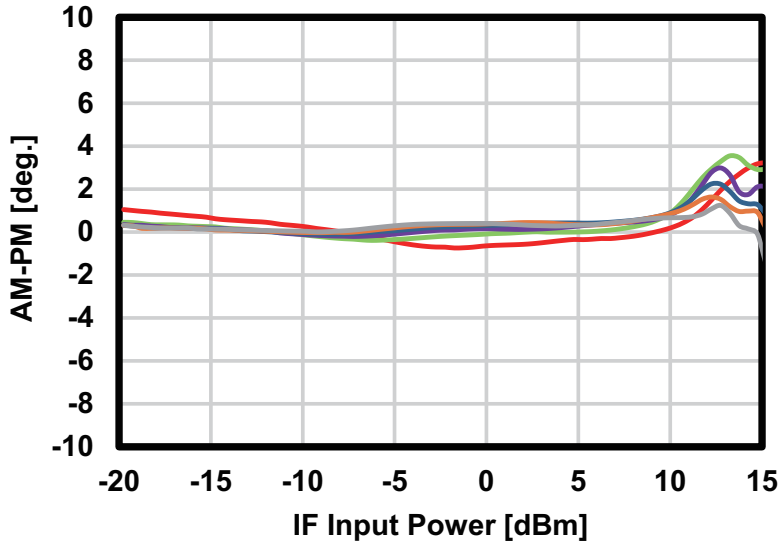


Figure 5.3: Simulated AM-PM of the mixer for several frequencies (3GHz to 33GHz with 6GHz step).

its saturated output power without any IM3 components appearing at the output as the following calculation suggests for a constant envelope signal $x(t) = A\cos(\omega t + \phi)$:

$$\begin{aligned} y(t) &= \alpha_3 x^3(t) + \cdots \\ &= \alpha_3 A^3 \cos^3(\omega t + \phi) + \cdots \\ &= \frac{3\alpha_3 A^3}{4}\cos(\omega t + \phi) + \textit{3rd harmonic} \end{aligned} \tag{5.1}$$

However, mismatches between the outphasing paths result in the appearance of additional undesired signals that have wide bandwidth and cause the overall EVM to degrade. The bandwidth of each path is also several times the output signal due to the large phase excursions [1]. Although the AM-AM does not have a large effect on the saturated mixer which is driven by a constant envelope signal, the AM-PM can cause EVM degradation if it is frequency dependent. The simulated AM-PM of the subharmonic mixer for several frequencies is shown in Fig. 5.3. The wideband characteristics of the mixer result in a total difference of less than 2 degrees for the whole band.

Operating the mixer at its saturated output power improves the average power of the transmitter by several dB compared to the single mixer case as shown in Fig. 5.4(a),(b). The 6dB back-off (or the PAPR of the modulation scheme in the outphasing case) is from the mixer saturated power instead of its 1dB compression point.

The TX mode operation is explained in Fig. 5.5. The input constant envelope signals

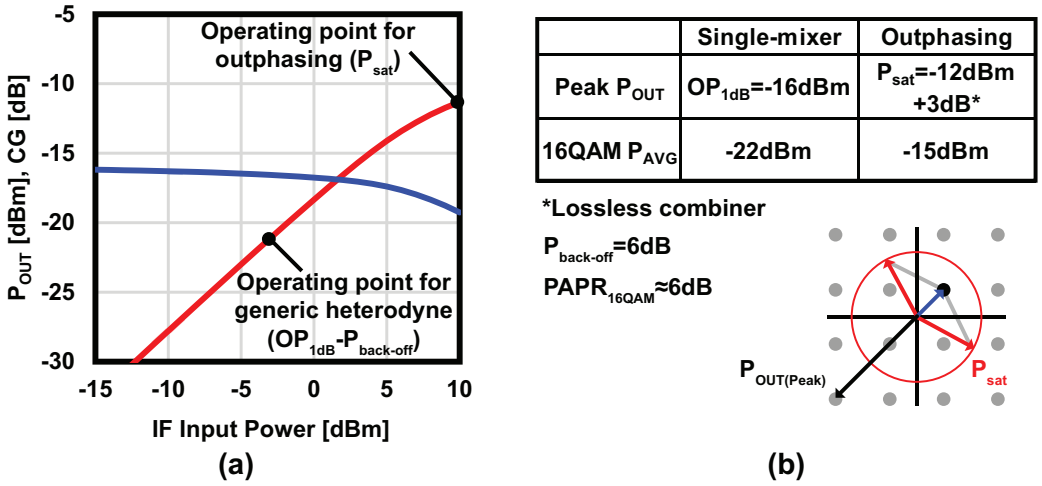


Figure 5.4: (a) Mixer simulated characteristics and operating point options. (b) Improvement on average power by outphasing.

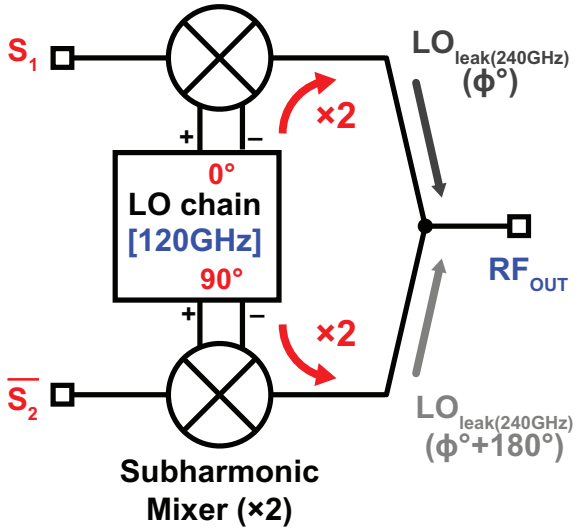


Figure 5.5: LOFT cancellation technique.

can be expressed as follows [45, 87]:

$$S_1(t) = \frac{A_M}{2}\cos(\omega_{IF}t + \theta + \phi) \tag{5.2}$$

$$S_2(t) = \frac{A_M}{2}\cos(\omega_{IF}t + \theta - \phi) \tag{5.3}$$

where $S_1(t)$ and $S_2(t)$ are the input outphasing signals, ω_{IF} is the IF angular frequency, θ is the modulated phase, and ϕ is the outphasing angle. Both of these signals are upconverted using the subharmonic mixers with a relatively high LOFT. The second order nonlinearity

of the subharmonic mixers converts the applied LO signal with an angular frequency of ω_{LOm} and two additional phase shifts (ζ for beamforming and ξ for mode selection) as follows:

$$\begin{aligned} LO(t,\xi) &= (A_{\mathrm{LOm}}\cos(\omega_{\mathrm{LOm}}t+\zeta+\xi))^2 \\ &= \frac{A_{\mathrm{LOm}}^2}{2}(1-\cos(2\omega_{\mathrm{LOm}}t+2\zeta+2\xi)) \\ &= \frac{A_{\mathrm{LOm}}^2}{2}(1-\cos(\omega_{\mathrm{LO}}t+2\zeta+2\xi)) \end{aligned} \tag{5.4}$$

it can be observed that the system LO frequency becomes $\omega_{\mathrm{LO}} = 2\omega_{\mathrm{LOm}}$ as the DC component can be ignored due to the presence of biasing circuits. Also, the previously applied phase shifts double providing wider phase range. To cancel the LOFT at the TX mode, the phase ξ is set to 0° in one outphasing path and to 90° in the other path. The phase of the second outphasing input $S_2(t)$ is inverted to recover the phase of the desired signal. The resulting output at the combining node from the first path can be calculated as follows:

$$\begin{aligned} S_1(t)LO(t,0^\circ) = \frac{A_{\mathrm{M}}}{2}\cos(\omega_{\mathrm{IF}}t+\theta+\phi) \\ \cdot\frac{A_{\mathrm{LO}}^2}{2}\cos(\omega_{\mathrm{LO}}t+2\zeta) \end{aligned} \tag{5.5}$$

$$LO_{\mathrm{Leak}}(t,0^\circ) = \frac{\alpha A_{\mathrm{LO}}^2}{2}\cos(\omega_{\mathrm{LO}}t+2\zeta) \tag{5.6}$$

and the calculated output of the second path is:

$$\begin{aligned} \overline{S_2(t)}LO(t,90^\circ) = \frac{A_{\mathrm{M}}}{2}\cos(\omega_{\mathrm{IF}}t+\theta-\phi+180^\circ) \\ \cdot\frac{A_{\mathrm{LO}}^2}{2}\cos(\omega_{\mathrm{LO}}t+2\zeta+180^\circ) \end{aligned} \tag{5.7}$$

$$LO_{\mathrm{Leak}}(t,90^\circ) = \frac{\alpha A_{\mathrm{LO}}^2}{2}\cos(\omega_{\mathrm{LO}}t+2\zeta+180^\circ) \tag{5.8}$$

The TX output is calculated by adding all the mixing and the leak components together:

$$\begin{aligned} RF_{\mathrm{OUT}} = S_1(t)LO(t,0^\circ) + \overline{S_2(t)}LO(t,90^\circ) \\ + LO_{\mathrm{Leak}}(t,0^\circ) + LO_{\mathrm{Leak}}(t,90^\circ) \end{aligned} \tag{5.9}$$

The leak components cancel each other out and the final output formula of the desired RF

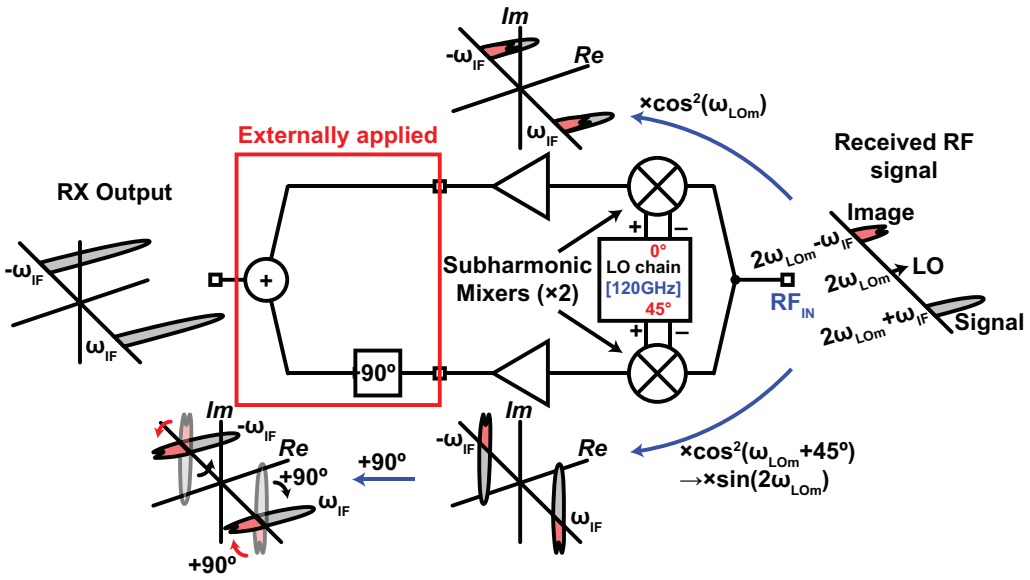


Figure 5.6: The operation of the Hartley receiving mode.

output signal (excluding the image components) is as follows:

$$RF_{\mathrm{OUT}} = \frac{A_{\mathrm{M}}A_{\mathrm{LO}}^2}{8}(\cos((\omega_{\mathrm{LO}}+\omega_{\mathrm{IF}})t+2\zeta+\theta+\phi) + \cos((\omega_{\mathrm{LO}}+\omega_{\mathrm{IF}})t+2\zeta+\theta-\phi)) \tag{5.10}$$

The LOFT is completely canceled by applying a 90° phase difference between the LO signals of the two outphasing paths without affecting the desired RF signal by using the proposed technique. The phase of the output signal is twice that of the input LO signal reducing the phase range requirements of the phase shifters. The same operation can be used at the RX mode by inverting one of the output IF signals before combining them.

5.1.2 Hartley Receiver

The RX can be operated at two different modes depending on the desired characteristics. First, the LO emission cancellation mode mentioned in the previous sub-section is used when the image signal is suppressed by the bandpass characteristics of the antenna. The other mode is for high received image power situation as the Hartley architecture can be applied. Fig. 5.6 illustrates the Hartley operation of the RX. A 45° phase difference is

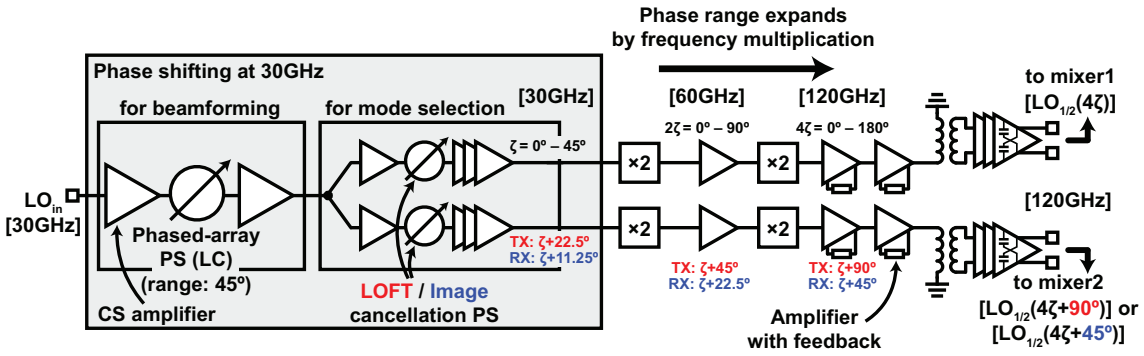


Figure 5.7: LO chain block diagram.

applied to the LO inputs of the two mixers, and is translated to 90° between the IF outputs:

$$RF(t)LO(t,45^\circ) = \frac{A_{\mathrm{RF}}}{2}\cos(\omega_{\mathrm{RF}}t) \cdot \frac{A_{\mathrm{LO}}^2}{2}\cos(\omega_{\mathrm{LO}}t + 2\zeta + 90^\circ) \tag{5.11}$$

An additional 90° phase shift is applied externally to completely cancel the image signal while combining the desired signal.

5.2 Circuit Implementation

After implementing the bi-directional subharmonic mixer circuit, the main focus of this work is on achieving bi-directional amplification using the IF amplifier, and flexible phase generation for beamforming and mode selection. The detailed LO chain and IF amplifier circuit implementation of the proposed transceiver chip will be introduced in the remaining part of this section.

5.2.1 LO Chain

Fig. 5.7 shows the LO chain design details. The phase shifting is done mainly at the input LO frequency at 30GHz. One phase shifter is used for beamforming, and two more phase shifters are used for LOFT and image cancellation. The frequency multiplier chain up-converts the LO frequency to 120GHz and quadruples the phase range. The outputs of the two phase shifting paths are applied to baluns to generate the differential LO inputs of the mixers. The required phase resolution at the output for 0.05dB array factor degradation is around 11.05° at the RF frequency, so a 1.38° maximum resolution is allowed at 30GHz considering the multiplier chain and the subharmonic mixing.

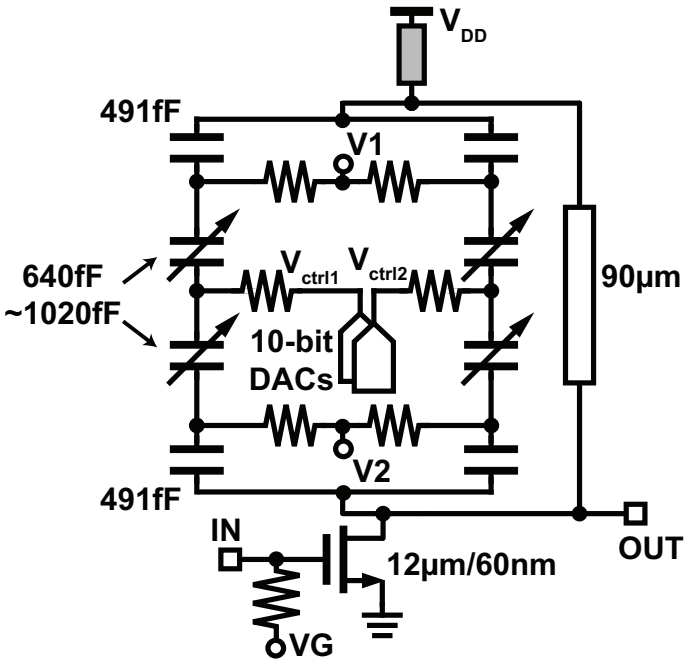


Figure 5.8: Phase shifter core schematic.

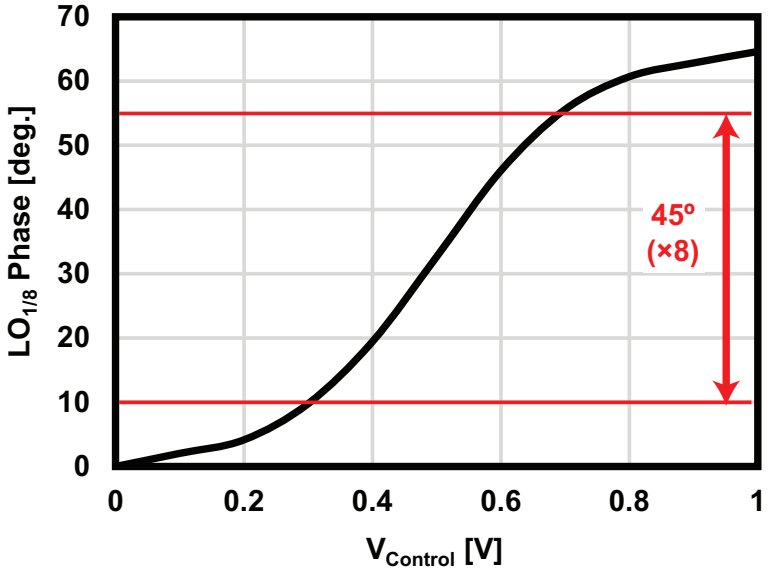


Figure 5.9: Phase shifter measured phase range.

Fig. 5.8 shows the circuit schematic of the 30GHz phase shifter. A varactor/transmission line combination is used as a load of a common-source stage to generate the required

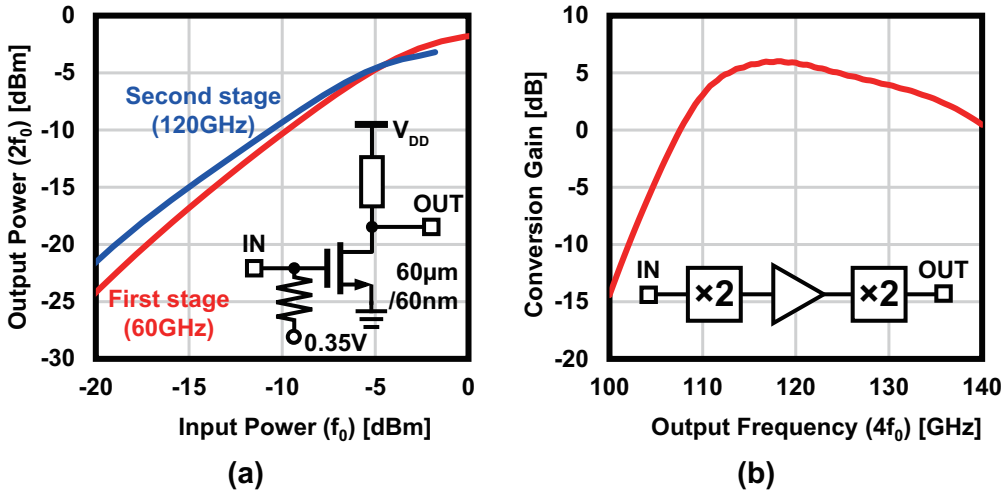


Figure 5.10: (a) Frequency doubler schematic and simulated output power, (b) Simulated conversion gain of the quadrupler chain.

phase shift. Based on small-signal analysis, the voltage gain of the phase shifter is:

$$A_v = g_m \frac{j\omega_{LOin}(1/C_{PS})}{1/L_{PS}C_{PS} - \omega_{LOin}^2 + j\omega_{LOin}(1/r_0 C_{PS})} \tag{5.12}$$

where C_{PS} and L_{PS} are the capacitance and the inductance at the drain of the transistor. The phase shift is calculated as follows:

$$\phi = \tan^{-1}\left(\frac{r_0}{\omega_{LOin}L_{PS}} - \omega_{LOin}C_{PS}r_0\right) \tag{5.13}$$

So, the value of C_{PS} which is directly related to the varactor capacitance value controls the phase of the output signal. The varactor utilizes a parallel combination to extend the tuning range ensuring that the required phase range is covered. The varactor control voltage is generated using a 10-bit DAC [2]. Fig. 5.9 shows the measured phase range at 30GHz by sweeping the control voltage. The required 45° is totally covered by around 400 DAC steps, so the phase resolution is around 0.1125° (0.9°@240GHz). The simulated jitter of the phase shifter is around 5.55ps at 30GHz and that corresponds to a 0.06° phase error. The resulting phase error at the RF is around 0.48°. The achieved resolution and phase error are much lower than the required ones for beamforming, and they are suitable for the fine-tuning of the LOFT cancellation signals.

The frequency doublers are based on the CMOS device non-linearity by biasing it

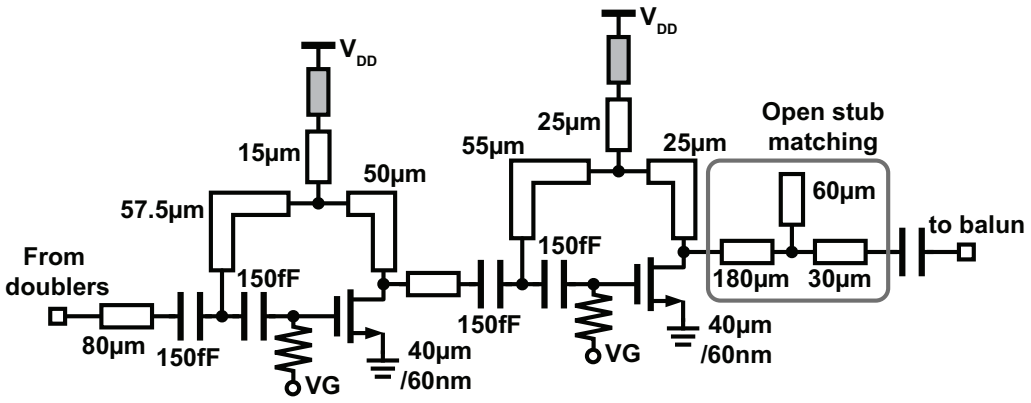


Figure 5.11: Schematic of the two-stage 120GHz single-ended LO Buffer using the maximum achievable gain.

around its threshold voltage:

$$i_{\mathrm{d}} = g_{m1} v_{\mathrm{gs}} + g_{\mathrm{m2}} v_{\mathrm{gs}}^2 + g_{\mathrm{m3}} v_{\mathrm{gs}}^3 + \ldots \tag{5.14}$$

This circuit is quite simple and has good output power as shown in the simulation results in Fig. 5.10(a). Both the first stage (30GHz to 60GHz) and the second stage (60GHz to 120GHz) provide more than -5dBm output power. The simulated conversion gain after adding a buffering stage between the two doublers is shown in Fig. 5.10(b). The doublers also multiply the phase of their input signals by two as the subharmonic mixer does in (5.4)

$$i_{\mathrm{d2}} = g_{m2} A_{\mathrm{LOin}}^2 \cos(2\omega_{\mathrm{LOin}} t + 2\delta) \tag{5.15}$$

The 45° coverage of the phase shifter at 30GHz is translated to 360° at 240GHz at the output after the frequency multipliers and the subharmonic mixer.

The 120GHz LO buffers are divided into two parts: The single-ended stages, and the differential stages. Amplification at 120GHz using CMOS is not straightforward as that frequency is pretty close to the $\mathrm{f_{max}}$. The single-ended stages are designed to fulfill the conditions of the maximum achievable gain [53, 90, 91] as shown in Fig. 5.11. The passive feedback is formed using transmission lines to increase the total gain and output power. The target optimal voltage gain and phase of the transistor calculated using the transistor's Y-parameters to obtain the maximum achievable gain are [91]:

$$A_{\mathrm{opt}} = \frac{\left|Y_{12} + Y_{21}^*\right|}{2G_{22}} \tag{5.16}$$

$$\Phi_{\mathrm{opt}} = (2k+1)\pi - \angle(Y_{12} + Y_{21}^*) \tag{5.17}$$

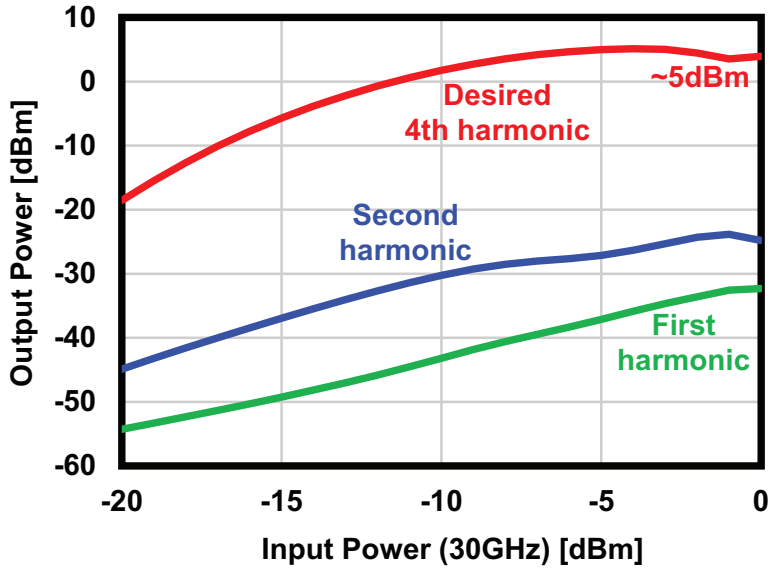


Figure 5.12: The simulated output power of the single-ended LO chain (balun input).

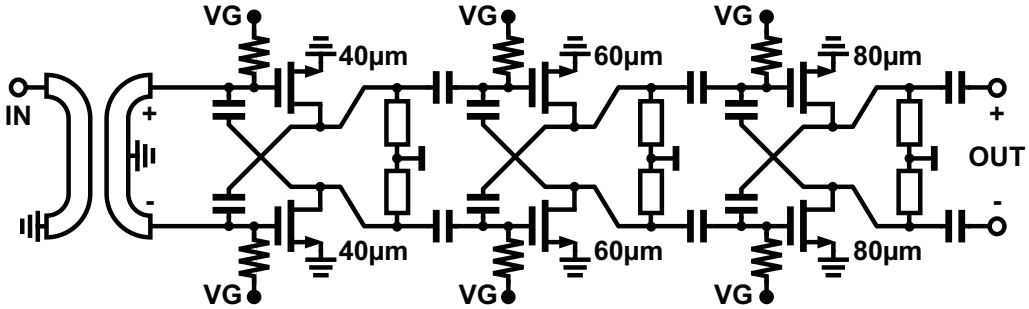


Figure 5.13: (a) Differential LO buffer schematic.

Transmission lines are used for inter-stage matching to save the area, and an open stub is used to match the inductive impedance of the balun at the output. Fig. 5.12 shows the simulated power provided by the single-ended doublers and buffers chain to the balun input. Around 5dBm LO signal power and more than 30dB suppression of the other harmonics is achieved.

The differential part is based on neutralized buffers using cross-coupled capacitors. Fig. 5.13 illustrates the schematic of the three differential stages. The simulated input/output power characteristics of the differential amplifiers are shown in Fig. 5.14. The achieved power (at each end) is around 5dBm (8dBm differentially), and this power drives the mixer directly.

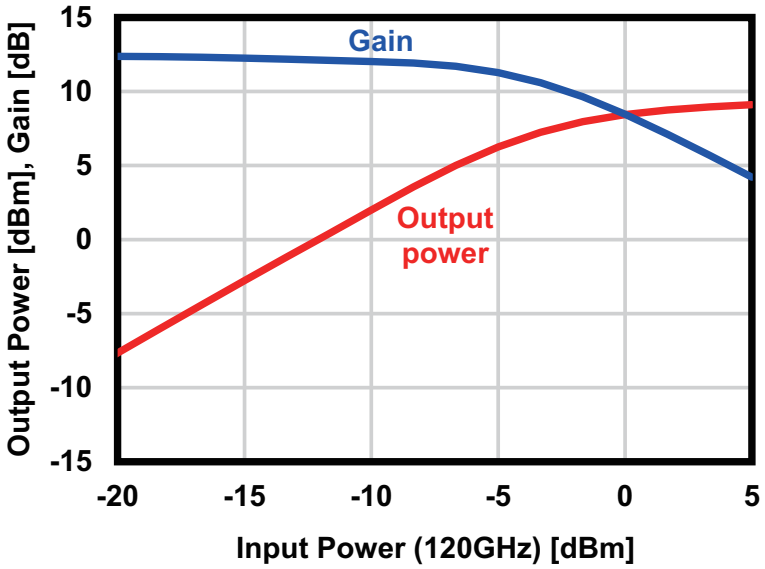


Figure 5.14: Differential neutralized LO buffer chain output power characteristics (mixer LO input power)

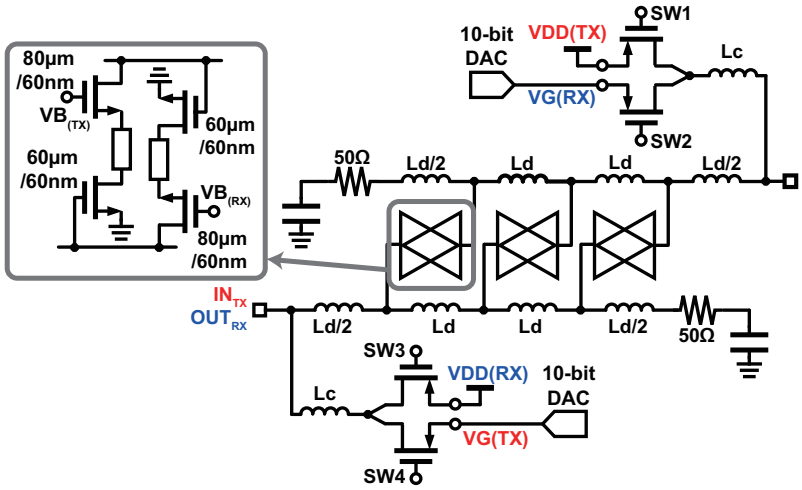


Figure 5.15: Bi-directional distributed variable-gain IF amplifier schematic.

5.2.2 IF Distributed Amplifiers

To achieve the full bi-directional operation, the IF amplifiers must also have a bi-directional structure. Knowing that the mixer bandwidth is very wide, the system bandwidth is decided by the bandwidth of the IF amplifiers. The amplifier is also supposed to have a controllable gain to provide the ability of mismatch compensation as the mismatch between the two outphasing paths in TX or the two Hartley paths in RX causes serious degradation on the EVM of the system.

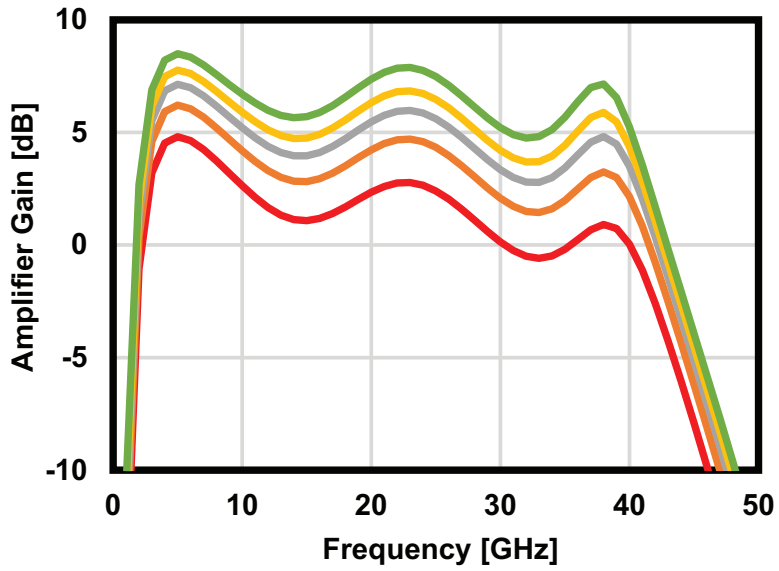


Figure 5.16: IF amplifier simulated gain for several voltages.

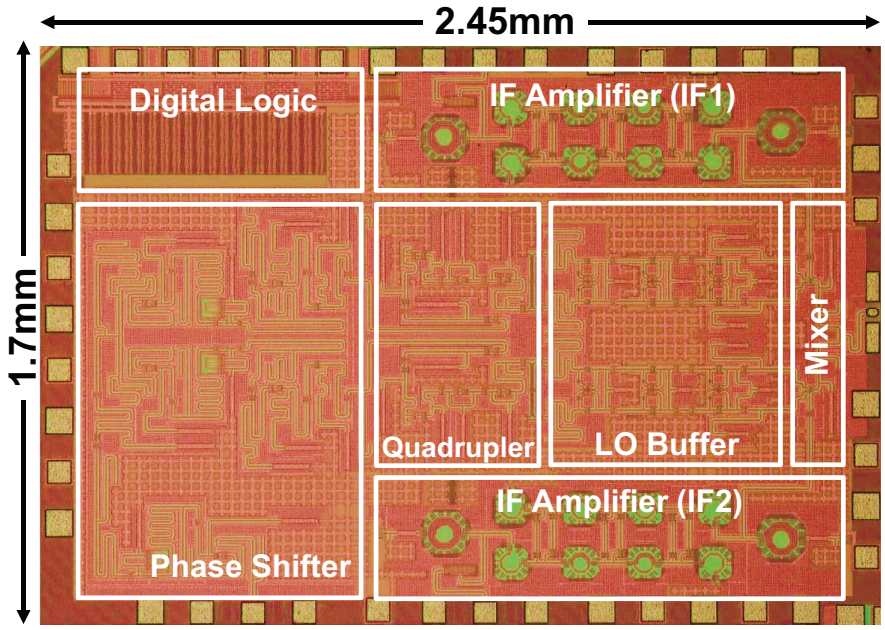


Figure 5.17: The die micrograph. (© 2021 IEEE)

In this work, the distributed amplifier circuit is adopted to provide wide bandwidth operation at low frequencies. Three cascode stages are used with a bi-directional structure [92] to provide several dB gain to the TX and the RX paths. The operation mode (TX or RX) is selected by controlling the switches SW1-4 and the biases of the cascode

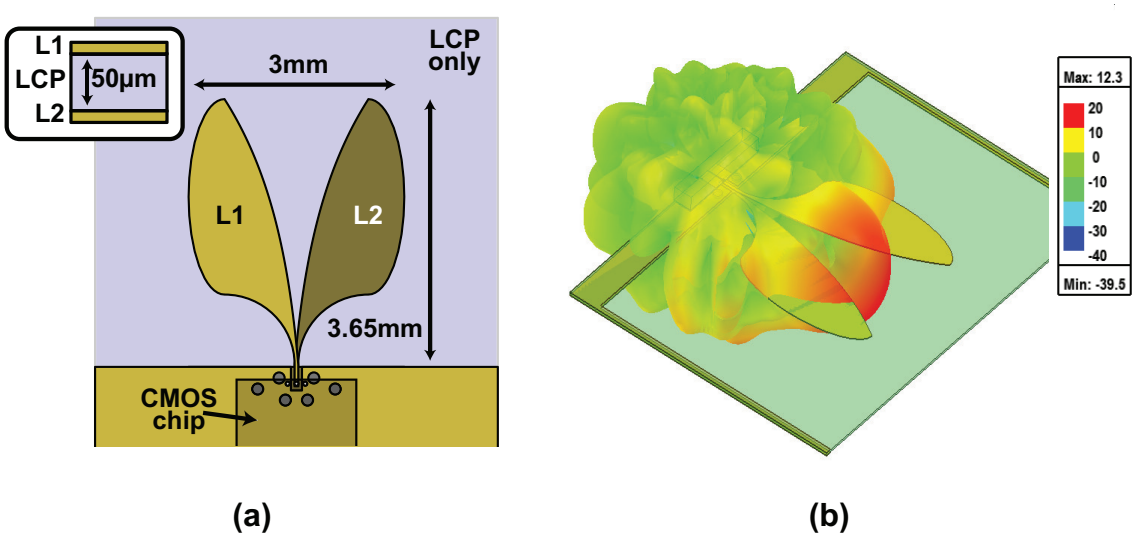


Figure 5.18: Vivaldi antenna (a) design, (b) simulated 3D pattern.

transistors. The schematic of the bi-directional distributed amplifier is shown in Fig. 5.15. The gain of the amplifier can be controlled by adjusting the bias voltage of the transistors using a DAC to make sure the outphasing signals amplitudes are equal in the TX case and the image signal amplitudes are equal in the RX Hartley case. The gain simulation results for several control voltages are shown in Fig. 5.16.

5.3 PCB and Phased-Array Implementation

The proposed 300GHz-band transceiver chip is fabricated in a 65nm CMOS process. Fig. 5.17 shows the chip micrograph. The chip size is 2.45mm×1.7mm.

An on-PCB antenna is used To build the phased-array. Fabricating an on-chip antenna as in [57–61] is possible due to the short wavelength, and it can be used to implement an on-chip array with a suitable antenna pitch, but the chip area will be huge and the antenna gain will be very limited due to the large silicon substrate loss. The designed phased-array Vivaldi antenna is shown in Fig. 5.18(a). The Vivaldi antenna was chosen due to its wide bandwidth and high gain. However, the material for the 300GHz-band Vivaldi antenna must be carefully chosen to avoid the breaking up of the main beam, by fulfilling the optimal value of the effective substrate thickness normalized to the free-space wavelength which is between 0.005–0.03 and defined by [93]:

$$\frac{t_{\text{eff}}}{\lambda_0} = \left(\sqrt{\varepsilon_{\text{r}} - 1}\right)\frac{t}{\lambda_0} \tag{5.18}$$

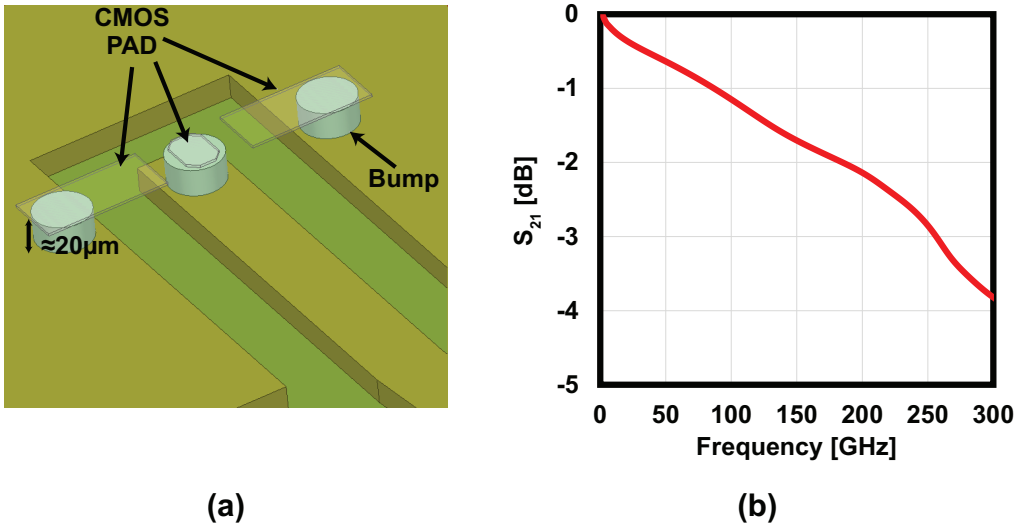


Figure 5.19: Bump connection between the CMOS and the LCP PCB (a) model and (b) simulated loss.

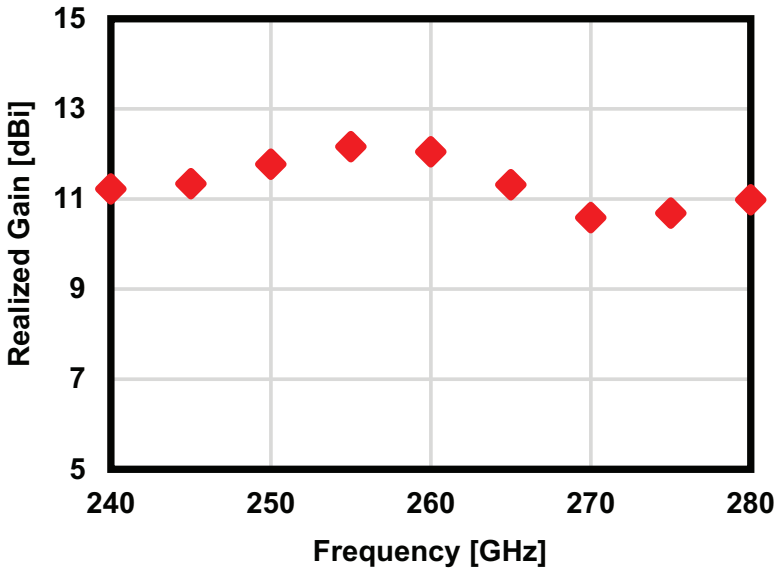


Figure 5.20: Vivaldi antenna simulated realized gain (including the connection to CMOS).

where t is the substrate thickness.

From (5.18), it can be observed that the thickness and permittivity requirements become more severe as the frequency increases. The LCP material is used to fabricate the PCB in this work to take advantage of its thin substrate (50μm), low permittivity ($\varepsilon_r = 3$), and flexible characteristics as will be shown later in this section. The 3D radiation pattern of the antenna is shown in Fig. 5.18(b).

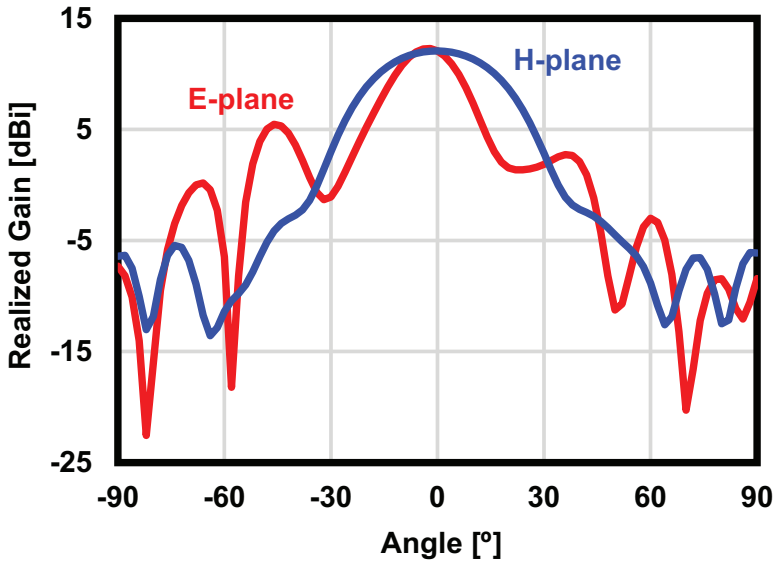


Figure 5.21: Vivaldi antenna simulated realized gain in the E-plane and the H-plane (including the connection to CMOS).

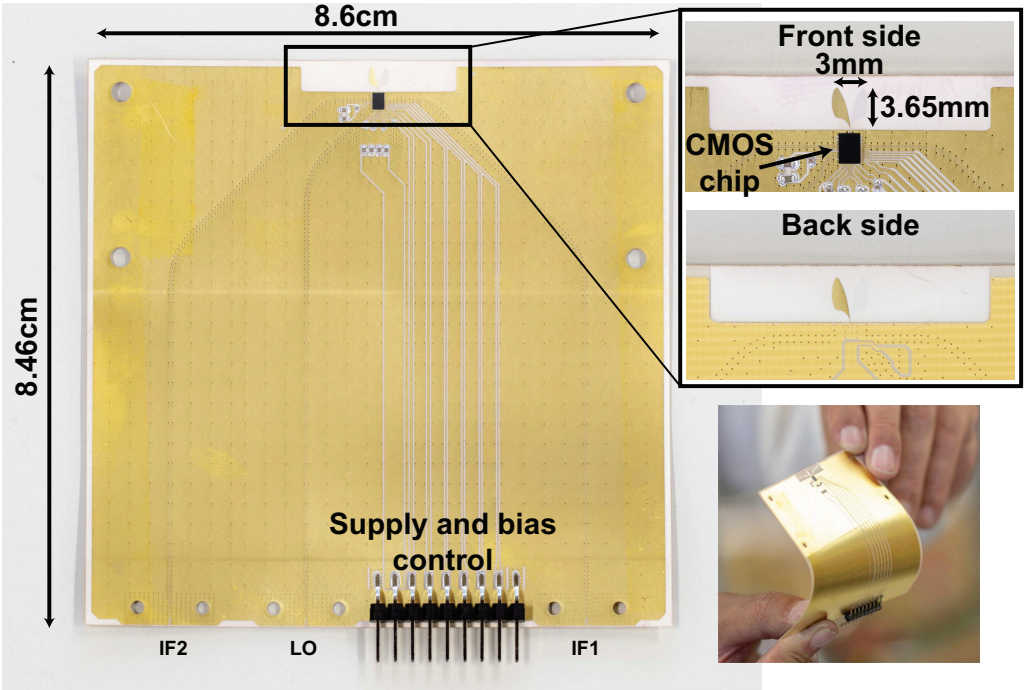


Figure 5.22: Photographs of the PCBs used for phased-array implementation.

The CMOS-to-antenna flip-chip connection must also be designed very carefully to avoid large losses in the RF band. The CMOS signal pad size was chosen to be as small as possible. The dimensions are 25um by 35um. Such a small pad has less capacitance

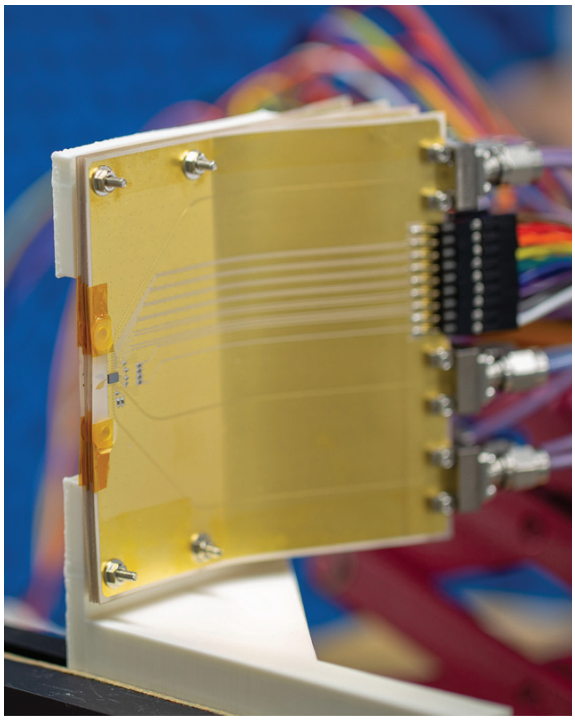


Figure 5.23: A photograph of the implemented 4-element phased-array.

and less reflection as its impedance is close to 50Ω. However, some difficulties may appear in the implementation as the pad is slightly smaller than the connecting bump. The 3D model of the CMOS pads and bumps is shown in Fig. 5.19(a). The simulated loss including CMOS and PCB connecting transmission lines is around 3dB at the band of interest as shown in Fig. 5.19(b). The bandwidth of the Vivaldi antenna including bump losses covers the whole band with more than 10dBi gain as shown in Fig. 5.20. The simulated E-plane and H-plane patterns of the antenna are shown in Fig. 5.21.

The antenna pitch is much smaller than the V-band connector size, so a flexible part of the LCP PCB is slightly bent to fit the connectors. The detailed photos of the flexible 50μm LCP PCB are shown in Fig. 5.22, and the implemented 4-element phased-array photo is shown in Fig. 5.23.

Due to the measurement difficulties of the phased-array-to-phased-array condition, an additional evaluation board is designed. The evaluation board has an on-PCB transition from the CMOS coplanar waveguide structure to a WR-3.4 rectangular waveguide. The rectangular waveguide provides the measurement flexibility as high gain horn antennas can be used. Fig. 5.24 shows the shape of the transition component, and Fig. 5.25 shows a photo of the evaluation board including the waveguide part attached. The transition loss is simulated using ANSYS HFSS and the results are shown in Fig. 5.26

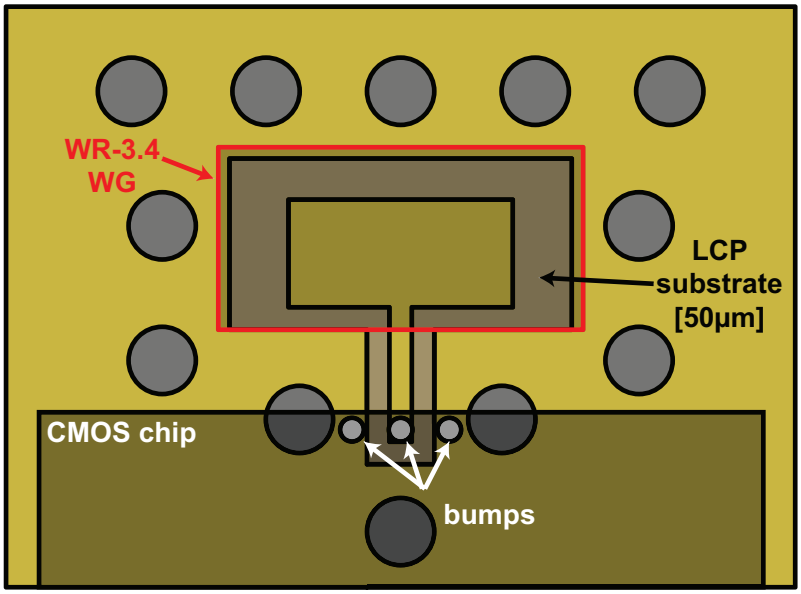


Figure 5.24: CMOS-to-PCB transition design for PCB evaluation board.

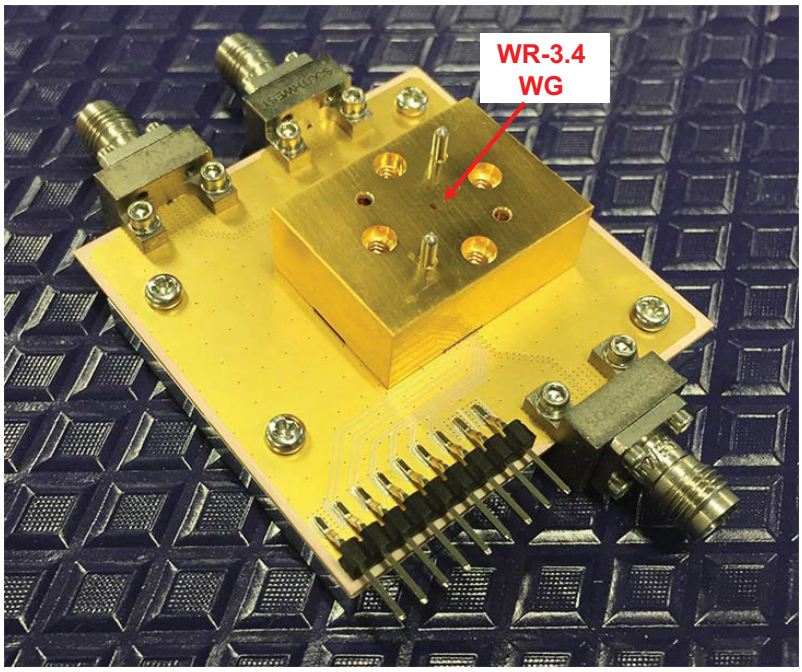


Figure 5.25: Evaluation board photo (The CMOS-to-PCB transition module installed).

5.4 Measurement Results

The on-wafer characteristics are evaluated first by implementing a PCB with wire-bonding connections to the CMOS chip except for the RF port. The RF port is connected to the measurement equipment using a waveguide probe with known loss. Fig. 5.27 shows the

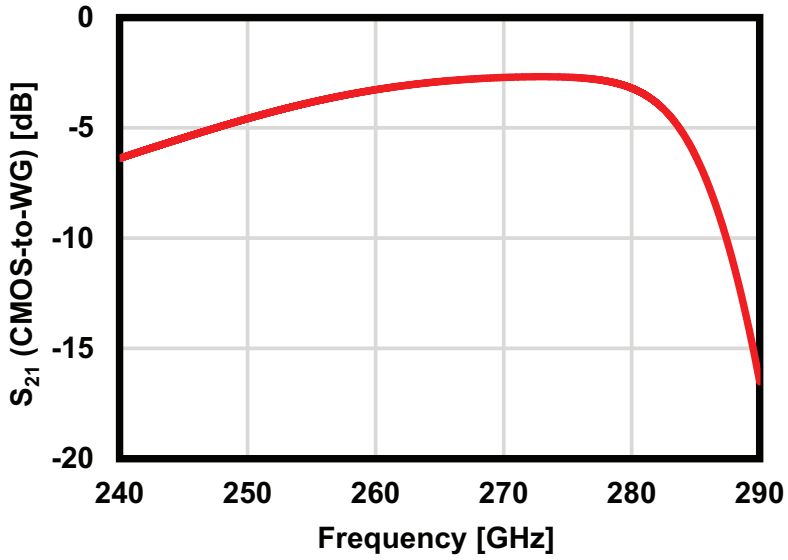


Figure 5.26: Simulated loss of the CMOS-to-WG transition.

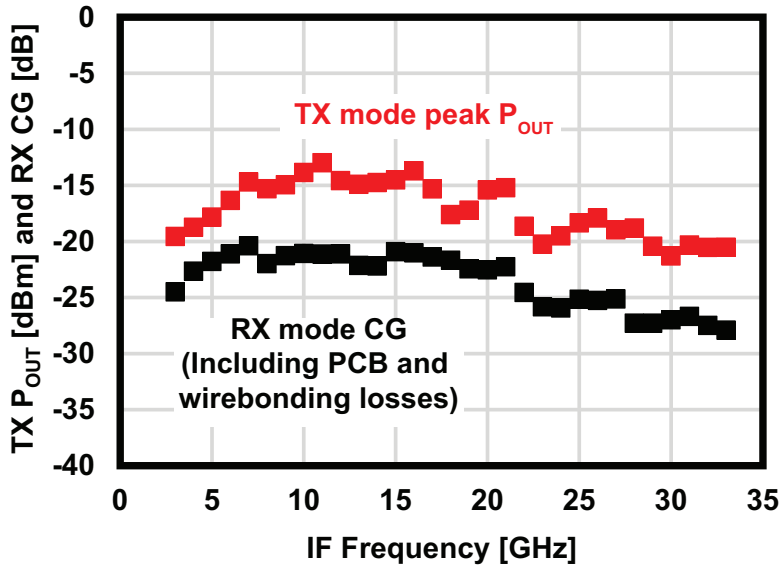


Figure 5.27: Measured TX mode output power and RX mode conversion gain.

measured maximum output power of the TX mode for the whole frequency band. The output power is not high compared to the other works due to the bi-directional design of the mixer, but using the outphasing means that the average power is closer to the P_{sat}. The RX conversion gain is also shown in Fig. 5.27 including the bonding wires and the PCB losses at the IF side. Fig. 5.28 shows the TX EVM for different output power situations (Symbol rate: 5Gbaud). Thanks to the outphasing technique, the IM3 effect on the EVM

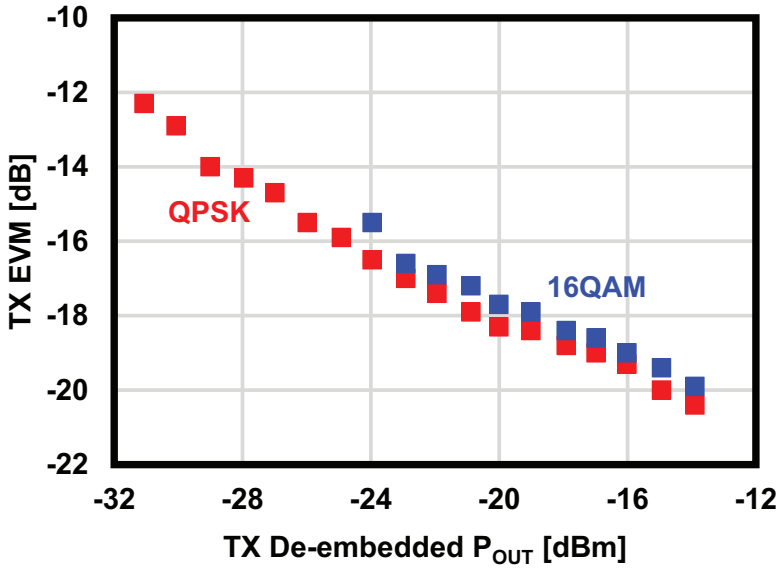


Figure 5.28: Measured transmitter EVM.

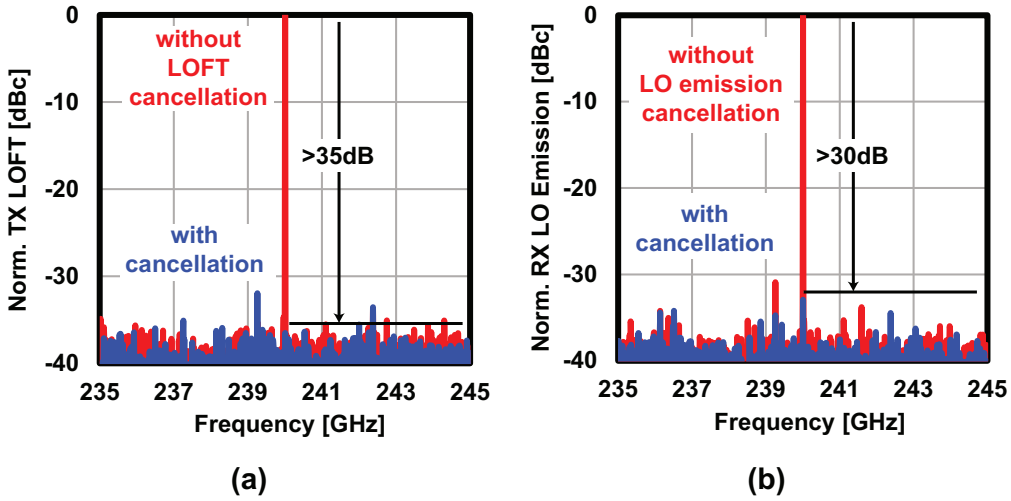


Figure 5.29: Measured LOFT cancellation (a) in the TX mode and (b) the RX LO emission rejection mode.

is not observed as the EVM saturates with the output power.

The LOFT cancellation was also tested for both the TX mode and the RX mode (LO emission cancellation). Fig. 5.29(a) shows the TX mode LOFT cancellation. More than 35dB cancellation is possible by using the proposed technique with the fine resolution of the phase shifter. The LO emission cancellation of the RX mode is shown in Fig. 5.29(b) with more than 30dB suppression as well. The Hartley RX mode was tested by down-converting a DSB signal provided by an external mixer using a slightly shifted

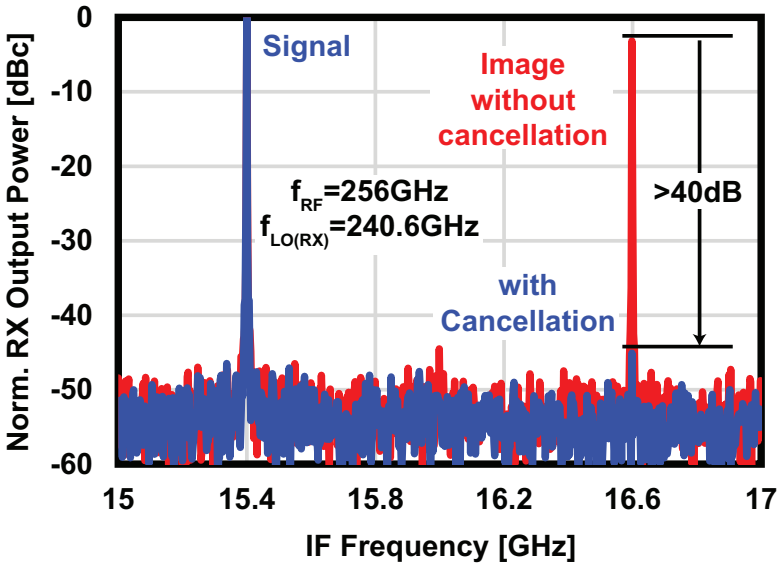


Figure 5.30: Measured image rejection of RX Hartley mode.

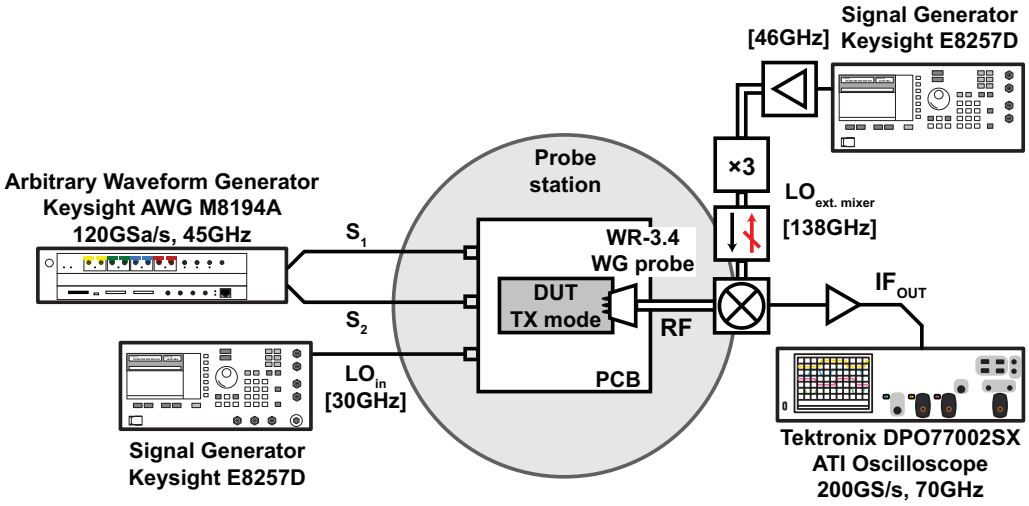


Figure 5.31: Measurement setup for TX mode EVM.

LO frequency. The external mixer up-converts a 16GHz signal using an LO frequency of 240GHz to generate two sidebands at 224GHz and 256GHz. The RX chip LO frequency is set to 240.6GHz to down-convert the desired signal and the image at two different frequencies (The desired signal at 15.4GHz and the image at 16.6GHz). Both signals are observed using a spectrum analyzer and the image rejection measurement results are shown in Fig. 5.30. More than 40dB image rejection is achieved at a single frequency for a worst-case situation (the signal power is equal to the image power).

Fig. 5.31 and Fig. 5.32 illustrates the setup used to evaluate the TX mode and the

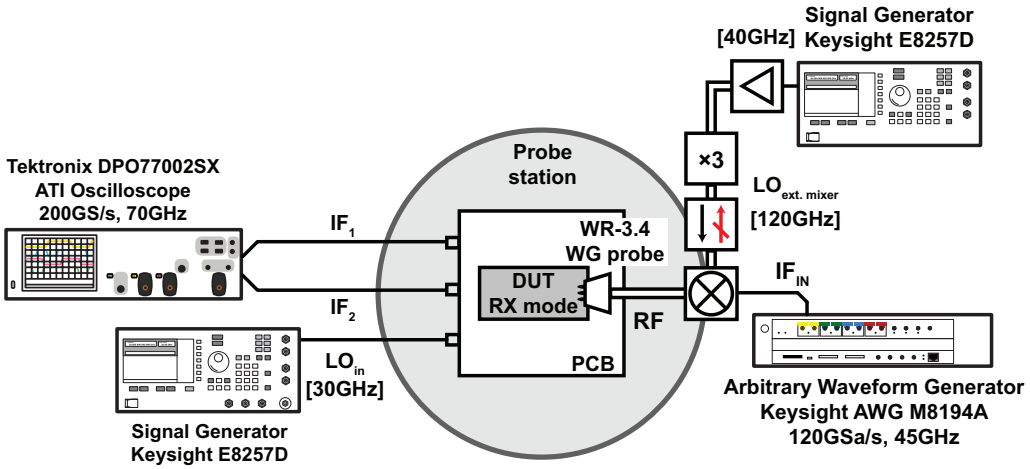


Figure 5.32: Measurement setup for RX mode EVM.

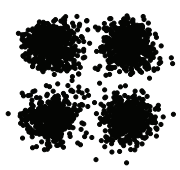
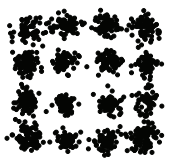
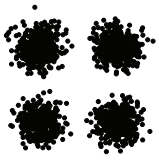
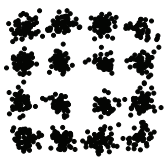
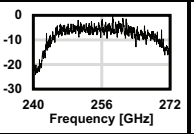
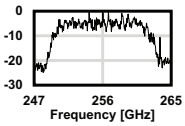
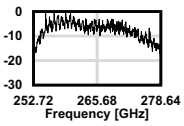
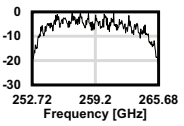
TX mode				
	Maximum data rate conditions		IEEE802.15.3d channels	
Channel ID	N/A	N/A	Ch. 66	Ch. 57
Modulation	QPSK	16QAM	QPSK	16QAM
f_{center} [GHz]	256	256	265.68	259.2
Symbol rate [Gbaud]	26	12	21.12	10.56
Data rate [Gb/s]	52	48	42.24	42.24
TX down converted constellation				
TX spectrum				
TX EVM [dB]	-9.8	-16.6	-11.5	-16.8

Figure 5.33: Measured EVM and constellations of TX mode.

RX mode EVM separately while probing the RF signal. The previously mentioned PCB was placed on a probe station with all the IF and LO connections provided using wire-bonding. For the TX mode EVM measurement, the outphasing signals are generated using the Keysight arbitrary waveform generator (AWG) M8194A with the phase inversion applied by the AWG as well. The TX output signal is applied to an external subharmonic mixer through a waveguide probe. The LO of the external mixer is set at a higher frequency (138GHz×2=276GHz) and is generated using a signal generator and a tripler. The down-converted signal is amplified and observed using the Tektronix DPO77002SX

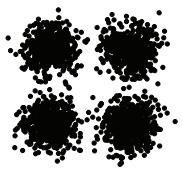
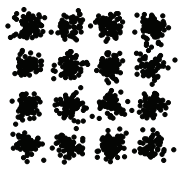
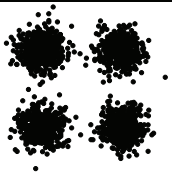
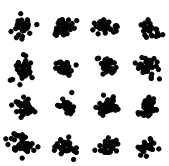
RX mode				
	Maximum data rate conditions		IEEE802.15.3d channels	
Channel ID	N/A	N/A	Ch. 57	Ch. 2
Modulation	QPSK	16QAM	QPSK	16QAM
f_{center} [GHz]	256	256	259.2	255.96
Symbol rate [Gbaud]	18	3	10.56	1.76
Data rate [Gb/s]	36	12	21.12	7.04
RX down converted constellation				
RX EVM [dB]	-10.1	-16.8	-10.8	-17.1

Figure 5.34: Measured EVM and constellations of RX mode.

oscilloscope. The TX mode setup is illustrated in Fig. 5.31.

The RX mode measurement setup is shown in Fig. 5.32. This time, the RF input signal is generated externally using the same external mixer with a 120GHz×2=240GHz LO frequency to make sure that the image signal appears in-band so that the image rejection can be tested. The IF outputs are then observed using the oscilloscope. The 90° phase shift and signal combining are performed inside the oscilloscope.

Fig. 5.33 summarizes the TX mode EVM performance for several situations measured using the setup in Fig. 5.31. The maximum baud rate achieved is 26Gbaud with an EVM of about -9.8dB, and the center frequency of the IF, in this case is 16GHz. The data rate here is 52Gb/s. Using the same IF center frequency and a narrower bandwidth, 16QAM modulation scheme is also achievable. The maximum symbol rate that is used to achieve 16QAM required EVM is 12Gbaud (48Gb/s). IEEE 802.15.3d channels were also evaluated and Fig. 5.33 shows the results of two channels. The ch. 66 that has a wide bandwidth of 25.92GHz can provide a symbol rate of 21.12Gbaud assuming a 0.25 roll-off factor. The EVM achieved using this channel is -11.5dB, which means that QPSK modulation is usable with a 42.24Gb/s data rate. Ch. 57 has a narrower bandwidth of 12.96GHz and the EVM achieved there is -16.8dB, so the 16QAM is used to obtain a data rate of 42.24Gb/s.

The RX mode EVM performance measured using the setup in Fig. 5.32 is summarized in Fig. 5.34. The maximum baud rate achieved is 18Gbaud with a -10.1dB EVM at an RF center frequency of 256GHz. The maximum data rate achieved by the RX is 36Gb/s. 16QAM modulation is also achieved at the same RF center frequency with a 3Gbaud symbol rate (12Gb/s). The results of IEEE 802.15.3d ch. 57 and ch. 2 are also shown. 21.12Gb/s is achieved in ch. 57 using QPSK modulation, and 7.04Gb/s is achieved using

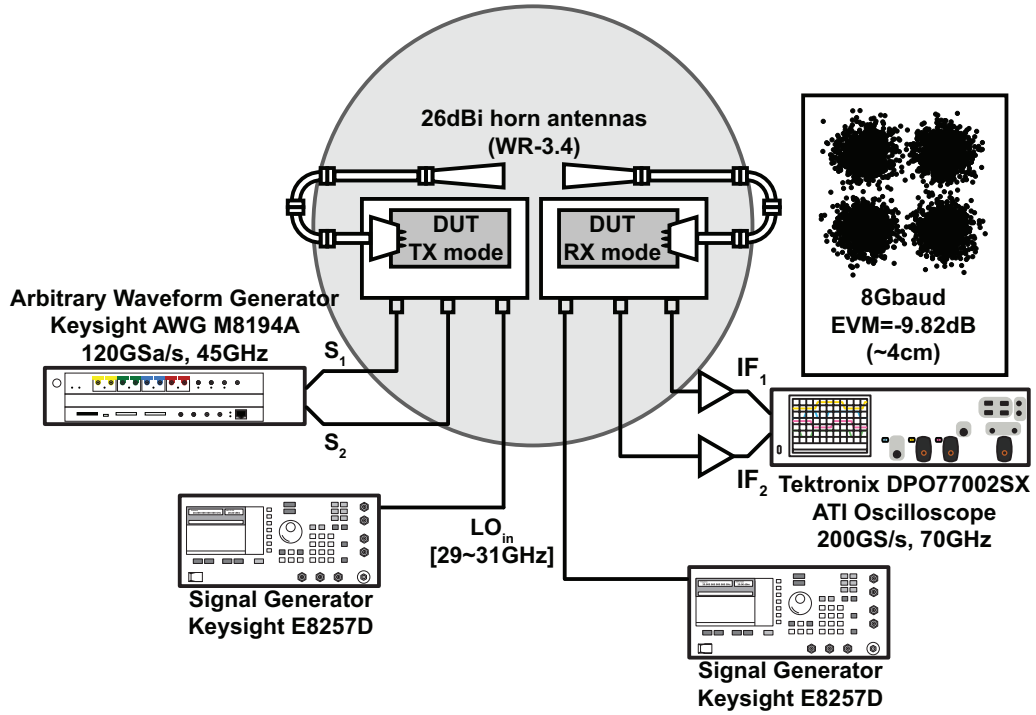


Figure 5.35: Measurement setup of OTA measurement.

16QAM in ch. 2.

To evaluate the OTA performance of a single-element-to-single-element case, Two transceivers were placed on the probe station as shown Fig. 5.35. The outphasing signals with inverted phase are applied to the input of the first transceiver which operates at the TX mode. The 300GHz-band signal is applied to the input of a 26dBi horn antenna using waveguide bends and a waveguide probe. The U-like shape makes it possible to align the antennas as the same connection is used for the second transceiver which operates at the RX mode. the output of the RX is observed by the oscilloscope where the 90° phase shift and the combining take place. Different signal generators are used for the TX and RX to calibrate the image cancellation by shifting the down-conversion frequency. The maximum data rate achieved over an estimated distance of 4cm between the phase centers of the horn antennas is 16Gb/s.

The beam pattern of the 4-element phased-array was measured using the setup in Fig. 5.36 and Fig. 5.37. The evaluation board with lossy transition module was used for the down-conversion as a single-element RX, so a compensating III-V semiconductor amplifier was attached. The measured beam is shown in Fig. 5.38. The steering range in the H-plane covers the angles from -18° to 18°.

Table 5.1 shows the power consumption breakdown for a single element of the proposed phased-array transceiver. The measured power consumption in both transmitter

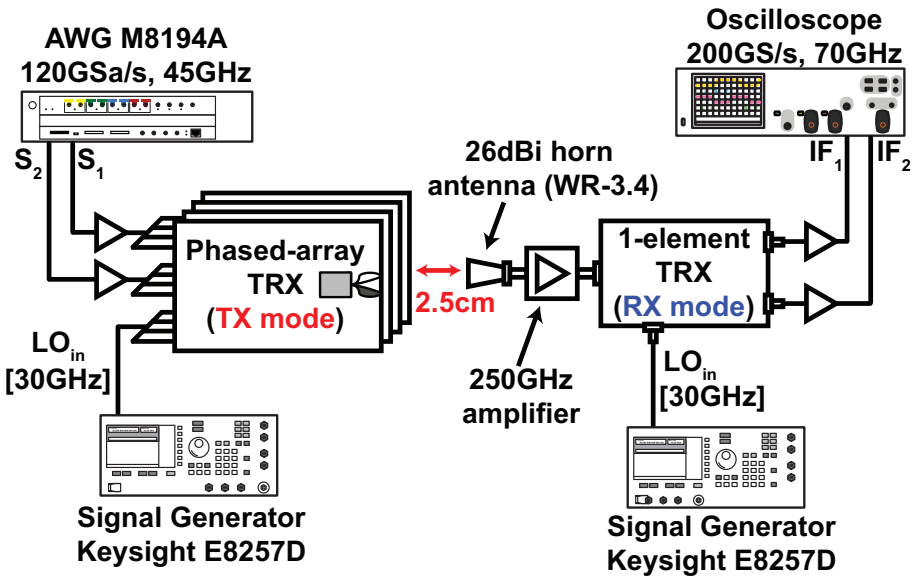


Figure 5.36: Array pattern measurement setup block diagram.

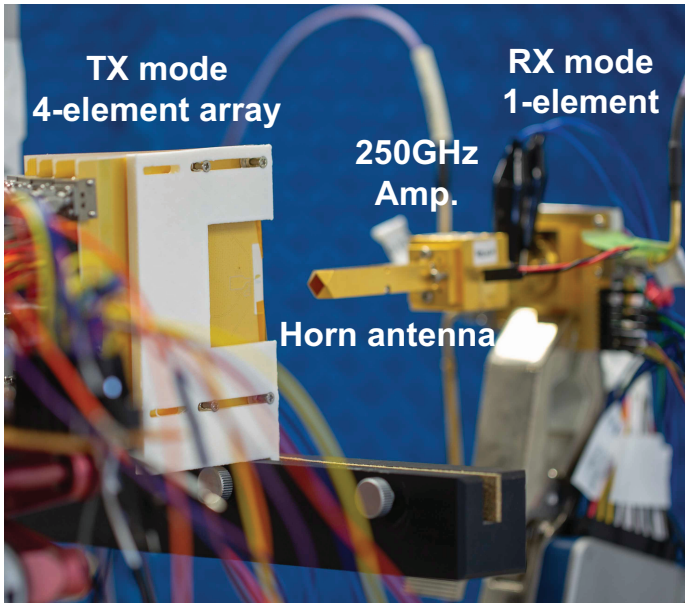


Figure 5.37: Array pattern measurement setup photograph.

mode and receiver mode is around 0.75W. In Table 5.2, this work is compared with several state-of-the-art 300GHz-band CMOS transceivers. The bi-directional architecture reduces the area considerably and the mixer-distributed amplifier combination contributes to the very wide operating bandwidth. This work demonstrates the first phase-array transceiver that operates at above 200GHz.

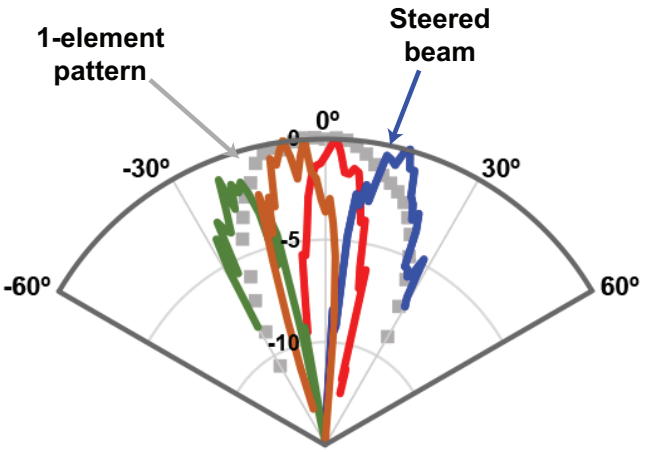


Figure 5.38: Measured steered beam pattern.

Table 5.1: Power consumption of transceiver blocks (single-element)

TX mode and RX mode (same power consumption)	
IF distributed amplifiers	72mW
Frequency quadruplers (all 4 stages)	110mW
LO buffers and phase shifters	580mW
Total TX/RX	762mW (measured=750mW)

5.5 Conclusion

In this chapter, a 300GHz-band CMOS bi-directional 4-element phased-array transceiver is introduced. The outphasing technique is used to overcome the low output power issue of the bi-directional subharmonic mixer in the TX mode. The flexible phase generation enables several additional features including LOFT cancellation (TX and RX) and image rejection (RX). The TX and RX achieve 26Gbaud and 18Gbaud symbol rates, respectively. The stacked Vivaldi antenna structure makes it possible to have a good beam steering range as the antenna pitch can be close to the $\lambda/2$ at the RF band. The measured beam pattern demonstrates a coverage from -18° to 18° in the H-plane of the stacked Vivaldi antennas.

Table 5.2: Performance Comparison with State-of-the-Art 300GHz-band Transceivers

	This work	**TokyoTech [44]**	**Hiroshima [40]**	**Hiroshima & NICT [38, 39]**	**UCB [34, 35]**
Process	65nm CMOS	65nm CMOS	40nm CMOS	40nm CMOS	65nm CMOS
RF frequency [GHz]	242-275*	278-304	252-279	290**	240**
Structure	Phased-array	Single-element	Single-element	Single-element	Single-element
Antenna sharing	Yes	No	No	No	No
TX topology	Outphasing	1-path / mixer-last	Power comb.	Power comb.	1-path / tripler-last
Max. baud rate [Gbaud]	TX:26 RX:18	17	TX:28 RX:N/A	TX:21 RX:14	TX:8 RX:8
PDC [W]	TX:0.75 RX:0.75	TX:0.27 RX:0.14	TX:0.89 RX:0.9	TX:1.4 RX:0.65	TX:0.22 RX:0.26
Area [mm^2]	TRX:4.17	TX:1.9 RX:1.9	TRX:11	TX:5.19 RX:3.15	TX:2 RX:2

* Usable frequency band. ** Center frequency.

Chapter 6

Conclusion and Future Work

6.1 Conclusion

This thesis presents novel circuits and techniques to discover reliable, low power, and high performance 300GHz-band CMOS and hybrid transceiver design options. 300GHz-band is expected to be one of the key enablers of 6G technology, but the anticipated system performance requirements are quite difficult to achieve using CMOS process with acceptable chip area and power consumption. Facing the design challenges in the 300GHz-band phased-array transceivers, this thesis provides a detailed design methodology and novel possible solutions.

Both system-level and circuit-level considerations are discussed for realizing 300GHz-band links with good performance. Several frequency multiplier circuit techniques are proposed to improve the conversion gain and the output power without increasing the chip area, the complexity, and the power consumption. Furthermore, techniques to suppress balun mismatches that always appear in the differential systems are proposed to improve the circuit block and the system overall performance. Single-ended and differential frequency multipliers are introduced in details, and their effect on reducing the system power consumption is also demonstrated.

To simplify the 300GHz-band transceiver system and to reduce its power consumption, a high-conversion-gain subharmonic mixer is proposed. The mixer supports bi-directional operation and provides good linearity and wide bandwidth due to its passive switching architecture. The conversion gain of the mixer is around -16.5dB and it OP1dB is -16dBm. The proposed mixer is used to build a low power 300GHz-band transceiver system that achieves 34Gb/s data rate over a 1cm distance while consuming a total DC power of less than 410mW.

Higher data rate performance is possible by adding amplifiers to the CMOS mixer-last

TX mixer-first RX system due to the improved linearity and noise figure, so InP amplifiers are added to the CMOS transceiver. The proposed hybrid transceiver achieves much better SNDR and the maximum data rate is extended to 56Gb/s. The hybrid transceiver SNDR is high enough to achieve 30Gb/s using 64QAM modulation proving the difficulty of the CMOS-only wireless link implementation. Although the power consumption and area are increased by adding the InP amplifiers, the availability of the CMOS part enables many options such as system on chip and on-chip processing.

To reduce the manufacturing cost of the 300GHz-band phased-array transceivers that include several elements, the bi-directional architecture is introduced in this work. The bi-directional characteristics of the proposed mixer makes it possible to share all the chip components and the antennas between the transmitter and the receiver. The improved average output power of the transmitter by applying the outphasing technique to the passive mixers RF ends contributes to a good array performance with medium antenna gain. The proposed phased-array transceiver demonstrates a 36° beam angle range. With the proposed techniques, the required core area for a single-element is 4.17mm^2.

To summarize, this thesis introduces novel techniques for improving system SNDR, power consumption, and area. The introduced 300GHz-band transceiver and phased-array could be considered as early demonstrations of the circuits to be used in the future 6G networks.

6.2 Future Directions

The 6G technology has the 300GHz-band within its scope to achieve extremely high data rate communication exceeding 100Gb/s. However, the propagation models and characteristics of the 300GHz-band need to be studied and tested thoroughly so that the suitable network topologies can be designed. In addition, baseband circuits such as ADCs, DACs, and digital processing circuits must provide ultra-wideband operation while consuming low power and small area. Some 6G applications will require data rates higher that 100Gb/s, calling for the usage of spectrum efficient techniques such as multiple-input and multiple-output (MIMO). For example, dual-polarization MIMO can be used to double the data rate while using the same frequency band. Phased-array implementation is then used to extend the communication distance. To have a simple idea of how high the data rate can be, we assume that the full 69GHz bandwidth of the IEEE Std. 802.15.3d can be used, and hence, 56.32Gbaud symbol rate is possible. The achievable data rates in this case for BPSK (maximum EVM=6.8dB), QPSK (maximum EVM=9.8dB), 16QAM (maximum EVM=16.5dB), 64QAM (maximum EVM=22.5dB), and 256QAM (maximum EVM=28.5dB) are 56.32Gb/s, 112.64Gb/s, 225.28Gb/s, 337.92Gb/s, and 450.56Gb/s,

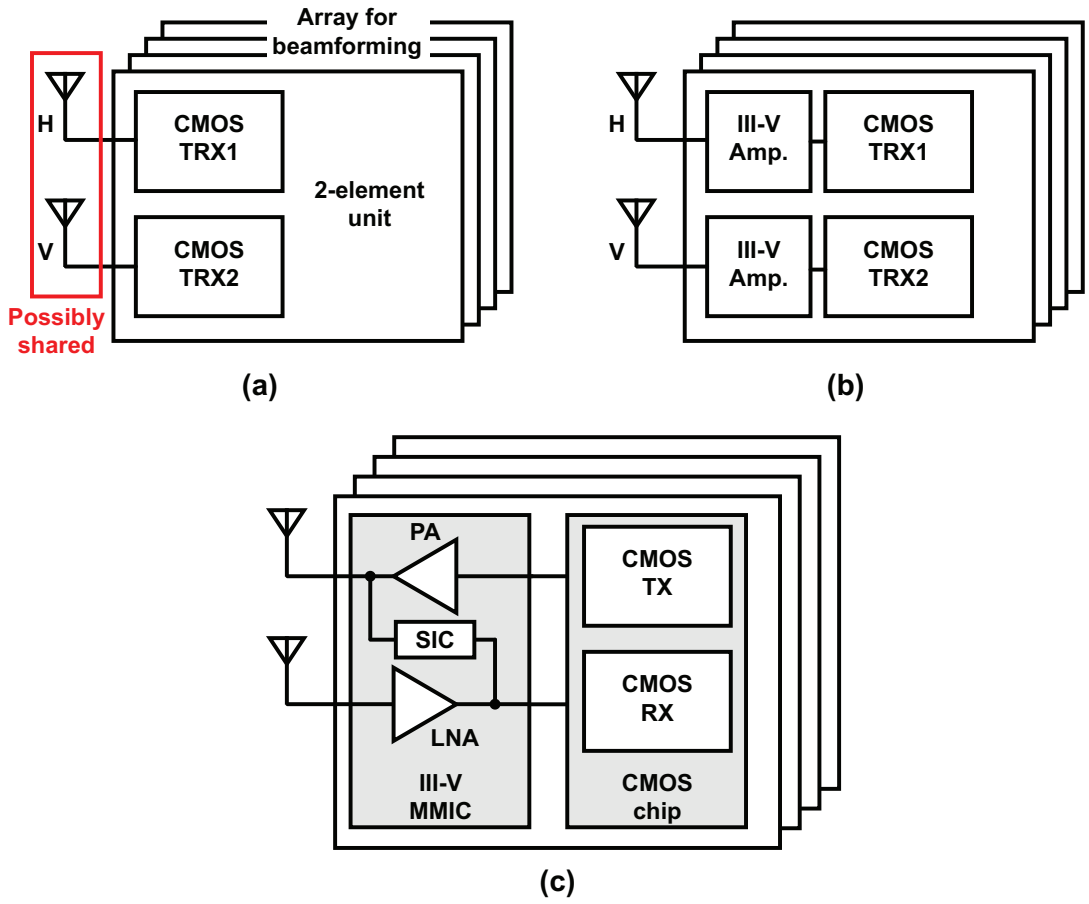


Figure 6.1: Potential 6G transceiver architecture options. (a) CMOS-only phased-array with dual-polarization. (b) Hybrid phased-array with dual-polarization. (c) Full-duplex hybrid phased-array.

respectively. However, 64QAM and 256QAM SNDR requirements are too difficult to satisfy in this situation due to the extremely wide bandwidth that results in a high noise floor and the large path loss. III-V semiconductor devices can be used along the CMOS process as demonstrated in section 4.4 to achieve the required SNDR, but the output power and noise figure of the III-V components must be improved. Now by applying the MIMO method to a system that supports a 69GHz bandwidth and 256QAM modulation scheme, the data rate will become as high as 901.12Gb/s, which is not too far from 1Tb/s.

For the baseband processing, the ADC and DAC may limit the system performance as the required sampling rates and analog bandwidth are extremely high and difficult to achieve, so some relaxing techniques such as frequency interleaving can be used. a fully III-V semiconductor RF front-end (ADCs, mixers, and amplifiers) can be and option for some applications that do not prioritize the low power consumption and chip area

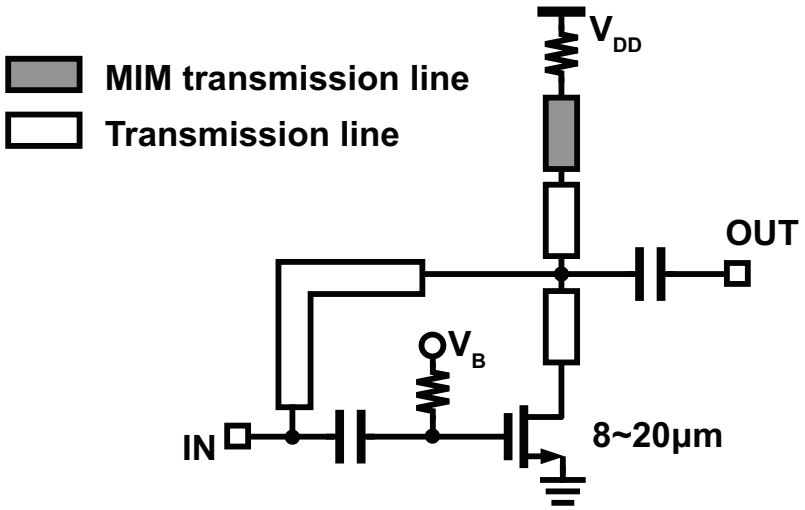


Figure 6.2: 300GHz-band CMOS amplifier circuit.

requirements.

The communication distance limitation at 300GHz-band is expected to be faced by using lower frequency bands to fulfill the extreme coverage requirements of the 6G technology. However, a communication link over 100m distance can be implemented by utilizing high-gain optical lens antennas which can provide more than 50dBi gain. RF amplification is a must to successfully implement such systems, so the hybrid transceiver architecture is most likely the suitable option here.

Another parameter that is required to be minimized in 6G is the latency. The full-duplex architecture reduces the latency compared to the time-division duplexing as the transceiver transmits and receives at the same time without TX/RX switching delays. However, self-interference cancellation (SIC) techniques are required to avoid SNDR degradation. The full-duplex system requires separate implementation of TX and RX, so larger area is expected for this system. The 6G 300GHz-band transceiver options are illustrated in Fig. 6.1.

In the following part of the section, some possible improvements on the 300GHz-band transceiver systems to meet the 6G expected requirements are introduced.

6.2.1 Boosting the Output Power

The absence of a PA at the output of the transmitter degrades the SNDR characteristics, and hence, the maximum data rate and communication distance. Placing a frequency multiplier as the last stage before the antenna is still the best option for realizing high output power [34, 40, 41], but the constellation distortions and the undesired harmonics

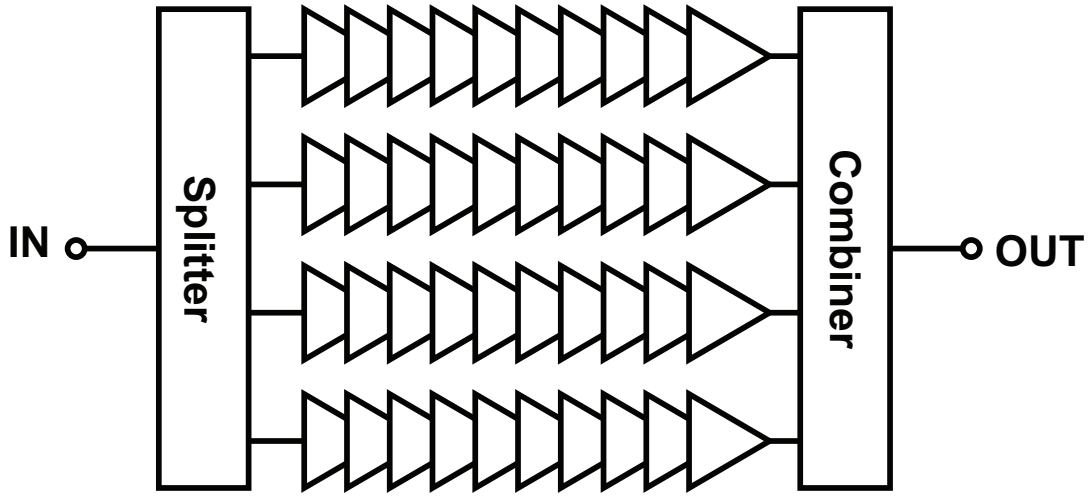


Figure 6.3: Possible CMOS 300GHz-band power amplifier structure.

are very big obstacles to overcome for such implementation.

On the other hand, the recent demonstrations of CMOS amplifiers that operate around 300GHz [53, 54] have proven that it is still possible to realize CMOS amplification at the 300GHz-band using special techniques. Fig. 6.2 shows the schematic of a single stage that provides the maximum achievable gain for amplification at high frequencies. The positive feedback is used to generate the optimal voltage gain and phase of the transistor so that the maximum output power conditions are met. It can be observed here that a small transistor size (8–20μm) is required to get the highest $f_{\max}$ as the positive feedback cannot increase that value. As a result, the gain and linearity of a single stage are not enough to provide the desired improvement of the system SNDR. So, cascading many stages is a must to get acceptable gain and bandwidth, while parallel connection of these cascaded stages is a must to improve the linearity of the amplifier. Fig. 6.3 illustrates a possible architecture for the CMOS 300GHz-band amplifiers. Such implementation also suffers from large area requirements and combiner losses, but it can be a very important solution for certain applications.

6.2.2 Two Dimensional Phased-Array

The phased-array transceiver proposed in this thesis utilizes the stacked structure to enable a relatively wide steering range in one dimension (or plane). However, adding more elements to the stacked array to improve the array gain and the output power is limited by the external components and the PCB/connector structure. Hence, to increase the number of elements, two-dimensional orientation can be considered. Fig. 6.4 shows the possible

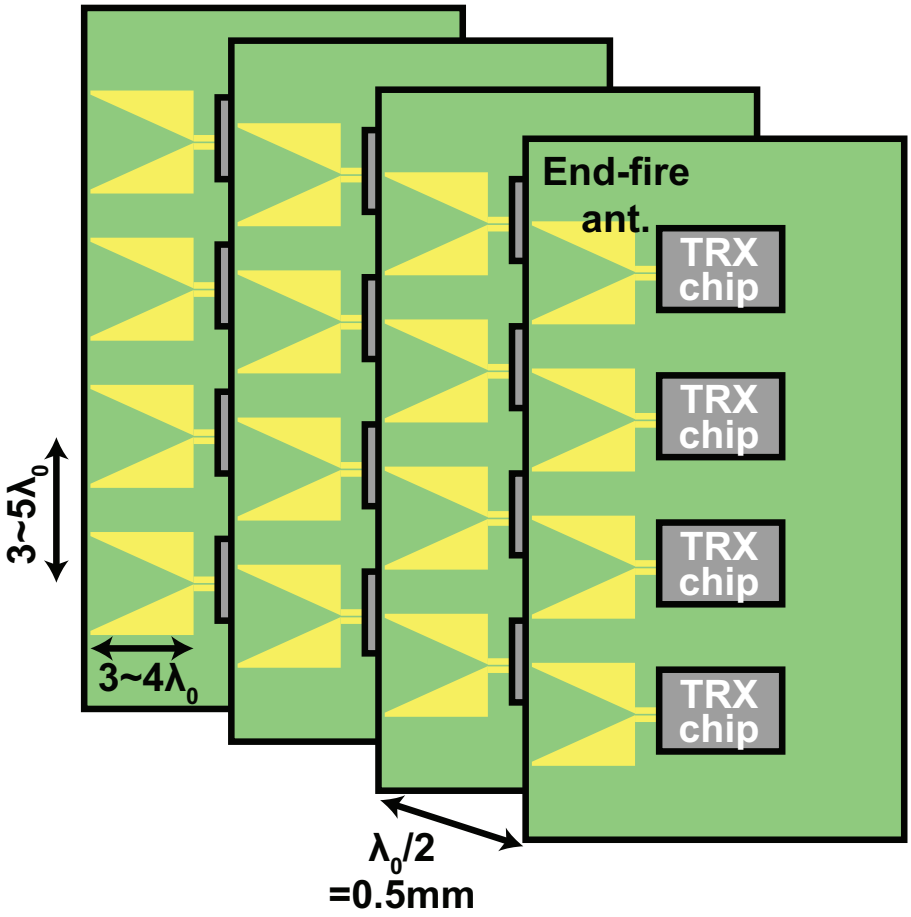


Figure 6.4: Two-dimensional array implementation using stacked PCBs.

implemented structure of a two-dimensional phased-array. Additional elements are placed in every PCB in the stack, and on-PCB dividers can be designed to apply the LO and IF signals. This way, the EIRP of the array improves by a total of 12dB. However, the beam steering in the vertical direction is not possible due to the long antenna pitch.

For a wider steering angle and E-plane/H-plane coverage, a patch array similar to the one introduced in section 2.5, Fig.2.5(b) should be considered with careful consideration of the Connections between the CMOS chips and the antennas. Several on-chip Vivaldi antennas implemented on the same chip and stacked as in Fig. 6.4 is also a possible solution, but the number of adjacent elements will be limited by the chip size.

6.2.3 Options for Enhanced Implementation

Flip chip implementation is used as the main method for CMOS-Antenna and CMOS-transition connection in this thesis. The reason behind this choice as mentioned in the

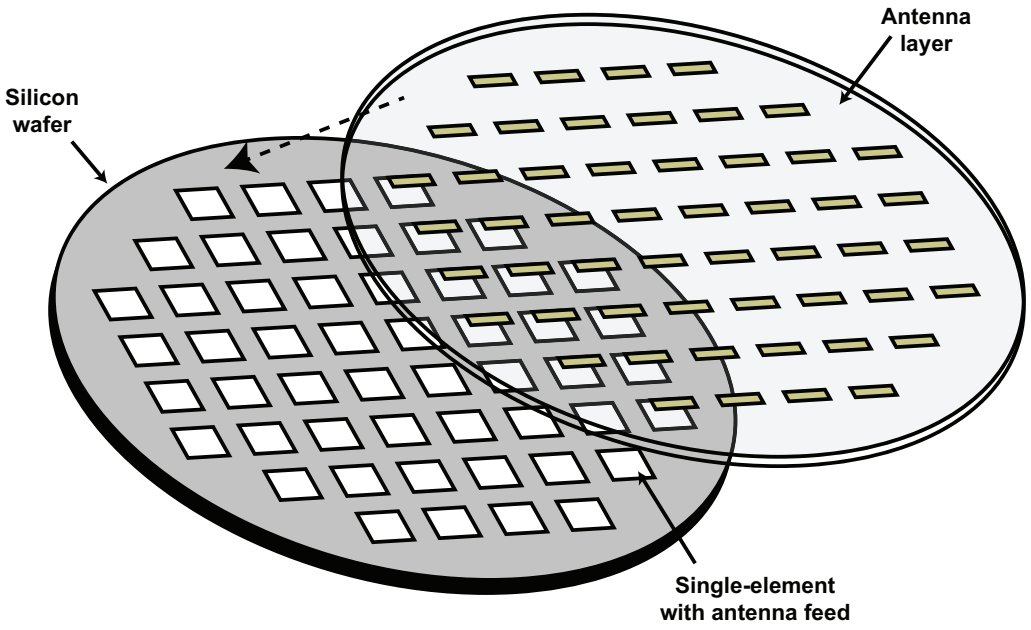


Figure 6.5: Wafer-scale phased-array concept.

earlier chapters is the short bump compared to the wavelength. The flip chip technology surely is much better than the wire bonding at 300GHz, but there are several other technologies that may be more reliable than the flip chip process if optimized in a suitable way.

Wafer level chip size packaging (WLCSP) and wafer-scale phased-arrays are being used recently to implement high performance millimeter-wave phased-arrays as in [94, 95]. The trade-off between the chip cost and the PCB cost is one of the main considerations before choosing the suitable packaging option. Smaller chips may cost less due to the high yield, but an expensive PCB is required to implement the high frequency connections. On the other hand, a wafer-scale phased-array has all the high-frequency connections on-chip, but the chip area is very large. The wafer-scale phased-array concept is shown in Fig. 6.5. This concept has been applied successfully for frequencies as high as 440GHz [94].

The small antenna size also enables the on-chip antenna and the on-chip array options. At 300GHz, the wavelength is 1mm, and that means that the antenna dimensions can be in the order of several hundred μm. Several works have demonstrated on-chip array implementation for radiators as in [57–61], but the low resistivity of the silicon substrate causes the antenna efficiency to drop heavily. To solve this issue, ion irradiation is a very promising solution, as it has been already used to improve the on-chip dipole antenna efficiency successfully as in [96].

6.2.4 Hybrid Transceiver Board/Module

It is shown in section 4.4 that very high performance can be achieved using a CMOS-InP combination given that a low-loss connection is utilized between the two chips. There are several options in this regard, but firstly we can rule out the wire bonding due to its inductance, loss, and effect on the matching. Both chips can be attached to a board in a flip chip fashion, but PCB connecting line requirements to achieve reasonable connection loss can be very strict considering the small PAD dimensions normally used in 300GHz-band chips.

Hence, a novel implementation technique must be considered to improve the hybrid transceiver overall SNDR. On-PCB implementation can be based on the flip chip process with some techniques to reduce the distance between the CMOS chip and the InP chip, while module implementation can utilize the metal structure to provide a good transition between the two chips.

6.2.5 Maximizing the Data Rate to Leverage the Wide Bandwidth

The bandwidth defined by IEEE Std. 802.15.3d is extremely wide and its widest channel covers around 69GHz. If we assume that a transceiver can operate over the whole band with an SNDR enough to get low BER even when 16QAM is used, around 220Gb/s data rate becomes possible without additional techniques. This kind of system is still out of reach for the current technologies, but some improvements on the system architecture and blocks may open the door for such implementation:

- Wideband IF amplifiers: The bandwidth of the mixer-last TX mixer-first RX systems is limited by the IF amplifiers as the mixer bandwidth is quite wide. Distributed amplifiers as shown in Chapter 5 provide very wide bandwidth, but the gain is quite limited for the simple types.

- Direct conversion: The systems in this thesis focus on heterodyne transceiver architecture, so the whole RF bandwidth is required to be supported in the IF amplifiers. By using direct conversion, the required bandwidth of the baseband amplifiers becomes half of the RF bandwidth, saving the trouble to be faced in the 70GHz distributed amplifier design. However, direct conversion transceivers suffer from several issues including I/Q mismatch and DC offsets.

- Frequency Interleaving and MIMO: Many techniques can be used to improve the spectrum usage such as frequency interleaving (where several paths are used to up- down-convert the signals) and MIMO (where several signals can be sent at

the same frequency and in the same medium without interference). The system complexity increases by applying these techniques, but the data rate improves by several multiples.

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Appendix A

Publication List

A.1 Journal Papers

- **Ibrahim Abdo**, Carrel da Gomez, Chun Wang, Kota Hatano, Qi Li, Chenxin Liu, Kiyoshi Yanagisawa, Ashbir Aviat Fadila, Takuya Fujimura, Tsuyoshi Miura, Korkut Kaan Tokgoz, Jian Pang, Hiroshi Hamada, Hideyuki Nosaka, Atsushi Shirane, and Kenichi Okada "A Bi-Directional 300GHz-Band Phased-Array Transceiver in 65nm CMOS with Outphasing Transmitting Mode and LO Emission Cancellation," IEEE Journal of Solid-State Circuits (JSSC), Vol. , No. , (under review).

- **Ibrahim Abdo**, Korkut Kaan Tokgoz, Atsushi Shirane, Kenichi Okada, "F-band Frequency Multipliers with Fundamental and Harmonic Rejection for Improved Conversion Gain and Output Power," IEICE Transactions on Electronics, Vol. advpub, 2021.

- **Ibrahim Abdo**, Hiroshi Hamada, Hideyuki Nosaka, Atsushi Shirane, Kenichi Okada, "64QAM Wireless Link with 300GHz InP-CMOS Hybrid Transceiver," IEICE Electronics Express, Vol. 18, No. 17, pp. 1-4, 2021.

A.2 International Conferences and Workshops

- **Ibrahim Abdo**, Carrel da Gomez, Chun Wang, Kota Hatano, Qi Li, Chenxin Liu, Kiyoshi Yanagisawa, Ashbir Aviat Fadila, Jian Pang, Hiroshi Hamada, Hideyuki Nosaka, Atsushi Shirane, Kenichi Okada, "A 300GHz-Band Phased-Array Transceiver Using Bi-Directional Outphasing and Hartley Architecture in 65nm CMOS," IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers, San Francisco, CA, Feb. 2021, pp. 316-318.

- **Ibrahim Abdo**, Takuya Fujimura, Tsuyoshi Miura, Korkut K. Tokgoz, Atsushi Shirane, Kenichi Okada, "A 0.41W 34Gb/s 300GHz CMOS Wireless Transceiver," IEEE/ACM Asia South Pacific Design Automation Conference (ASP-DAC), Tokyo, Japan, Jan. 2021, pp. 3-4.

- **Ibrahim Abdo**, Takuya Fujimura, Tsuyoshi Miura, Korkut Kaan Tokgoz, Hiroshi Hamada, Hideyuki Nosaka, Atsushi Shirane, and Kenichi Okada "A 300GHz Wireless Transceiver in 65nm CMOS for IEEE802.15.3d Using Push-Push Subharmonic Mixer," IEEE MTT-S International Microwave Symposium (IMS), Los Angeles, CA, June 2020, pp. 623-626.

- **Ibrahim Abdo**, Takuya Fujimura, Tsuyoshi Miura, Atsushi Shirane, and Kenichi Okada, "A 300GHz Dielectric Lens Antenna," IEEE Global Symposium on Millimeter Waves (GSMM), Sendai, Japan, May 2019, pp. 17-19.

- **Ibrahim Abdo**, Korkut Kaan Tokgoz, Takuya Fujimura, Kenichi Okada, Akira Matsuzawa, "A 100-123GHz CMOS frequency doubler with 5.5dBm output power and high fundamental rejection," IEEE Int. Symp. on Radio-Frequency Integration Technology (RFIT), Seoul, Korea, Aug. 2015, pp. 138-140. (Best student paper award)

- **Ibrahim Abdo**, Korkut Kaan Tokgoz, Takuya Fujimura, Kenichi Okada, Akira Matsuzawa, "Comparison Between L-2L and Thru-Reflect-Line De-embedding Methods for W-Band CMOS Amplifier Design," IEEE Int. Symp. on Radio-Frequency Integration Technology (RFIT), Seoul, Korea, Aug. 2015, pp. 34-36.

A.3 Domestic Conferences and Workshops

- **Ibrahim Abdo**, Korkut Kaan Tokgoz, Takuya Fujimura, Jian Pang, Atsushi Shirane, Kenichi Okada "CMOS Transistor Layout Optimization for Sub-THz Amplifier Design," 2019 IEICE Society Conference, Osaka University, Osaka, C-12-33, Sep. 2019.

- **Ibrahim Abdo**, Korku Kaan Tokgoz, Shotaro Maki, Jian Pang, Takuya Fujimura, Atsushi Shirane, Kenichi Okada, "A 120Gb/s 16QAM CMOS W-band Frequency-Interleaved Wireless Transceiver," LSI and System Workshop 2018, The University of Tokyo, Tokyo, May 2018.

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A.4 Co-Author

A.4.1 Journals and Letters

- Hiroshi Hamada, Takuya Tsutsumi, Hideaki Matsuzaki, Takuya Fujimura, **Ibrahim Abdo**, Atsushi Shirane, Kenichi Okada, Go Itami, Ho-Jin Song, Hiroki Sugiyama, and Hideyuki Nosaka "300-GHz-band 120-Gb/s Wireless Front-end Based on InP-HEMT PAs and Mixers," IEEE Journal of Solid-State Circuits (JSSC), Vol. 55, No. 9, pp. 2316 - 2335, Sep. 2020.

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A.4.2 Conferences

- Hiroshi Hamada, Takuya Tsutsumi, Hiroki Sugiyama, Hideaki Matsuzaki, Ho-Jin Song, Go Itami, Takuya Fujimura, **Ibrahim Abdo**, Kenichi Okada, and Hideyuki Nosaka "Millimeter-wave InP Device Technologies for Ultra-high Speed Wireless Communications toward Beyond 5G," IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, Dec. 2019.

- Jian Pang, Korkut Kaan Tokgoz, Shotaro Maki, Zheng Li, Xueting Luo, **Ibrahim Abdo**, Seitarou Kawai, Hanli Liu, Bangan Liu, Makihiko Katsuragi, Kento Kimura, Atsushi Shirane, Kenichi Okada "A 28.16-Gb/s Area-Efficient 60GHz CMOS Bi-Directional Transceiver for IEEE 802.11ay," IEEE Asian Solid-State Circuits Conference (A-SSCC), Tainan, Taiwan, Nov. 2018, pp. 77-78.

- Hiroshi Hamada, Takuya Fujimura, **Ibrahim Abdo**, Kenichi Okada, Ho-Jin Song, Hiroki Sugiyama, Hideaki Matsuzaki, Hideyuki Nosaka, "300-GHz, 100-Gb/s InP-HEMT Wireless Transceiver Using a 300-GHz Fundamental Mixer," IEEE MTT-S International Microwave Symposium (IMS), Philadelphia, PA, June 2018, pp. 1480-1483.

- Korkut K Tokgoz, Shotaro Maki, Jian Pang, Noriaki Nagashima, **Ibrahim Abdo**, Seitaro Kawai, Takuya Fujimura, Yoichi Kawano, Toshihide Suzuki, Taisuke Iwai, Kenichi Okada, Akira Matsuzawa, "A 120Gb/s 16QAM CMOS Millimeter-Wave Wireless Transceiver," IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers, San Francisco, CA, Feb. 2018, pp. 168-169.