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Study of High Temperature and High Efficiency Operation of Membrane Photonic Integrated Circuits on Si Substrate

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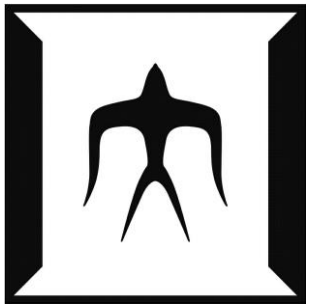

A DOCTORAL DISSERTATION

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Study of High Temperature and High Efficiency Operation of Membrane Photonic Integrated Circuits on Si Substrate

Contents

Chapter 1 Introduction

Chapter 2 Thermal characteristics analysis for membrane semiconductor laser

Chapter 4 Membrane laser for low thermal resistance and high temperature operation

Chapter 5 Membrane photonic integrated circuits fabricated by surface activated bonding

Chapter 1

Introduction

1.1 Introduction

The development of optical fiber communication is accompanied by the popularization of global network communication. Undersea fiber optic cables enable high-speed connections between continents. Today, optical communication technology is gradually moving from long-distance optical communication to short-distance optical communication. Cables in datacenters are being replaced by optical fibers, which not only saves space but also improves transmission capacity. Therefore, optical modules including transmitter, modulator, Multiplexer/Demultiplexer (MUX/DeMUX), detector are getting huge demand. Comparing with the conventional optical modules using discrete components, the Si-photonics can achieve high-level of integration and the mature VLSI (very-large-scale-integrated circuits) fabrication process can be applied with slight modification to the large-scale production of Si-photonics. However, due to the in-

direct bandgap of Si, efficient light emission is difficult. To enhance the level of integration and performance of Si-photonics, the III-V-on-Si hybrid integration technology has been developed recent years, consisting of wafer bonding and direct growth on Si. Among many optical components, semiconductor lasers play an important role. A high-speed and low power consumption laser is the key in optical interconnection, extremely in on-chip optical interconnection. The downscaling of transistor increases the speed of LSI, but the same is not true for the interconnection. The propagation delay was limited by the RC time constant and material, which is so called interconnect bottleneck in VLSI. One way to solve this problem may be the optical interconnect using photons as bits of information propagate in waveguide with less heat dissipation and low delay. For this purpose, hybrid integration of a low power consumption photonic integrated circuits on Si-LSI is need. In this thesis, a membrane structure-based photonics integrated circuit (MPIC) on Si-substrate using modified room temperature surface activate bonding was studied for on-chip interconnection.

In this chapter, the motivation of research of direct bonded MPICs using membrane DFB lasers and related background and technology will be discussed. Section 1.2 briefly introduces the development of optical communication especially the fiber communication. The interconnect bottleneck in electrical wiring of LSI will be given in section 1.3, and the novel electrical interconnect and optical interconnect will be introduced. The optoelectronic devices relay on the fiber communication development will be described in section 1.4. Section 1.5 described the wafer bonding technologies for photonic integration. Section 1.6 introduced photonic integrated circuits and laser integration to Si-substrate. Section 1.7 gives the brief study overview of semiconductor membrane laser in our group and the other group. Finally, problems remained in previous work and the objectives of this thesis will be given in the section 1.8.

1.2 Development of optical communication systems

In 1880, A. G. Bell, an American telephone inventor, has already studied and successfully transmitted and received optical telephones. In 1881, Bell wrote a paper entitled "On the Production and Reproduction of Sound by Light"[1] reporting on his "photophone" device. Unfortunately, Bell's photophone has never been practical. Because it had some flaws that prevented it from being practical:

(1) No reliable, high-intensity light source.

(2) No stable, low loss transmission medium.

In 1917, Einstein published an article "The Quantum Theory of Radiation"[2], which theorized that when light interacts with matter, in addition to absorption and spontaneous emission, there is a third process—"stimulated radiation". Based on this concept, MASER (Microwave Amplification by Stimulated Emission of Radiation) came out, and many research groups have thought that the since MASER can be manufactured in the microwave frequency band, can the population inversion be realized in the higher frequency band to build a LASER in the light wave band? C. H. Townes believed that the lasing of light was natural progression of MASER, so he called the device "Optical MASER". The paper "Infrared and Optical MASERs"[3] published in 1958 written by Schawlow and Townes predicted theoretically that the feasibility of laser for the first time, and the laser output generated by optical pumping of potassium vapor was analyzed in detail when the Fabry-Pert cavity acted as a resonant cavity.

On May 16, 1960, Theodore Maiman stood out from dozens of research groups in the world and made the first laser in human history[4]. Figure 1.1 shows the structure of ruby laser designed by T. Maiman. A Spiral pump lamp coated by silver reflects all the light black to the inserted ruby rod that acted as a gain medium in the middle of the spiral tube. At the same time, he plated silver on both sides of the ruby crystal, and cut a small hole in one of them, so that the light could be partially transmitted, and the resonator was ready. In this way, all three elements of laser are in place: the spiral flash lamp as the pimp source, the ruby crystal as the gain medium, and the Fabry-Perot cavity as the resonator.

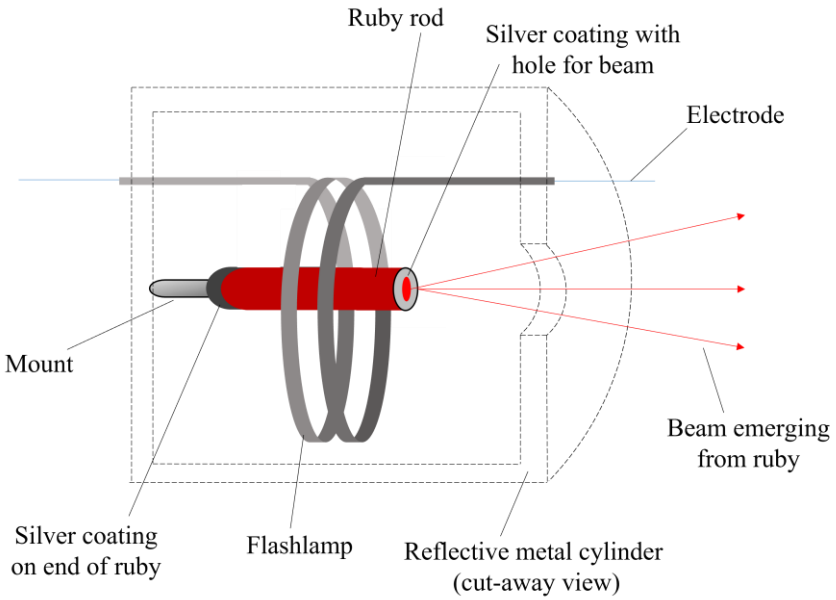


Fig. 1.1 Structure of ruby laser designed by T. Mainman

The world's first laser enables people to have a new light source with narrow spectrum linewidth and high brightness, bringing new hope to optical communication. Early waveguide optical communication used light transmission methods such as hollow optical waveguide, thin film optical waveguide, and lens array optical waveguide. Due to the large size of these optical waveguide systems, it is inconvenient to install and use, and can only be effectively transmitted when the beam is strictly aligned with the axis of the pipeline, which is difficult to achieve for long-distance communication, so it has not been practically applied and promoted.

In 1966, British-Chinese scholars C. K. Kao and C. A. Hockham published a paper " Dielectric-fibre surface waveguides for optical frequencies"[5] on the new concept of transmission medium, pointing out that the possibilities and technical approaches for information transmission by using of optical fiber have laid the foundation of modern optical communication ---- optical fiber communication. It indicates the development direction of "low loss optical fiber for long-distance communication can be produced through the purification of raw materials".

In 1970, a major breakthrough was made in the development of optical fibers. Corning's F. P. Kapron et al. announced that they had succeeded in prototyping and

commercializing a 20 dB/km low-loss optical fiber[6]. The global challenge to make a low-loss fiber was accepted by many teams[7]-[12]. In 1986, the minimum loss was 0.154 dB/km[13] at 1.55-1.56 μm achieved by Sumitomo Electric using pure-silica-core fiber (PSCF). And they commercialized PSCF with a low loss of 0.17 dB/km in 1988 under the trade name "Z fiber". Then, by reducing the density fluctuation of pure silica core, an extremely low loss of 0.14 dB/km was realized in 2018[14].

In 1970, at the same time, substantial progress has been made in optical fiber communication light sources. The room-temperature operation of GaAlAs heterostructure semiconductor laser was achieved[15], which laid the foundation for the development of semiconductor lasers. In 1979, Tokyo Institute of Technology, Kokusai Denshin Denwa Co. Ltd. (KDD), Nippon Telegraph and telephone corporation (NTT) and bell Labs announced continuous room temperature operation of long wavelength laser one after another[16]-[19]. Long-term reliability is important for practical use. It has been clarified that there is no problem even if the wavelength is as long as 1.55 μm, as with the 1.3 μm band laser. Around this time, research on photodiodes made of InGaAs, which has high sensitivity in the long wavelength band, was also advanced for photodetectors. It can be said that 1979 was a major milestone year from the viewpoint of long-distance fiber optic transmission.

In practical optical fiber communication system development, Bell Labs established a first optical fiber communication system with the data transmission rate of 45 Mbps between Atlanta and Washington in 1976. The light-emitting diode (LED) light source with a wavelength of 0.85 μm and multimode optical fiber were used in this system. Japan has successively carried out experiments on a step-index (SI) multimode optical fiber communication system with a rate of 34 Mbps and a gradient-index (GI) multimode optical fiber communication system with a rate of 100 Mbps in 1976 and 1978. The Japan Transit Optical Fiber Network was constructed in 1985. Subsequently, the first transatlantic TAT-8 submarine optical cable communication system initiated by the United States, United Kingdom and France was completed in 1988. The first trans-Pacific TPC-3/HAW-4 submarine optical cable communication system was built in 1989. Since

then, the construction of the submarine optical cable communication system has been carried out in an all-round way, which has promoted the development of the global communication network.

Looking at the overall situation, modern optical fiber communication can be divided into 6 generations.

First generation (1966 ~ 1979): Development period from basic research to commercial application. The system used 0.8 μm wavelength GaAs semiconductor lasers and multimode fibers and operated at 45 Mbps with the repeater spacing of 10 km and became commercially available in 1980[20]. Multimode dispersion and loss of fiber are keys to limit the repeater spacing.

Second generation (early 1980s): Great development period that aims to improve the transmission rate and increase the transmission distance (by reducing fiber dispersion). The system used 1.3 μm wavelength GaInAsP semiconductor lasers and single mode fiber and operated at 1.7 Gbps with the repeater spacing of 50 km. Fiber losses in 1.3 μm (0.5 dB/km loss) limited the repeater spacing.

Third generation (late 1980s and early 1990s): A period in which new technology research is carried out with the goal of ultra-large capacity and ultra-long distance (by reducing fiber loss). The system used 1.55 μm wavelength GaInAsP semiconductor lasers and single mode dispersion-shifted fiber and operated at 2.5 ~ 10 Gbps with the maximum repeater spacing of 100 km. The electronic repeater is the drawback of 1.55 μm system typically by 60 ~ 70 km. The coherent system can improve the receiver sensitivity which can increase repeater spacing. Such system was under development during 1980s, and commercially used with the advent of fiber amplifier.

Fourth generation (after the 1990s): Long repeater spacing by making use of optical amplification and high capacity by making use of wavelength-division multiplexing (WDM). The fiber losses are compensated using erbium-doped fiber amplifiers (EDFA) every 60 ~ 80 km in most wavelength division multiplexing (WDM) system. The data transmission over 14,000 km at 5 Gbps using recirculating-loop configuration was experimentally showed in 1991[21]. This performance reveals that intercontinental

communication can be realized using an amplifier based all optical submarine transmission system.

Fifth generation (after the early 2000s): In EDFA-based multi-relay long-distance transmission systems, the received optical power remains constant, so the importance of high receiving sensitivity of coherent optical receivers has diminished, and research and development of coherent optical communication has been suspended worldwide. The capacity of optical transmission systems using the intensity modulation-direct detection (IM / DD) method using EDFA and WDM technology has rapidly increased in fourth generation, however, when transmitting a high-speed signal such as 100 Gbps over a long distance, the distortion characteristics (wavelength dispersion, polarization mode dispersion) of the optical fiber have a great influence on the signal transmission, and the conventional IM-DD method limits the transmittable distance. For this reason, research on DPSK (differential phase shift keying) or DQPSK (differential quadrature phase shift keying) transmission method has regained attention, and in 2005, a new concept of digital coherent receivers was introduced, which solves the technical difficulties of conventional coherent receivers by combining phase diversity homodyne receivers and high-speed digital signal processing. A 600 Gbps digital coherent transmission has practically used so far[200].

Sixth generation (future): It is estimated that the maximum transmission capacity of the current single mode fiber (SMF) is about 100 Tbit / s from the viewpoint of the limit of frequency utilization efficiency improvement and the band limitation of the optical amplifier[201]. Under these circumstances, aiming for large-capacity transmission of petabit class and even exabit class, in addition to time division multiplexing (TDM) and WDM, research and development on the expansion of transmission capacity by introducing space division multiplexing (SDM) is being actively carried out. A few-mode Fiber (FMF) that propagates a plurality of modes in one core and a multi-core fiber (MCF) in which cores in the same cladding are arranged have been proposed. FMF can transmit different information for each mode, and MCF can transmit different information to each core for spatial multiplexing.

Optical interconnects are becoming mainstream within data centers, and the original copper wires are gradually being replaced by optical fibers. The evolution of optical interconnection into the computer system, from the rack level, board level to chip level, promotes the continuous breakthrough of computer architecture in speed. Moore's Law is still in effect, driving the continuous improvement of processor performance. The internal and external I/O interconnection performance of computer systems is far lower than the processor performance, becoming the bottleneck of computer systems. Links based on copper wire interconnection have obvious bottlenecks at rates above 10 Gbps, and the interconnection between equipment racks, boards, board modules, and between chips cannot meet the requirements of rapidly growing demands for computing and data. The optical interconnect was introduced to where it deserves to be introduced. However, in ultra-short distance communication, the electrical interconnect still dominates. If the optical interconnect can be improved faster in speed and power consumption lower than electrical interconnect in ultra-short distance communication, a great improvement of data processing capacity of the computer system can be expected.

1.3 On-chip interconnect

Driven by Moore's Law, the goal of chip development is always higher performance, lower power consumption and lower cost by higher integration. As the number of transistors integrated on a single chip is increasing, the process nodes are getting smaller and smaller, the tunneling effect is gradually obvious, and the leakage or uniformity problems are becoming more and more prominent, resulting in the frequency increase approaching the bottleneck. In order to further improve the system performance, the chip is developed from a single core to a multi-core system. The signal interconnect also becomes more complex as nodes getting smaller. To overcome the limitations, such as signal delay and heating, of traditional copper-based electrical interconnects, optical interconnects has begun looking at novel interconnect alternative. In this section, the electrical interconnect bottleneck will be proposed at first, and several novel electrical interconnect and on-chip optical interconnection technologies will be introduced.

1.3.1 On-chip electrical interconnect bottleneck

Moore's Law "The number of elements on one chip doubles in two years" was an empirical prediction, but in fact there is a law that supports the theory is called “scaling law”[23]. The scaling law proposed by R.H. Dennard et al. in 1974 showed that it was possible to improve the performance of integrated circuits by miniaturizing components and became an indicator of the future direction of integrated circuit technology. S is the scaling factor which is used to represent the scaling of transistors. Figure 1.2 shows the concept of scaling in transistor, and Table 1.1 shows the scaling factor. We can know that as the size of device scaling by S, the gate delay and power dissipation are scaled by $1/S$ and $1/S^2$, respectively, that improved the properties of single device.

In wire scaling, we could try to scale interconnect at the same rate S as device dimension. Here, the wiring layer in the LSI is roughly divided into a local wiring for connecting logic devices in the lowest level, semi-global wiring above local wiring have

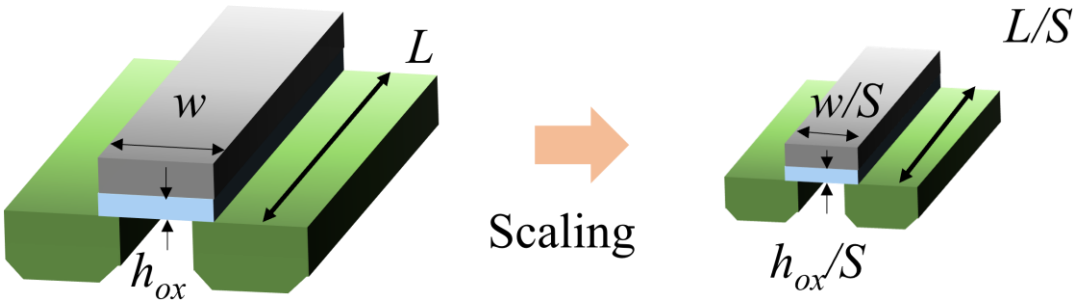


Fig. 1.2 Scaling law on single device

Table 1.1 Scaling factors in single device

Device parameters	Scaling factor
Device dimensions L, w, h_{ox}	$1/S$
Doping concentration	S
Voltage	$1/S$
Field	1
Current	$1/S$
Gate Delay	$1/S$
Device power dissipation	$1/S^2$

larger cross-sectional dimension and a global wiring for connecting system blocks (Fig. 1.3), such as clock signals, buses, etc. The wire scaling makes sense for local wires, however, the global interconnections will not scale in length. The length of global interconnect is proportional to die size or system complexity. S_{chip} expresses this factor. Looking at local interconnect, everything was scaled by $1/S$, including the width of wire W, the height or thickness of wire h, the length of wire L and the distance between wire and ground H. If this is down, the capacitance will be proportional to 1/S, the resistance of wire will be proportional to S, so, the propagation delay RC stays constant. Reminder that the delay of transistors is scaled by $1/S$, therefore, the delay of local interconnect increases relative to transistors. Next, looking at global interconnect. The same time is going to do by scaling S in the parameters of W, h, and H. This time, the L does not be scaled if the chip size does not change. The capacitance will be constant, the resistance of global wire will be scaled by S^2, and hence, the delay RC will be scaled by S^2, that

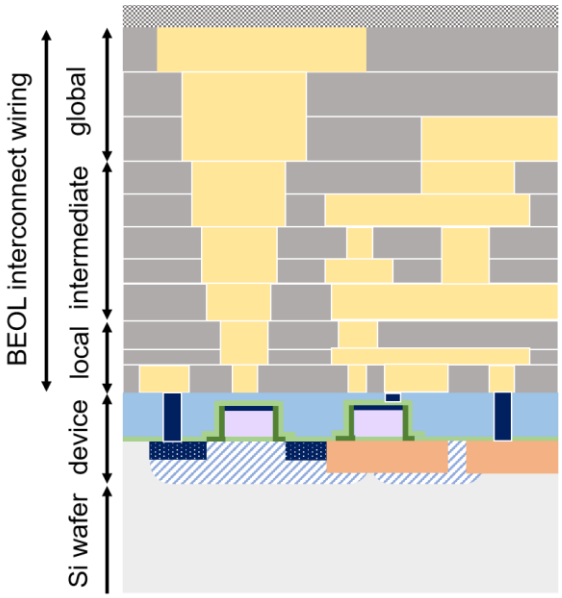
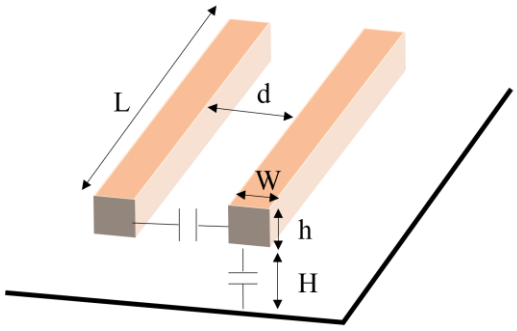


Fig. 1.3 Schematic of electrical interconnects in LSIs.



Parameters	Scaling factor (Local wire)	Scaling factor (Global wire)
L	$1/S$	S_{chip}
W, d	$1/S$	$1/S$
H, h	$1/S$	$1/S$
Resistance R	S	$S^2 \cdot S_{chip}$
Capacitance C	$1/S$	S_{chip}
RC delay	1	$(S \cdot S_{chip})^2$

Fig. 1.4 Scaling in local wire and global wire

means the long wire delay really increases, and was cubic larger than the transistor delay. And if the chip size grows, L actually increases. This time, the capacitance C will be scaled by S_{chip} and the RC delay will be scaled by $S^2 \bullet S_{chip}$. Therefore, whereas device speed increases with scaling, local interconnect speed stays constant, and global interconnect delays increase quadratically. The interconnect delay is often the limiting factor for speed of LSI[24]-[25]. One thing can be done is to keep the wire thickness h fixed, which would provide $1/S$ for local wire delays, and S for constant length global wires, but the fringing or coupling capacitance would increase.

The intel group has shown the interconnect length distribution of local and global wire

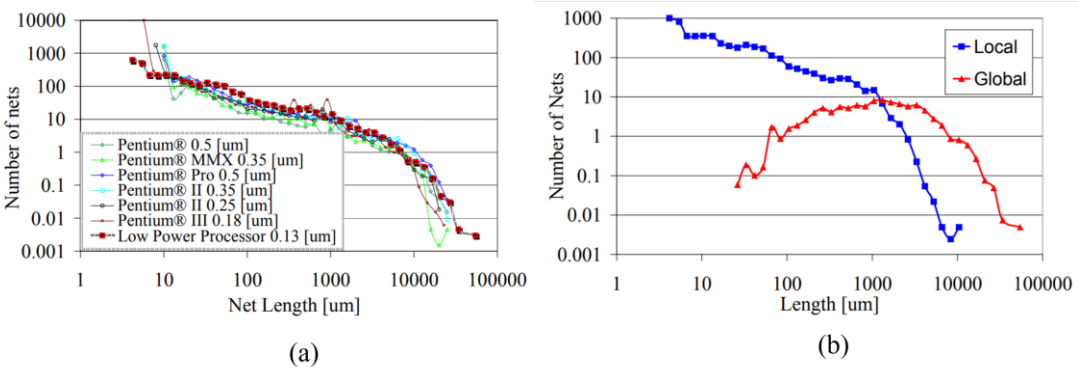


Fig. 1.5 (a) Net length distribution of nets number using seven processors, (b) Interconnect length distribution of local and global nets[26].

using seven real processors (Fig. 1.5). When the net length increases, the number of nets decreases dramatically, which appears in five different generations of technology. Most of the nets are local wires shorter than 1 mm. There are always the long wires near up to cm level, because they are proportional to the die size, and the global wire dominates it. The power consumption of these long global nets is not minor even the number of nets is very small[26].

To solve the problems existing in wire scaling, many methods were proposed, which consists of use of low-*k* insulation, insertion of repeater buffer, and hierarchy of wire. The low-k material is a material with a specific dielectric constant *k* less than 3.0. Since the use of the low *k* material as the insulation film between layers can reduce the capacitance between wirings and suppress the wiring delay. Many low *k* materials with low dielectric constants have been proposed[27]-[30]. However, the mechanical strength is rapidly decreasing using low-*k* material[31].

As the insertion of repeater buffer, figure 1.6 shows a scheme of repeater insertion in metallic interconnection. By inserting the repeaters[32]-[33], long wire L was divided into N section. The total delay will become proportional to the factor $(L/N)^2N$, for the RC delay is proportional to the L^2 in the wire length of L. If the segment N increases, the delay finally will be proportional to the length of L. The signal delay can indeed be reduced with an increase of the numbers of repeaters, however, a large number of repeaters results in increment of power consumption and waste of chip area. Hence, the repeater buffer is

not a solution for problems in global wiring even if it can alleviate the increase of delay.

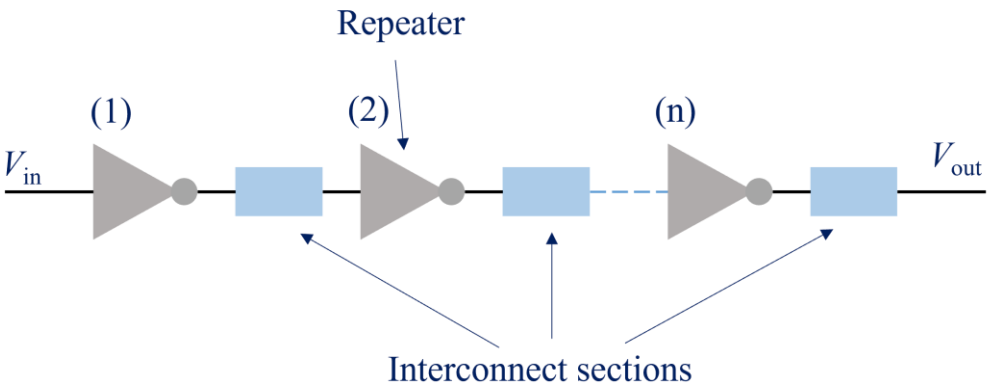


Fig.1.6 Concept of repeater insertion in interconnect

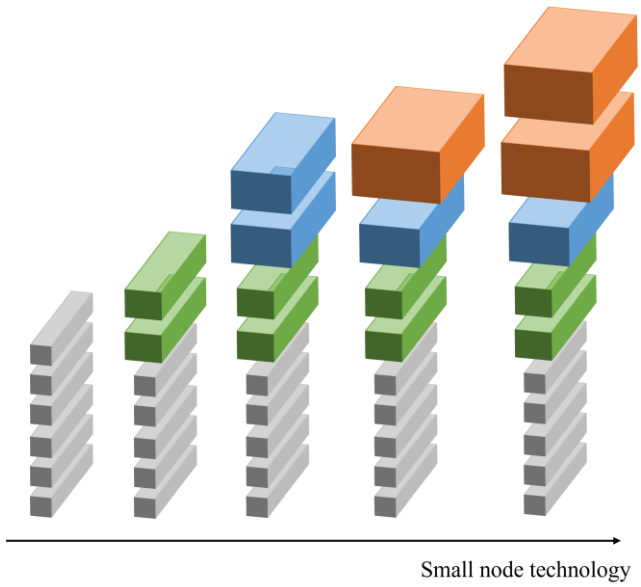


Fig. 1.7 Concept of metal stack growth

About the hierarchy of wire, figure 1.7 shows a concept of metal stack growth. The lower layer metals are used for local interconnect. So, they are thin and dense. The higher layer metals are used for global wire, so they are thicker, wider and spaced farther apart, which has a low delay a low heat. In the left side of Fig. 1.7, all the wires were the same, and with the technology node decreasing, three or four types of metal were used. This hierarchy of wire was also shown in Fig. 1.3. The different layer from local, intermediate to global, has different type of metal size.

1.3.2 Novel on-chip electrical interconnect

To address the issues of the increased latency and power consumption of LSI interconnection in local and global wiring, common methods have been introduced in the previous section. This subsection introduces several novel and electrical based solutions. It contains carbon nanotube (CNT) in the application of LSI interconnection, Three-dimensional integrated circuit, and on-chip differential transmission line.

【***Carbon nanotubes***】

In 1985, the discovery of the "football" structure of C_{60}, so-called “fullerene” attracted worldwide attention[34], and H. W. Kroto, R. E. Smalley, and R. F. Curl also won the 1996 Nobel Prize in Chemistry for the joint discovery of C_{60} and the confirmation and confirmation of its structure. Driven by research on fullerenes, in 1991 an even more exotic carbon structure—carbon nanotubes—was discovered by Dr. Iijima of NEC Corporation[35]. According to International Technology Roadmap for Semiconductors (ITRS) 2013[36], along with the miniaturization of wiring, there is a demand for an increase in the maximum allowable current density to flow through the wiring, and it is necessary to have fine wiring that can withstand higher current densities. Carbon nanotubes (CNTs) and multilayer graphenes (MLGs) are listed as one of the next-generation LSI wiring materials. In addition to application to local wiring, application to via layer (Fig. 1.8) is also considered[37]-[38]. CNT and MLG have high current density resistance over $10^{8\text{-}9}$A / cm^2[39]-[40], low electrical resistance[41]-[43], and high thermal conductivity of over 3000-5000 W / (K • m)[44]-[47]. The thermal resistance is not determined only by the via part but depends on the heat dissipation path including the insulating film, and greatly depends on the proportion of metals and CNTs with high thermal conductivity. The thermal resistance of the wiring layer, which has a relatively large proportion, is small, however, the thermal resistance of the via layer, which has a very small proportion, is large. Since the thermal resistance of the via layer is the parallel thermal resistance of the insulating material and the via material, if the thermal resistance of the via material becomes low, the temperature rise of the Cu wiring can be suppressed.

The comparison of the temperature rise of the top layer wiring in the case of Cu via and the case of CNT via for the 14-layer Cu wiring with the substrate temperature fixed at 105 ºC was studied[48]. By changing the Cu via to the CNT via, the wiring temperature of the uppermost layer is suppressed from 661 ºC to 165 ºC (Fig. 1.9). The first demonstration of GHz digital signals transmission between transistors using CNT interconnects was shown in 2008[49].

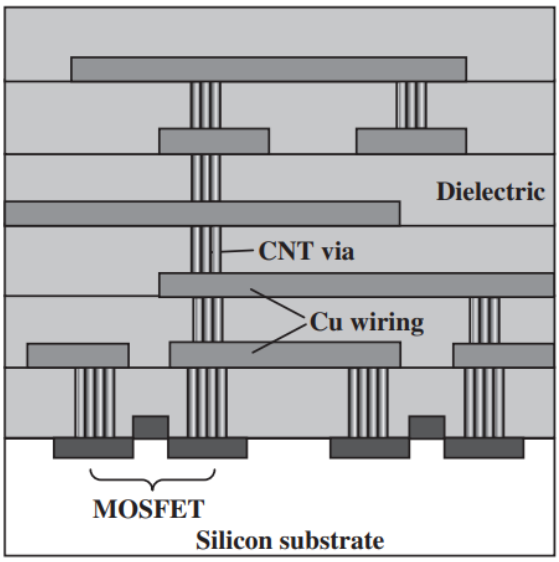


Fig. 1.8 Schematic of CNT via in the LSI interconnect[37]

Fig. 1.9 Interconnect temperature [K] using different proportion of CNT via layer[48]

【*Three-dimensional integrated circuit (3D-IC)*】

The best way to reduce interconnect delay and power consumption without compromising performance is to reduce the interconnect length. However, transistors are placed on a single plane in most modern semiconductor processes where global wiring across the entire chip inevitably become long. To shorten the interconnect length, 3D-IC has been proposed. Since the 3D-IC is a 3D structure rather than a planar IC, small footprint chip can be achieved. The 3DIC is a single chip, which is also a feature differentiating from the stacked die with perimeter connections using silicon photonics, and all layers are connected via on-chip interconnect rather than inter chip connection, such as wire bonding. Through-silicon-vias (TSVs)[50]-[53] is one technology allows high density of electrical connections passing through the silicon substrate between different IC layers. Figure 1.10 shows the TSV structure in fabricated DRAM of Samsung. High speed and low power can be obtained because of its smaller parasitic capacitance and resistance compared with that in global wiring in planar structure. However, the manufacturing is unstable.

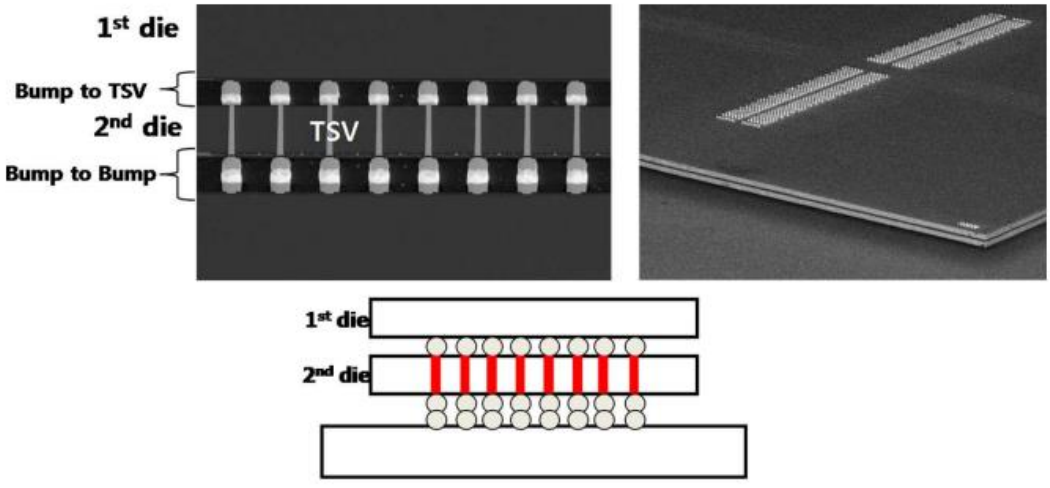


Fig. 1.10 Photograph of 2-stacked DRAM[54]

In addition to use direct connection in 3D-IC, wireless communication, such as capacitive[55]-[56] or inductive[57]-[59] coupling. Figure 1.11 shows the concept view of three types of physical connection in 3D-IC. The main idea in wireless communication is to replace on-chip wires with integrated on-chip antennas communicating via electromagnetic waves. Both magnetic flux and electric field are media that transmit signals vertically. The transceiver can be fabricated using a 2D process in capacitively/inductively coupled link, which is the advantage different from TSV. High data rates of 11 Gbps and low power consumption of 0.14 pJ/bit can be achieved in the existing capacitive and inductive coupled designs[60], both of which are comparable to TSV. The communication distance in capacitive coupling is much shorter than that in inductive coupling, which limits it to be used only in face-to-face stacking. However, much larger area is needed in capacitively/inductively coupled link than TSV ranging from hundreds to tens of thousands of square microns[60], which leaves a question towards high density 3D integration.

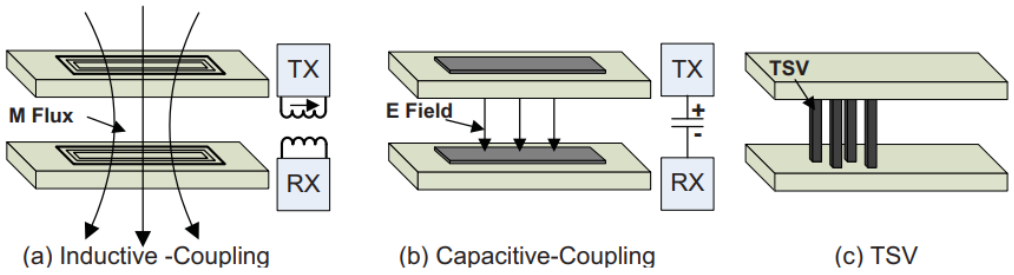


Fig. 1.11 A concept view of inductive coupling, capacitive coupling and TSV[60].

【***On-chip differential transmission line***】

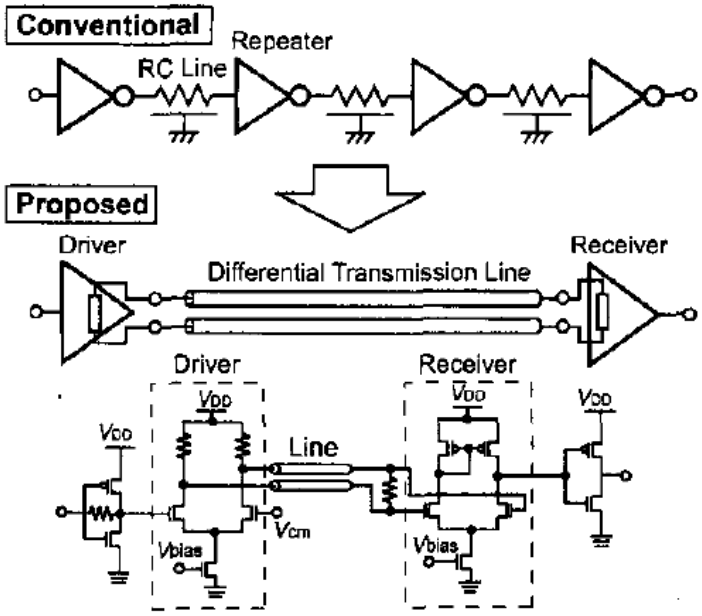


Fig. 1.12 Conventional global interconnect and proposed on-chip differential transmission line interconnect[61].

When the frequency of electrical wiring becomes high and the signal wavelength cannot be ignored with respect to the line length, it is necessary to think of the signal as an electromagnetic wave transmitting in a transmission line. Assuming that the wavelength with respect to the basic frequency of the signal is λ, if the line length L is longer than $\lambda/40$, it is considered as a transmission line[62]. A transmission line (TL) interconnect has been proposed to reduce global interconnect delay[63]. It is reported that TLIs have better power efficiencies than conventional on-chip lines as a line length and a signal frequency increase[64]. However, single ended transmission lines normally require a large ground plane, such large dimension is not suitable for on-chip wiring. To break this barrier, differential transmission line (DTL) consists of a pair of transmission line (TL) has been proposed (Fig. 1.12). The DTL have much better design flexibility and it can be driven by low-voltage differential signaling (LVDS) since the strong tolerance of crosstalk. A 10 Gbit/s transmission through 5 mm long DTL was demonstrated with energy consumption per bit of 270 fJ/bit[63].

1.3.3 On-chip optical interconnect

It is claimed that optical interconnects will be suitable replacements for global on-chip interconnects, where they can be advantageous because of their inherent low propagation delay, low crosstalk, and a near constant power profile over long distances. Optical interconnects offer many advantages[65]:

i. Enormous intrinsic data bandwidths can be support in the order of several Gbps using only simple on-off modulation schemes.

ii. Being immune to electrical interference due to crosstalk, parasitic capacitances and inductance.

iii. The power dissipation is independent of transmission distance at the chip level.

iv. Routing and placement are simplified since it is possible to physically intersect light beams with minimal crosstalk. After an optical path is established, data can be transmitted end to end without the need for repeating or buffering, which can lead to significant power saving.

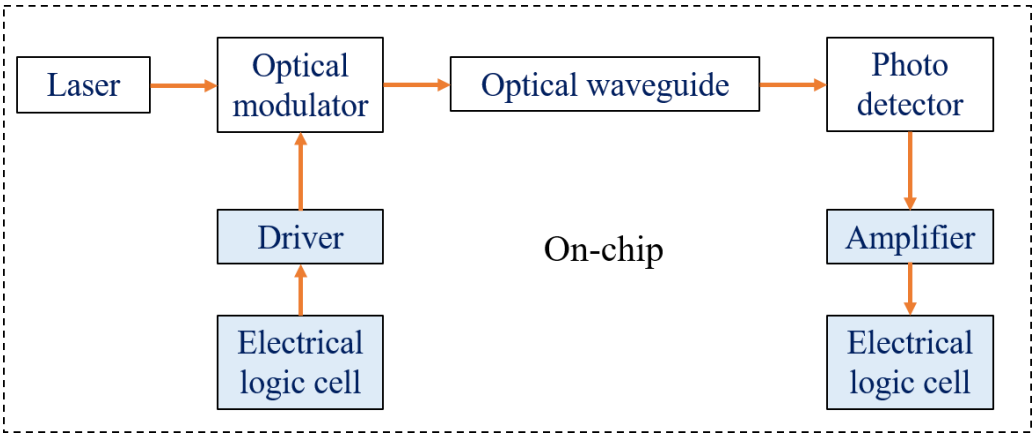


Fig. 1.13 Block diagram of the optical interconnects system

Figure 1.13 shows a block diagram of an on-chip optical interconnects system. All components are integrated on a chip. Two modulation methods are used in the optical link. Direct modulation that modulation electric signals are input into lase. External modulation that using external modulator such as Mach-Zehnder modulator[66] and electro-absorption (EA) modulator[67]. The data transmission performance over 10 Gbps or higher is easier to be improved using indirect modulation. Mach-Zehnder

interferometer-based silicon modulators have higher extinction ratio, bandwidth and temperature stability but a large power consumption and greater silicon footprint[68]. While EA modulators have advantages in terms of compactness and lower power consumption.

A comparison was made by K. C. Saraswat et al. in Stanford University[69] between electrical and optical wiring. Figure 1.14 (a) shows the comparison of latency for different wiring schemes as a function of length. Figure 1.14 (b) shows the energy consumption for different wiring schemes as a function of length. It is assumed that the single-wall CNT bundle with packing density of 33% and optical interconnects consists of III-V MQWs modulators, silicon waveguides, Ge detector and an off-chip laser. In terms of latency, the optical interconnection retains its advantage, and the increment is very slow. In the case of energy cost, optical interconnection is nearly approximated to a constant while the energy consumption of electrical interconnection is proportional to the wiring length. Figure 1.15 shows the latency and the energy consumption versus wire bandwidth for both wire circuit schemes for the 22 nm technology and the length is assumed as 10 mm. It reveals that the optics still shows the lowest delay and energy cost for all bandwidth range.

Generally, light is difficult to confine in a narrow space by nature. Optical devices are overwhelmingly larger in size than electronic devices and have been difficult to integrate. In addition, it is not enough to simply make it smaller, and the energy consumption of

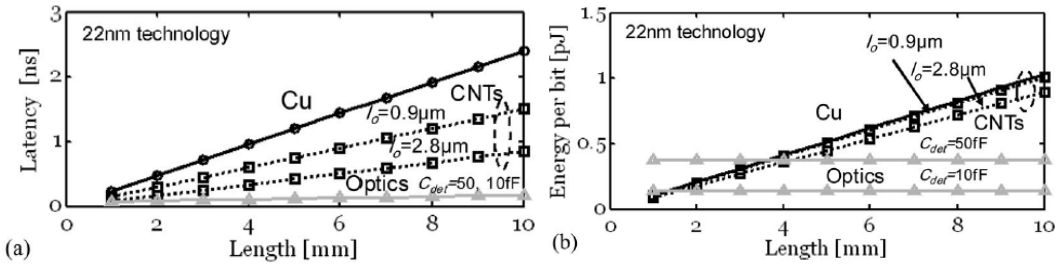


Fig. 1.14 (a) Comparison of latency;(b) Comparison of energy consumption per bit[69]

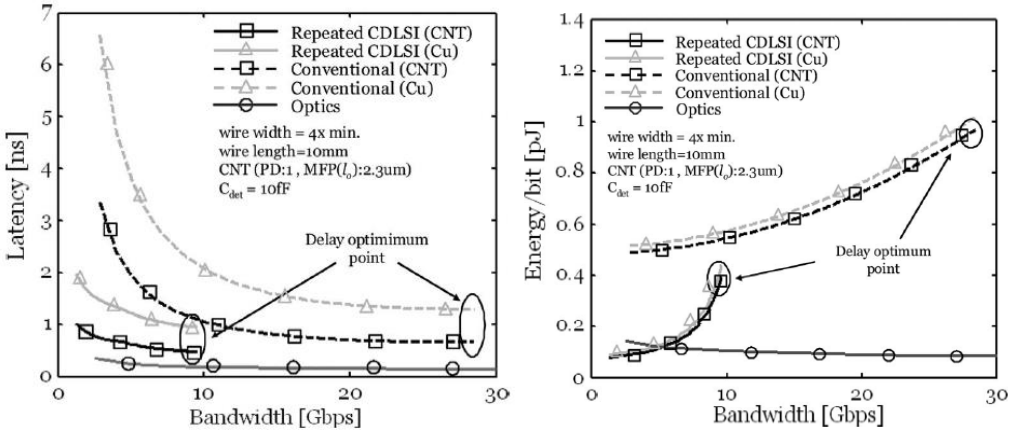


Fig. 1.15 Comparison of latency and energy consumption per bit versus bandwidth[69]

each device must be low, but the energy consumption of current optical devices is about 1 to 100 pJ / bit. No matter how low the transfer cost is, it is meaningless if the optical device also consumes pJ. In the application of global wiring using optical interconnect, Prof. D. A. B Miller indicated that optical interconnects on chip need a total system energies consumption of ~ 100 fJ/bit to be competitive on energy grounds, and therefore, ~10 fJ/bit energy cost was needed for optical output devices[70].

1.4 Semiconductor devices in optical interconnect

In order to realize the on-chip optical interconnect, a low power consumption semiconductor laser, low loss waveguide, and high responsivity photodiode are needed to form a fundamental optical link. This section, the performances and characteristics of these optical devices and optical links will be introduced.

Low power consumption lasers

【*Vertical cavity surface emitting lasers (VCSELs)*】

VCSELs are semiconductor lasers that emit light perpendicular to the surface of a substrate and are characterized by the ability to integrate a large number of components two-dimensionally on the same substrate. The first operation of VCSEL using current injection was realized in 1979[71]. Here, a GaInAsP / InP system with a wavelength of 1.3 μm was used, and the threshold current was 700 mA in pulse current operation at a low temperature of 77 K. In 1984, the first room-temperature (RT) pulse operation of VCSEL was achieved by using GaAlAs/GaAs system[72], and the threshold current was as low as 510 mA. After that, for lowering the threshold current of VCSEL, high reflectivity of distributed Bragg reflector (DBR) and small cavity narrow current structure were proposed. The first RT-continuous wave (RT-CW) operation of VCSEL was obtained in 1988[73]. Small cavity length of ~ 5.5 μm was used, and the threshold current ranged from 28 to 40 mA was obtained. J. L. Jewell et at. achieved 1.3 mA low threshold current with 958 nm output wavelength in 1989[74]. The sub-mA low threshold current of 0.65 mA was achieved in 1993 using GaAlAs/GaAs system[75].

As the promising device with low cost and low power consumption light source for optical interconnect in the data center and supercomputers, VCSELs received much attention in recent years. The high-power conversion efficiency of 62% was achieved in 2008[76] by K. Takaki, (Furukawa electric). Low energy cost of 81 fJ/bit was demonstrated in 2011[77] and 56 fJ/bit in 2012[78]. Further, the 50 fJ/bit for 40 Gbps non-return-to-zero (NRZ) and 48 fJ/bit for 60 Gbps Pulse Amplitude Modulation 4 (PAM4) were recorded

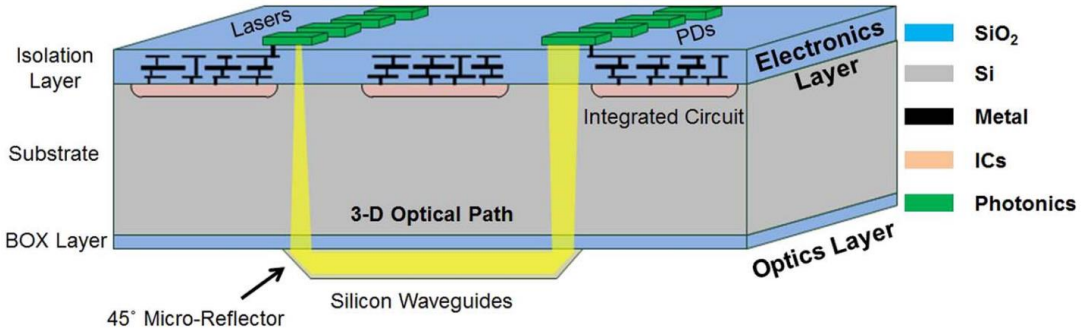


Fig. 1.16 Concept of chip level optical interconnect using 45 º mirror and 3D optical path[80].

in 2021[79]. However, another mechanical structure of 45 º mirror (Fig. 1.16) was necessary for an in-plane optical integrated circuit[80]-[82], which is the problem should be solved for on-chip optical interconnect.

【*Photonic crystal laser*】

Although research on photonic crystals has been in progress since 1887, it was not until 1987, a hundred years later, that the term "photonic crystal" was first used in two papers by Eli Yablonovitch[83] and Sajeev John[84], respectively, published in Physical Review Letters. Photonic crystals are photonic band gap materials. From the perspective of material structure, photonic crystals are a class of artificially designed and fabricated crystals with periodic dielectric structures on the optical scale. Similar to the modulation of the electronic wave function by the semiconductor lattice, the photonic bandgap material can modulate the electromagnetic wave with the corresponding wavelength. When the electromagnetic wave propagates in the photonic bandgap material, it is modulated due to Bragg scattering, and the energy of the electromagnetic wave forms energy band. A band gap appears between the energy bands, which is called the photonic band gap. Photons with energies within the photonic band gap cannot enter the crystal. The motion of photons can be controlled by designing and fabricating photonic crystals and device.

The Distributed Feedback (DFB) and DBR structure are one-dimensional type photonic crustal. An introduction of defect region into periodic structure can construct a wavelength scale cavity, in which the light can be strongly confined. Based on this idea, the first two-dimensional photonic crystal laser (PhCs) by optical pumping was reported[85] in 1999. The electrical pumped PhCs at RT-pulse[86]-[88] and RT-CW[89] conditions were demonstrated later. In these typical photonic crystal cavity, thin layer including gain material distributed by air hole was used for optical confinement. However, high thermal resistance caused by air hole and low pumping efficiency by no carrier confinement limited the characteristics of those PhCs. A buried hetero (BH) structure (Fig. 1.17) based PhCs by optical pumping was demonstrated, that achieved 1.3 μW low

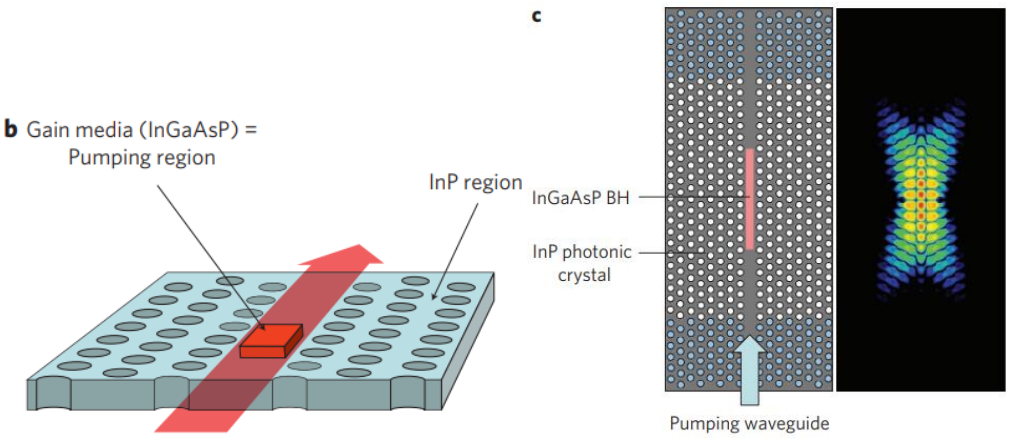


Fig. 1.17 Schematic of PhCs laser with buried GaInAsP active region[90]

threshold input power and 13 fJ/bit low power consumption at modulated output power of 5 GHz[90]. A 20 Gbps NRZ modulation with the energy coat of 8.76 fj/bit was achieved later[91]. Subsequently, current injection type PhCs were obtained[92]-[93]. High temperature operation was demonstrated up to 95˚ under CW condition[94], and a 14 fJ/bit at 12.5 Gbps was shown. The lowest threshold current recorded at 4.8 μA and the energy cost of 4.4 fJ/bit has been reported[95]. For on-chip optical interconnect, the PhCs or λ-Scale Embedded Active Region Photonic Crystal (LEAP) laser was fabricated on Si substrate (Fig. 1.18) by O_2 plasma assisted wafer bonding[96]-[97]. However, low output power is still a problem that limited its application in on-chip wiring.

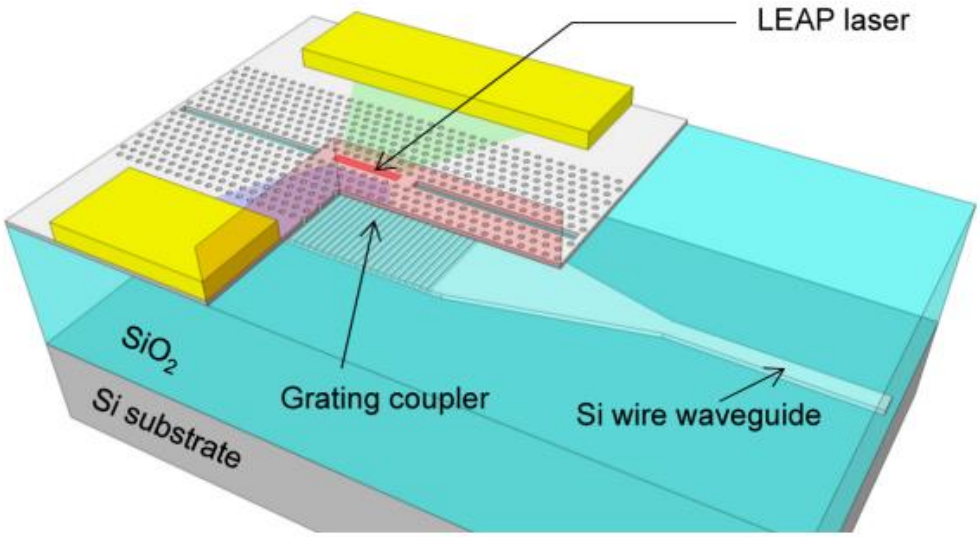


Fig. 1.18 Schematic of LEAP laser on Si substrate by O_2 plasma assisted wafer bonding[97]

Waveguides in optical interconnect

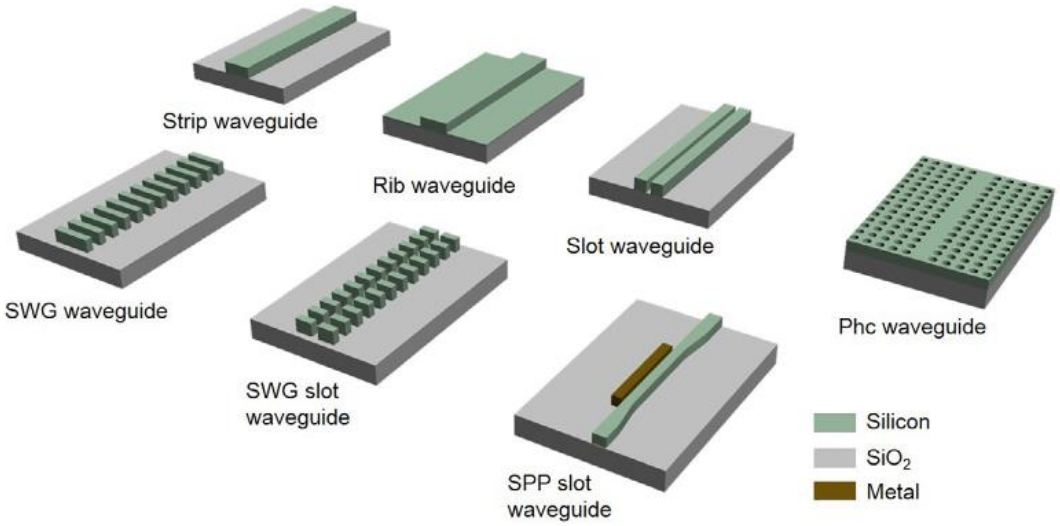


Fig.1.19 Various types of Si waveguide in Si photonics[98]

There are various types of waveguides used in on-chip optical interconnect. Figure 1.19 shows them using Si. Stripe waveguide is the most commonly used structure in Si photonics. High refractive index difference between Si (n = 3.5) and SiO_2 (n =1.4) offers Si stripe waveguide a tight bending radius. So, in compact optical routing, such waveguide is typically used. The typical propagation loss is 1 ~ 2 dB/cm. The rib waveguide was widely used in modulators that allows the connection of electrode more easily[99]. The first theoretical and experimental demonstration of slot waveguide using Si/SiO_2 were reported in 2004[100]-[101], showing the light can be confined in a low refractive index material region. Stronger nonlinearities can be obtained inserting nonlinear material in the slot region[98]. This surface enhanced super mode confined in slot region suffers no scattering[102]. The photonic crystal waveguide discussed here is usually 2-D photonic crystal. High optical confinement exists in photonic waveguide, and sharp bends for 90 º bend with zero radius was achieved[103]. However, it suffers high scattering loss in the vertical direction[104]. The subwavelength grating (SWG) waveguide offers a z-axis direction guided mode, such as grating coupler, or a refractive index modulation effect, which can be sued in DFB/DBR structure. The SWG waveguide which consists of a slot formed a SWGS waveguide. The surface plasmon polariton (SPP) slot waveguide is a hybrid plasmonic waveguide. The light confinement capacity of plasmonic waveguide is not limited by diffraction[105], thus, tighter light confinement can be obtained.

Recently, the silicon oxynitride (SiON) or silicon nitride (SiN) is attracting attention in the photonic integrated circuits. The lowest loss has recorded as 0.1 dB/m using a high-aspect-ratio Si_3N_4 core[106]-[108]. The InP[109]-[110] or GaInAsP[111] III-V waveguide were also studied for a InP based platform photonic integrate circuits, or on Si substrate through wafer bonding technology. These types of waveguides were suitable to the back-end process on Si-LSI integration using InP-based optical interconnect.

Photodetector in optical interconnect

In order to integrate in optical circuits, the waveguide-type photodetector was usually used. The germanium-on-Si p-i-n photodiode has the competitiveness because of its high absorption coefficient in the near-infrared range with compactness. The development of direct growth of Ge on Si reduced the cost and created a new possibility of Ge in optical interconnect. An ultra-compact Ge waveguide photodiode on Si-photonics was reported[112]. The small footprint of 1.3 × 4 μm^2 results in a low intrinsic capacitance of 1.2 fF. A responsivity of 0.8 A/W, and 3-dB bandwidth of 45 GHz was obtained. High speed photodetector for 3-dB bandwidth over 100 GHz using InP-based was reported[113]-[115]. Recently, an ultra-fast Si-waveguide coupled Ge p-i-n photodiode on SOI (Fig. 1.20) based on epitaxially growth with a 3-dB bandwidth of 265 GHz at a photocurrent of 1.0 mA at -2 V reverse bias voltage has been demonstrated[116].

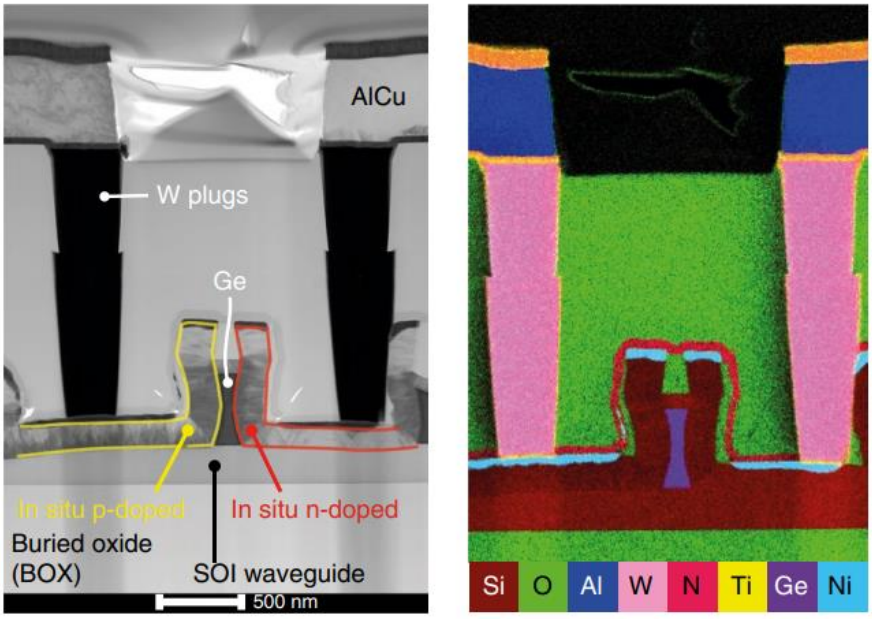


Fig. 1.20 STEM and EDX image of Ge on SOI substrate[116]

1.5 Wafer bonding technology

With the continuous improvement of the requirements for integrated circuits, there are more and more applications of other semiconductor materials, such as germanium, gallium arsenide, silicon carbide, etc. Bonding can combine two or more materials into one, which can broaden the application range of devices. The devices used in optical interconnect were introduced in the last section. The integration of between III-V semiconductor to Si-LSI is a key technology for optical wiring. Recently, the layer transfer by wafer bonding was wieldy used in III-V/Si hybrid integration, which can make up for disadvantage that Si cannot emit light as an indirect bandgap material. In this section, various wafer bonding methods will be introduced from high temperature to room temperature bonding.

High temperature bonding

【*Si fusion bonding*】

The direct wafer bonding means two mirror polished, clean and flat wafers were boned to each other without adhesive. Since the birth of the first integrated circuits in 1985, silicon technology has dominated the production of integrated circuits, and silicon wafers are the basic material for LSI or silicon photonics. The Si direct bonding was studied at Toshiba[117] and IBM[118] in 1985. Two mirror-polished Si wafer were brough into contact at room temperature, then annealed at high temperature (800 ~ 1000 °C) for enhancing bonding strength. After cleaning the surface of wafer, the bonding can be divided into hydrophilic and hydrophobic bonding based on the surface condition. Van der Waals

Hydrophilic: $$Si\text{-}OH + HO\text{-}Si \rightarrow Si\text{-}O\text{-}Si + H_2O \quad (1.1)$$

Hydrophobic: $$Si\text{-}H + H\text{-}Si \rightarrow Si\text{-}Si + H_2 \quad (1.2)$$

forces almost exist on all the substance[119], and it is inversely proportional to the cube of the distance. Therefore, any surfaces could be bonded to each other while the surfaces are to get close enough for van der Waals force. The bonding mechanism model was proposed

by Q. Tong, and U. M. Gosele[119]. For hydrophilic bonding, RCA solution (mixed NH_4OH, H_2O_2 and H_2O) or piranha solution (mixed H_2SO_4, H_2O_2 and H_2O) is mainly used to treat surface to form a high density of hydroxyl (-OH) surface, and wafer molecules in the atmospheric environment are easily adsorbed on this hydrophilic surface. The weaker intermolecular forces (van der Waals forces and hydrogen bonds) between the interfaces during high-temperature annealing are transformed into stronger siloxane Si-O-Si covalent bonds, resulting in a strong bonding interface. For hydrophobic bonding, hydrofluoric acid (HF) is generally used to remove the natural oxide film on the surface of the silicon wafer. The surface of the silicon wafer is covered with silicon-hydrogen bonds (Si-H) with hydrophobic properties. The treated silicon wafer is first bonded at room temperature. The subsequent annealing process follows the reaction formula Eq. (1.2), and Si-Si covalent bonds are formed at the interface. The bonding energy of hydrophobic and hydrophilic Si-Si bonding was shown in Fig. 1.21. Hydrophobic bonding can only meet the mechanical strength required for subsequent processing of bonded wafers after a high annealing temperature. When the annealing temperature is

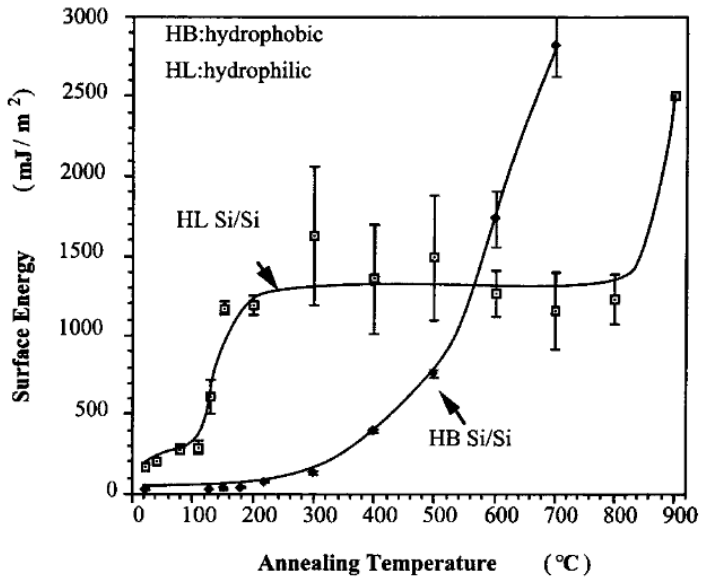


Fig. 1.21 Bonding energy versus annealing temperature in Si-Si hydrophobic and hydrophilic bonding[119].

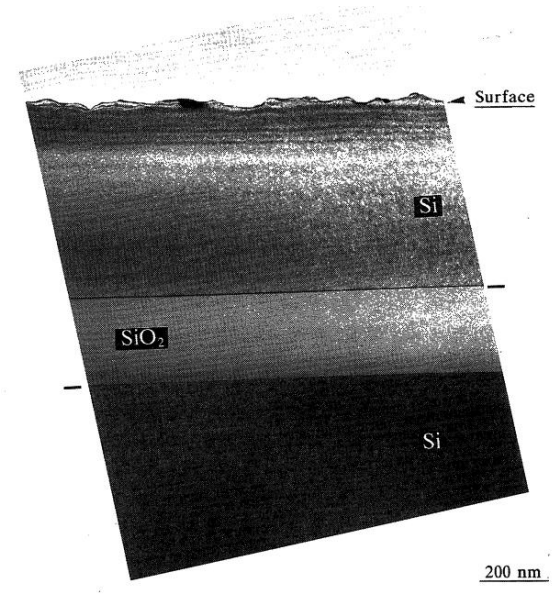


Fig. 1.22 Cross sectional image of fabricated SOI wafer by hydrogen implantation and hydrophilic wafer bonding[120]

lower than 600 ºC, the bonding energy obtained by the hydrophilic method is higher than that obtained by the hydrophobic bonding method, and after 200 ºC annealing, the bonding anergy does not change a lot. In this stage, the water molecules between wafers are almost removed, and the bonding energy is limited by surface roughness. 2 J/m^2 high bonding energy needs the annealing temperature higher than 700 ºC, where the thermal oxide starts to fill the gap by viscous flow.

Hydrophilic wafer bonding has commercially used in silicon-on-insulator (SOI) wafer fabrication. Figure 1.22 shows a cross sectional image of fabricated SOI wafer by hydrogen implantation for smart-cut process and hydrophilic wafer bonding. A Si wafer covered with a thermally grown SiO_2 layer was treated by hydrogen implantation at first. Then, two wafers were bonded at room temperature after surface cleaning. Two steps annealing process was followed. During the first step, 400 ~ 600 ºC annealing was carried out for splitting, the crack surface is shown in the top of Fig. 1.22. In the second step,

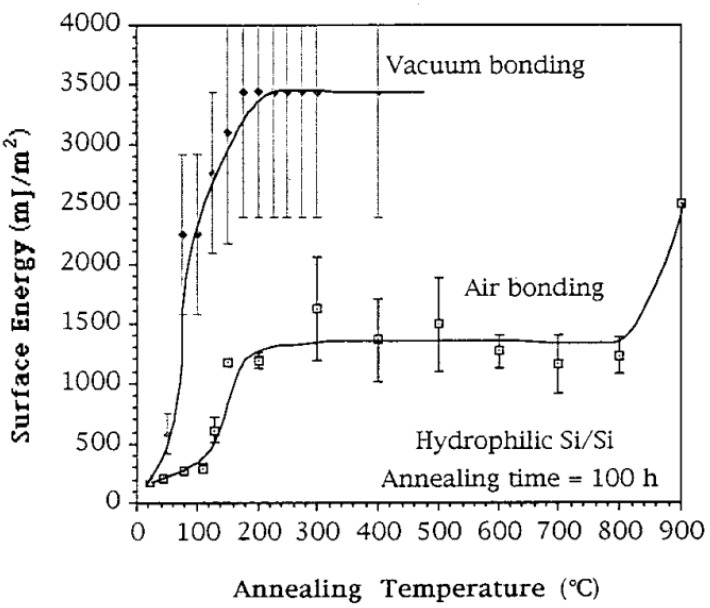


Fig. 1.23 Comparison of bonding energy in air bonding and vacuum bonding of Si-Si hydrophilic bonding[121]

1100 ºC high annealing temperature was for increasing the bonding strength between SiO_2 and Si.

The bonding condition introduced above is the atmospheric bonding. Low vacuum bonding can easily increase bonding energy[121]. Figure 1.23 shows the comparison of bonding energy in air bonding and vacuum bonding of Si-Si hydrophilic bonding. The annealing time of 100 hours was used. From this results, low temperature bonding < 200 ºC can be achieved with a high bonding energy, which is important for photonic integration on Si-LSI, because the high temperature annealing process can induce thermal stress in internal components and worse diffusion of doping elements.

Low temperature bonding

【*plasma activated bonding (PAB)*】

The annealing temperature can be reduced, and bonding energy can be increased at the same time by plasma treatment before bonding, which was experimentally proved by many studies. The mechanism of plasma activated bonding was discussed from multiple perspectives. Wieldy accepted changes after plasma treatment are listed below:

(1) Surface cleaning by removing containment. After plasma treatment, this cleaning effect produced more dangling bond to enhance bonding strength.

(2) Higher hydrophilicity. After plasma treatment, even in room temperature, the bonding energy is higher than non-plasma activated wafer (Fig. 1.24), which indicates that more silanol groups (Si-OH) were produced and the bonding strength determined by siloxane bond (Si-O-Si) that through the reaction of Eq. (1.2).

(3) The diffusion rate of water and gas is enhanced at the interface after plasma treatment, which accelerates the reaction of Eq. (1.2) and increases hydrogen bond at room temperature.

In the model proposed by C. Tan et al.[123], viscous flow should have occurred at low

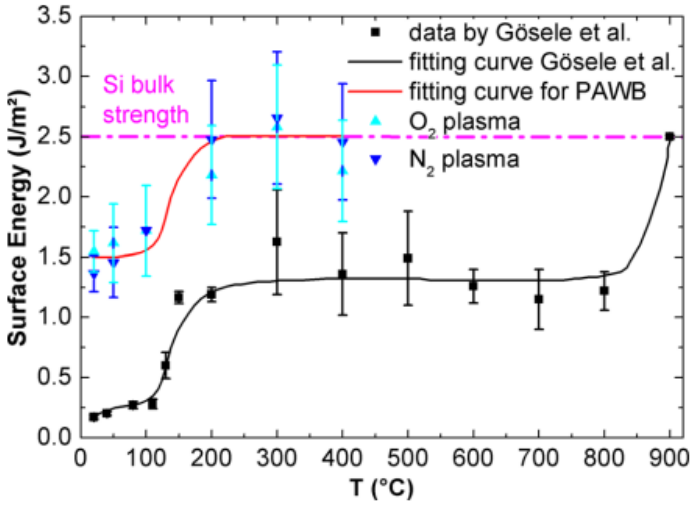


Fig. 1.24 Enhanced bonding energy by plasma activated bonding at low temperature[122].

temperature, because after low temperature annealing ~ 200 °C, the same bonding energy as 800 °C annealing in the conventional air hydrophilic bonding. However, T. Plach et al. have another idea[122]. They think that since the bonding energy enhanced again over 800 °C in conventional hydrophilic bonding was due to closure of nanogap in bonding interface, the same bonding energy was obtained in low temperature annealing indicates the nanogap closed at this low temperature, and that could not be viscous flow but oxide growth through the reaction of Eq. (1.3). Ventosa et al.[124] have found the native oxide growth at the interface of Si/SiO_2 from 150 °C. The oxide layer would be grown near the nanogap and reduce the total energy of the system.

$$Si + 2H_2O \rightarrow SiO_2 + H_2 \tag{1.3}$$

The plasma activated bonding usually generates bubble at the bonding surface, which was not only because of the contamination but also due to the unremoved water and reaction of Eq. (1.3). An appropriate plasma treatment and bonding condition can alleviate this phenomenon[124], and a trench pattern was also proved a way to achieve a bubble-free bonding[125]. In recent research, sequential plasma activation method (two or three step different plasma treatment) was studied for low temperature bonding of Si and glass material. A room temperature bonding of Si-Si was obtained by O_2 plasma and N radical activation without annealing[126]-[129]. The quartz glass bonding strength was strengthened by the activated sequence of O_2 plasma, N_2 plasma and N radical at low temperature annealing of 200 °C[130]-[131]. The same method was also used in fused silica, sapphire, and aluminosilicate glass bonding[132].

Room temperature bonding

【*Surface activated bonding (SAB)*】

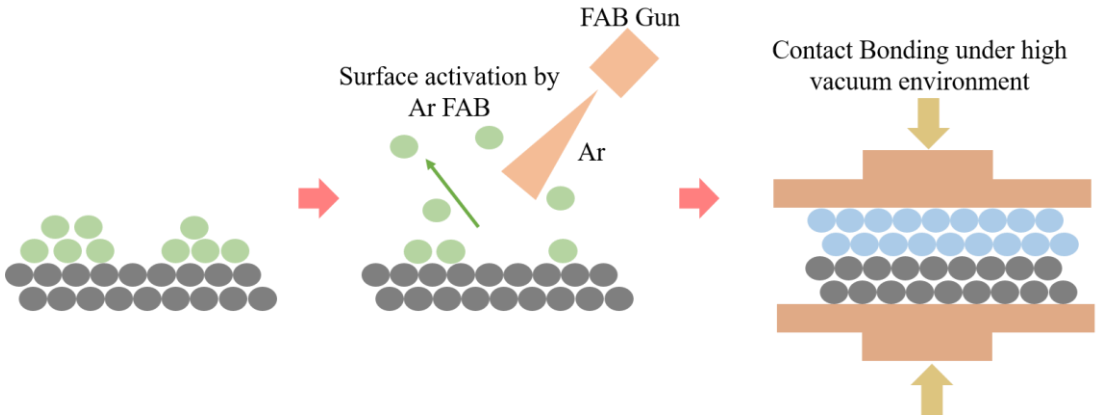


Fig. 1.25 Schematic of surface activated bonding by Ar fast atom beam.

Adhesion occurs on bare metal with clean and smooth surfaces in ultra-high vacuum environments, and the same phenomenon occurs in a mirror polished glass or wafer, which is the case of "cold welding". In 1965, H. I. Smith and M. S. Gussenhoven have studied on the bonding between quartz and quartz in ultra-high vacuum environment[133], but the bonding between the interfaces mainly relies on van der Waals force, so the obtained bonding strength is weak. In 1967, D. Haneman et al. reported the vacuum bonding of germanium, and realized the covalent bond between the interface atoms[134]. The realization of vacuum bonding mainly relies on the extremely high activity of atomically clean surfaces, and the bonding easily occurs at low temperature or even room temperature. The development of surface-activated bonding methods mainly began in the 1990s[135], and the research group of Professor T. Suga of the University of Tokyo, Japan, took the lead in the research on room temperature bonding. The basic principle of surface activated bonding (SAB) is to use argon fast atom beam (FAB) or ions to bombard the wafer surface in a high vacuum environment ($<10^{-5}$ Pa) to remove the surface oxide film and other contaminants (Fig. 1.25). Then a certain pressure is applied to make the two surfaces whose oxide films have been removed are brought into contact in a high vacuum environment. Good bond strength and quality can be achieved at room temperature (~

25 °C).

Many materials bonded by SAB such as Al-Al[136], Al-ceramic[137], Al- Si_3N_4[138], Al-Si[139], Cu-Cu[140], Si-Si[135], Si-GaAs[141], Si-$LiNbO_3$[142] have been realized. Since the surface activity after fast atom beam bombardment is extremely high, if this process is carried out in a non-ideal state, the problem of secondary oxidation or secondary pollution is very likely to occur. Therefore, the process of bombardment and bonding is often carried out in ultra-high vacuum. Although the surface activated bond method has been widely concerned by the semiconductor industry since its birth, there are still two problems that limit the application of this method:

1. This method is not suitable for oxide material (such as silicon dioxide, quartz and glass). The bonding strength at room temperature is very low[143], and an annealing process is still required.
2. This method requires a high vacuum system, and the equipment is complex and expensive.

【***Extended surface activated bonding***】

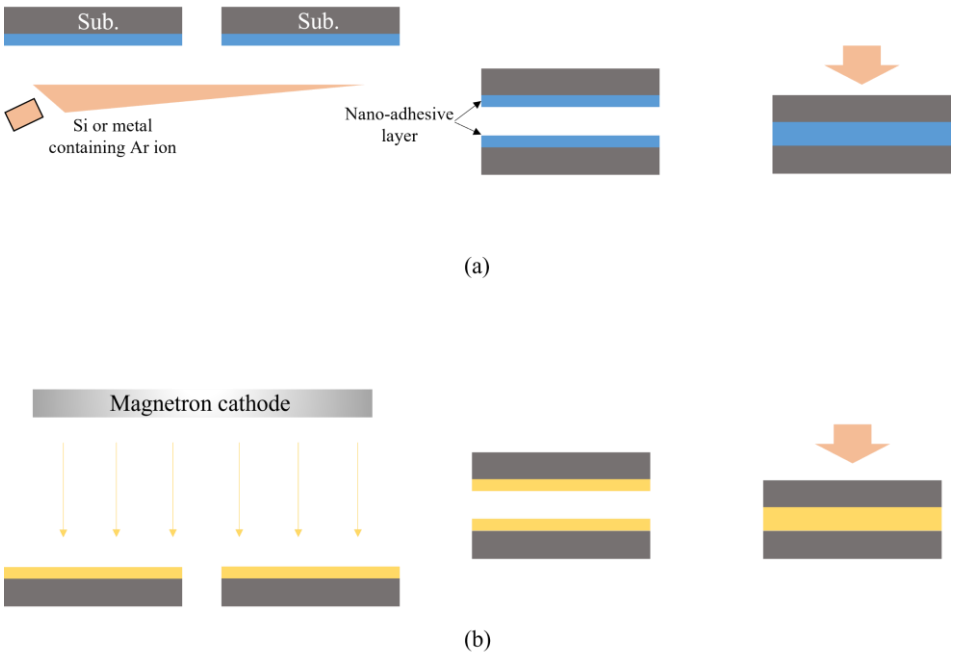


Fig. 1.26 (a) Extended SAB, nanofilm was formed by irradiation of FAB. (b) ADB, nano metal film was formed in high vacuum then bond directly.

For glass and carbon materials, the life of the active dangled bond that should be generated by ion impact is expected to be extremely short due to its highly flexible structure, and in fact, the standard surface activation cannot bond completely. For these materials that are difficult to bond with standard SAB, a thin intermediate layer (nano-adhesion layer), such as active metal, Si, or an oxide film that can be bonded at room temperature is proposed, which is called extended surface activated bonding[144]. The process sequence is shown in Fig. 1.26 (a). Nanofilms can be formed by sputter in high vacuum. The thickness of films is less the several nm, and it does not have to be a continuous film but may be distributed in an island shape. When metal thin films are formed in ultra-high vacuum, the surface remains active independent of ion impact. Contact of the two surfaces immediately induces diffusion and grain growth, resulting in bonding. This method, proposed by Professor T. Shimazu of Tohoku University in Japan, is called atomic diffusion bonding (ADB)[145] (Fig. 1.26 (b)) and is currently being applied and put into practical use in photonic devices.

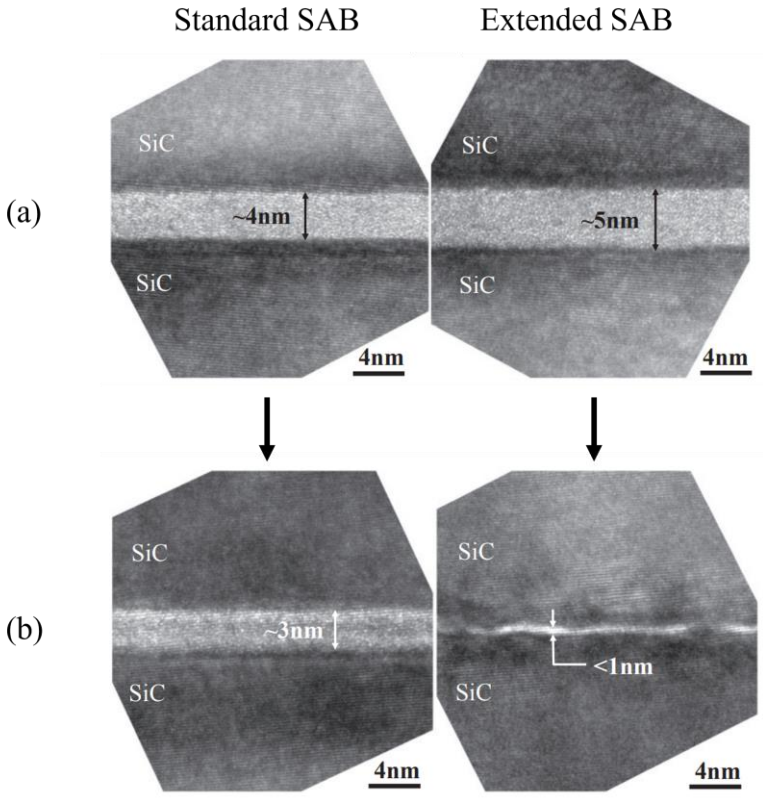


Fig. 1.27 TEM images of SiC-SiC bonding using standard SAB and extended SAB[146]

SiC is valued as a high thermal conductivity material. A comparison of SiC-SiC direct bonding using standard SAB and extended SAB using Si nano-adhesion layer[146]. A Si-containing Ar ion source was prepared in the experiment. Figure 1.27 (a) shows the Transmission Electron Microscope (TEM) images of two type boned interface. Both have a SiC amorphous layer in the bonding interface, which was due to the Ar ion irradiation. The 1 nm thicker in the extended SAB may because the Si in Si-containing Ae ion source sputtered to SiC. The bonding energy and tensile bonding strength in extended SAB was both 30% higher than that in standard SAB. Figure 1.27 (b) shows the TEM images after 1000 °C annealing for 3 min. The reduced thickness in extended SAB was because of the crystalline. The bonding strength is enhanced after annealing.

SiC-Si was also studied using extended SAB[147]. In this study, a Si target was used as the sputter source, and the Ar-FAB was used to irradiation. The process was shown in Fig. 1.28. After cleaning the surface of SiC wafer, a thin Si nano layer was sputtered on SiC by Ar-FAB irradiation. Then the SiC was irradiated again, hence the sputtered Si layer was etched a little for cleaning. Finally, two wafers were brought into contact for bonding. 15 nm Si layer was observed in the interface. The averaged bonding strength by tensile test after 1000 °C annealing can reach to 18 ~ 19 MPa.

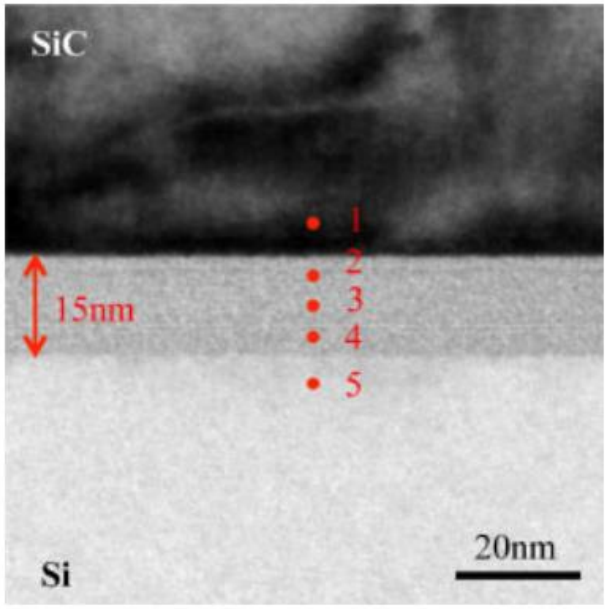


Fig. 1.28 TEM images of bonded SiC-Si interface[147].

All of the above SABs are characterized by bonding at room temperature. The necessary condition for that was the process of surface activation. However, on the other hand, there are many applications that can be fully satisfied if the temperature is lower than before, even if it is not at room temperature. In that case, the low temperature bonding that discussed in the last section is appropriate. Table 1.2 gives the comparison of several direct bonding technologies discussed in this chapter.

Table 1.2 Comparison of several direct bonding technologies

Bonding method	Conventional fusion bonding	PAB	Standard SAB	Extended SAB
Mechanism	-OH	-OH	Covalent	Nanofilm
Bonding ionic materials	Suitable	Suitable	Poor	Good
Bonding metallic materials	Poor	Poor	Good	Good
Bonding strength at RT	Poor	High	Very high	Very high
Void formation after annealing	Frequent	Frequent	No	No
Ambient atmosphere in process	Atmospheric	atmospheric	High vacuum	High vacuum
Cost of bonding equipment	Low	Low	High	High

Adhesive bonding

【*Benzocyclobutene(BCB) bonding*】

The adhesive bonding is more tolerant to surface topography and particle contamination compared to direct bonding. Many choices for intermediate layer such as SU-8, spin-on glass (SOP), polyamide and BCB are used. BCB is a good choice for hybrid bonding because it has a low dielectric constant, low curing temperature and high degree of planarization. Usually, it was used in packaging and electrical interconnect as an insulation layer. The III-V/Si hybrid bonding using BCB was also well studied for photonics integration[148]. The process of BCB bonding includes two times of curing. Figure 1.29 shows the BCB curing as a function of temperature and time. After spin coating, the BCB will suffer the first cure (pre-cure) for semi-gelled, which is the most important step in BCB bonding process. It is better to keep a 50 ~ 70 % BCB transfer to gel at the pre-cure step. Low ratio may introduce bubble in the bonding, and high ratio may prevent the bonding due to a high solid proportion. Then after the bond of wafer in room temperature, a post hard cure was needed to transfer BCB to solid. From Fig. 1.29, a low temperature annealing (~ 250 °C) can be achieved when both consider temperature

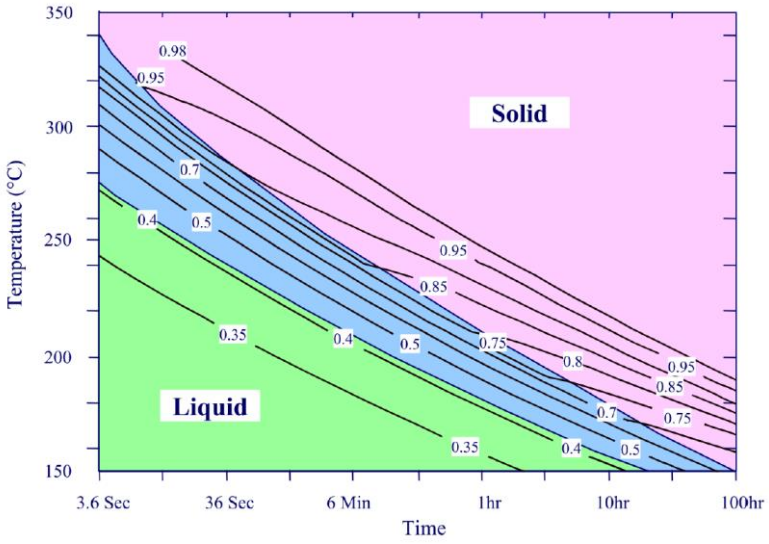


Fig. 1.29 BCB curing as a function of temperature and time[149].

and process time. Our group started the BCB bonding since 2000 and the detailed bonding process will be discussed in chapter 3. Table 1.2 shows a comparison of adhesive and direct bonding in device integration. The advantage of adhesive bonding using BCB is the high surface tolerance. In the real situation, the bonding interface of two wafers are not always flat, hence, the BCB bonding was suitable to variety of situations. In an empirical experiment, the surface roughness should lower than 1.0 nm in direct bonding process. The chemical mechanical polishing before bonding may be needed after several process before bonding. However, the thermal conductivity of BCB is extremely small that limited the thermal diffusion.

Table 1.3 Comparison of adhesive and direct bonding in device integration

	Adhesive bonding (BCB)	Direct bonding
Full wafer scale	✓	✓
Surface tolerance	high	Surface roughness lower than 1 nm or chemical mechanical polishing is needed
Bonding materials	Most of materials	Limited by bonding method
Thermal characteristic	Poor (low thermal conductivity of BCB)	high
Bonding strength	Lower	Higher
Voids at surface	less	Depends on bonding method

1.6 Photonic integrated circuits (PICs)

The optical components in photonic integrated circuits were introduced in the section 1.4. In this section, the photonic integrated circuits will be introduced for on-chip interconnection. The III-V compound semiconductor based or Si-based PICs are wildly developed. III-V PICs are easy to integrate each photonic component, however, the high cost and low mechanical strength leads to the unavailability of large-scale integration and mass production. Si photonics has the low cost and high integration density, however, it is difficult to integrate a light source because of the indirect bandgap of Si.

【*Photonic crystal laser based PICs*】

The PhC laser was introduced in section 1.4, which has a large optical confinement due to the photonic crystal structure. The PIC based on PhC laser, PhC waveguide and PhC p-i-n PD was demonstrated in 2015[150]. Figure 1.30 shows the IR camera image of fabricated device. This PhC laser based PIC consists of a LEAP laser, and PD. The whole

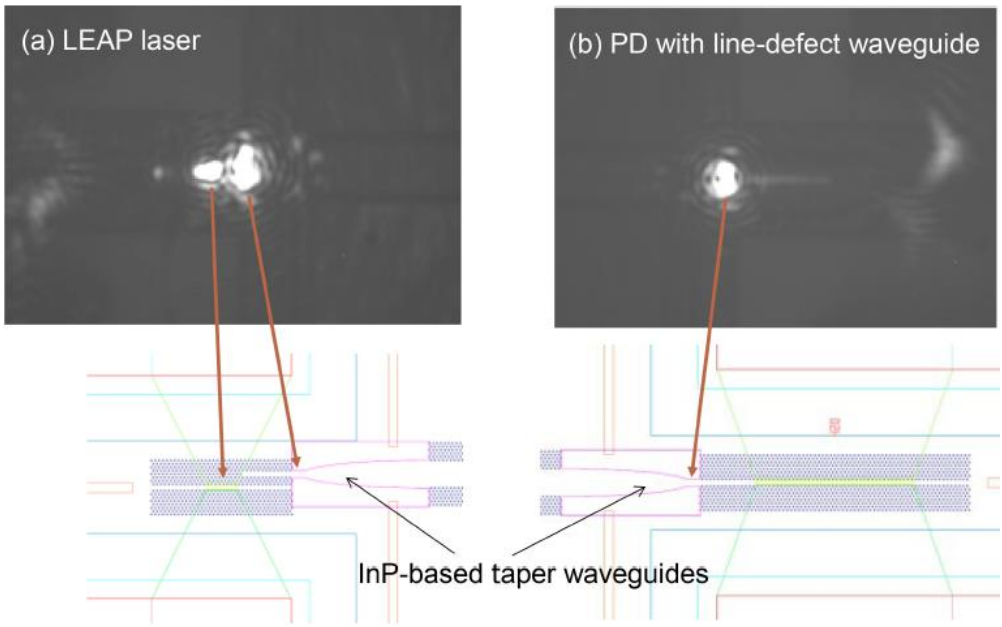


Fig. 1.30 Photonic integrated circuit based on PhC laser, PhC waveguide and PhC p-i-n PD[150].

PIC was constructed with InP-based III-V compound semiconductors. The LEAP laser had an active region length of 3.4 μm. The waveguide width was 3 μm and the transmission length was 500 μm. The PD absorption length was 17 μm. The responsivity of PD was about 0.68 A/W at the waveguide range from 1505 to 1540 nm under the reverse bias voltage of – 3 V. The 3-dB bandwidth was about 3.87 GHz at the reverse bias voltage of – 2 V. The LEAP laser had a low threshold current of 22 μA, and a maximum conversion efficiency of 8.5% (laser current to detected photocurrent) was achieved. The maximum photocurrent of 9.7 μA was achieved at the PD bias voltage of – 1 V. In dynamic data transmission characteristics, an energy cost of 28.5 fJ/bit was obtained at the speed of 4 Gbps, which is the smallest value in the integrated optical link.

This PIC is attractive to the on-chip optical interconnection, because all the III-V photonic components can be integrated at same process line, and the fabricated optical link can be easily integrated to Si by wafer bonding technology. The energy cost is also small, it has the potential to achieve an energy cost lower than 10 fJ/bit at 10 Gbps if the series resistance and slope efficiency of laser were improved. On the other hand, the drawback of this optical link is obvious. The small output power and large thermal resistance limit the higher temperature and higher speed operation.

【*Si photonics*】

The existence of SOI wafers has played a large part in the active research into silicon photonics. High-density integration can be expected because strong light confinement is realized due to the large refractive index difference between the SiO_2 cladding and the Si core, and low loss and compact device can be manufactured. In silicon photonics, research on passive devices, mainly silicon waveguides, is progressing, and silicon nitride (SiN) is emerging as the most suitable material for waveguides in a wide range of applications[151]. However, in Si photonics, since silicon is an indirect transition semiconductor, it is difficult to obtain luminous efficiency comparable to that of group III-V semiconductors, which are direct transition semiconductors. Therefore, it is difficult

to fabricate light-emitting active devices such as light sources and SOA (Semiconductor Optical Amplifiers).

Laser integration on Si photonic integrated circuits

- **Disaggregated lasers**

  The disaggregated lasers are mostly used in Si PICs today. In this system, a separate III-V laser chip coupled to Si PICs through fiber to avoid the difficulty of hybrid integration of Si and III-V. However, high cost (additional packaging and connecting) and large footprint are the disadvantages.

- **Hybrid integration**

  A hybrid integrated solution is to remove the gain chip next to the Si PICs and butt coupled. Individual III-V chip and Si chip are also used. The fabrication process is easy, and no performance sacrifice exists in devices. Figure 1.31 shows an example of silicon photonic hybrid ring-filter external cavity (SHREC) wavelength tunable laser hybrid integration with a passive alignment process[152]. The drawbacks are the requiring precise alignment, high cost in aligning and packaging and large footprint.

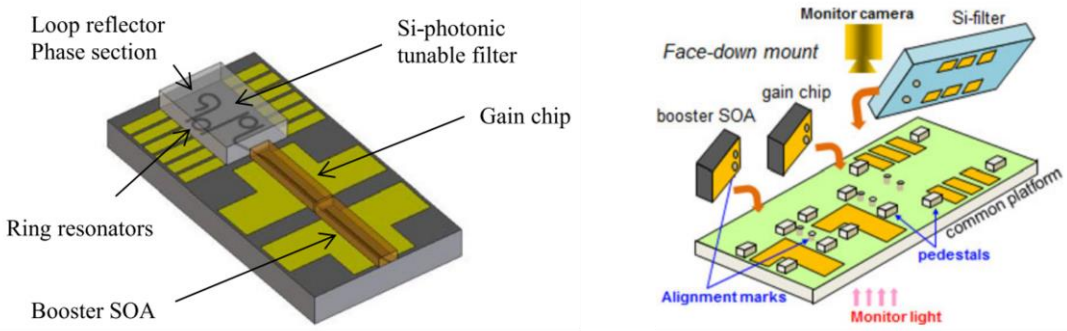


Fig. 1.31 (a) Schematic of silicon photonic hybrid ring-filter external cavity wavelength tunable laser. (b) hybrid integration with passive alignment[152].

➢ **Heterogeneous integration**

The heterogeneous integration solution uses the wafer bonding technology to integrate III-V layers and Si. Various bonding technologies were investigated, which was introduced detailly in section 1.5. This method usually integrates a processed passive Si photonics wafer and processed or unprocessed III-V layers at first. After bonding, a followed processes were carried out to form the laser. It is the promising solution for mass commercial production. The thermal management (thermal stress in bonding interface or thermal resistance in laser), and the fabrication complexity are needed to concern. The current injection AlGaInAs-Silicon hybrid laser was reported by UCSB since 2006 using O_2 PAB[153] (Fig. 1.32). Our group reported low threshold current density operation of a GaInAsP/InP/SOI hybrid laser since 2013 using N_2 PAB[154]. In addition, our group and NTT's group reported membrane laser on Si substrate by BCB bonding or O_2 PAB, which will be introduced detailly in section 1.7.

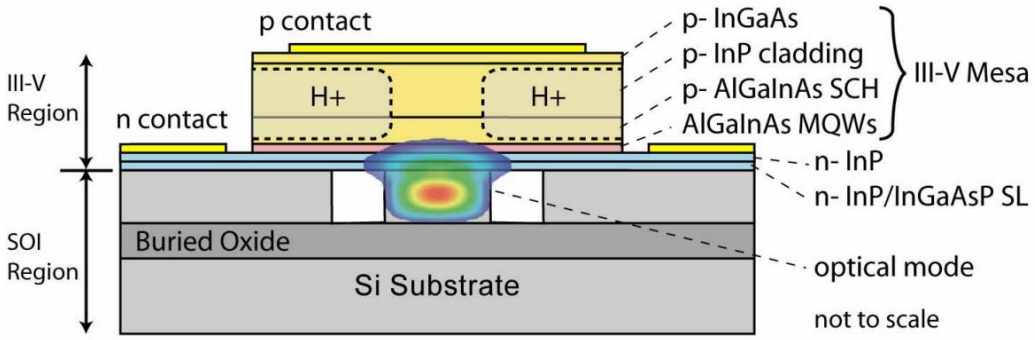


Fig. 1.32 Cross section of AlGaInAs-Silicon hybrid laser fabricated by O_2 PAB[153].

➢ **Monolithic integration**

The monolithic integration solution uses epitaxial III-V growth on Si substrate, which may be the ultimate solution making the most use of existing Si PIC technologies. It has the lower costs, higher integration density and can save unwanted III-V materials. However, the challenges in heteroepitaxy are CMOS compatibility and high density of defects generated from III-V/Si interfaces. The quantum dot laser directly grown on Si (Fig. 1.33) was reported by UCSB[155]-[157].

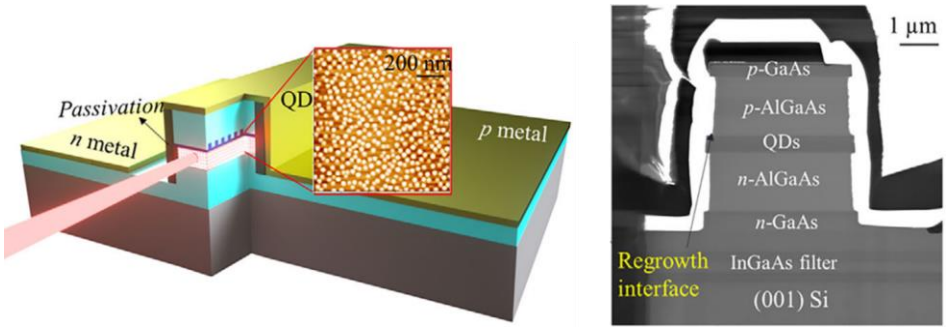


Fig. 1.33 Monolithic integration of quantum dot laser on Si by heteroepitaxy[157].

The path to the photonics integration

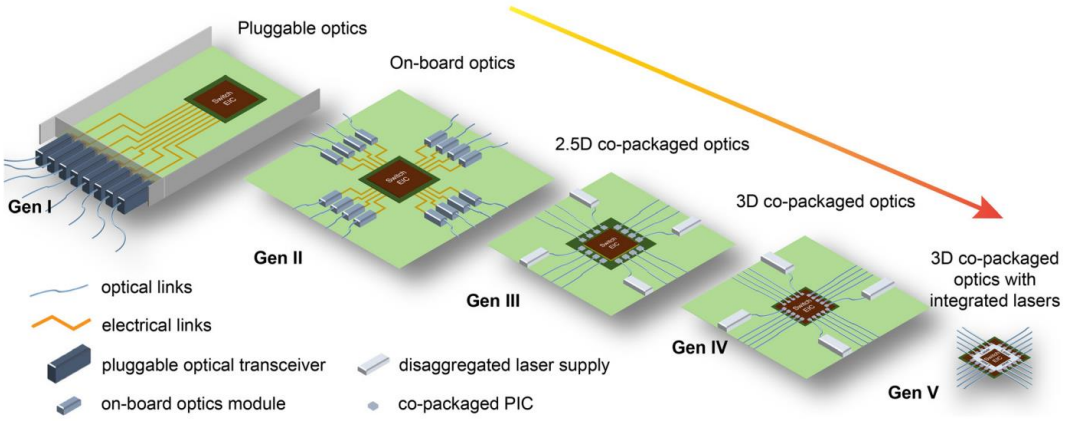


Fig. 1.34 Generation of optics and co-packaging technologies in data center applications[158].

Figure 1.34 shows the path to the photonics integration. In the communication of application-specific integrated circuits (ASICs) and optical link, the optical ports are plugged into a front panel of the host system as an independent system to connect switch serializer/deserializer (SerDes) ports, which was deployed in mass volume in the last 20 years. However, with density and speed increase of optical link, more power consumption of re-timing in optical modules and cost and loss in electrical interconnect between ASIC and pluggable optical modules will gradually emerge[158]. The introduction of CPO (co-packaged optics), a new architecture that replaces part of the electrical wiring with optical wiring and the optical port is placed near the switch within the same package, is expected.

Intel has demonstrated the first 12.8 Tbps programmable Ethernet switch co-packaged with 1.6 Tbps silicon photonics engine in 2020[159]. In “Gen V”, fully integrated (laser) high density Si photonics CPO system releases the large volume of pluggable modules and addresses coupling cost. Overall, the discussion above is to use the Si photonics as an optical I/O. Ultimately, inside the chip, the performance of Si-LSI suffers the increased signal delay and joule heat. The optical interconnect inside a chip to replace the electrical wiring in global wire is an attracting solution. In this case, the surface of Si-LSI distributed transistor devices and SiO_2 cover layer. The general fully integrated Si photonics chip with laser, Si waveguide and PD is difficult to integrated above Si-LSI, because two time of heterogeneous integration should be processed, which reduces the fabrication reliability. We have proposed a concept of membrane structures based optical integrated circuits using III-V materials integrated above the Si-LSI as a global optical wiring to solve this problem, which will be discussed in the next section.

1.7 Semiconductor membrane photonic integrated circuit

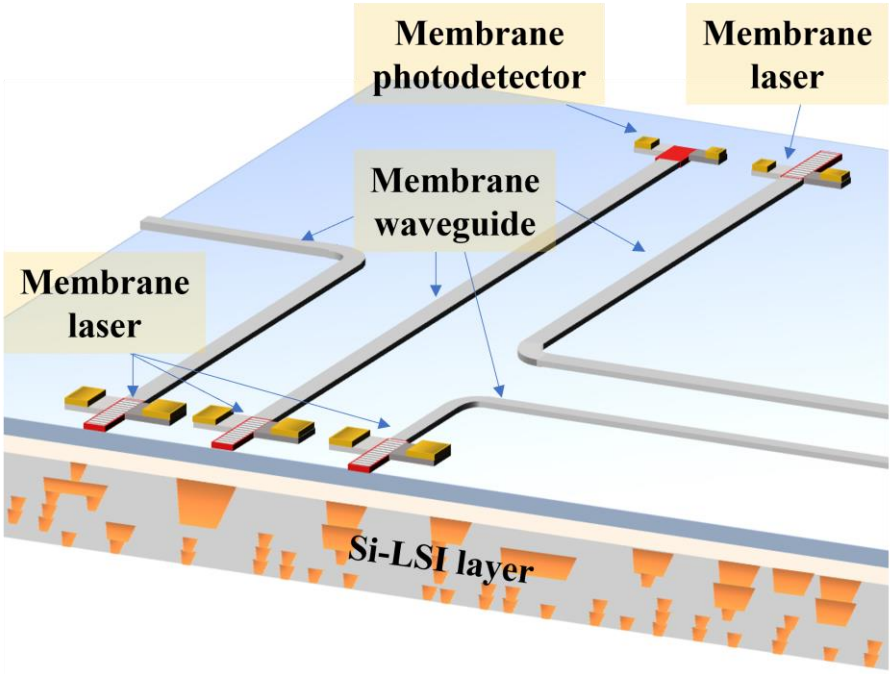


Fig. 1.35 Concept image of membrane photonic integrated circuits (MPICs) on Si-LSI

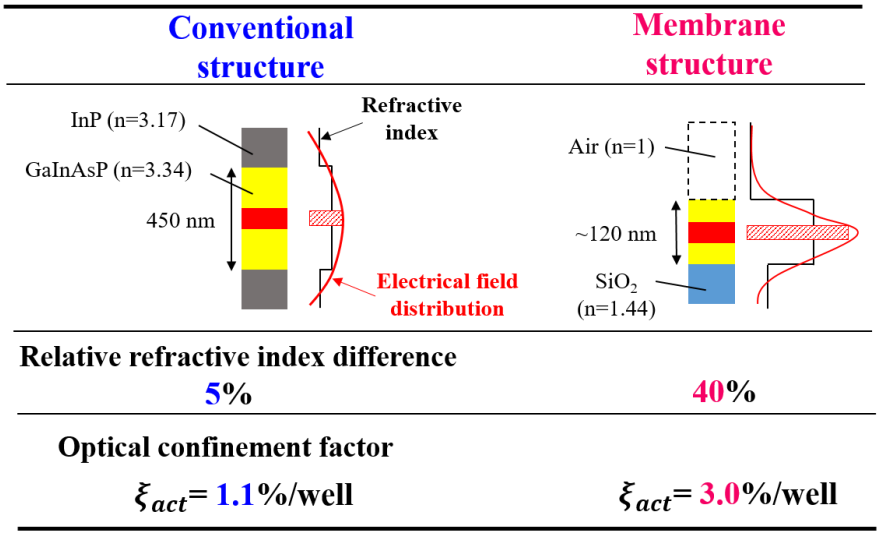


Fig. 1.36 Comparison of optical confinement between membrane and conventional structure

As discussed in section 1.3.1, low power consumption optical devices, especially lasers, are required in on-chip optical interconnect. The light source discussed in section 1.4 have problems such as difficult to integrate to in-plane on-chip optical interconnect or poor output power. Here introduces a light course for on-chip optical interconnect proposed by our group using a "membrane structure" to overcome such problems. Figure 1.35 shows the concept image of InP-based membrane optical link on Si-LSI by BCB adhesive bonding including membrane DFB or DR laser, GaInAsP or InP waveguide, and membrane p-i-n photodiode. The operating wavelength is not limited, however, considering the low-driving volage of Si-LSI, the 1.55 μm long wavelength laser which has a low turn-on voltage, typically 0.82 V, that is suitable to the low power supply by Si-LSI. Therefore, the active layer of GaInAsP was selected and 1.55 μm operating wavelength was used in membrane DFB or DR laser. A III-V waveguide was used to connect laser and photodetector because it is easy to integrate to the membrane optical link, even though more popular materials, such as Si waveguide or SiN waveguide discussed in section 1.4, were widely utilized in Si-photonics. The use of III-V waveguide allows the optical circuit and Si-LSI to be fabricated on different production lines to ensure quality and finally the two circuits are integrated by wafer bonding technology. If introduce a Si waveguide, two times of bonding process are required that would greatly increase the complexity of the fabrication process. In addition, multi-longitudinal mode is not impossible for on-chip optical signal transmission because of the short transmission distance. However, Fabry-Perot structure needs a cleaving facet as the reflection mirror that was difficult to integrate into on-chip optical link, and a DFB or DR based single longitudinal mode structure not only reduce the threshold mode gain but also enhance the stability in the signal modulation. The membrane structure is shown in the Fig. 1.36. The conventional structure is a vertical current injection type, which needs the *p*- and *n*-doped material on the upper side and bottom. For the narrow current structure, a buried hetero structure is necessary. Thus, the index confinement effect is small to the optical mode. On the contrast, the membrane laser adopts a lateral current injection (LCI) structure, and the active core layer ($n = 3.5$) is sandwiched by low refractive-index material such as SiO_2 (n

= 1.4), BCB (n = 1.5) or air (n = 1.0). The refractive-index difference can reach up to 40%, and 3% in a single quantum-well. This large refractive-index difference also results in a strong grating index-coupling reached from 2000 cm^{-1} to 4000 cm^{-1} with the surface InP grating etching depth from 60 to 100 nm. Such strong grating index-coupling lets an ultra-short cavity become possible while maintain enough κL. To the membrane p-i-n photodiode, strong optical confinement can shorten the absorber length while keeping an enough light absorption leading to a larger 3-dB bandwidth (smaller capacitance). In this section, the history of MPICs is described until I started the research.

1.7.1 Research history of membrane optical link in our lab

Membrane laser

【*Optically pumped membrane laser (2001 ~2008)*】

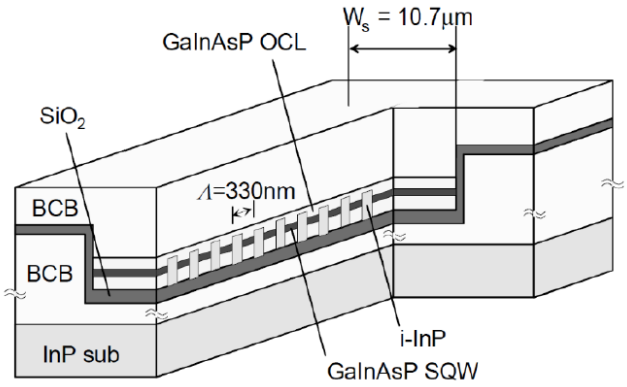


Fig. 1.37 Schematic of first membrane DBF laser operated by optical pumping[160]

Our group has been started the research of membrane laser since around 1999. In the beginning, membrane laser operated by optical pumping. First room-temperature continuous-wave operation of a membrane DFB laser with wire-like active region by optical pumping was demonstrated in 2001[160]. Figure 1.37 shows this structure. 2-μm-thick BCB was coated on both sides. The threshold pump power was 38 mW. In the next 4 years, single mode operation with 0.64 mW low threshold pump power was realized by introducing a narrow stripe structure[161]-[163], and multiple-wavelength laser arrays with

maximum wavelength range of 75 nm were also performed by DFB grating period, grating duty ratio and stripe width modulation[163]-[165]. In 2006, hydrophilic direct bonding on SOI was successfully applied in forming a membrane structure[166]. One year after, the CW operation under optical pumping of membrane laser with rib-waveguide structure was obtained[167]. And at the same year, air-bridge type buried heterostructure membrane laser by optical pumping was demonstrated[168] and also lased up to 85 ºC by Bragg wavelength detuning[169]. At the same time, improvement of temperature dependence on lasing wavelength of membrane BH-DFB laser was successfully achieved by controlling the thickness of core layer and BCB cladding layers[170]. The $d\lambda/dT$ was 0.0245 nm/°C which was approximately 20% - 30% of conventional semiconductor laser. The lowest threshold pump power of 0.34 mW was realized also in 2007 by 80 μm short cavity structure and high index coupling coefficient of 4200 cm^{-1} using surface corrugation grating[171](Fig. 1.38).

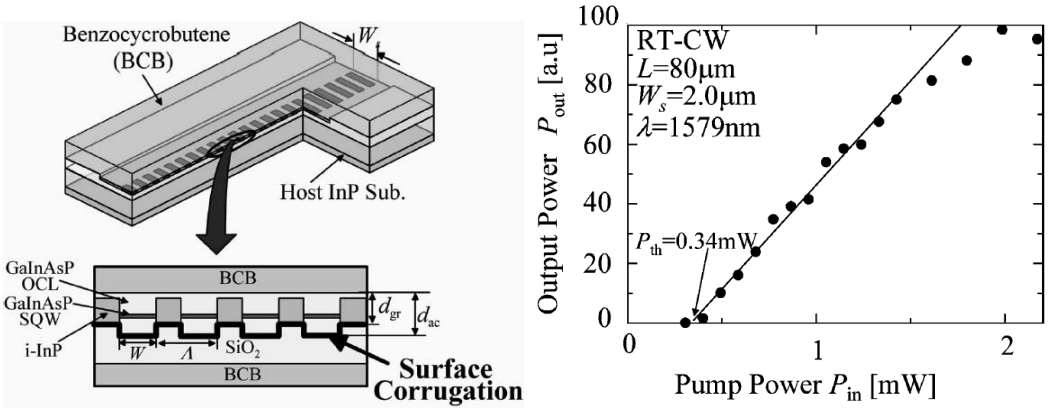


Fig. 1.38 Membrane BH-DFB laser with surface corrugation grating and lowest optical pump threshold power[171].

【*LCI type lasers (2008 ~2012)*】

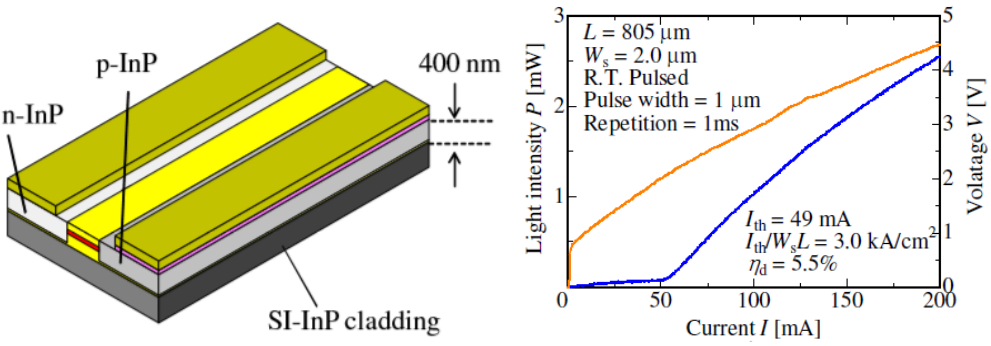


Fig. 1.39 Schematic of first LCI-FP laser on SI-InP in our group[173]

From 2009, for achieving the current injection type membrane lasers, the LCI laser was first investigated. In 2009, room-temperature-pulse operation of current injection type GaInAsP/In/Si DFB laser bonded on SOI wafer with 104 mA threshold current was obtained although it was not based on membrane structure[172]. Then the first LCI-FP laser on simi-insulating (SI) InP in our group was realized in 2009 with 49 mA threshold current[173] (Fig. 1.39). This LCI structure fabricated by two-step OMVPE regrowth. After that, RT-CW operation with a threshold current of 11 mA was obtained by reducing the waveguide loss and increasing the internal quantum efficiency (five quantum wells)[174] with a uniformly distributed quantum wells structure. For further improvement of internal quantum efficiency, the distributed quantum well structure was introduced, and 70% internal quantum efficiency was obtained, which is comparable to that of vertical current injection type semiconductor laser[175] (Fig. 1.40). Another way to improve the internal quantum efficiency is to suppress the surface recombination at the interface between top InP cap layer and optical confinement layer (OCL). Hence, a little thicker InP cap layer, about 50 nm, was introduced. In this case, 66% internal quantum efficiency was obtained[176]. In 2011, a 5.8 mA low threshold current using $\lambda/4$ phase shifted grating, and high external differential quantum efficiency of 43%/facet for uniform grating were demonstrated in the LCI laser with surface a-Si grating[177]-[178].

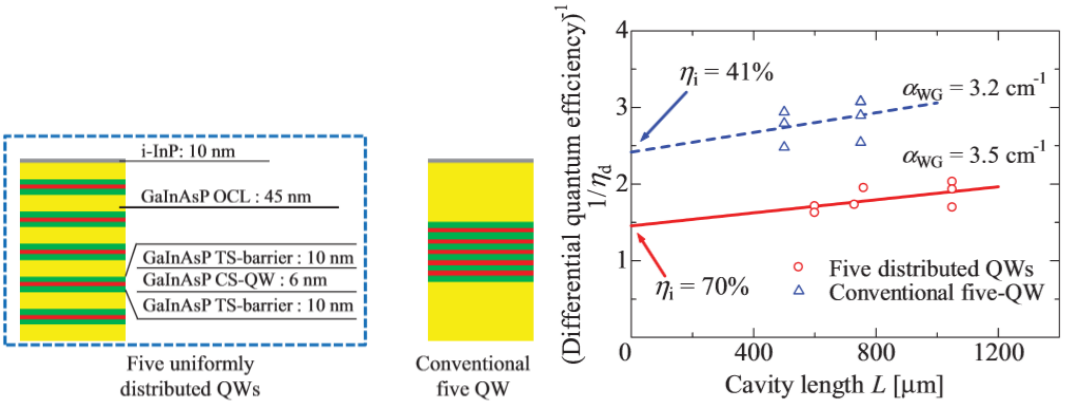


Fig. 1.40 Internal quantum efficiency improvement by introducing distributed QWs[175].

【*LCI membrane lasers (2011~)*】

Lasers explained above all are not based on membrane structure, but those achievements are important to realize the LCI membrane laser. The first LCI type membrane DFB laser was reported in 2011[179]. This laser fabricated by OMVPE regrowth and BCB adhesive bonding using air and SiO_2 as the cladding layer and having a wire-like active region. 83 mA threshold current under RT-pulse operation was obtained. After that, in order to reduce the threshold current, surface grating was used, and 11 mA threshold current was obtained under RT-pulse condition[180]-[181]. One of the causes of the high threshold operation is the degradation of optical property due to impurity diffusion. Thus, Zn-doped GaInAs contact layer was replaced by Be-doped GaInAs contact layer, because that Zn has a large diffusion coefficient and Be or C are well known as p-type dopants with low diffusion coefficient. As a result, 3.8 mA lower threshold current under the RT-pulse condition was obtained[182] (Fig. 1.41). Towards realization of continuous wave operation, thermal properties of membrane DFB laser were analyzed[183], and a thin BCB layer can reduce the thermal resistance according to the analysis. Then a thinner core layer for higher optical confinement and 2 μm thinner BCB (6 μm for previous structure) for lower thermal resistance were introduced. This structure realized the first RT-CW operation of membrane FP laser with a 3.5 mA lower threshold current[184]. By

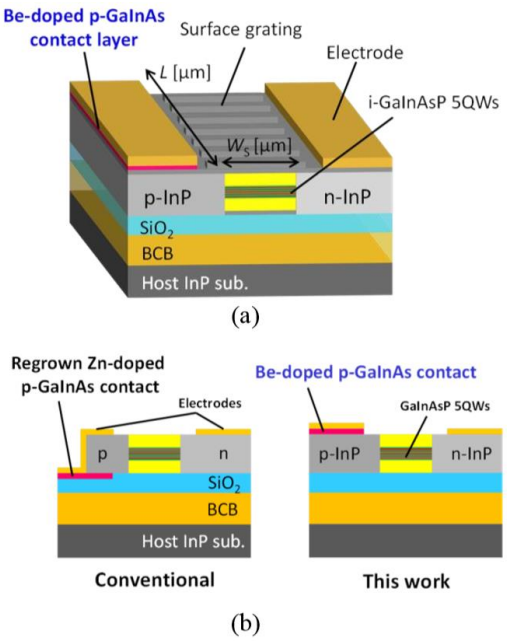


Fig. 1.41 Schematic of the LCI membrane laser with Be-doped contact laser[182].

further reducing the core layer thickness to 158 nm, 0.39 mA low threshold current was obtained[185]. This time, 30 nm surface grating was fabricated, and strong optical confinement limited the output power (3.1% of external differential efficiency). In the same year (2015), DR structure was introduced. It consists of a 30 μm active DFB section and a 90 μm passive DBR section. The passive waveguide was formed by butt-joint built-in (BJB) regrowth process. As a result, 0.25 mA threshold current, 11% of front external differential efficiency was obtained[186]. In 2017, by adopting a lower doping concentration of the p-InP side cladding layer and a shorter distance between the p-side electrode and the active region (0.7 μm) than those of previous work. A threshold current of 0.21 mA, an external differential quantum efficiency of 32% from the front facet, and a power-conversion efficiency of 12% were obtained[187] (Fig. 1.42). Next, a relatively low index-coupling structure (an index-coupling coefficient of around 800 cm^{-1}) was adopted (suppress the surface scattering loss) to improve the differential quantum efficiency, and a differential quantum efficiency of 36% and power conversion efficiency of 14.6% were obtained[188]. Finally, 90 ºC CW operation of membrane DR laser was obtained by Bragg wavelength detuning[189] (Fig. 1.43).

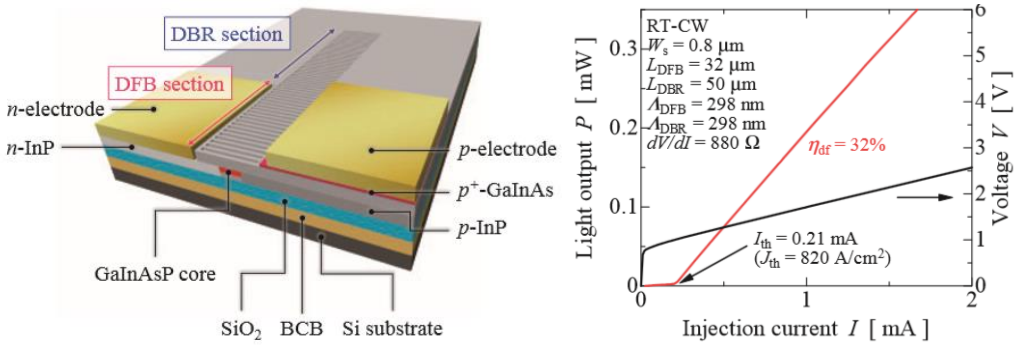


Fig. 1.42 Low threshold and high efficiency membrane DR laser[187].

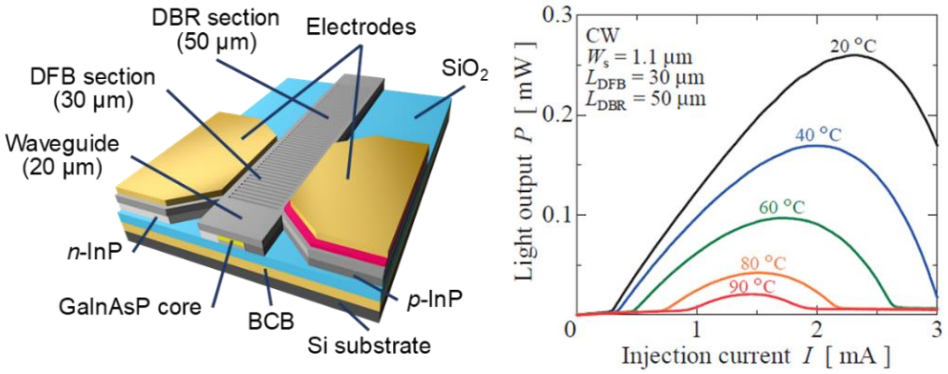


Fig. 1.43 High temperature operation of membrane DR laser[189].

Membrane waveguide

【*GaInAsP wire waveguide (2008~2012)*】

The first GaInAsP wire waveguide was reported in 2009[190]. The design and SEM image are shown in Fig. 1.44. 200-nm-thick BCB was used in the bonding process. Unfortunately, a large propagation loss of 21 dB/cm was obtained, due to a large side wall roughness (3σ = 6 nm), and a poor bonding quality leading to a micro bend of wire waveguide can be considered. After that, improving bonding quality by changing the pre-cure time of BCB leaded to a no serious void bonding. This time, 17 dB/cm propagation loss was achieved[191]. In 2012, the negative resist ma-N2405 was changed to positive resist ZEP520A/ZEP-C_{60}, and the side wall roughness (3σ) was reduced from 3.2 nm to 1.9 nm. The propagation loss was reduced from 17 to 4 dB/cm (Fig. 1.45).

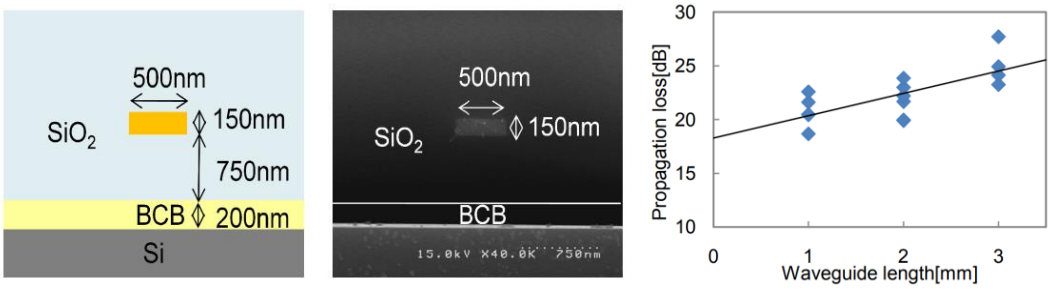


Fig. 1.44 Design and first fabricated GaInAsP wire waveguide on Si substrate[190].

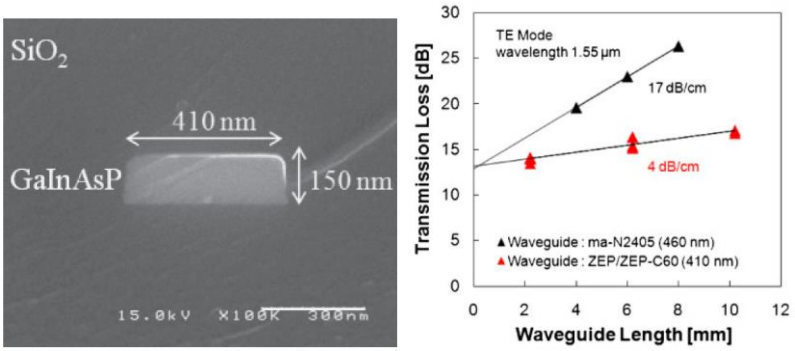


Fig. 1.45 GaInAsP wire waveguide fabricated by an improved BCB bonding process and side wall roughness[192].

Membrane photodiode (2011~)

The first proposed lateral junction membrane photodiode used a five quantum wells and 400 nm core layer that is almost the same with LCI laser in 2011[193] (Fig. 1.46). The device was fabricated on SI-InP substrate using the same process with LCI laser with a 1.4 μm stripe width and 220 μm absorber. A 0.9 A/W responsivity was obtained at 1500 nm and 0.27 A/W at 1550 nm including fiber-chip coupling loss. The 3-dB bandwidth of 7.5 GHz was achieved under a bias voltage of – 2 V. 10 Gbps large data modulation with a clear eye opening obtained with a bit-error-rate (BER) of less than 10^{-12}. In 2013, to increase the responsivity at 1550 nm. The absorber material was changed to GaInAs, and a narrow stripe width of 0.85 μm was fabricated towards high-speed operation[194]. The responsivity was measured to be 0.39 A/W at 1550 nm, and a 3-dB bandwidth of 8.8 GHz was obtained at the bias voltage of -2 V. Also, a 10 Gbps clear eye opening was observed.

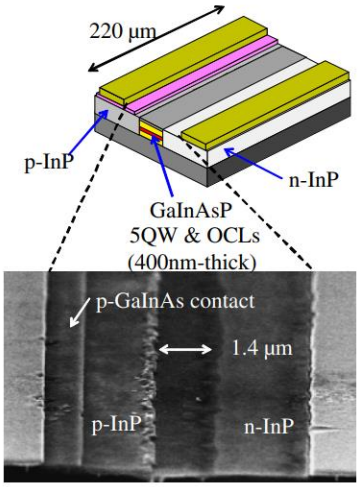
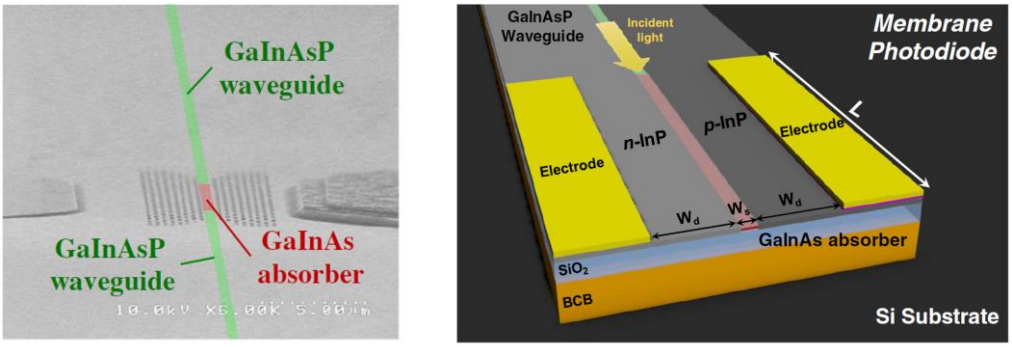


Fig. 1.46 Schematic of MOWs membrane photodiode on SI-InP and SEM top view image[193].

Later, a membrane photodiode on Si substrate fabricated by BCB bonding with photonic crystal structure was theoretically designed[194] and fabricated[195] (Fig. 1.47 (a)). The fabricated PhC membrane photodiode had an absorption length of 7.5 μm and a stripe width of 0.7 μm, both of which was smaller than the previous structure. A 0.19 A/W was obtained at 1550 nm. The GaInAs p-i-n membrane photodiode was fabricated (Fig. 1.47 (b)) at the same time[195][196]. The device had a device length of 30 μm and stripe width of 0.7 μm. A large responsivity of 0.95 A/W was obtained at 1550 nm. The measured 3-dB bandwidth was 13.3 GHz at a bias voltage of -3 V. Finally, the 20 Gbps data rate with a BER less than 10^{-9} was achieved.



(a) (b)

Fig. 1.47 (a) fabricated PhC membrane photodiode (b) GaInAs membrane photodiode on Si[196]

Membrane optical link (2015 ~)

First demonstration of membrane optical link consists of membrane DFB laser of 30-μm-length, GaInAsP buried waveguide of 500-μm-length and MQWs p-i-n photodiode of 200-μm-length was reported at 2015[197]. The membrane DFB laser has the threshold current of 0.28 mA, and maximum output power of ~ 3.5 μW measured from the rear cleaving facet. The dark current of 0.8 nA was obtained at the reverse bias voltage of -1V. The responsivity of the photodiode was estimated about 0.8 A/W at 1550 nm. The maximum detected photocurrent was about 4 μA. The low power of membrane laser may be due to the short cavity length of DFB laser and high loss of front waveguide. The higher responsivity of photodiode at 1550 nm thanks to the higher vertical optical confinement. In 2017, a characteristic improved membrane optical link (Fig. 1.48) was reported[198], and the dynamic property was shown. The length of DFB laser was increased to 80 μm, that leaded to the output power increased up to ~ 43 μW, and the maximum detected current up to 158 μA at the bias voltage of -1V. The measured 3-dB bandwidth was 11.3 GHz at the bias current of 2.73 mA and voltage of -3 V. The 10 Gbps data transmission was achieved with a clear eye opening with a BER of 6×10^{-7} at bias current of 2.5 mA.

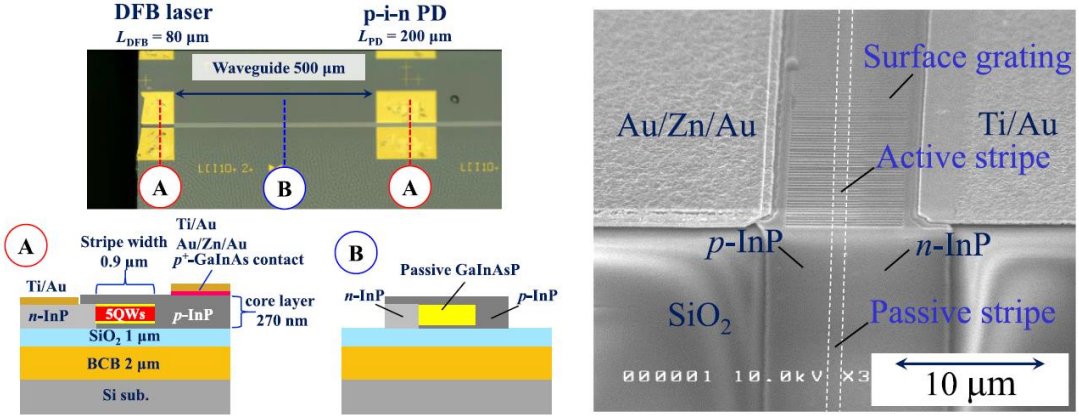


Fig. 1.48 Membrane optical link on Si by BCB bonding[198].

Summary

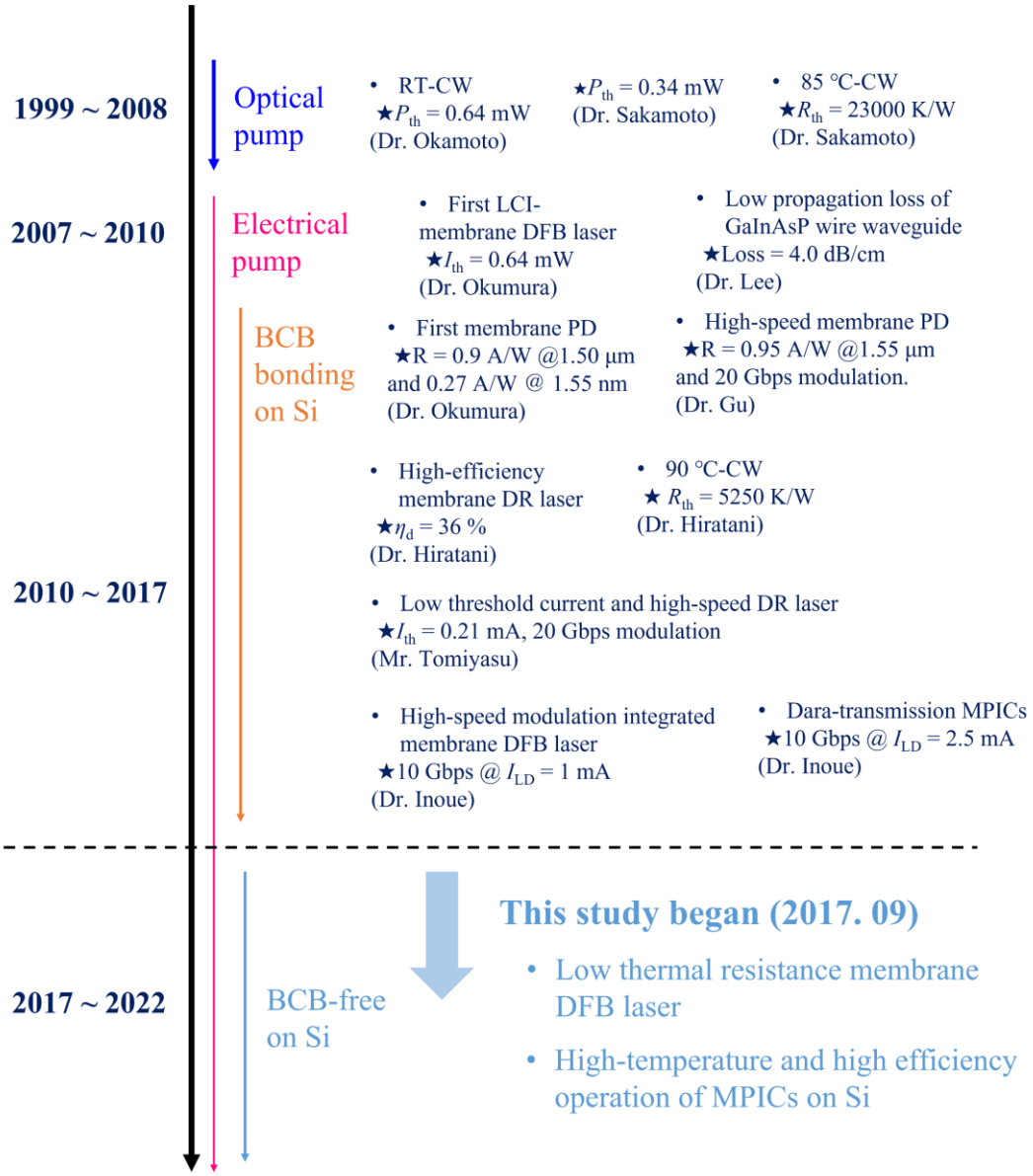


Fig. 1.49 Development of research for membrane optical integrated circuits

Figure 1.49 shows the development of research for membrane optical integrated circuits on Si-LSI. Before this study began, each optical component in membrane on-chip optical interconnect were well studied, and a preliminary demonstration of MPICs was reported. However, all the active devices have a very large thermal resistance, which should be overcome. In addition, lower waveguide loss is needed for cm level data transmission in optical link.

1.7.2 Research history of membrane laser in other groups

The NTT device technology Labs started to study membrane lasers from establishing the technology of GaInAsP/InP buried hetero structure on SiO_2/Si substrate using epitaxial growth after direct bonding (low temperature O_2 plasma assisted hydrophilic bonding at 200 ºC in 2014[202]. The first membrane DFB laser was demonstrated in 2014[203]. The device structure and fabrication process were shown in Fig. 1.50 and 1.51, respectively. They focused on combining low power consumption laser and Si-photonics to reduce the power consumption in optical networks in data centers. The bonding process was before the epitaxial growth for high alignment accuracy between laser and Si waveguide. On the other hand, the bonding process was after the epitaxial growth in our fabrication process because transistors in LSI cannot withstand high temperature in epitaxial growth based on our research background of on-chip optical interconnect. This laser consisted of 150-nm-thick GaInAsP active layer with 6 quantum wells (WQs) sandwiched by 50-nm thick InP layers. The cavity length was 120 μm, and the stripe width was 0.8 μm. A threshold current of 1.8 mA and maximum output power of 1.57

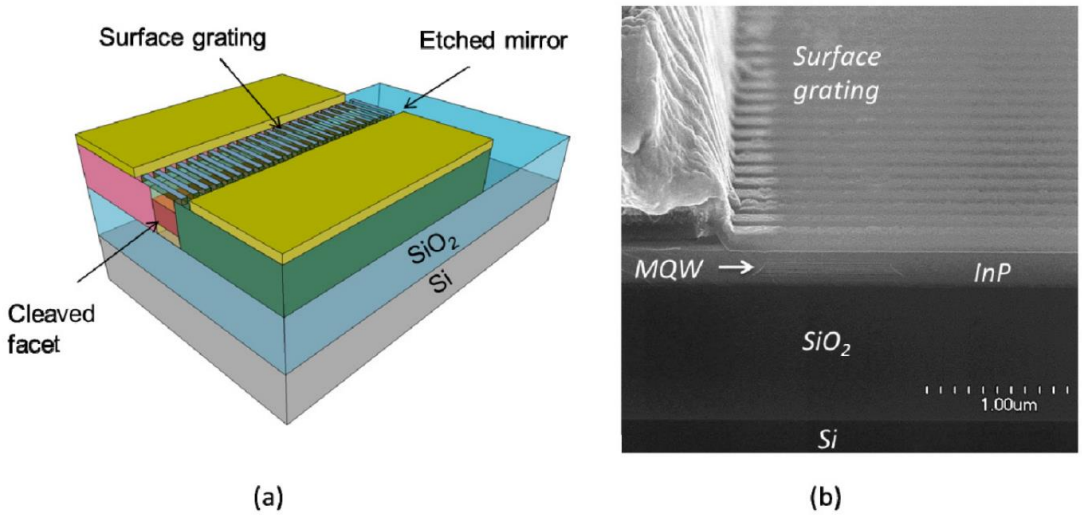


Fig. 1.50 (a) Schematic of fabricated membrane DFB laser. (b) SEM image of the device[203]

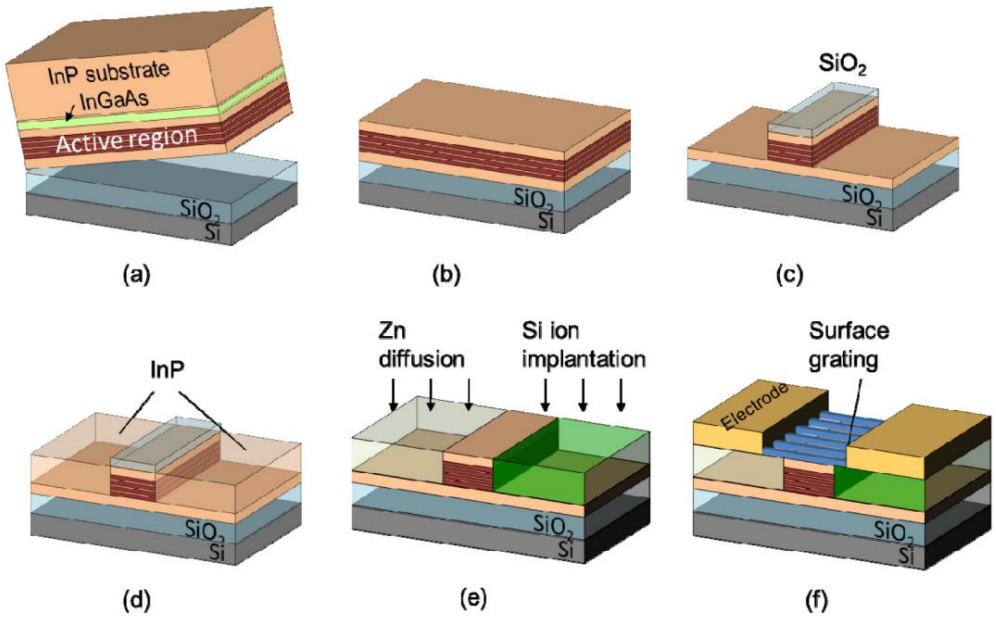


Fig. 1.51 Fabrication process of membrane laser in NTT group[203]. (a) low temperature direct bonding of active layer. (b) Removing unnecessary layers. (c) laser mesa formation. (d) Buried hetero structure growth. (e) Zn thermal diffusion and Si ion implantation. (f) surface SiO_2 grating and electrodes formation

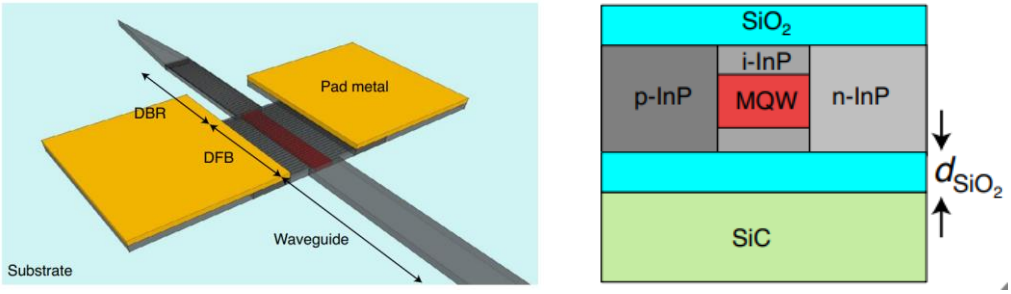
mW were obtained at 25 ºC, and high temperature CW operation up to 100 ºC was achieved. The device operated with a 25.8 Gbps NRZ signal at 50 ºC. Subsequently, 40 Gbps direct modulation was obtained[204]. The low energy cost of 171 fJ/bit was obtained in 25.8 Gbps NRZ signal modulation at 25 ºC[205]. The membrane DR laser with the SiO_x-based spot size convertor (SSC) was demonstrated in 2015[206]. A high modulation efficiency of 9.4 GHz/mA$^{1/2}$ was achieved. The InP wire waveguide on Si substrate by direct bonding with propagation loss of 5 dB/cm was achieved in 2015[110]. After that, the CW operation of membrane DBR laser with 10 μm ultra-short cavity and InP wire waveguide based DBR structure was realized[207]. 0.17 mA low threshold current was recorded in this research.

Membrane DR laser with 20-μm-length $\lambda/4$ shifted DFB and twin DBR mirror on Si was reported from since 2016[208]-[209]. 11.4 GHz/mA$^{1/2}$ modulation efficiency and 163 fJ/bit energy cost at a bit rate of 25.8 Gbps were achieved. 1.3-μm direct modulated membrane DR laser array on Si with InGaAlAs active layer on Si was demonstrated in

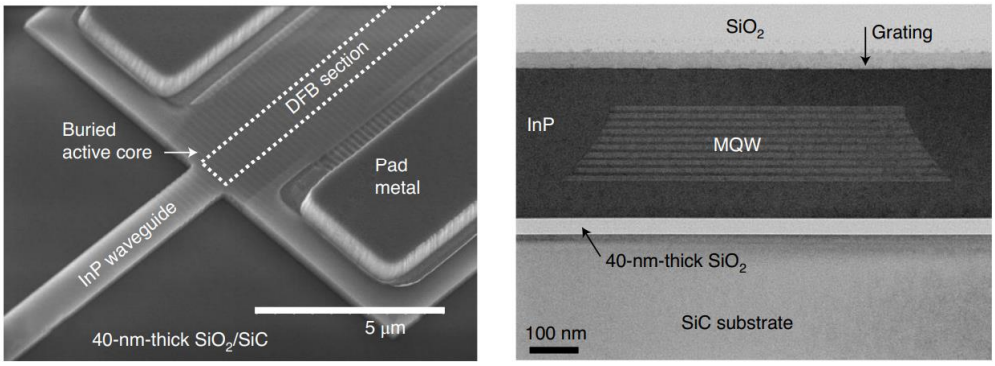
2016[210]. 8-channel, 25.8 Gbps modulation with ~ 200 fJ/bit energy cost was reported.

A thicker active layer of 350 nm was introduced to reduce the series resistance and temperature rise[211]. 97 fJ/bit lower energy cost was obtained at the bit rate of 25.8 Gbps at 25 ºC, and 50 Gbps modulation was also demonstrated. Then, the 1.3-μm membrane DR laser was first used in a short-reach discrete multi-tone (DMT) system, and only 13.6 mA (28.2 mW) of driving current (power) was required[212]. 8-channel 56 Gbps membrane DR laser array integrated with an SSC to connect InP and SiN waveguide and a SiN arbitrary waveform generator (AWG) filter was demonstrated with overall footprint of 1.8 × 2.0 mm^2[213]. The first integration of membrane laser and Si waveguide was demonstrated in 2018[214]. The thickness of Si waveguide was 200 nm. After Si waveguide formation the SiO_2 was deposited, and the active layer of membrane laser was bonded after chemical mechanical polishing (CMP). The fiber output power of 4.6 mW and maximum operated temperature of 130 ºC were achieved with the cavity length of 500 μm, and the thermal resistance was calculated to be 197 K/W. In addition to laser, the 8-channel 56 Gbps PAM-4 (Pulse Amplitude Modulation) signals were successfully detected by membrane PDs[215].

The membrane laser on SiC substrate was firstly demonstrated in 2019[216]. 1.3-μm membrane laser was bonded on 6H-SiC (n ~ 2.58) by 40-nm thick SiO_2 intermediate layer. the highest operation temperature was recorded as 130 ºC with the cavity length of 110 μm. Later, the integration of membrane laser with Mach-Zehnder modulator[217]-[218], electro-absorption (EA) modulator[219] or width-modulated Si waveguide[220] were demonstrated. In 2021, the directly modulated membrane DR laser on SiC substrate using photon-photon resonance (PPR) effect was successfully obtained a 3-dB bandwidth of 108 GHz [221]. Figure 1.52 shows the schematic and SEM images of fabricated device. The ultra-low energy consumption of 38 fJ/bit at the rate of 25.8 GHz of 5-μm length membrane DBR laser was reported[222] and over 67 GHz bandwidth membrane EADFB laser on Si was achieved[223] recently.



(a)



(b)

Fig. 1.52 (a) Schematic of membrane DR laser on SiC. (b) SEM images of fabricated device[221].

1.8 Objective and outline of this thesis

As described above, the study of membrane optical link until this study beginning was in the stage of improving data transmission performance based on the first demonstration of membrane optical link. The remained problems are as follow:

(1) The membrane DR laser operated at the stage temperature of 90 ºC under CW condition by using Bragg wavelength detuning. However, a large thermal resistance of 5250 K/W is a bottleneck which limited output power and high-temperature performance.

(2) The membrane optical link has achieved a 10 Gbps data transmission at room temperature using membrane DFB laser. However, the low slop efficiency of I_{PD}-I_{LD}, low output and high waveguide loss are problems, and the high-temperature operation was limited by high thermal resistance of membrane DFB laser.

Therefore, the objectives of this thesis are given as follows:

【Objective 1】 Investigation of design of high heat dissipation membrane laser structure

(a) Calculation of structure dependence of thermal resistance

(b) Estimation of effect of heat generated from LSI on the laser active layer.

【Objective 2】 Realization of low thermal resistance membrane laser

(a) Investigation of fabrication process

(b) Characterization of thermal properties

【Objective 3】 Realization of high temperature and high efficiency operation of membrane optical link

(a) Investigation of fabrication process

(b) Characterization of static and dynamic properties under various temperature

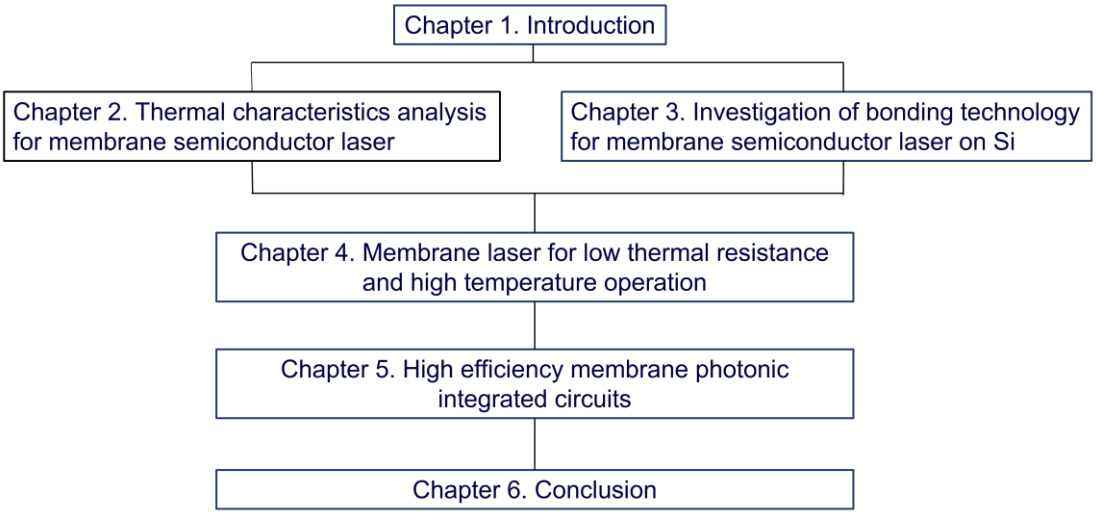


Fig. 1.53 Outline of this thesis

Figure 1.53 shows the outline of this thesis. In chapter 2, after estimating the power and thermal resistance requirement of membrane laser operating at high temperature, the structure dependence of thermal resistance was theoretically analyzed using 3-D finite element method (FEM), and high heat diffusion structures of membrane laser were proposed. Next, the influence of heat generated by Si-LSI on active region was calculated. Then, the laser characteristics were calculated considering self-heating. In chapter 3, various bonding technologies were studied for achieving a low thermal resistance of membrane laser, which included ultra-thin BCB bonding, O_2 plasma activated bonding, and extended surface activated bonding using a-Si nanolayer. In chapter 4, a new fabrication process for BCB-free membrane laser on Si based on chemical mechanical polishing (CMP) and extended surface activated bonding was first investigated. Subsequently, the membrane FP lasers and membrane DFB lasers were fabricated, and the thermal characteristics were estimated. In chapter 5, the membrane photonic integrated circuit on Si by extended surface activated bonding at room temperature with a buried-ridge-waveguide (BRW) structure was fabricated and the static and dynamic characteristic were measured under various ambient temperature. After that, a low loss InP-rib waveguide was investigated, and a InP-rib waveguide integrated membrane

optical link was first demonstrated and measured preliminary, and future prospects were given. Finally, the summary of this thesis will be given in chapter 6.

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Chapter 2

Thermal characteristics analysis for membrane semiconductor laser

2.1 Introduction

In current injection type semiconductor laser, heat generation caused by Joual heating and non-radiative recombination. The electrical resistance of membrane DFB laser was as high as several kΩ[1] at the beginning because of the thin semiconductor layer in lateral current injection (LCI) structure and short cavity design. In order to improve high-temperature characteristics of membrane laser by reducing electrical resistance to reduce self-heating is an effective method. Several methods have been proposed to reduce electrical resistance, such as increasing doping concentration of p-InP side cladding layer, reducing distance between p-electrode and active region, and using Au/Zn/Au to replace Ti/Au p-electrode to reduce specific contact resistance. Fortunately, all methods have been experimentally confirmed to be effective[2]-[4]. Another method can also reduce the self-heating, but instead of reducing the calorific value of heat source, it increases the thermal diffusion, which means low thermal resistance. Thermal resistance is only related to the device structure. The structure dependence of thermal resistance of membrane laser

was investigated in previous works by two-dimensional (2D) finite element method (FEM) using COMSOL Multiplier. This method is suitable for FP cavity. However, when considering waveguide integrated structure and cavity length dependence, 3D-FEM is needed. The membrane laser was bonded on Si wafer now, but the LSI chip would be used in the future. How the heat generated by LSI affects the membrane laser is worth considering. In this chapter, power and thermal resistance requirement of laser at high temperature of 85 °C will be discussed in section 2.2. The structure dependence of thermal resistance by 3D-FEM will be described in section 2.3 and it will be separated into three directions to discuss. The thermal impact of LSI will be discussed in section 2.4. The thermal resistance dependence of threshold current, laser output power and relaxation oscillation frequency will be discussed in section 2.5.

2.2 Requirement of membrane optical link in high temperature

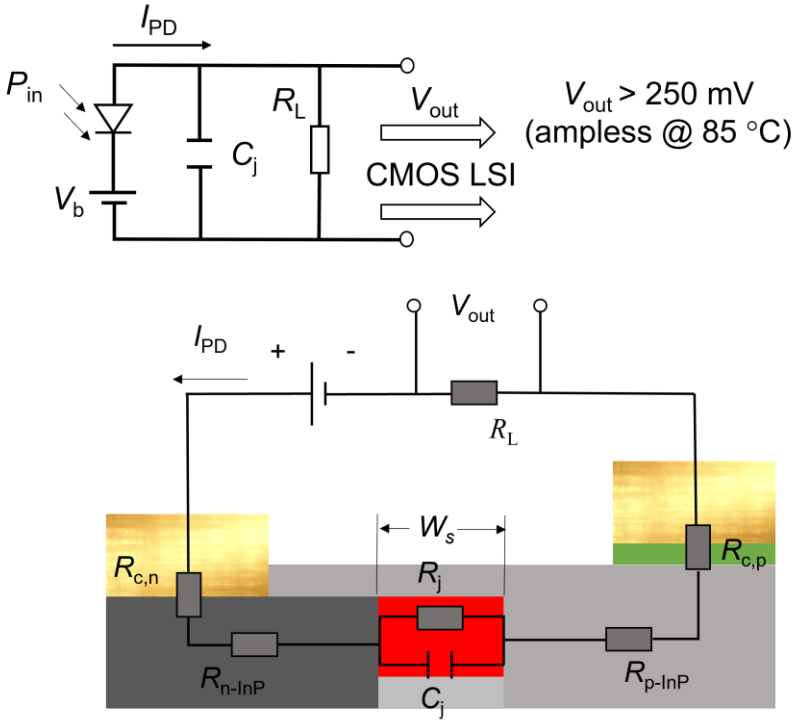


Fig. 2.1 Calculation model of membrane p-i-n photodiode at 85°C

The minimum operation voltage of CMOS circuit $V_{DD,\,limit}$ can be $8kT/q$ (200 mV at 20 °C, 250 mV at 85 °C), which was proposed by R. M. Swanson and J. D. Meindl in 1972[5], where k is the Boltzmann constant, T is the absolute temperature, and q is the elementary charge. As the theory is updated, $V_{DD,\,limit}$ can be $2(\ln 2)kT/q$ (36 mV at 20 °C)[6]. In this calculation, $8kT/q$ was used for considering the practical realization. As the optical wiring on LSI, the membrane photonic integrated circuit should operate at various temperature, such as "un-cooled" signal transmission condition of 85 °C, or even over 100 °C in some extreme cases. Figure 2.1 shows the calculation model of membrane p-i-n photodiode (PD) at 85 °C. For achieving the high output voltage from PD without amplifier, a large load resistance was design to be inserted into PD circuit. Because the PD is operated at a reverse bias voltage, the 3-dB bandwidth is dominated by junction capacitance C_j and load resistance R_L. Thanks to the membrane PD has a high optical confinement factor, the absorption length can be small resulting a small C_j and large bandwidth.

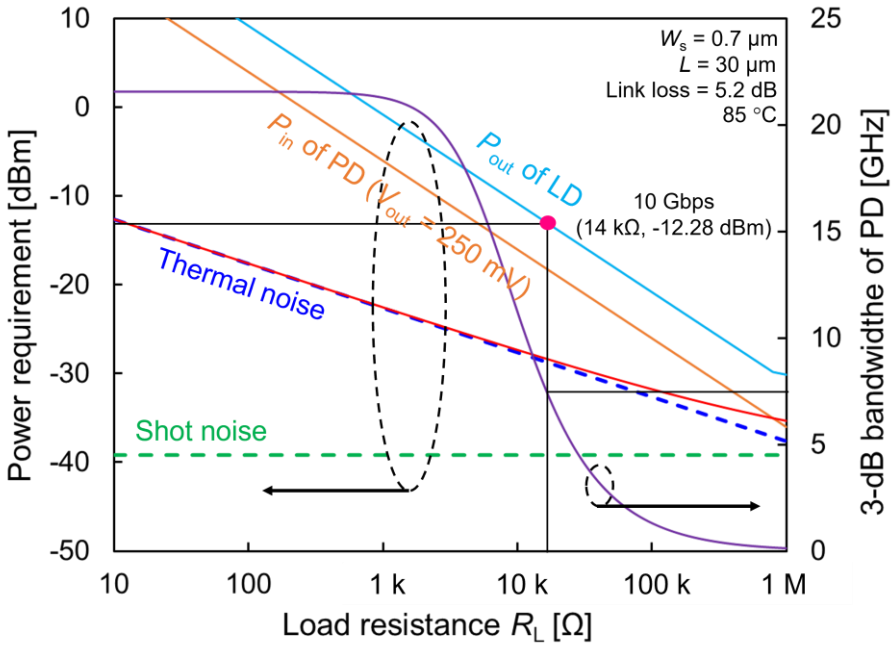


Fig. 2.2 Power requirement of PD, LD and 3-dB bandwidth of PD at 85 °C

Table 2.1 Requirement of membrane optical interconnect at 85 °C for 10 Gbps

Minimum required power of PD	Coupling loss (waveguide/LD/PD)	Propagation loss (2 cm)	Margin	Required laser output power
250 mV output	Theoretical minimum value	Theoretical value		
-17.48 dBm (18 μW)	0.1 dB × 2	1 dB/cm × 2	3 dB	-12.28 dBm (59 μW)

A high speed of 20 Gbps membrane photodiode has been achieved with an absorption length of 30 μm, and a stripe width of 0.7 μm [7]. This model was used in the calculation. Figure 2.2 shows the power requirement of PD, LD and the 3-dB bandwidth of PD. The purple line shows the 3-dB bandwidth of PD as the dependence on load resistance. For achieving the 10 Gbps data transmission, the minimum bandwidth of 7.7 GHz is needed. In this case, the maximum load resistance of 14 kΩ can be found. At the same time, the minimum required power of PD and LD can be found in the orange line and light blue line. Table 2.1 summarized the power requirement of PD and LD. The coupling loss and propagation loss was theoretically assumed, and a fabrication margin of 3 dB loss was

also considered this time. Finally, the laser required power at 85 °C for 10 Gbps data transmission was estimated to be -12.28 dBm (59 μW).

The f_{3dB} of PD can be calculated by Eq. 2.1 ~ 2.3. The junction capacitance was defined by Eq. 2.4. The f_{TT} is the transit frequency. The parameters used in calculation was shown in Table 2.2.

$$\frac{1}{f_{3dB}^2} = \frac{1}{f_{RC}^2} + \frac{1}{f_{TT}^2} \tag{2.1}$$

$$f_{RC} = \frac{1}{2\pi(R_L)C_j} \tag{2.2}$$

$$f_{TT} = \frac{\sqrt{2}}{\pi}\frac{v_{sat}\cdot tanh\left(\mu_h \cdot \frac{v_i}{W_s}\cdot\frac{1}{v_{sat}}\right)}{W_s} \tag{2.3}$$

$$C_j = \frac{\varepsilon_{GaInAs}\cdot\varepsilon_0\cdot h\cdot L}{W_s} \tag{2.4}$$

Table 2.2 Parameters used in 3-dB bandwidth calculation of membrane PD

Discription	**Parameters**	**value**
Slab thickness	h	0.27 μm
Relative permittivity of GaInAsP	$\varepsilon_{GaInAsP}$	13.5
Load resistance	R_L	10 Ω ~ 1MΩ
Saturated hole drift velocity	v_{sat}	4.8×10^4 m/s
Hole mobility	μ_h	0.042 $m^2/V \cdot s$
Vacuum Permittivity	ε_0	8.85×10^{-12} F/m
Bias voltage	v_i	-1 V
Absorber length	L	30 μm
Stripe width	W_s	0.7 μm

$$V_{out}(\text{PD}) = P_{in}(\text{PD}) \times R \times R_L \tag{2.5}$$

$$P_{out}(\text{LD}) = P_{in}(\text{PD}) + \alpha_{wg} + 2\times\alpha_{coupling} + \text{margin} \tag{2.6}$$

Eq. 2.5 ~ 2.6 shows the calculation method of P_{in} (PD) and P_{out} (LD). R is the responsivity of PD, 1 A/W was assumed in the calculation for a simple estimation.

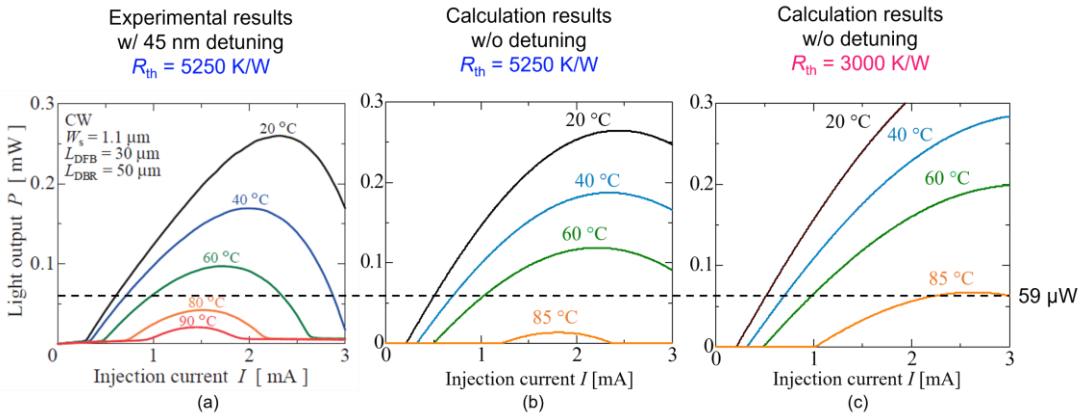


Fig. 2.3 *I-L* characteristic of membrane DR laser for fitting the requirement of thermal resistance. (a) experimental results with 45 nm Bragg wavelength detuning and R_{th} = 5250 K/W[8], (b) calculation results without Bragg wavelength detuning and R_{th} = 5250 K/W, (c) calculation results without Bragg wavelength detuning and R_{th} = 3000 K/W.

After estimating the minimum required power of laser at 85 °C, the required thermal resistance of laser was fitted combining experimental and calculation results. Figure 2.3 shows the fitting result. The detailed calculation method of *I-L* characteristic will be introduced in section 2.5. In the calculation, a typical characteristic temperature T_0 of 50 K of 1.5 μm band GaInAsP laser was used at the temperature range of 20 ~ 70 °C. Since the T_0 itself will be degraded at high temperature, 45 K was used in the temperature over 70 °C for a simple estimation. Figure 2.3 (a) shows the high temperature operation of membrane DR laser with 45 nm Bragg wavelength detuning and the thermal resistance was measured as 5250 K/W. The output power at 80 °C is not enough for the power requirement. Figure 2.3 (b) shows the calculated *I-L* curve to fit the results in Fig, 2.3 (a) without detuning. Figure 2.3 (c) shows the *I-L* curve with the maximum thermal resistance for achieving the required power of 59 μW at 85 °C, which means that at least 43% thermal resistance should be reduced in the future considering the current PD performance and link loss.

2.3 Structure dependence of thermal resistance

In this section, the thermal resistance of membrane laser will be calculated theoretically. The temperature distribution was obtained by using 3D-FEM in COMSOL Multiplier. Heat dissipated power was discussed by using a thermal model of membrane laser including Joule heat and non-radiative recombination. Section 2.3.1 shows the calculation model, and sections 2.3.2 – 2.3.4 show thermal resistance depending on structure, which consists of waveguide and cavity length in cavity direction, electrode thickness, thermal shunt using buried metal, distance between electrode and active region in lateral direction, and BCB thickness, SiO_2 thickness in vertical direction.

2.3.1 Temperature distribution calculated by 3D-FEM

The heat equation is expressed as a function of time t and three-dimensional space coordinates (x, y, z). Since the equation for x and t in one-dimensional space can be easily extended to three-dimensions. Here we start with the derivation of one-dimensional heat equation.

Figure. 2.4 shows a one-dimensional heat transfer model. Assuming that the material has a uniform density and cross-section temperature. Moreover, the heat conduction is only in x direction, and there is no heat diffusion in other directions.

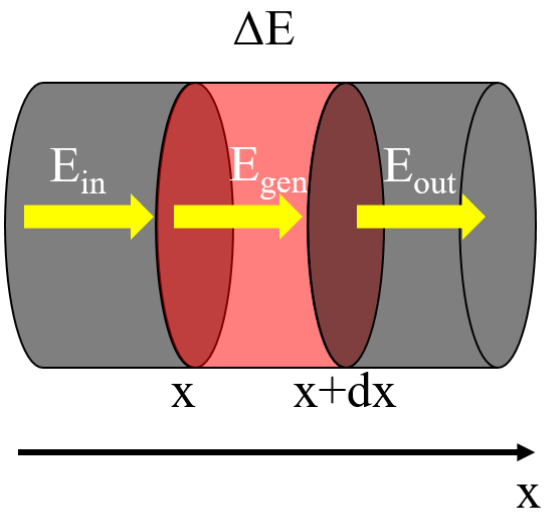


Fig. 2.4 1-D heat transfer model

where,

E_{in}: Heat energy input from outside of the material within Δt seconds.

E_{gen}: Heat energy generated by other energy inside the material within Δt seconds.

E_{out}: Heat energy output from the inside of the material within Δt seconds.

ΔE: Heat energy change inside the material within Δt seconds.

In order to derivate the one-dimensional heat equation, we focus on the [*x, x+dx*] section of this material. Based on the law of conservation of energy, we can obtain:

$$E_{\text{in}} + E_{\text{gen}} - E_{\text{out}} = \Delta E \tag{2.7}$$

Assuming that $T(x,t)$ is the temperature of the material at point x and time t. This time, the heat energy stored inside the material in [*x, x+Δx*] will be:

$$c\rho A\Delta x T(x,t) \tag{2.8}$$

where,

c is the specific heat capacity, [J/K].

ρ is the density, [kg/m^3].

A is the cross-section area of the material, [m^2].

Therefore, the heat energy change within Δt will be:

$$\Delta E = c\rho A\Delta x T(x,t+\Delta t) - c\rho A\Delta x T(x,t) \tag{2.9}$$

The law of heat conduction, also known as Fourier's law, states that the rate of heat transfer through a material is proportional to the negative gradient in the temperature and to the area.

$$q = -\kappa A\frac{\partial T}{\partial x} \tag{2.10}$$

where,

q is the local heat flux density, [W/m^2].

κ is the material's thermal conductivity, [W/(m·K)]

The heat energy passing through the cross-section in x within Δt:

$$E_{\text{in}} = -\Delta t\kappa A\frac{\partial T}{\partial x}|_x \tag{2.11}$$

The heat energy passing through the cross-section in $x+\Delta x$ within Δt seconds:

$$E_{\text{out}} = -\Delta t \kappa A \frac{\partial T}{\partial x}|_{x+\Delta x} \tag{2.12}$$

Assuming that the amount of heat energy generated by a unit volume of material per unit time is Q, which is proportional to volume and time. Therefore, the amount of heat energy generated in section [x, x+dx] within Δt will be:

$$E_{\text{gen}} = \Delta t \Delta x A Q \tag{2.13}$$

Substituting the (2.9), (2.11), (2.12) and (2.13) into (2.7), the following equation can be derived.

$$\begin{aligned} &\left(-\Delta t \kappa A \frac{\partial T}{\partial x}|_x\right) + (\Delta t \Delta x A Q) - \left(-\Delta t \kappa A \frac{\partial T}{\partial x}|_{x+\Delta x}\right) \\ &= c\rho A \Delta x T(x, t+\Delta t) - c\rho A \Delta x T(x, t) \end{aligned} \tag{2.14}$$

Summarize the equation above:

$$\Delta t \kappa A\left(\frac{\partial T}{\partial x}|_{x+\Delta x} - \frac{\partial T}{\partial x}|_x\right) + \Delta t \Delta x A Q = c\rho A \Delta x [T(x, t+\Delta t) - \Delta x T(x, t)] \tag{2.15}$$

Dividing Ac$\rho$$\Delta$t$\Delta$x both side of the equation:

$$\frac{\kappa}{c\rho}\frac{\frac{\partial T}{\partial x}|_{x+\Delta x} - \frac{\partial T}{\partial x}|_x}{\Delta x} + \frac{Q}{c\rho} = \frac{T(x, t+\Delta t) - \Delta x T(x, t)}{\Delta t} \tag{2.16}$$

When $\Delta x \to 0, \Delta t \to 0$, we can obtain the one-dimensional heat equation:

$$\frac{\kappa}{c\rho}\frac{\partial^2 T}{\partial x^2} + \frac{Q}{c\rho} = \frac{\partial T}{\partial t} \tag{2.17}$$

Now we can extend one-dimensional heat equation to three-dimensional heat equation:

$$\frac{\kappa}{c\rho}\left(\frac{\partial^2 T}{\partial x^2} + \frac{\partial^2 T}{\partial y^2} + \frac{\partial^2 T}{\partial z^2}\right) + \frac{Q}{c\rho} = \frac{\partial T}{\partial t} \tag{2.18}$$

In steady state, we can ignore the term of time derivative, so the following equation can be derived[9].

$$-\nabla \cdot (\kappa \nabla T) = Q \tag{2.19}$$

To solve this equation, some boundary conditions are needed. In COMSOL Multiphysics, the following three boundary conditions are often used.

(1) Initial temperature

$$T = T_0 \tag{2.20}$$

This is a boundary condition that sets a fixed temperature in any parts. The bottom of heat sink was set to room temperature (293.15 K).

(2) Heat flux

$$\boldsymbol{n} \cdot (\kappa \nabla T) = q_0 + h\left(T_{inf} - T\right) + \varepsilon\sigma(T_{surr}^4 - T^4) \tag{2.21}$$

where,

$\boldsymbol{n}$ is the direction vector.

q_0 is the heat flux density, [W/m^2].

h is the heat transfer coefficient, [W/(m^2·K)]

ε is the emissivity of the surface.

σ is the Stefan-Boltzmann constant, [J/(m^2·s·K^4)]

T_{inf} is the infinite (far-enough, ambient) temperature, [K]

T_{surr} is the surround temperature, [K]

The first term (heat flux density) can be used as conductance per unit area at the interface with solids. The second term (convection heat transfer) is defined at the interface with the fluid. The third term (radiative heat transfer) is expressed as a boundary condition in the case of radiating. This time we ignored the effect due to radiation since it is not the dominant heat transfer mechanism[10]

(3) Thermal insulation

$$\boldsymbol{n} \cdot (\kappa \nabla T) = 0 \tag{2.22}$$

The thermal insulation is the condition that it is in contact with the ideal material whose thermal conductivity is 0, which means there is no heat flows even if there is a temperature gradient at the interface. This boundary condition was not used in our calculation, because virtually all boundaries have heat exchange.

【***Simulation model***】

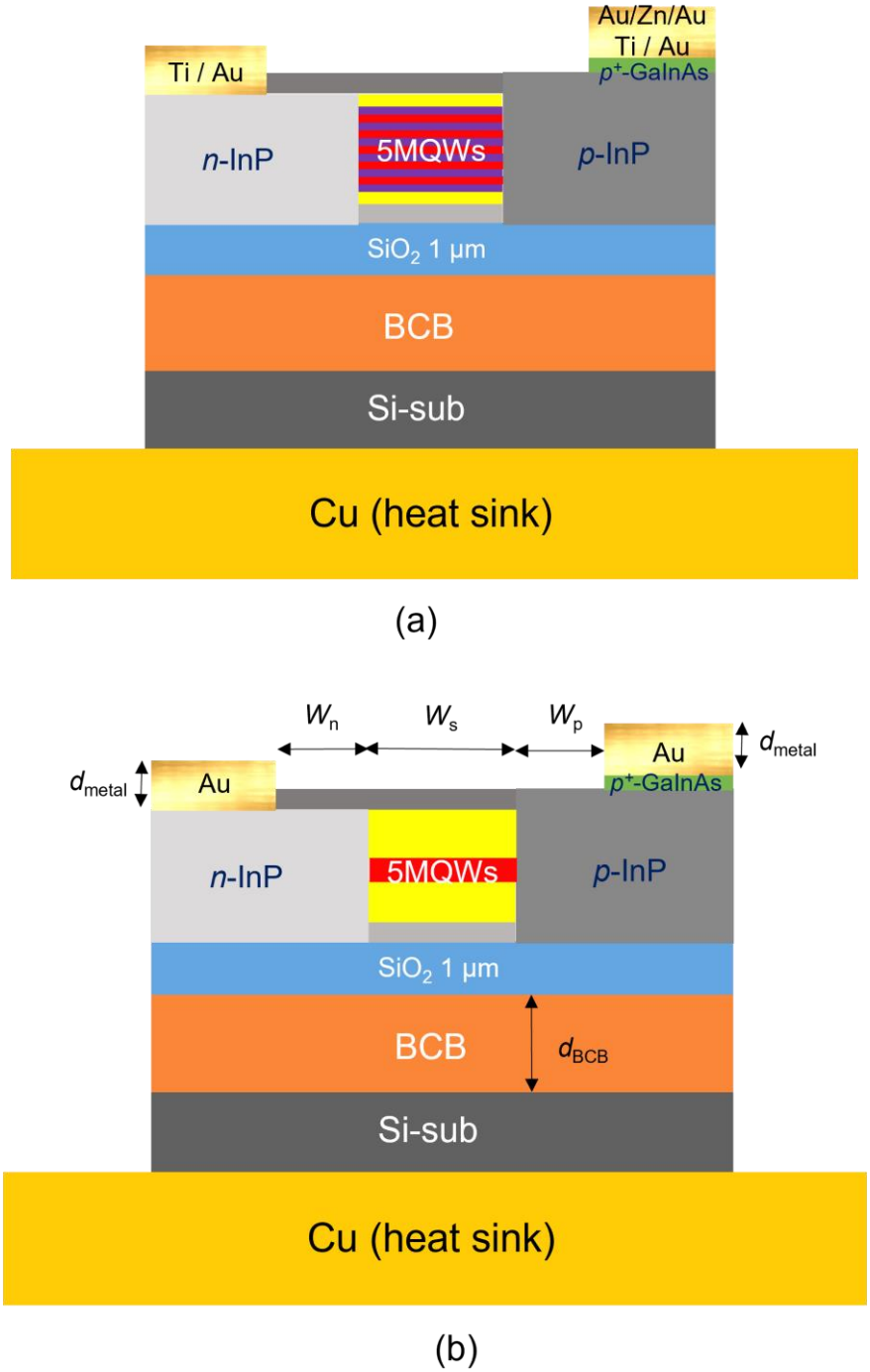


Fig. 2.5 (a) the cross-sectional structure of membrane laser (b) simplified cross-sectional model of membrane laser in heat distribution simulation

The cross-sectional structure of membrane laser was shown in Fig. 2.5 (a). It consists of a 270-nm-thick core layer inluding five quantum wells (6-nm/well $Ga_{0.22}In_{0.78}As_{0.81}P_{0.19}$, 1% compressive strain, λ_g=1520 nm), six barriers (10-nm/barrier $Ga_{0.26}In_{0.74}As_{0.49}P_{0.51}$, 0.15% tensil strain, λ_g=1200 nm) and two optical confinment layers (15-nm/layer $Ga_{0.21}In_{0.79}As_{0.46}P_{0.54}$, λ_g=1200 nm). On the side, there are two InP side cladding layers. The n-electrode of Ti/Au and p-electrod of Au/Zn/Au/Ti/Au are deposited on *n*-InP and *p*-InP, respectively. Under the *p*-electrode, there is a p^+-GaInAs contact layer for reducing contact resistance[11]. Under the core layer, there is a 1-μm-thick SiO_2 cladding layer, a BCB bonding layer and Si-substrate. For shorten the calculation time and reduce the complexity of mesh in simulation model, the simplified model was shown in Fig. 2.5 (b). In this model, there is a 30-nm-thick GaInAsP in the center of active region as the heat source and the rest GaInAsP layers do not participate in heat generation. The metal was changed to Au, because the thickness of Ti and Zn was too thin compared with that of Au. The laser was vacuum chucked on the Cu heat sink for abmient temeprature contron ing. The thermal conductivity of each parts were shown in the Table 2.3. The SiO_2 and BCB has a low thermal conductivity, which maks it difficult to the heat diffusion.

Table 2.3 Thermal conductivity of materials in this simulation[12]-[14]

Material	Thermal conductivity [W/K·m]
Au	319
Cu	403
Si	158
InP	68
SiO_2	1.4
BCB	0.29
GaInAsP	5
GaInAs	4.4

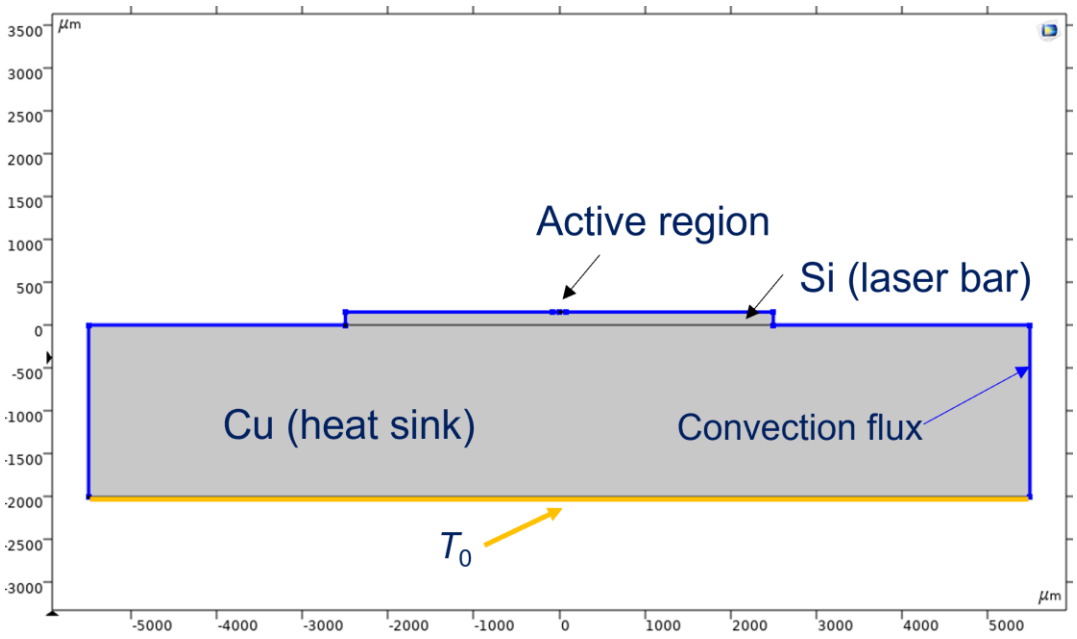


Fig. 2.6 Cross-sectional view of boundary conditions in simulation model

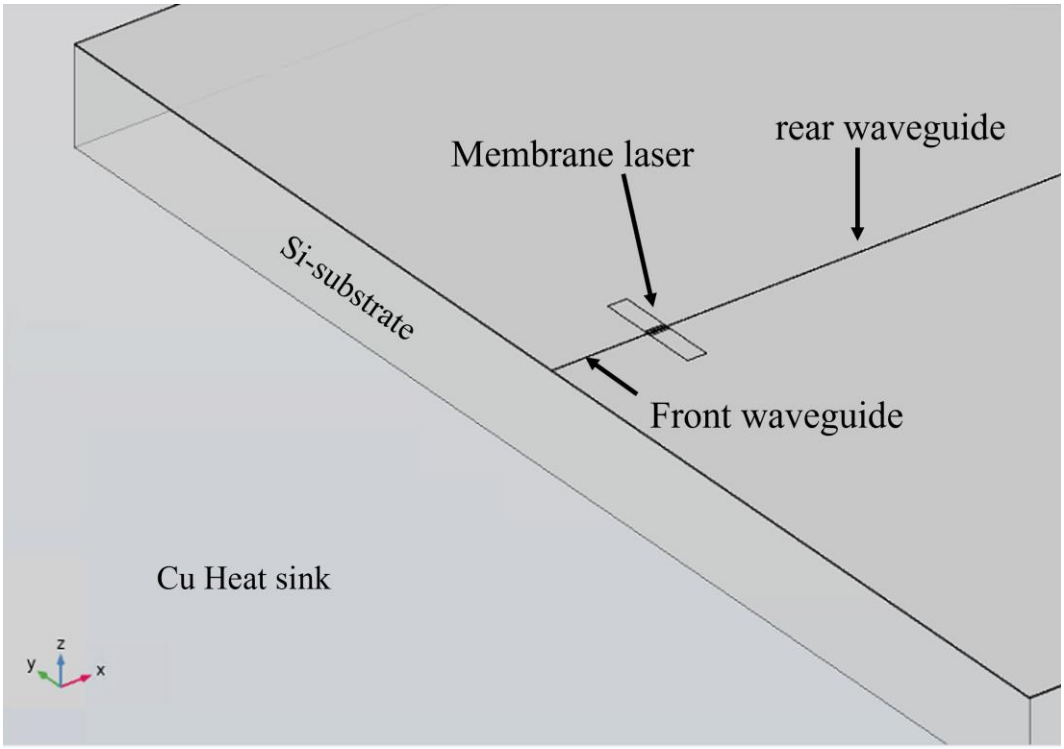


Fig. 2.7 Simulation model in 3D structure view

Figure 2.6 shows the cross-sectional view of boundary conditions in simulation model. The blue line is the convection flux line which represents that all the boundary has the heat exchange with air. The heat transfer coefficient h was set to 4.6 W/(K·m^2) mimicking in an indoor environment. The orange line incidates a fixed temperature on the bottom of heat sink representing a stage temrpature controling environment. The T_0 usually set to 293.15 K. Figure 2.7 shows the 3D structure view of simulation model. The membrane laser was integrated a front and rear passive waveguide for optical integration. In this 3D model, heat can diffuse to the waveguide region and the cavity length direction. The Si substrate thickness was 150 μm. The laser bar has a size of 2000-μm-width and 500-μm-length and the width of n- and p- electrode was 80 μm.

【***Heat source***】

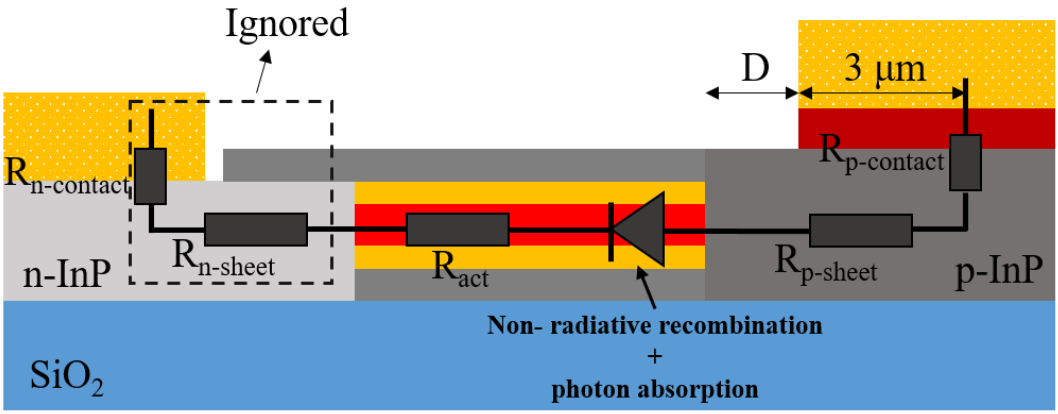


Fig. 2.8 Thermal model of membrane laser

Figure 2.8 shows the thermal model of membrane laser. There are contact resistance between electrode and n, p-electrode, respectively. The R_n, R_p, and R_{act} are the resistance in *n*-, *p*-InP and active region, respectively. These resistors will be the sources of Joule heating. In active region, when electrons and holes are injected, they recombine and realease energy. Two possible recombination process may exist. One is radiative recombination, during witch photons are generated. Another one is non-radiative recombination. Phonons or heat will be generated through phonon recombination or

Auger recombinaiton. In addition, photon absorbtion in spontaneous radiation and stimulated radiation also generates heat. Here, two heat generating mechanisms will be analyzed separately.

1. Joule heat.

Figure 2.9 indicates that the resistivity of InP decreases as the doping concentration increases. Also, it can be seen that the resistivity of *n*-InP is one order of magnitude lower than *p*-InP. The effective mass of electrons in the conduction band is lighter than that of in the valence band. Thus the mobility of electrons is larger than that of holes, resulting in a difference in resistivity between *p*-type and *n*-type InP. Therefore, the resistance of *n*-side InP cladding layer is too small to and can be ignored. too small to ignore. The contact resistance of n-side can also be ignored by assuming the ideal contact resistance of approximately 10^{-6} Ω·cm^2[14]-[15].

Figure 2.10 shows a simplified contact resistanc model in calculation. The voltage drop of the contact resistance on the *p*-InP is due to the sheet resistance R_{sk} of the *p*-InP directly under the contact, and R_{sk}=R_{sh}[16]. And we assume that the current transfer length was 3 μm, where the current transfer length defined as the length of the contact used for transferring most of the current from the semiconductor to the metal or from the metal to the semiconductor. Therefore, the region generated joule heat by *p*-InP is the current

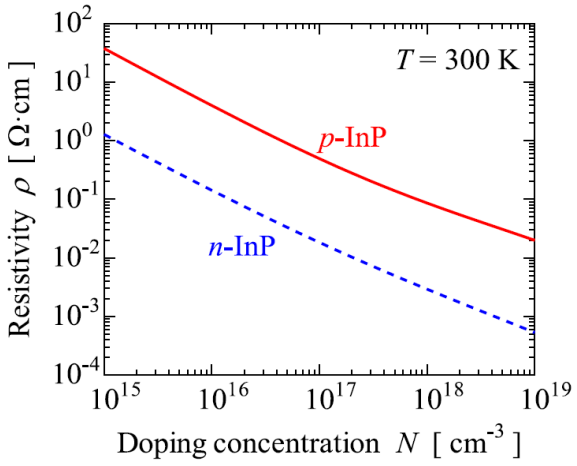


Fig. 2.9 Resistivities of *p*-InP and *n*-InP as a function of doping concentration[17]

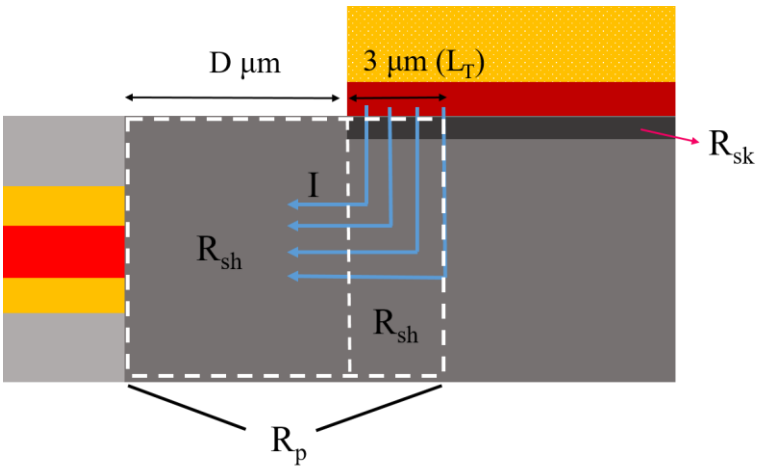


Fig. 2.10 simplified contact resistance model

transfer distance (D+3) μm in p-InP (R_p). As the discussion above, the joule heat can be expressed as Eq. (2.17). In the calculation, the whole differential resistance can be obtained in I-V characteristic of device, and the sum of p-InP resistance and contact resistance is the difference between whole differential resistance and the resistance of active layer. The resistance value of the active layer was estimated from previous research to be 34 Ω for a stripe length of 1.5 μm with a DFB length of 500 μm[18].

$$P_{\text{joule}} = P_{\text{joule,act}} + P_{\text{joule,p}} = (R_{\text{act}} + R_{\text{p}})I^2 \tag{2.23}$$

2. Non-radiative recombination and photon absorption

① **Before lasing ($I<I_{th}$)**[19]

Non-radiative recombination:

$$Q = V_d I_{th}(1 - \eta_{spon}) \tag{2.24}$$

Photon absorption:

$$Q = V_{\text{d}} I_{\text{th}} \eta_{\text{spon}}(1 - f) \tag{2.25}$$

where,

V_{d} is voltage drop across the active region. [V]

I_{th} is the threshold current. [A]

η_{spon} is the spontaneous emission efficiency.

f is the spontaneous emission escape factor (fraction of spontaneous emission escaping the active region)

Eq. (2.25) implies that all the spontaneous emission trapped in the laser is eventually absorbed and dissipated as heat.

3. **After lasing ($I \geq I_{th}$)**[20]

Non-radiative recombination:

$$Q = V_d I_{th}\left(1 - \eta_{spon}\right) + V_d (I - I_{th})(1 - \eta_i)(1 - \eta_{spon}) \tag{2.26}$$

Photon absorption:

$$Q = V_d I_{th} \eta_{spon}(1 - f) + V_d (I - I_{th})(\eta_i - \eta_d) + V_d (I - I_{th})(1 - \eta_i)\eta_{spon}(1 - f) \tag{2.27}$$

where,

η_i is the internal quantum efficiency.

η_d is the external quantum efficiency.

The second term in Eq. (2.26) represents the non-radiative recombination above threshold. The second term in Eq. (2.27) includes the loss of optical energy inside the cavity due to the free-carrier absorption and the diffraction[20]. And the third term in Eq. (2.27) represents the absorption of spontaneous emission above the threshold.

In this study, we assume that the light output of spontaneous emission is zero ($f = 0$), and the light output only comes from stimulated emission for simplicity. Here, the output power to the outside of the resonator is:

$$P_{st} = \eta_d \frac{h\upsilon}{q}(I - I_{th}) = \eta_d E_g (I - I_{th}) \quad (I > I_{th}) \tag{2.28}$$

Where, E_g is the bandgap, and E_g=0.8 eV was used. In other words, the removal of P_{st} from the total power dissipation of the diode is the heat generation. According to the discussion above, the power to heat sources can be expressed as Eq. (2.29) and Eq. (2.30)[21]-[22].

$$P_{act} = V_d I \quad (I < I_{th}) \tag{2.29}$$

$$P_{act} = V_d I - \eta_d E_g (I - I_{th}) \quad (I > I_{th}) \tag{2.30}$$

Next, the voltage V_d was considered. Usually, V_d can be calculated by the following equation.

$$V_d = V - IR_s \tag{2.31}$$

where, R_s is the resistance of device, which means R_{act}+R_P. And a measured value from real device was used in calculation. The bias voltage V before lasing can be expressed by the following equations[23].

$$V = \frac{nkT}{q}\left[\ln\left(\frac{I}{I_s}\right) + 1\right] + IR_s \quad (I < I_{th}) \tag{2.32}$$

Since the stimulation radiation is dominant after lasing, the carrier density is constant, and the voltage applied to the diode is also constant. Therefore, the bias voltage after lasing is:

$$V = \frac{nkT}{q}\left[\ln\left(\frac{I_{th}}{I_s}\right) + 1\right] + IR_s \quad (I > I_{th}) \tag{2.33}$$

where,

n is a dimensionless parameter called the ideality factor, usually included in the I-V relationship to take into account nonideal diode behaviors[23]. In this calculation, n=2 was used[24].

I_s is the reverse saturation current. [A] (7×10^{-11}A[24])

k is the Bolzmann constant [J/K].

T is the temperature [K]. (293 K)

q is the elementary charge [C]

Based on the discussion above, Here, gives an example of calculation of heat source. Table 2.4 shows the parameters used in calculation.

$$\begin{aligned}\text{Heat power } (p-\text{InP}) &= I^2R(InP) = 0.001^2 \times 1087.3 \times 1000\, mW \\ &= 1.09\, mW\end{aligned} \tag{2.34}$$

$$\begin{aligned}\text{Heat density } (p-\text{InP}) &= \frac{\text{Heat power}(p-InP)}{\text{volume}(p-InP)} \\ &= \frac{1.09\ \times 10^{-3}}{(L\cdot 10^{-6})(d_{core}\cdot 10^{-6})[(Lw+Ltp)\cdot 10^{-6}]} \\ &= \frac{1.09\ \times 10^{-3}}{(30\times 10^{-6})(0.27\times 10^{-6})[(3+3)\cdot 10^{-6}]} \\ &= 2.24\times 10^{13}\ W/m^3\end{aligned} \tag{2.35}$$

$$\begin{aligned}\text{Heat power } (act-joule) &= I^2R(act) = 0.001^2\times 62.7\times 1000\ \text{mW} \\ &= 0.06\ \text{mW}\end{aligned} \tag{2.36}$$

$$\begin{aligned}\text{Heat density } (act-joule) &= \frac{\text{Heat power } (act-joule)}{\text{volume}(act)} \\ &= \frac{0.06\times 10^{-3}}{d\_\text{well}\cdot n\_\text{well}\cdot 10^{-6}\cdot \text{Ws}\cdot 10^{-6}\cdot L\cdot 10^{-6}} \\ &= \frac{0.06\times 10^{-3}}{0.006\times 5\times 10^{-6}\times 1.1\times 10^{-6}\times 30\times 10^{-6}} \\ &= 6.33\times 10^{13}\text{W/m}^3\end{aligned} \tag{2.37}$$

$$\text{Voltage V before lasing} = \frac{nkT}{q}\left[\ln\left(\frac{I}{I_s}\right)+1\right]+IR \tag{2.38}$$

$$\text{Voltage V after lasing} = \frac{nkT}{q}\left[\ln\left(\frac{I_{th}}{I_s}\right)+1\right]+Ith\cdot R+(I-Ith)R \tag{2.39}$$

$$\begin{aligned}\text{Voltage } V_{th} \text{ at lasing point } &= \frac{nkT}{q}\left[\ln\left(\frac{I_{th}}{I_s}\right)+1\right]+Ith\cdot R \\ &= \frac{2\times 1.38\times 10^{-23}\times 293}{1.6\times 10^{-19}}\times\left[\ln\left(\frac{0.29\times 10^{-3}}{7\times 10^{-11}}\right)+1\right] \\ &+ 1150\times 0.29\times 10^{-3} = 0.82+0.33 = 1.15\ \text{V}\end{aligned} \tag{2.40}$$

$$\begin{aligned}\text{Voltage } V(1mA) = V_{th}+(I-I_{th})R = 1.15+(1-0.29)\cdot 1150 = \\ 1.97\ \text{V}\end{aligned} \tag{2.41}$$

$$\text{Voltage drops } V_d\ (1mA) \text{ in active region} = V(1mA) - I \cdot R = 1.97 - 1 \times 10^{-3} \times 1150 = 0.82\ \text{V} \tag{2.42}$$

$$\text{Light output } P_{out}\ (1\ mA) = E_g \cdot \eta_d \cdot 2 \cdot (I - I_{th}) = 0.8 \times 0.23 \times 2 \times (1 - 0.29) = 0.26\ \text{mW} \tag{2.43}$$

$$\text{Non-radiative recombination } P\ (1mA) = I \cdot V_d - P_{out} = 1 \times 0.82 - 0.26 = 0.56\ mW \tag{2.44}$$

$$\text{Heat density}(\text{Non} - \text{radiative recombination}) = \frac{\text{Non-radiative recombination } P\ (1mA)}{volume(act)} = \frac{0.56\times10^{-3}}{\text{d\_well}\cdot\text{n\_well}\cdot10^{-6}\cdot\text{Ws}\cdot10^{-6}\cdot L\cdot10^{-6}} = \frac{0.56\times10^{-3}}{0.006\times5\times10^{-6}\times1.1\times10^{-6}\times30\times10^{-6}} = 5.65 \times 10^{14}\text{W/m}^3 \tag{2.45}$$

$$\text{Heat density}(act) = \text{Heat density}(act - joule) + \text{Heat density}(\text{Non} - \text{radiative recombination}) = 6.33 \times 10^{13} + 5.65 \times 10^{14} = 6.28 \times 10^{14}\ \text{W/m}^3 \tag{2.46}$$

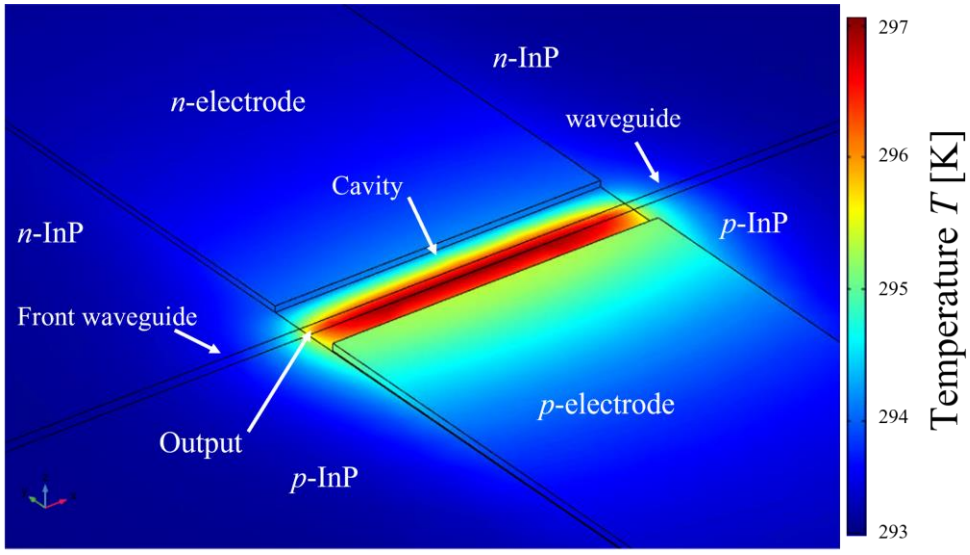
Table 2.4 Parameters used in heat source calculation

Parameters	Value
Stripe width *W*s [μm]	1.1
Current transfer length L_{tp} [μm]	3
Distance between electrode and active region L_w [μm]	3
Cavity length L_{DFB} [μm]	30
Threshold current I_{th} [mA]	0.29
Thickness of core layer *d*_core [μm]	0.27
Charge element amount q [C]	1.6×10^{-19}
Reverse saturation current I_s [A]	7×10^{-11}
Bandgap E_g [eV]	0.8
Number of quantum-well *n*_well	5
Differential resistance *R* [Ω]	1150
R(act) [Ω]	62.7
R(*p*-InP) [Ω]	1087.3
External differential quantum efficiency η_d/facet	0.23
Bias current *I* [mA]	1
Boltzmann constant k [J/K]	1.38×10^{-23}
Room temperature T [K]	293.15
Ideality factor n	2
Thickness of quantum well *d*_well [μm]	0.006

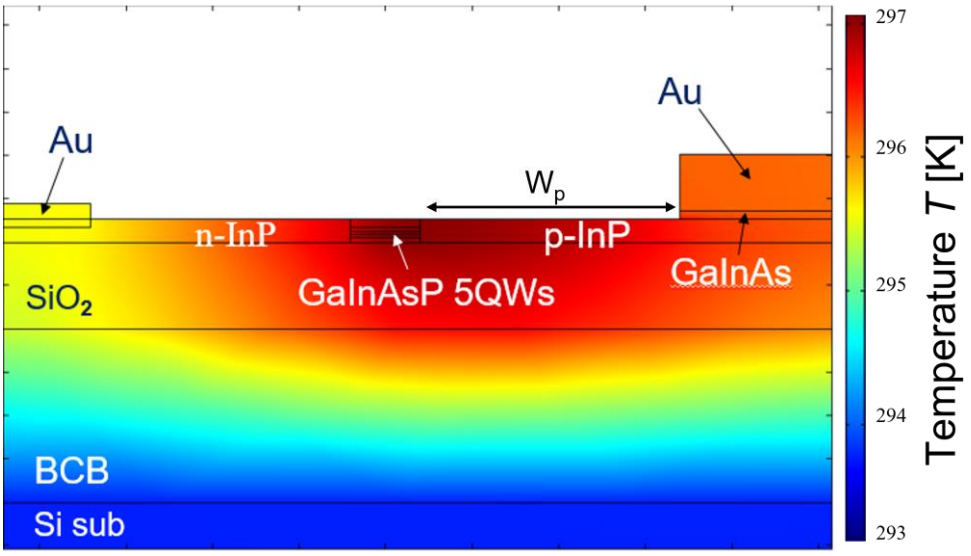
From the calculation above, the heat density of InP and active region are very large in membrane laser. And the heat density of active region is one order of magnitute larger than heat density of InP, which indicates the non-radiative recombination dominate the laser self-heating. Figure 2.11 shows the temperature distribution using 3D-FEM model. From 3D view, it is clear that the heat diffused into waveguide and cavity length. From cross-sectional view, the thick BCB layer prevents the heat to transfer into Si, indicating that a thin BCB layer or removing BCB layer is a promising solution to reduce thermal reseitance of membrane laser. The detailed calculation of thermal resistance will be discussed in the next section.

For calculation of thermal resistance, Eq. (2.47) was used. After inputing the initial temperature of simulation model and heat density of heat sources, the temrpature change ΔT of active region can be obtained from COMSOL.

$$R_{th} = \frac{\Delta T}{P_{joule,p} + P_{joule,act} + P_{act}} \tag{2.47}$$



(a)



(b)

Fig. 2.11 Temperature distribution of membrane laser (a) 3D view (b) cross-sectional view

2.3.2 Cavity direction

From Eq. (2.47), the thermal resistance depends on temperature rise of active region and the whole heat dissipated power, and the temperature rise of active region depends on the thermal conductivity of meterial surrounding it. Figure 2.12 shows a concept diagram of heat diffusion using 2D model and 3D model. In 2D simulation, there is no z axis. Therefore, heat can only diffuse to x and y direction at the point of $z = 0$. However, in 3D model, heat can diffuse to x and y direction at each point of z axis and z direction.

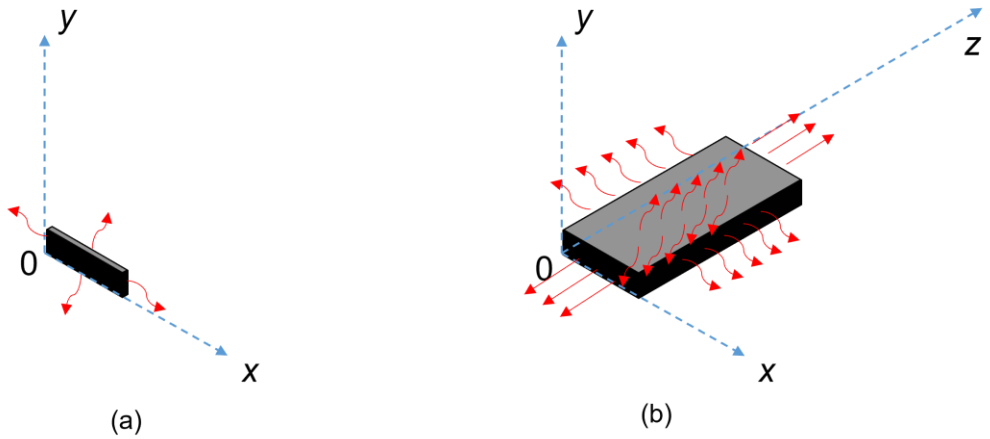


Fig. 2.12 Heat diffusion concept diagram of (a) 2D model (b) 3D model

When considering a heat transfer to vertical direction to the heat sink, lateral direction to electrode or cavity direction to waveguide based on Fourier's law (Eq. (2.10)), the area A was increased or distance was shortened in $\partial T/\partial x$ while canvity becomes longer, which indicates that the thermal resistance is reverse proportional to the cavity length. Figure 2.13 shows the thermal resistance and active region temperature depend on cavity length with a fixed heat density of InP (2.24×10^{13} W/m^3) and active region (6.28×10^{14} W/m^3). Because the heat density was fixed, every cross-sectional structure equals to a 2D model. However, the cross-sectional area of each face becomes larger leading to a lower thermal resistance, which is similar with the electrical resistance. When the cavity length is 10 μm, over 7000 K/W thermal resistance exist even with a condition of well contact to heat sink.

Figure 2.14 shows a comparision of thermal resistance calculation by using 2D and 3D

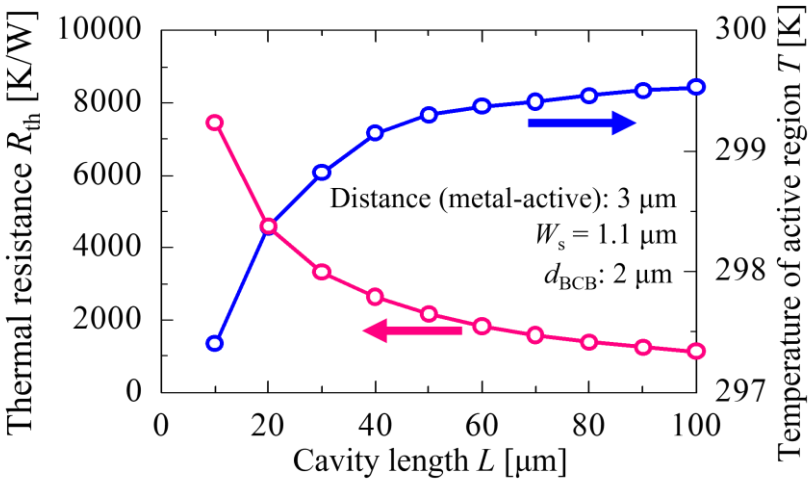


Fig. 2.13 Thermal resistance and active region temperature depend on cavity length with a fixed heat density of InP (2.24×10^{13} W/m^3) and active region (6.28×10^{14} W/m^3)

model. 3D model shows a lower thermal resistance compared with that of in 2D model because the heat can diffuse from heat sources to waveguide and cavity direction. The value was lower than the measured thermal resistance in real device due to the thermal contact resistance exist between device and heat sink. During the heat transfer process of solid surface contact, it is generally considered that the two surfaces in contact with the surfaces are flat and smooth, and the contact between the two surfaces is good. In practice, however, solid surface contact is generally unlikely to be tight. At the micro or nano scale, their contact surface has obvious surface roughness, more point contact or uneven small area contact. This means that the heat conduction between the solid walls is actually composed of the conduction of the contact part, the air convection in the gap formed by the contact point, and the cavity radiation formed by the gap. Because air is a poor conductor of heat, relative to good surface contact, this part adds additional heat transfer resistance during the thermal conduction process of the object, which is called thermal contact resistance. The factors affecting the contact thermal resistance are complex, which includes the type of material, the surface roughness of the material, the surface flatness, the matching of the hardness of the two surface materials, the positive pressure on the contact surface, the clean state of the surface material, the degree of oxidation, and the

filling medium between the two surfaces. So the numerical calculation of contact thermal resistance needs to be determined by experiments,

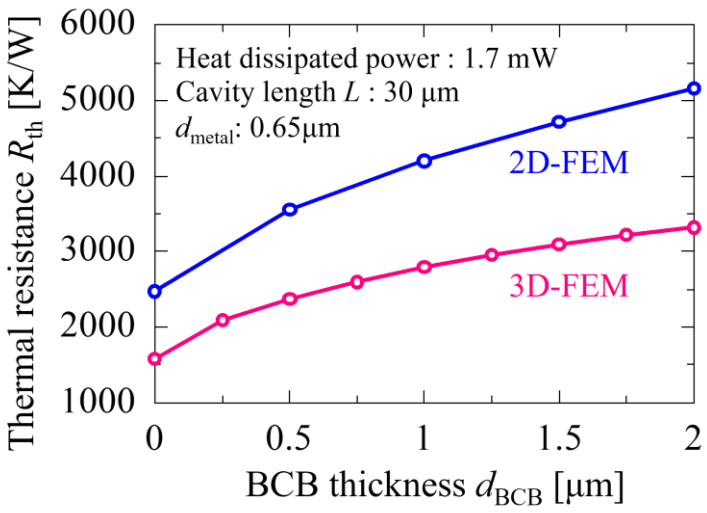


Fig. 2.14 Comparison of thermal resistance calculation by using 2D and 3D model

2.3.3 Lateral direction: thermal shunt

In lateral direction, distance between electrode and active region W_p and thickness of electrode d_{Au} deserve attention. Figure 2.15 shows the thermal resistance depends on distance between *p*-electrode and active region. The distance between *n*-electrode and active region was designed with a fix value of 3 μm considering the fabrication tolerance, since the heat generated from *n*-InP is smaller than *p*-InP. The thermal resistance is slightly reduced when the distance becomes short. Previous calculation showed that it is better to keep a $W_p > 1.6$ μm in flatten structure for low waveguide loss in active region and this value can be reduced to 1.0 μm in ridge structure in active region[21]. Therefore, this method has little influence to the thermal resistance, however, it has a more influence to electrical resistance.

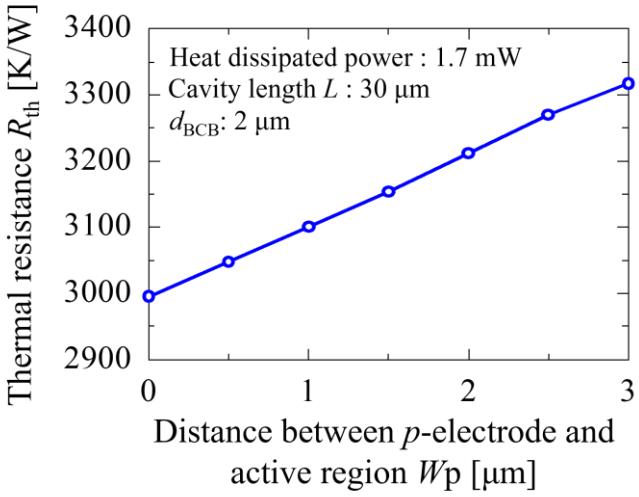


Fig. 2.15 Thermal resistance depends on distance between p-electrode and active region

Figure 2.16 shows the thermal resistance depends on electrode thickness. The thicker the electrode, the larger the surface area for exchanging heat with the air, and the lower the thermal resistance. The heat diffision saturated at the thickness near 3 μm. 38% thermal resistance can be reduced at $d_{Au} = 3$ μm. So far, a 0.65 μm thick metal was used in the electrode deposition. For thicker electrode, a plating technic can be used for considering both process time and material consumption.

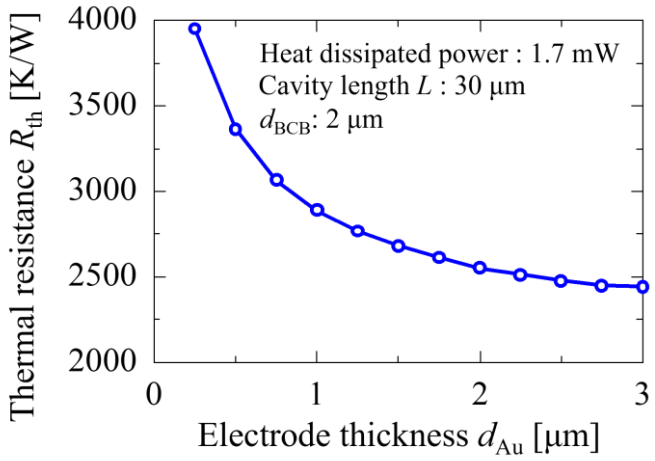
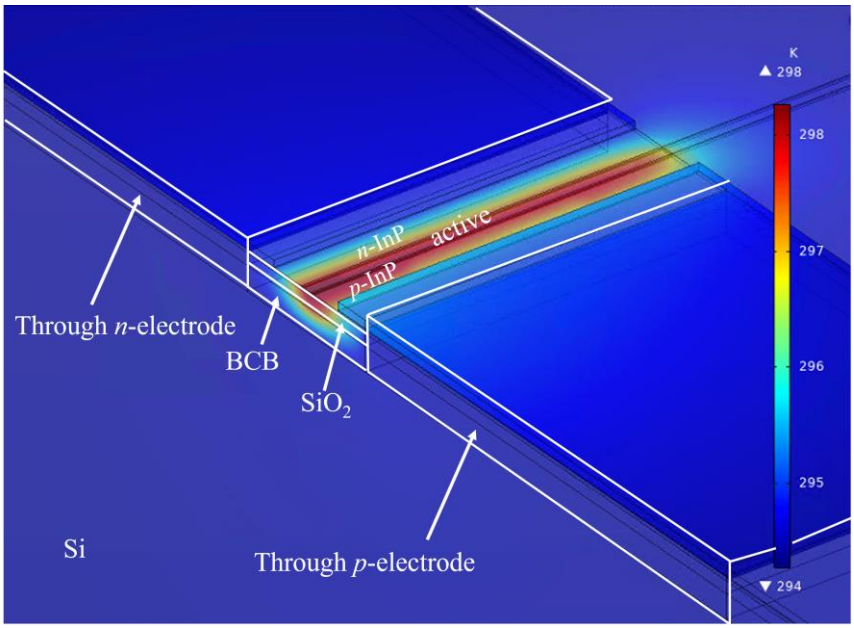


Fig. 2.16 Thermal resistance depends on electrode thickness d_{Au}.

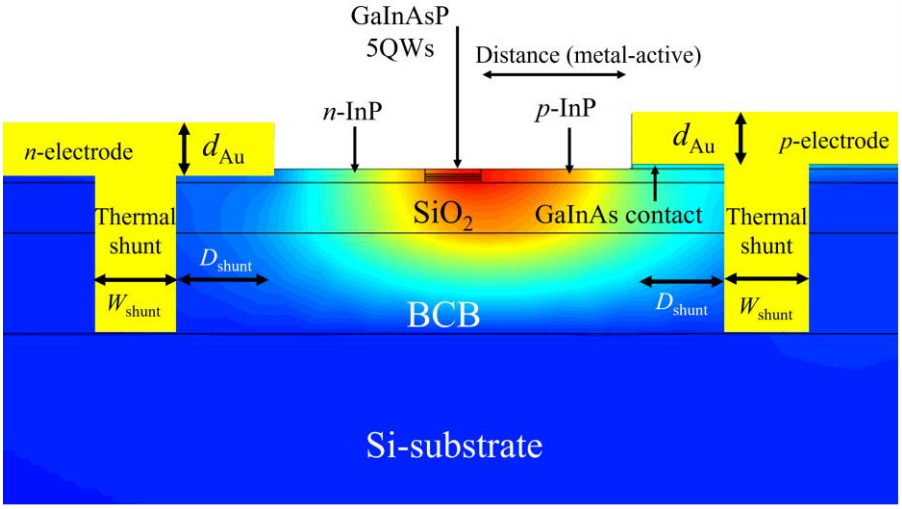
【*Thermal shunt*】

In addition to considering the electrode thickness, a effective heat evacuation of membrane laser using buried metal as a thermal shunt was proposed. In previous structure, surface electrodes could only spread heat to the air above. In this method, the surface metal can dissipate heat to the bottom Si substrate trough buried metal. Also, this method allows the high thermal conductivity metal to surround the heat source, thereby improving the lateral diffusion of heat. The buried metal can be formed after etching InP, SiO_2 and BCB layers. Figure 2.17 (a) shows a 3D view of thermal shunt structure in membrane laser on Si substrate. The buried metal penetrates deep into the Si surface. Figure 2.17 (b) shows the cross-sectional view. To determine the structure of buried metal, parameters such as thermal shunt width W_{shunt} and distance between buried metal to edge of surface electrode D_{shunt} (make sure the current flowing to the p^+-GaInAs layer) should be considered.

Figure 2.18 shows the thermal resistance dependence on electrode thickness with and without the thermal shunt structure. Compared with the structure which has 0.5-μm-thick electrode without the shunt structure, the thermal shunt structure with thick electrode can reduce the thermal resistance by 45%. When the electrode thickness both are 3 μm, the



(a)



(b)

Fig. 2.17 Thermal shunt structure using buried metal (a) 3D view (b) cross-sectional view.

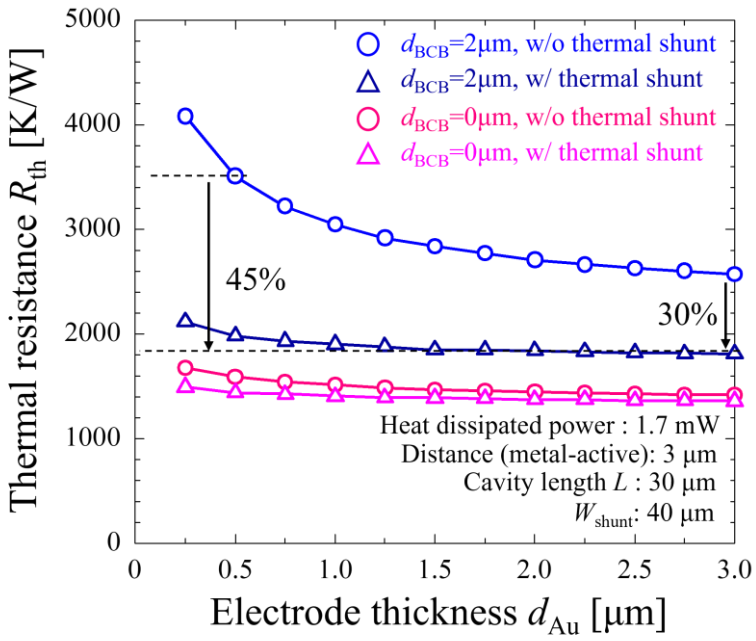


Fig. 2.18 Thermal resistance dependence on electrode thickness with and without thermal shunt structure

thermal resistance can be reduced by 30% with thermal shunt compared with that in without thermal shunt, which shows the net effect of thermal shunt. It indicates that the thermal shunt structure is an effective way to increase the heat evacuation. However, when $d_{BCB} = 0$, both thermal shunt and thick surface electrode have little improvement to the heat dissipation, which reveals that BCB plays a major role in blocking thermal diffusion, and thermal shunt structure is the method that effectivly reducing thermal resistance while remaining current BCB bonding process.

Figure 2.19 shows the structure design of thermal shunt. Figure 2.19 (a) shows the D_{shunt} dependence of thermal resistance. It indicates that the heat flow cannot be spread through upper electrode to far region, which means the buried metal must close to active region. The minimum D_{shunt} was set to 3 μm for a current tranfer path through p^+-GaInAs for reduce contact resistance in p-side thermal shunt. In n-side thermal shunt, the D_{shunt} can be 0. Figure 2.19 (b) shows the thermal resistance depends on width of thermal shunt. The result reveals the heat dissipation saturated when W_{shunt} >10 μm. Considering material consumption of metal, 10 μm W_{shunt} is suitable in fabrication.

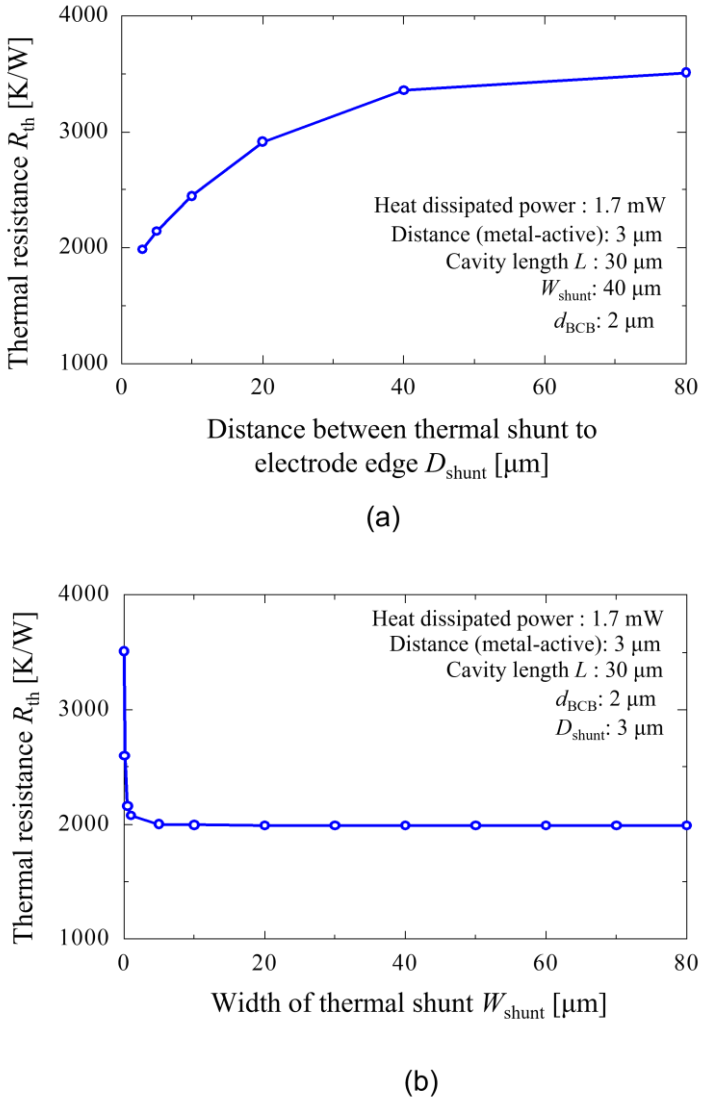


Fig. 2.19 Structure design of thermal shunt, thermal resistance depends on (a) distance between thermal shunt to electrode edge (b) width of thermal shunt.

Figure 2.20 shows the thermal resistance depends on thermal shunt depth with different D_{shunt}. Positions A-F represent the through-InP/SiO_2/BCB-via depth. F is the position of top SiO_2 while etching all the InP layers; D is the position of half SiO_2 while etching all InP and half SiO_2 layers; C is the position of top BCB while etching all InP and SiO_2 layers; B is the position of half BCB while etching all InP, SiO_2 and half BCB layers; A is the position of top S-i-substrate while etching all InP, SiO_2 and BCB layers. When depth is B to F, the buried matal thermal shunt structure assites heat to transfer to surface metal

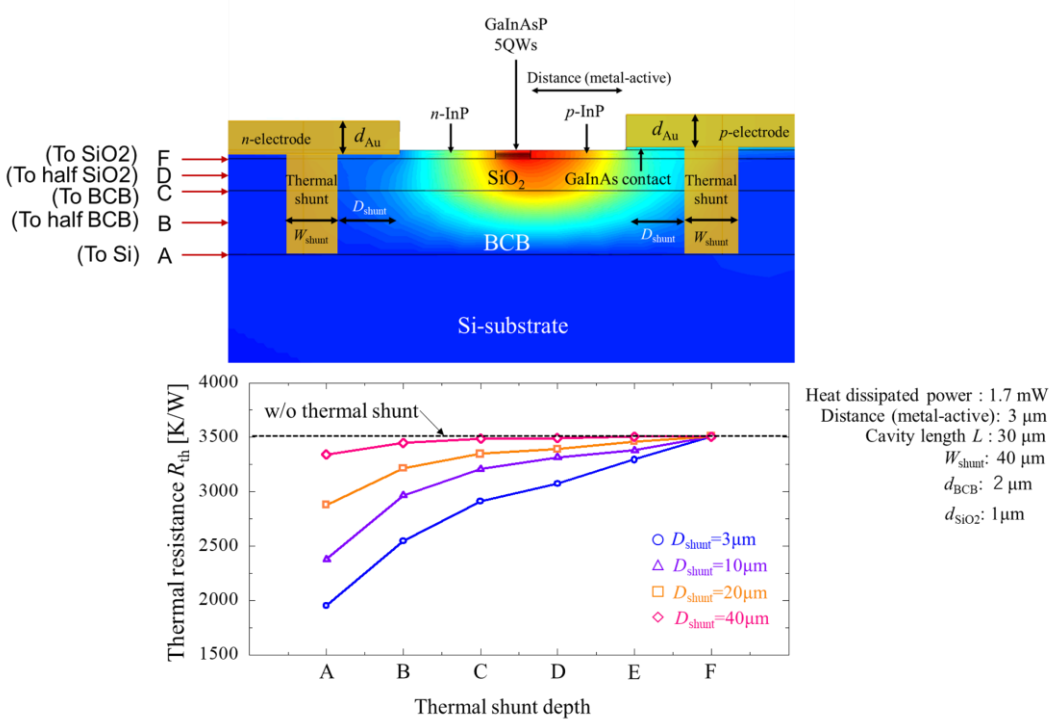


Fig. 2.20 Thermal resistance depends on thermal shunt depth with different D_{shunt}.

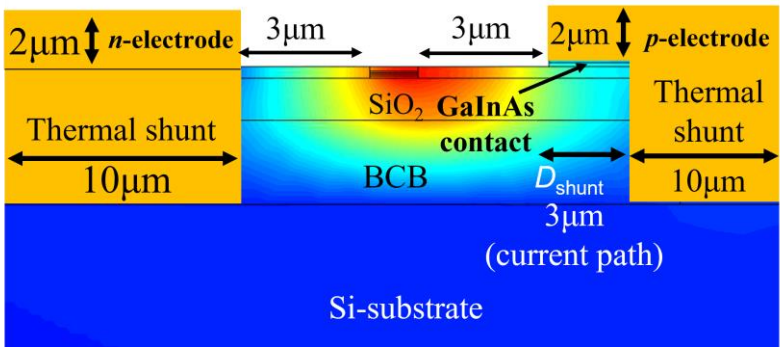


Fig. 2.21 Design of thermal shunt structure using buried metal

and exchange heat energy with air. When the position reached A, the heat can diffuse to not only surface electrode but also to bottom Si-substrate, which explain the slope of A-B increases sharply. Based on the dissusion above, the final structure of thermal shunt using buried metal is shown in Fig. 2.21.

2.3.4 Vertical direction

In vertical direction, thickness of BCB and SiO_2 should be considered. As shown in Fig. 2.14, both 2D and 3D model shows a large thermal resistance reduction by removing all BCB bonding layer. Here, Fig 2.22 shows again about thermal resistance versus BCB thickness using 3D model. By removing BCB bonding layer, thermal resistance can be reduced by 53% in calculation. Comparing with the structure dependence discussed in the previous section, BCB has the most influence to the thermal resistance due to the extrimely low thermal conductivity of 0.29 W/(K·m). However, a new direct bonding process including chemical mechanical polishing needs to be investigated.

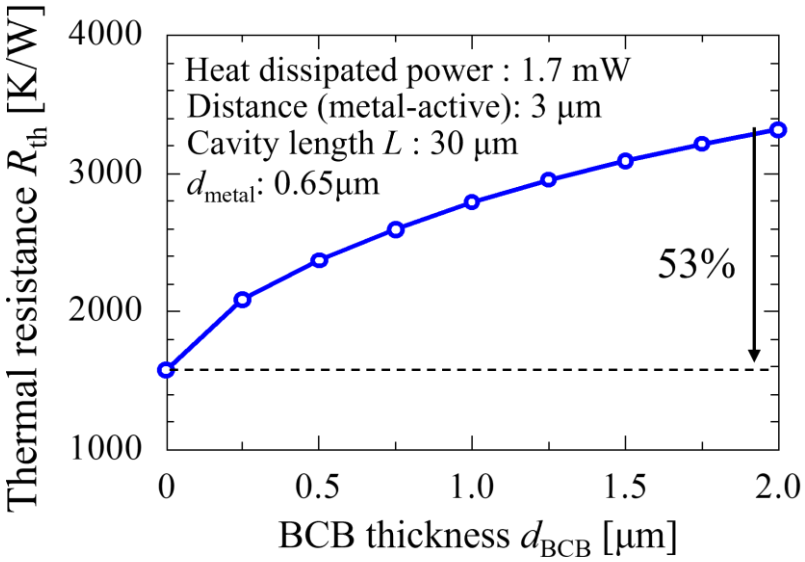


Fig. 2.22 Thermal resistance depends on BCB thickness.

Figure 2.23 (a) shows the thermal resistance depends on thickness of SiO_2. In addition to BCB, SiO_2 has the low thermal conductivity of 1.4 W/(K·m). Since the SiO_2 layer was used as the optical confinment claddingl layer, the thickness of SiO_2 should not be too thin. The optical confinment factor was calculated and shown in Fig. 2.23 (b). When the thickness is thiner than 0.3 μm, the optical mode started to leak into Si-substrate. A SiO_2 layer with 0.4 ~ 0.5-μm thick is suitable when considering both thermal resistance and optical confinment with process tolerance.

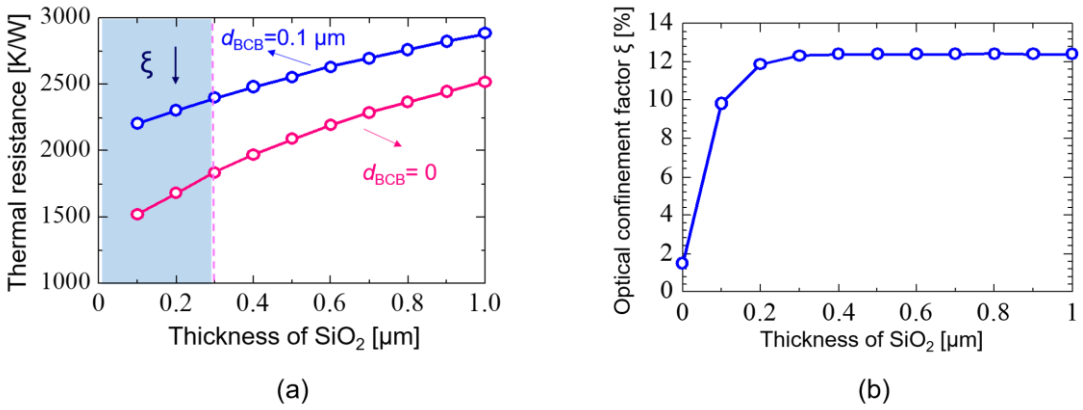


Fig. 2.23 (a) Thermal resistance versus thickness of SiO_2 (b) optical confinement factor versus thickness of SiO_2.

For achieving a lower thermal resistance, materials shown above can be considered to replace SiO_2. The thermal conductivity of Al_2O_3 is ~ 30 W/(K·m), which is larger than SiO_2, and the refractive index is ~ 1.75 which is a little larger than SiO_2. The diamond has a high thermal conductivity up to ~ 2000 W/(K·m), and the refractive index is ~ 2.4 which is larger than SiO_2. The SiC has high thermal conductivity of 490 W/(K·m), and the refractive index is as large as ~ 2.6. Although the thermal conductivity becomes larger using such materials, however, the refractive index also becomes large, which affects optical confinement in vertical direction leading to a larger threshold current.

2.4 Influence on active region temperature of Si-LSI heating

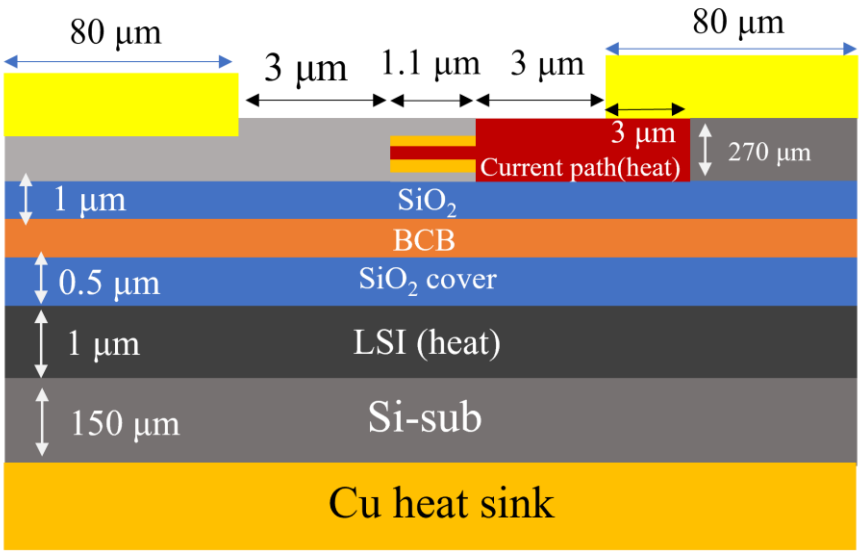


Fig. 2.24 Cross-sectional view of simulation model including a heat source of LSI on Si-substrate

The power used for calculation by the computer is finally converted to heat by the electrical resistance of the LSI circuit. In a general personal computer, a fan is turned to cool the CPU with air. If it is not cooled, it will reach 100 °C or higher. With the improvement of CPU performance, heat density has also increased. The heat generation density of the "Kyo" supercomputer CPU is approximately 15 kW/m^2, and "Tomiyake" is 80 kW/m^2 or more[26]. If it is not cooled, the temperature will wxceed 1000 °C in a blink of an eye.

The heat generated from laser was investigated in the previous section. For achieving an optical wiring on Si-LSI, the membrane photonic integrated circuits will be bonded on Si-LSI in the future. Therefore, the impact to membrane laser by heat generation from Si-LSI should be investigated. In this section, a temperautre rise of active region caused by mixed effects of Si-LSI and lsaer self-heating was studited using 2D-FEM model.

Figure 2.24 shows the 2-D model of membrane laser bonded on Si-LSI. The device layer on top Si of 1 μm, and the cover layer of SiO_2 of 0.5 μm were used in the simulation. Other parameters in simulation were the same with the calculation used in the previous sectoin. Figure 2.25 shows the temperautre of active region versus heat density of Si-LSI

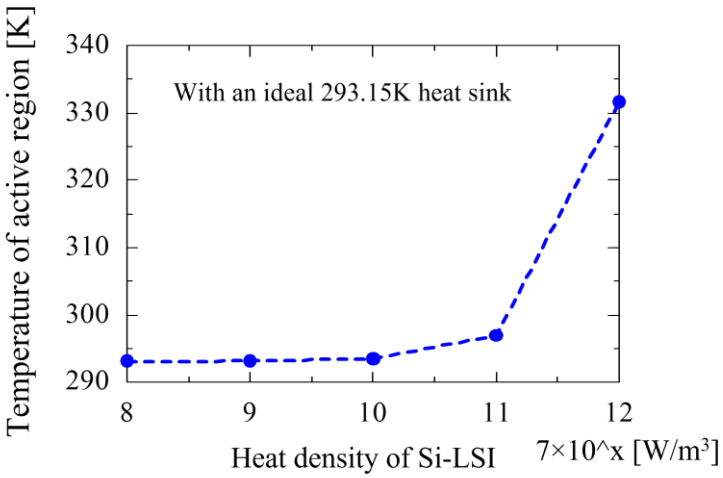


Fig. 2.25 Temperature of active region versus heat density of Si-LSI with an ideal heat sink.

with an ideal room-temperature heat sink. This calculation only considered the heat of Si-LSI. COMSOL always assumes 3D physics in calculation. Here, 2D geometry was used and COMSOL assumes 1 m per depth in the *z* direction and applies coherent simplification ot the physics. The area of Si-LSI is much larger than the area of laser, therefore, how the heat spreads from bottom to top of laser needs only to be considered. From Fig. 2.25, the temperautre of active region was controlled by heat sink when the heat density of LSI was smaller than 7×10^{10} W/m^3. Therefore, for clear understanding how temperature change occurred in active region when considering LSI and self-heating of laser, > 7×10^{10} W/m^3 heat density was used in calculation. Figure 2.26 shows the temrpeature rise of active region when only individual heat sources are considered, seperatly, with a heat sink and initail temprature of 293.15 K. When only consider the heat source of LSI (7×10^{11} W/m^3), temperature rise of active region was 3.85 K and it is not affected by thickness of BCB, which is because 1). the heat can only diffuse to upper and bottom direction, 2). 2 μm BCB is not thick enough, 3). all material was well contact in the simulation. Therefore all the component would be the same temperautre at last. When only consider the self-heating of laser, the results was shown in orange line. This result was correspond to Fig. 2.26. And the temperautre rise was affected by BCB thickness because the heat can diffuse to lateral and upper direction. Finally, when

consider all heat source, the results were shown in red line of Fig. 2.26. The relation between this three group can be summaried as Eq. (2.48)

$$\Delta T[\mathrm{Q(LSI)}] + \Delta T[\mathrm{Q(InP + act)}] = \Delta T[\mathrm{Q(LSI) + Q(InP + act)}] \tag{2.48}$$

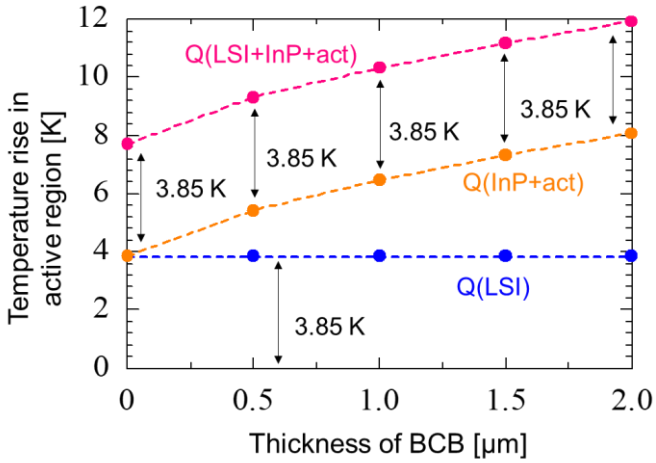


Fig. 2.26 Temperature rise of active region when considering individual heat sources and mixed effect.

From the results discussed using the model above, the heat of LSI affects the ambient temperature of laser operation with heat sink.

2.5 Thermal characteristic of membrane laser

In this section, thermal characteristics of membrane laser was theoretically analyzed. The thermal resistance dependence of threhsold current, output power, and relaxation resonance frequency would be introduced in the following sub-section.

【***Threshold current***】

The mechanism of threshold change is a little complicated. As the temperature rises, the electrons (and holes) injected into the band become thermally distributed to high energies, so the number of electrons / holes of a specific energy that can contribute to lasing is effectively reduced and the gain is reduced. To compensate for the reduced gain, the carrier density must be further increased. In other words, the threshold current rises. A few things happen as the threshold rises. As the carrier density increases, the internal loss of the cavity increases. It is mainly due to scattering to a spin orbit band, and is a mechanism of light absorption called Inter Valence Band Absorption (IVBA). This raises the threshold gain (balanced with the loss) required for oscillation. However, since the gain is not linear with respect to the carrier density and actually saturates at a high carrier density, there is a limit to the increase in the gain, and a higher carrier density is required. In addition, long wavelength band lasers have a strong Auger effect, which is a non-radiative recombination process, which is proportional to the cube of the carrier density. This does not increase the threshold carrier density, but consumes extra current, resulting in Joule heat and reducing gain. This is also a negative feedback. In fact, even if the temperature is kept constant on the bottom surface using thermoelectric controller (TEC), the temperature of active layer is higher than it due to thermal resistance. This temperature difference is as high as 50 °C at high bias current values near the peak of the *I-L* curve. Therefore, at temperatures high enough to stop lasing, the contribution of Joule heat is considerable. The combination of these three, 1. decrease in gain, 2. increase in internal loss, and 3. increase in non-radiative process, causes the threshold to increase exponentially with temperature. The expression of threshold current can be expressed as

Eq. (2.49)[27].

$$I_{\mathrm{th}}=\frac{qVCN_{tr}^{3}}{\eta_{\mathrm{i}}}\mathrm{e}^{3(\langle\alpha_{\mathrm{i}}\rangle+\alpha_{\mathrm{m}})/\xi g_0} \tag{2.49}$$

where, V is the active region volume, C is the Auger coeffieient, N_{tr} is the teansparent carrier density, $\langle\alpha_i\rangle$ is the interal loss of cavity, α_m is the mirror loss, ξ is the optical confinment factor, and g_0 is the gain coefficient. Based on the discussion above, N_{tr}, g_0, and $\langle\alpha_i\rangle$ have a significant temperature dependence. These observations suggest that the threshold current and external can be approximately modeled by

$$I_{th} = I_{th0}\exp\left(\frac{T}{T_0}\right) \tag{2.50}$$

where, T is the temperature in active region, I_{th0} is the fitting coefficient, and it can be found by making a fitting in exponential function using measured data. T_0 is the characteristic temperature. Up to about 50-70 °C, T_0 can be expressed by a constant formula, but at higher temperatures, T_0 itself deteriorates (decreases) further, and lasing itself becomes impossible. In this region, it is understood that the major cause is carrier overflow, in which carriers thermally overflow from the active layer (quantum well) to the layer around the clad, SCH layer, barrier layer, etc. due to temperature rise. The same model can be used for external quantum differential efficiency.

$$\eta_d = \eta_{d0}\exp\left(-\frac{T}{T_1}\right) \tag{2.51}$$

where, T_1 is generally two or three times larger than T_0. In GaInAsP/InP 1.55μm long wavelength membrane FP, DFB or DR laser, measured values tend to fall in the 50-70 K. Here, the mode-gain alignment issues was not considered in the calculation model and experimental data. The lsing occurred at the gain peak was assumed. In a Bragg wavelength detuned cavity, the lasing mode can be forced to away from the wavelength where the gain is a maximum. Thus, such lasers can be designed to have anomolous temperautre behavior because of the different shift rates versus tmeprature between cavity mode and gain peak. In this design, it is possible to make the threshold current go down with increasing temperature at first. In practice, it is more interested in the relative changes in threshold current and external differential quantum efficiency as the

temperature changes rather than the absolute values. More useful expressions are given as: $(T_\beta > T_\alpha)$

$$I_{th\beta} = I_{th\alpha}\exp\left(\frac{T_\beta - T_\alpha}{T_0}\right) \tag{2.52}$$

$$\eta_{d\beta} = \eta_{d\alpha}\exp\left(-\frac{T_\beta - T_\alpha}{T_1}\right) \tag{2.53}$$

For example, the threshold current in continuous-wave (CW) condition can be estimated by using the Eq. (2.52) due to self-heating. Some iterate is needed[27]. At threhold, the ouput power from the laser can be neglected, therefore, the dissipated power is equal to the input power,

$$P_d = P_{in} = I_{th}^2 \cdot R_s + I_{th}^2 \cdot V_d \tag{2.54}$$

$$\Delta T = P_d \cdot R_{th} \tag{2.55}$$

$$I'_{th} = I_{th} \cdot \exp\left(\frac{\Delta T}{T_0}\right) \tag{2.56}$$

R_{th} is the thermal esistahce, I_{th} is the pulse threshold current. I'_{th} is the calculated CW threshold current. Then, using I'_{th} to calculate the dissipated power and repeat the process. After some iterations, the I'_{th} converges.

【*Output power*】

The output power without considering the self-heating in continuous-wave condition can be expressed as Eq. (2.57) and (2.58).

$$P_{out} = \eta_d \eta_{spon} \mathrm{B} E_g I \quad (\mathrm{I} < I_{th}) \tag{2.57}$$

$$P_{out} = \eta_d \eta_{spon} \mathrm{B} E_g I_{th} + \eta_d E_g (I - I_{th}) \quad (\mathrm{I} \geq I_{th}) \tag{2.58}$$

where, η_{d} is the external differential quantum efficiency, η_{spon} is the spontaneous emission efficiency and B is the spontaneous emission coefficient. Since this research ignores spontaneous emission, the output power becomes

$$P_{out} = 0 \quad (\mathrm{I} < I_{th}) \tag{2.59}$$

$$P_{out} = \eta_d E_g (I - I_{th}) \quad (\mathrm{I} \geq I_{th}) \tag{2.60}$$

Substituting Eq. (2.52) and (2.53) into (2.60), and note that $\Delta T = R_{th}P_d$, the output power considering temperature dependence will be:

$$P_{out} = 0 \quad (\mathrm{I} < I_{th}) \tag{2.61}$$

$$P_{out} = \eta_d \exp\left(-\frac{R_{th}P_d}{T_1}\right)E_g\left(I - I_{th}\exp\left(\frac{R_{th}P_d}{T_0}\right)\right) \quad (\mathrm{I} \geq I_{th}) \tag{2.62}$$

To calculate the output power for bias current of I at an environment temperature of T, the following can be carried out: assuming that the output power is negligible, the dissipated power, the temperature increase, and the increase in the threshold current and the decrease in the differential efficiency can be calculated. At that point, the output power can be computed. To iterate, the output power value was removed from heat dissipated power as the new heat dissipated power and repeat the process. After a couple of steps, the process converges[27].

Round(1):

$$P_d(1) = P_{in} = I^2 \cdot R_s + I \cdot V_d \tag{2.63}$$

$$\Delta T(1) = P_d 1 \cdot R_{th} \tag{2.64}$$

$$I'_{th}(1) = I_{th} \cdot \exp\left(\frac{\Delta T(1)}{T_0}\right) \tag{2.65}$$

$$\eta'_d(1) = \eta_d \cdot \exp\left(\frac{-\Delta T(1)}{T_1}\right) \tag{2.66}$$

$$P_{out}(1) = E_g\eta'_d(1)(I - I'_{th}) \tag{2.67}$$

Round(2):

$$P_d(2) = P_d(1) - P_{out}(1) \tag{2.68}$$

$$\Delta T(2) = P_d(2) \cdot R_{th} \tag{2.69}$$

$$I'_{th}(2) = I_{th} \cdot \exp\left(\frac{\Delta T(2)}{T_0}\right) \tag{2.70}$$

$$\eta'_d(2) = \eta_d \cdot \exp\left(\frac{-\Delta T(2)}{T_1}\right) \tag{2.71}$$

$$P_{out}(2) = E_g\eta'_d(2)(I - I'_{th}) \tag{2.72}$$

…

Round(N): $$P_d(N) = P_d(N-1) - P_{out}(N-1) \tag{2.73}$$

$$\Delta T(N) = P_d(N) \cdot R_{th} \tag{2.74}$$

$$I'_{th}(\mathrm{N}) = I_{th} \cdot \exp\left(\frac{\Delta T(N)}{T_0}\right) \tag{2.75}$$

$$\eta'_d(\mathrm{N}) = \eta_d \cdot \exp\left(\frac{-\Delta T(N)}{T_1}\right) \tag{2.76}$$

$$P_{out}(N) = E_g \eta'_d(N)(I - I'_{th}) \tag{2.77}$$

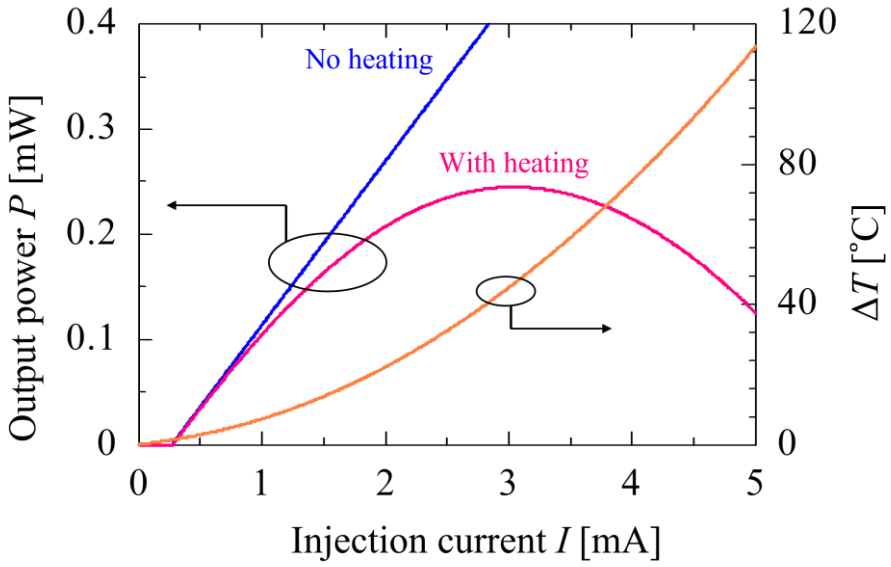


Fig. 2.27 Illustration of membrane laser heating as a function of bias current, *I-L* curve with thermal roll off and ideal *I-L* curve.

Table 2.5 Parameters used in *I-L* calculation

Parameters	**value**
Pulse threshold current [mA]	0.2
η_d	0.2
Thermal resistance R_{th} [K/W]	5000
Differential resistance R [Ω]	750
T_0 [K]	50
T_1 [K]	100
E_g [eV]	0.8
V_d [V]	0.82

Figure 2.27 shows the calculated *I-L* curve with and without self-heating and tempreature rise in active region. The parameters used in calculation are shown in Table 2.5. The membrane laser has a high thermal resistance by using BCB bonding. However, the self-heating is not large around threshold thanks to the low threshold current. The temperature rise in active region increased quickly because of the high thermal resistance and high differential resistance. Hence, the optical saturation current was low, which limits the output power. Figure 2.28 shows the calculated *I-L* curve of membrane laser with different thermal resistance at room temperature. The optical saturated current can be expanded up to 10 mA when thermal resistance was lower than 500 K/W, and the output power can be enhanced up to 1 mW. This can be achieved by adjust the laser structure for high heat dissipation, such as removing BCB bonding layer, shorten distances between electrodes and active region, enhance the thickness of electrodes and increasing the cavity length a little from 30 μm to 70~80 μm while keeping a low threshold current.

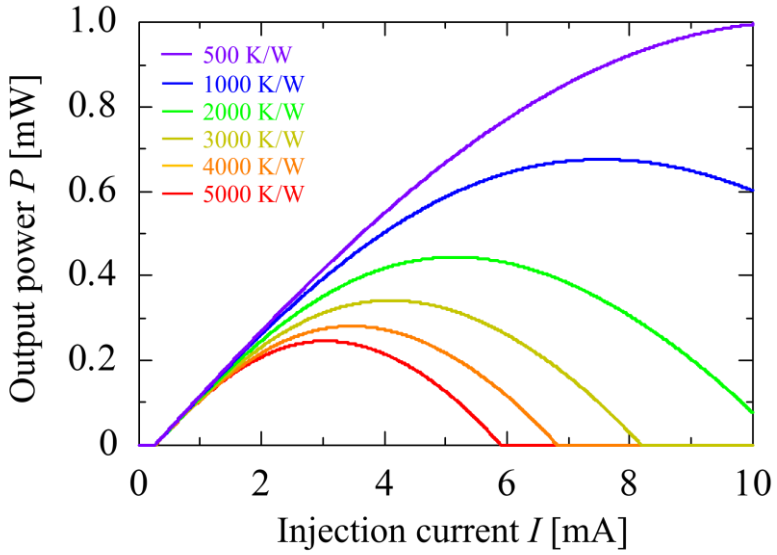


Fig. 2.28 Calculated *I-L* curve of membrane laser with different thermal resistance at room-temperature.

【*Relaxation ocsillation frequency*】

In directly modulation of semiconductor laser, relaxation ocsillation frequency (f_R) aways limits the modulation bandwidth. The expression of f_R is shown in Eq. (2.78).

$$f_R = \frac{1}{2\pi}\sqrt{\frac{\xi v_g a}{qV}\eta_i(I - I_{th})} = \frac{1}{2\pi}\sqrt{\frac{\xi v_g a}{qV}\eta_i} \cdot \sqrt{(I - I_{th})} \tag{2.78}$$

where, ξ is the optical confinment factor, v_g is the group valocity, a is the differential gain, η_i is the injection effieiency, I is the bias current, and I_{th} is the threshold current. As the laser has a low thermal resistance, the optical saturated current is extended. And for a fixed temeprature rise in active region, the low thermal resistance laser can have a larger bias current, which shows a higher c, and 3-dB bandwidth. Figure 2.29 shows the f_R versus square root of (I-I_{th}) when considering self-heating. The modulation efficiency

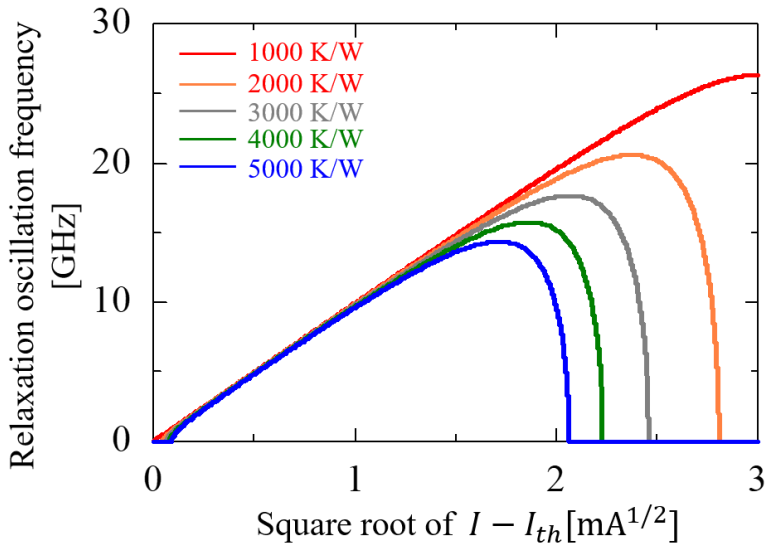


Fig. 2.29 Relaxation oscillation frequency as the function of square root of the bias current above threshold

of 10 GHz/mA$^{1/2}$ was assumed in the calculation. The c increased linearly in a certain range and then growth will be flat due to damping. Finally, droping because of heat. When do not consider heat, f_R will be constant with the current increasing after damping. The maximum f_R was extended by 32% when thermal resistance becomes half than before.

Figure 2.30 shows the estimation of f_R in membrane DFB laser with 80 μm cavity

length and 2.16 μm^3 active region volume[28]. The thermal resistance of 1400 K/W was estimated in calculation. The f_R increased linearly until injection current of 1.48 mA corrsponding the temprature rise of 3.9 K. Therefore, assuming the f_R increases linearly until the temperature rise is 3.9 K. When removing the BCB bonding layer, thermal resistance can be reduced to about 600 K/W in calculation. Thus, bias current can be extended to 2.45 mA with the same temperature rise. Figure 2.30 (b) shows the f_R enhancement. 41% increment can be obtained in the linear range.

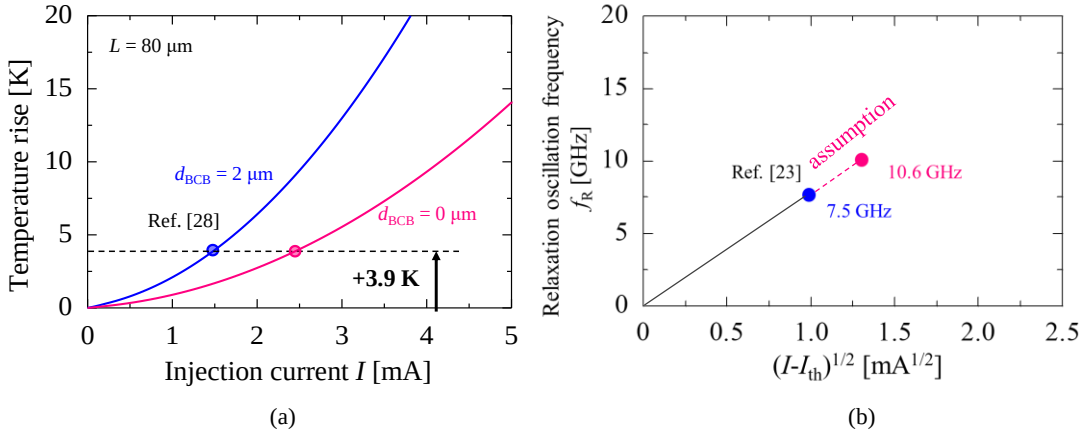


Fig. 2.30 (a) Temperature rise in active region versus injection current, (b) relaxation oscillation frequency as the function of square root of the bias current above threshold

2.6 Conclusion

In this chapter, thermal characteristic of memrbane laser was discussed. First, the power and thermal resistance of membrane laser at 85 ºC was investigated. Next, a 3D model thermal model of membrane laser bonded on Si substrate on Cu heat sink was constructeds. The thermal resistance dependece of device structure was investigated. Three directions heat transfer were coonsidered. In cavity length, heat can spread to waveguide region, and with the cavith length increasing, the area of heat transfer from heat source to heat sink increased leading to a lower thermal resistance. In lateral deirection, distance between electrode to active region affects the heat transfer distance from heat source to electrode. This distance needs to be as short as possible while maintaining a low waveguide loss in active region. A structure of thermal shunt using buried metal through InP/SiO_2/BCB via was studied. The thermal resistance can be reduced by 45% in 2-μm-thick BCB bonding process, which shows an effective heat dissipation. However, this structure has little effect in a direct bonded membrane laser. In vertical direction, the influence of thichkness of SiO_2 and BCB bonding layers to thermal resistance was discussed. 0.5-μm-thick SiO_2 was needed for optical confinment and process tolerance. Reducing BCB layer from 2 to 0 μm would reduce the thermal resistance by 53% while a new direct bonding with surface flatten process need to be established.

After disscusing the thermal resistance of membrane laser, how heat from Si-LSI affects temperature of active region was studied. A 2D model including 1-μm-thick LSI heat source and 0.5-μm-thick SiO_2 cover layer was used in calculation. The results show that the heat of LSI affects the ambient temperature of laser with heat sink, which means the tempreature rise of mixed effect of LSI and self-heating was the same of that individual heat source operated respectively. Finally, laser characteristics of threshold current, output power and relaxation oscillation frequency were introduced when considering self-heating. A laser with lower thermal resistance has a high optical saturation current, high power and high modulation bandwidth.

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Chapter 3

Investigation of wafer bonding technology for membrane platform on Si

3.1 Introduction

Chapter 1 has introduced the general wafer bonding technology and the III-V compound semiconductor on Si integration using wafer bonding. In the membrane platform, as SiO_2 is chosen as a cladding layer for optical confinement, the wafer bonding technology is necessary in membrane structure integrated on another substrate. Section 3.2 described previous works on wafer bonding for fabrication of laser including BCB bonding, hydrophilic bonding and N_2 plasma activated bonding. For reducing thermal resistance while maintaining mature BCB bonding process, ultra-thin BCB bonding method is described in section 3.3. For large scale and further reducing thermal resistance, two direct bonding methods was investigated. One is hydrophobic plasma activated bonding using O_2 plasma, another one is surface activated bonding in room temperature assisted by sputtered amorphas silicon (a-Si), which will both be demonstrated in section 3.4.

3.2 Previous research of wafer bonding

Various bonding process have been studied in our laboratory for fabricating laser such as hydrophilic bonding, BCB bonding, plasma activated bonding and surface activated bonding based on fast atom beam at room temperature. In this section, these methods will be reviewed.

【 *Hydrophilic bonding for membrane laser on SOI* 】

In 2007, the membrane DFB laser with wirelike active region on SOI substrate was demonstrated. The membrane structure was formed using air and buried 2 μm SiO_2 by hydrophilic direct bonding[1]. The bonding process was as follow. First the GaInAsP/InP wafer was cleaned using HCl:CH_3COOH solution, the surface turned to hydrophilic. Cleaning for SOI started with organic wafer cleaning (Acetone and Methanol), then SC-I for 10 min, 50% HF, SC-II for 10 min was followed. To remove the natural oxide layer on the surface of SOI, BHF was used and the surface become hydrophobic, then SOI was treated with H_2SO_4:H_2O_2:H_2O solution at 50 °C to make the surface hydrophilic. Two hydrophilic surfaces were taken into contact in DI wafer in room temperature under the

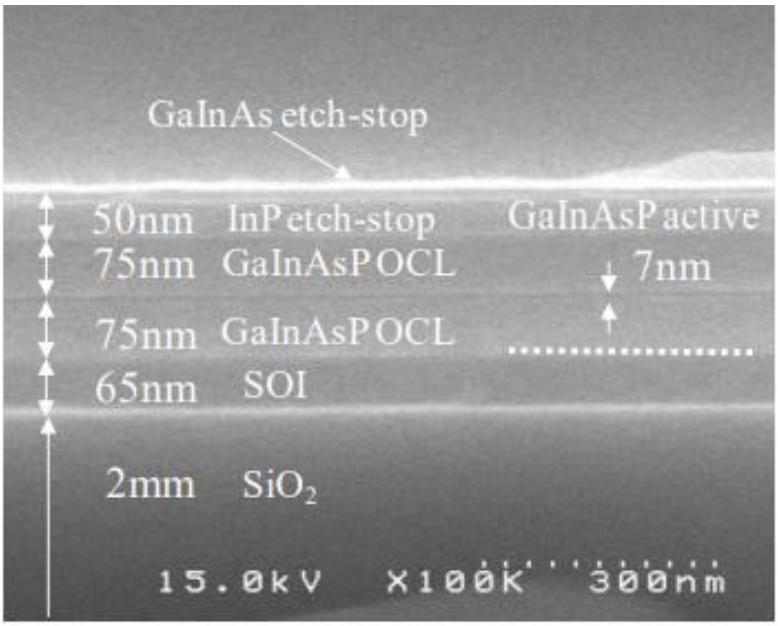


Fig. 3.1 SEM image of GaInAsP/InP membrane laser on SOI waveguide[2].

pressure of near 4 kg/cm^2 and dried by N_2. Then, wafers were put into H_2 furnace for 60 min static heating. Previous works showed the annealing temperature should be lower than 500 °C for a good crystalline quality[2], and a rapid heating up to 500 °C may let the InP broken. Figure 3.1 shows the SEM image of the bonding interface at a heating temperature of 450 °C. In the device fabrication, 250 °C was used. This method is the most common and the earliest method used in our laboratory. The merits of this method are that it is simple to operate and does not need specific machine. However, the anneal temperature is high and the loading uniformity in annealing furnace is hard to guarantee.

【 *BCB bonding for membrane laser on Si* 】

Around 2012, the BCB bonded GaInAsP wire waveguide for membrane photonic circuits was demonstrated[3]. The membrane structure using air and SiO_2 was formed by BCB bonding on Si. The thickness of BCB was 6 μm when BCB bonding was first used in membrane laser process. And BCB was spin coated on both host substrate and process wafer (Fig. 3.2). However, BCB is the material with high viscosity, so edge beat around wafer appears prominently, which inhibits the adhesion of two wafers. Therefore, new spin coating method that only coating on host substrate wafer was proposed and reducing the thickness of BCB from 6 μm to 2 μm, which also reduced the thermal resistance of

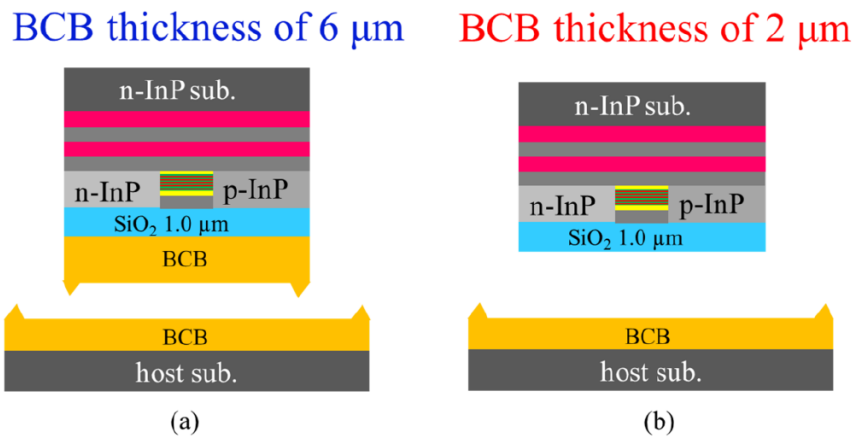


Fig. 3.2 Comparison of BCB bonding process[4]

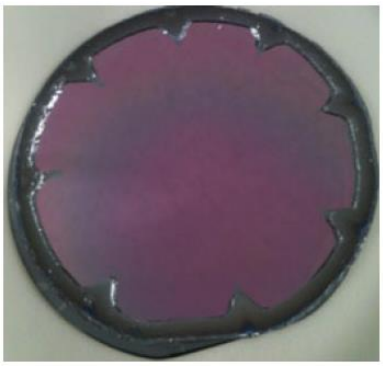


Fig. 3.3 2 μm BCB bonding wafer after selective wet-etching[3]

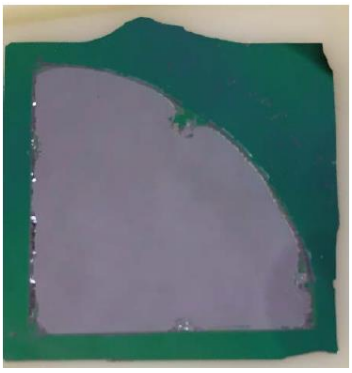
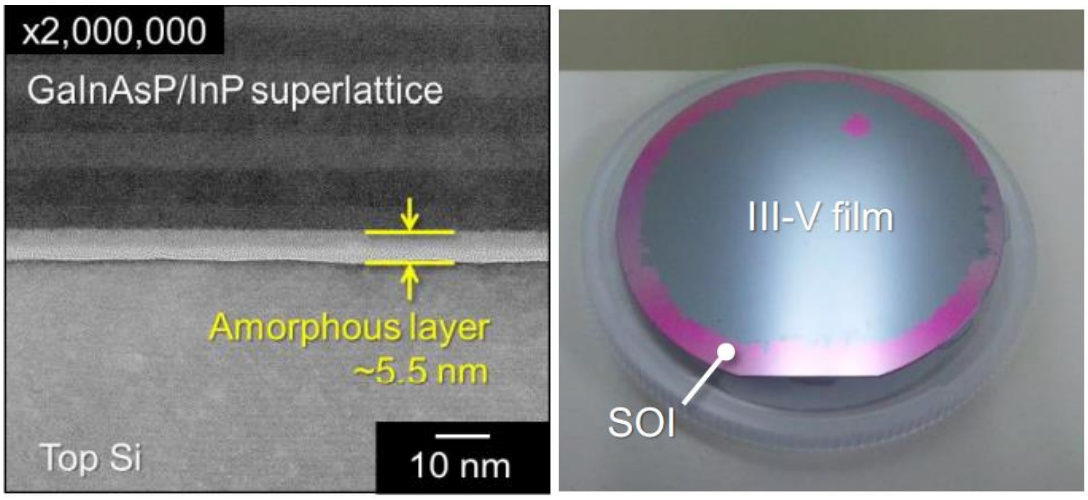


Fig. 3.4 0.5 μm BCB bonding wafer after selective wet-etching[5]

membrane laser. After finding the relation between bonding strength and pre-cure time, the pre-cure condition was selected in 210 °C N_2 oven for 40 min. The hard baking condition is 250 °C in N_2 oven for 60 min. The wafer after bonding and selective wet-etching of the InP substrate and etch-stop-layers was shown in Fig. 3.3. Next, for further reducing the thermal resistance, 0.5 μm thinner BCB bonding process was proposed. In this process, only the pre-cure time was changed from 40 min to 10 min, and the wafer after bonding and thinning process was shown in Fig. 3.4. After several times of epitaxial regrowth, the surface of processed III-V wafer is uneven. 2-μm-thick BCB bonding is the most general process of membrane laser fabrication in our lab in the next 10 years. The merit is the low requirement for surface roughness. However, it needs high temperature annealing for hard-bake of BCB, which takes a long time and remains thermal stress like hydrophilic bonding.

【 *Plasma activated bonding for hybrid laser on Si* 】

A GaInAsP/Si hybrid laser was fabricated by N_2 plasma activated bonding in our laboratory in 2013[6]. The bonding started with the typical wet cleaning process and followed with Megasonic wafer cleaning (the system will be introduced in 3.3.2 in detail). Then wafers were loaded into a vacuum chamber and irradiated by RF plasma at 500 W for 10 sec in a N_2 atmosphere at 120 Pa room temperature chamber. Next, chamber was evacuated to 10^{-4} Pa to sustain the activation state, and two wafers were temporarily



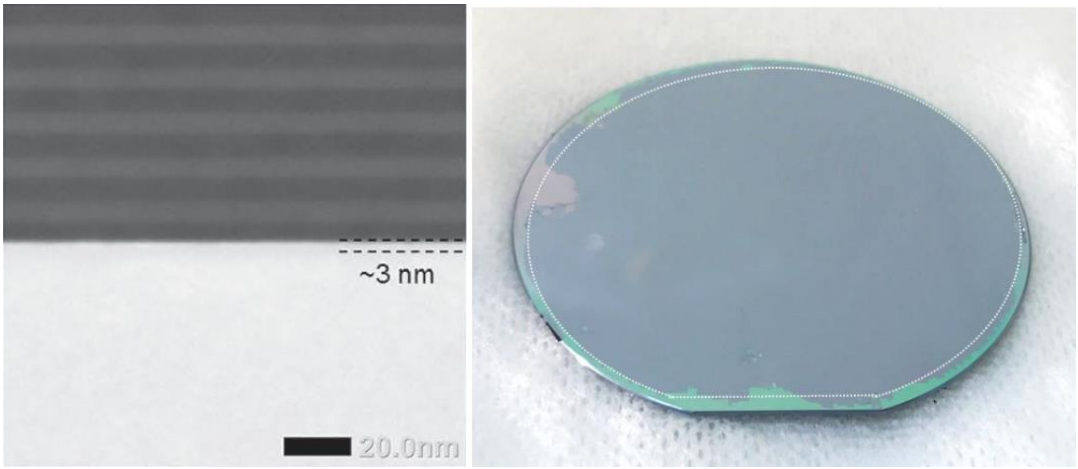
(a) (b)

Fig. 3.5 N_2 plasma activated bonding (a) bonding interface (b) bonding area[7]

bonded for 180 sec under the pressure of 50 kgf. Finally, to further strengthen the bond, wafers were held together under the pressure of 50 kgf and the chamber temperature was increased to 150 °C over 2 hours. This bonding method is a hydrophobic bonding. Ar and O_2 plasma were also investigated for InP-Si bonding in our previous works[2]. The Ar gas will cause a large surface roughness and O_2 plasma will introduce the OH^- for oxidation, which has a bad influence on low temperature bonding. The bonding strength is as high as 2 MPa in wafer scale. The SEM image and bonding area are shown in Fig. 3.5. The amorphous layer was caused during plasma irradiation. The merit of this method is the annealing temperature was reduced to 150 °C while keeping a large bonding strength. However, the natural cooling in vacuum after annealing using the specific bonding machine caused a long process time, usually, 12 hours is needed.

【 *Surface Activated Bonding for hybrid laser on Si* 】

Our laboratory studies surface activated bonding at room temperature using fast atom beam since 2017. Some achievements have been obtained in the previous works[8]. We experimented Ar, Ne, Xe and Kr gases in the irradiation condition. As a result, Xe has the minimum damage to the quantum well layer in different depth. Then, Ar for Si and Xe for InP was used in Si/InP bonding for hybrid laser on Si. The bonding also started with the typical cleaning process followed by Meganonic cleaning. Then wafers were loaded into the chamber and irradiated by fast atom beam in different gas species, current and time condition. Finally, two wafers were brought into contact at the room temperature for 200 kgf and 180 sec. During this experiment, we also measured the surface roughness after irradiation and PL intensity to the GaInAs/InP wafer. Over 2.0 MPa bonding strength was obtained in 2-inch InP /Si wafer. For III-V hybrid integration, wafer thinning experiment was followed. Figure 3.6 shows the bonding interface of InP-Si and III-V film bonding area on a bare SOI wafer. The amorphas layer was due to the FAB irradiation, and a large bonding area was obtained. The merit of this method is that there is no need to anneal after bonding and which also reduce the process time. While this method needs a specific machine to support a high vacuum chamber and FAB gun.



(a) (b)

Fig. 3.6 Surface activated bonding (a) InP-Si bonding interface[8] (b) bonding area[9]

3.3 Wafer bonding for low thermal resistance membrane laser

We first used 6-μm-thick BCB as the bonding layer, however the room temperature continuous wave operation of the current injection type membrane laser could not be achieved, because the edge beat strongly influenced the fabrication and also the thermal resistance is high. This is due to the very high thermal resistance of membrane laser. After that we tried to spin coated BCB on one side of Si substrate only and reduced thickness of BCB to 2-μm with an optimized bonding process. This time the room temperature continuous wave operation of membrane laser was achieved[10]. For higher temperature operation, 0.5-μm-thick BCB bonding process was investigated. In 3.3.1 section, 0.1-μm-thick ultra-thin BCB bonding process would be discussed. This is the most effective way to minimize thermal resistance while keeping the original process unchanged. However, if the surface level difference of the substrate is larger than the thickness of the BCB film, it will be a very challenging problem that cannot be ignored. If direct bonding is used, the thermal resistance will be greatly reduced, but in this way, the process that has been built before will no longer be applicable, and a new process system including chemical mechanical polishing (CMP) must be introduced. The discussion about these would be shown in section 3.3.2 and 3.3.3. Section 3.3.2 shows a O_2 plasma activated bonding (PAB) based on our previous work about N_2 PAB. The bonding interface was imagined as SiO_2-SiO_2. Section 3.3.3 shows a modified surface activated bonding using a-Si nanofilm at room temperature. The bonding interface was transformed from SiO_2-Si to Si-Si.

3.3.1 Ultra-thin BCB bonding

The BCB that we used is CYCLOTENE 3022-35. Its viscosity is not very high (14 cSt@25℃) in the CYCLOTENE 3000 series, and the thickness range is 1.0~2.4 μm[11]. In our group, Delta-80 RC was used to spin coat BCB into 2-inch Si wafer. Fig. 3.8 shows the photograph of the equipment appearance. And the spin coating condition is shown in Table 3.1. The Delta-80 RC (Fig. 3.7) spin coating system has a cover structure in the rotating table which can minimize the turbulent air flow due to substrate rotation, so it is possible to apply a large area uniformly. For further reducing the thickness of BCB layer, thinner should be mixed in undiluted BCB solution. BCB content in the solution has more impact on the film thickness than the rotation speed[12]. For a 1:1 thinner : BCB solution (50% BCB mass content), average thicknesses achieved with 0.5 μm under the Table 3.1 condition. So, we used only the thinner : BCB solution ratio as a variable parameter to achieve the desired bonding layer thickness.

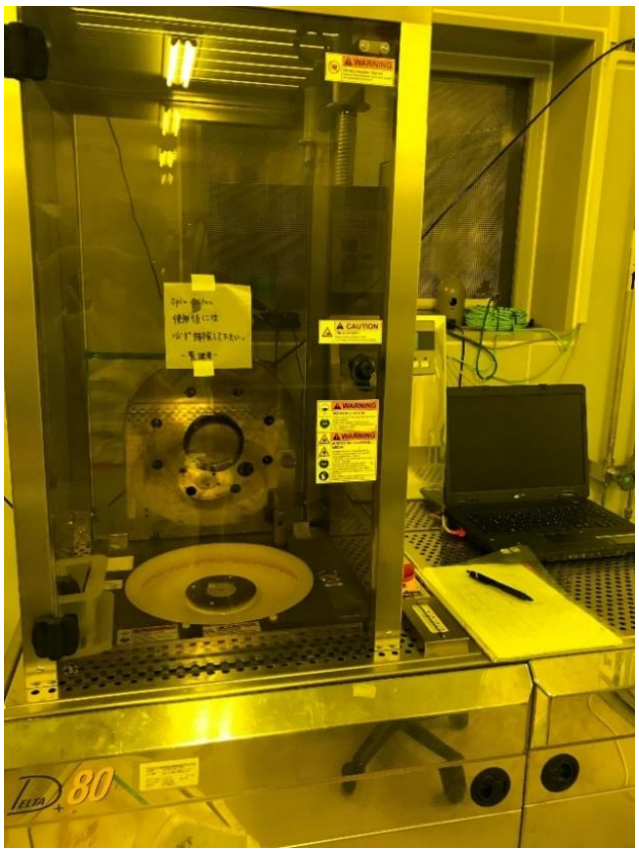


Fig. 3.7 Delta-80 RC spin coater (SUSS Micro Tec)

Table 3.1 Spin coating condition of Delta-80 for BCB (CYCLOTENE 3022-25)

Step	Rotation speed [rpm]	Acceleration [rpm/s]	Cover	Time [sec]
1	0	1000	Close	7
2	500	1000	Close	5
3	1000	1000	Close	16
4	1900	5000	Close	1
5	0	5000	Close	2
6	0	1000	open	6
7	1000	1000	open	180
8	0	1500	open	0

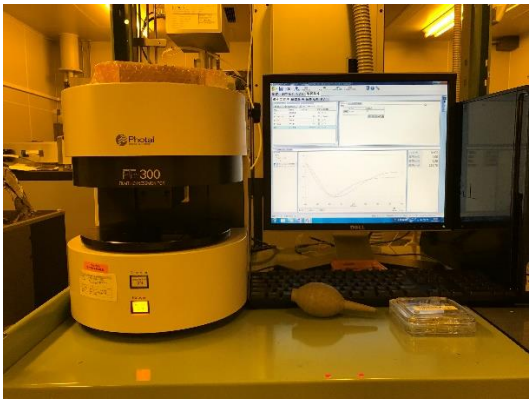


Fig. 3.8 Film thickness monitor FE-300

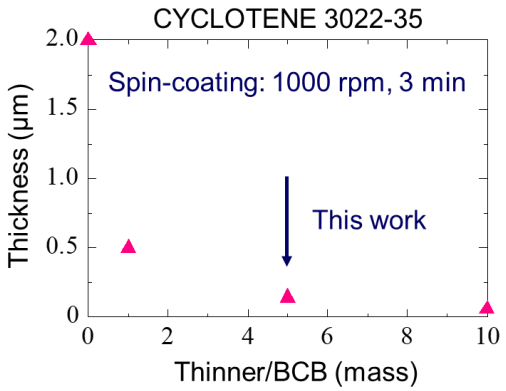


Fig. 3.9 BCB thickness dependence on the thinner : BCB solution ratio

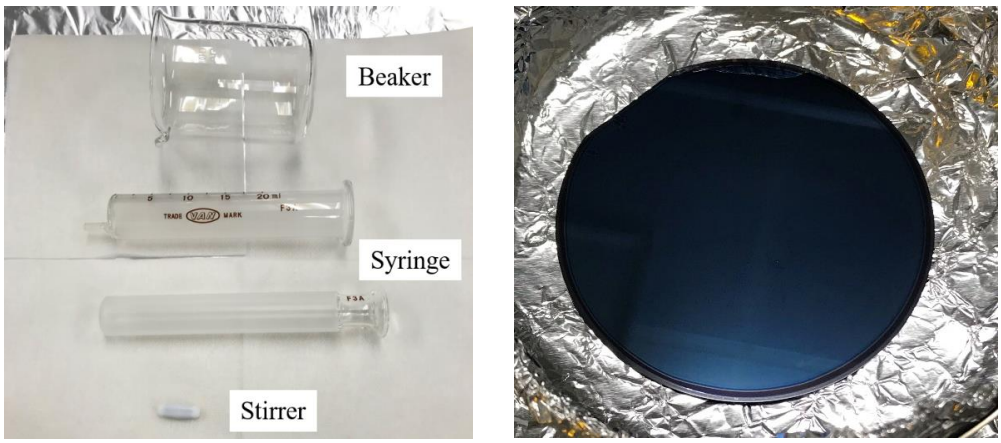


Fig. 3.10 140 nm spin coated BCB

To measure this thickness, FILMTHICKNESSMONITOR FE-300 (Photal OTSUKA ELECTRONICS) was used. This film thickness monitor is based on comparison of the measured reflectance with the reflectivity of the material in the database in a certain wavelength range to give the matching degree of the input film thickness by the least squares method. The higher the match degree, the closer to the true value. Fig 3.8 shows the appearance of this machine. Fig 3.9 shows the BCB thickness dependence on the thinner : BCB solution ratio. In this research, 100 nm BCB layer (thinner : BCB=5:1) was used.

The process of ultra-thin BCB bonding starts with the cleaning process. Preparing the beaker, syringe, and stirrer (Fig. 3.10), and putting them in the acetone (130 °C) in 15 min, then ultrasonic cleaning 15 min was done. After that, 30 min baking in an oven will be carried out. When the cleaned beaker was cooled down in a room temperature, mixing thinner and BCB in it on the electronic scale and using a mixer to stir them in 24 hours. Finally, using the syringe and a filter to transfer the solution to the bottle. Figure 3.10 shows that we have obtained a uniform surface of 140 nm BCB.

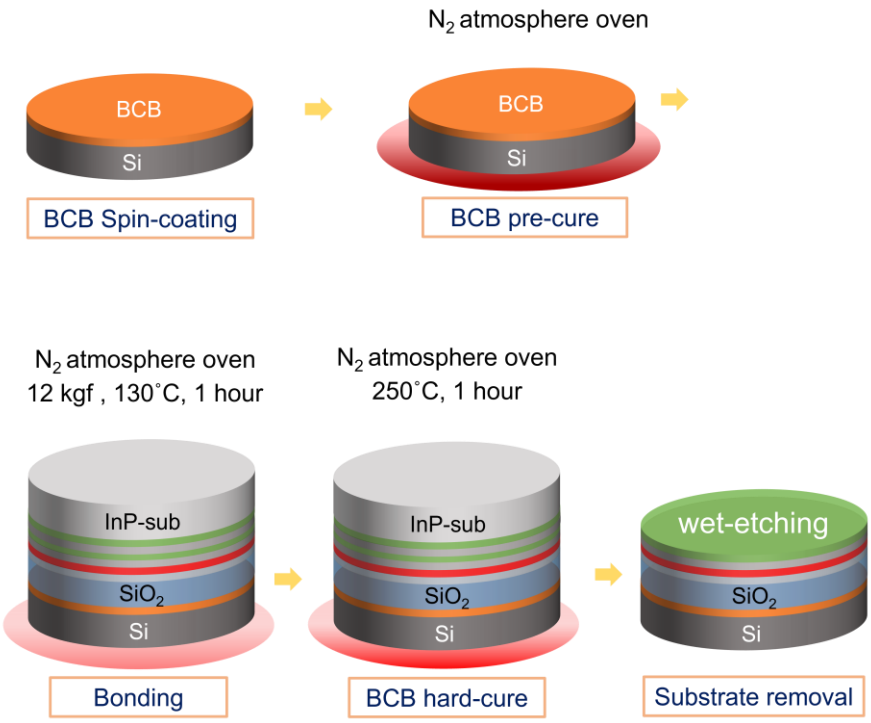


Fig. 3.11 Common BCB bonding process for membrane laser

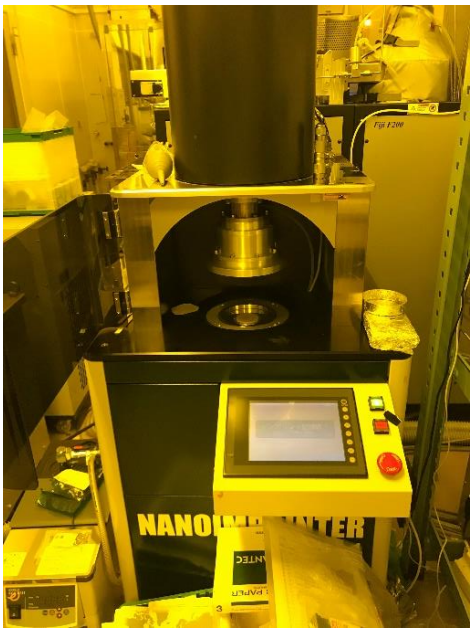


Fig. 3.12 Nano-imprinter system (MEISYO-KIKO)

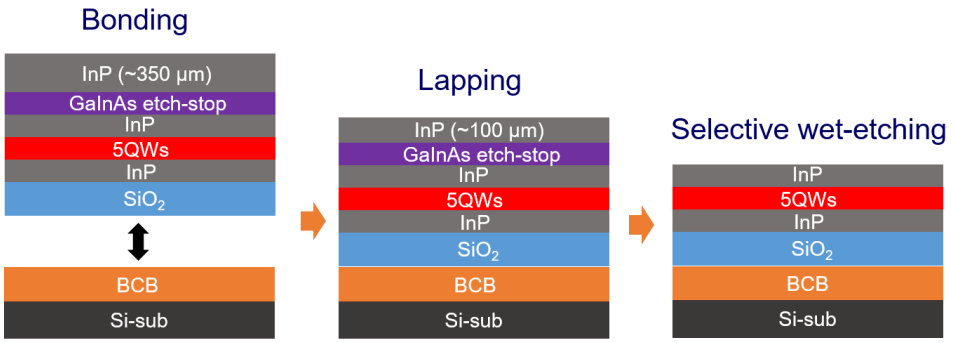
Table 3.2 BCB bonding condition in Nano-imprinter

Step	Force [N]	Temperature [°C]	Time [min]
1	0	30	5
2	120	130	10
3	120	130	60
4	0	30	60

A common BCB bonding process for membrane laser was shown in Fig. 3.11, which includes BCB spin coating, BCB pre-curing, bonding and BCB hard-curing. First of all, 1 μm SiO_2 was deposited on the membrane process wafer by PECVD as a cladding layer, then BCB was spun coated on a 2-inch Si substrate wafer using Delta-80 under the condition shown in Table. 4.1. And BCB-coated Si was pre-cured at an oven in the N_2 atmosphere in 210°C to let BCB from liquid form to partial solidification form. After that, Nano-imprinter (Fig. 3.12) was used to bond the membrane process wafer and BCB-coated Si under the condition of Table 3.2. Next, bonded wafer was hard-cured at an N_2 atmosphere oven in 250 °C.

In the previous research, the pre-cure time strongly determines the bonding quality[3].

The pre-cure has two important effects. One is to transform liquid BCB into gel rubber, another one is to have thinner evaporated. Therefore, for ultra-thin BCB bonding, pre-cure time was discussed as an important parameter. The wafer thinning experiment by selective wet-etching was used to estimate the bonding quality. Dummy III-V wafer including 100 nm InP, 120 nm GaInAsP, 50 nm InP, 100 nm GaInAs etch stop layer, and a 350 μm InP substrate was prepared for the experiment.



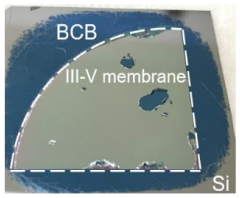
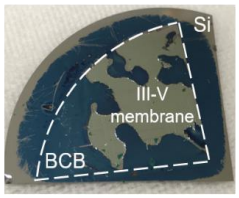
Bonding area			
	~90%	~50%	~0%
Pre-cure time	2 min	6 min	10 min

Fig. 3.13 BCB bonding area dependence on pre-cure time

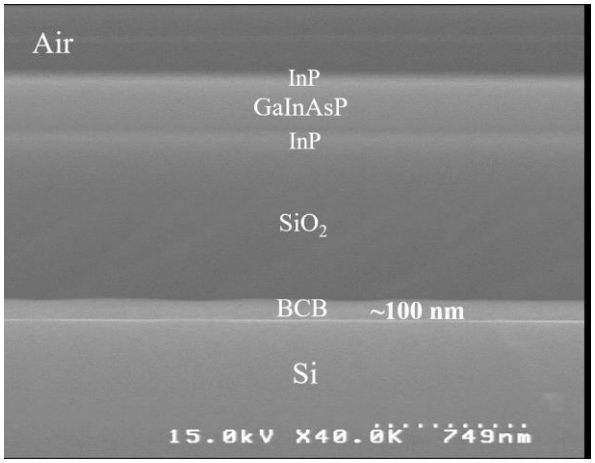


Fig. 3.14 SEM image of bonding interface under 2 min pre-cure time condition

The results are shown in Fig. 3.13. Before selective wet-etching, a mechanical polishing process (lapping) was carried out, which can reduce the InP substrate thickness to about 150 μm, then wet-etching using HCl: CH_3COOH=3:1 solution. It is clear that 2 min pre-cure time seems the better condition, for a 90% bonding area was obtained. And its SEM picture was shown in Fig. 3.14, about 100 nm ultra-thin BCB layer was obtained. PL intensity is shown in Fig. 3.15, and the intensity decrease is smaller than 10%. In pre-cure time of 6 min, about 50 % bonding area can be seen, but it was not uniform, and in pre-cure time of 10 min, there were not III-V layer can be seen in the surface. The reason may be considered that long pre-cure time make most of the BCB to become solid before bonding, and in wet-etching, the etchant went into the bottom of the wafer, the InP was etched from down side, and the wafer was peeled.

Next, a III-V die with 50 nm thickness etched pattern was bonded under the condition of 2 min pre-cure time. The bonding area and its SEM picture were shown in Fig. 3.16. Almost 60 % III-V film left on the surface. The SEM image shows a clear 50 nm step in the BCB layer, which indicates the ultra-thin BCB bonding can be used in membrane laser's fabrication if surface step less than 50 nm was obtained.

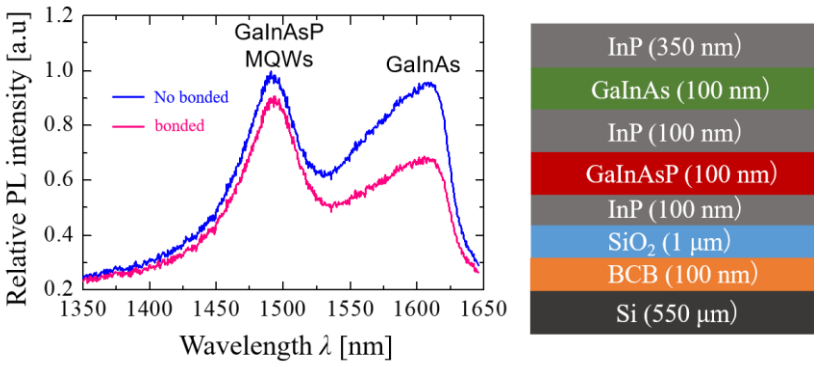


Fig. 3.15 Normalized PL intensity before and after ultra-thin BCB bonding

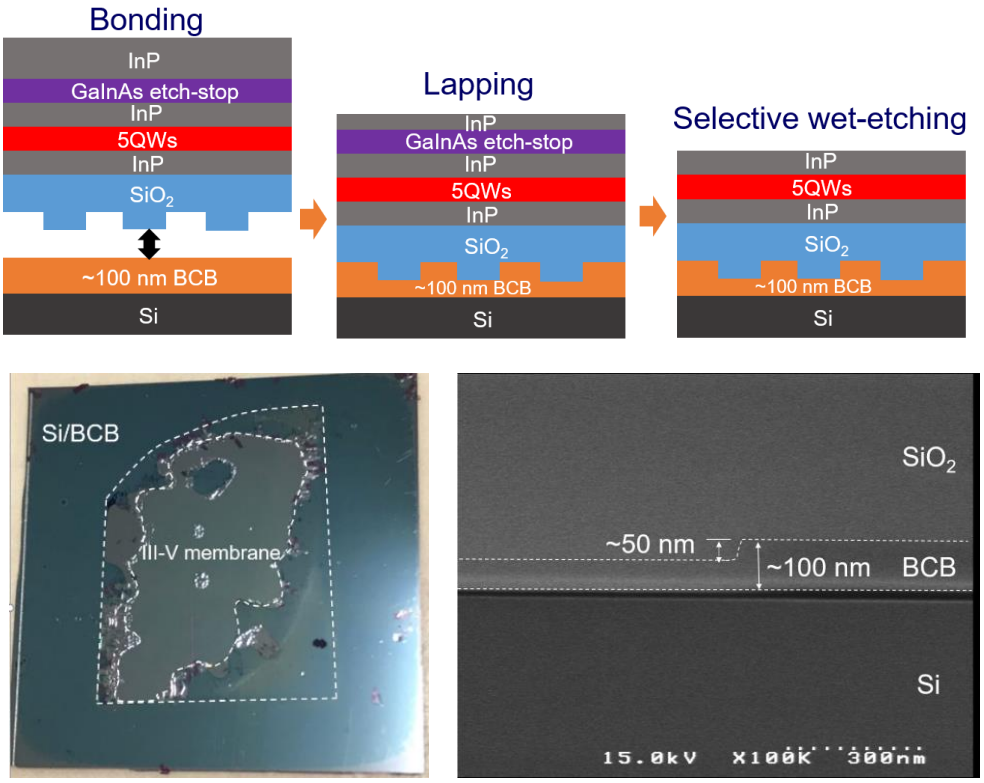


Fig. 3.16 Die to wafer ultra-thin BCB bonding

3.3.2 SiO_2-SiO_2 O_2 plasma activated bonding

In this section, the plasma activated bonding using O_2 plasma will be discussed. The fundamental concept of direct bonding using plasma irradiation is to remove the native oxide and organic contaminants layer on the wafer surface by plasmas such as radical plasma[13]-[14] and reactive ion etching plasma[15]-[20]. The concept image of bonding procedure was shown in Fig. 3.17. After cleaning process, two wafers were irradiated by

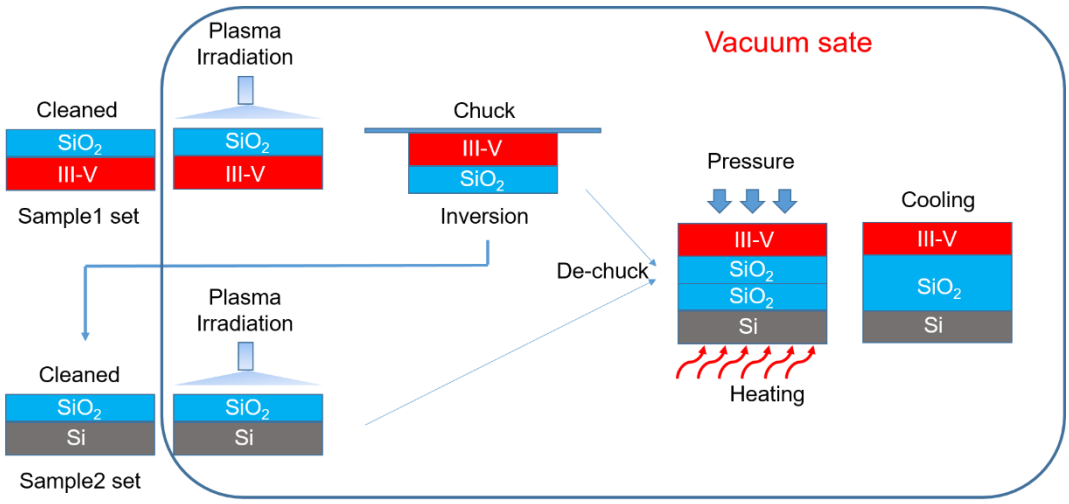


Fig. 3.17 Plasma activated bonding in Membrane

O_2 plasma in a high vacuum chamber (< 10^{-4} Pa). Then, pre-bond at room temperature. Finally, the annealing process would strengthen the bonding strength. Figure 3.18 shows the equipment (VE-07-18 Ayumi industry). The bonding experiment sequence is as follow, and the bonding conditions are shown in Table 3.3.

1. Wafer cleaning and baking.
2. Wafer ① was irradiated in the irradiation room and then be transferred to inversion room. Next, wafer ② was irradiation in the irradiation room, and then be transferred to inversion room contacting with wafer ①. Then, pre-bond at alignment room.
3. Wafer ① and wafer ② were transferred to the bonding room and bond with loading and heating. After bonding, natually cooling to the room temperautre in the vacuum chamber.

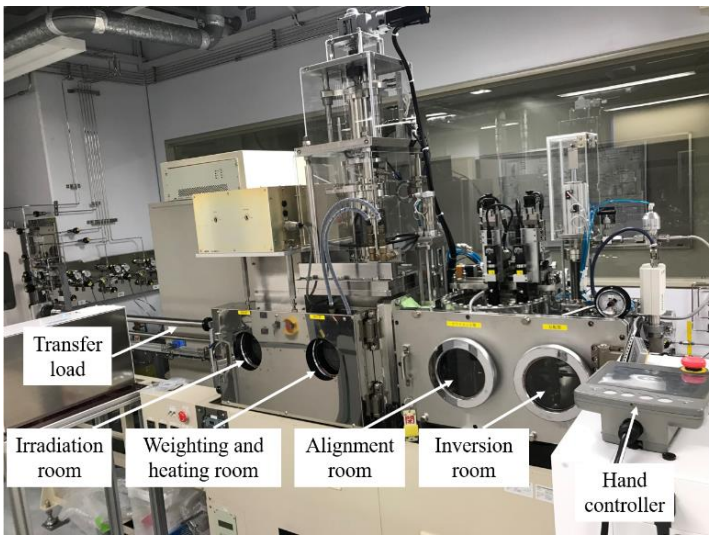


Fig. 3.18 Plasma activated bonding apparatus VE-07-18 (Ayumi industry)

Table 3.3 bonding conditions

Wafer Cleaning	H_2SO_4 2min, DI wafer rinse 10 min, Megasonic 1 min
Baking	200°C, 400 sec with N_2 airflow (EVG 105)
Plasma activation	Gas: O_2 Pressure: 120 Pa Plasma Power: 500 W Time: 10 sec
Pre-bonding	Load: 50 kgf Time: 180 sec
Bonding	Background pressure 10^{-5} Pa Temperature: 25°C ~ 300°C Load: 0.25 ~ 1.0 MPa Time: 2 hours Natural cooling time: 10 hours

A special cleaning process in our laboratory should be introduced, which is the megasonic cleaning. Figure 3.19 (a) shows the appearance of megasonic wafer cleaning mechine EVG301. So far, the removal of 10 μm particles was the limit in the RCA cleaning[21]-[22] and ulrasonic cleaning[23]-[25]. However, the removal range could be expanded to 0.1 μm by introducing megasonic cleaning using an operation frequency of

(a) (b)

Fig. 3.19 (a) Megasonic wafer cleaning system, (b) baking equipment. EVG105

MHz. The baking process was based on the precious work[26] for reducing surface void using EVG105 equipment (Fig. 3.19 (b)). The SiO_2 used for bonding was deposited by plasma enhanced chemical vapor deposition (PECVD). Before bonding, the surface roughness was measured by Atomic Force Microscope (AFM). Figure 3.20 shows the root mean square (RMS) of surface roughness. The RMS was smaller than 0.5 nm, the empirical value for direct bonding, which was suitable to the experiment.

In membrane laser, there are two bonding interface that can be chosen. One is SiO_2-SiO_2, another one is SiO_2-Si. Figure 3.21 gives the comparison of bonding strength under different load pressure condition. The annealing temperature of 150°C was used. The

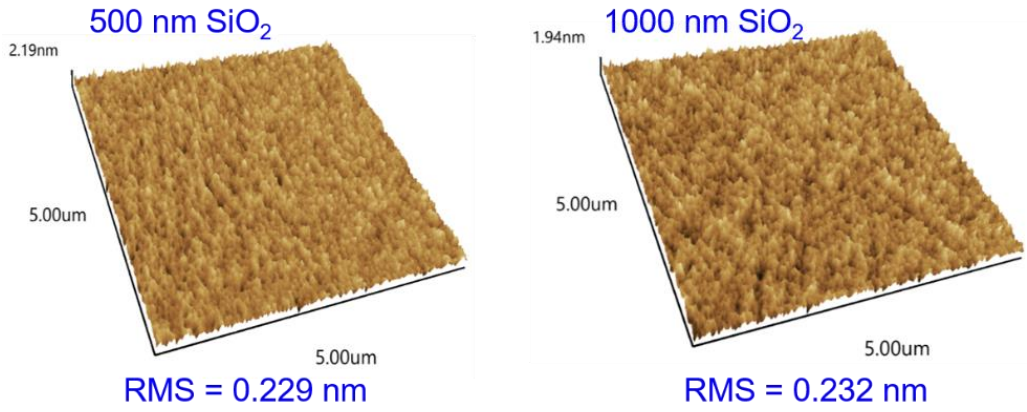


Fig. 3.20 Surface roughness of SiO_2 grown by PECVD

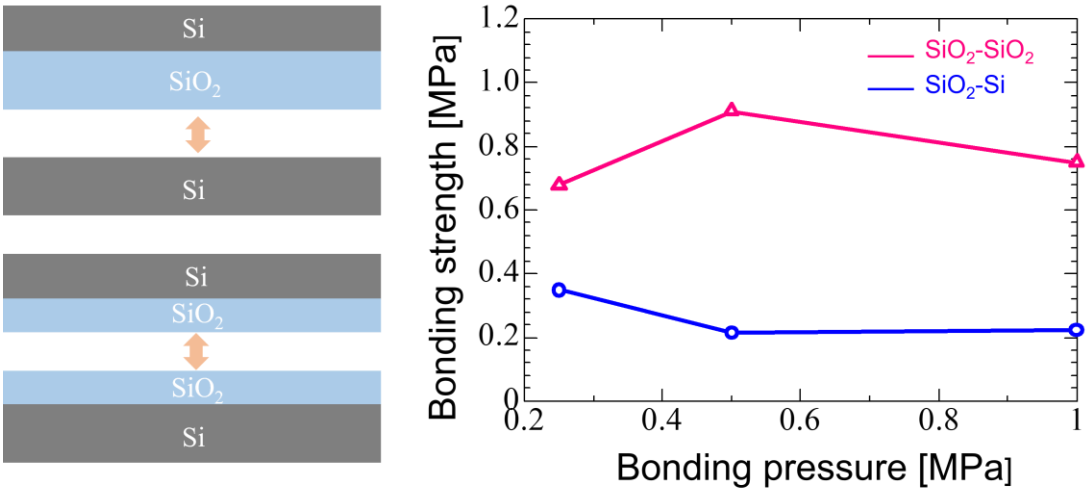


Fig. 3.21 bonding strength by using different bonding interface

bonding strength was measured by using a tensile test. This test using a measurement system applies a tensile force (max: 5000 N) to wafers, and wafers are fixed on the fixture by strong glue (Fig. 3.22). The bonding strength was not sensitive to the bonding pressure from the result, due to the OH^- still remaining at the bonding surface. And the bonding strength of SiO_2-Si was smaller than that of SiO_2-SiO_2, which has the same result as using Ar beam irradiation at room temperature[27]. These bonding strength values are similar to that of in N_2 PAB previous research but the whole bonding strength is small which maybe

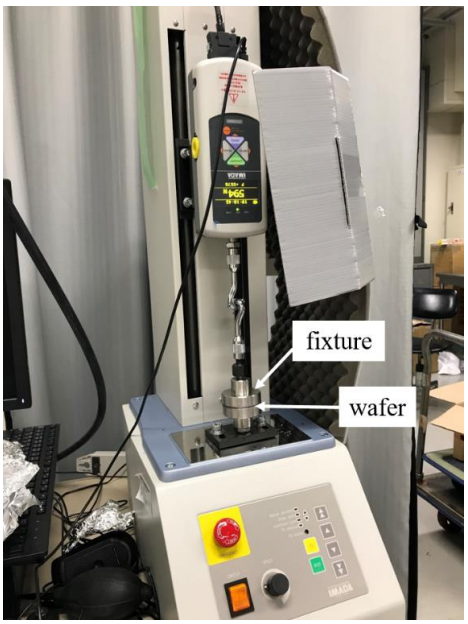


Fig. 3.22 Tensile test system

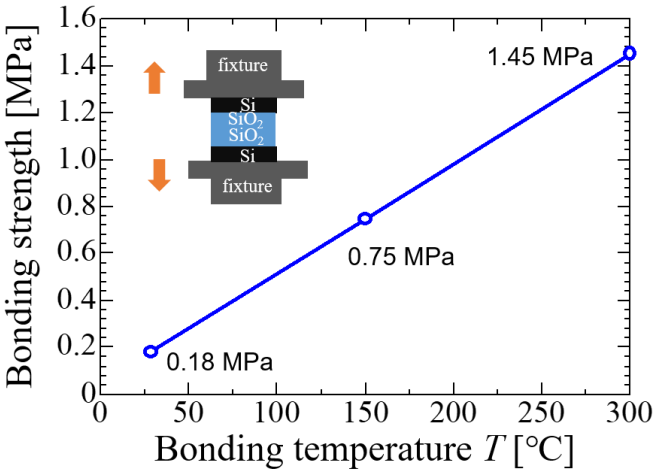


Fig. 3.23 SiO_2/SiO_2 bonding strength dependence of temperature

result of the O_2 plasma irradiation time or power is not enough. The annealing temperature dependence of bonding strength is shown in Fig. 3.23. 1.45 MPa strong bonding strength was obtained at the annealing temperature of 300 °C, which shows the high temperature remove the H_2O at the bonding interface and Si-O-Si bond was formed. 2×2 cm size chip to wafer bonding was also tried under the condition of 1.5 MPa load pressure 150 °C annealing temperature for the previous research indicated that thigh temperature will have a big damage to the active layer[6]. As a result, this chip to wafer bonding obtained a 1.75 MPa strong bonding strength.

After estimating the bonding strength using both Si-substrate, the wafer thinning experiment after bonding using III-V epitaxial wafer with etch stop layer was carried out. Figure 3.24 shows the bonding area using a quarter of wafer. Before doing the selective wet-etch (HCl), a mechanical polishing using Br: methanol = 1: 8 solution was done first. Unfortunately, when the temperature was lower than 200°C, no III-V membrane was bonded on the substrate. The bonding area rise to ~30% with the temperature rise to 300 °C. However, 300 °C high annealing temperature indeed generated a big damage to the active layer, which is the same trend with the previous research. The reason is that high annealing temperature can cause thermal stress due to the thermal expansion coefficient mismatch. The thermal stress is expected to induce strain on MQW and lattice defects in laser structure, resulting in concerns such as bandgap shift of MQW,

degradation of emission efficiency.

The reason of small bonding area could be considered as follow:

1. After O_2 plasma irradiation, the surface of SiO_2 was hydrophilized, and the H_2O did not be completely removed under the low annealing temperature and some voids existed on the bonding interface by residual moisture. So, in this case, the local bonding quality may not high even if the whole bonding strength is strong (the strong bonding strength in the tensile test may be due to the strong bonding strength in some limited local areas).
2. Different with the crystal material such as Si and InP, amorphous oxide like SiO_2 is not adapted to the bonding mechanism using the inherent bonding force in atoms which means the surface activation lifetime is short.

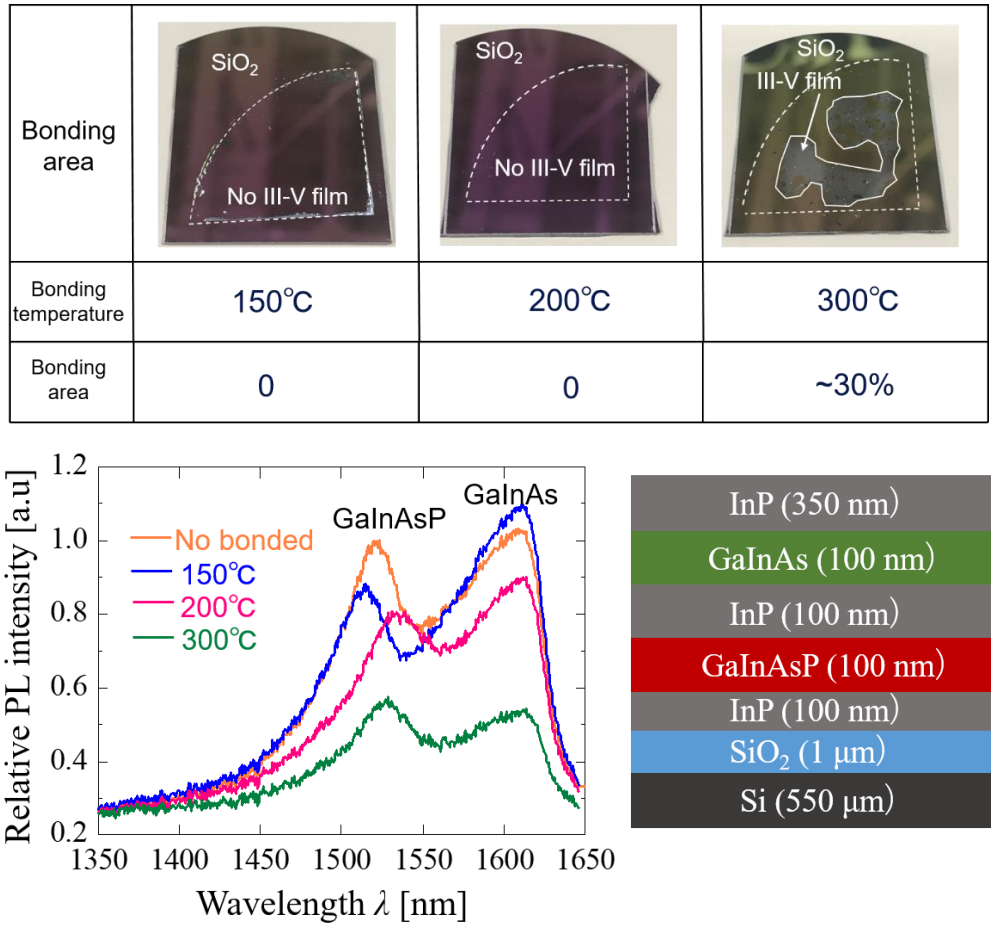


Fig. 3.24 Bonding area and PL intensity after O_2 PAB

3.3.3 SiO_2-Si surface-activated bonding assisted by a-Si nanofilm

As described in Chapter 1, the principle of surface-activated bonding in a room temperature is that interatomic atoms are brought into contact after surfaces which have been activated by physically removing a natural oxide film or organic contamination layer. the advantages include 1. No thermal stress occurs; 2. Low damage to the device; 3. Do not need heating and cooling time. Various materials are easily bonded by this method, but bonding of amorphous oxide like SiO_2 is difficult due to quick reformation of dangling bond at the surface [28]. In order to bond Si/SiO_2 in membrane laser process, a novel idea that using Si nanofilm assisted bonding was proposed[29]-[30]. The process sequence of fabricating GaInAsP/InP membrane structure is shown at Fig. 3.25.

First, an initial epi-wafer consists of a GaInAsP core layer (5 quantum wells and optical confinement layers), two InP cap layers and etch-stop layers was grown by OMVPE. Then, a SiO_2 cladding layer was deposited by PECVD on the epi-wafer. After

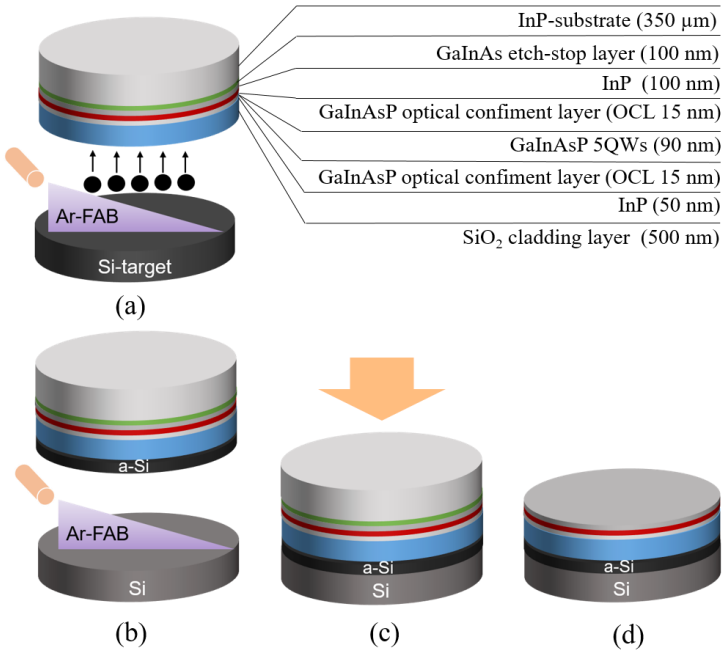


Fig. 3.25 Bonding process sequence of GaInAsP/InP membrane on Si substrate: (a) Sputtering of a-Si nanofilm using Ar-FAB. (b) normal surface activation process to a new Si wafer. (c) room temperature bonding. (d) Removing unnecessary layers by wet etching.

Table. 3.4 Bonding conditions of SAB

Sputtering condition		**Si irradiation condition**	
Voltage	~1.5 kV	Voltage	~1.2 kV
Current	100 mA	Current	50 mA
Irradiation time	5, 10, 15 min	Irradiation time	90 sec
Gas flow	Ar, 30 sccm	Gas flow	Ar, 30 sccm
Chamber pressure	< 10^{-5} Pa	Chamber pressure	< 10^{-5} Pa
Bonding condition			
Temperature	Room temperature		
Load pressure	200 kgf, 500 kgf		
Bonding time	5 min		
Chamber pressure	10^{-6} Pa		

the deposition, the epi and Si-target (sputtering source) wafers were positioned at top and bottom in a high vacuum chamber (<10^{-5} Pa), respectively. Before bonding, the target Si wafer was irradiated using Ar-FAB to sputter a thin a-Si on the surface of SiO_2 (Fig. 3.25(a)). Then, the target Si wafer was removed, and a new Si wafer (2-inch) was introduced as a substrate for bonding. Subsequently, the new Si wafer was irradiated by Ar-FAB [Fig. 3.25 (b)] for removing natural oxide layers and contamination. Finally, two wafers were brought into contact at room temperature (Fig. 3.25 (c)). After that, no post annealing process was followed, which usually requires longer than half a day including the cooling time. When finishing the bonding, the thick InP substrate and GaInAs etch-stop layer were removed by selectively wet-etching (HCl and H_2SO_4:H_2O_2:H_2O=1:1:40) (Fig. 3.25 (d)). The sputtering and irradiation conditions are shown in Table 3.4.

Figure 3.26 shows the bonding equipment of room-temperature surface-activated bonding (MUSASHINO ENGINEERING) in our lab. It supports the bonding chamber

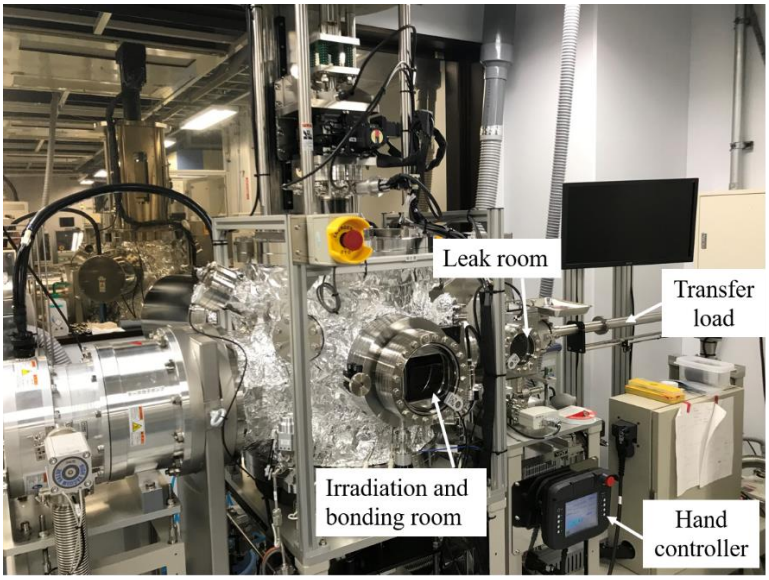


Fig. 3.26 Surface activated bonding equipment (Musashino engineering)

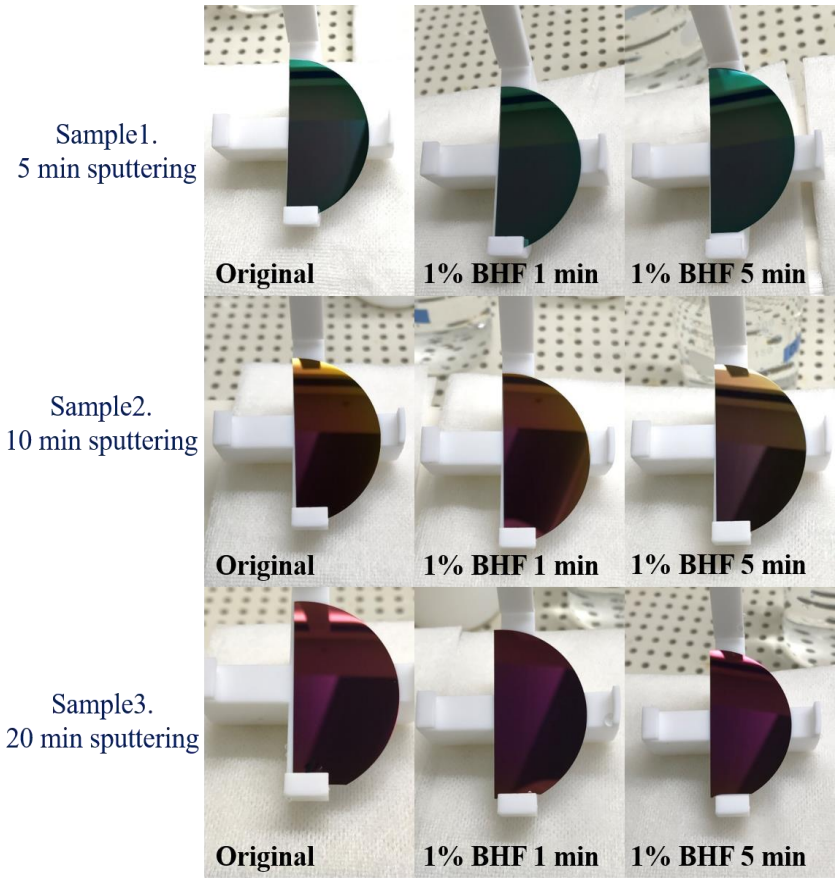


Fig. 3.27 Si nano-film deposition verification

pressure lower than 10^{-5} Pa, and Leak chamber pressure lower than 10^{-4} Pa. Various Gas such as Ar, Ne, Kr, Xe, N_2 can be used. The maximum loading now was 500 kgf .

Before testing the idea in Fig. 3.25, Si nanofilm sputtering effect was estimated by using 1% BHF. The etching speed of 1% BHF to the SiO_2 is about 1 nm/sec. Figure 3.27 shows three samples (Si/SiO_2) that were sputtered with a-Si by 5 min, 10 min and 20 min (current: 100 mA, Ar-FAB). They were soaked in 1% BHF for 5 min. The color of wafers did not change and the thickness of SiO_2 did not change as well, which was measured by ellipsometer. This result indicates the a-Si was successfully sputtered on the surface of SiO_2 by using Ar-FAB irradiation in our SAB machine.

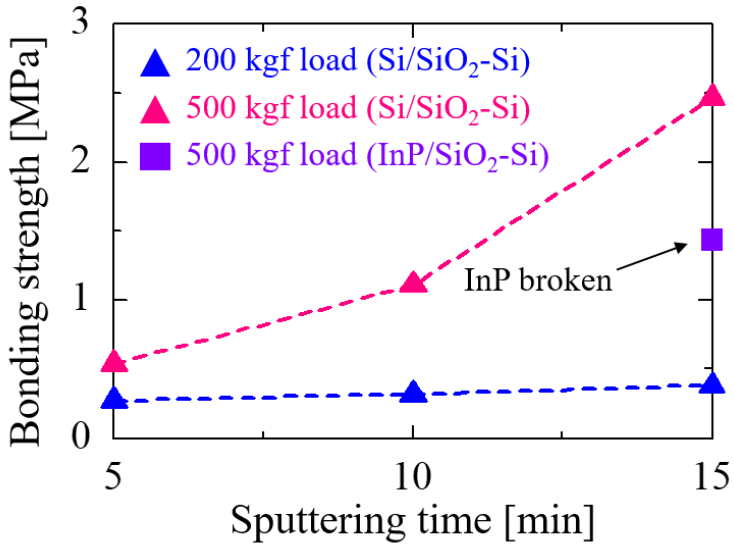
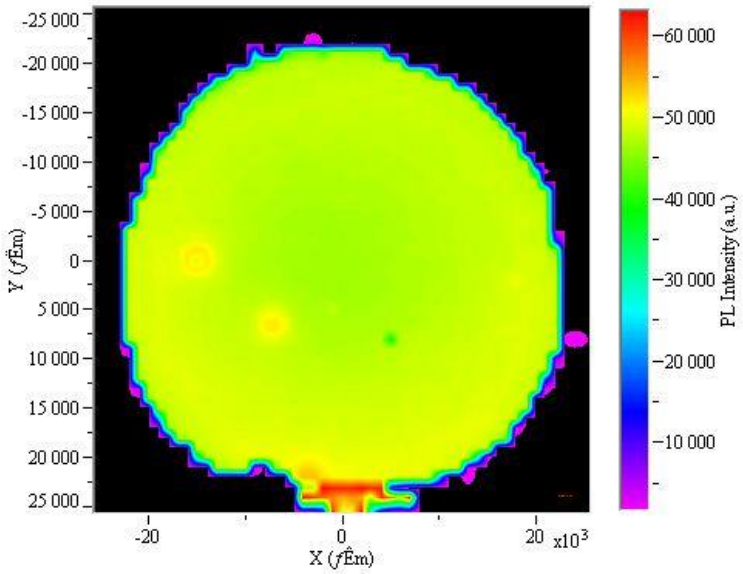


Fig. 3.28 Physical tensile strength dependence on load force and sputtering time[31].

The next step, $InP/SiO_2/Si$ or $Si/SiO_2/Si$ bonded wafers were used in tensile strength (breakdown strength of bonded wafer) measurement was conducted through a vertical tensile test. The parameters used here were sputtering time and load force value in bonding process. Figure 3.28 shows the results of the tensile strength measurements. It indicates that the load value has a significant impact on the tensile bonding strength, which may be the large load force enhance atomic diffusion. In the high load value (500 kgf) condition, sputtering time strongly affects the tensile bonding strength, and in contrast, the sputtering time has little influence in tensile bonding strength when the load value is 200 kgf. The reason can be considered that the uneven sputtered a-Si with low sputtering rate affected the surface contact at short sputtering time condition. Under the sputtering time of 15 min and a 500 kgf load force conditions, an extremely strong tensile

bonding strength over 2.47 MPa was obtained using $Si/SiO_2/Si$ bonded wafer, that reached the measurement limit of our test system. In the case of $InP/SiO_2/Si$, conditions of 15 min sputtering and 500 kgf load were used. A lower bonding strength (1.43 MPa) compared with 2.47 MPa was recorded because of the breaking of InP itself and not from the bonding interface.

(a)



(b)

Fig. 3.29 (a) Bonding area after removing unnecessary layers by selective wet-etching. (b) Uniform PL intensity mapping image.

After checking the tensile bonding strength, a GaInAsP/InP membrane structure was bonded on Si substrate based on conditions discussed above. Figure 3.29 (a) shows the bonding area after wafer thinning process, in which the unnecessary 350-μm-thick InP substrate and GaInAs etch-stop layer were removed by HCl for 60 min and piranha

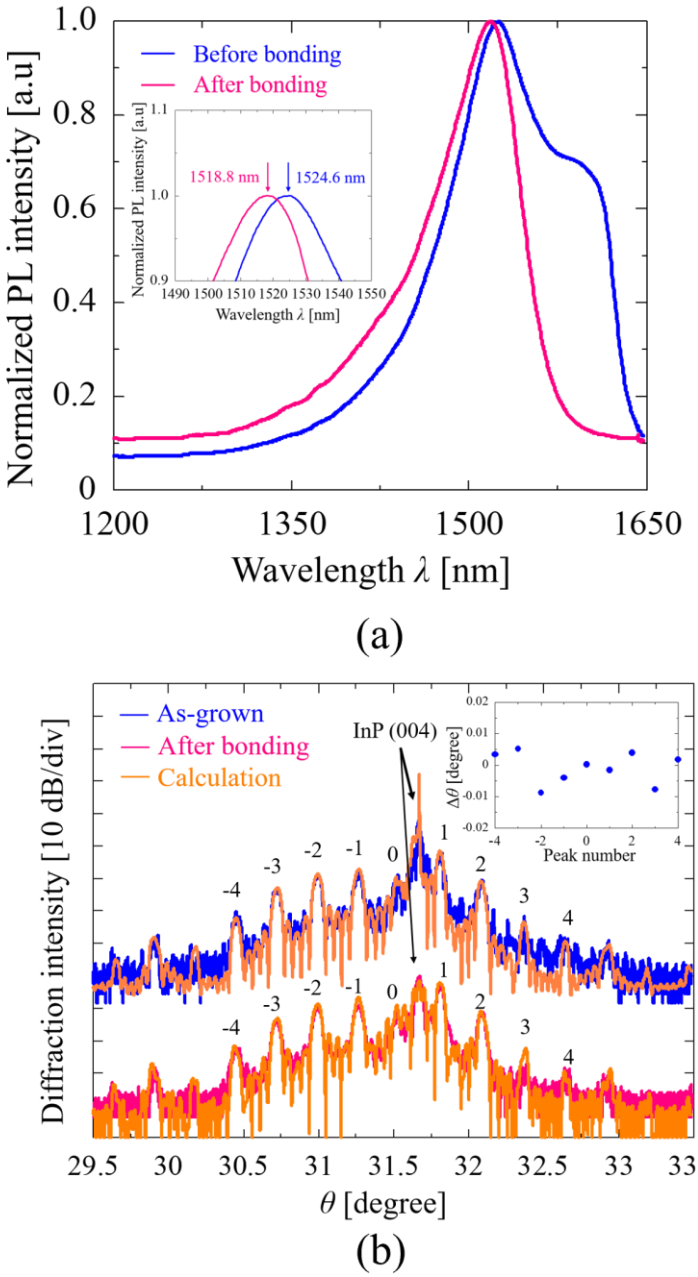


Fig. 3.30 (a) Normalized PL peak wavelength before and after bonding (5.8 nm blueshift), (b) XRD ω-2θ scan data of measurement and calculation.

solution (H_2SO_4:H_2O_2:H_2O=1:1:40) for 5min. A large area over 90% was obtained successfully without obvious voids. Figure 3.29 (b) shows the photoluminescence (PL) intensity mapping image after bonding. A uniform mapping intensity was achieved which shows the GaInAsP/InP membrane was successfully transferred from InP substrate to Si substrate.

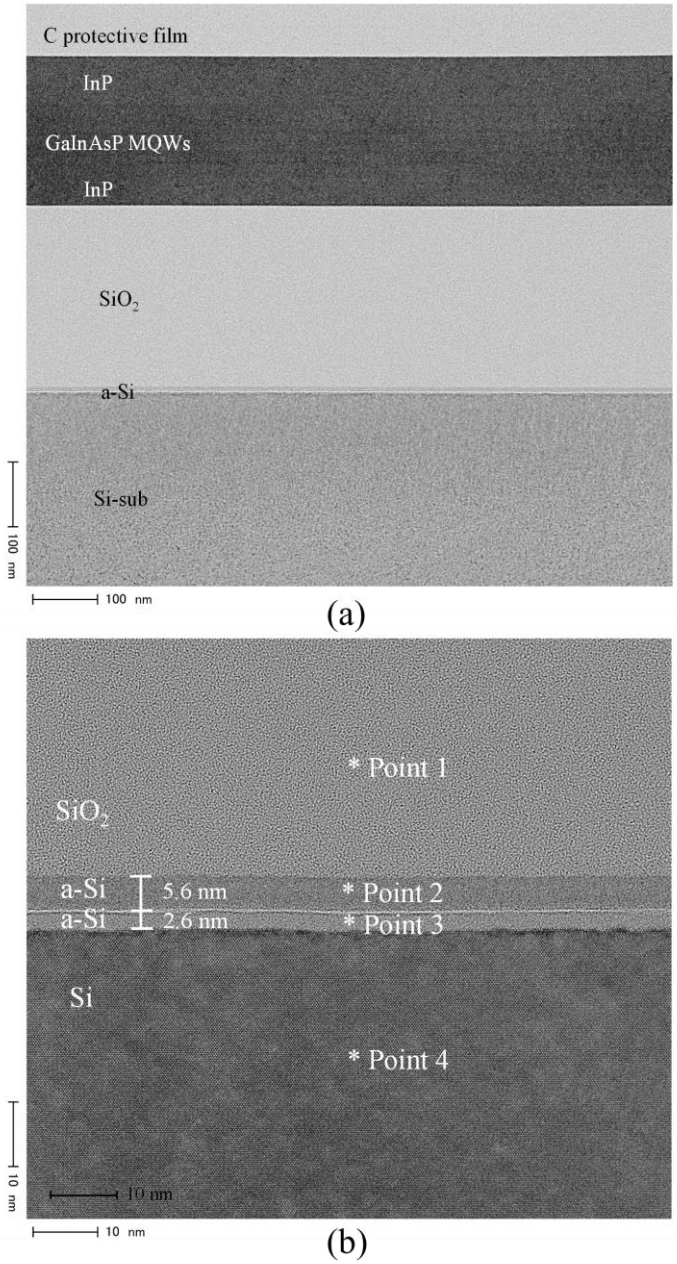


Fig. 3.31 Cross section TEM image of bonding interface (15 min sputtering) (a) Low magnification (b) high magnification.

The quality of MQWs after bonding was estimated by PL peak wavelength and X-ray diffraction (XRD) measurement. Figure 3.30 (a) shows the normalized PL peak wavelength before and after bonding. A slight wavelength blueshift can be observed (5.8 nm) after wafer thinning process. The shoulder at 1630 nm disappeared after bonding because the 300 nm GaInAs etch-stop layer was removed in wafer thinning process. Figure 3.30 (b) shows the XRD ω-2θ scan data of measurement and calculation. Before bonding, the (004) InP peak was dominated by 350-μm thick InP substrate in epi-wafer, and the reduced peak in after bonding line was dominated by 150-nm thick InP cap layers in GaInAsP/InP membrane. The angle shift of satellite peaks from -4 to +4 after bonding were smaller than 0.01 degree shown in the inset figure in Fig. 3.30 (b), which indicates that the position of MQWs peaks were well maintained after bonding. From the fitting calculation, the compressive net strain in MQWs was reduced by 0.02% (0.96% to 0.94%), which can be considered that a strain relaxation occurred when thick InP substrate was removed, and it caused a heavy hole level dropping in valance band of quantum wells resulting in a blueshift in PL peak intensity.

The transmission electron microscope (TEM) image of bonding interface was shown in Fig. 3.31. In Fig. 3.31 (a), an a-Si like layer can be seen between SiO_2 and Si. In the high magnification image of Fig. 3.31 (b), two a-Si layers can be observed. The upper a-Si was 5.6-nm-thick, and the bottom a-Si was 2.6-nm-thick, and they were formed by different mechanism. The different color was due to the different other elements. To understand the elements distribution, Figure 3.32 to 3.33 showed the energy-dispersive X-ray spectroscopy (EDX) measurement in each point shown in Fig. 3.31 (b). Peaks of O, Si, Fe, Ti, C, Ga and Ar were detected. The Ga peaks were caused by TEM observation sample fabrication using Ga ion souse. The C peaks may be due to the contamination in TEM observation by electron beam irradiation. The metal elements such as Fe, Cu and Ti were from the metal wafer holder, which can be avoided by using a large Si wafer as a wafer holder. In point 1 and 4, Si and O or Si dominated the peaks, representing the SiO_2 and Si material in point 1 and 4, respectively. In point 2, Ti had a high peak intensity, which may be from the sputtering process and Si also had a high intensity, which indicates

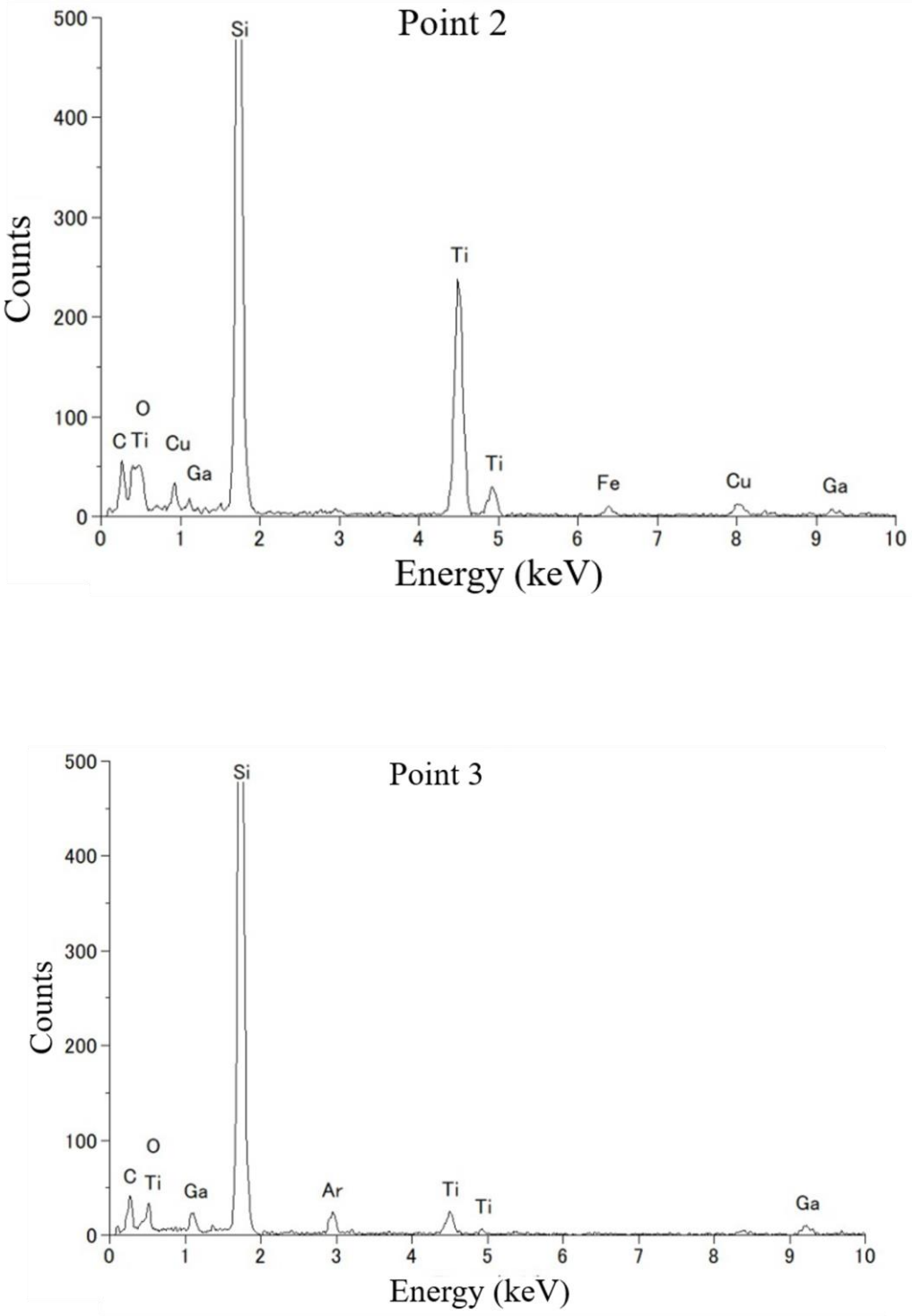


Fig. 3.32 EDX analysis of point 2 and point 3 shown in Fig. 3.31 (b)

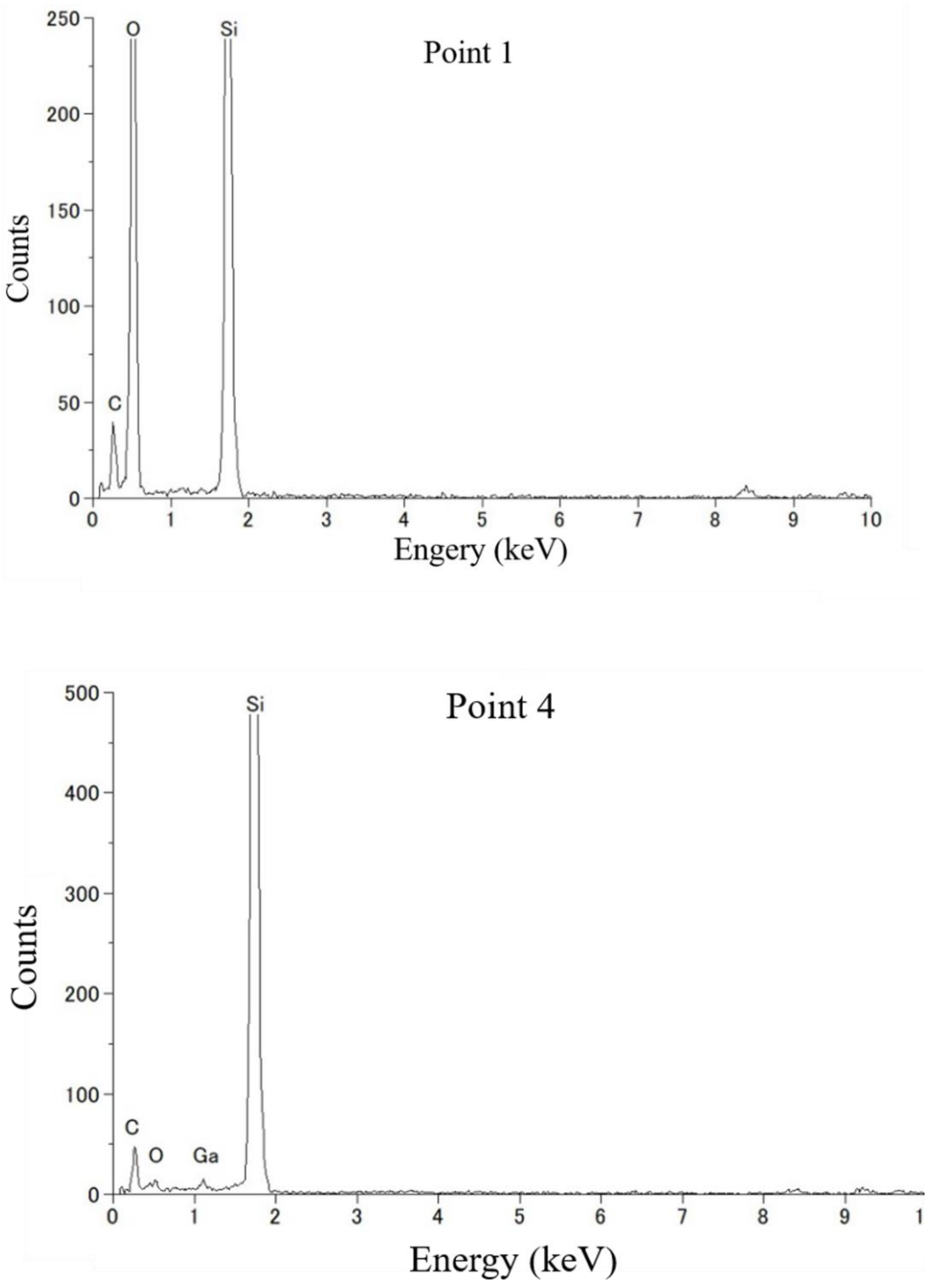


Fig. 3.32 EDX analysis of point 1 and point 4 shown in Fig. 3.31 (b)

that the upper a-Si was formed by sputtering. In point 3, the metal elements peak was not strong, and Ar had a little peak intensity, which reveals that the bottom a-Si layer was formed by Ar-FAB irradiation to the new Si wafer in bonding process and the surface crystal Si was transferred to a-Si. The elements of metal came to the bottom side due to the atom diffusion.

By summary the results discussed above, GaInAsP/InP membrane structure was transformed from InP to Si by a high quality room temperature bonding technology with no treading dislocation and the a good MQWs characteristic remaining.

3.4 Conclusion

In this chapter, bonding technologies for reducing thermal resistance of membrane laser have been discussed. Studies of various bonding technologies in our lab were reviewed at first. Then, ultra-thin BCB bonding and direct bonding including O_2 plasma activated bonding and room-temperature surface-activated bonding were investigated. The comparison between three bonding methods was summarized in Table 3.5. The ultra-thin BCB bonding has a stable fabrication process and large bonding area. Even though the bonding strength is smaller than other methods, it is enough to fabricate membrane laser. The annealing temperature up to 250 °C and long process time are its demerits. The O_2 plasma activated SiO_2-SiO_2 bonding has a large bonding strength. Unfortunatly, the low temperature, large area bonding was not achieved in this study. Other group has achieved a good quality bonding using the same way annealing at 200 °C. To futher increase the bonding quanlity, different plasma power, irradiation time should be optimized. Also, for keeping surface activation of SiO_2, the time interval between two wafers irradiation should be considered, although it may be limited by the system of

Table 3.5 Comparison between three bonding methods in this study

	100 nm BCB	**O_2 PAB**	**a-Si SAB**
Bonding strength	0.9 MPa [2]	1.45 MPa	>2.47 MPa
Bonding area	~ 90%	~ 30%	~ 90%
Process time	~6 hours	~12 hours	~2 hours
Anneal temperature	250 °C	>300 °C	RT
PL decrease	< 10%	~44%	< 10%
For membrane laser	Surface flattening is needed before bonding		

machine. The a-Si nanofilm assisted surface-activated room-temperature bonding is the novel method for membrane laser. In this way, large bonding stength , bonding area, no post annnealing, and short process time are the attracting points. Actually, this method can tranform any meterial bonding to Si-Si bonding. It has broad prospects and can be used to integrate most of devices to any substrate. for fabricating membrane laser, using direct bonding can minimize thermal resistance, but surface flattening of SiO2 is neede before bonding, and we would like to use chamical machanical polishing (CMP) to sove this problem, which would be discussed in Chapter 4.

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Chapter 4

Membrane laser for low thermal resistance and high temperature operation

4.1 Introduction

The fabrication of membrane laser started with buried hetero structure formation, which needs three-times epitaxial growth for 1.22-μm GaInAsP (waveguide material), *n*-doped and *p*-doped InP. Then, the bonding will be followed after deposition of SiO_2. However, the surface is not flat after three-times epitaxial growth, that will be discussed at section 4.2.2 in detail, so as to the surface of SiO_2. This thickness difference is over 130 nm in a narrow region. Therefore, the direct bonding or 100-nm ultra-thin BCB bonding cannot be used without any surface flatten process.

In this chapter, chemical mechanical polishing (CMP) planarization technology was newly introduced for surface flattening of SiO_2. The wet-etching used in grating formation for reducing damage to active region was unstable in the previous work. This time, the dry-etching using RIE system was used again. The result shows little affect to the laser properties, meanwhile, the process became more controllable and stable.

The chapter started with the equipment introduction and key technologies investigation of grating formation, CMP and surface activated bonding assisted by a-Si discussed in chapter 3. Next, the entire process flow will be shown with optical microscope photos. The lasing and thermal characteristic of thin BCB bonded membrane DR laser, direct bonded membrane Fabry-Perot laser and DFB laser is shown in section 4.3. The thermal resistance reduction due to direct bonding was confirmed and it agrees with the calculation results. For high temperature operation, special cavity using Bragg waveguide detuning was introduced, which supports a 110 °C continuous-wave (CW) operation of membrane DFB laser.

4.2 Fabrication process

4.2.1 Equipment

【*OMVPE: Organometallic Vapor Phase Epitaxy*】

OMVPE is a chemical vapor deposition method i for preparing compound semiconductor single epitaxial or polycrystalline thin films proposed by Rockwell Corporation in 1968. The OMVPE was developed by H. M. Manasevit in 1968[1], and suddenly promoted its research and development due to the success of room temperature continuous lasing of AlGaAs/GaAs double heterostructure laser by Dupuis and Dapkus in 1978[2].

Other similar names such as: MOVPE (Metal-organic Vapor-Phase Epitaxy) or MOCVD (Metal-organic Chemical Vapor Deposition), etc. The first two letters "MO" or "OM" refers to the reaction source used in the growth of the semiconductor film is the metal organic "Metal-organic" or the organometallic compound "Organometallic". The "CVD" refers to grow an amorphous film, and "VPE" refer to grow a crystalline film. In general, "CVD" refers to the growth of amorphous films, which is classified as "Deposition" and "VPE" refers to the growth of films with crystalline, which is "Epitaxy".

In the OMVPE method, both the raw materials of group III and group V elements for crystal growth can be carried as a vapor, which is the biggest difference from other crystal growth methods such as the liquid phase epitaxy (LPE) method and molecular beam epitaxy (MBE) method, and the characteristics of the OMVPE method are film thickness uniformity and film thickness controllability over a large area, crystal composition uniformity, and even steepness. In this research, OMVPE was used for regrowth process of GaInAsP waveguide and InP for the formation of lateral p-i-n junction. Tri-methyl Indium (TMI), Tri-methyl Gallium (TEG), PH_3 and AsH_3 (1%) are used as materials for growth of GaInAsP. When growing InP, TMI and PH_3 are used. The photo of the OMVPE system (NIPPON SANSO: HR3255) was shown in Fig. 4.1.

Fig. 4.1 Organometallic vapor-phase epitaxy system

【***PECVD: Plasma enhanced chemical vapor phase deposition***】

Plasma-enhanced chemical vapor deposition (PECVD) is a widely accepted technology in the industry. PECVD uses an electrical source of energy to generate plasma and sustain the reaction process rather than thermal energy for the majority of the CVD processes. It converts the reactive gas into a plasma state and causes a chemical reaction on the target substrate to generate active free radicals and ions on the target substrate to form a thin film for deposit. The main reason for its acceptance is its ability to operate at a lower temperature than thermal CVD[3]. At present, there are still many unclear points about the plasma CVD process involving chemical reactions[4]. Nevertheless, the plasma CVD method has the excellent feature of being able to form thin films of various functional materials at relatively low temperatures, so it is an industrially very important technology, and its application fields are expanding more and more[5].

One of the typical application examples of plasma CVD is low-temperature deposition of silicon and its oxides and nitrides, which are indispensable for manufacturing

electronic devices such as thin-film solar cells. In recent years, research has been actively conducted for higher functionality and lower cost of these devices.

Dielectric materials such as silicon dioxide (SiO_2) are often deposited by PECVD for use as gate oxides[6], inter-metal dielectrics[7] or passivation layers for integrated circuits[8]. Organosilanes, such as tetraethoxysilane (TEOS), have been used since the 1960s to deposit SiO2 by PECVD[9]. TEOS has reduced toxicity and hazard compared to more conventional sources[8]. Furthermore, TEOS provides better conformality and void free films with superior step coverage even at geometries less than 0.5 μm[8]. Although SiO_2 films deposited from pure TEOS show hydrocarbon incorporation in this film, addition of an oxidant such as O_2 or O_3 eliminates this film contaminant[10]. Generally, in order to obtain an oxide film using TEOS, the reaction shown in the following equation

$$Si(OC_2H_5)_4+12O_2 \rightarrow SiO_2+8CO_2+10H_2O \quad (4.1)$$

Figure 4.2 shows the appearance of the PECVD system (SAMCO: PD-100ST). TEOS (Tetraethyl orthosilicate) and oxygen are introduced into the chamber as material gases, and a high frequency voltage is applied to plasmatize the material gases to form a film of

Fig. 4.2 Plasma-enhanced chemical vapor phase deposition (PECVD) system

SiO_2. There are two main situations we use SiO_2, one is for deposition of semiconductor transfer masks, another one is optical cladding layer. Table 4.1 shows the deposition condition of SiO_2 used in the fabrication process of membrane laser.

Table 4.1 Deposition condition of SiO_2

Parameters		Setting value
Gas Flow	TEOS	3 sccm or 1sccm
	O_2	233 sccm
RF power		30 W
Pressure		70 Pa
Temperature (upper/bottom electrode)		280℃/280℃
Deposition rate		~50 nm/min or ~25nm/min

【***Maskless Photolithography system***】

The maskless photolithography machine uses a digital micromirror device (DMD) manufactured by Texas Instruments, Inc. in the United States to generate the exposure pattern, so no mask is required. It is possible to reduce the cost and the time to exposure because the mask is not manufactured. It is also useful for small-lot, high-mix production and research and development applications. Fig. 4.3 shows the outward appearance of maskless machine (DNK). The maximum exposure power is 100 mJ/cm^2, the exposure area is 100 ×100 mm, and maximum exposure speed is 3.6 mm/s. A semiconductor laser is used as the light source, the wavelength of laser is 375 ± 5 nm. In membrane process, all the photolithography processes, expect grating and InP-rib waveguide, are using maskless lithography machine.

Fig. 4.3 Maskless photolithography system (DNK IP-1007-2(MX-1204))

【***RIE: Reactive ion etching***】

In this research, for obtaining a vertically etched surface, dry etching was used for the patterning o the SiO_2 mask and the formation of the III-V compound mesa. Figure 4.4 shows two types of RIE system (RIE-10NR SAMCO). One is used for etching SiO_2 to transfer photoresist mask to SiO_2 using the CF_4. The other one is used for etching of III-V compound semiconductor with SiO_2 mask using CH_4/H_2 = 10/40 sccm. However, when etching using mixture of CH_4 and H_2, accumulated polymer will prevent a vertical etched surface. Therefore, a repeated process of CH_4/H_2 etching and O_2 ashing is needed. The conditions for CF_4 and CH_4/H_2 were concluded in Table 4.2 and 4.3.

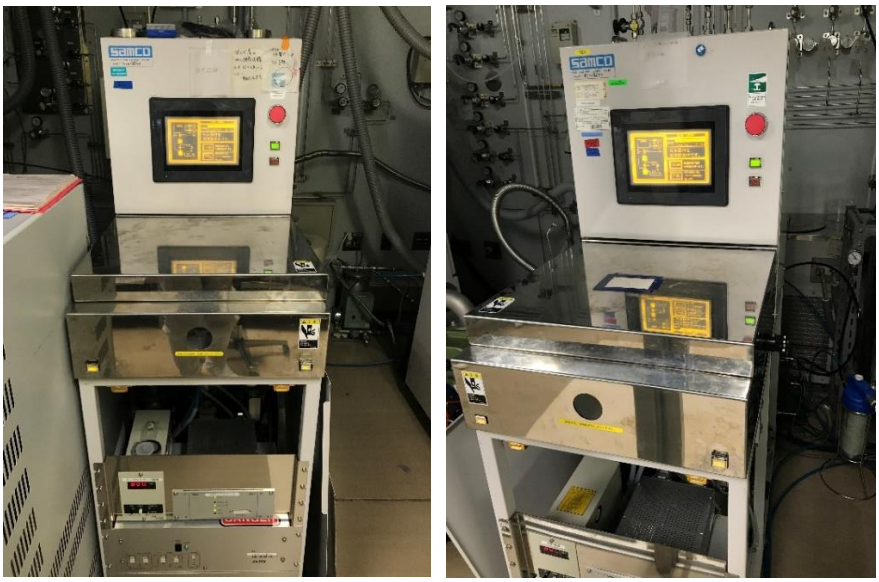


Fig. 4.4 RIE system (RIE-10NR SAMCO)

Table. 4.2 Etching condition of III-V semiconductor using CH_4/H_2 RIE

Parameters		Step 1	Step 2
Gas flow	CH_4	10 sccm	-
	H_2	40 sccm	-
	O_2	-	30 sccm
RF power		100 W	50 W
Pressure		6 Pa	10 Pa
Time		60 sec	40 sec

Table. 4.3 Etching condition of SiO_2 using CF_4 RIE

Parameters	Setting
Gas flow (CF_4)	10 sccm
RF power	25 W
Pressure	1 Pa
Time	10 min

【***Resistive thermal evaporation***】

In this research, we use resistive thermal evaporation system (TOKYO VACUUM, EG-240) to deposit Au/Zn/Au p-type electrode. The picture was shown in Fig. 4.5. The heating temperature based on e-beam can be extremely high, so there is a risk that Zn will explosively boiling. In this system, the thermal evaporation is performed by heating the source material using a resistive coil. The maximum heating temperature is limited, and temperature can be increased gradually, explosive boiling of Zn can be avoided.

Fig. 4.5 Resistive thermal evaporation system (TOKYO VACUUM, EG-240)

【***Electron beam evaporation***】

Electron beam or electron beam evaporation is a form of physical vapor deposition in which a target material used as a coating is bombarded with an electron beam from a charged tungsten filament to evaporate and convert it into a gaseous state to be deposited on the material to be coated. In a high vacuum chamber, these atoms or molecules then precipitate in the gas phase and form a thin film coating on the substrate. When the electron beam hits the surface of the evaporator, the kinetic energy of its movement is converted into heat by the impact. Although the energy released by a single electron is small, there are lots of them. The total energy released is quite high, usually more than a

few million watts per square inch. Therefore, it is easy to understand that the hearth holding the evaporate must be water-cooled to prevent melting. The heating temperature based on E-beam can be extremely high, metals such as Ti, which has a high melting point, is suitable in this system. In the membrane laser fabrication, Ti/Au for n and p type electrode was used in deposition. The photo of electron beam evaporation system was shown in Fig. 4.6.

Fig. 4.6 Electron beam evaporation system

【***RTA: Rapid thermal annealing system***】

This system (RTP-6 Adcance RIKO, Inc) can concentrate heat on a substrate surface by the infrared light emitted from the flash lamp, so that a short time annealing can be achieved. The maximum temperature of this system is 1100℃, and we used it for annealing process after deposition of Au/Zn/Au p-electrode in 350℃ for 1 minute and natural cooling to room temperature.

Fig. 4.7 Rapid thermal annealing system (RTP-6; Advance RIKO, Inc)

【***Electron beam lithography system***】

Compared with mask photolithography system, the electron beam lithography system can provide much more precise control for patterns. The accuracy of lithography is affected by the scattering of photons on the wavelength scale. The shorter the wavelength of light used, the higher the precision that lithography can achieve. According to De Broglie's matter wave theory, electrons are waves with extremely short wavelengths. In this way, the accuracy of electron beam exposure can reach nanometer scale, which provides a useful tool for making nanowires. In membrane laser's fabrication process, it is used when forming the grating of the DFB and DBR region. And the design of the

exposure patterns is based on the AutoCAD software. Figure 4.8 shows the electron beam (EB) lithography system of JEOL JBX-6300UA.

Fig. 4.8 EB lithography system of JEOL JBX-6300UA.

【***Dicing machine group***】

The dicing saw is a kind of cutting machine, which was used to cut Si wafer into bar for measurement in membrane laser fabrication at last. Half-cut to cut 2/3 or 3/4 degree of wafer thickness at first and break the wafer using breaking machine to form a cleaving surface was follow for keeping a good cleaving surface for laser. The wafer was first mounted on the UV curable tape using mounter machine (Fig. 4.9 (a)), then cut by dicing saw (Fig. 4.9 (b)) into bar structure. After cutting, the cleaving surface was formed by breaking machine (Fig. 4.9 (c)). Then, each bar was separated by a certain distance using expander machine (Fig. 4.9 (d)). Finally, the sample was removed after UV irradiation (Fig. 4.9 (e)) for reducing the stickiness of UV tape.

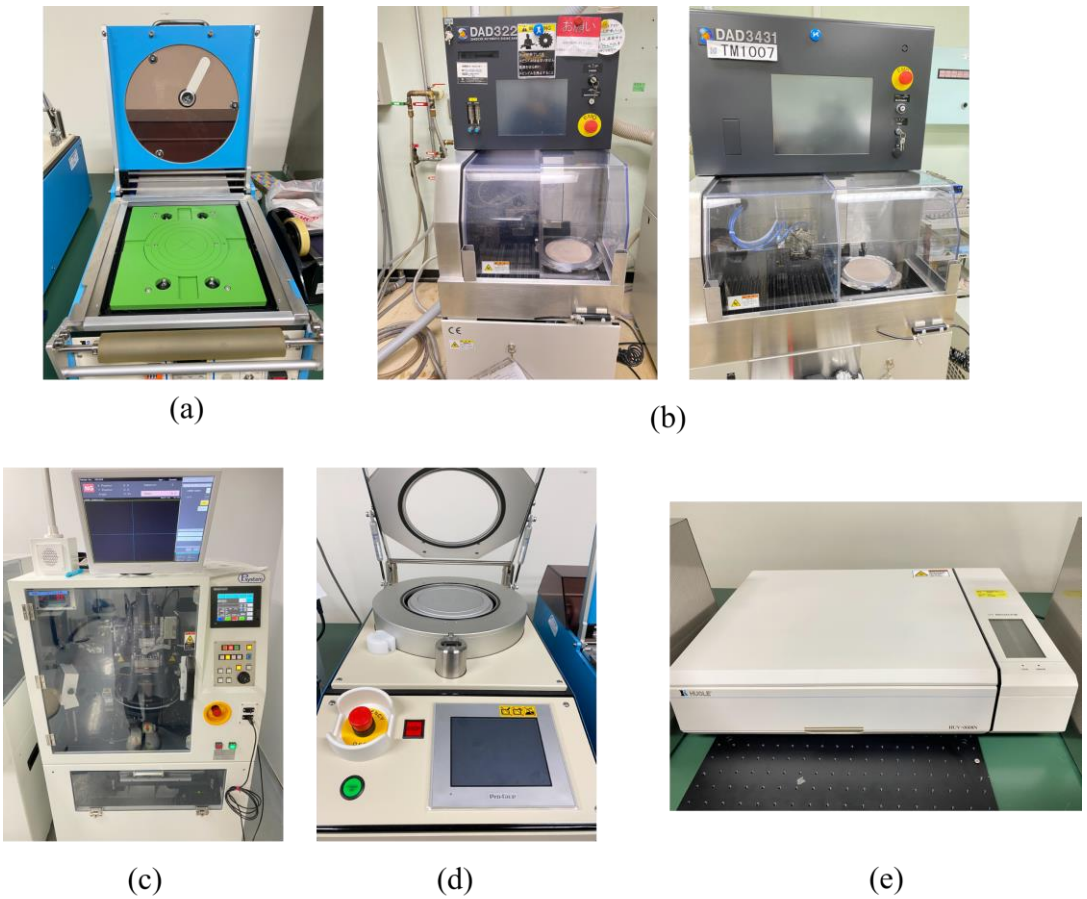


Fig. 4.9 Dicing machine group (a) mounter (UV tape) (b) automatic dicing saw (DAD322 and DAD 3431, DISCO) (c) breaking machine (d) expander machine (e) UV irradiation machine

4.2.2 Chemical mechanical polishing

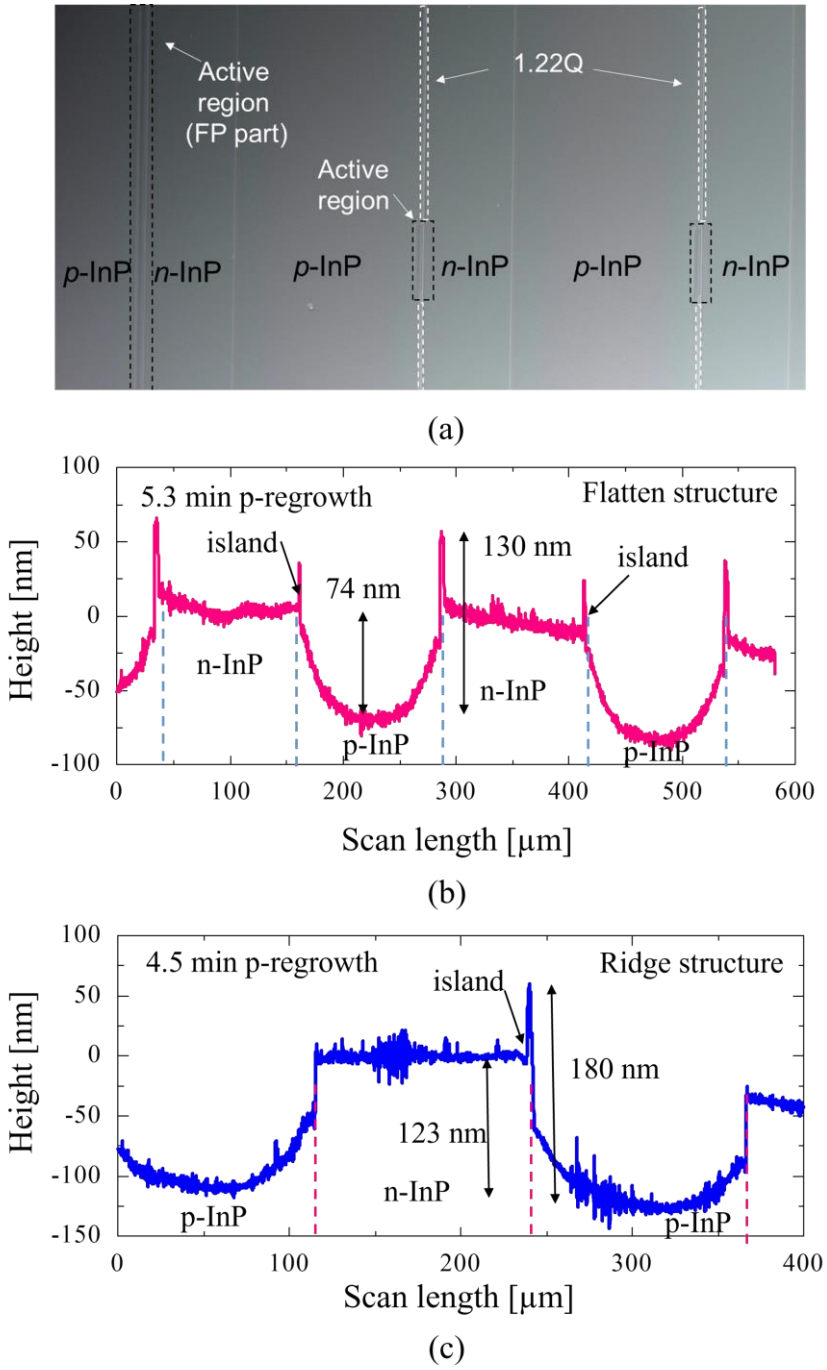


Fig. 4.10 (a) Optical microscope photos before bonding (b) Surface thickness scan data in flatten structure (c) Surface thickness scan data in Ridge structure.

As discussed in section 4.1, the fabrication of membrane laser started with three-times OMVPE process, and the SiO_2 would be deposited. Subsequently, the bonding between III-V and Si wafer would be followed. Finally, surface grating or electrodes formation was carried out. After *n*-side and *p*-side InP regrowth, the surface thickness distribution was shown in Fig. 4.10. The regrowth process keeps the thickness of *n* and *p*- InP near active region flatten, but the far region is not. Also, the different mask width design leads to different thickness of *n* and *p*-InP and some "over-regrowth" occurred at the edge of mask. The thickness distribution would remain after SiO_2 deposition by PECVD. Figure 4.10 (b) shows a 130 nm thickness step in flatten-waveguide-structure, and more large step of 180 nm in ridge-waveguide-structure[11] (Fig. 4.10 (c)). The BCB bonding can easily overcome this problem, however, the situation is not the same in direct bonding. CMP is introduced to flatten the surface of SiO_2. Figure 4.11 shows the CMP system including a hard urethane polishing pad, a metal pad conditioner with diamond on surface, a wafer chuck, DI water tube and slurry tube. *In-situ* polishing method was used to improve the in-plane uniformity. The *In-situ* polishing means that when the wafer is polished, the pad is polished by pad conditioner at the same time. In the experiment, the in-plane uniformity, surface roughness, polishing rate were checked at first using bare wafer at first, then, the surface step polishing was check. Finally, combining the CMP and SAB, the bonding quality was checked.

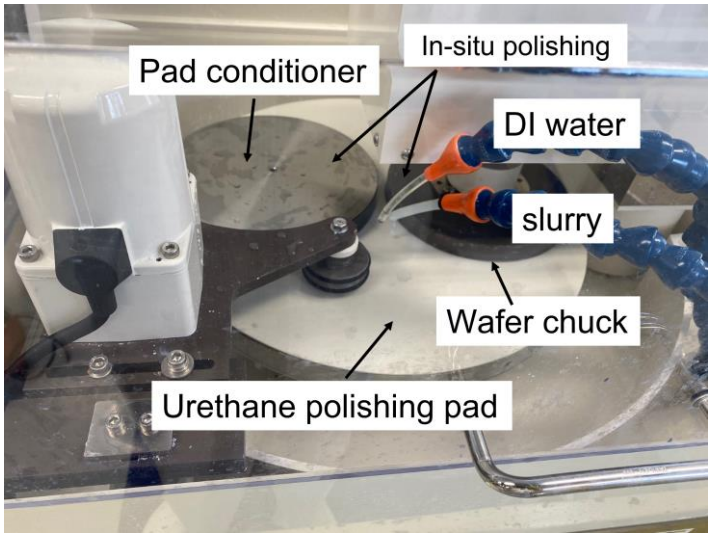
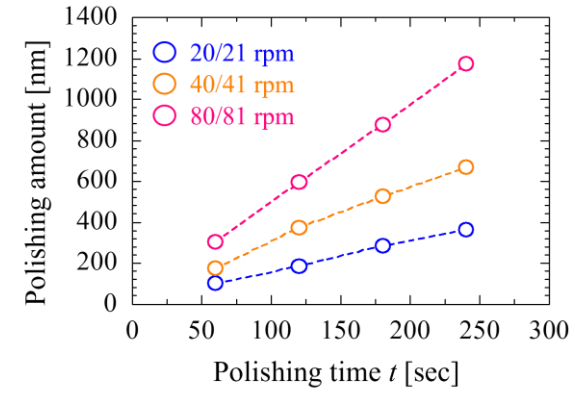


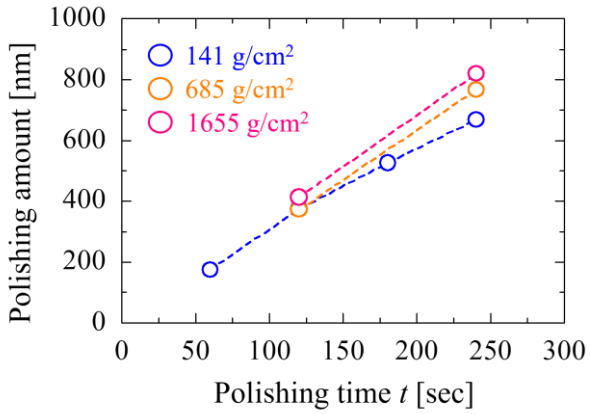
Fig. 4.11 CMP system (MAT. Inc)

1. Polishing rate dependence

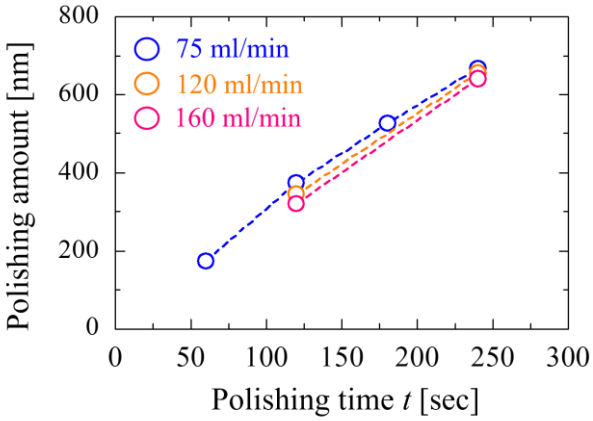
(2 cm × 2 cm chip)



(a)



(b)



(c)

Fig. 4.12 Polishing rate dependence (a) rotation speed (b) polishing pressure (c) slurry flow rate

From Fig. 4.12, it indicates that the most important influence on the polishing rate is the rotation speed of polishing pad and head followed by polishing pressure. The flow rate of slurry has little effect on polishing rate maybe because 75 ml/min reaches the saturation point of polishing rate. Also, the photo after polishing shows different color on the surface, which is the thickness difference of SiO_2. The color become deep when polishing amount increasing, which means the in-plane uniformity gradually deteriorating. The surface pattern is only determined by the wafer shape.

2. In-plane uniformity.

(2 cm × 2 cm chip)

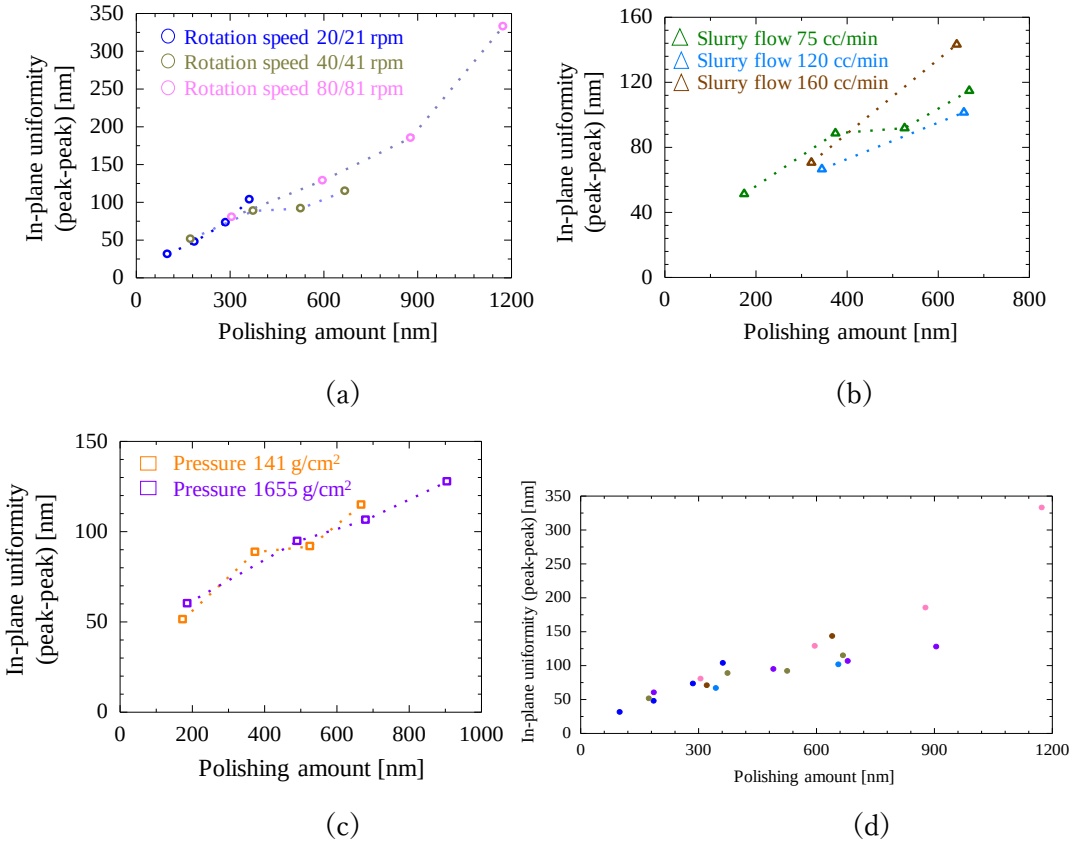


Fig. 4.13 The in-plane uniformity dependence (a) rotation speed (b) polishing pressure (c) slurry flow rate (d) overall view.

The in-plane uniformity was estimated by measuring 9 points of 2 cm × 2 cm chip and calculating the thickness difference between maximum value and minimum value. Figure 4.13 (d) shows that the in-plane uniformity increases with the polishing amount increasing. The rotation speed, pressure, and slurry flow rate have little effect on alleviating the in-plane uniformity deteriorating. The same situation also occurred in 2-inch wafer polishing. This phenomenon occurred because that the line speed of each point in wafer is different determining the different polishing rate of each point. The longer the polishing time, the more obvious the thickness difference due to the difference in polishing speed. Therefore, in bonding process, reducing the overall polishing amount as much as possible is necessary while smoothing the local level difference.

3. Surface roughness

(2 cm × 2 cm chip)

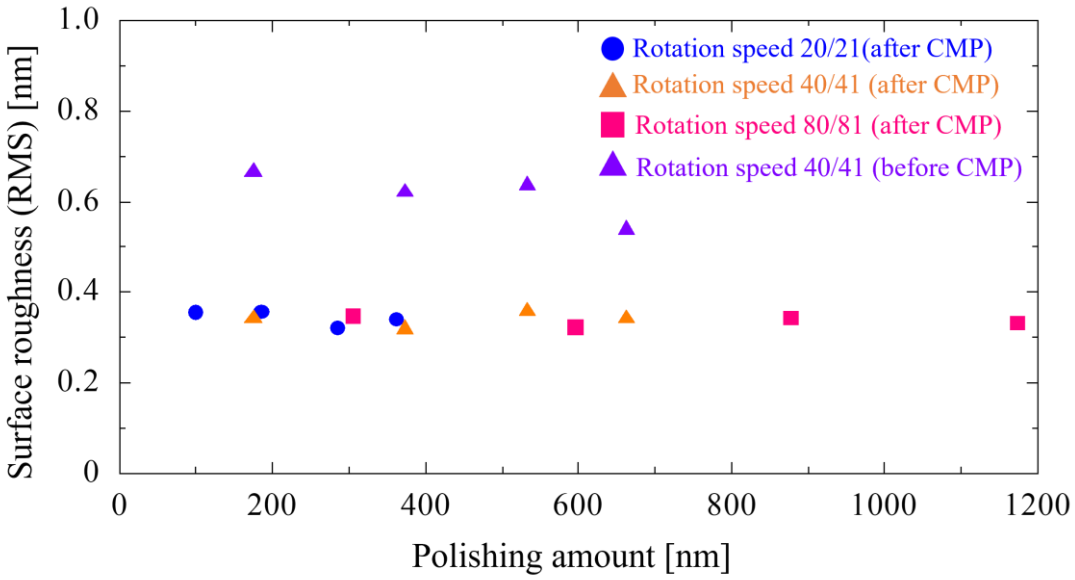


Fig. 4.14 Surface roughness dependence on polishing amount

Semi-Sperse 25 (SS25) slurry was used in the experiment. Figure 4.14 shows the surface roughness after polishing. The RMS was 0.3 ~ 0.4 nm after polishing whatever the polishing amount is even with different rotation speed. In addition, the slurry flow rate and pressure also have little effect on surface roughness in other experiments. When

the slurry changed to ILD4221, the surface roughness after polishing was 0.4 ~ 0.5 nm. based on the data above, the surface roughness only determined by slurry itself.

4. Polishing with local thickness level difference.

(2-inch wafer)

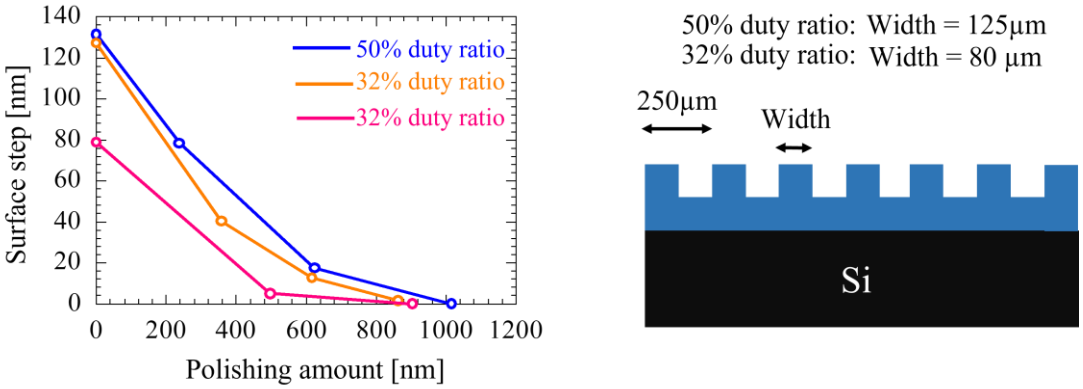


Fig. 4.15 Surface step vs polishing amount

After checking the basic conditions of polishing, a 2-inch wafer with local thickness level difference on the surface to simulate the real situation was used in the polishing experiment. The surface pattern is shown in Fig. 4.15. 2-μm-thick SiO_2 was deposited by PECVD at first and the pattern was formed by photolithography and RIE dry-etching. The period was set as 250 μm which is the same distance with two laser islands in real CAD design. Different initial step and different duty ratio are parameters in the experiment. The polishing rate is fast at first, then gradually lowering with the polishing amount increasing. This is because the rectangle-like shape becomes sine wave shape as polishing continues, making the flattening process difficult. When the initial step is 130 nm, over 1000 nm polishing amount is needed. In this time, the thickness different between edge and center of the 2-inch wafer was over 100 nm, which shown in Fig. 4.16. The surface shape of 2-inch wafer is shown in Fig. 4.17. The relatively flat area becomes large comparing with the 2 cm × 2 cm chip because of the large size of wafer.

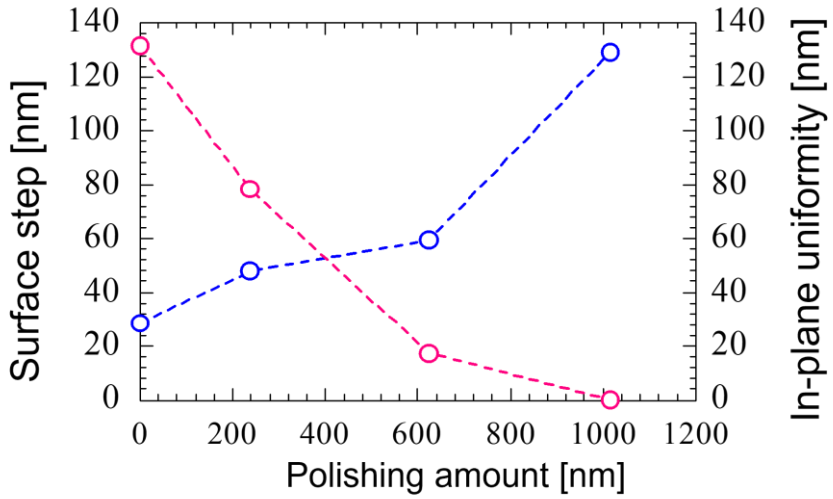


Fig. 4.16 Surface step and in-plane uniformity vs polishing amount, the in-plane uniformity was estimated by measuring 17 points distributed on 2-inch wafer and calculating the thickness difference between maximum value and minimum value

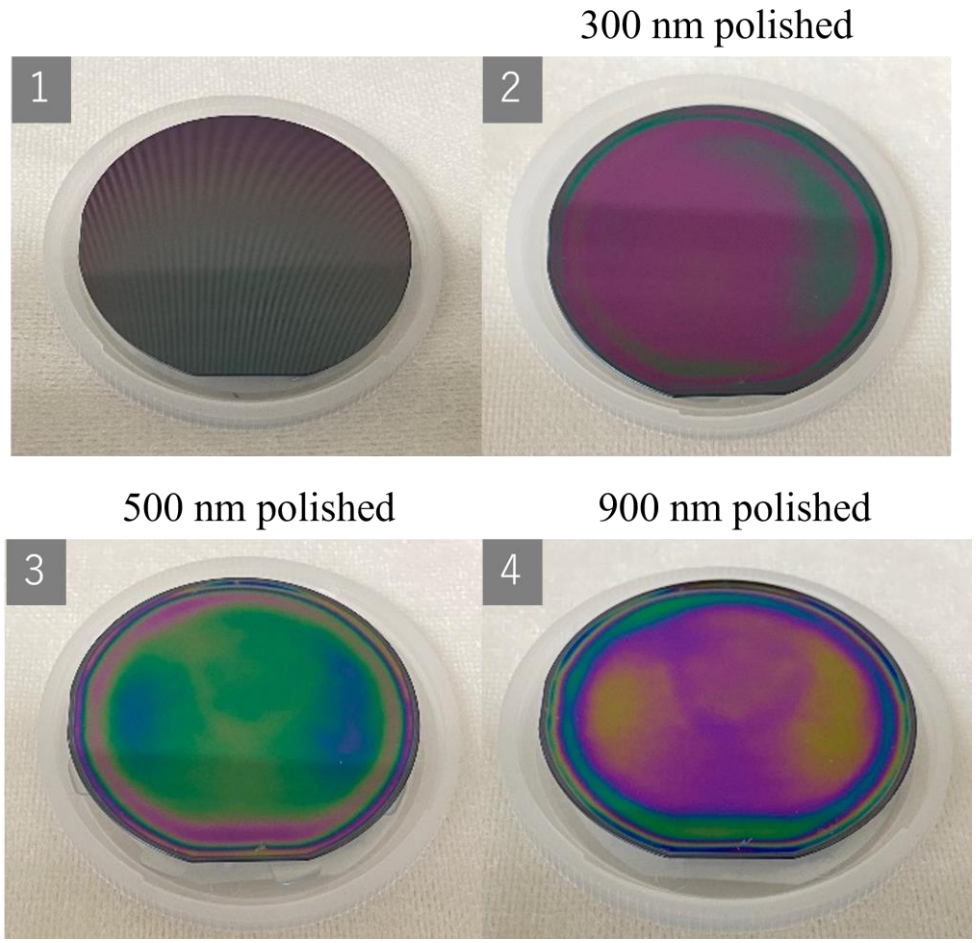


Fig. 4.17 Surface shape while polishing in 2-inch wafer

5. Slurry cleaning after polishing

After polishing, the slurry cleaning is important. It affects the surface roughness. Several methods were tried to remove the surface slurry on wafer listed in Table 4.4.

Table 4.4 several methods for cleaning slurry

(A)	DI water rinse 3 min
(B)	Acetone boiling 10 min + Acetone ultrasonic cleaning 5 min
(C)	CMP-B01 ultrasonic cleaning 15 min + DI water rinse 3min
(D)	PVA sponge brush (DI water)
(E)	PVA sponge brush (CMP-B01)

The CMP-B01 in (C) and (E) is the alkaline-type CMP cleaning solution. Ultrasonic frequency in (B) and (C) was set as 40 kHz. The Megasonic cleaning system supports the PVA sponge brush cleaning using DI water. The brush cleaning using CMP-B01 in (E) is handling by hand. The cleaning results are shown in Fig. 4.18. The results indicate that the brush is a very effective method even though the CMP-B01 is not used. The common methods like DI water rinse and Acetone ultrasonic cleaning cannot remove the alkaline-type SiO_2 polishing slurry.

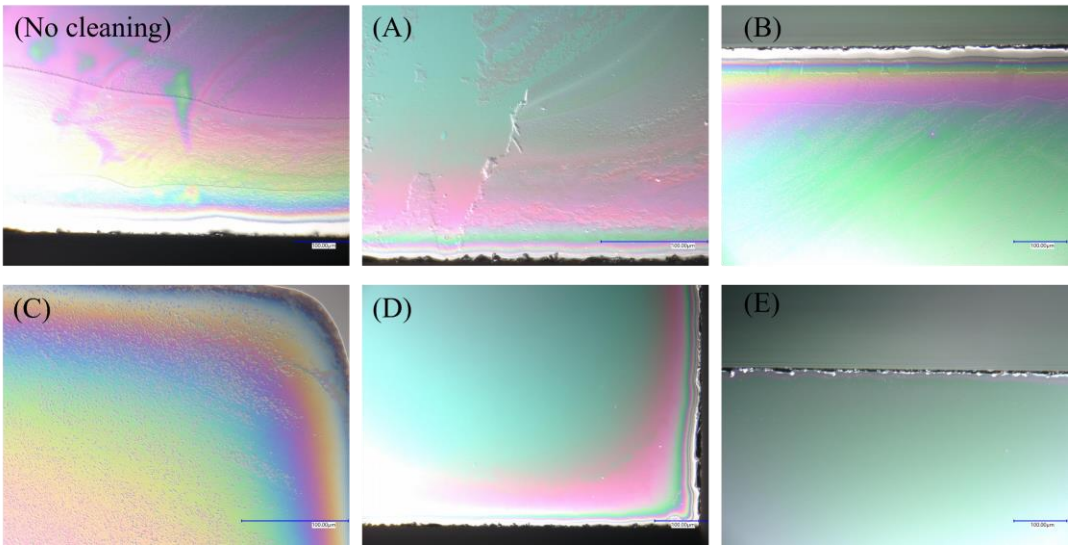


Fig. 4.18 Optical microscope photos of CMP cleaning

6. Polishing and bonding

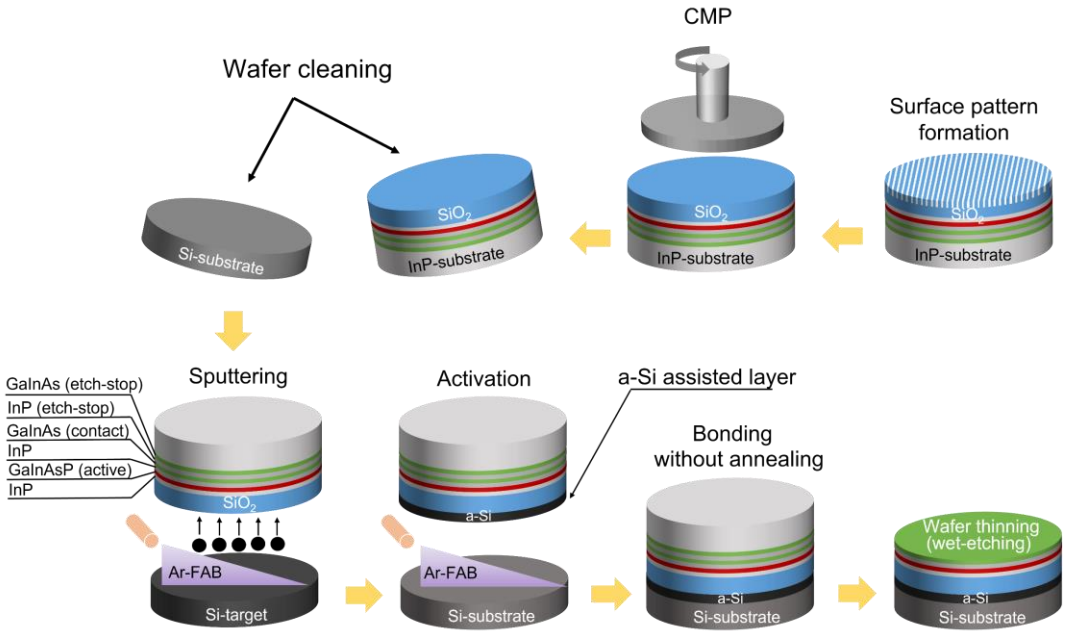


Fig. 4.19 Process flow combining CMP and SAB

In the previous subsections, the basic CMP parameters to the in-plane uniformity and surface roughness were investigated. The local thickness level difference polishing and cleaning after polishing were also discussed. Finally, Combining the CMP and SAB which investigated in Chapter 3 is the most important thing towards membrane laser fabrication. Figure 4.19 shows the procedure of process. First, an epitaxial wafer includes active layer and etch-stop layers deposited 2-μm-thick surface SiO_2 on surface with 130 nm thick triangle-like pattern was prepared. Then, the CMP, wafer cleaning, and SAB was carried out. The process conditions are shown in Table 4.5 ~ 4.7. The photos after wafer thinning using selective wet-etching are shown in Fig. 4.20. Two samples show the large bonding area even though there is >100 nm thickness different exists between center and edge (and the color difference on surface was due to the thickness difference of SiO_2), which means the ~100 nm in-plane uniformity distributed in 2-inch wafer has little effect to the direct bonding process.

Table 4.5 CMP conditions

Rotation (head / platen)	41/40 rpm
Slurry	SS25
Slurry flow	100 ml/min
Pressure	50 g/cm^2
Polishing rate	100 ~ 130 nm/min
Polishing time	10 min
Slurry cleaning	PVA sponge brush (hand and megasonic system)

Table 4.6 wafer cleaning before bonding conditions

Si wafer	
H_2SO_4	2 min
DI water rinse	10 min
7% BHF	1 min
DI water rinse	5 min
Megasonic	1 min
Baking	400 sec at 200˚C
Epi wafer	
Megasonic	1 min
Baking	400 sec at 200˚C

Table 4.7 surface activated bonding conditions

Sputtering irradiation	
Current	100 mA
Voltage	1.5 kV
Time	15 min
Gas flow	Ar, 30sccm
Si substrate surface-activate irradiation	
Current	50 mA
Voltage	1.2 kV
Time	90 sec
Gas flow	Ar, 30sccm
Bonding	
Temperature	Room-temperature
Time	5 min
Load value	500 kgf
Chamber pressure	< 10^{-5} Pa

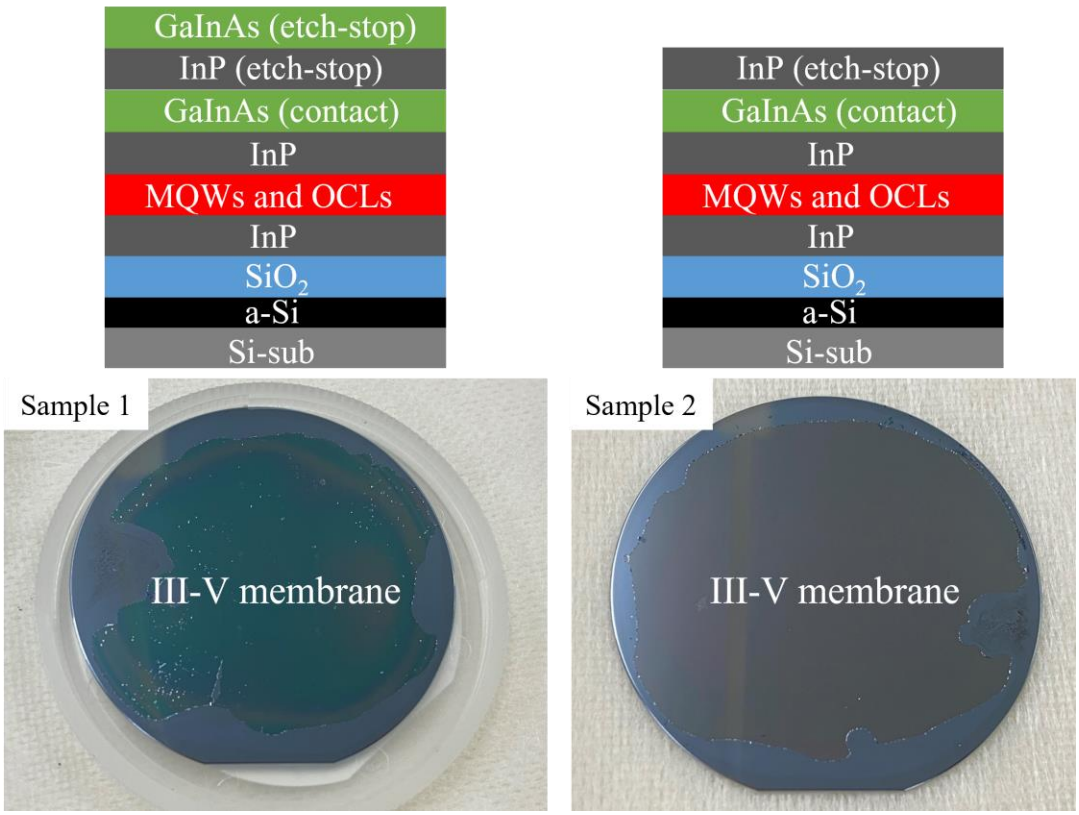


Fig. 4.20 Bonding area after CMP – SAB process

4.2.3 Grating formation using dry etching

As the bonding process changed in the laser fabrication, the layer under SiO_2 was changed, which leads to the EB-lithography change because of the changed back scattering of electron. A test 2-inch bonded wafer was prepared for EBL condition check.

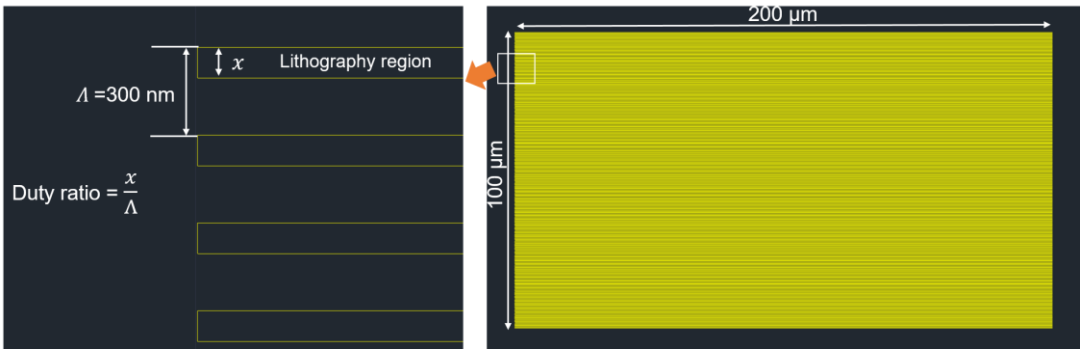


Fig. 4.21 Check pattern design in CAD

Figure 4.21 shows the check pattern design in CAD. For easily observing and sampling in SEM observation, the whole pattern was designed in 200 μm long and 100 μm width. The grating pitch was fixed as 300 nm and x is the width of lithography region. The duty ratio was defined as x/Λ. In design, 30%, 35%. 40%, 45% and 50% was used. And when doing the EB lithography, the exposure intensity of 110, 120, 130, 140, 150, 160, 170, 180, 190, and 200 μC/cm^2 were used. Figure 4.22 shows the whole pattern and samples after dicing.

The condition check experiment procedure of EB-lithography and dry-etching were

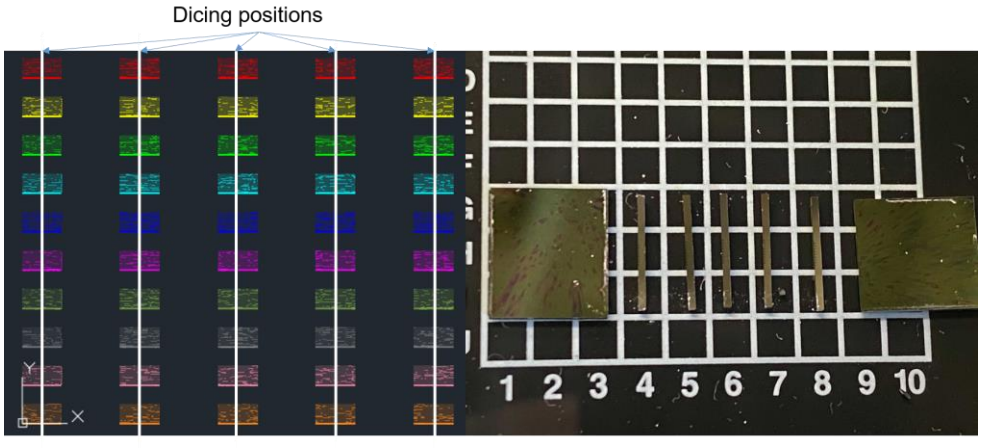


Fig. 4.22 Whole check pattern and samples after dicing

shown in the following:

1. Wafer bonding (SAB) and wafer thinning.
2. 25-nm-thick SiO_2 mask deposition by PECVD.
3. ZEP-520A spin-coating (1000 rpm for 3 sec, 6000 rpm for 120 sec), ~300 nm
4. Baking (180 ℃ for 20 min in oven)
5. Lithography (exposure intensity: 110 ~ 200 μC/cm^2) using JBX-6300UA (50 keV, 100 pA) (Numerical Proximity Effect Correction (PEC) was used for pattern correction in each exposure intensity, short pitch was also changed with the exposure intensity increasing)
6. Development (ZED-N50: 30 sec, IPA: 60 sec)
7. RIE (CF_4: 10 sccm, Pressure: 1 Pa, Power: 25 W, Time: 7 min) for 25-nm-thick SiO_2 mask transforming.
8. RIE (CH_4: 10 sccm, H_2: 40 sccm, Pressure: 6 Pa, Power: 100 W, Time: 90 sec) for InP transforming.

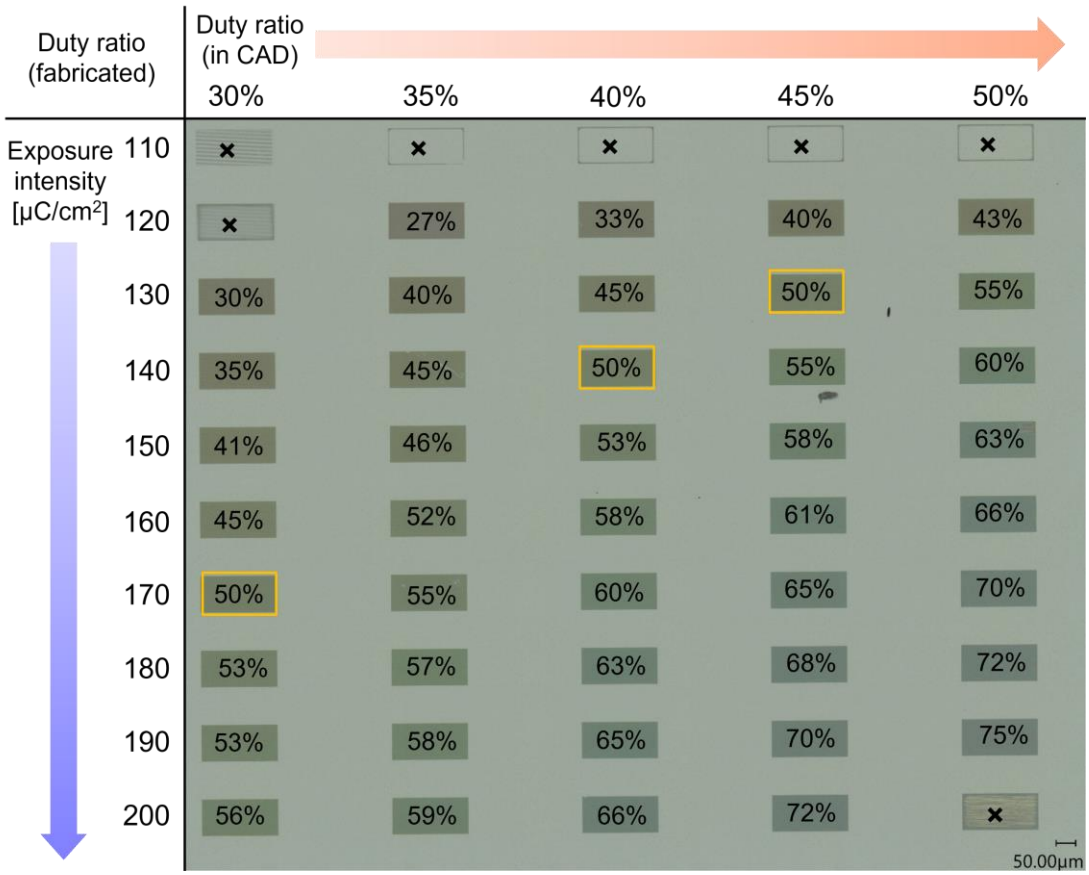


Fig. 4.23 Optical microscope photo of check pattern after dry-etching

Figure 4.23 shows the results of the condition check. The picture was taken after InP etching. The duty ratio was measured from the top view of SEM images. For fabricating the 50% duty ratio grating, there are three points conditions can be chosen. They are (130 μC/cm^2, 45%), (140 μC/cm^2, 40%) and (170 μC/cm^2, 30%). Considering the uniformity of verticality pattern, (130 μC/cm^2, 45%), (140 μC/cm^2, 40%) are acceptable. Figure 4.24 shows the SEM images. After 90 sec etching, near 66 nm InP was etched in a single etching condition.

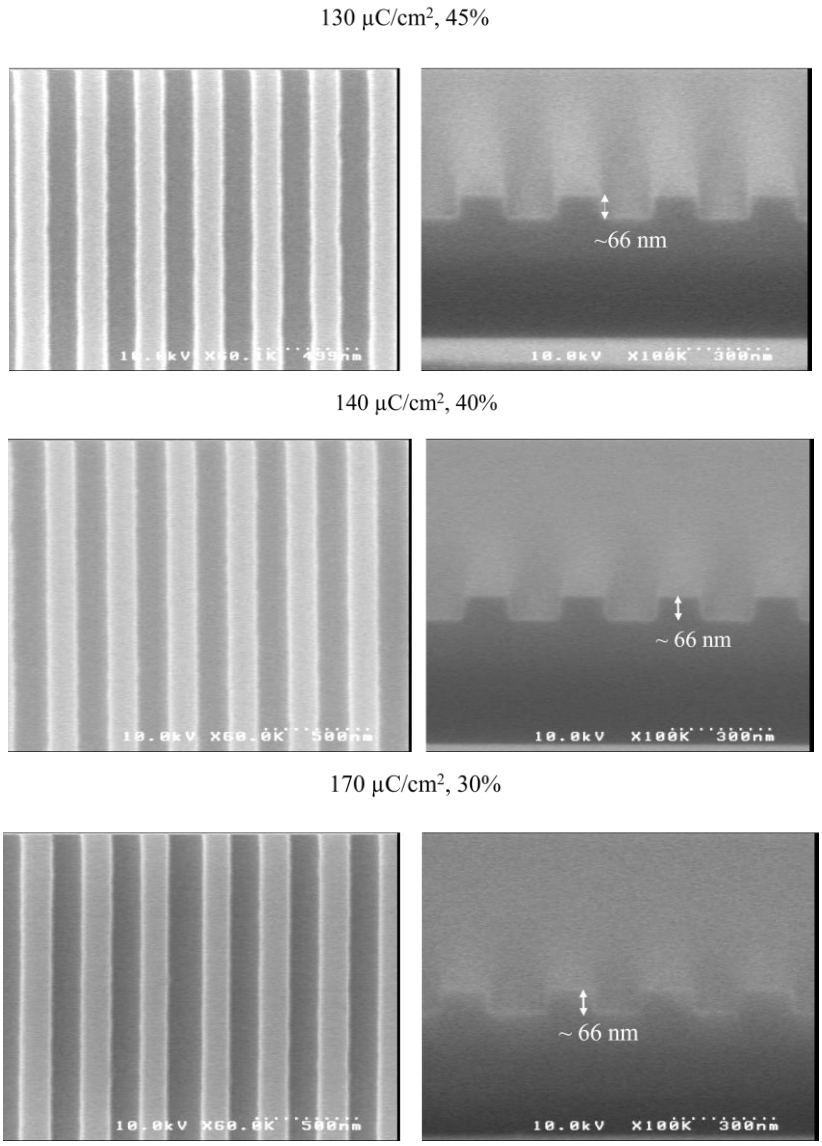


Fig. 4.24 SEM images of fabricated grating of 50% duty ratio

4.2.4 Laser fabrication procedure

The initial wafer is grown by OMVPE. The Table 4.8 gives the previous initial wafer structure for fabrication of membrane Fabry-Perot (FP) laser. The initial wafer consisted of a 267-nm-thick GaInAsP/InP core layer including a GaInAsP five-quantum-well active layer (5.4 nm/well) and optical confinement layers, a *p*+-GaInAs contact layer (8×10^{18} cm^{-3}, 100 nm), a GaInAsP (λ = 1.3 μm) layer and GaInAs (un-doped, 300 nm), InP (undoped, 100 nm) etch-stop layers.

Table 4.8 Initial wafer layer structure

Layer	Material	Wavelength [nm]	Thickness [nm]	Doping level [cm^{-3}]
InP protection	*u*-InP		10	
GaInAs protection	*u*-$Ga_{0.47}In_{0.53}As$		10	
Cap	*u*-InP		50	
u-OCL	$Ga_{0.21}In_{0.79}As_{0.46}P_{0.54}$	1200	15	
TS -0.15% barrier	$Ga_{0.26}In_{0.74}As_{0.49}P_{0.51}$	1200	10	
CS 1.0% well	$Ga_{0.22}In_{0.78}As_{0.81}P_{0.19}$	1520	5.4	
TS -0.15% barrier	$Ga_{0.26}In_{0.74}As_{0.49}P_{0.51}$	1200	10	
CS 1.0% well	$Ga_{0.22}In_{0.78}As_{0.81}P_{0.19}$	1520	5.4	
TS -0.15% barrier	$Ga_{0.26}In_{0.74}As_{0.49}P_{0.51}$	1200	10	
CS 1.0% well	$Ga_{0.22}In_{0.78}As_{0.81}P_{0.19}$	1520	5.4	
TS -0.15% barrier	$Ga_{0.26}In_{0.74}As_{0.49}P_{0.51}$	1200	10	
CS 1.0% well	$Ga_{0.22}In_{0.78}As_{0.81}P_{0.19}$	1520	5.4	
TS -0.15% barrier	$Ga_{0.26}In_{0.74}As_{0.49}P_{0.51}$	1200	10	
CS 1.0% well	$Ga_{0.22}In_{0.78}As_{0.81}P_{0.19}$	1520	5.4	
TS -0.15% barrier	$Ga_{0.26}In_{0.74}As_{0.49}P_{0.51}$	1200	10	
u-OCL	$Ga_{0.21}In_{0.79}As_{0.46}P_{0.54}$	1200	15	
Cap	*u*-InP		100	
1.3 Q	*p*-GaInAsP	1300	50	Be: 4×10^{18}
p-contact	*p*-$Ga_{0.47}In_{0.53}As$		100	Be: 8×10^{18}
InP etch stop	*u*-InP		100	
GaInAs etch stop	*u*-$Ga_{0.47}In_{0.53}As$		300	
Substrate	*n*-InP		350000	

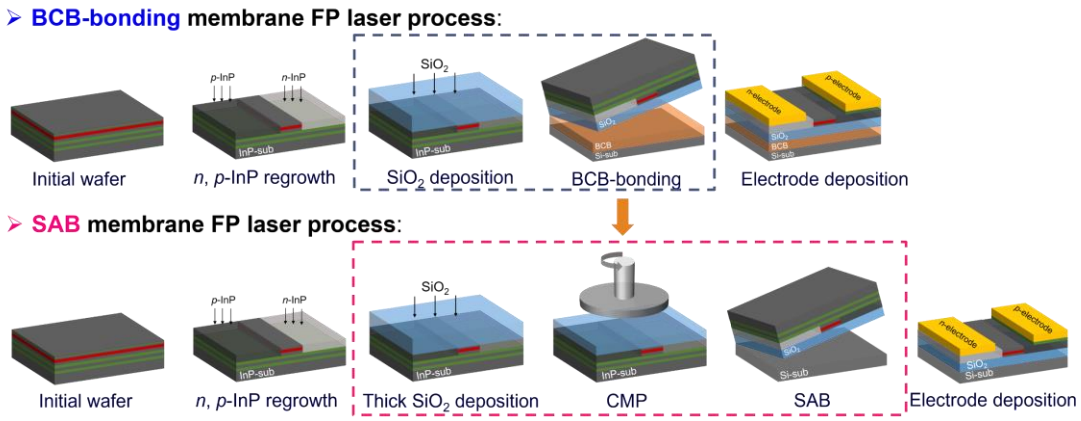


Fig. 4.25 Fabrication change by using BCB-free structure

The changing points were shown in Fig. 4.25. In BCB-bonding membrane laser process, 1-μm-thick SiO_2 cladding layer was deposited by PECVD and followed by BCB bonding. In SAB membrane laser process, 2-μm-thick SiO_2 cladding layer was deposited for CMP process. 1-μm-thick SiO_2 would be polished in CMP process, hance, the final thickness of SiO_2 was 1 μm in order to make a comparison of thermal resistance with precious work.

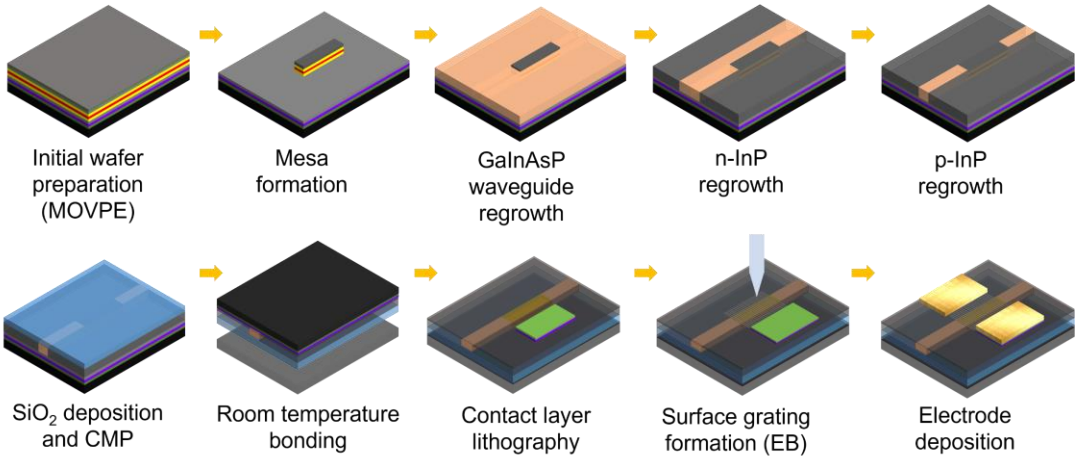


Fig. 4.26 Fabrication procedure of SAB membrane DFB laser

The SAB membrane DFB laser fabrication process was shown in Fig. 4.26. The grating formation was changed to before electrode deposition for obtained a flat ZEP film around active region after spin-coating. The process started with a mesa formation for active cavity. After three times of epitaxial regrowth by OMVPE, the surface of SiO_2 was flattened by CMP and followed by SAB. Then, the unnecessary layers were removed by selective wet-etching and remaining the contact layer. Next, surface grating was

fabricated by EB lithography and RIE dry-etching. After that, Au/Zn/Au p-electrode was evaporated by resistive thermal evaporation. Then, after annealing Au/Zn/Au up to 350 ˚C, Ti/Au n and p-electrode were evaporated by EB evaporation. The detailed process and fabrication condition were shown as follow (All the process was based on 2-inch wafer size):

(0) Initial wafer

The layer structure was shown in Table 4.8. For enhancing the high temperature characteristic of DFB laser, the thickness of quantum well was reduced to 5.4 nm. And for reducing the p-side contact resistance, a band tailing was down by introducing a 50-nm-thick GaInAsP (λ = 1.3 μm) between cap InP and p^+-GaInAs contact layer.

(1) Island masa formation

The fabrication process was started from the removal of protective cap layers. GaInAsP QWs island of 10-μm-width and L-μm-length was formed by combining dry-etching and we-etching. Firstly, 50-nm-thick SiO_2 mask was deposited on the wafer by PECVD using condition of Table 4.1. Then, OAP was spin-coated on the SiO_2 mask making surface hydrophobization to enhance adhesion (1st 1000 rpm, 3 sec, 2nd 6000 rpm, 60 sec). S1818 photoresist was then spin-coated on the surface (1st 1000 rpm, 3 sec, 2nd 6000 rpm, 60 sec). The island pattern was exposed by maskless photolithography system with i-line wavelength (365 nm) with the exposure power of ~ 80 mJ/cm^2 and speed of 3.6 mm/sec. MF320 developer was used for development (70~80 sec at room-temperature). After that O_2 ashing was followed for removing the residual resist. Secondly, pattern was transferred to SiO_2 by CF_4 RIE dry-etching using condition in Table 4.3. The S1818 then was removed by Acetone spray (No boiling). The etching of semiconductor was divided into two steps. First, CH_4/H_2 RIE dry-etching was performed by condition in Table 4.2 for removing100 nm u-InP and a little GaInAsP active layer. Second, a piranha solution (H_2SO_4:H_2O_2:H_2O = 1:1:40) was used for removing the rest GaInAsP. By controlling the wet-etching time, side etching amount can be controlled.

(2) OMVPE regrowth of the passive GaInAsP layer (λ = 1.22 μm)

The passive waveguide layer was selectively regrown around the GaInAsP by OMVPE. A Butt-joint built-in (BJB) structure was formed by precisely controlling the wet-etching time and regrowth time. The detailed condition investigation was shown in the previous work in[12]. After regrowth, the SiO_2 mask was removed by 7% buffered HF (BHF) for 1 min.

(3) Stripe mesa formation and *n*-InP regrowth

A 7-μm-width stripe mesa was formed by using the same lithography and etching method described in (2). The *n*-InP was grown on bottom *p*-InP layer at 600 ˚C.

(4) Stripe mesa formation and *p*-InP regrowth

A 125-μm-width stripe mesa was formed by using the same lithography method for flat structure. An 80-μm-width stripe mesa was used for buried-ridge-waveguide (BRW) structure. In this step, the regrown *n*-InP and bottom 100-nm-thick *p*-InP were removed together by HCl:CH_3COOH = 1:3 solution. The *p*-InP would be grown on the GaInAsP (λ = 1.3 μm) layer.

(5) Metal mark formation

In order to see a clear mark in lithography process after bonding, the metal marks, including EB mark and maskless mark, were deposited before bonding. No SiO_2 mask was need in this process. First, AZ5218 photo resist was spin-coated on the wafer surface (1^{st} 1000 rpm, 3 sec, 2^{nd} 5000 rpm, 60 sec). The metal mask pattern was exposed by maskless photolithography system with i-line wavelength (365 nm) with the exposure power of ~ 25 mJ/cm^2 and speed of 3.6 mm/sec. A reversal baking at 120 ˚C on hot plate for 120 sec was followed. Then, a full exposure with exposure power of 250 mJ was carried out. MIF300 developer was used for development (60 sec in room temperature). The dry-etching was down until bottom 100 nm InP layer was removed. Hance, after bonding, the mark would appear at surface. A Ti/Au (25 nm/200 nm) was evaporated by

EB evaporation.

(6) Chemical mechanical polishing

2-μm SiO_2 was deposited by PECVD, then, the wafer was polished by using condition Table 4.5. ~ 1 μm SiO_2 would be polished. After polishing, the wafer was cleaned by PVA sponge brush by hand and megasonic system. Surface condition was measured using a probe-scan surface profiler and AFM.

(7) Surface activated bonding

The wafer cleaning condition and bonding condition used the Table 4.6 and Table 4.7. after bonding, 350-μm-thick InP substrate was removed by HCl for approximately 1 hour. GaInAs etch-stop layer was removed by H_2SO_4:H_2O_2:H_2O = 1:1:40 for 6 min, and InP etch-stop layer was removed by HCl:CH_3COOH = 1:4 for 1 min.

(8) Selective remove contact layer

A 250-nm-thick SiO_2 mask was deposited by PECVD. The p^+-GaInAs contact layer was only remined on p-InP around active region. The lithography method was the same as described in (2). SiO_2 and semiconductor transfer was down by wet-etching.

(9) Grating formation by EB lithography

~ 370-nm-thick ZEP was spin-coated on the substrate (1st 1000 rpm, 3 sec, 2nd 6000 rpm, 120 sec). Then, baking for 20 min in oven. The grating was patterned by Electron-Beam lithography with a dose of 140 μC/cm^2. The pattern transform method was the same as described in **section 4.2.3**. InP dry-etching time of 75 sec was used for 50 nm etching.

(10) Au/Zn/Au deposition

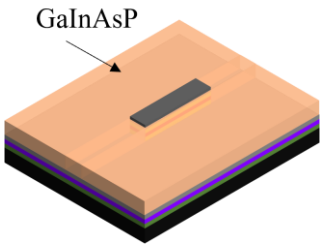
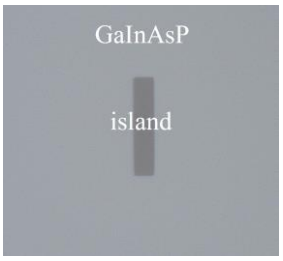
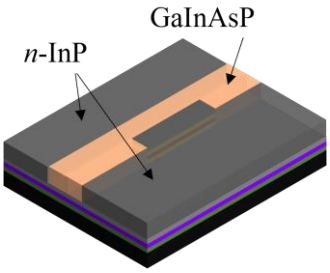
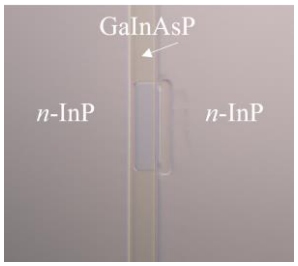
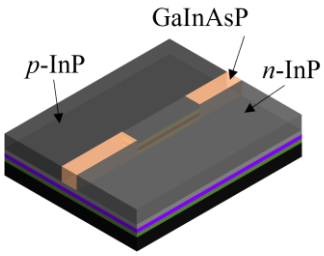
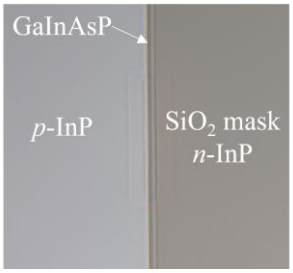
The pattern was formed on p-side InP by using AZ5218 and maskless lithography, the condition was the same as described in (5). No SiO_2 mask was needed. Before deposition, the surface of p^+-GaInAs was processed by H_2SO_4:H_2O_2:H_2O = 1:1:40 for 3 sec to clean

the surface. Then, Au/Zn/Au (25/50/300 nm) metal layers were evaporated by resistive thermal evaporation. After lift-off, the wafer was annealed at 350 ˚C for 1 min in N_2 atmosphere in order to diffuse Zn.

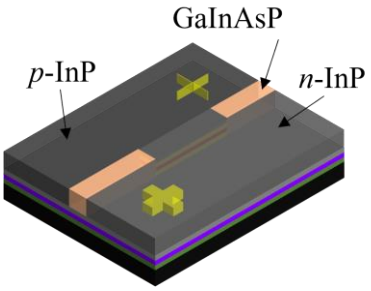
(11) Ti/Au deposition

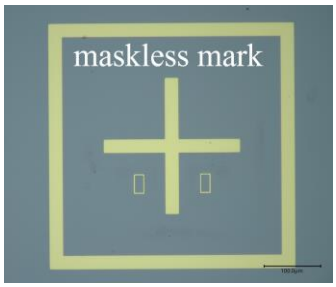
The pattern was formed both p-side and n-side of InP, the method was the same as described in (5). Before deposition, top p-InP was removed by dry-etching. Then, Ti/Au (25/200 nm) were deposited by EB evaporation.

Table 4.9 Optical microscope images for each step of fabrication

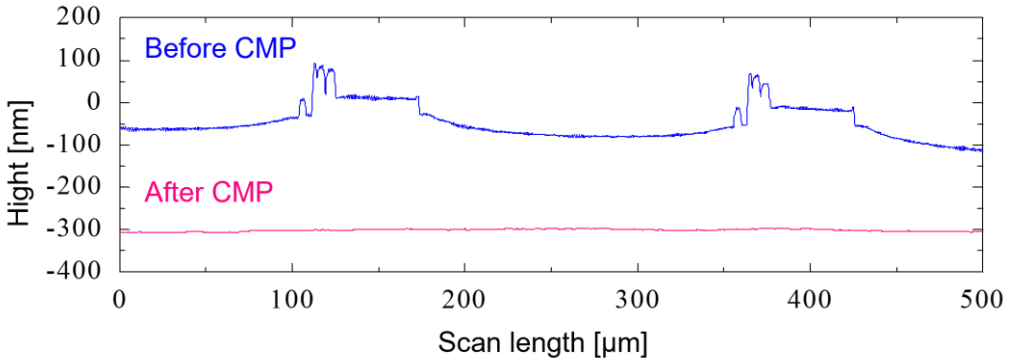
Process flow	Schematic	Optical microscope image
1. GaInAsP passive waveguide regrowth		
2. *n*-InP regrowth		
3. *p*-InP regrowth		

4. Metal mark formation

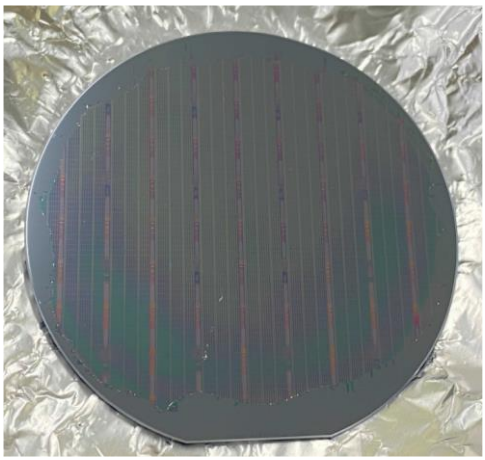


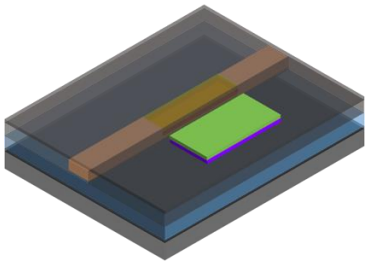
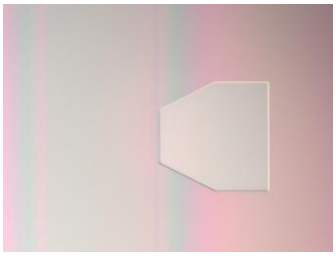
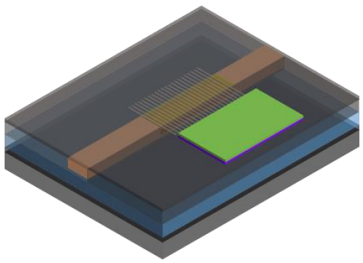
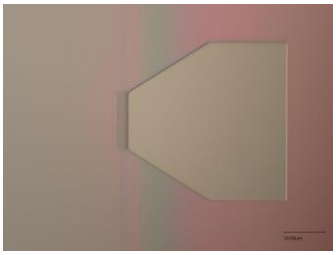
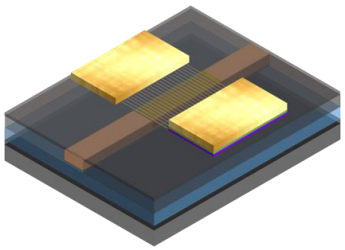
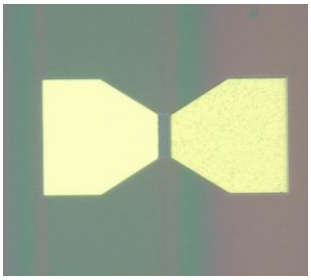


5. CMP



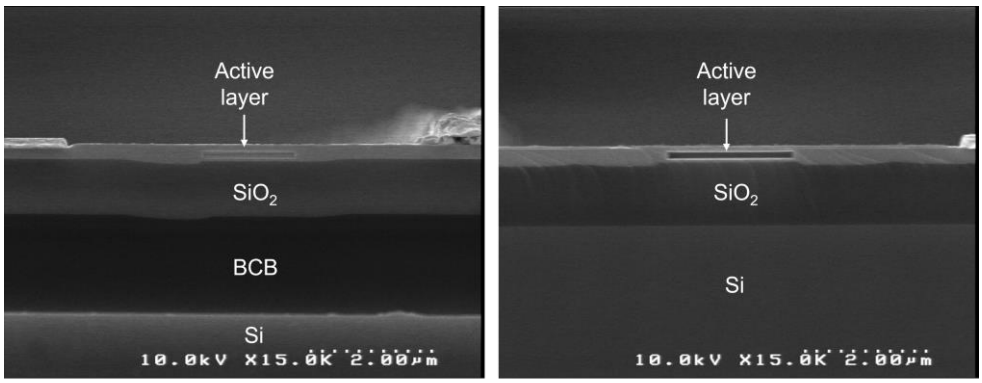
6. Surface activated bonding



7. Contact layer removal		
8. Grating formation		
9. Electrodes evaporation		

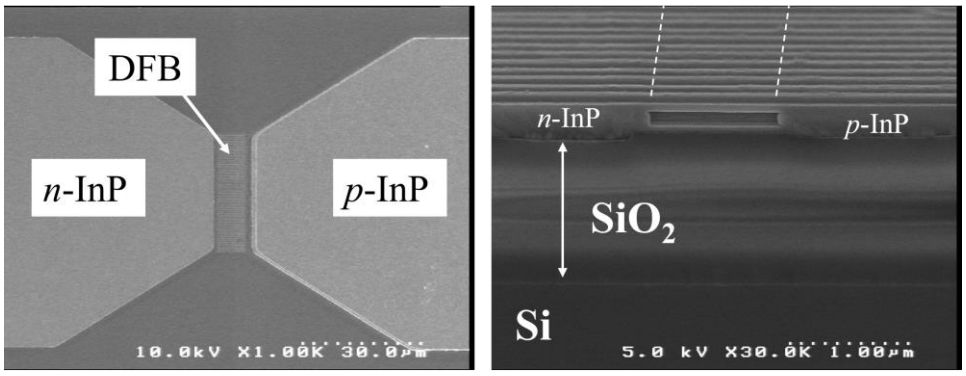
***Process for SAB membrane DFB laser**

Figure 4.27 shows the SEM images of BCB-bonding type and SAB type. A flat bonding interface can be seen in Fig. 4.27 (b) thanks to CMP process and no threading dislocation was observed. The SiO_2 was near 1 μm at both BCB-bonded and SAB membrane laser. Figure 4.28 shows the SEM images of fabricated membrane DFB laser. The grating and BJB structure were successfully formed. The p and n-electrode were deposited at two sides of active region, which formed a lateral current injection (LCI) structure.



(a) (b)

Fig. 4.27 SEM images of (a) BCB bonding type (b) SAB type



(a) (b)

Fig. 4.28 SEM images of (a) top view of DFB laser (b) cross sectional view of DFB

4.3 Low thermal resistance membrane laser

In this section, membrane laser with low thermal resistance would be introduced. It contains 500-nm-thick thin BCB bonded membrane DR laser, membrane FP laser and membrane DFB laser bonded by surface activated bonding (so-called "SAB membrane FP laser" and "SAB membrane DFB laser"). For higher temperature operation, Bragg wavelength detuning was used to compensate the gain in high temperature. The results show that 110˚C CW operation of SAB membrane DFB laser was obtained with 20 nm detuning value.

4.3.1 Thin BCB bonded membrane DR laser

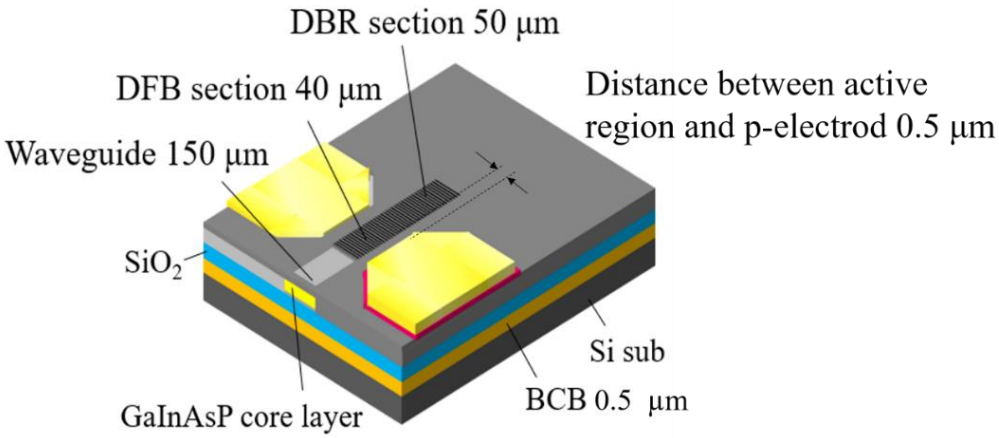


Fig. 4.29 Structure of fabricated membrane DR laser with thin BCB layer

The fabricated membrane DR laser was characterized in terms of light output power and lasing spectrum in different temperature. High temperature operation and low thermal resistance were experimentally confirmed. As calculated in Chapter 2, for reducing the thermal resistance of membrane laser, thin BCB layer and short distance between p-electrode and active region was used in this fabrication. The device structure is shown in Fig. 4.29. In this structure, While the thickness of the BCB was 2 μm and the distance between the active region to the p-electrode was 3 μm in our previous report[13]-[14], this time both of them were reduced to 0.5 μm. Others, the device consists of a 0.8 μm stripe width, 40 μm DFB region, 50 μm DBR region, 150 μm front waveguide and with 50-nm deep surface grating which corresponds to a grating coupling coefficient of around 1800

cm^{-1}. Figure 4.30 shows the lasing characteristics of fabricated membrane DR laser. 0.3 mA threshold current was obtained, which is almost the same as the previous work[13]. The external differential quantum efficiency was calculated as 10.9%. And a differential resistance of 375 Ω, which was about 1/3 of the previous report[13], was obtained thanks to the shortening of the p-electrode distance. Figure 4.31 shows the wavelength spectrum in different temperature, a 34 dB SMSR was obtained in this device.

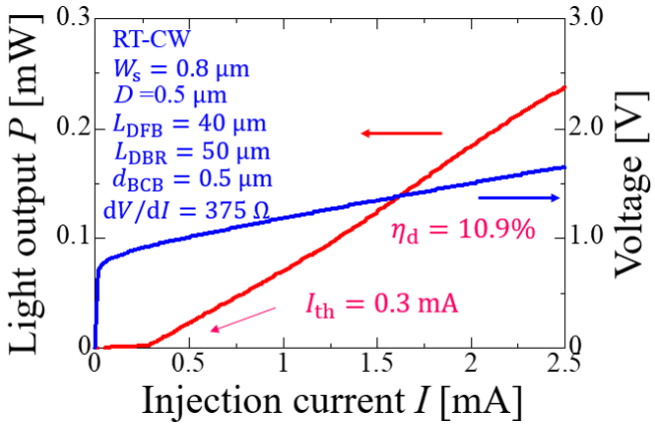


Fig. 4.30 Measured I-L-V characteristic of membrane DR laser

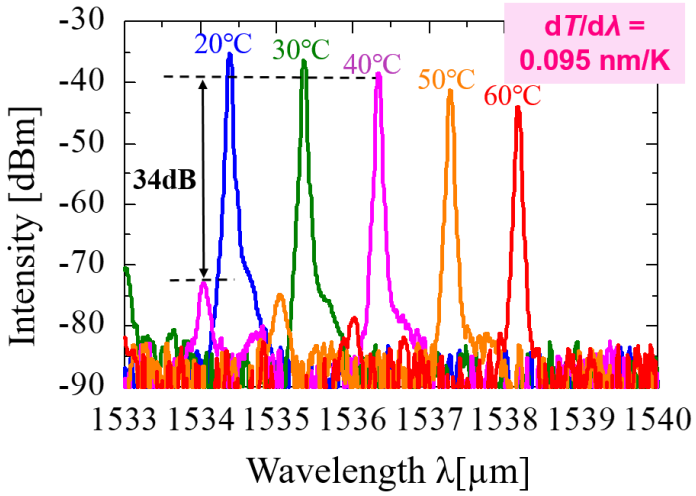


Fig. 4.31 Lasing spectrum in different temperature

Figure 4.32 shows the temperature dependence of the current-light output characteristics. Even though some mode jumps attributed to the reflection from the front facet (approximately 20% reflectivity) were observed, the DR laser operated up to 100 ºC under a continuous-wave (CW) condition.

Figure 4.33 (a) shows the temperature dependence of the lasing wavelength under a fixed injection current of 1 mA (CW condition). The wavelength varied almost linearly with the temperature and the slope of 0.095 nm/K was quite similar to 0.098 nm/K of the

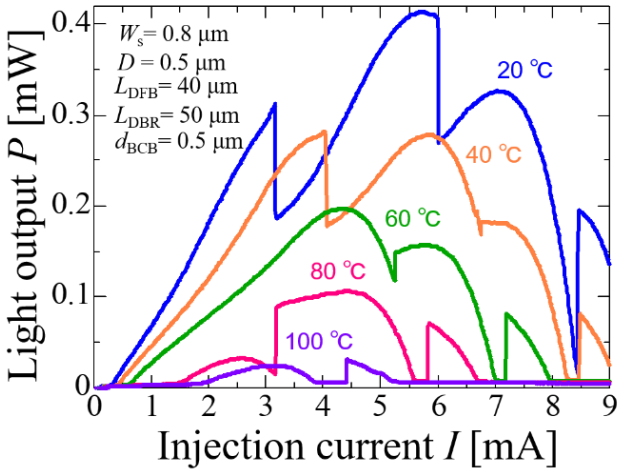


Fig. 4.32 Current-light output characteristics of measured membrane DR laser at various temperatures under a CW condition.

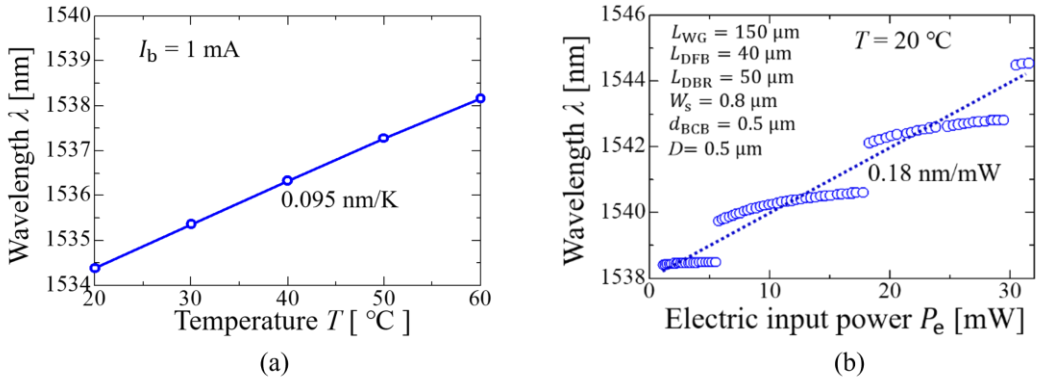


Fig. 4.33 (a) Temperature dependence of the lasing wavelength measured at a fixed injection current of 1 mA (b) Lasing wavelength as a function of input electric power measured at 20 °C. An interpolated slope including mode jumps was 0.18 nm/mW.

previously reported one[13] and conventional GaInAsP/InP DFB and DR lasers. Figure 4.33(b) shows the lasing wavelength as a function of input electrical power (a product of the injected current and the bias voltage) between 0 to 32 mW under a fixed temperature of 20ºC. In this device, light output is small compared with input power, so the dissipated power (IV-P_{out}) is almost the same as input power. The averaged slope including some mode jumps was 0.18 nm/mW, which was around 1/3 of the previously reported one (0.52 nm/mW), and the thermal resistance was estimated to be around 1900 K/W (0.18 nm/mW / 0.095 nm/K) which was 1/3 of that in [13].

However, in low input electrical power range (< 6 mW, Fig. 4.34), the slope was interpolated to be 0.019 nm/mW, which was very small (1/27) compared with that in[13]. This may be attributed to not only reduced electric resistance (by short distance between p-electrode and active region) and reduced thermal resistance (by thin BCB), but also a coupled cavity effect and heat propagation with the 150-μm long front waveguide section which is immune from the refractive-index variation due to an injection current into the DFB section.

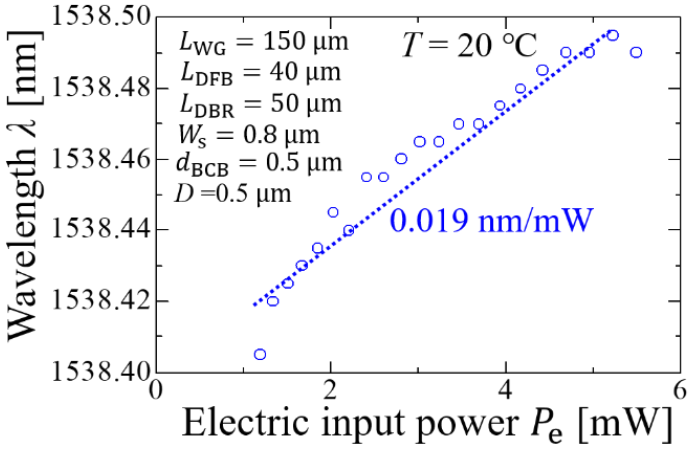


Fig. 4.34 Lasing wavelength as a function of input electric power of less than 5.5 mW where longitudinal lasing mode was fixed.

4.3.2 Membrane FP laser by Surface Activated Bonding

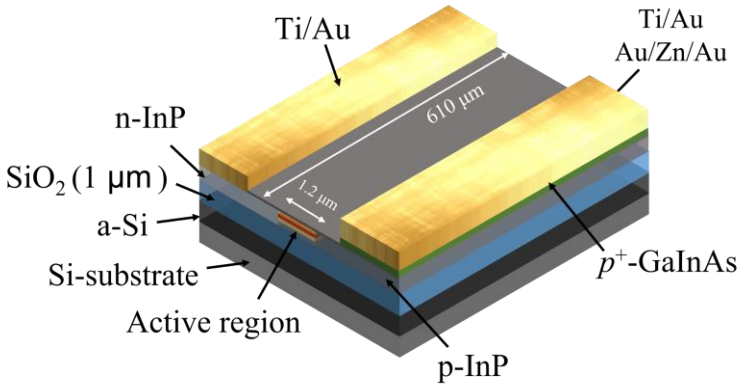


Fig. 4.35 Structure of fabricated SAB membrane FP laser

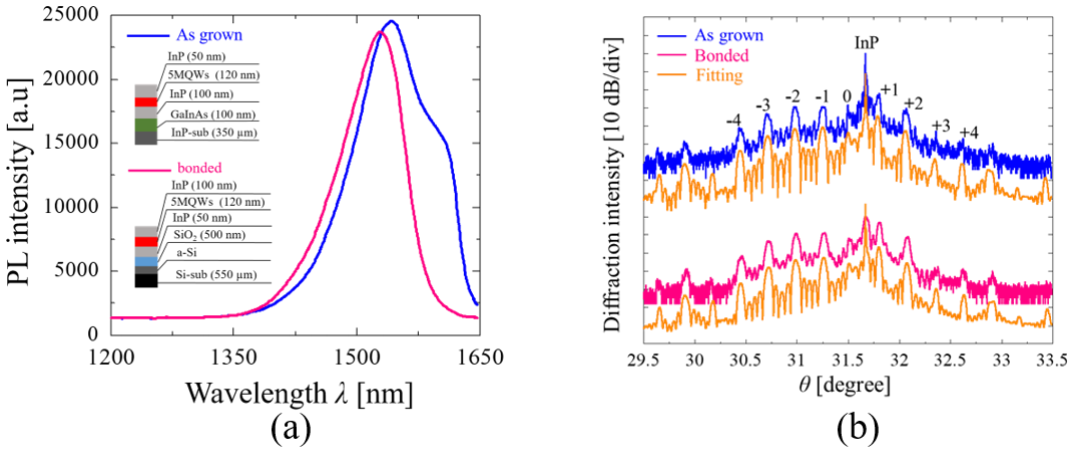


Fig. 4.36 MWQs quality check after bonding using a test wafer (a) PL peak wavelength intensity of as grown and after wafer thinning. (b) XRD measurement.

The SAB membrane FP laser used a conventional layer structure in initial epitaxial wafer, which did not include the λ = 1.3 μm GaInAsP layer, the thickness of quantum well is 6 nm. Figure 4.35 shows the structure of the fabricated SAB membrane FP laser. The stripe width is 1.2 μm, and the cavity length is 610 μm. Figure. 4.36 shows the PL peak wavelength intensity and XRD measurement using a test wafer during fabrication process for confirming the quality of SAB. The small peak wavelength blueshift in Fig. 4.36 (a) was due to the compressive net strain relaxation when 350-μm-thick InP-substrate was removed, which was almost the same results with that discussed in Chapter 3. The peak

intensity reduction is not large as well. Based on the measurement in Fig. 4.36 (b), the relative positions of each satellite peaks were maintained after wafer thinning process, and a net strain in MQWs was reduced by 0.03% (0.50% to 0.47%) can be obtained based on the fitting results.

Figure 4.37 shows the *I-L* characteristics in room temperature of BCB bonded and SAB membrane FP laser. Two types of lasers were cleaved with similar cavity length. The stripe width of BCB bonded FP laser was 1.5 μm, and that was 1.2 μm in SAB membrane FP laser. The differential resistance of SAB FP laser is 2 times larger than that in BCB bonded one because of the large distance between electrode and active region. The external efficiency of SAB was also larger than BCB bonded device even they had a same threshold current about 5.5 mA. The reason is not from the laser structure but the external measurement error due to different thickness of Si substrate (150 μm in BCB bonded device and 550 μm in SAB device). Even with the problem of large differential resistance, the SAB FP laser had a larger optical saturation current representing a higher heat dissipation.

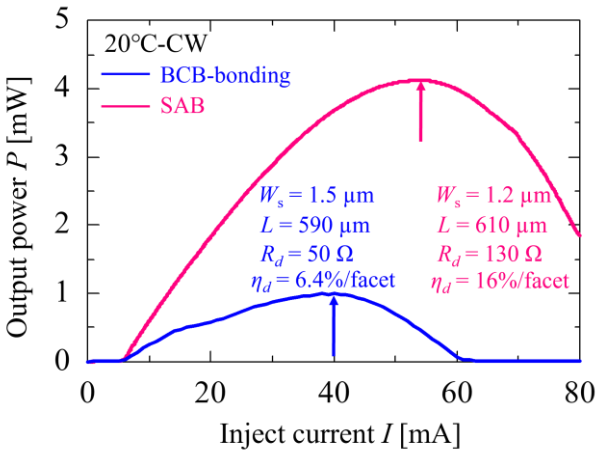


Fig. 4.37 *I–L* characteristics of devices fabricated via SAB and BCB-bonding.

Figure 4.38 shows the temperature characteristic of fabricated devices. Figure 4.3.8 (a) shows the stage temperature versus lasing wavelength. The slight difference in slope (0.54 nm/K and 0.52 nm/K) was due to the different surface temperature caused by different Si substrate thickness in two types of membrane FP lasers. Figure 4.38 (b) shows the heat dissipation power (the input power minus the output power) versus lasing wavelength at

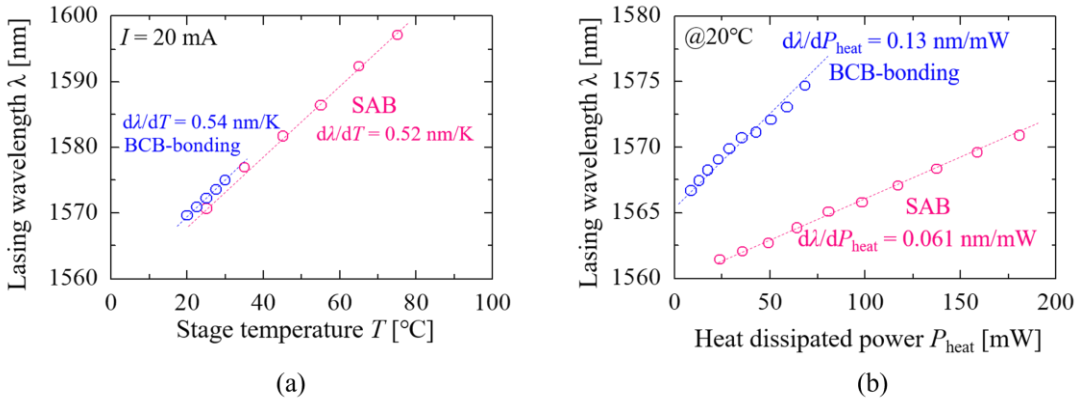


Fig. 4.38 Temperature characteristic of fabricated devices (a) Stage temperature versus lasing wavelength at 20 mA injection current. (b) Heat dissipated power versus lasing wavelength at fixed stage temperature of 20 °C.

a fixed stage temperature of 20 ºC. The average slope in SAB (0.061 nm/mW) was 2 times smaller than that in BCB bonded one (0.13 nm/mW), which shows a much stable wavelength characteristic. The thermal resistance can be calculated from the measured results as 240 K/W in BCB bonded membrane FP laser and 120 K/W in SAB membrane FP laser. This result was experimentally confirmed the 50% reduction by removing 2-μm BCB layer, which agrees with the simulation result.

Figure 4.39 shows the *I-L* characteristics of fabricated devices under various stage temperature. A higher maximum operation temperature of 95 °C was obtained in SAB device thanks to the lower thermal resistance even it had a higher differential resistance.

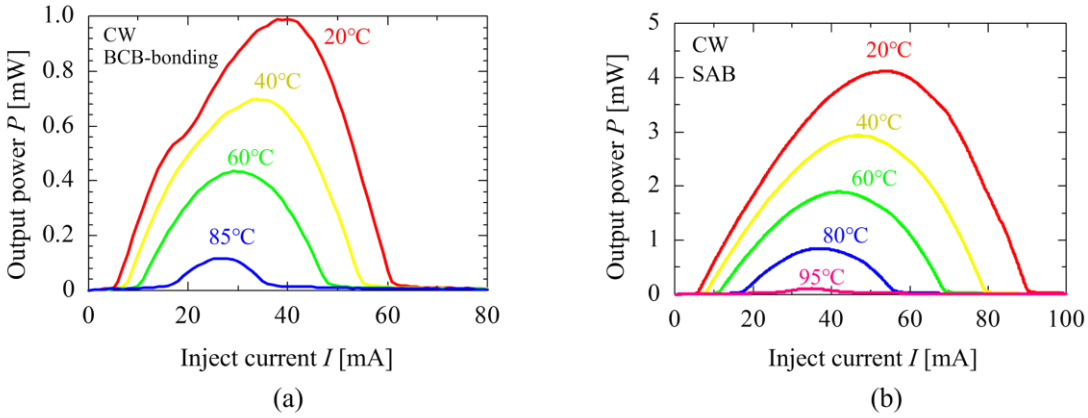


Fig. 4.39 *I-L* characteristics in various stage temperature of (a) BCB bonded membrane FP laser, (b) SAB membrane FP laser

4.4.3 Membrane DFB laser by Surface Activated Bonding

Figure 4.40 shows the fabricated SAB membrane DFB laser, which has a 70-μm-length DFB section, 0.7-μm-width stripe, 160-μm-length front waveguide, 270-μm-length rear

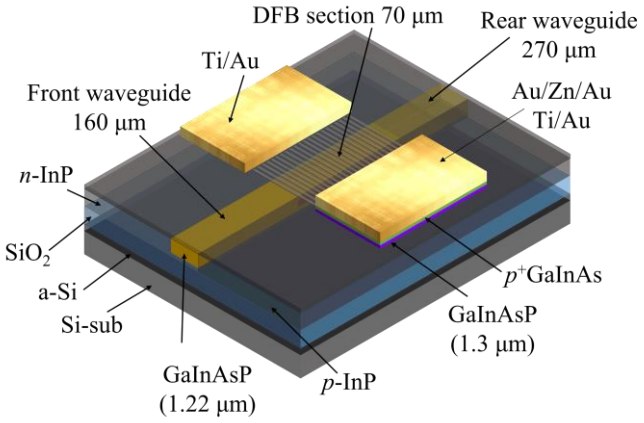


Fig. 4.40 Structure of fabricated SAB membrane DFB laser

waveguide and 40-nm-deep grating corresponding to a grating coupling coefficient κ of around 920 cm^{-1}. The layers of initial wafer were the same as Table 4.8. Figure 4.41 shows the *I-L-V* characteristics. The external differential quantum efficiency is 3.2%/facet, which is a little higher than the previous work with 80-μm-length DFB cavity[15]. The differential resistance is 950 Ω because it has a large distance between *p*-electrode and

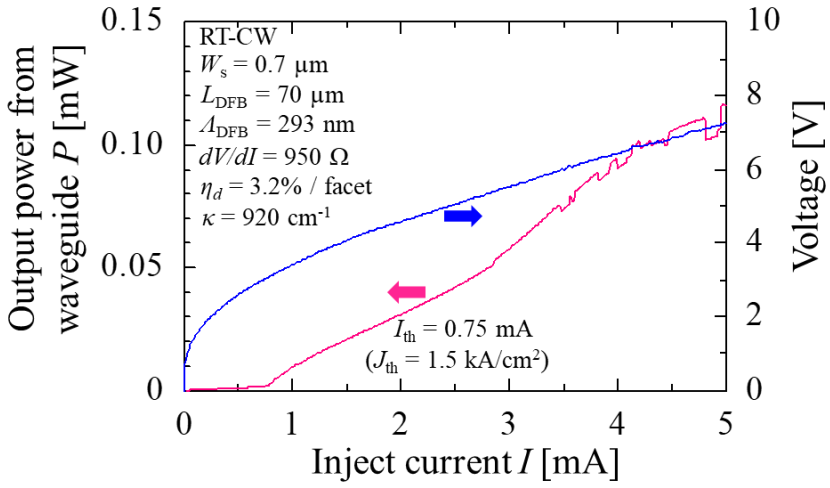


Fig. 4.41 *I-L-V* characteristic of SAB membrane DFB laser

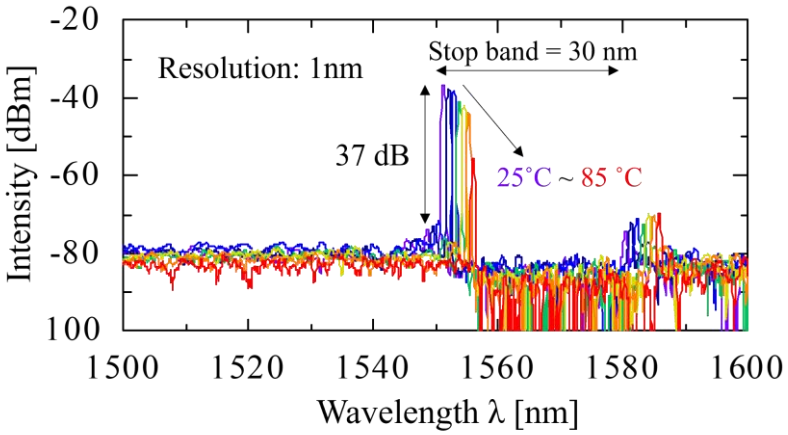


Fig. 4.42 Lasing spectrum under various stage temperature

active region of ~5 μm. The threshold current is larger than the previous work[15] due to the small κ and fabrication error which leads to a high scattering loss on the surface grating. With the problems above, it still has a large optical saturation current over 5 mA. Figure 4.42 shows the lasing spectrum under various stage temperature. A clear stop band of 30 nm can be seen and 37 dB SMSR was obtained at 25 °C.

Figure 4.43(a) shows the stage temperature versus lasing wavelength measured at a fixed injection current of 5 mA. A 0.08 nm/K slope was obtained, which was comparable with the BCB bonded membrane DFB laser using conventional active layers. Figure 4.43(b) shows a very small value (0.041 nm/mW) of lasing wavelength versus heat dissipated power at 25 °C, which is the 1/12.7 of previous work of 0.52 nm/mW, although

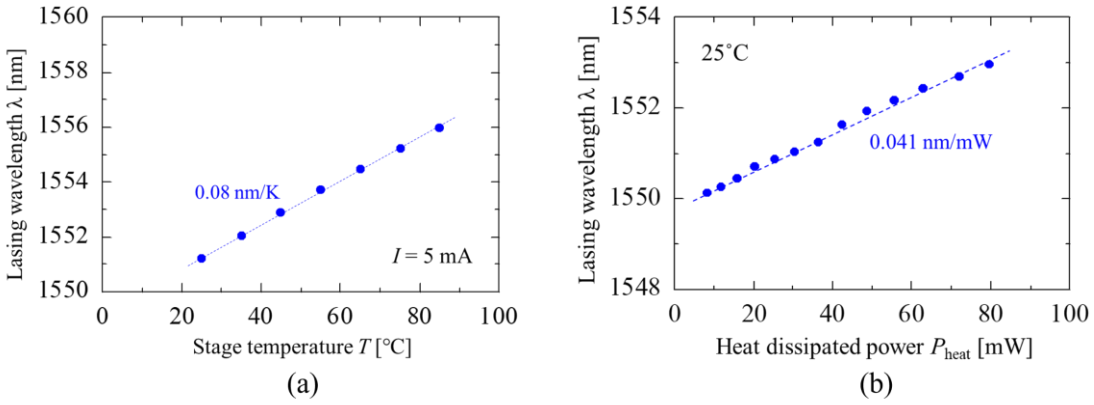


Fig. 4.43 Temperature characteristic of fabricated devices (a) Stage temperature versus lasing wavelength at 5 mA injection current. (b) Heat dissipated power versus lasing wavelength at fixed stage temperature of 25 °C.

the device has a little longer cavity length of 70 μm compared with the previous work of 40 μm. This is not only BCB layer was removed, but also the heat can diffuse to the front and rear waveguide. The thermal resistance was estimated to be around 510 K/W (0.041 nm/mW / 0.08 nm/K) which was 1/10 of that in [13] (5250 K/W).

【*Bragg wavelength detuning*】

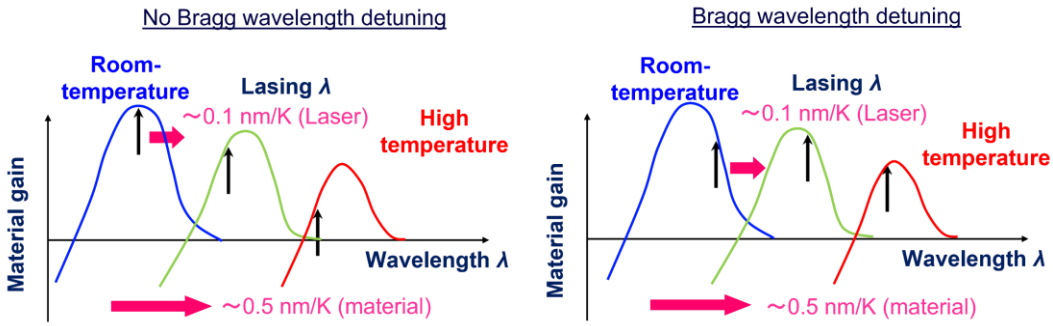


Fig. 4.44 Conceptual diagram of Bragg wavelength detuning

Bragg wavelength detuning is usually a cavity design used in high temperature operation of laser. Figure 4.44 shows a conceptual diagram of Bragg wavelength detuning. The bandgap becomes smaller as the temperature rises because the lattice spacing expands due to thermal expansion. For example, GaInAsP (λ near 1.5 μm) has the redshift typical value of ~ 0.5 nm/K. When it comes to changes in gain peak, the remaining two effects were often considered together. One is band filling effect. As the temperature rises, the threshold current of laser rises. Then, the carrier density injected into the active layer increases, which means that the carriers are distributed to higher energies, so the gain peaks move to shorter wavelength. Another one is called a many-body effect or bandgap renormalization. Considering the exchange energy between electrons that are fermions, there is also the effect that the bandgap shrinks as the carrier density increases. However, the main cause of the redshift of gain peak is the reduction of bandgap due to temperature increasing. The lasing wavelength of DFB laser almost determined by grating pitch. The refractive index of grating increases as the temperature rises, so the lasing wavelength of

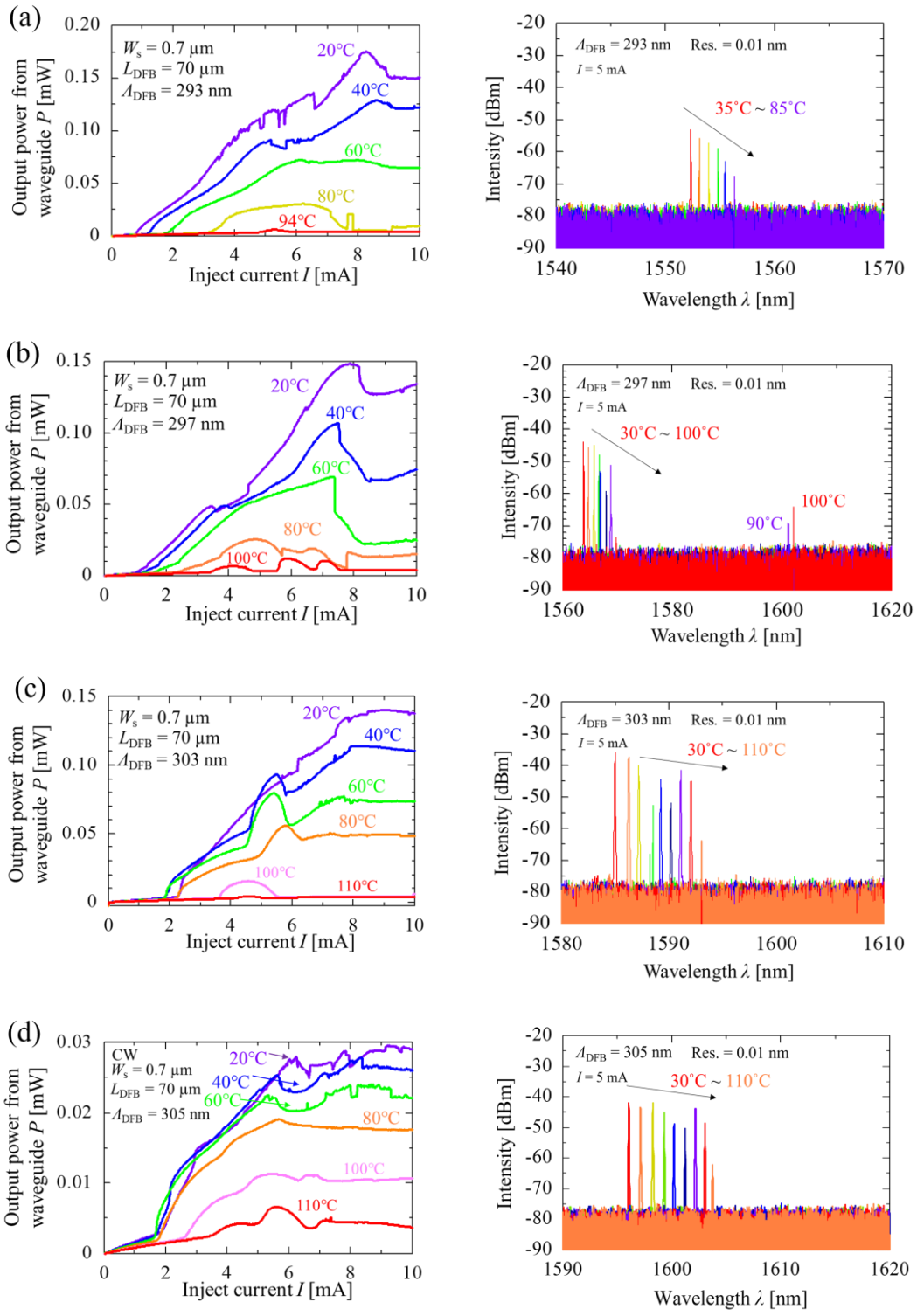


Fig. 4.45 I-L characteristics and lasing wavelength at a fixed current of 5 mA in various DFB grating pitch

DFB laser also has a redshift. It usually has a value of ~ 0.1 nm/K, which is smaller than the shift speed of gain material. In general case, the lasing wavelength was designed to match the gain peak at room temperature for obtaining a low threshold current, and the threshold current increases monotonically as the temperature rises. In Bragg wavelength detuning case, the lasing wavelength was designed larger than the gain peak intentionally. So, the lasing wavelength would match the gain peak at higher temperature because of the different shift speed.

Figure 4.45 shows the *I-L* characteristic and lasing wavelength (5-mA fixed bias current) of membrane DFB laser with the grating pitch of 293 nm, 297 nm, 303 nm and 305 nm. The kinks on the *I-L* figure are caused by light feedback from front and rear waveguide facets because no anti-reflection (AR) coating was performed. The stopband can be seen in the device of 293 nm, 297 nm pitch, but cannot be seen in the device of 303 nm and 305 nm, which maybe because the detuning value is deep, and the longer lasing wavelength cannot obtain enough gain from material and sensitivity of GaInAs photodiode is not high over 1620 nm. The lasing wavelength changed from shorter wavelength to longer wavelength at 100 °C, because of the faster redshift of material. 110 °C high stage temperature CW operation was obtained in the device with 305 nm grating pitch. Higher stage temperature operation was not measured due to the measurement system limitation.

Figure 4.46 shows the threshold current dependence on the stage temperature. The threshold current increases monotonically in the devices with Λ_{DFB} = 293 nm and Λ_{DFB} = 297 nm showing a negative detuning value. The threshold current decreases at first and increases as the stage temperature increasing in the devices with Λ_{DFB} = 303 nm and Λ_{DFB} = 305 nm showing a positive detuning value. A stable threshold current between 30 °C to 60 °C and 30 °C to 80 °C in the device with Λ_{DFB} = 303 nm and Λ_{DFB} = 305 nm, respectively. In order to estimate the detuning value, here considering a simple way that is assuming the lasing wavelength matched the gain peak at the temperature that the device had the lowest threshold current. The lowest threshold current exists at 50 °C and 70 °C in the device with Λ_{DFB} = 303 nm and Λ_{DFB} = 305 nm, and the lasing wavelength were

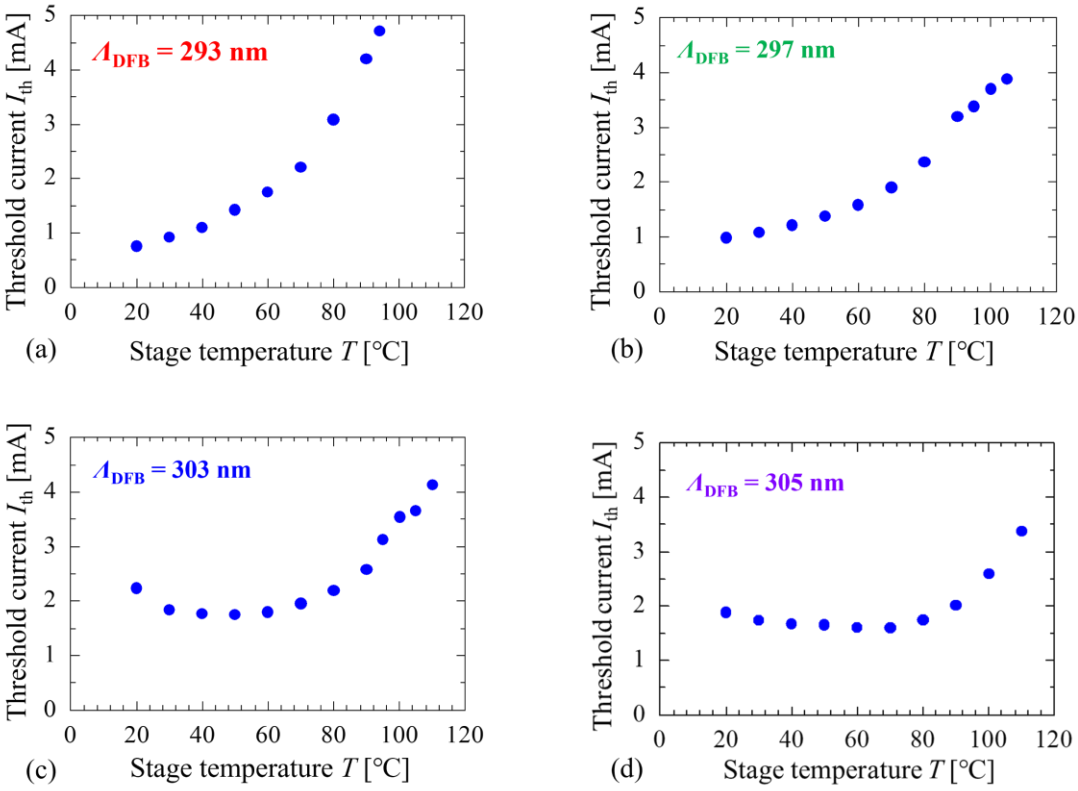


Fig. 4.46 Stage temperature dependence of threshold current (a) Λ_{DFB} = 293 nm with the lowest threshold current at 20 °C; (b) Λ_{DFB} = 297 nm with the lowest threshold current at 20 °C; (c) Λ_{DFB} = 303 nm with the lowest threshold current at 50 ˚C; (d) Λ_{DFB} = 297 nm with the lowest threshold current at 70 °C.

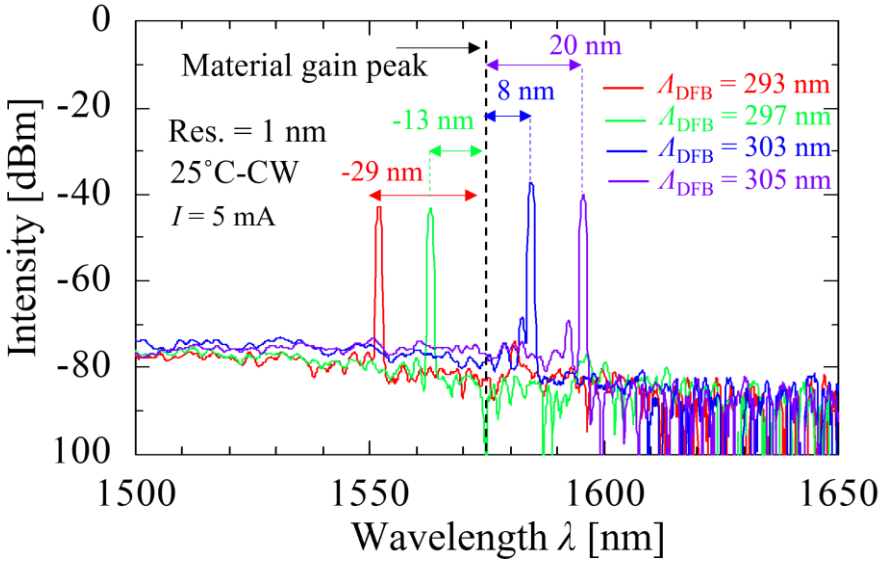


Fig. 4.47 detuning value of device with various pitch of grating

1587.2 nm and 1600.2 nm, respectively. Therefore, the gain peak can be calculated as 1574.7 nm and 1577.7 nm at 25 °C with the injection current of 5 mA using the typical shift speed of 0.5 nm/K. The little difference of two calculated gain peak wavelength due to the self-heating difference in device variability with the injection current of 5 mA. Based on the discussion above, the estimated detuning value were shown in the Fig. 4.47 under the condition of current injection of 5 mA at 25 °C.

4.4 Conclusion

In this chapter, a high flexibility and stable fabrication process of directly bonded membrane laser using CMP-SAB was established. The low thermal resistance membrane FP laser and DFB laser were fabricated successfully, and the thermal characteristics were estimated in experiment. CMP and SAB as the key technologies of the directly bonded membrane laser were discussed detailed. According to the measurement result of condition check in CMP process, the biggest factor affecting the polishing rate is the rotation speed of platen and head. The in-plane uniformity becomes worse as the polishing amount increases, which is due to the line speed of each point on the wafer is different and finally the surface shape caused by thickness difference of SiO_2 is only dependent on wafer size and shape. After 1-μm polishing of SiO_2, there is over 100 nm thickness difference on 2-inch wafer, but the bonding result indicates that it has no effect on bonding process. The reason may be considered that the low film thickness changes do not affect atomic diffusion in bonding process. After polishing, the surface roughness is about 0.3 nm, which fully meets the empirical criteria for direct bonding. Also, the surface roughness is only depending on the type of slurry. In membrane FP laser, the thermal resistance reduction of 50% was confirmed compared with that of the device using 2-μm-thick BCB bonding layer with almost the same cavity length. A higher optical saturation current and 4 times higher maximum output power was obtained. In SAB membrane DFB laser, a little higher threshold current obtained this time because of the fabrication error. However, an optical saturation current about 8 mA obtained in all devices with different grating pitch, which shows a high heat dissipation structure in SAB membrane DFB laser. A 510 K/W thermal resistance was obtained experimentally, which is the lowest value we have achieved, although the cavity length is 70 μm.

Figure 4.48 shows a comparison of thermal resistance. The numerical calculation was based on 3D simulation of temperature distribution of membrane laser. In the previous work, usually near 30-μm-length short cavity was studied for obtaining a low threshold current in membrane DR laser. In membrane DFB laser, the general maximum output

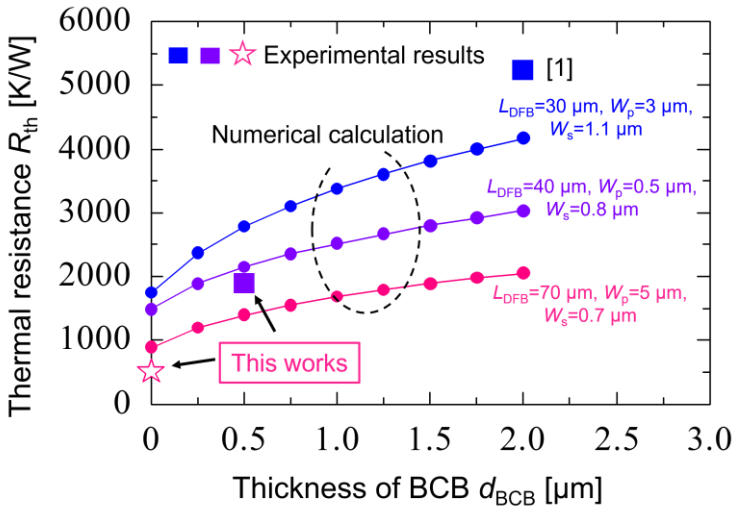


Fig. 4.48 Comparison of thermal resistance of fabricated device

power was about 30 ~ 40 μW with the cavity length of 50 μm, and ~ 50 μW with the cavity length of 70 μm using BCB bonding. In this experiment, unfortunately, a higher electrical resistance and threshold current existed due to the fabrication error and there is about 20% reflection on the front facet leads to a light feedback effect caused a lower detected output power compared with the laser in full optical integration device. Even with these the problems, 3 times higher output power and low thermal resistance were obtained at room temperature. The next chapter will show a membrane optical link using SAB membrane DFB laser with a high output even under the stage temperature of 100 °C with the optimized fabrication process.

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Chapter 5

Membrane photonic integrated circuits fabricated by surface activated bonding

5.1 Introduction

This chapter describes the integration of membrane DFB laser, GaInAsP passive waveguide and GaInAsP MQWs membrane p-i-n photodiode with buried-ridge-waveguide[1] (BRW) structure on Si-substrate by a-Si assisted room-temperature surface-activated bonding. The bonding method and quality estimation were explained in chapter 3. The lower thermal resistance and high temperature operation of waveguide integrated membrane DFB laser was realized in chapter 4. The membrane link was studied in the previous works[2]-[3]. However, the output power was not enough for high-speed data transmission, and the high temperature characteristic was not demonstrated. For the

optical link using membrane structure operates under various ambient temperature, an integration of low thermal resistance membrane laser, passive waveguide and membrane p-i-n photodiode is necessary. The cavity length of 70 μm was used in the experiment for larger output and good comparison with previous works. The BRW structure enhanced the lateral optical confinement, which maintained a low threshold current operation of membrane laser while increasing the cavity length for low thermal resistance and high output power. Section 5.2 describes the structure and fabrication process of surface-activated bonded membrane integrated circuits (SAB-MPICs) at first For electrical isolation between laser and photodiode, a dry-etching for removing unnecessary surface InP was carried out. This isolation process not only prevent the cross talk in the high-speed modulation test between laser and photodiode, but also formed a trench structure on laser reducing leak current. An I_{LD}-I_{PD} fundamental characteristic was shown at first. The measurement was under an on-wafer test environment without cleaving. In the temperature characteristic, the stage temperature and wafer surface temperature were well calibrated before measurement. Finally, the data transmission was measured for small signal and large signal modulations. Section 5.3 described a InP-rib waveguide integrated membrane photonic integrated circuit for cm level data transmission. The fabrication process was given at first, and the static characteristic was measured premilitary. Section 5.4 made a comparison to the NTT's work at first, and future prospects were proposed for low power consumption membrane photonic integrated circuits.

5.2 High temperature and high efficiency operation of membrane optical link

5.2.1 Device structure

The schematic of the membrane optical integrated circuits was shown in Fig. 5.1(a). This membrane optical link consists of a membrane DFB laser with the cavity length of 50~90 μm, passive GaInAsP waveguide with the length of 500~1000 μm, and p-i-n membrane PD with the absorption length of 200 μm. The membrane laser and photodiode are connected with waveguide by straight butt-joint built-in (BJB) structure. The details of BJB conditions were described in previous works[4]. The absorption layer structure in photodiode is as same as the active layer of DFB laser. The initial epitaxial wafer consisted of a 267 nm thick core layer including a GaInAsP five-quantum-well active layer (5.4 nm/well, 10 nm/barrier) with a photoluminescence peak wavelength of 1549 nm sandwiched between GaInAsP optical confinement layers, a p^+-GaInAs contact layer, and InP/GaInAs etch-stop layers grown by OMVPE. All membrane optical devices were bonded on Si by room-temperature surface-activated bonding assisted by a-Si nanofilm. Unnecessary surface InP layer was removed by dry-etching, hence the SiO_2 cladding layer was exposed on the surface. This electrical isolation structure between laser and photodiode not only reduced leak current of laser, but also reduced cross talk of RF probs in modulation measurement. Figure 5.1 (b) and (c) show the cross-sectional view of membrane DFB laser, photodiode and waveguide. The thickness difference in BRW structure was 50 nm in design and fabricated by controlling regrowth time and wet-etching time before regrowth. In data transmission, electrical signals were input into membrane DFB laser through RF probs and converted to optical signal using directly modulation. The optical signals transmitted to membrane photodiode through passive waveguide and were converted to electrical signals again.

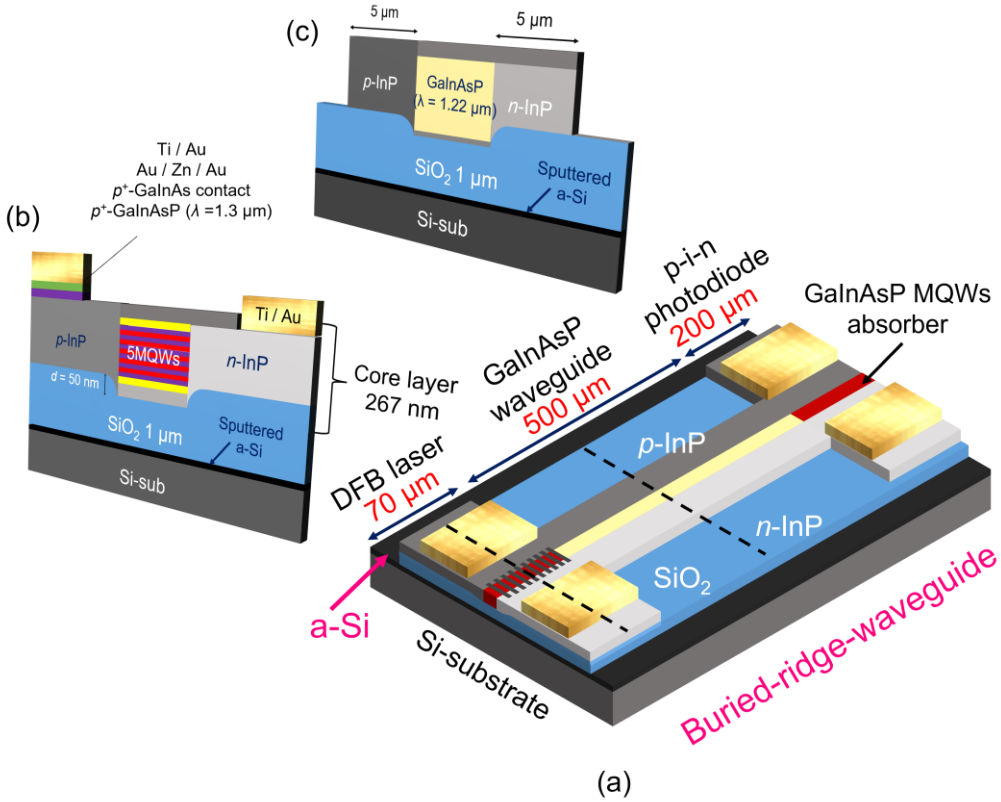


Fig. 5.1 Schematic of membrane optical link (a) top view (b) cross-sectional view of active region and absorber (c) cross-sectional view of passive waveguide.

5.2.2 Fabrication process

The fabrication process is shown in Fig. 5.2. The layer structure of initial wafer is the same with Table 4.8. Here shows again in Table 5.1. Two mesas were formed at the same time for laser and photodetector. The device fabrication then started with three-steps OMVPE selective area regrowth to form a passive waveguide n- and p-InP side cladding layers, which was the same as the fabrication of membrane DFB laser shown in chapter 4. By controlling the growth time of selective area regrowth in the OMVPE process in *n*-

Table 5.1 Initial wafer layer structure

Layer	Material	Wavelength [nm]	Thickness [nm]	Doping level [cm^{-3}]
InP protection	*u*-InP		10	
GaInAs protection	*u*-$Ga_{0.47}In_{0.53}As$		10	
Cap	*u*-InP		50	
u-OCL	$Ga_{0.21}In_{0.79}As_{0.46}P_{0.54}$	1200	15	
TS -0.15% barrier	$Ga_{0.26}In_{0.74}As_{0.49}P_{0.51}$	1200	10	
CS 1.0% well	$Ga_{0.22}In_{0.78}As_{0.81}P_{0.19}$	1520	5.4	
TS -0.15% barrier	$Ga_{0.26}In_{0.74}As_{0.49}P_{0.51}$	1200	10	
CS 1.0% well	$Ga_{0.22}In_{0.78}As_{0.81}P_{0.19}$	1520	5.4	
TS -0.15% barrier	$Ga_{0.26}In_{0.74}As_{0.49}P_{0.51}$	1200	10	
CS 1.0% well	$Ga_{0.22}In_{0.78}As_{0.81}P_{0.19}$	1520	5.4	
TS -0.15% barrier	$Ga_{0.26}In_{0.74}As_{0.49}P_{0.51}$	1200	10	
CS 1.0% well	$Ga_{0.22}In_{0.78}As_{0.81}P_{0.19}$	1520	5.4	
TS -0.15% barrier	$Ga_{0.26}In_{0.74}As_{0.49}P_{0.51}$	1200	10	
CS 1.0% well	$Ga_{0.22}In_{0.78}As_{0.81}P_{0.19}$	1520	5.4	
TS -0.15% barrier	$Ga_{0.26}In_{0.74}As_{0.49}P_{0.51}$	1200	10	
u-OCL	$Ga_{0.21}In_{0.79}As_{0.46}P_{0.54}$	1200	15	
Cap	*u*-InP		100	
1.3 Q	*p*-GaInAsP	1300	50	Be: 4×10^{18}
p-contact	*p*-$Ga_{0.47}In_{0.53}As$		100	Be: 8×10^{18}
InP etch stop	*u*-InP		100	
GaInAs etch stop	*u*-$Ga_{0.47}In_{0.53}As$		300	
Substrate	*n*-InP		350000	

and *p*-InP regrowth, a difference in thickness (~50 nm) was occurred between the core layer and the InP side cladding layer. This ridge structure enhanced the refractive index difference in the lateral direction, which resulted in larger optical confinement than that of the conventional flat structure. After regrowth, the metal marks (Ti/Au) including maskless lithography and EB lithography marks were evaporated on the surface. Then, the surface was deposited with SiO_2 of 2 μm thick as the cladding layer by plasma-enhanced chemical vapor deposition and flattened by CMP. After CMP, the thickness of the SiO_2 layer was approximately 1 μm. Subsequently, the wafer was bonded to Si by a-Si-assisted room-temperature surface-activated bonding without annealing. The detailed bonding process is the same as shown in chapter 3. The 350 μm thick InP substrate was removed by HCl for about 1 hour and etch-stop layers were removed by selective wet etching. The 100 nm thick contact GaInAs and 50 nm thick 1.3Q GaInAsP layers were removed by (H_2SO_4:H_2O_2:H_2O = 1:1:40) and only p-side current path region on laser and photodetector were remained. In this moment, ~370 nm ZEP520A was spin-coated on the 2-inch processed wafer and baked for 20 min in oven. Surface grating was only formed on the DFB laser region with the grating pitch from 287 nm to 305 nm by electron beam lithography and reactive ion dry etching. Layers of Au/Zn/Au (25/50/300 nm) was deposited by thermal resistance evaporation as *p*-electrode and annealed at 350 ºC for 1 min. In addition, Ti/Au (25/200 nm) was deposited as both *p*- and *n*-electrode. Finally, laser and detector were electrically isolated by removing unnecessary InP (5 μm width InP was remained at both side of waveguide), which suppressed the leakage current and crosstalk in the integrated structure.

Figure 5.3 shows a photograph of fabricated device. Large-bonded area shows the stability of surface-activated bonding assisted by a-Si in SiO_2-Si bonding. The waveguide length was designed in 500 and 1000 μm. The stripe width was designed from 0.5 to 1.5 μm and distance from p-electrode to active region was designed from 1.7 to 3.0 μm. The laser and PD were staggered in distribution, which was shown in Fig. 5.4. Each laser was connected with two membrane p-i-n PD, hence, the light reflection can be effectively prevented. The different color appeared in p- and n-InP region was due to the different

thickness of SiO_2. High magnification images near laser and PD were shown in the right side of Fig. 5.4. About 11 μm width InP layer was remained on the surface for the buried GaInAsP waveguide. The cavity length of DFB laser was fabricated from 30 to 150 μm, and all the membrane PDs have the absorption length of 200 μm.

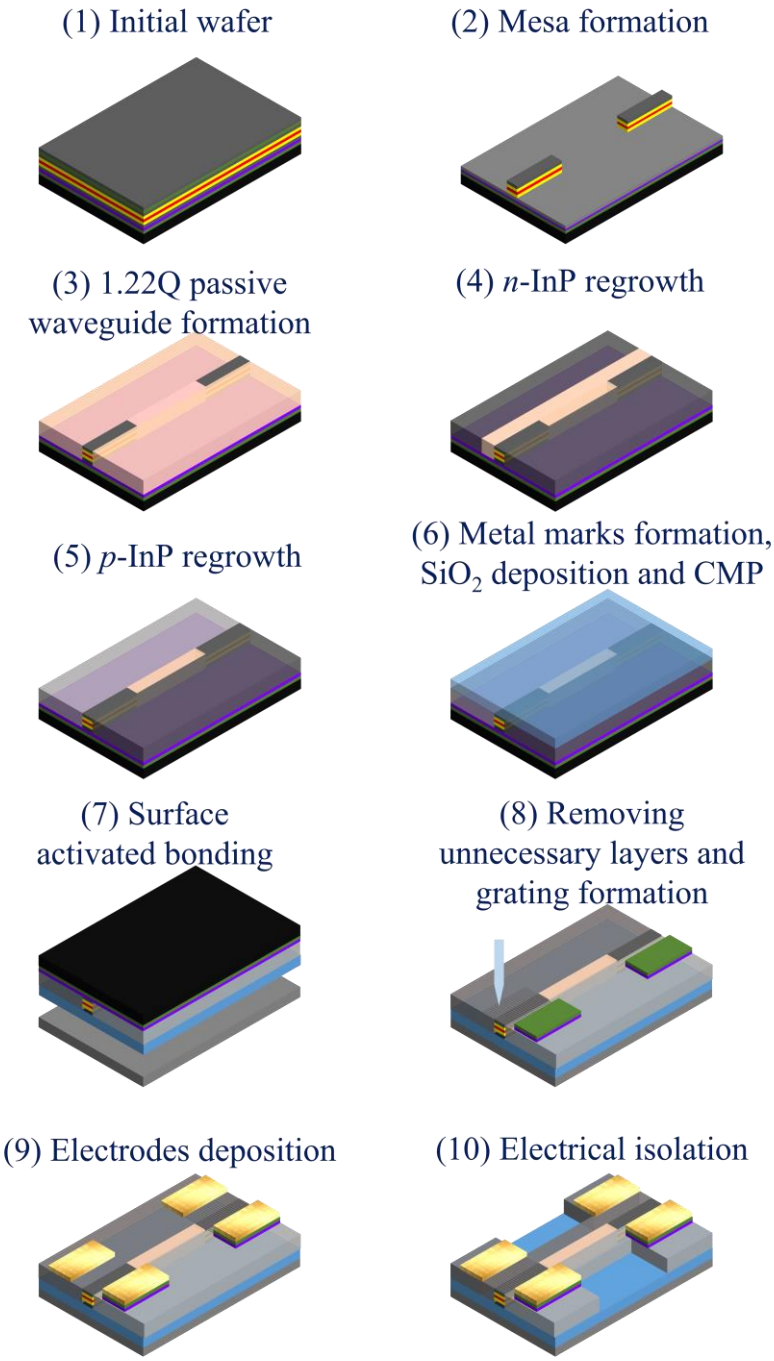


Fig. 5.2 Fabrication process of membrane photonic integrated circuits by a-Si assisted room-temperature surface-activated bonding

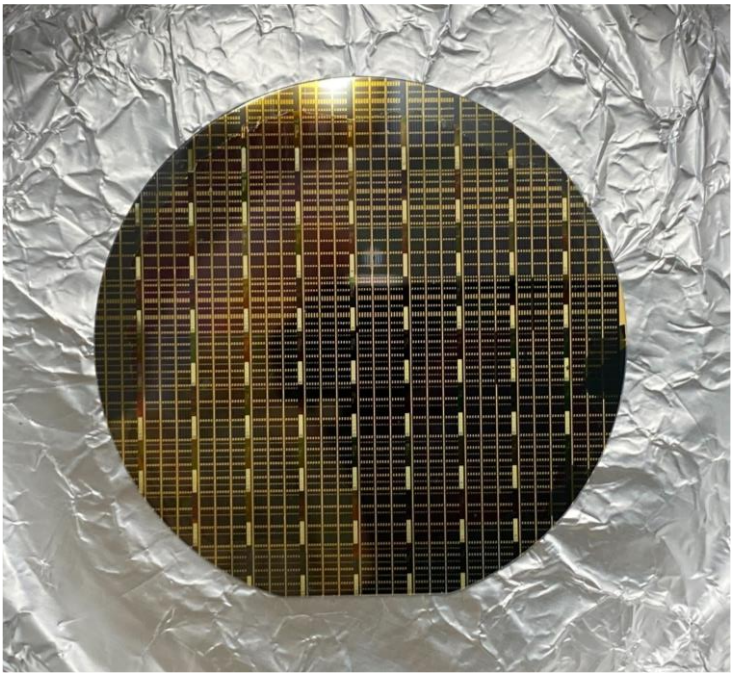


Fig. 5.3 Photograph of fabricated device.

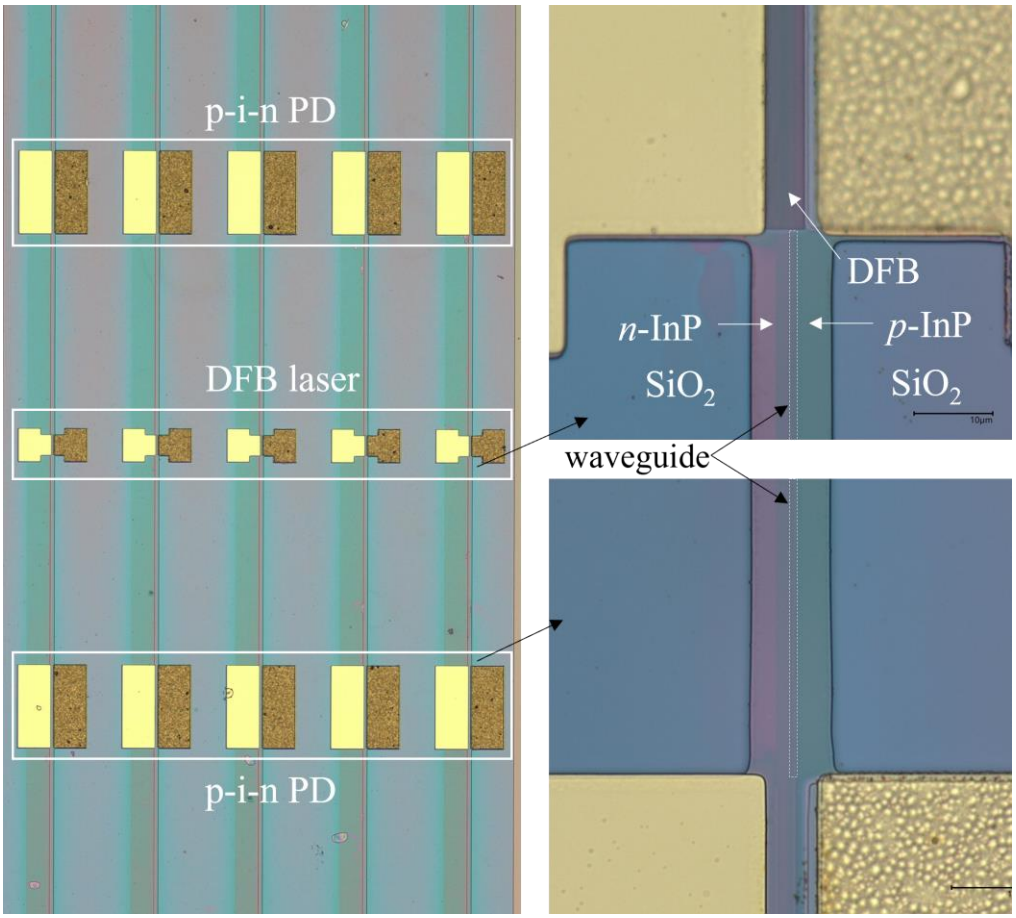


Fig. 5.4 Optical microscope images of fabricated device.

5.2.3 Static characteristics

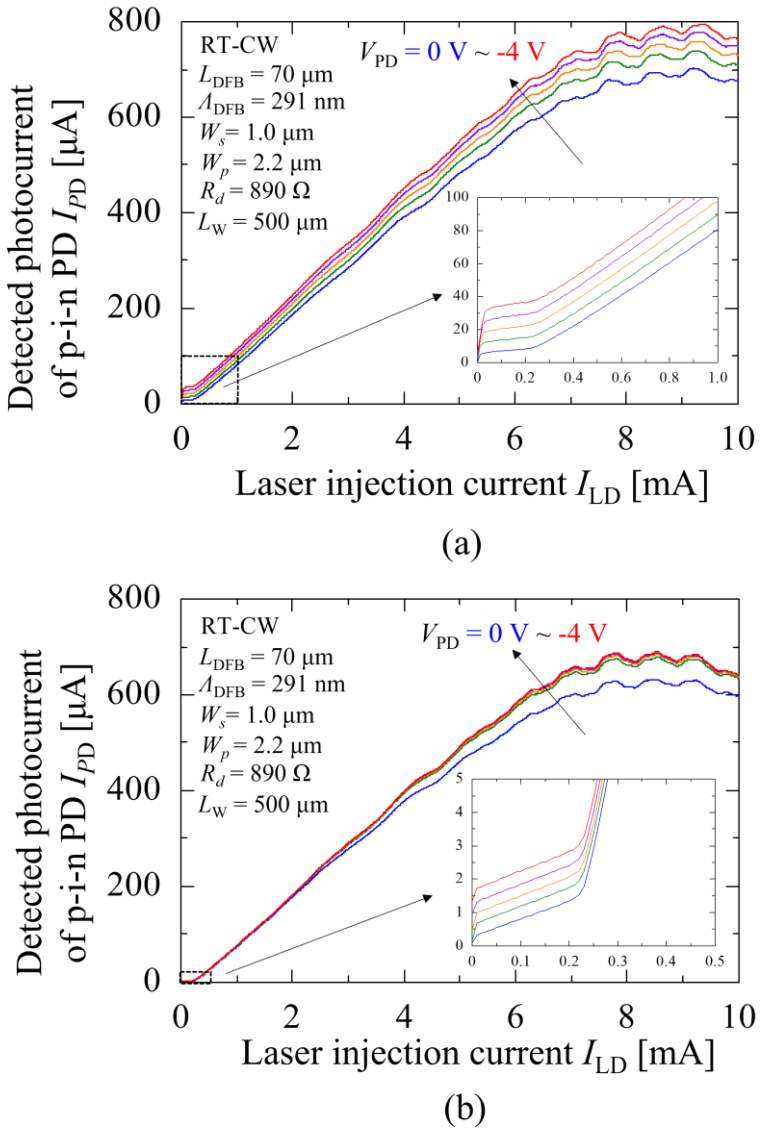


Fig. 5.5 I_{LD}-I_{PD} characteristics of (a) before electrical isolation (b) after electrical isolation

The membrane optical integrated circuits were estimated statically by measuring optical transmission between membrane DFB laser and p-i-n PD. A current bias source was applied on laser and a voltage bias source was applied on p-i-n PD at the same time, and the whole measurement was under an on-wafer test environment. The light output from laser was detected by p-i-n PD, and the detected photocurrent I_{PD} as a function of laser injection current I_{LD} before and after isolation process were shown in Fig. 5.5. The

threshold current was 0.22 mA. Before isolation, the obtained photocurrent below threshold came from the leak current from p-electrode in laser to p-electrode in p-i-n PD and the leak current was reduced to be <1/10 of that after isolation process. With the reverse bias voltage increasing in p-i-n PD, the detected photocurrent increased due to increased leak current.

Next, the influence of electrode shape design on leak current was investigated. Figure 5.6 shows the I_{LD}-I_{PD} characteristics before and after electrical isolation process with the cavity length of 50 μm and the shape of electrode. The threshold current was reduced 50

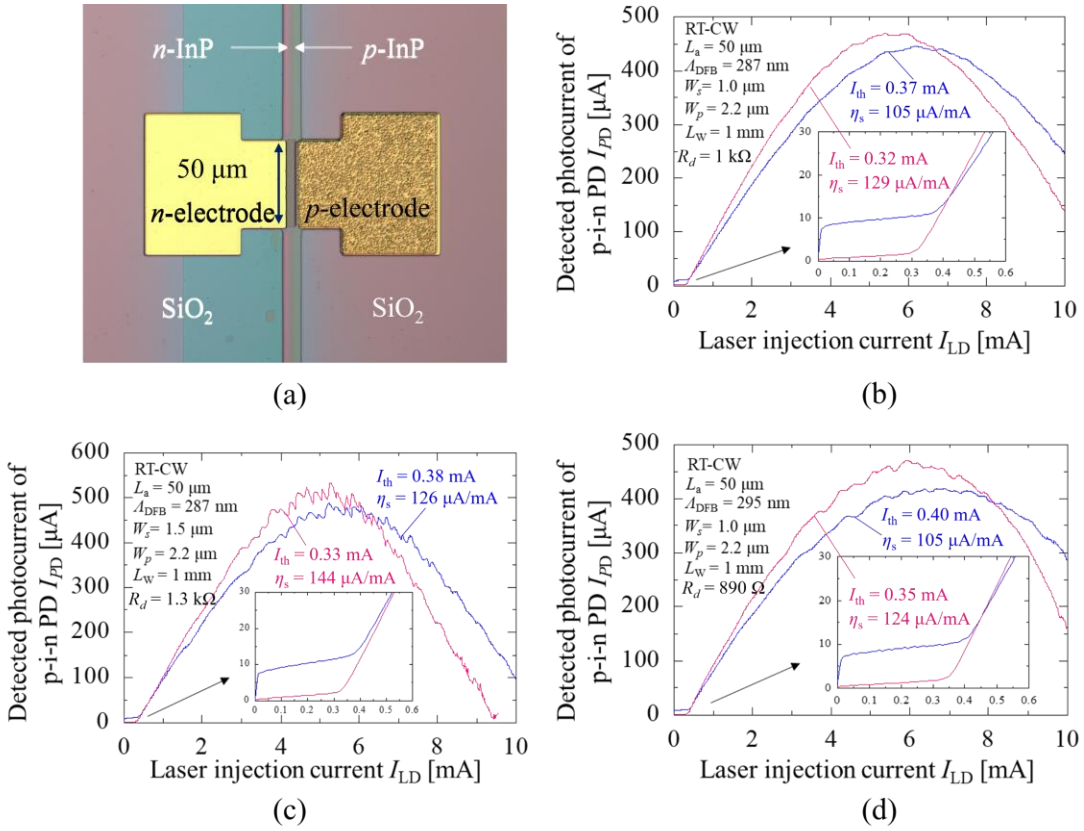


Fig. 5.6 (a) Top view of fabricated device with the cavity length of 50 μm, (b)(c)(d) I_{LD}-I_{PD} characteristics before and after electrical isolation process. (V_{PD} = -1 V)

μA after electrical isolation process, and the slope efficiency was increased 15% ~ 23%, which was because the injection efficiency η_i increased while leak current reduced. Figure 5.7 shows the I_{LD}-I_{PD} characteristics before and after electrical isolation process with the cavity length of 70 μm and the shape of electrode. In this situation, there are almost no change observed in the threshold current and slope efficiency after electrical isolation process (Fig. 5.7 (b)~(d)), which indicates that the leak current near electrode is extremely small in the design of Fig. 5.7 (a). Therefore, for short cavity membrane laser (30 ~ 50 μm) using the electrode design like Fig. 5.6 (a) or similar design shown in Chapter 4, the electrical isolation process was not only for isolation between laser and p-i-n PD in the integration structure, but also good for reducing leak current (trench structure).

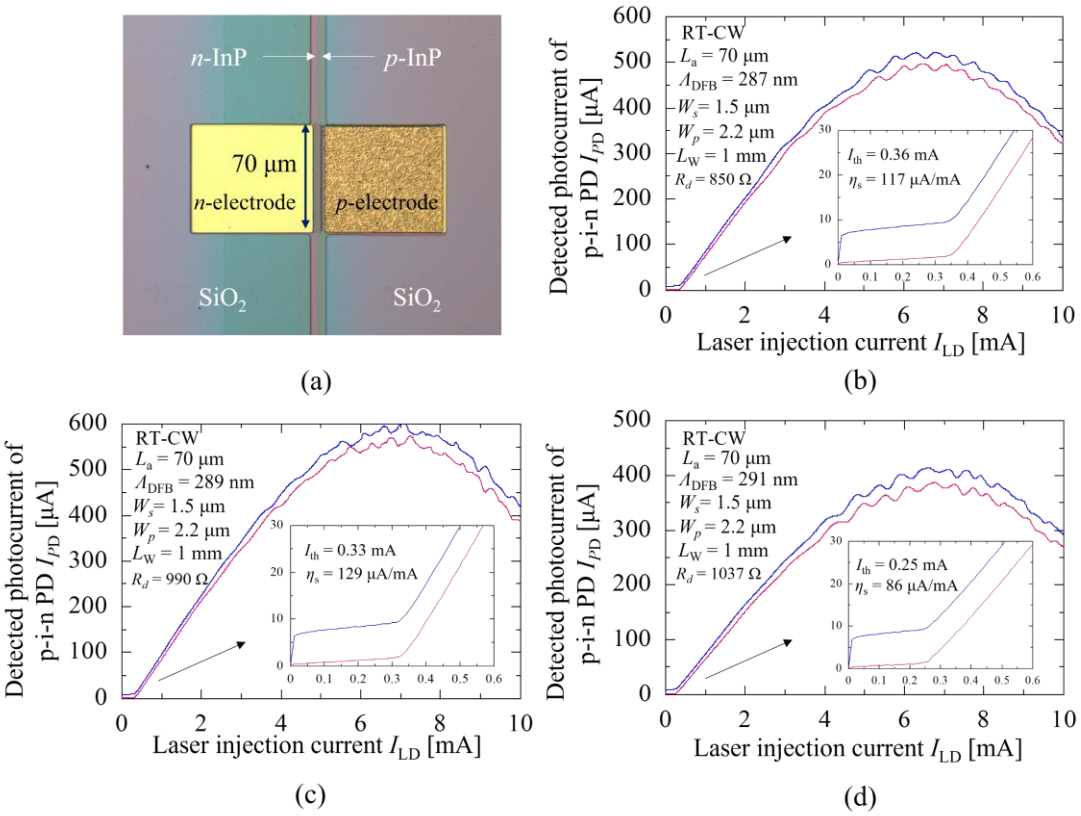


Fig. 5.7 (a) Top view of fabricated device with the cavity length of 70 μm, (b)(c)(d) I_{LD}-I_{PD} characteristics before and after electrical isolation process. (V_{PD} = -1 V)

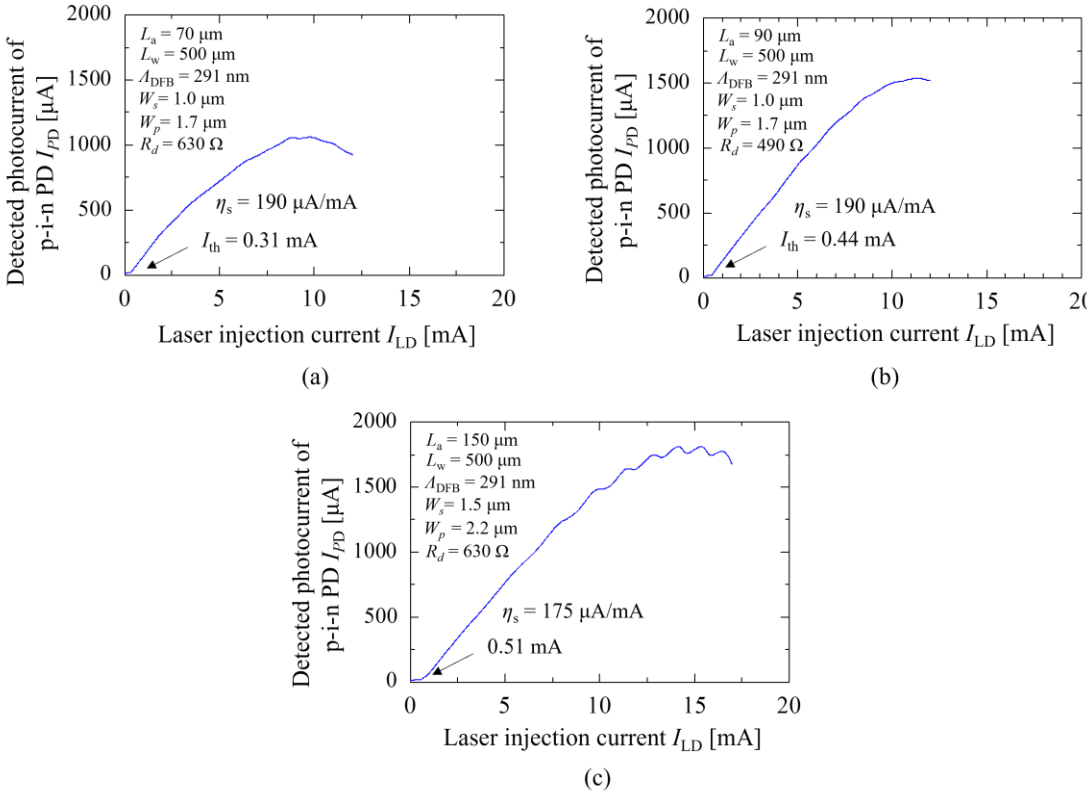
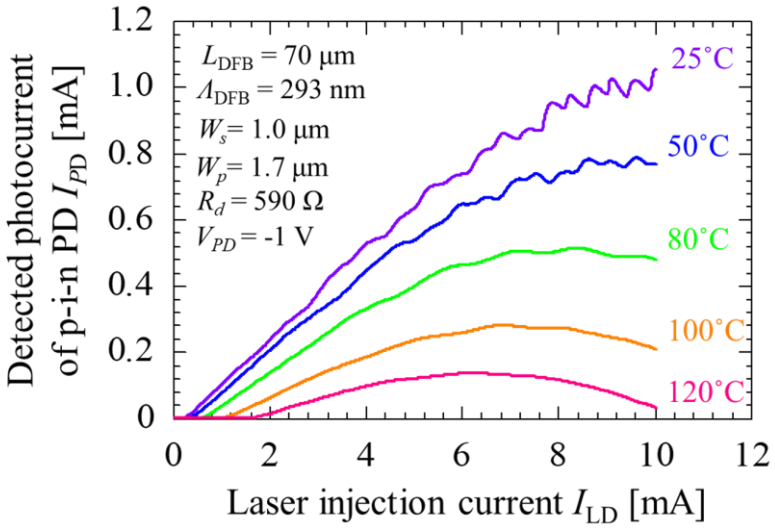


Fig. 5.8 I_{LD}-I_{PD} characteristics with different cavity length of DFB laser (a) 70 μm (b) 90 μm and (c) 150 μm

Figure 5.8 shows the I_{LD}-I_{PD} characteristics with different cavity length of DFB laser from 70 to 150 μm with 500-μm-length waveguide. The detected photocurrent was over 1 mA in the 70-μm-length device, which was 6.3 times larger than previous work[3], and the optical saturation current was near 10 mA. In the chapter 4, ~500 K/W thermal resistance had been obtained in SiO_2/Si direct bonded membrane laser with 70-μm-length cavity. Based on the calculation in Fig. 2.25, chapter 2, the membrane laser has the output power of about 1 mW and optical saturated current of about 10 mA by assuming the differential resistance was 750 Ω, which agrees with this experimental result by assuming the responsivity of p-i-n PD was 1.0 W/A. Figure 5.8 (b) and (c) shows the results of longer cavity device. Over 1.75 mA photocurrent was obtained in the 150-μm-length device.

Temperature dependence of I_{LD}-I_{PD} characteristics was shown in Fig. 5.9. Low threshold current of 0.22 mA and high slope efficiency of 0.14 mA/mA were obtained at 25°C. The highest recorded operation temperature was up to 120 °C, which is also the

highest operation stage temperature in our study so far. The detected photocurrent was over 100 μA even at the stage temperature of 120 °C. The threshold current increased monotonically with temperature increasing, which means no positive Bragg wavelength detuning effect existed. The device successfully operated at high temperature up to 120 °C not only result of low thermal resistance, but also thanks to the lower differential resistance compared with the device shown in chapter 4. In addition, the reduced quantum well thickness from 6 nm to 5.4 nm in initial epitaxial wafer increased energy difference between the first and second energy levels in quantum wells, which also beneficial for high temperature properties of membrane laser.



T [°C]	slope efficiency [mA/mA]	threshold current [mA]
25	0.140	0.22
50	0.121	0.34
80	0.100	0.61
100	0.067	1.07
120	0.043	1.70

Fig. 5.9 Temperature dependence of I_{LD}-I_{PD} characteristics

5.2.4 Dynamic characteristics

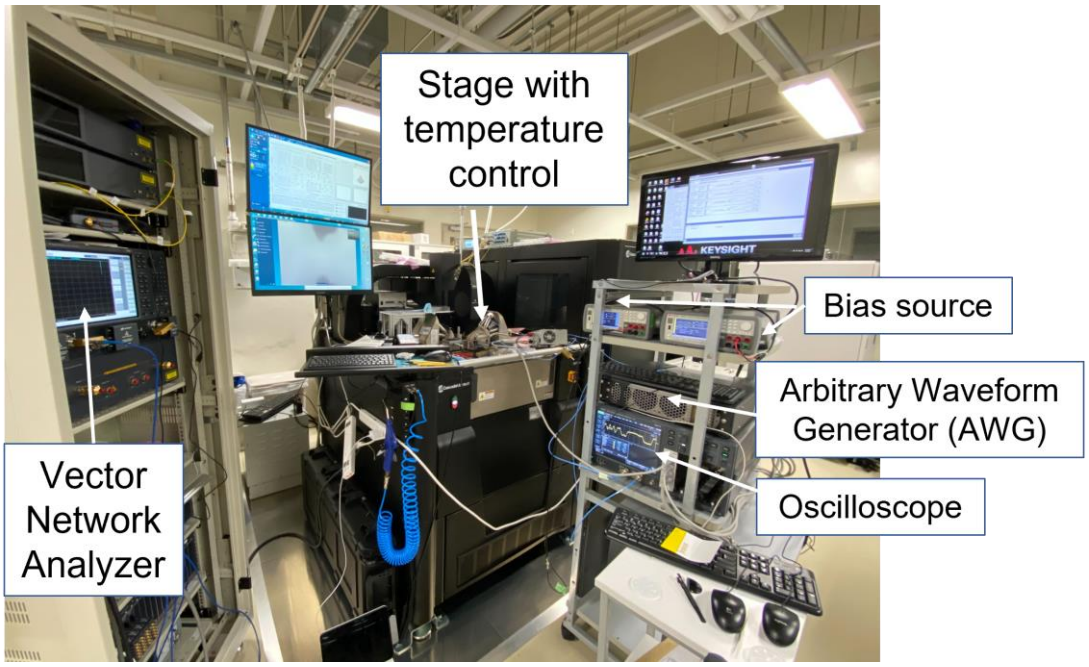
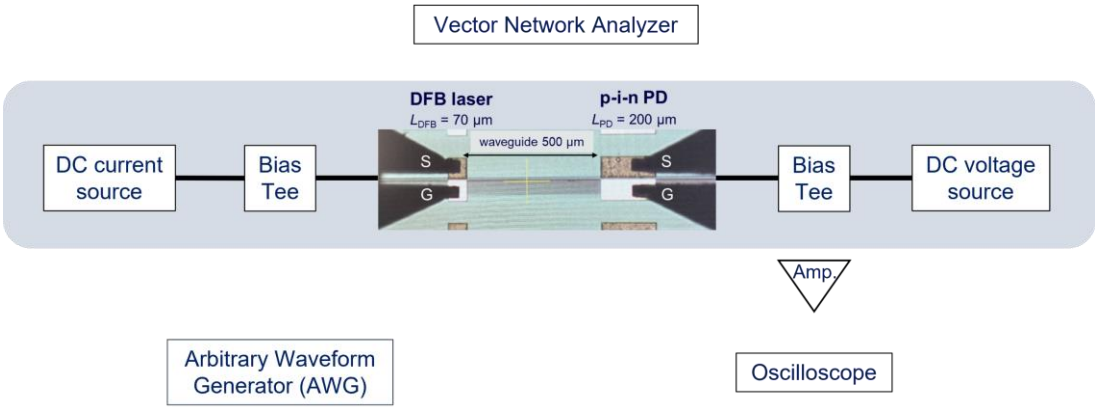
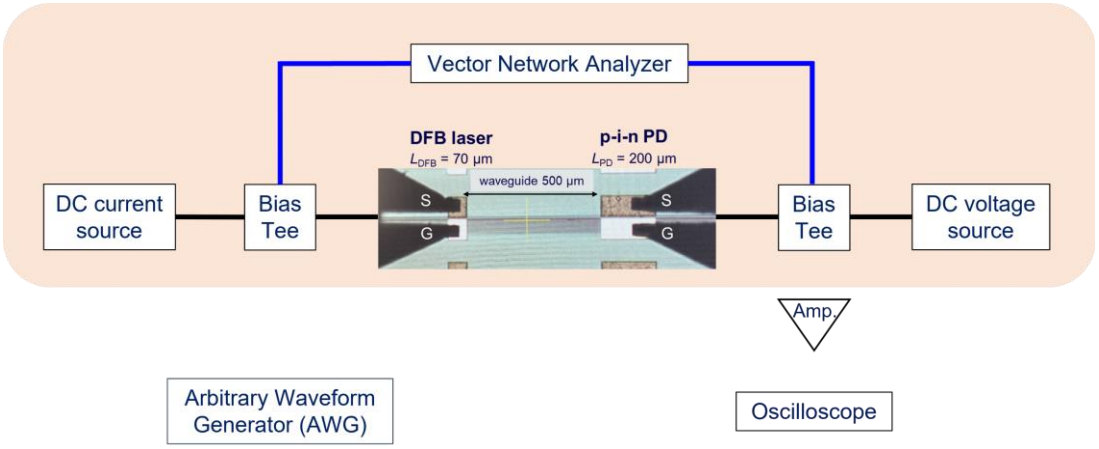


Fig. 5.10 Dynamic measurement system

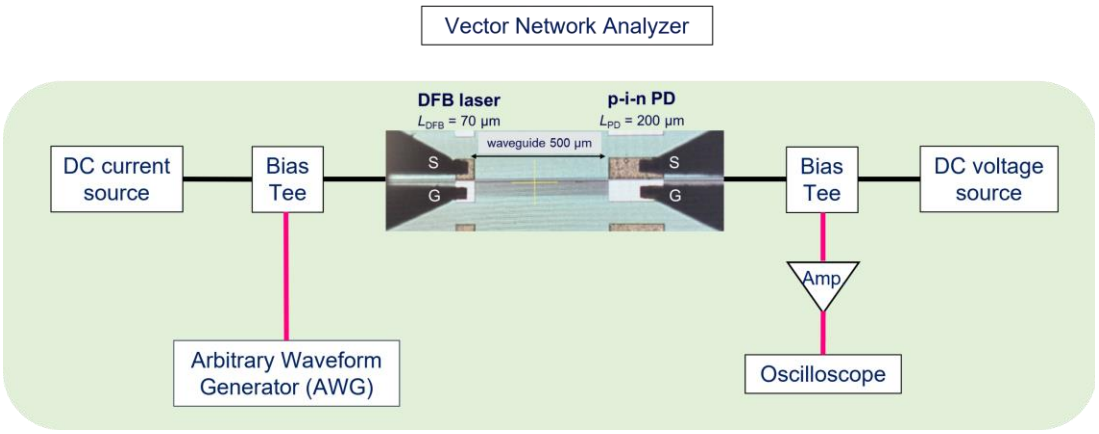
Figure 5.10 shows the system of dynamic measurement. Two bias sources including DC current source and DC voltage source drive laser and p-i-n PD through bias tee. The vector network analyzer (VNA) was used to measure the small signal S_{21} response of membrane integrated circuits. In large signal measurement, the input signal was generated by arbitrary waveform generator (AWG). A pseudorandom binary sequence (PRBS) of 2^{15}-1 non-return-to-zero (NRZ) signal was used. For both small signal and large signal analysis, the frequency characteristics of electrical parts including cables, bias-Tees and amplifiers are eliminated by calibration functions of VNA and AWG. All the measurement were still under on-wafer test environment without cleaving. The stage temperature was controlled in the test. The temperature range in dynamic measurement was from 25 ~ 80 °C.



(a)



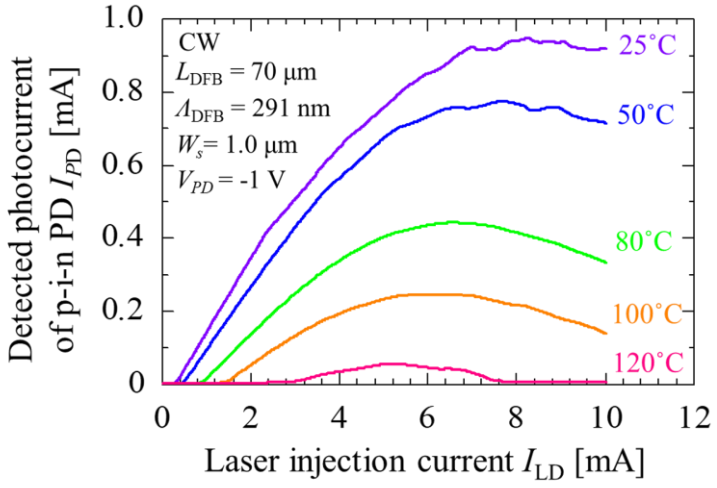
(b)



(c)

Fig. 5.11 Schematic diagram of measurement system of (a) static characteristic, (b) small signal S_{21} characteristic and (c) large signal transmission

Figure 5.11 shows the schematic of measurement system. The electrical connection was done with 40 GHz, 100-μm-pitch GS/SG-type RF probes. Figure 5.11 (a) was used in static measurement, and as can be seen in Fig. 5.11 (b) and (c), the system of static measurement was a part of dynamic measurement system. Therefore, it is convenient to measure the I_{LD}-I_{PD} characteristic before dynamic measurement to confirm the device fundamental operation, especially in high temperature measurement.



T [°C]	slope efficiency [mA/mA]	threshold current [mA]
25	0.203	0.27
50	0.174	0.43
80	0.122	0.86
100	0.086	1.36
120	0.031	2.89

Fig. 5.12 Static characteristic of the device used in dynamic measurement.

Figure. 5.12 shows the temperature static characteristic of the device used in dynamic measurement. This device has a low threshold current of 0.27 mA and a high efficiency of 0.203 mA/mA at room temperature. The efficiency was 3 times higher than that of in the previous work[3]. It gives us the slope efficiency of integrated SAB membrane DFB laser, including coupling and waveguide loss, of 0.203 W/A by assuming p-i-n PD

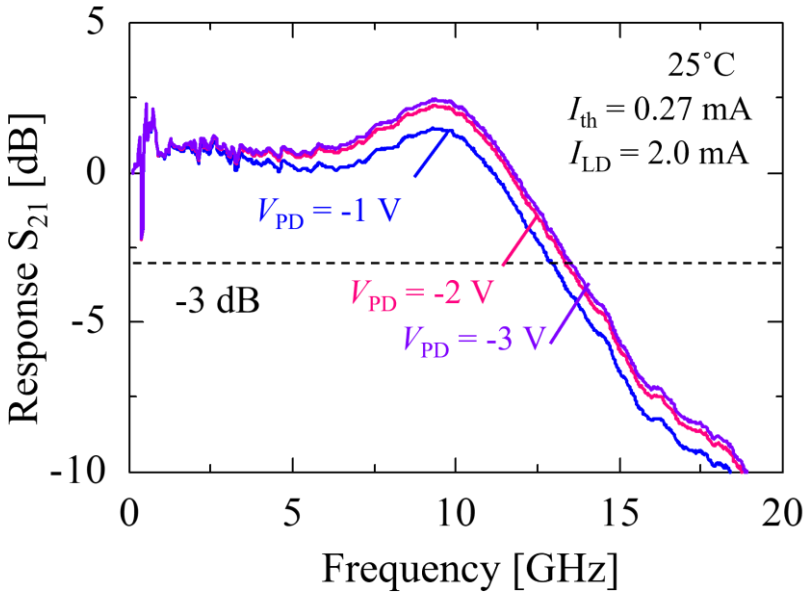


Fig. 5.13 Small-signal S_{21} response of bias voltage dependence with a bias current of 2.0 mA

responsivity of 1.0 A/W. The maximum detected photocurrent was 0.95 mA. Even at 100 ˚C stage temperature, there was still 0.246 mA photocurrent at the laser injection current of 5.8 mA. A 120 °C high temperature CW operation was achieved as well.

Figure 5.13 shows the small-signal S_{21} response with different bias voltage of p-i-n PD for a fixed bias current of membrane laser of 2.0 mA at room temperature. Increased reverse bias voltage had a larger 3-dB bandwidth due to that strong electric field shorten the transit time of photogenerated carriers. The spike near 0.4 GHz was due to the measurement system but not the device. The maximum 3-dB bandwidth obtained at the bias voltage of -3 V.

Figure 5.14 shows the small-signal frequency response and slop efficiency at various stage temperature. The p-i-n PD bias voltage was fixed to -3 V. The peak frequency increased with the DFB laser bias current increase, which indicates that the response is not electrical crosstalk between two RF probs. The 3-dB bandwidth of the MPIC was 16.8 GHz at a DFB laser bias current of 4.0 mA and a 10.3 GHz/mA$^{1/2}$, 6.8 GHz/mA$^{1/2}$ modulation efficiency was obtained for f_{3dB} and f_R. The modulation efficiency was determined by the slope of the 3-dB bandwidth and relaxation oscillation frequency as a

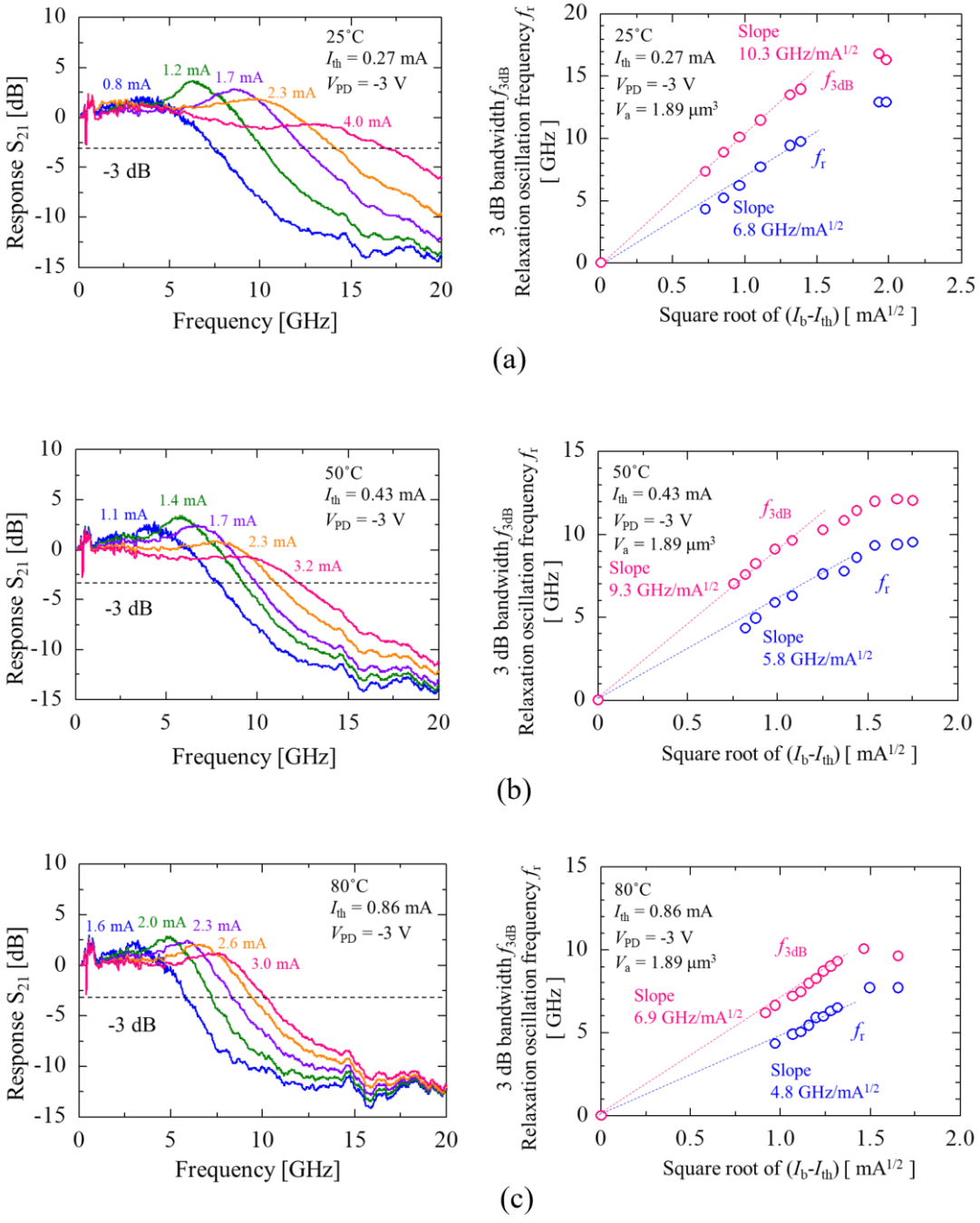
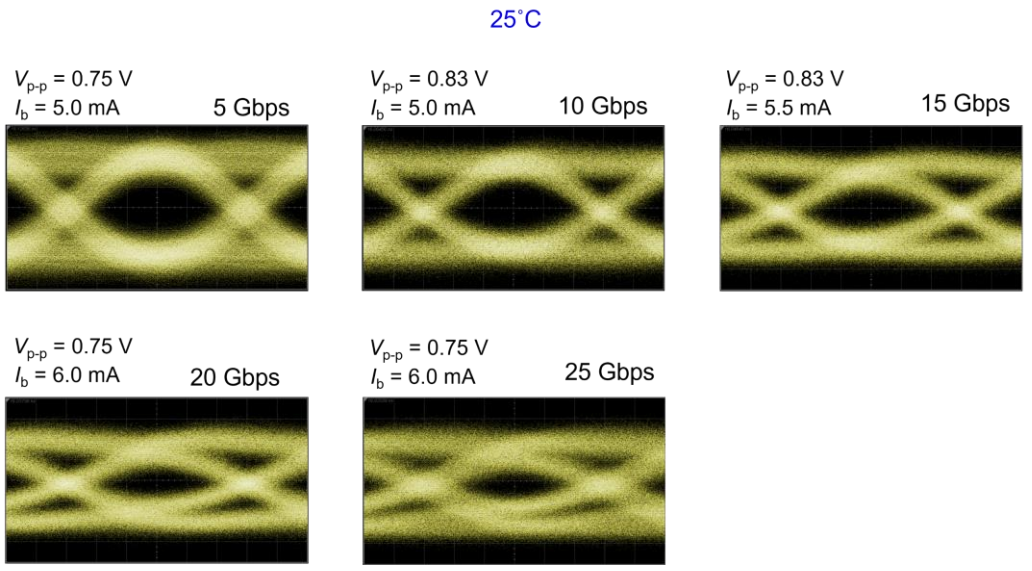
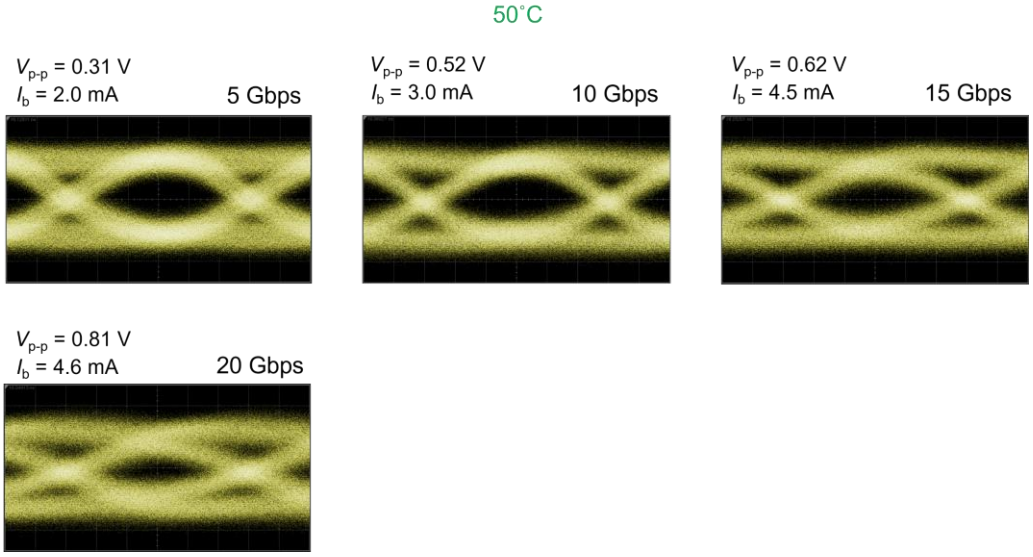


Fig. 5.14 Small-signal response S21 and slop efficiency at various stage temperature (a) 25 ˚C (b) 50 ˚C and (c) 80 ˚C.

function of the square root of the bias current above threshold. These values were comparable to our previous research with similar volume of active region. When the ambient temperature was higher than room temperature, a 12.1 GHz and 10.1 GHz 3-dB



(a)



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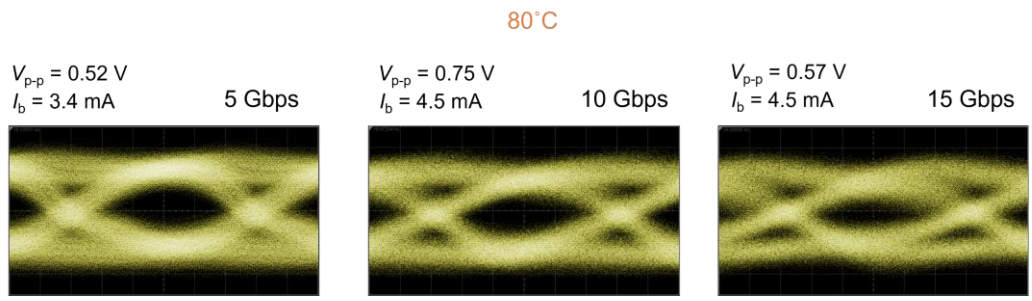


(c)

Fig. 5.15 Eye diagram of various data transmission rate at (a) 25 ˚C, (b) 50 ˚C and (c) 80 ˚C

bandwidth were obtained with the bias current of 3.2 and 3.0 mA at 50 ˚C and 80 ˚C, respectively. The slop efficiency of 9.3 GHz/mA1/2, and 6.9 GHz/mA1/2 were obtained for f_{3dB} at 50 ˚C and 80 ˚C as well. These values were smaller than that of at-room-temperature because the differential gain decreases as the temperature increasing.

Next, a data transmission was performed in MPIC. As mentioned before, Degradation of the signals by electrical cables are compensated by the function of AWG, but no pre-emphasis to the device was applied. The signals from p-i-n PD were recorded by a sampling oscilloscope. Figure 5.15 shows the eye diagram of data transmission at various stage temperature. A clear eye opening was obtained of 25 Gbps at 25 ˚C, 20 Gbps at 50 ˚C and 15 Gbps at 80 ˚C, respectively, which are the highest bit rate we have recorded at room temperature and higher temperature. These results show the MPIC has the potential to work at various ambient temperature as the optical wiring.

【*Discussion*】

In static characteristic, the device that has a 70-μm length DFB laser with the resistance of about 750 Ω obtained a maximum near 1.0 mA photocurrent at room temperature and the optical saturated current was near 10 mA. The thermal resistance can be assumed to be near 500 K/W based on the measurement results in chapter 4. Assuming the responsivity of PD is 1.0 A/W, the output power from 500 μm waveguide should be near 1.0 mW. These results almost agreed with the calculation results shown in Fig. 2.25, chapter 2. At 80 °C, the output power was over 0.4 mW, which is highly larger than the power requirement shown in chapter 2. In dynamic characteristics, the 3-dB bandwidth has a linear increase until the bias current near 2.3 mA shown in Fig. 5.14 (a), which also almost agrees with the calculation results shown in Fig. 2.27. The modulation efficiency estimated in room temperature of 10.3 GHz/mA$^{1/2}$ with a designed active volume of 1.89 μm^2 is a little smaller than the 10.8 GHz/mA$^{1/2}$ previous work with the active volume of 2.16 μm^2. The reason can be considered that the size error of device occurred from fabrication, or the differential gain in epi-wafer is smaller than before, which should be

investigated in the future.

In this experiment, the laser and PD cannot be measured separately, otherwise the device would be broken. Here gives the theoretical calculation of 3-dB bandwidth and explain the difference in this experiment and real optical wiring application. The calculation method is the same with that shown in chapter 2, while the absorption length was 200 μm and stripe width was 1 μm in this calculation. The load resistance was 50 Ω of the connected cable. The calculated 3-dB bandwidth is about 21 GHz at the bias voltage of -3 V shown in Fig. 5.16 (b). In the application of optical wiring, a large load resistance will be loaded in the PD circuit, for output a high drive voltage. In that case, the absorption length of device should be shortened as much as possible while maintaining an enough light absorption to reduce the junction capacitance.

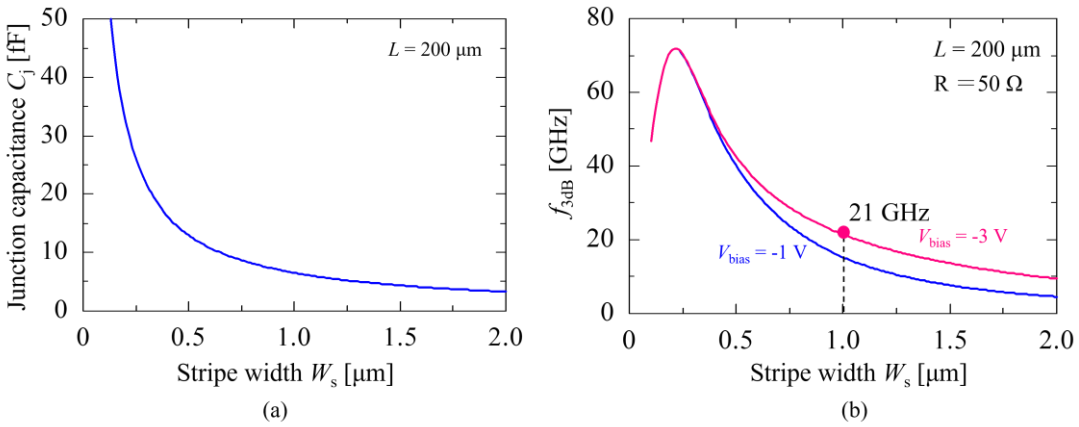


Fig. 5.16 (a) Calculated junction capacitance versus Stripe width, (b) calculated 3-dB bandwidth of fabricated membrane PD.

5.3 InP-rib waveguide integrated membrane optical link

5.3.1 Device structure

A GaInAsP wire waveguide was studied in the previous work and a 4 dB/cm low loss has been achieved[4]. The waveguide used in membrane optical link in section 5.2 and chapter 4 was a buried GaInAsP passive waveguide at the bandgap waveguide of 1.22 μm. This waveguide has advantages of low coupling loss, easy to integrate DBR structure, and great fabrication tolerance in straight waveguide structure. However, the side cladding layer of highly doped *p*-InP caused a high loss by free-carrier and intervalence absorption. 8 dB/cm was obtained in the previous work[3]. In addition, the buried GaInAsP waveguide was formed at the same time with *n*-, *p*-InP regrowth, the waveguide width may vary due to mismatch of regrowth mask when fabricating bending waveguide. Therefore, short distance on-chip optical interconnection is acceptable using this waveguide. In future prospect, a low loss waveguide is needed at the application of optical wiring under cm level transmission length. For this propose, a deeply etched InP rib-waveguide was proposed. The absorption could be ignored because only u-InP will be used in the structure, hence, scattering loss is mainly contributed to propagation loss. The deep-rib structure may have a larger scattering loss because that the optical field interacts with the side-wall roughness. However, the strong optical confinement leads to a short bend radius. In the compact and high-density integration of optical circuits, bending radius can be smaller than 10 μm. Considering the research propose of optical wiring using GaInAsP/InP membrane platform, the InP waveguide is easy to be integrated with membrane optical link.

The structure design of InP-rib waveguide has been studied in the previous work[5]. As the scattering loss increases with the waveguide width deceasing (strong optical confinement caused a high interaction between guided mode and sidewall of waveguide), the widest waveguide width was taken when the etching depth was fixed while maintaining a single TE_0 fundamental transverse mode. Based on the calculation, the structure of 220 nm etching depth and 420 nm width (laser core 270 nm) was chosen

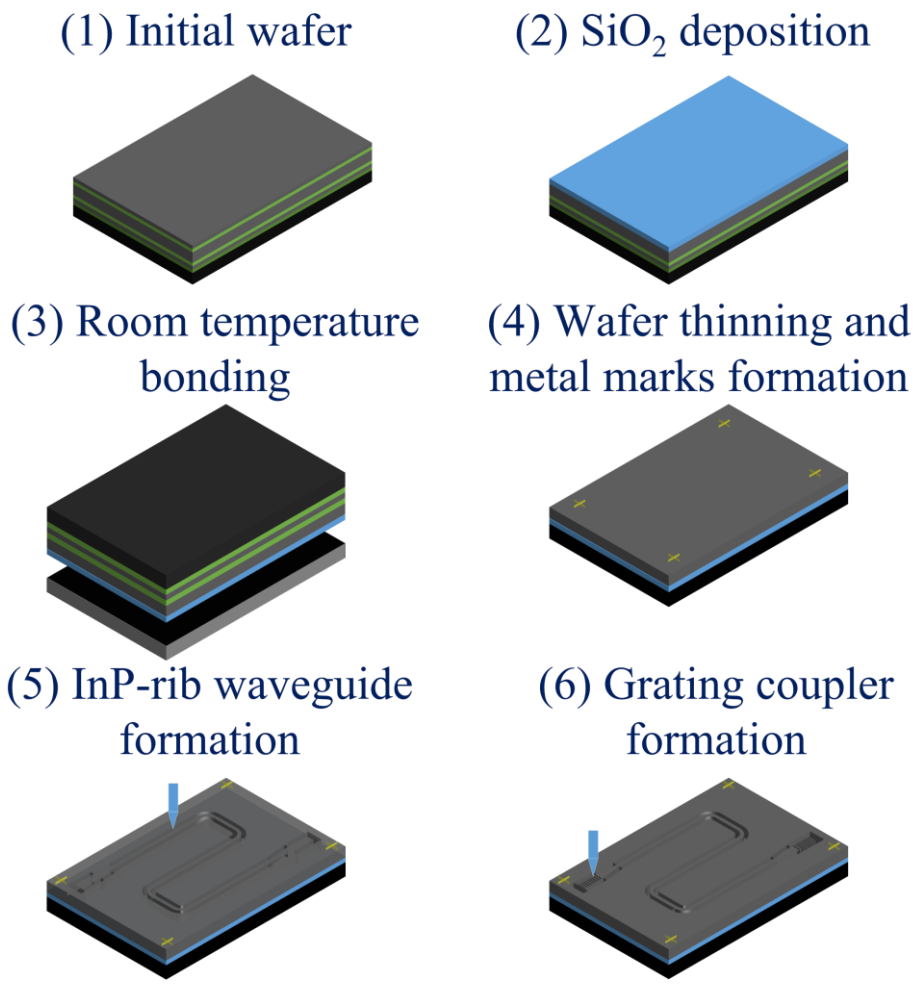


Fig. 5.17 Fabrication pross of InP-rib waveguide and grating coupler

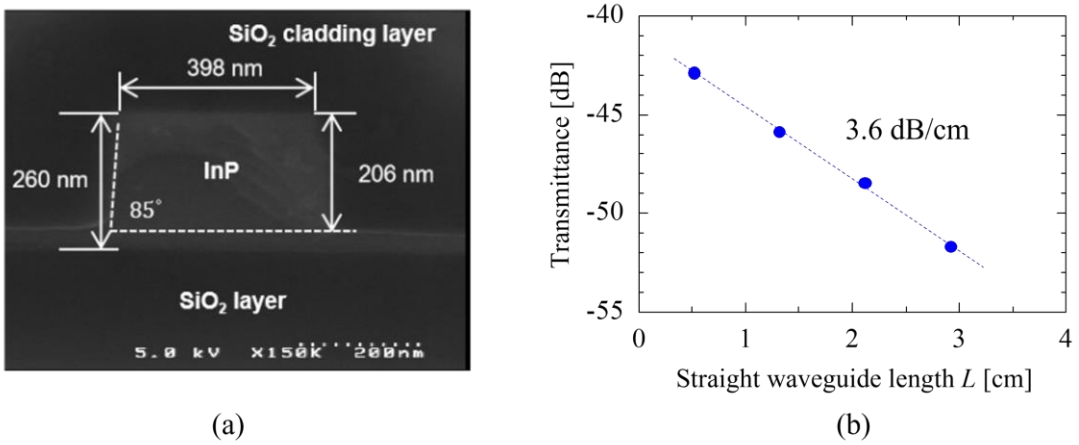


Fig. 5.18 (a) Fabricated InP-rib waveguide on Si substrate (b) transmission characteristics of fabricated InP-rib waveguide with 3.6 dB/cm loss[6].

considering 90º bending radius < 6 μm (assuming bending loss < 0.1 dB). The scattering loss could < 1dB/cm when assuming the roughness autocorrelation length of 22 nm, and line edge roughness of 2.5 nm ($3\sigma'$). The sidewall roughness strongly depends on the fabrication process. In previous works, the measurement of waveguide transmission characteristic was conducted by cleaving two side of waveguide and light was input and detected through lensed fiber. For enhancing the coupling and stability of measurement, a grating coupler for waveguide loss measurement was studied[6].

Figure 5.17 shows the fabrication process of InP-rib waveguide and grating coupler. The Initial wafer consists of 270-nm-thick u-InP core layer, GaInAs and InP etch stop layers and cap layers. The process started with SiO_2 cladding layer deposition in order to form the same cladding structure with membrane laser. Then, room temperature surface activated bonding assisted by a-Si nanofilm was followed. Before, waveguide formation, metal marks were evaporated for position alignment. 300-nm-thick ZEP-520A was spin coated on the substrate (500 rpm, 3 sec; 6400 rpm, 120 sec)). 220 μC/cm^2 exposure dose (100 kV acceleration voltage, 100 pA current) was used in EB lithography. Development time of 45 sec was used. The SiO_2 pattern transfer condition was the same with that discussed in chapter 4.2.3. Dry etching condition of InP was also the same with that discussed in chapter 4.2.3, while one cycle etching time was 1 min. 4 cycles + 40 sec were used in InP-rib waveguide and 75 sec × 2 etching in grating coupler formation. The InP-rib waveguide and grating coupler were formed in two times. Finally, the top SiO_2 cladding layer was deposited by PECVD.

Figure 5.18 (a) shows the sectional view of SEM image of fabricated InP-rib waveguide. The total thickness of 260 nm InP was slightly smaller than the design value of 270 nm, which was caused by regrowth error in OMVPE process. The transmittance was shown in the Fig. 5.18 (b). Longitudinal intercept equals to the sum of bending and coupling loss. A 3.6 dB/cm low propagation loss was obtained in the experiment with a sidewall roughness of 4.6 nm, which was smaller than the 4 dB/cm of GaInAsP wire waveguide, and ~ 8 dB/cm buried GaInAsP waveguide. However, this value was still larger than the expected propagation loss of 1 dB/cm. Further reducing the sidewall

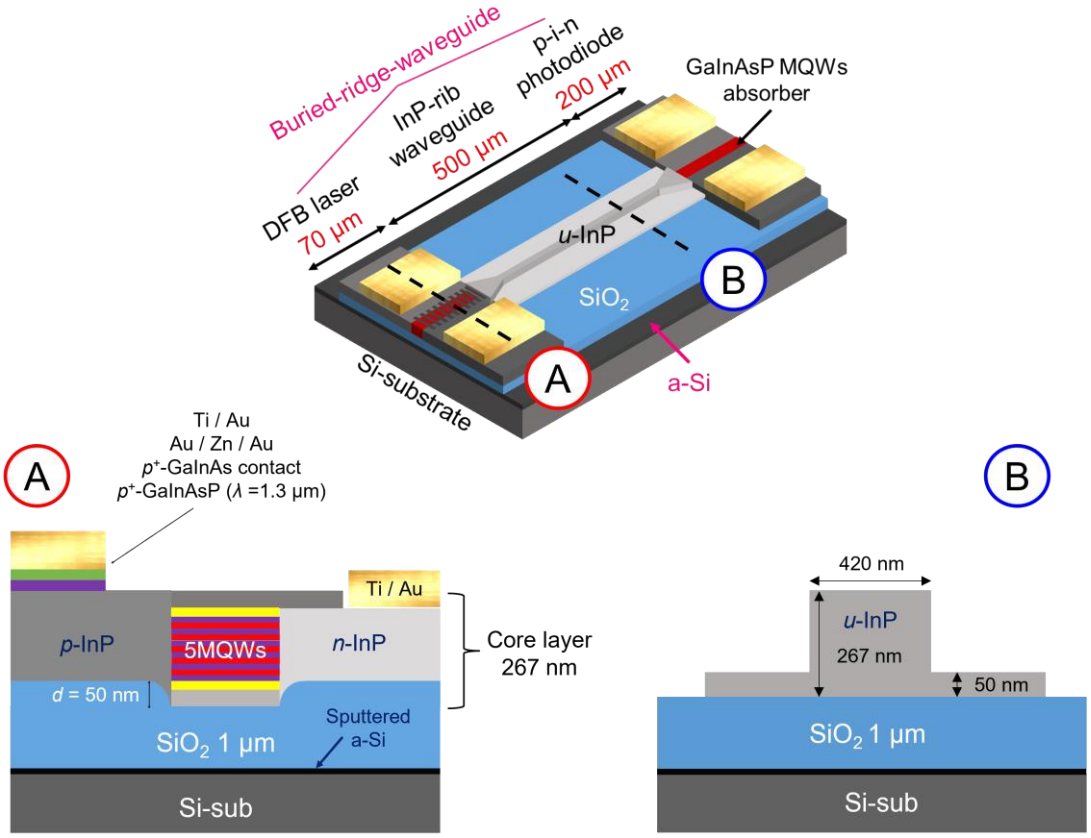


Fig. 5.19 Schematic of InP-rib waveguide integrated membrane optical link

roughness and optimizing the size of waveguide should be carried out.

After estimating the single device of InP-rib waveguide, the integration with membrane laser and p-i-n PD should be considered. Figure 5.19 shows the schematic of InP-rib waveguide integrated membrane optical link. The structure of membrane DFB laser and p-i-n PD are the same as described in section 5.2.1. The taper structure was used to connect membrane DFB laser, p-i-n PD to InP-rib waveguide. The u-InP layer can be formed by the same BJB regrowth method.

5.3.2 Fabrication process

The fabrication process is shown in Fig. 5.20 and Fig. 5.21. The whole process flow was the same as the process of GaInAsP integrated membrane optical link described in Fig. 5.2. Two fabrication steps should be changed. One is the regrowth material; another one is that two times EB lithography are needed. In step (2), the mesa formation should be etched to 1.3Q GaInAsP layer for removing the bottom 100 nm p-InP, although this p-InP could be changed to u-InP in initial epitaxial wafer. Subsequently, the u-InP was regrowth on whole wafer for formed a InP-rib waveguide material. After that, n-InP was only regrowth on two sides of active layer of laser and absorption layer of p-i-n PD. Finally, the p-InP was regrowth on one side of active layer of laser and absorption layer of p-i-n PD. The InP waveguide and taper structure was fabricated almost the same with that described in single InP-rib waveguide. The detailed process was shown as follows.

(12.1) ZEP resist spin coating

300 nm ZEP-520A was spin coated on the substrate as EB lithography resist.

(12.2) EB lithography

Dose: 220 μC/cm^2, voltage: 100 kV, current: 100 pA.

(12.3) Development

ZED-N50 45sec, IPA 60sec.

(12.4) SiO_2 mask transfer

The resist pattern was transferred onto SiO_2 (25 nm) by CF_4 RIE (CF_4: 10 sccm, Pressure: 1 Pa, Power: 25 W, Time: 10 min).

(12.5) ZEP removal

ZEP-520A was removed by O_2 plasma ashing (RIE, O_2: 30 sccm, Pressure: 10 Pa, Power: 50 W, Time: 10 min).

(12.6) InP etching

The InP layer was etched by CH_4/H_2 RIE (CH_4: 10 sccm, H_2: 40 sccm, Pressure: 6 Pa, Power: 100 W, Time: 1 min, 5 cycles)

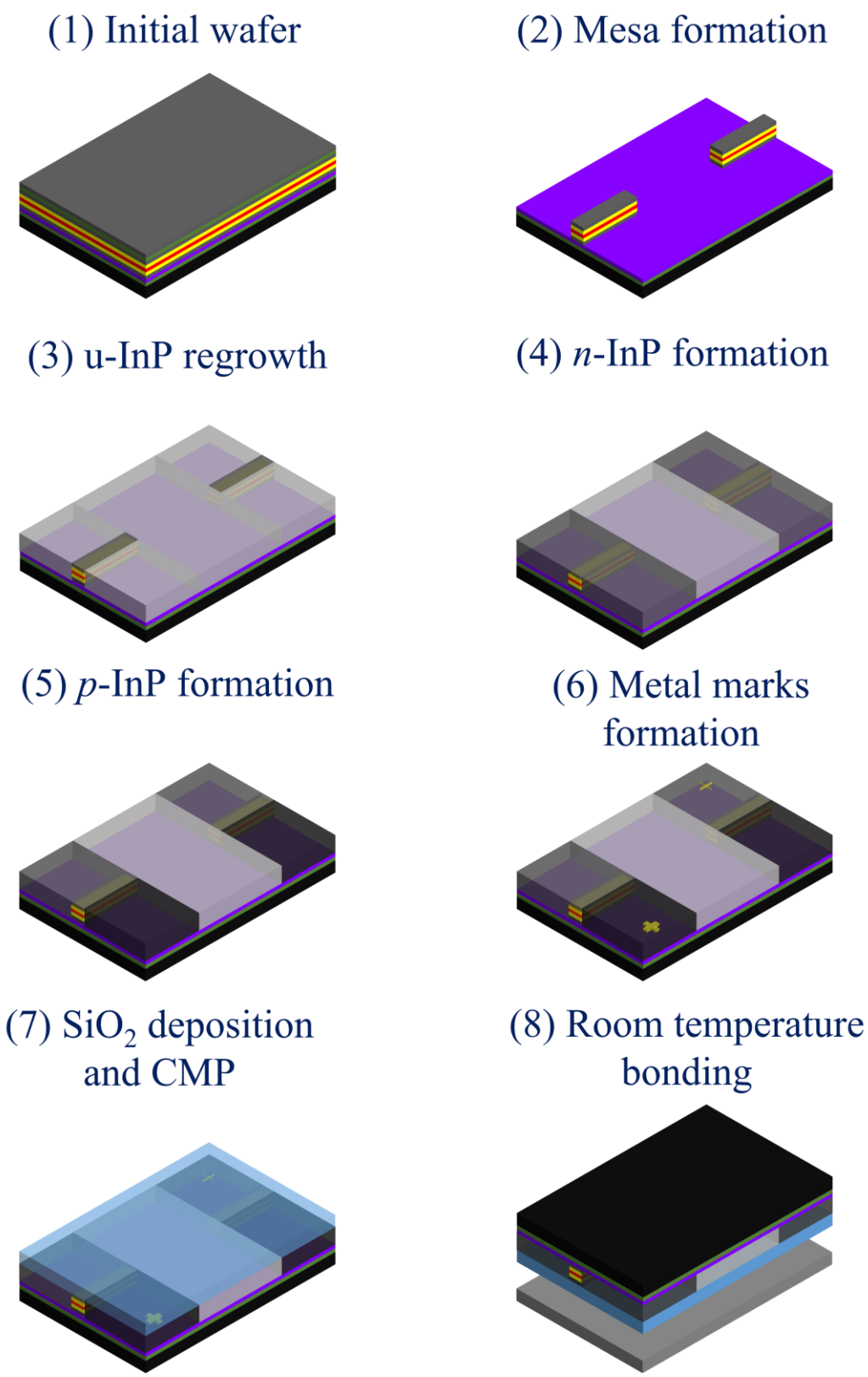


Fig. 5.20 Fabrication process of InP-rib integrated membrane optical link (Initial epitaxial wafer preparation to room temperature bonding)

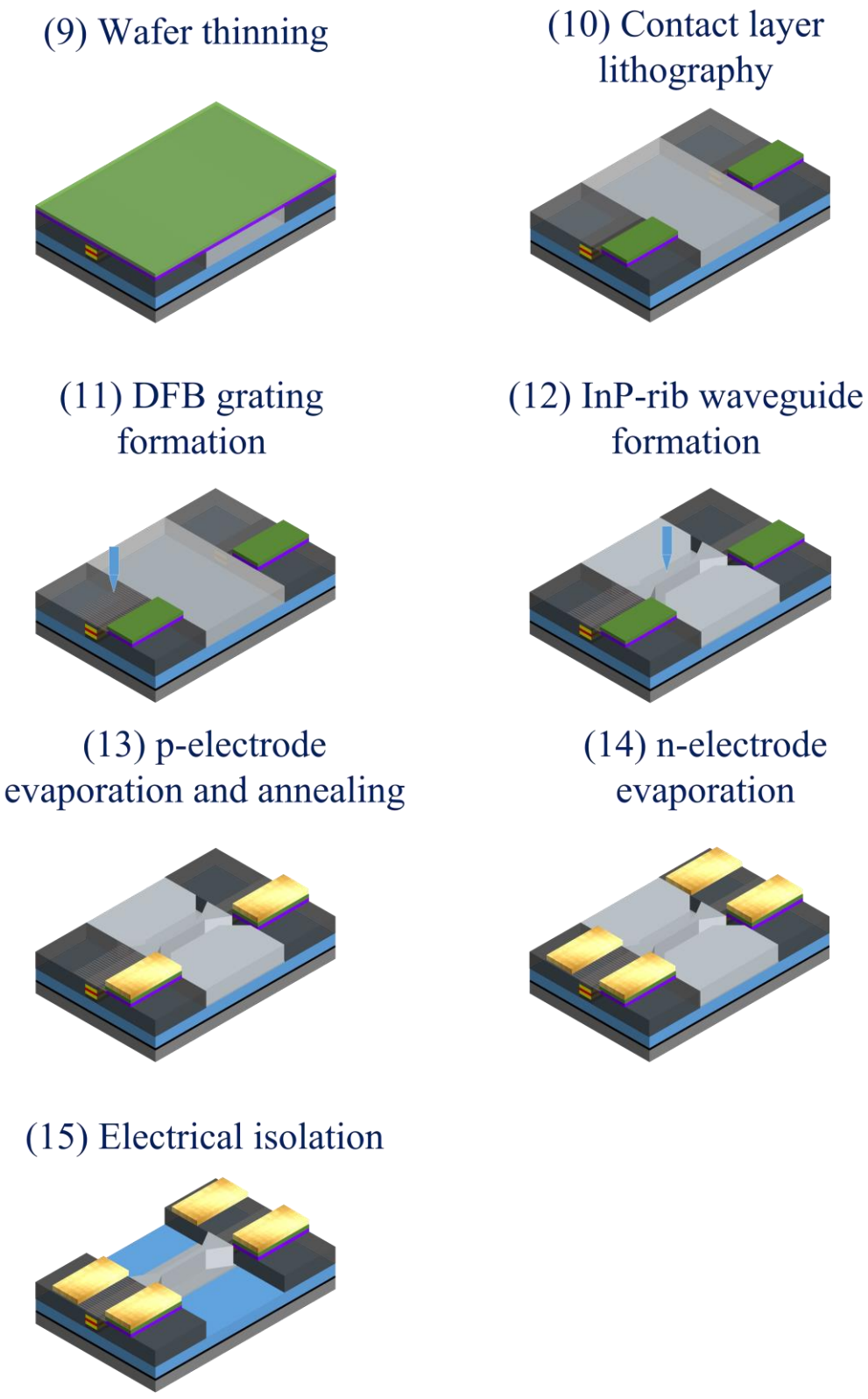


Fig. 5.21 Fabrication process of InP-rib integrated membrane optical link (wafer thinning to electrical isolation)

5.3.3 Preliminary experimental results

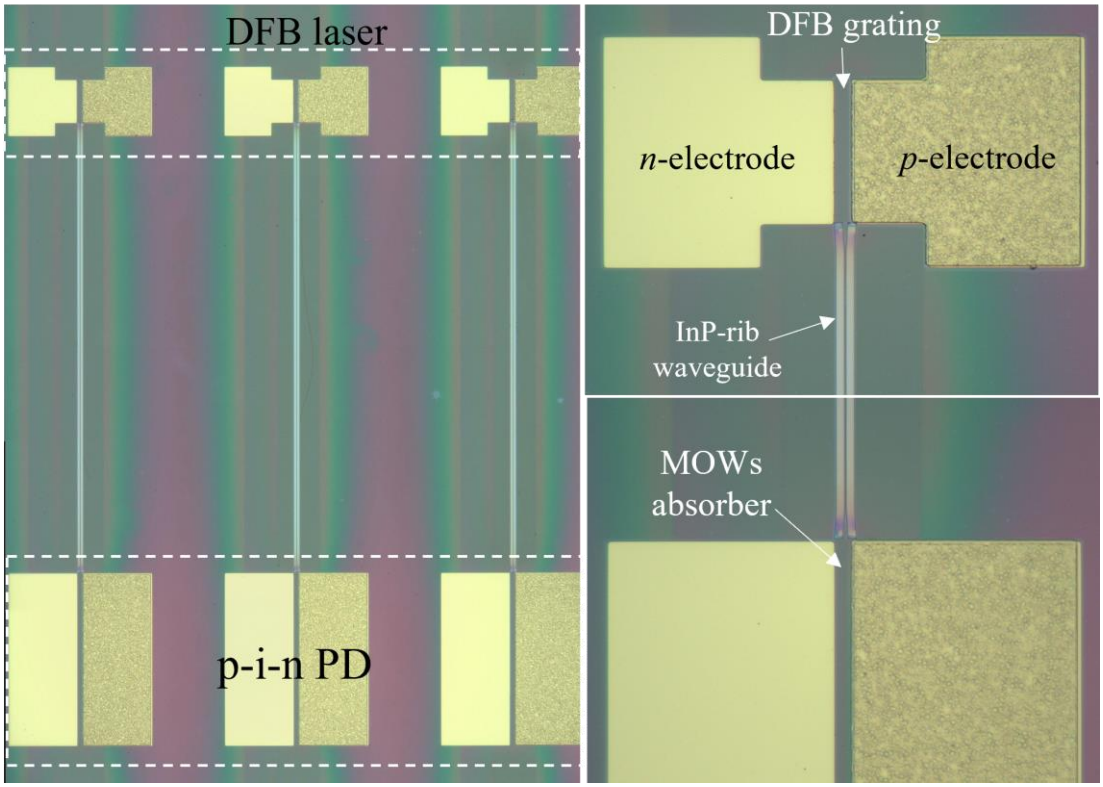


Fig. 5.22 Optical microscope images of fabricated device (before electrical isolation)

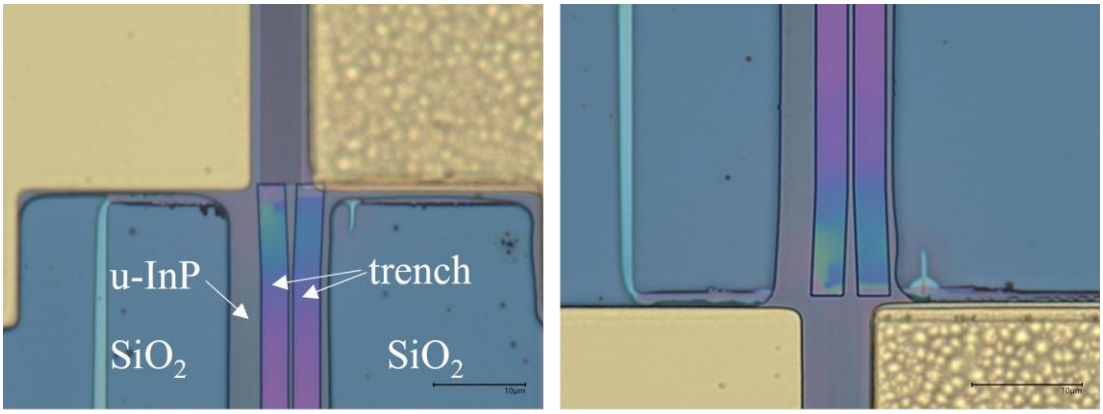


Fig. 5.23 Optical microscope images of fabricated device (after electrical isolation) (a) front side of membrane DFB laser (b) front side of p-i-n PD

Figure 5.22 shows the top view of fabricated membrane optical link integrated with InP-rib waveguide. One cell of device includes only membrane DFB laser, InP-rib waveguide and p-i-n PD. The device was fabricated at the same wafer with the device using GaInAsP buried waveguide described in section 5.2. Therefore, the active region has the same PL peak at room temperature without current injection of 1549 nm. The cavity length of DFB laser was from 30 to 150 μm. The trench width was fixed at 3 μm. 500 to 1000 μm waveguide length were fabricated. And the absorption length of p-i-n PD was also fixed at 200 μm. Figure 5.23 shows the top view of fabricated device after electrical isolation process. The different color near trench of taper structure was due to the regrowth thickness difference near regrowth mask.

Figure 5.24 shows the static I_{LD}-I_{PD} characteristics at room temperature with the grating pitch from 291 to 305 nm. The blue line represents the I_{LD}-I_{PD} before electrical isolation process, and the red line represents the I_{LD}-I_{PD} after electrical isolation process. The light transmission through InP-rib waveguide was confirmed at the first time in membrane

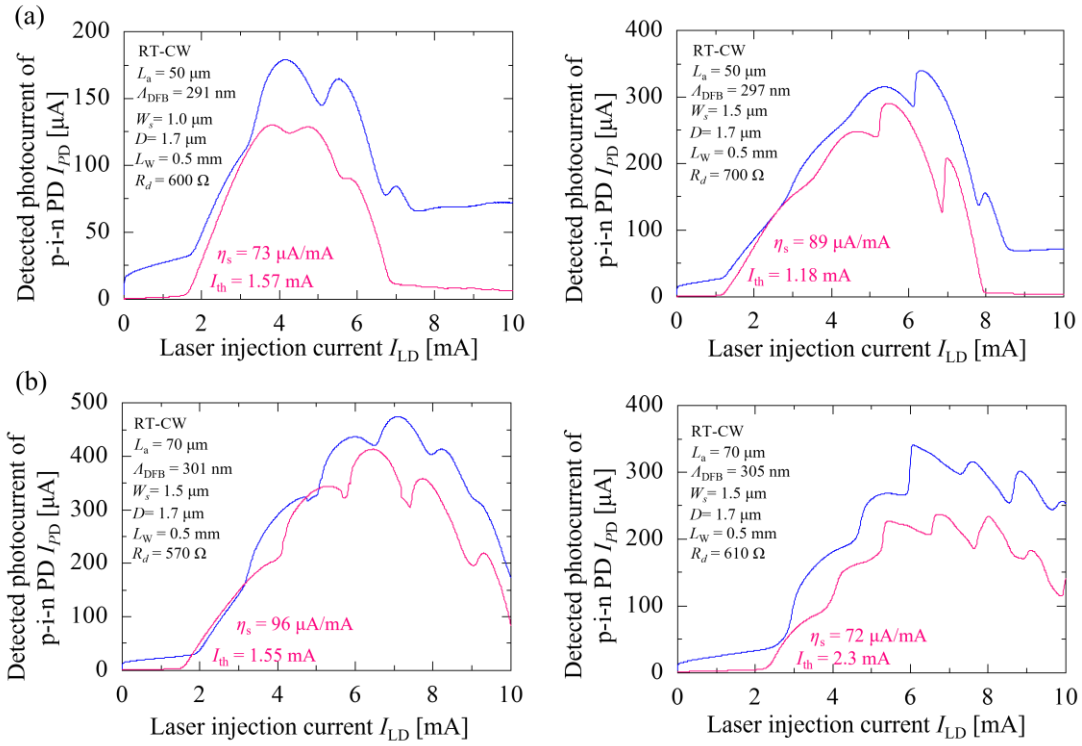


Fig. 5.24 I_{LD}-I_{PD} characteristics with different cavity length of DFB laser (a) 50 μm and (b) 70 μm (blue line: before electrical isolation, red line: after electrical isolation)

optical link. However, there were large threshold currents over 1.0 mA at each grating pitch and cavity length. The slope efficiencies were dropped at the range from 70 ~ 100 μA/mA, which was smaller than the device using GaInAsP buried waveguide. The detected photocurrents were also smaller than the device using GaInAsP buried waveguide, and the maximum detected photocurrent was ~ 410 μA after electrical isolation process.

【*Discussion*】

The internal differential quantum efficiency η_i (injection efficiency) of InP-rib waveguide integrated device should be the same as the device with GaInAsP buried waveguide for the reason of those two types of devices were fabricated at the same wafer and the same electrical isolation etching process was carried out. The difference in structure of two types of devices is the coupling with front and rear waveguide. In the GaInAsP buried waveguide integrated device, the front and rear side of membrane DFB laser were coupled well with waveguide, and in the rear side, another p-i-n PD was followed to absorb light, hance, the influence of feedback light was small. This can also be found in smooth I_{PD}-I_{LD} curves. In InP-rib waveguide integrated devices, the back side of membrane laser was a bare InP layer. No light can be guided in this region, so, the feedback from back side can be ignored. At front side, low slop efficiency represents a low summation of coupling loss and propagation loss. Considering the short transmission length of waveguide, the worse coupling efficiency between laser, p-i-n PD to taper was predominant, which can be contributed to the misalignment between taper and waveguide of laser cavity. In addition, based on the fabrication process shown in Fig. 5.20, the sequence of epitaxial regrowth was 1).*u*-InP, 2). *n*-InP and 3). *p*-InP. The design of regrowth masks was shown in Fig. 5.25. For fabricating am undoped InP-rib waveguide, a u-InP region should be protected in the n- and p-InP regrowth. However, if the misalignment occurred in the UV lithography, the layers at the facet between laser and taper waveguide would become complicated, which also leads to an optical mode

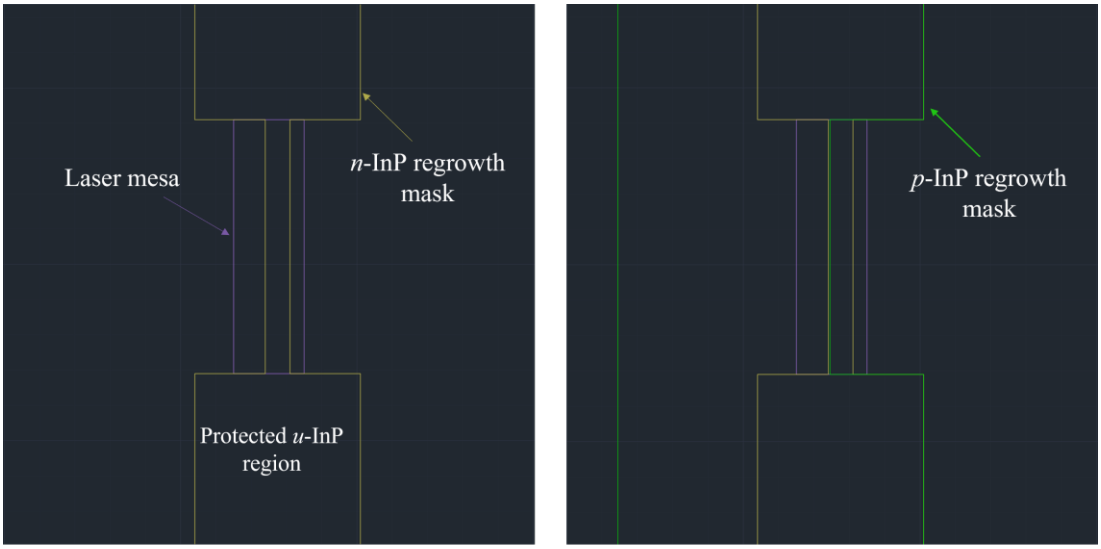


Figure 5.25 Regrowth masks design of (a) *n*-InP (yellow line) and (b) *p*-InP regrowth (green line)

mismatch at the facet and reflection. The same thing happens around p-i-n PD absorber at the same time. Therefore, an external oscillation would occur in waveguide. Many kinks appeared in I_{PD}-I_{LD} curves of Fig. 5.24 proving that strong light feedback effect existed in InP-rib waveguide integrated devices. The light feedback gives a change in mirror loss of laser, and the change in mirror loss gives rise to a shift in the threshold modal gain and threshold carrier density. The perturbed threshold current can be described as follows:

$$I'_{th} = I_{th} - |\Delta I_{th}|\cos(2\beta L_p) \tag{5.1}$$

where L_p is the length of passive cavity, β is the propagation constant, ΔI_{th} can be found by defining a differential gain per unit current density[7]. When the external reflection is in phase, the threshold current decreases due to an increase in effective mirror reflection. When the external reflection is out of phase, the threshold current increases due to a decrease in effective mirror reflection.

5.4 Comparison and future prospects

This sub-section describes the comparison between this work and works in NTT's group, and future prospects about membrane photonic integrated circuits. In this work, room temperature direct bonding for membrane optical link was achieved in chapter 3. Low thermal resistance membrane lasers were obtained in chapter 4. High-temperature and high efficiency membrane optical link has been realized in chapter 5.2. The NTT's group achieved a membrane laser on SiO_2/Si substrate at beginning, the comparison will be introduced in section 5.4.1. The InP-rib waveguide integrated membrane optical link was fabricated preliminary and static characteristic was measured and discussed in section 5.3. However, some problems still existed in this device. The proposal of low power consumption and high-speed membrane optical link was described in section 5.4.2 including the process optimization. The direct bonding process discussed in the previous chapters showed a bonding interface of SiO_2-Si. In the application of optical wiring on Si-LSI, the bonding interface should be SiO_2-SiO_2 considering a SiO_2 cover layer existing on the surface of LSI device layer. Section 5.4.3 describes a modified SiO_2-SiO_2 surface-activated bonding at room temperature assisted by a-Si nanofilm for membrane optical link on Si-LSI substrate.

5.4.1 Comparison

As introduced in chapter 1, the investigation of membrane laser in NTT's group started with the direct bonding of GaInAsP/InP membrane on Si substrate by O_2 plasma activated hydrophilic bonding. Since their research did not focus on the on-chip optical wiring, the device design and fabrication process are different with our design. Here, the different points in device design and fabrication process are listed again.

- **Difference in device design.**
  1. The cavity length was long (usually > 70 μm) for high output power coupling to optical fiber, while in our work, the cavity length was short for low threshold current operation. Although they demonstrated the ultra-short cavity length of 5 μm membrane laser with twin DBR mirror. In most cases, the cavity length was

longer than that in our work.

2. In surface grating, the coupling coefficient κ was several hundred cm^{-1} using SiO_2 or SiN for low scattering loss, while in our work, κ was designed very large (1 ~ 2 thousand cm^{-1}) for low threshold current operation.
3. In membrane structure, the SiO_2/Si was always used in our work considering the application of on-chip optical wiring. While, recently, the SiC substrate was used also as the cladding layer for high heat dissipation structure in their works as shown in chapter 1.

➢ **Difference in fabrication process.**

1. In their work, an active layer was bonded on Si substrate by O_2 plasma activated hydrophilic bonding at first, then, the buried heterostructure was formed by epitaxial growth an ion diffusion. While, in our work, considering the CMOS compatibility, the epitaxial growth was finished before integration to the Si substrate.

Based on the difference discussed above, for comparison with their work, a similar device structure design was selected as blow.

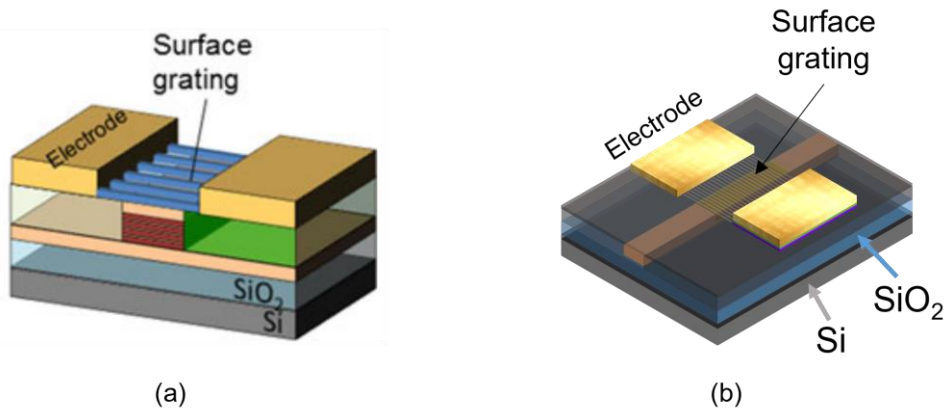


Fig. 5.26 Device structure of membrane DFB laser on SiO2/Si (a) NTT's group[8], (b) our lab.

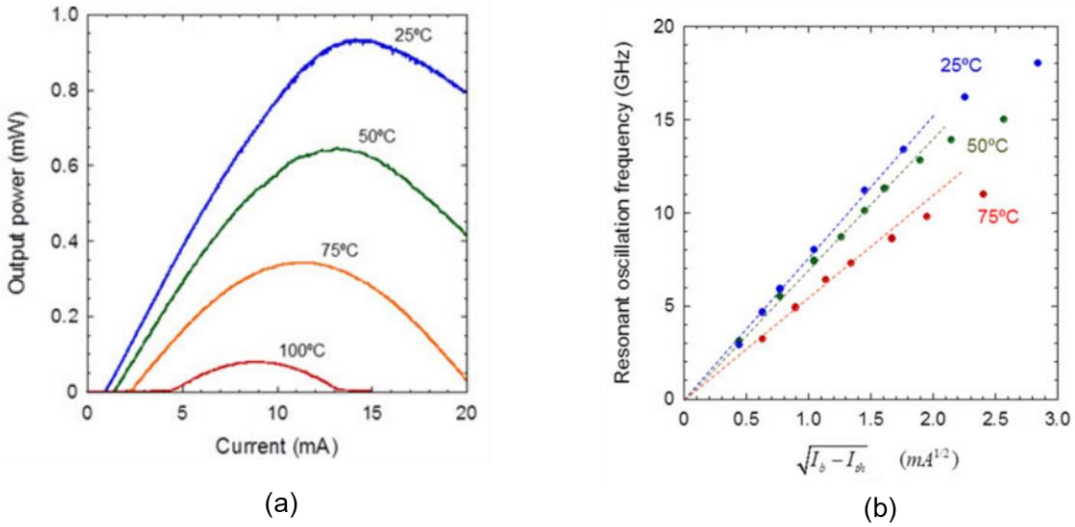


Fig. 5.27 Membrane DFB laser characteristics in NTT's group[8] (a) I-L characteristic (b) modulation efficiency.

Figure 5.26 shows the membrane DFB laser on SiO_2/Si in NTT's group[8] and our lab. The cavity length was 73 μm which is similar with the device shown in this thesis (70 μm). The strip width was 1 μm. The active layer with 6 quantum wells was sandwiched by 50-nm InP layers and the core layer was 250 nm in total. Figure 5.27 shows the static and dynamic characteristics. The threshold current in 25 ˚C was 0.9 mA with the coupling coefficient of 600 cm^{-1}. The maximum output power was 0.93 mW. The slope efficiency was about 0.09 W/A from Fig. 5.27 (a). The differential resistance was estimated as 172 Ω (3.5 ~ 4.5 times lower than this work), and a 100 ˚C CW (120 ˚C in this work) operation was achieved. In the temperature operation, $d\lambda/dT$ of 0.08 nm/K (same with that shown in chapter 4) and $d\lambda/dP$ of 0.0556 nm/mW (a little larger than that shown in chapter 4, 0.041 nm/mW) were calculated, which leads to a thermal resistance of 697.7 K/W. In the modulation efficiency, a 7.7 GHz/$mA^{1/2}$ slope was obtained in the room temperature, which is a little higher than that (6.8 GHz/$mA^{1/2}$) shown in Fig. 5.14 (a). This difference may come from the different differential gain in active layers. The energy cost of 25.8 Gbps was 171 fJ/bit (bias current of 3.2 mA) while in our device the value was about 470 fJ/bit in 25 Gbps (bias current of 3.5 mA, the device with a grating pitch of 293 nm).

In summary, the devices demonstrated in this thesis were comparable with the work in NTT's group. The threshold current in our device 0.2 ~ 0.4 mA (different grating pitch) is small thanks to the BRW structure. The slope efficiency in our DFB laser shown in section 5.2.3 was estimated about 0.12 ~ 0.2 W/A assuming the responsivity of integrated PD is 1 A/W, which is high thanks to the well coupled integrated structure. The thermal resistance is this work was about 500 K/W with the cavity length of 70 μm, which is a little lower than that in NTT's work. The maximum operation temperature in our work was 120 ˚C thanks to the lowered quantum well thickness (5.4 nm/well). The differential resistance in our device is about 4 times larger than that in NTT's group, which leads to a large power consumption. Table 5.2 shows the summary of the comparison.

Table 5.2 Comparison with the device in NTT's group with similar device design.

Parameters		**NTT**	**This thesis**
Cavity length [μm]		73	70
Stripe width [μm]		1	1
Core layer thickness [nm]		250	270
Quantum well number		6	5
Threshold current [mA]		0.9	0.2 ~ 0.4
Slope efficiency [W/A]		0.09	0.12 ~ 0.2 (Assuming 1 A/W in PD)
Differential resistance [Ω]		172	600 ~ 800
Maximum output power [mW]		0.95	0.95 ~ 1.1 (Assuming 1 A/W in PD)
Maximum operation temperature [°C]		100	120
Thermal resistance [K/W]		697.7	500 ~ 640
Modulation efficiency of f_R [GHz/mA$^{1/2}$]	25 °C	7.7	6.8
	50 °C	7.0	5.8
	80 °C	5.5 (75 ˚C)	4.8
Energy cost [fJ/bit] at 25 Gbps 25 °C		171	470

5.4.2 Proposal of low power consumption membrane optical link

【Requirement of lower power consumption MPIC】

For achieving a low power consumption of membrane laser (< 10 fJ/bit), the required receiving power of PD and the link loss should be reduced. Since the previous work[9] demonstrated the absorption length of PD could be shorten to 12 μm (stripe width = 0.8 μm), the junction capacitance could be reduced, and a larger load resistance could be used. The larger load resistance, the smaller required receiving power and 3-dB bandwidth of PD. Figure 5.28 summarized the power requirement of PD and LD in various operation conditions. It shows that if the link loss could be reduced to 2.2 dB (theoretical value), the required laser output power could be reduced to -20.81 dBm (8.30 μW) for 10 Gbps, -16.55 dBm (20.70 μW) for 20 Gbps operation at 20 °C, with the load resistance of 40

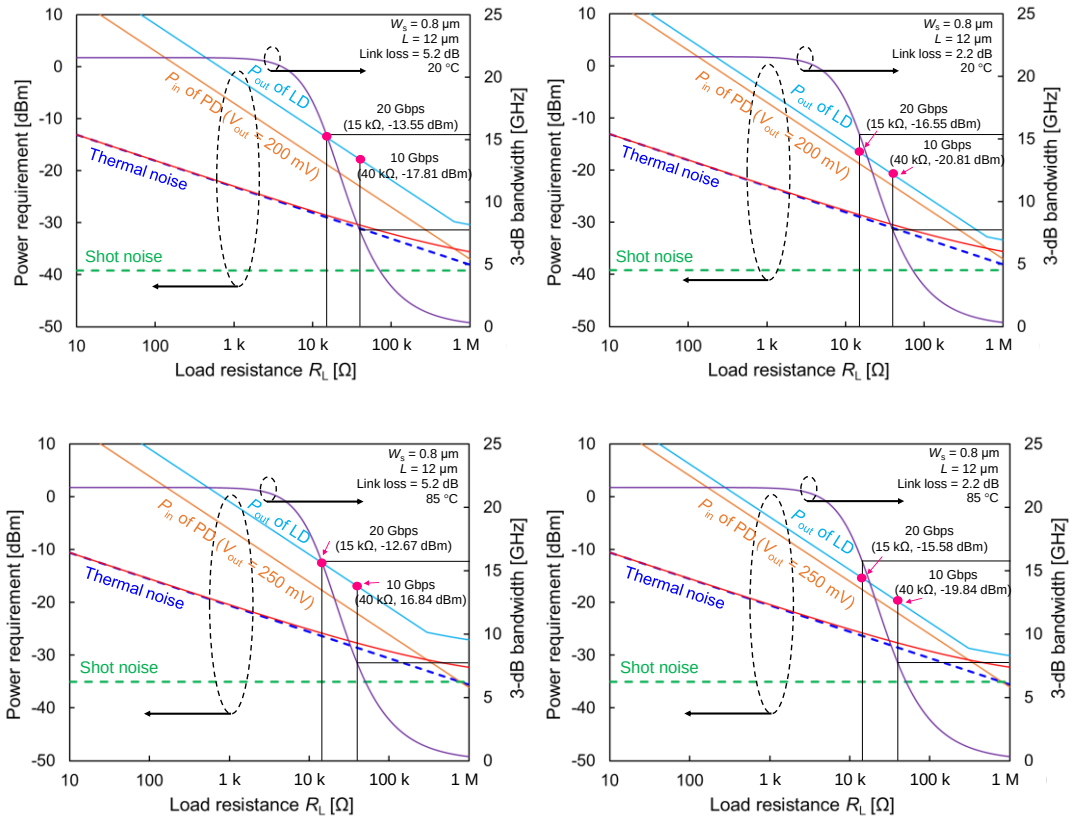
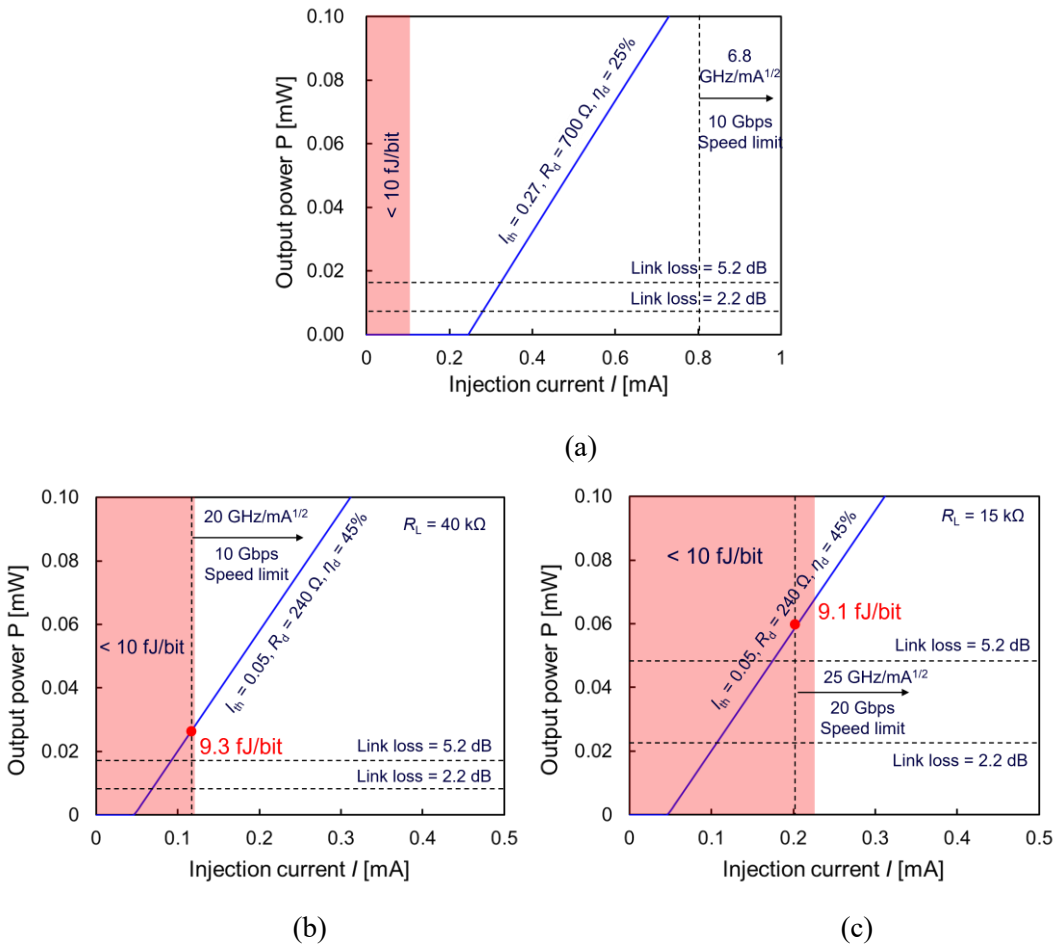


Fig. 5.28 Power requirement of membrane laser in on-chip optical interconnection.

kΩ and 15 kΩ, respectively. At 85 °C, -19.84 dBm (10.38 μW) for 10 Gbps, -15.58 dBm (27.67 μW) for 20 Gbps operation, which is smaller than that calculated in chapter 2.2, because of the smaller capacitance and larger load resistance.

Figure 5.29 shows the calculation of SAB membrane laser for achieving the energy cost < 10 fJ/bit. Figure 5.29 (a) shows the SAB membrane DFB laser shown in Fig. 5.12. The red region indicates the bias current range of energy cost smaller than 10 fJ/bit. The required bias current limitation is about 0.11 mA with the differential resistance of 700 Ω. Because of the extremely bias current and a 0.82 V threshold voltage, reduction of differential resistance has little effect on increasing the 10 fJ/bit energy cost required current limitation. The modulation efficiency of 6.8 GHz/mA$^{1/2}$ of f_R limited the required



(a)

(b) (c)

Fig. 5.29 Energy cost of laser (a) current SAB DFB laser, (b) calculated SAB DR laser in 10 Gbps modulation speed for < 10 fJ/bit, (c) calculated SAB DR laser in 20 Gbps modulation speed for < 10 fJ/bit.

bias current of achieving 10 Gbps data transmission bandwidth. The speed limit line is outside the energy requirement red region (speed limit current > energy consumption limit current), which means that for achieving the modulation speed of 10 Gbps, it is impossible to have the energy cost < 10 fJ/bit in this SAB membrane DFB laser (threshold current was also larger than 0.11 mA). Figure 5.29 (b) and (c) show the calculation results of SAB membrane DR laser. The differential resistance of 240 Ω (0.12 mA of energy limit) can be expected by shortening the distance between electrode and active region and increasing the doping concentration of *p*-InP. The threshold current of 0.05 mA was assumed, which can be expected to be achieved by introducing ultra-short cavity length of 5 μm (twin DBR structure at rear and front waveguide can be considered) and reducing the scattering loss of grating. The results show that at least 20 GHz/mA$^{1/2}$ modulation efficiency of f_R for 10 Gbps and 25 GHz/mA$^{1/2}$ modulation efficiency of f_R for 20 Gbps operation are needed to make the speed limit current smaller than energy limit current (speed limit line inside red region). Since the required power of laser is quite small by using the large load resistance, the power is enough with the external efficiency of 45%. If the link loss can be reduced to 2.2 dB, the 30 % and 25 % external efficiency is enough in Fig. 5.29 (b)

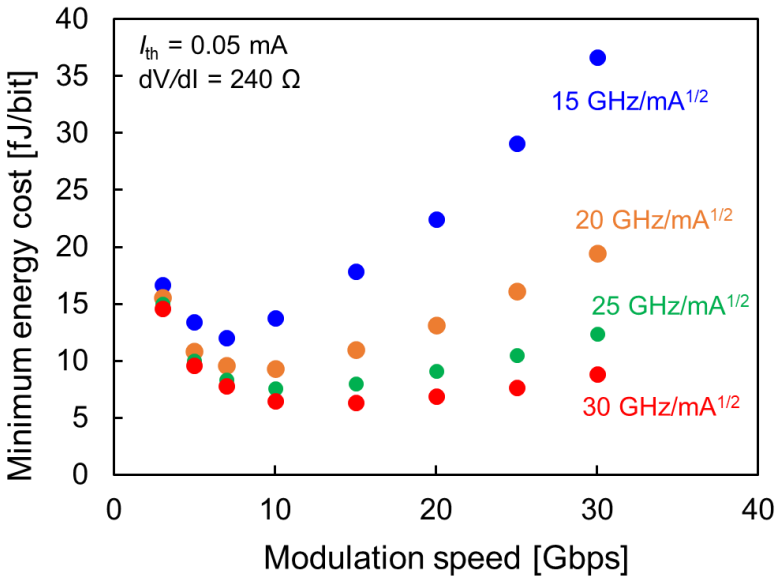


Fig. 5.30 Calculated minimum energy cost of membrane laser with different modulation efficiency of f_R.

and (c), respectively. It is possible to achieve the energy cost < 10 fJ/bit if the above conditions are meted in the future.

Figure 5.30 shows the minimum energy cost of membrane laser with different modulation efficiencies of f_R. The result shows that the modulation speed that has the minimum energy cost increased with the modulation efficiency increased, and within the modulation efficiency < 30 GHz/mA$^{1/2}$, the energy cost in 10 Gbps operation is smaller than 20 Gbps operation.

【Device design】

To achieve a low power consumption and high-speed membrane optical link, some improvement should be performed.

1). A structure with high process tolerance and high coupling efficiency between InP-rib waveguide to membrane laser and PD should be studied, especially between buried ridge waveguide of active layer to InP-rib waveguide.

2). The regrowth procedure of u-InP should be optimized. The suggestion of regrowth sequence change for process optimization is shown in Fig. 5.31. The *u*-InP was changed to the third step, which has two merits to the process. One is that after regrowth of *n*- and

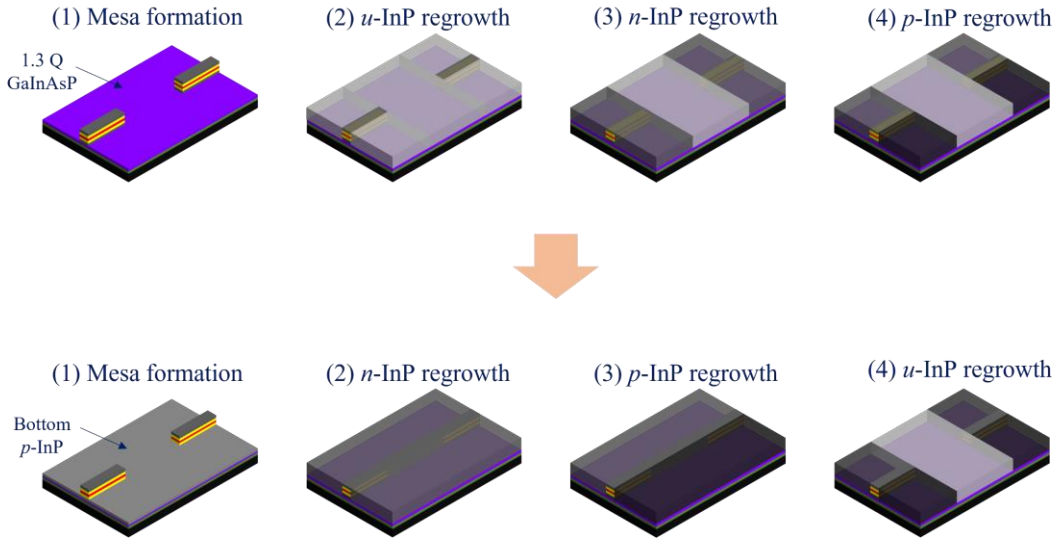


Fig. 5.31 Regrowth sequence change for process optimization

p-InP, misalignment will not occur in the regrowth in *u*-InP, and a clear facet will be formed between active region and InP-rib waveguide. Another one is that the electrical isolation between laser and p-i-n PD will be formed naturally while finishing the *u*-InP at last.

3). Integration of a GaInAs-bulk membrane p-i-n PD. The p-i-n PD used in chapter 5.2 and 5.3 was a MQWs p-i-n PD. For achieving an enough light absorption, 200 μm length was used. In that experiment, the PD was operated in reverse bias and the load resistance was 50 Ω by the connected cable. Therefore, the RC constant was determined by junction capacitance and 50 Ω load resistance. The calculated 3-dB bandwidth of PD was 21 GHz. However, in the application of optical wiring, a large load resistance will be loaded in the PD circuit. The 3-dB bandwidth will become small using current structure (2.5 GHz 3-dB bandwidth in calculation). The detailed calculation had been shown in Fig. 5.28.

4). Integration of a membrane DR laser to increase external efficiency. In previous structure of membrane DR laser, the surface DBR grating was formed at the same time with DFB grating, for the core material was both GaInAsP. In the case of InP waveguide, we are focusing the design of a new DBR structure in a InP-rib waveguide integrated circuits. The results showed that a shallow-etched InP-rib waveguide at the back side of DFB laser was needed, and a 97% coupling efficiency can be obtained with the laser active region width of 0.8 μm and shallow-rib waveguide width of 1.2 μm while keeping the single mode condition.

5). Reducing threshold current less than 0.1 mA by introducing ultra-short cavity length or redesign the core layer and the scattering loss should also be reduced by optimizing the fabrication process or using other materials as surface grating.

6). The thermal resistance is low enough now, and since the bias current is small, the reduction of differential resistance also has little influence on power consumption < 10 fJ/bit. The most importance for achieving low power consumption < 10 fJ/bit at 10 Gbps is to enhance the modulation efficiency higher than 20 GHz/mA$^{1/2}$.

Figure 5.32 shows the final design of membrane optical link towards low power consumption, high-efficiency, high-speed and high-temperature operation at cm order data transmission. The optical link was bonded on Si by room temperature surface activated bonding. The membrane DR laser consists of DFB section and an integrated shallow-etched InP-rib DBR. DR structure enhanced the efficiency and output power at the front side of laser. The BRW structure enhanced the lateral optical confinement and reduced electrical resistance indirectly. Deep-etched InP-rib waveguide can adapt compact and high-density optical integration. The BRW GaInAs bulk p-i-n PD with back DBR has the small size and large modulation bandwidth. However, as introduced the u-InP and GaInAs, the regrowth process should be four times and three times of EB lithography are needed for DFB, DBR grating and InP waveguide, which makes the fabrication process more complicated.

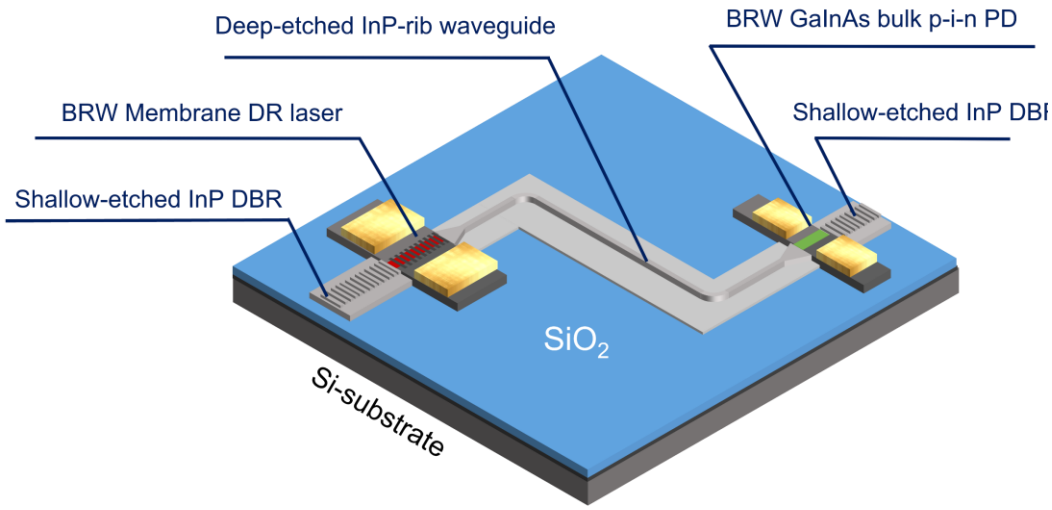


Fig. 5.32 Membrane optical link includes BRW membrane DR laser, deep-etched InP-rib waveguide and BRW GaInAs bulk p-i-n PD with back DBR bonded on Si by room temperature surface activated bonding

5.4.3 SiO_2-SiO_2 room temperature bonding for membrane link on Si-LSI

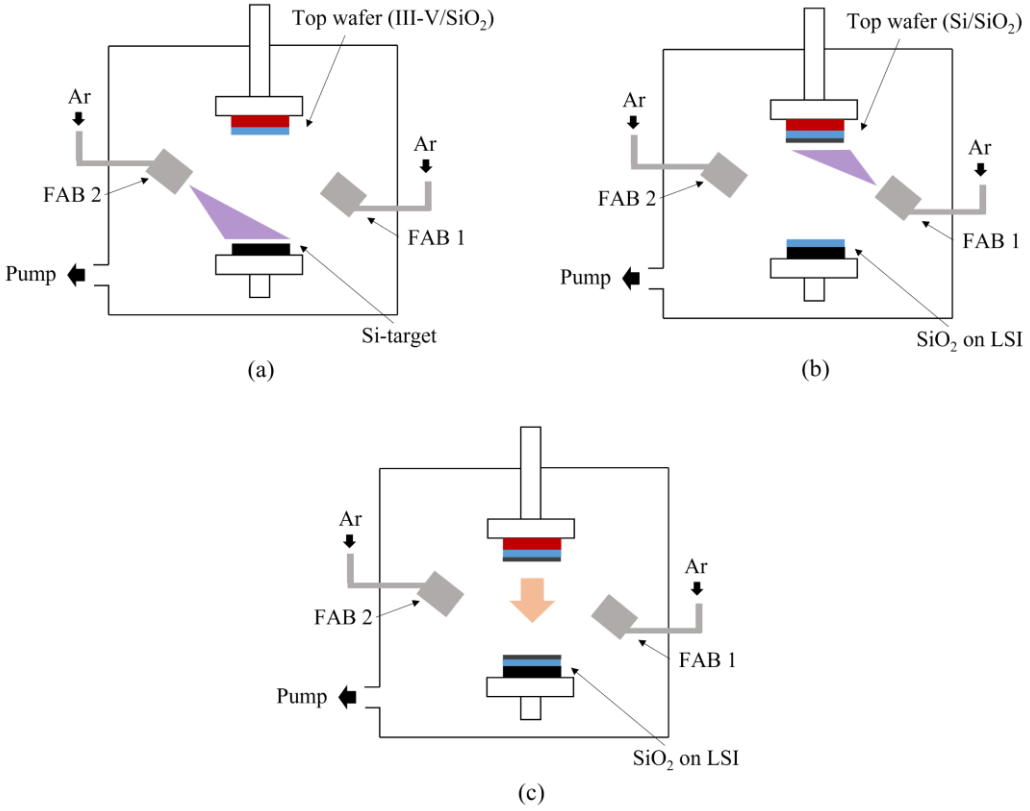


Fig. 5.32 SiO_2-SiO_2 room temperature surface activated bonding assisted by a-Si nanofilm

The surface activated bonding process used in membrane optical link on Si substrate was the SiO_2-Si bonding assisted by a-Si. One time sputtering was needed in which process. 100 mA, 15 min was used in the sputtering step. From Fig. 3.31 (b) in chapter 3, the thickness of sputtered a-Si was 5.6 nm. In the application of optical wiring on Si-LSI, the surface of Si-LSI would be a SiO_2 cover layer, therefore, a SiO_2-SiO_2 room temperature surface activated bonding should be investigated. Figure 5.32 shows a method of bonding process. Two times of sputtering should be carried out in this method. First, a target Si wafer was set on the bottom side of chamber, and an Ar-FAB (FAB2 of Fig. 5.32 (a)) was used to irradiate the target Si wafer for the first sputtering, which was the same as described in Fig. 3.25. A thin a-Si was deposited on the surface of SiO_2 of upper chucked wafer. Subsequently, FAB1 (Fig. 5.32 (b)) was used to irradiate the upper

chucked wafer for the second sputtering. Then, a thin a-Si will be deposited on the surface of SiO_2 cover layer on Si-LSI substrate. Finally, two wafers are brought into contact (Fig. 5.32 (c)) without any annealing. Since the conversion ratio (deposited a-Si / consumed a-Si) of sputtering is not clear in the sputtering process on the chamber using Ar-FAB irradiation, for achieving a uniform sputtering of a-Si, the sputtering time of 20 min in the first time and 10 min in the second time should be reasonable.

5.5 Conclusion

In conclusion, we have demonstrated a SAB-MPIC with BRW structure working under various stage temperature. The membrane DFB lasers have the low threshold current at the range of 0.2 ~ 0.4 mA in the cavity length shorter than 70 μm at room temperature. The highest slope efficiency of 0.203 mA/mA was obtained at 25 °C, and most of the devices have the efficiency of > 0.12 mA/mA, which shows a high efficiency operation of MPIC using membrane DFB laser and MQWs p-i-n PD was obtained. Large photocurrent of > 1.0 mA was detected at 25 °C and > 0.2 mA were detected at 100 °C. This high output thanks to the low thermal resistance of direct bonded membrane DFB laser. The recorded maximum operate temperature was up to 120 °C was achieved at first time. The 3-dB bandwidth of 16.8 GHz and 10.1 GHz were achieved at 25 ˚C and 80 °C, and the MPIC was successfully operated at 25 Gbps and 15 Gbps data transmission at 25 °C and 80 °C, respectively. These results show the MPIC has the ability to work at various temperature.

For a cm level long distance on-chip optical interconnection using membrane platform, a low loss InP-rib waveguide integrated membrane optical link was designed and fabricated preliminary. The light transmission through InP-rib waveguide was confirmed, however, the threshold current increased due to the light feedback effect, and the worse coupling efficiency between waveguide to laser and PD was high, which should be improved in the future study.

For achieving a low power consumption MPIC for on-chip optical wiring in the future, the requirement of LD, PD and link loss were discussed. A membrane DR laser would be introduced to further increase the efficiency and output power, a process and design optimized InP waveguide would be introduced to form a connection between laser and PD, and back DBR structure. A GaInAs bulk p-i-n PD with short absorber length would also be introduced to reduce the junction capacitance and increase the load resistance for reducing required output power of laser. The thermal resistance is enough now, and differential resistance is not significant to the energy cost < 10 fJ/bit, because of the low

bias current. The modulation efficiency was indicated to be the critical parameter for low power consumption. Finally, a method of integration on Si-LSI was discussed using SiO_2-SiO_2 surface activated bonding assisted by a-Si nanofilm.

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Chapter 6

Conclusion

The purpose of this research is to realize the high temperature and high efficiency operation of membrane optical integrated circuits (MPICs) on silicon for on-chip optical interconnection. Silicon LSIs have improved the performance by increasing the degree of integration. As a result, interconnection delays in inter-block data communication within the chip (especially between CPU and cache memory) are becoming a major limiting factor in LSI performance, known as the "interconnection bottleneck". The on-chip optical interconnect is attracting attention for overcoming this bottleneck. On-chip optical wiring has less transmission delay and electromagnetic interference. It also supports multiplexing of large-capacity data transmission. Therefore, it is proposed that a membrane structure based optical monolithic integration in which a semiconductor laser, passive waveguide and a photodetector (PD) that can be formed on silicon LSIs by a back-end process only of III-V semiconductors. The membrane structure is to form a III-V semiconductor layer (GaInAsP/InP in this research) of several hundred nm including the active layer region of the laser sandwiched between air and SiO_2. Since the refractive index of air and SiO_2 is much smaller than that of III-V semiconductor, strong optical confinement can be realized, which enables laser operation with extremely low power consumption compared with the normal semiconductor laser. Prior to the start of this research, low threshold and high efficiency lateral current injection (LCI) membrane distributed reflector (DR) laser on silicon by benzocyclobutene (BCB) bonding was realized. However, the short cavity structure for achieving low threshold current operation caused a large thermal resistance. This causes problems such as increase of threshold current and decrease of differential efficiency and output power during high temperature operation. In addition, a MPIC integrated with membrane DFB laser, passive GaInAsP buried waveguide, and p-i-n PD had been fabricated, however, the thermal resistance limited the output power of membrane DFB laser and high-temperature operation was not investigated. Therefore, based on the above problems, the following objectives were

listed and studied in this thesis.

【Objective 1】 Investigation of design of high heat dissipation membrane laser structure

(c) Calculation of structure dependence of thermal resistance

(d) Estimation of effect of heat generated from LSI on the laser active layer.

【Objective 2】 Realization of low thermal resistance membrane laser

(c) Investigation of fabrication process

(d) Characterization of thermal properties

【Objective 3】 Realization of high temperature and high efficiency operation of membrane optical link

(c) Investigation of fabrication process

(d) Characterization of static and dynamic properties under various temperature

The summaries of each chapter are described as follows:

Chapter 1 described the development of related technologies of on-chip optical interconnect. A brief history of optical communication was introduced at first. Optical fibers (low loss transmission medium) and lasers (reliable source) laid the foundation for modern optical communications. The history of Si-LSIs is the history of technological evolution based on the concept of scaling. Transistors have evolved year by year due to miniaturization according to Moore's law. In high-density integration by introducing such fine transistors, the signal speed in the wiring connecting the LSIs limits the entire system. Many novel structures of electrical wiring were proposed, such as conductive coupling and differential transmission line. However, high-speed and low consumption are difficult to achieve in such high-density integration using electrical wiring. As a solution to the problem, on-chip optical interconnection technology that replaces the electrical wiring on

the LSIs with optical wiring is attracting attention. Then, various optical devices used in optical link were introduced, especially semiconductor lasers. The wafer bonding is a key technology to the integration of III-V optical device and Si substrate. Our group proposed a MPIC using membrane DFB laser by BCB adhesive wafer bonding for on-chip optical interconnect. After an introduction of the history of our research and other group's research about membrane laser, the problems mentioned in this chapter and objectives of this research were given.

As the answer of objective 1, chapter 2 described the thermal analysis of membrane laser. A 59 μW output of laser at 85 °C and 43% thermal resistance should be reduced. 3D thermal model of membrane laser bonded on Si substrate on Cu heat sink was used in the calculation of temperature distribution. Several device structure dependences of thermal resistance were calculated numerically, which consisted of cavity length in cavity direction; thickness of electrode, distance between electrode and active region in lateral direction; thickness of SiO_2 cladding layer and BCB bonding layer in vertical direction. Two structures were proposed with high heat dissipate effect. One is the thermal shunt using buried metal through InP/SiO_2/BCB via. Another one is the BCB-free structure. The thermal resistance can be reduced by 45 % using buried metal thermal shunt based on previous 2-μm-thick BCB bonding process, which shows a high heat dissipation effect. The calculation results also revealed that the buried metal is better to connect Si substrate and close to the active region as soon as possible for maximizing heat spread. In BCB-free structure, the thermal resistance can be reduced by 53 %, which showed a higher heat dissipation effect. Meanwhile, the buried metal thermal shunt hardly works in the BCB-free structure. After disscusing the thermal resistance of membrane laser, 2D model of how heat from Si-LSI affects temprature of active region was studied. The temprature rise of mixed effect of LSI and self-heating of laser was equivalent to that of idividual heat source operated respectively, which means the heat from LSI affects the ambient temperature of membrane laser. The laser characteristic includes ouput power, and relaxation oscillation frequency f_R were calculated considering thermal rsistance. The

output power of over 1 mW and optical saturated current of 10 mA were obtained if the thermal resistance was lower than 500 K/W (750 Ω differential resistance), which can be obtained in BCB-free structure. At the same time, the f_R can be increased by 41%.

As the answer of objective 2, chapter 3 discribed invastigation of various bonding technologies in membrane laser. 100 nm ultra-thin BCB bonding was discussed at first. The key point of BCB bonding is to control the pre-cure time after spin coating. 2 min was experimentally proved the best time in 100 nm BCB bonding. However, the BCB bonding needs an annealing temperature up to 250 °C, and the bonding strength is low. Next, direct bonding was studied toward BCB-free structure for minimizing thermal resistance. The hydrophobic O_2 plasma activated bonding (O_2 PAB) between SiO_2-SiO_2 showed a strong bonding strength of 1.45 MPa. However, this occurred at the annealing tempreature up to 300 °C, and the bonding area was small. Finally, to achieve a room temperature bonding of SiO_2, a modified surface activated bonding using a-Si intermediate layer was proposed. It solves the problem that SiO_2 cannot be bonded at room temperature. In fact, this method can even be used to bond most materials. An argon fast atom beam (Ar-FAB) was used to sputter a-Si onto SiO_2 in a high vacuum chamber. After Si substrate was cleaned by Ar-FAB as well, two wafers were bonded at room temperature with 5 min. A strong bonding strenght of > 2.47 MPa was obtained. The large bonding area (~ 90%) and uniform photoluminesence (PL) after bonding indicated its high reliability and bonding quality. The XRD measurement also showed that the structure of multi-quantum-wells was well maintained after bonidng. This methode provids a strong support to a direct bonding type membrane laser using thermal stress free bonding.

As the answer of objective 2, chapter 4 discribes the fabrication processs of BCB-free membrane laser and the thermal propoties estimation. In the laser fabrication, another difficulty that must be overcome is the unflatten surface due to OMVPE regrowth before bonding. Therefore, a chamical mechanical polishing (CMP) process was studied. The

basic process conditions including polishing rate, pressure, and slurry flow rate were invastigated in 2-inch wafer level CMP. The in-plane uniformity and surface roughness were served as evaluation indicators. The in-plane uniformity becomes worse as the polishign amount increases, however, the surface rougness after polishing is only determined by slurry type. The reults showed that 1000 nm polishing amount can flatten the surface of SiO_2 with the initial difference level of ~ 130 nm. After this polishing, there was over 100 nm thickness difference on 2-inch wafer, and the bonding results indicated that it has little effect to bonding process. The surface roughness after bonding using SS25 slurry was around 0.3 nm, which fully meets the criteria for direct bonding. So far, the key technology of CMP-SAB was successfully established. Based on this bonding process, a membrnae FP laser (610 μm cavity length) was fabricated. A larger optical saturated current was obtained compared with that of in the previous BCB boding structure. The thermal resistance reduction of 50 % was confirmed experimentally, which agrees with the simulation result. Next, membrane DFB lasers with different grating pitch were fabricated. Even though a little higher threshold current obtained compaired with that in previous work because of the light feedback effect and fabrication error, an optical saturation current over 8 mA obtained in all devices, which shows a high heat dissipation structure obtained in membrane DFB laser. A thermal resistance of 510 K/W was obtained in the cavity length of 70 μm. The different grating pitch provided a Bragg wavelength detuning effect to membrane DFB laser. The laser operated up to 110 °C when the detuning value was +20 nm.

As the answer of objective 3, chapter 5 discribes the MPIC fabricated by CMP-SAB. A buried-ridge-waveguide structrue was introduced to membrnae laser and p-i-n PD to enhance the lateral optical confinment. The electrical isolation process was conducted to reduce the cross talk between laser and p-i-n PD. First, the MPIC including membrane DFB laser, GaInAsP buried waveguide, and p-i-n PD was fabricated. The low threshold current was obtained at the range of 0.2 ~ 0.4 mA in the cavity length range of 50 ~ 90 μm at room temperature. The measurement was under the on-wafer measurement without

cleaving, and each laser was connected with two p-i-n PD, hence, the light feedback was suppressed. The slope efficiency of 0.203 mA/mA was obtained at 25 ˚C from the I_{LD}-I_{PD} curves. Large photocurrent of > 1.0 mA was detected at 25 ˚C, and even at 100 ˚C, > 0.2 mA photocurrent was obtained. The recorded maximum operation temperature was up to 120 ˚C, which was the highest temperature in our study so far. The stage temperature and wafer surface temperature were well calibrated before measurement. Next, the dynamic characteristics were estimated at various temperature. From the small signal S_{21} response, the 3-dB bandwidth of 16.8 GHz and 10.1 GHz were achieved at 25 ˚C and 80 ˚C, which shows a sufficient bandwidth for 10 Gbps data transmission even at 80 ˚C. In large signal modulation, an NRZ, PRBS of 2^{15}-1 signal was used. A clear eye opening was obtained in 25 and 15 Gbps data transmission at 25 ˚C and 80 ˚C, respectively. These results indicated that the high temperature and high efficiency MPIC fabricated by CMP-SAB was achieved. For a cm level long distance on-chip optical interconnection, a low loss deep-etched InP-rib waveguide integrated MPIC was fabricated and preliminary characterized. The light transmission was confirmed through I_{PD}-I_{LD} curves, however, some problems remained. The high light feedback existed due to the worse coupling efficiency caused by fabrication error, which leaded to a high threshold current and low detected photocurrent, and this can be solved by a high coupling efficiency design and process optimization. Comparison to the NTT's work was shown and toward prospects in future, some calculation, and ideas to final MPIC design for low power consumption were discussed. And to integrate on Si-LSI substrate, a modified SiO_2-SiO_2 surface activated bonding assisted by a-Si nanofilm was introduced at last.

Through the entire thesis, the high heat dissipation structure was proposed. A modified surface activated bonding combining with chemical mechanical polishing was established for membrane laser. Low thermal resistance membrane DFB laser was obtained, and high temperature and high efficiency MPIC was achieved. The obtained results showed the temperature characteristic of optical link using membrane platform was greatly improved

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[1] **W. Fang**, N. Takahashi, T. Horikawa, Y. Ohiso, R. Xue, S. Katsumi, T. Amemiya, and N. Nishiyama, "High-temperature and high-efficiency operation of membrane optical link with buried-ridge-waveguide bonded on Si substrate", *Optics express*, in press, DOI: https://doi.org/10.1364/OE.468192.

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