論文 / 著書情報
Article / Book Information

題目(和文)	
Title(English)	Study of Power Loss Reduction of an Active Front-end Rectifier Using an Instantaneous Reactive Power Compensator
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出典(和文)	学位:博士(学術), 学位授与機関:東京工業大学, 報告番号:甲第12296号, 授与年月日:2022年12月31日, 学位の種別:課程博士, 審査員:藤田 英明,千葉 明,萩原 誠,竹内 希,清田 恭平,和田 圭二
Citation(English)	Degree:Doctor (Academic), Conferring organization: Tokyo Institute of Technology, Report number:甲第12296号, Conferred date:2022/12/31, Degree Type:Course doctor, Examiner:,,,,,
学位種別(和文)	博士論文
Type(English)	Doctoral Thesis

Study of Power Loss Reduction of an Active Front-end Rectifier Using an Instantaneous Reactive Power Compensator

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A thesis submitted for the degree of

Doctor of Philosophy

December 2022

Acknowledgements

First of all, I would like to express my deepest gratitude to my supervisor, Prof. Hideaki Fujita, for giving me an opportunity to conduct research in the Power Electronics Laboratory at Tokyo Institute of Technology, for his skilful advice, meaningful suggestions, and invaluable encouragement during my study in the laboratory. He is always available and interested in the discussions on my research topic.

I would like to thank Assoc. Prof. Makoto Hagiwara and Asst. Prof. Kenichiro Sano for his invaluable suggestions and comments that encourage me in the improvement of my research.

I am also very grateful to the other fellow members, Mr. Hirose, Mr. Takayama, Mr. Watanabe, Mr. Cristian, Mr. Fiqih, Mr. Umano, Dr. Yamaguchi, Dr. Tesaki, Dr. Haneda, Dr. Nicola and Dr. Hadi for their warm friendship, their support in many issues including Japanese language, and making good atmosphere in the laboratory.

My study and stay in Japan could not be accomplished without the support of the Office of the Civil Service Commission (OCSC) of Thailand by means of their Scholarship. I also would like to thank the National Science and Technology Development Agency (NSTDA) and the National Electronics and Computer Technology Center (NECTEC) of Thailand that gave me this opportunity to study. I am deeply indebted to OCSC, NSTDA, NECTEC, and Thailand

I would like to thank Dr. Natchpong Hatti for introducing me to Prof. Fujita and for his suggestions during my study in Japan. I also would like to thank Dr. Kanokvate Tangpimolrat and other

laboratory members in NECTEC for encouraging me to apply for the scholarship and go study abroad.

Last but not least, I would like to express my gratitude to my mother, my father, my sister, my wife and my relatives for their warm support and encouragement.

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Chapter 1

Introduction

1.1 Research Background

Nowadays, climate change has been a problem affecting many lives around the world. Climate change causes the fluctuation of temperature, weather, and sea-level [1]. Therefore, humans need to adjust their behavior to live in this situation, especially agriculturists. Many activities of people are the main cause of the climate change problem. For example, some factories release wastes into rivers and the atmosphere from production. The report in [2] shows causes of the air pollution in U.S. in 2018 which came from the agriculture sector 10 %, commercial and residential sector 12%, electricity sector 27%, industrial sector 22% and transportation sector 28% of total emissions in 2018 equal to 6,677 million metric tons of carbon dioxide (CO_2) equivalent [2].

Coal and petroleum are the primary energy resources that can be transferred to other energies for utilization. However, the waste of these energy conversions is CO_2 which directly affects air pollution. Especially transportation, there are many engine cars on the roads worldwide, and it is not easy to control the released CO_2 from the vehicles. Recently, the critical government of many countries has been pushing for moving away from petroleum as the primary energy source for powering the engine vehicle. Therefore, a battery-electric vehicle (BEV) is an exciting choice to reduce the release of CO_2 into the atmosphere, and it is easier to manage the released CO_2 at power plants.

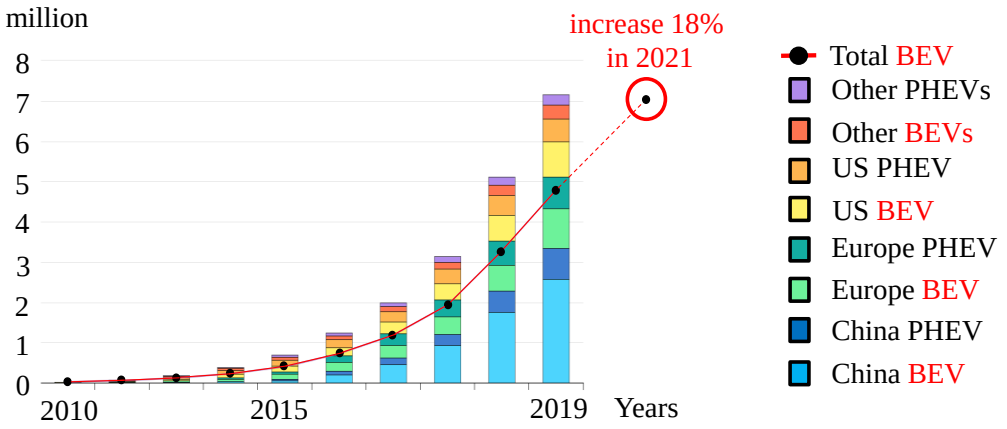

Figure 1.1: Global Electrical Vehicles Stock between 2010 and 2019 of US, Europe, and China.

Figure 1.1 shows the global electric vehicles stock of BEVs and plug-in hybrid electric vehicles (PHEVs) in China, Europe, and America from 2010 to 2019, as presented in [3]. Before 2016, the rate of BEVs was around the same as PHEVs. However, since the development of Li-ion batteries can reduce the price and increase power density, BEVs have been a popular vehicle than PHEV and have grown, as shown in the red line. As a result, the expectation of BEV production will be reached to around 7 million in 2021 or 18% of 2019.

The charging system plays the main role in filling energy in the battery of BEV. Figure 1.2 shows an example application of an EV DC fast charger, as presented by DELTA Electronics [4] consisting of the three-phase grid voltage, 50-kW DC fast charger, and lithium-ion battery module. The 50-kW DC quick charger consists of 2 main parts. Firstly, AC/DC rectifier is connected between the three-phase voltage input and the dc-link capacitor. The ac/dc converter has abilities to control the power factor, the dc voltage regulation, and sinusoidal waveshape for the ac currents. Secondly, the DC/DC converter is used for controlling the current and voltage of the lithium-ion battery. The efficiency of this system, as shown in [4], is 94% at 50-kW. The popular AC/DC rectifier topology is a pulse-width modulation (PWM) rectifier because of its simple structure and

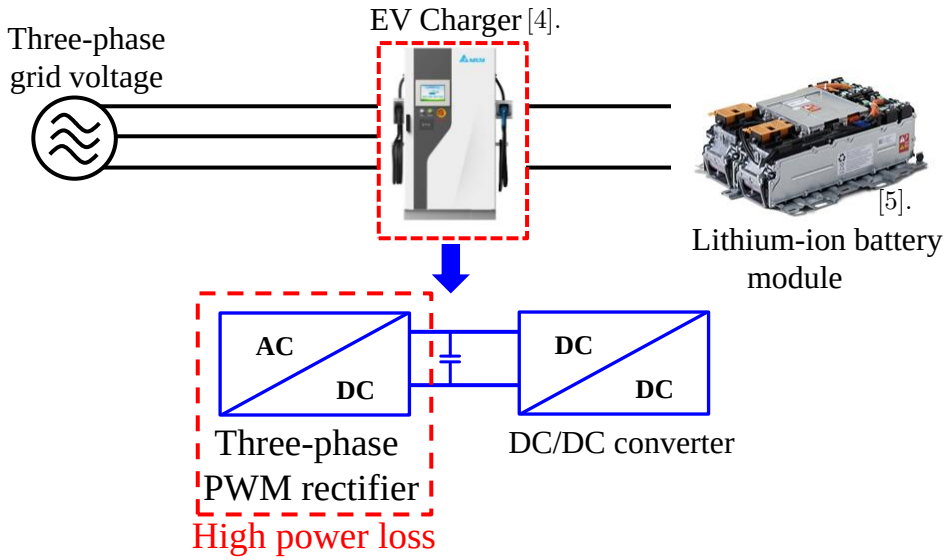

Figure 1.2: An example application of EV DC fast charger presented by DELTA Electronics.

simple control system. However, the PWM rectifier has relatively large power losses from switching devices, a high electromagnetic interference (EMI) [6][7] and bulky passive components such as ac inductors and a dc-link capacitor.

The wide bandgap (WBG) devices, such as silicon carbide (SiC) and gallium nitride (GaN) switching devices, are developed to improve the performance of switching power supplies [8] [9]. The advantages of these devices are a lower gate charge, a lower output capacitor (C_{oss}), and a faster time and a lower reverse recovery charge for the diode than the switching device based on silicon (Si). In addition, these give an opportunity for increasing the switching frequency, which can go up to several megahertz with a low switching loss. Therefore, the size of the passive components can be significantly decreased. However, the cost of these switching devices is still expensive.

In the past years, zero voltage switching (ZVS) techniques have been presented to reduce the switching losses of the conventional PWM rectifier. Articles in [10] to [12] presents a ZVS method that utilizes the increased current ripple technique to discharge the voltage across the switch to zero in the dead-time duration

before turning on the switch. However, this technique requires additional passive components for the resonant circuit, which reduces the reliability and increases the cost of the system.

A. Amirahmadi [13] and S. M. Tayebi [14] propose the ZVS technique without using auxiliary circuitry. The ZVS can be achieved by using a turn-off current to discharge a voltage across an output capacitor of switching device in during the dead-time. The benefits of this technique are able to reduce the switching losses and the inductor's volume because of the use of small inductance. The rms ac currents are increased around two times of its fundamental that causes relatively large conduction losses for switching devices. Thus, this technique is not suitable for high-power applications.

The interesting technique for improving the efficiency and power density of the ac/dc conversion system is the use of active power filters (APFs), which is connected in parallel with the ac side of the diode rectifier. The APF is used to inject a current to suppress the harmonic current of the rectifier. Especially, the APF can effectively compensate for the harmonic current produced by a rectifier equipped with a smoothing inductor because the rectifier can be considered as a harmonic current source. Furthermore, the required rms current rating of the APF is about 1/3 of the rectifier rating, and thus, it is expected to reduce the switching power loss in the APF and the volume of the whole system, compared with a conventional PWM rectifier.

On the other hand, it is difficult for an APF to compensate for the harmonic current caused by a diode rectifier with a smoothing capacitor. The diode rectifier behaves as a harmonic voltage source with a low impedance due to its large smoothing capacitor [15]. When the APF is enabled, the rectifier draws an increased harmonic current into its smoothing capacitor. The APF requires a large current rating and causes additional switching and on-state power losses. For this reason, a relatively large ac inductor is often connected to the ac terminals of the rectifier for reducing the harmonic current drawn from the APF [15].

The papers in [17] have proposed a grid-connected PV inverter system using a 120-degree inverter, a boost converter, and an instantaneous reactive power compensator (IRPC). The boot converter regulates its dc power under a maximum power point tracking condition. And then, the 120-degree inverter provides the

three-phase ac voltage to the grid at a fixed active power because a small film capacitor is only connected to the dc-link instead of a bulky electrolytic capacitor. As a result, the ac current of the inverter forms a square wave shape which consists of ac components in the instantaneous reactive power and a constant value for the instantaneous active power [16]. As a result, the IRPC needs to compensate only the ac components in the instantaneous reactive power, and no energy storage element is required in the dc capacitor on the dc side of the IRPC. Moreover, it is possible to reduce the volume of the ac inductor for the IRPC because the required rms current is around 32% of the rectifier rating making the power loss reduction in the switching devices of the IRPC circuit.

This thesis discusses the application of the IRPC to three-phase diode rectifiers. The system consists of a diode rectifier, a buck converter, and an IRPC. The IRPC essentially compensates for the ac components in the instantaneous reactive power produced by the diode rectifier. Thus, it is possible to reduce the power losses and system's volume compared with a conventional PWM rectifier. However, in this case, the diode rectifier causes an uncontrollable commutation overlap, unlike the 120-degree inverter in [17]. This thesis analyzes the overlap and instantaneous active and reactive power drawn into the diode rectifier and develops a new control method for the IRPC to improve the grid current THD. In addition, the modified control method is also proposed to reduce the output voltage/current ripples by providing a small instantaneous active power from the IRPC. Moreover, the power loss reduction by combining discontinuous pulse-width modulation and zero-voltage switching technique is proposed to extend the soft-switching areas of the proposed circuit operation. In this dissertation, a 4.5-kW laboratory setup was assembled and examined to verify the theory developed in this paper and compare the operating performance and power conversion efficiency with a conventional three-phase PWM rectifier. As a result, the proposed ac/dc rectifier exhibited an improved power conversion efficiency higher than 99%.

1.2 Research Objectives

The main objective of this dissertation is to study and improve the efficiency and power density of an ac/dc power conversion system that consists of the three-phase diode rectifier, the IRPC, and the dc/dc converter. The objectives of this dissertation are:

- Development of a new control method to control the three-phase diode rectifier with the IRPC. The proposed control method uses the estimation technique for calculating the instantaneous active and reactive power without using current sensors at the ac side of the diode rectifier. The estimated powers are used as the power commands for the IRPC to suppress the harmonic current of the diode rectifier. This technique can control the grid current sinusoidal.

- Development of the damping control methods to maintain stability of the system. Furthermore, this dissertation also proposes a method for reducing the ripple voltage/current output, which is suitable for battery charger applications.

- Development of a new method by using discontinuous PWM (DPWM) and zero-voltage switching technique to extend the soft-switching mode of the IRPC. This technique can effectively improve the efficiency of the proposed circuit in this dissertation.

1.3 Dissertation Outline

- **Chapter 1** This chapter describes an overview of the growing number of BEV. In the case of the DC fast charger, a conventional three-phase PWM rectifier is used as an active front-end of the charging system. This circuit has main drawbacks: high switching loss, bulky passive components, and high EMI. The outline of this dissertation is shown in this chapter.

- **Chapter 2** This chapter contains a literature review infrastructure of BEV, battery chargers, and DC fast-charging system. Moreover, this chapter also

reviews the active front-end, which is connected between grid voltages and a dc/dc converter.

- **Chapter 3** This chapter describes in detail the three-phase diode rectifier with an IRPC. The diode rectifier, which has two operating modes such as non-overlap and overlap commutation, is analyzed to calculate the instantaneous active power, instantaneous reactive power, and dc-link voltage and power. These estimated signals are the power command for the IRPC to inject the compensating current to eliminate the harmonic current of the rectifier.

- **Chapter 4** This chapter describes the stability problem of the proposed circuit, and the damping controller is presented to maintain the system's stability. The damping controller can be applied in either the IRPC or the dc/dc converter or both circuits to suppress the resonant current. Finally, the 4.5-kW laboratory setup is used to verify the control methods.

- **Chapter 5** This chapter expresses the combination between zero-voltage switching (ZVS) and discontinuous pulse-width modulation (DPWM) techniques for extending the soft-switching mode of the IRPC. The relationship of SV-PWM, CB-PWM, DPWM, the designed ac inductor to achieve ZVS area, and dead-time compensation are presented in this chapter. This method was verified using the experimental setup to compare the power loss breakdowns, efficiency, and EMI between the convention PWM for the IRPC circuit, and the combination between DPWM and ZVS technique of the IRPC circuit.

- **Chapter 6** This chapter analyzes and compares the switching losses in the IRPC circuit when is modulated by CPWM and DPWM with ZVS. Due to the current ripples resulting in the switching loss in the IRPC circuit, the analysis based on the actual measurement is used to estimate the switching loss by using the simulation compared with the experimental results. As a result, this method is possible to estimate the switching losses in the IRPC.

- **Chapter 7** This chapter concludes this dissertation and presents some future research topics.

Chapter 2

Literature Review of BEV Charging Systems and Active Front-End Rectifier

Battery Electric Vehicles (BEVs) have had the potential to decrease CO_2 emissions significantly. According to the report in [18], the number of BEVs had been grown around 98% from 2020 to 2021, and BEVs are expected to be the main role for zero-emission targets set in 2050. However, the barriers of BEVs are the high cost, the range concern, and the charging infrastructure. Even though the increase of battery cells can improve the range of the BEVs, the battery causes a significant rise in the price, making the high cost of BEVs. To improve this problem, a charging station plays the main role to fill the battery's energy. It can be assumed that if many charging stations cover every area, the increase of battery cells do not need to the BEV for improving the range. Thus, the charging station is a solution to optimize the total price of BEVs if the charging system can provide more power to reduce the charging duration which felling like a gas station.

This chapter reviews the charging system and infrastructure of an electric vehicle, DC fast charger system, and the part of active front-end, which plays the main role to control the quality of the input currents and provide the power to the dc charger.

2.1 Charging system and infrastructure of EV

A BEV charger is an important system for filling energy to the battery. The input of the charger system receives the energy from a grid voltage source or renewable energy resources such as wind turbines and PVs, which allow using clean energy instead of fossil fuel or petroleum.

Figure 2.1 shows an example of the battery charging station system for BEVs as presented in [19] [20]. The electricity is transferred from grid voltage through a low-frequency transformer converting the high-voltage to the operating voltage (250 V to 480 V) for the ac-link. The converters, such as ac/dc rectifier and dc/dc converter, convert power from the ac-link to charge a battery module in BEVs. In the diagram, renewable energy resources such as PV and wind turbine systems connect to the ac-link voltage by using the dc/ac inverter. Renewable energy resources can reduce power consumption at the grid voltages. However, renewable energy resources have a lot of fluctuated power. Thus, an energy storage system should be used in the system to decrease the fluctuation of the input power [21].

The BEV charger system can be classified as an on-board and off-board charger. These chargers would be operated in a unidirectional or bidirectional power flow. In the case, the on-board charger is installed inside of the vehicle, which has the limitations of installed area, weight, and total cost of BEVs. As a result, the rating power of the on-board charger is low. The single-phase or three-phase voltage system can be used to be a power supply for the on-board charger. This charger type spends a long time for charging the battery [23] [24]. These charger can be seen at user's home and office.

In the case of the off-board charger, it does not need to be concerned about the area, size, weight, and price of a vehicle because the off-board charger is installed outside from BEVs. For this reason, the off-board charger can provide a high rating power for charging a battery module that can provide BEV users with satisfactory charging speed. This charger type is like a filling gas station [25][26].

Figure 2.2 depicts the charging systems and infrastructure of BEV, which composes of three main parts of the power conversion system[22]. The first part is

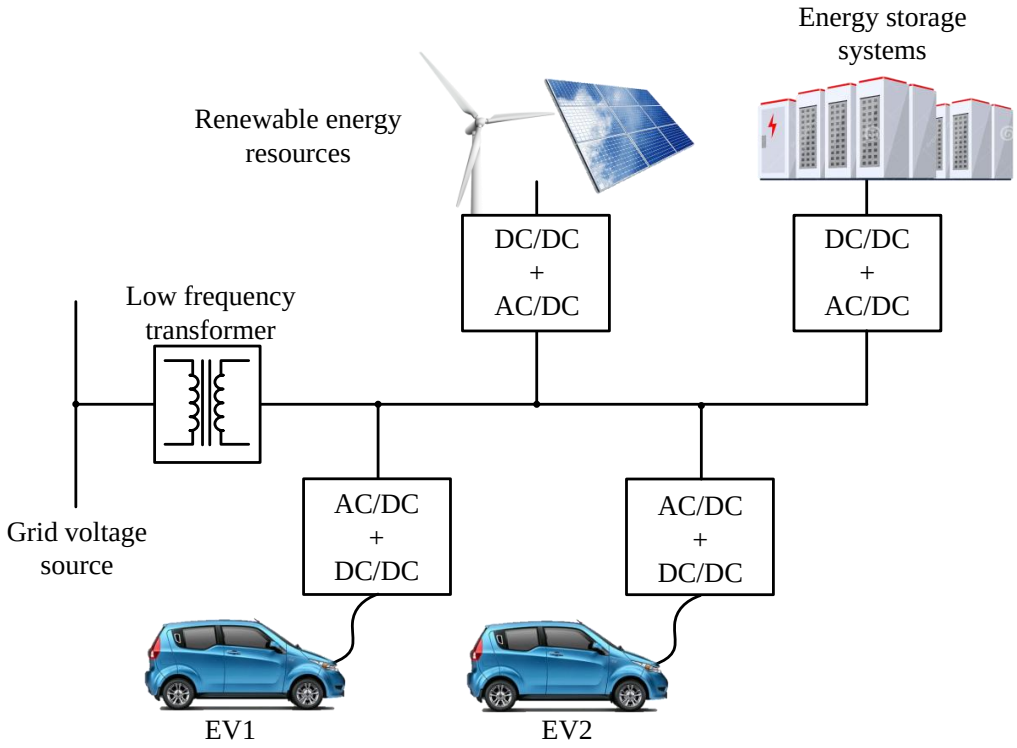

Figure 2.1: Battery electrical vehicle (BEV) charging system diagram.

the dc/ac inverter connected between the battery cells and the traction ac motor. This inverter converts the dc voltage of a battery module to a three-phase ac voltage supplying to a traction motor. The inverter adjusts the amplitude and frequency of the ac voltages to control the torque and speed of the traction motor. The second part is a dc/dc converter for converting a dc voltage of the battery to DC loads in BEV such as lights, air condition, monitors, etc. And the third part is an on-board charger used to fill energy in a battery module of BEV. This part has a thermal management and a battery management system (BMS) to balance the battery voltage of each cell. The left-hand side of this figure shows the AC charger level 1 and 2 and DC fast charger in Level 3 for transferring energy from the grid voltage to the battery charger. The Society of Automotive Engineers (SAE) has already defined the power level of the BEV charging system in North America in the SAE J1772 Standard [27] as follows:

The power level 1 or a slow charger has a rating power lower than 1.9 kW.

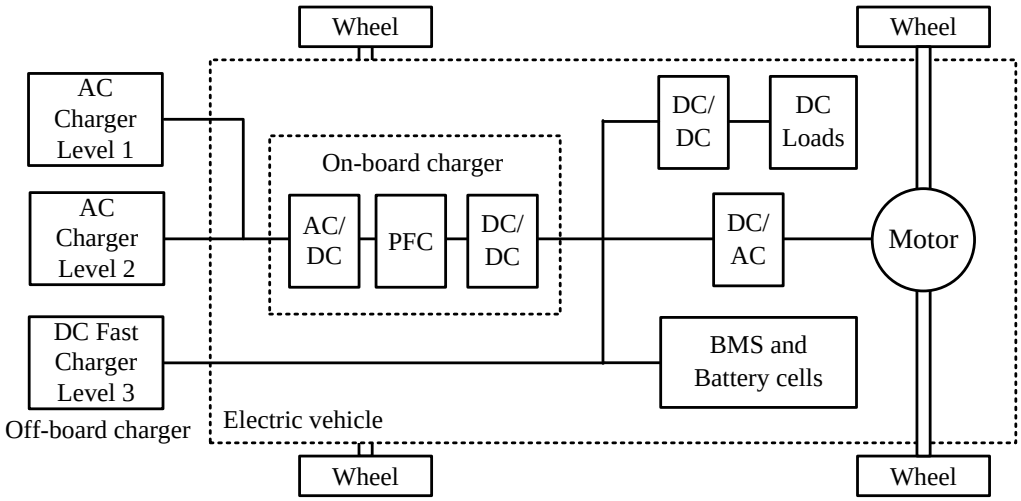

Figure 2.2: Charging systems and infrastructure of BEVs.

This charger connects to a single-phase grid voltage for charging EVs at home or office.

The power level 2 or a semi-fast charger has a rating power between 1.9 kW to 19.2 kW. This charger receives power from either a single-phase or a three-phase grid voltage source. This charger is located at private or public outlets.

In power levels 1 and 2 of the chargers, the power from ac grid voltage flows into the on-board charger before charging the battery.

The power level 3 or a dc fast charging, which is connected directly with the

Table 2.1: Comparison of the charger system in the power level 1, 2 and 3 in range and charging duration.

	Level 1 (1.4kW)	Level 2 (7.2kW)	DC Fast Charger (50kW)	TESLA Supercharge (140kW)	Extreme Fast Charger (400kW)
Range/Minute of charge(km)	0.132	0.676	4.7	13.148	37.498
Time to charge for 100km (minutes)	666	130	19	7	3

battery module, provides the high power from grid voltage of more than 50 kW to charge the battery. This dc fast charger is like a filling gas station. Thus, most of the dc fast charger is placed at filling stations.

Table 2.1 shows the comparison between the range against the charging duration of the BEV charger in the power level 1, 2, 3 when the BEV energy consumption is 177 Wh/km [28]. It can be seen that the charger in the power level 1 and 2, which have the power of 1.4 kW and 7.2 kW, can make the BEV move to 0.132 km and 0.676 km with the charging duration in 1 minute. So, in 100 km, the charger level 1 and 2 have to provide the power to the battery around 666 minutes and 130 minutes, which take a very long time for the BEV user.

The power level 3 of chargers can provide power of more than 50 kW. Table 2.1 depicts the examples of the charger level 3 such as DC fast charger (50 kW), Tesla Supercharge (140 kW), and Extreme Fast Charger (400 kW). It can be seen that the Extreme Fast Charger can provide the highest power to charge the battery, which can make the car move 37.498 km with a 1-minute charging duration. So, it can take 3 minutes to make the vehicle move 100 km, which can satisfy the BEV users.

2.2 DC fast charging system

A DC fast charger is a device for transferring energy from ac gid voltages to charge the battery. This charger is grouped in the power level 3 providing the power more

Table 2.2: Commercial dc fast chargers available on the market

Manufacturer Model	ABB Terra 53	Tritium Veefil-RT	PHIHONG DJ60	TESLA Supercharger
Power	50 kW	50 kW	60 kW	135 kW
Input AC 3 phase: DC:	480 V	380 V - 480 V 600 V - 900 V	380 V - 480 V	380 V - 415 V
Output voltage	50 V - 500 V	50 V - 500 V	50 V - 500 V	50 V - 750 V
Output current	120 A	120 A	125 A	330 A
Efficiency	94 %	92%	94.8%	91 %
Weight	400 kg	165 kg	350 kg	600 kg

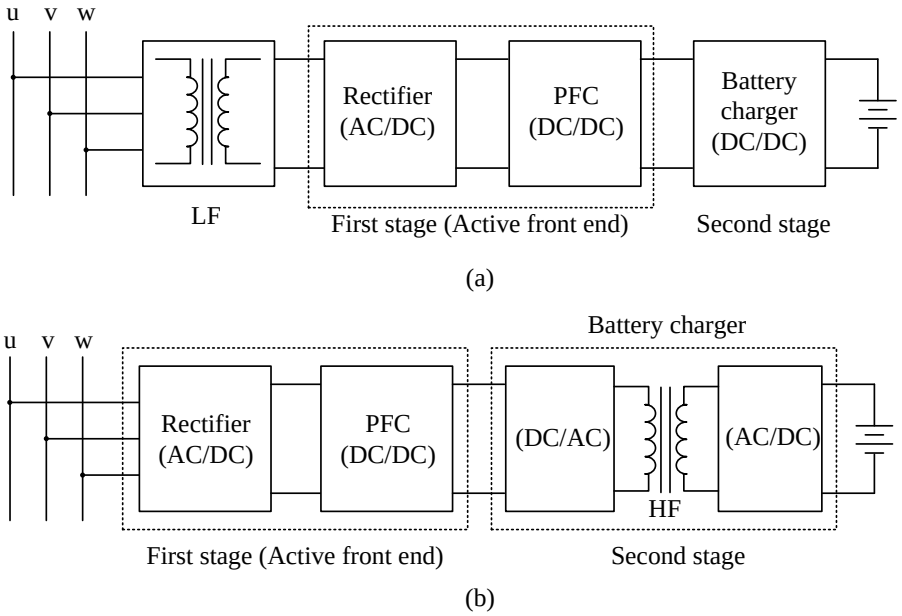

Figure 2.3: Block diagrams of dc fast charger (a) a low frequency transformer installed at ac grid voltage (b) a high-frequency transformer installed in a dc/dc converter.

than 50 kW. Normally, the charger system should have capable of controlling a dc voltage and a dc current of the battery with unity power factor. Table 2.2 depicts examples of the commercial dc fast charger available on the market. It consists of ABB, Tritium, PHIHONG and TESLA [29] [30] [31] [32]. The rating power has several levels between 50 kW to 135 kW, which can provide the dc voltage from 50 V to 750 V and the dc current from 120 A to 350 A, depending on the requirement from the thermal management system, and battery management system of the BEV. The thermal management system, and battery management system help to maintain the lift-time of the battery. For example, if the thermal of the battery is high during the charging process, the thermal management system and battery management system send the command to the charger to limit the charging current, and send the command to the cooling system in BEV to reduce the temperature of the batter [33].

The energy conversion system consists of two stages inside the DC fast charger. The first stage has several names: ac/dc converter, ac/dc rectifier, power factor

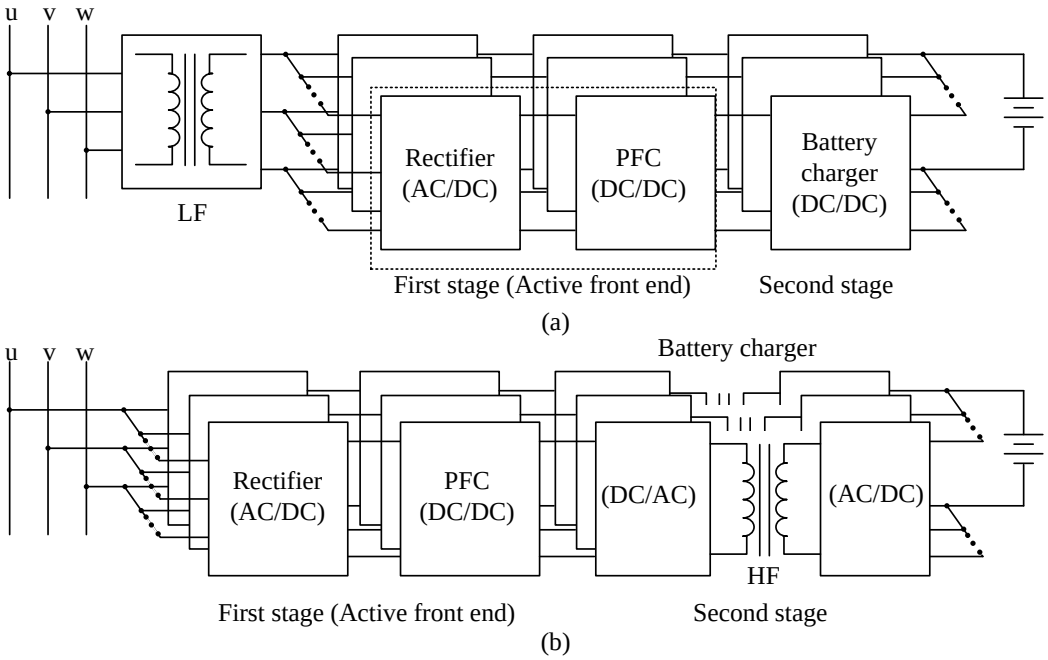

Figure 2.4: Block diagrams of parallel structure of dc fast charger (a) a low frequency transformer installed at ac grid voltage (b) a high-frequency transformer installed in a dc/dc converter.

collection (PFC), and active front-end (AFE) rectifier. This equipment is used to transfer a three-phase voltage to a dc voltage before providing energy to the second stage. The second stage is a dc/dc converter connected in series with the dc-link voltage to transfer all power to a BEV battery module.

Figure 2.3 expresses the simplified block diagram of the DC fast charger. Due to safety reasons, the battery cells have to always isolate from the power source outside of BEV [34]. Thus, the dc fast charger type is classified by the isolated transformer installed at the ac-side or inside the dc/dc converter. Figure 2.3 (a) shows the isolated low-frequency transformer is installed at the ac-link of the system. The weight of the low-frequency transformer is high. This system's dc/dc converter can be used in a simple circuit such as a conventional buck or buck-boost converter to provide the power from the dc-link to the battery. This system has a lot of advantages, such as using a simple controller and a basic structure, low cost. In addition, it has an excellent dynamic response for controlling the current, voltage, and power of a battery module [35].

A high-frequency transformer is in a dc/dc converter can be used instead of a low-frequency transformer. However, this system needs to have more power conversion systems, such as a dc/ac converter to create a high-frequency ac voltage for a primary coil before a secondary coil transfers an ac voltage to be an input of an ac/dc converter to charge a battery. In addition, the structure and controller of this system are complex and expensive [36].

Figure 2.4 shows a parallel structure of a dc fast-charging system to increase power which can be designed in both the isolated low-frequency transformer system and the isolated high-frequency transformer system as shown in Figure 2.4 (a) and Figure 2.4 (b), respectively. The main benefit of this method is when the charging system has a failure circuit, engineers can design the system to have the capability to transfer power without stopping the operation. Moreover, the parallel structure is easier and more convenient for maintaining the system [37].

This thesis focuses on developing the active front-end rectifier, which is shown in the first stage of the dc fast charger. Moreover, the active front-end rectifier is an essential circuit for many applications such as dc power supply for motor-driving inverters, induction heating applications, etc.

2.3 Active Front-End Rectifier

An active front-end rectifier is an ac/dc power conversion circuit connected between grid voltage and a dc-link. The active front-end rectifier consists of power electronic devices such as MOSFETs or IGBTs to provide the dc output voltage to dc loads, dc/ac inverters, or dc/dc converters, depending on applications. The main roles of the active front-end can be shown as follows:

- to control the power factor of the system due to some applications requiring to adjust the power factor.
- to control grid current sinusoidal,
- to provide a dc voltage to dc loads or other power conversion systems.

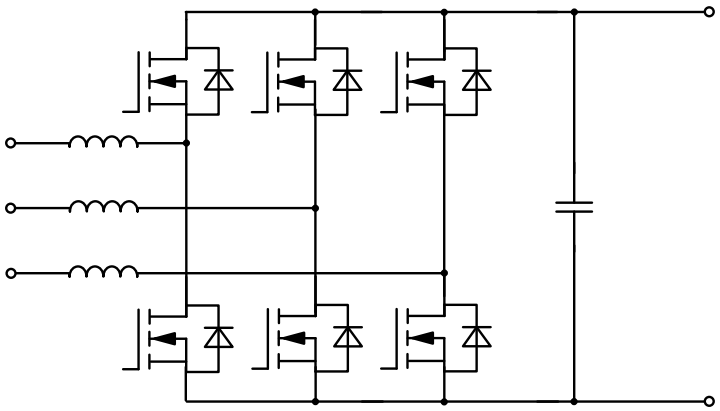

Figure 2.5: Structure of a three-phase PWM rectifier.

The three-phase active front-end rectifier topologies have been used in many applications. For example, the active front-end is used to be the power supply for battery chargers, extruders, compressors, pumps, grinding mills, fans, conveyors, rolling mills, blast furnace blowers, crushers, mixers, mine hoists, gas turbine starters, marine propulsion, reactive power compensation, hydro pumped storage, wind energy conversion, railway traction, and high-voltage direct-current (HVDC) transmission [38]-[41]. The most popular active front-end circuit is a three-phase PWM rectifier which is the boost-type converter. Figure 2.5 shows the structure circuit of the three-phase PWM rectifier consisting of a three-phase ac inductor, a three-phase switching device, and a dc-link capacitor. Due to the boost-type converter, the dc-link voltage is higher than the peak line-to-line grid voltage. This topology has the capability to control a bidirectional power flow, adjustable power factor, and a dc-link voltage regulation. The papers in [42] [43] [44] [45] show the application by using this topology to be an active front-end rectifier for dc fast charger systems. However, this circuit requires bulky passive components such as ac inductors and electrolytic capacitors. The cost of these components is high, and the use of electrolytic capacitors causes low reliability for the circuit because of its lifetime problems from the temperature and humidity of each installation area [46]. Furthermore, the major power losses are the switching and conduction losses of the switching devices occurring a high electromagnetic

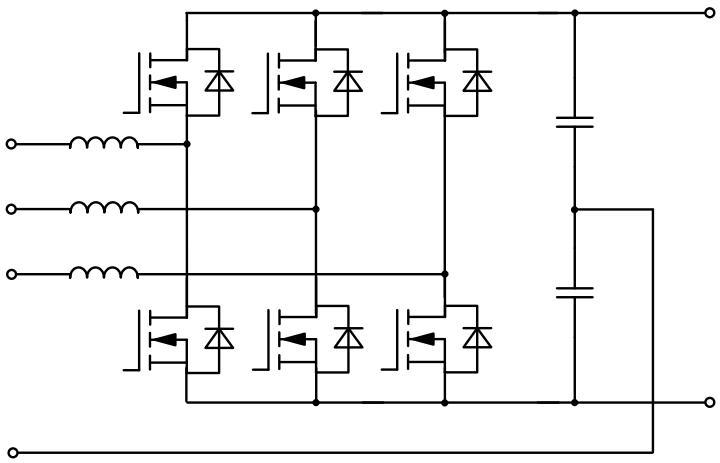

Figure 2.6: Structure of a three-phase PWM rectifier by using half-bridge control method.

interference (EMI). Thus, the cooling system and EMI filter are required in the circuit, causing an increase in circuit size. For this reason, the efficiency and the power density are pretty low.

The soft-switching technique is interesting technique to eliminate the switching losses and EMI issues for the three-phase PWM converter. Papers [47] to [49] proposed the increase of the current ripple to discharge the voltage across the switch to zero before turning on the switch. However, this technique required additional passive component for the resonant circuit which reduced the reliability, and increased the cost of the system.

A zero-voltage switch (ZVS) technique without additional passive component is introduced in the papers [50][51][52]. This technique needed to increase its current ripple by using a small ac inductance to reach the ZVS region. However, This circuit required the neutral cable connecting to the center tap or center voltage at the dc-link capacitor of a three-phase voltage as shown in Figure 2.6. Thus, the operating circuit is like a half-bridge rectifier. The ZVS operation was operated in the circuit during the dead-time. For example, when the current flowed in the negative polarity and the upper switching device of a phase leg was turned off, the current flowed to discharge the voltage across the lower switching

device in the same phase lag to zero during the dead-time. After that, the body diode of the lower switching device contained the current, and the lower switching device was able to be turned on under ZVS operation. Therefore, this circuit does not require any auxiliary circuits. The benefits of this technique can reduce the switching losses and the ac inductance of each phase. Unfortunately, as the rms value of the ac current increased around two times of the fundamental current, the conduction loss of each switching device was significantly increased, and the conduction loss caused the reduction of the efficiency of the whole system. Therefore, this technique was not suitable for high-power applications.

Another boost-type converter is a multilevel converter. The multilevel converter has been developed to offer in high-voltage and high-power applications. There are many topologies as reviewed in the paper [53] such as the neutral-point-clamped (NPC) converters, cascaded converters, flying capacitor converters, multilevel matrix converters, and hybrid converters. The benefits of these topologies over the PWM rectifier are shown as follows:

- Using the available switching devices in the market for high-power and high-voltage applications,
- Reducing the size of passive components, especially ac inductors,
- Decreasing the power losses of the switching devices,
- Maintaining or repairing the system without stopping the operation.

However, more multilevel voltage converters are not suitable in low-voltage and low-power applications because of high-conduction losses, complex structure circuits, complicated control systems, and high costs. Therefore, the three-level NPC converter, as shown in Figure 2.7, is enough to apply in the dc fast charger application for BEVs [54][55][56][57]. The three-level NPC converter has the capability to control a bidirectional power flow for the system and generate the three-level voltages on the ac side, which can decrease the voltage ripple across the ac inductors. As a result, this circuit is possible to reduce the ac inductance, and thus, it has an opportunity to decrease the size of ac inductors. Moreover, the switching losses of each switching device can be significantly decreased because

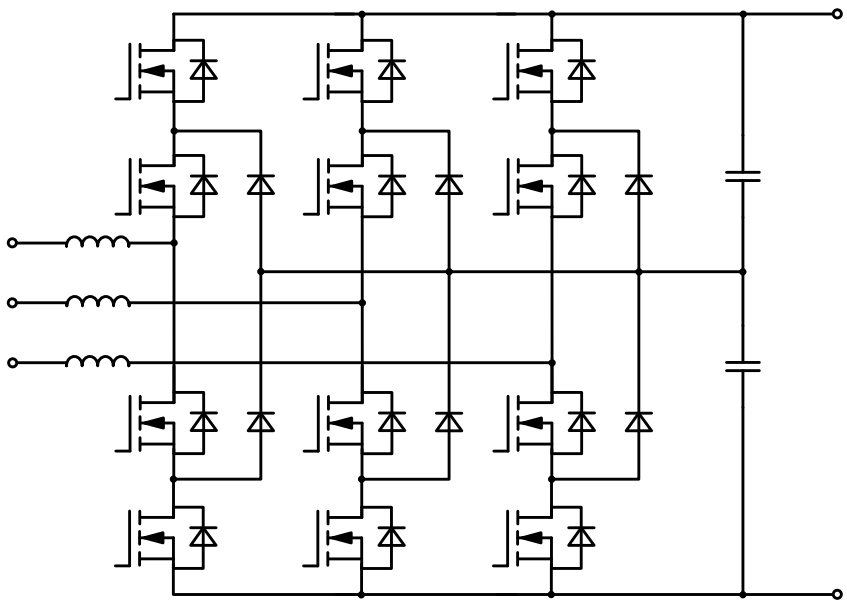

Figure 2.7: Structure of a three-phase neutral-point clamp rectifier.

of the reduction of voltage across each switching device. Therefore, the efficiency of the whole system would be improved. However, bulky electrolytic capacitors are needed for the dc-link voltage. Moreover, the control system has to control the voltage balancing across the dc-link capacitors of the circuit, which directly affects to performance of the system. This controller makes it more complex in the control system, circuit structure, and high cost.

The topologies mentioned above are the bidirectional power flow circuit suitable for developing the vehicle-to-grid (V2G) system. The V2G system can enable the users to sell the energy in their BEV to the grid system, which helps electricity authorities maintain the grid system's stability from the peak or fluctuation of the grid power. However, the cost of this system is higher than the unidirectional power flow topologies.

A diode rectifier that transfers power in only one direction from grid voltage to a dc-link voltage can reduce the cost of the whole system. However, a diode rectifier causes high distortion in the grid currents. Therefore, the active power filter is required to inject the harmonic currents of the rectifier. This technique will be discussed in the next Chapter.

Figure 2.8 shows the T-type Vienna rectifier as presented in [58][59][60][61]. This circuit is similar to the three-phase diode rectifier, but it has additional switching devices, which have the capability to enable a bidirectional power flow between the ac terminal and the middle point of the dc-link capacitor used for injecting the harmonic current at the ac side of the rectifier. Moreover, it can create a three-level voltage at the ac terminal. The advantages and disadvantages of this circuit are the same as a three-level NPC converter, but the limitations of this circuit are a unidirectional power flow and cannot adjust power factor [34].

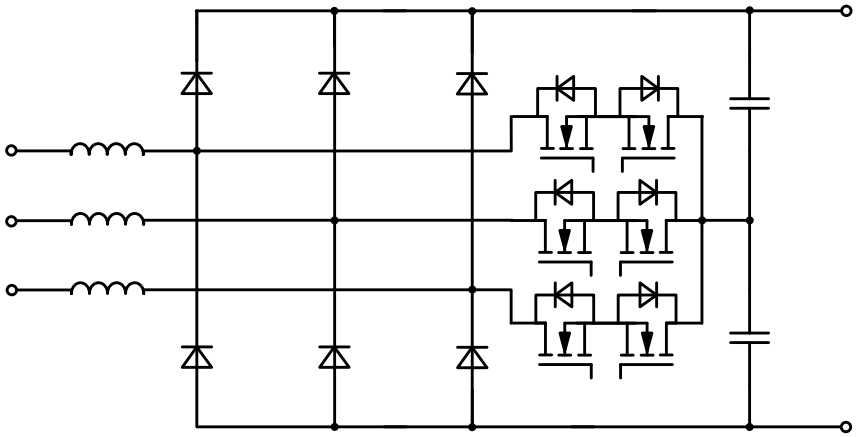

Figure 2.8: Structure of a T-type Vienna rectifier .

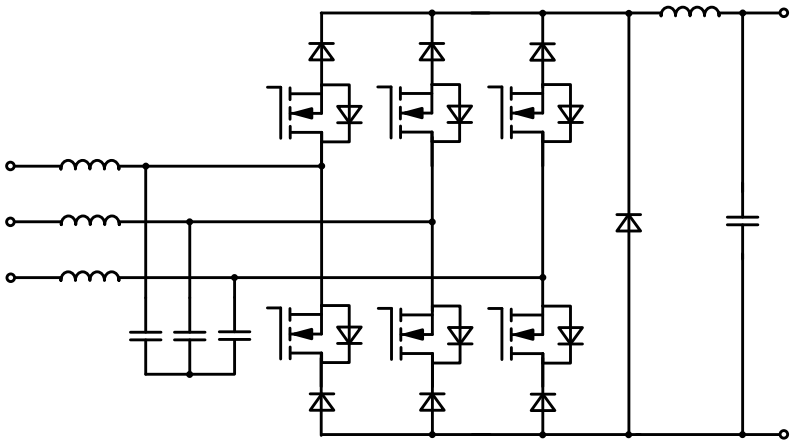

Figure 2.9: Structure of a buck type rectifier .

Figure 2.9 illustrates the buck-type rectifier, which can control the dc-link voltage lower than the peak value of line-to-link grid voltage as shown in the dc-fast charger applications in papers [62] and [63]. The switching devices of this circuit are connected in series with the diode. The switching devices are placed inversely with the diode of each phase as shown in Figure 2.9. From this circuit structure, if switches are turned off, the current from the ac grid voltage cannot flow into the dc-link voltage. On the other hand, the current from the ac grid voltage will flow into the dc-link voltage when switches are turned on. Thus, this circuit behaves like a buck converter in which the input ac current of each phase is chopped. For this reason, the three-phase LC-filter at the ac side is necessary to filter the switching harmonic current before flowing into the grid system. At the dc-side of the circuit, there is a diode placed between positive and negative of the dc-link voltage before connecting to the dc inductor and the dc-link capacitor to smooth the dc-link voltage to loads. The advantage of this circuit is that the short circuit protection does not need to be concerned because the diode of each phase clamps the circuit. Moreover, the active switching devices can be used in an inrush current control to prepare the dc-link voltage before starting a dc/dc converter. However, a low voltage causes a high current flowing into the circuit, and thus, the conduction losses are relatively larger than other circuits with the same power rating. Furthermore, this circuit still requests bulky passive components such as inductor and electrolytic capacitor for the dc-link voltage.

From the above-mentioned active front-end circuits, the ac inductor is a bulky component which can increase the cost and degrade the power density of the system, especially in the high power application. The size of the inductor is proportional to its energy storage (E) which can be calculated by

$$E = \frac{1}{2}Li^2, \tag{2.1}$$

when L is an inductance, and i is a current of an inductor. The inductance L can be calculated by

$$L = \frac{\mu_O N^2 A}{l}, \tag{2.2}$$

when μ_O is the permeability of free space ($\mu_O = 4\pi \times 10^{-7}$ H/m), N is turns the number winding, A is a cross-area of core, and l is a length of core. The relationship of magnetic flux can be expressed by

$$B = \mu_O H = \frac{\mu_O N i}{l}, \tag{2.3}$$

and the inductor current is given by

$$i = \frac{Bl}{\mu_O N}. \tag{2.4}$$

Replacing the inductance (2.2) and the current (2.4) into (2.1), the relationship between the energy storage of inductor (E) and the area/size of a core (Al) can be shown as follows:

$$Al = \frac{2\mu_O}{B^2} E. \tag{2.5}$$

It can be seen that if a high current flows into an inductor, the energy storage of the inductor is high, which relates to the size of the ac inductor. Therefore, to reduce the size of the inductor, it can be done by two techniques: decreasing the inductance (L) or reducing the inductor current (i).

Firstly, by increasing the switching frequency, it is possible to reduce the ac inductance. Nevertheless, the switching losses in switching devices will be significantly increased if an active front-end operates in the hard-switching mode. As a result, the efficiency of the whole system woulde be decreased.

Secondly, by reducing the current (i), the size of the inductor can be significantly decreased in term i^2. This technique is used to reduce the size of ac inductors in the proposed circuit, which will be presented in the next chapter.

2. LITERATURE REVIEW OF BEV CHARGING SYSTEMS AND ACTIVE FRONT-END RECTIFIER

Chapter 3

Three-Phase Didoe Rectifer with an Instantaneous Reactive Power Compensator (IRPC)

3.1 Introduction to three-phase didoe rectifer with an IRPC

Nowadays, harmonic-free ac/dc rectifiers have widely been used as dc power supplies for various applications. PWM rectifiers are one of the most popular rectifiers which have the capability of bidirectional power flow control, dc-link voltage regulation, and unity power factor. However, the PWM rectifiers cause a relatively large switching power loss and electromagnetic interference (EMI).

In this thesis, a three-phase diode rectifier with an instantaneous reactive power compensator (IRPC) is the interesting circuit to improve an efficiency and a power density of the ac/dc conversion system. The proposed circuit is similar to a conventional three-phase diode rectifier with an active power filter (APF). A conventional APF is connected in parallel with the ac side of the diode rectifier and only provide the compensating harmonic current to the rectifier. Especially, APFs can effectively compensate the harmonic current of the rectifier equipped with a smoothing inductor as shown in Figure 3.1, because it can be considered as a harmonic current source. The required rms current rating of the APF is

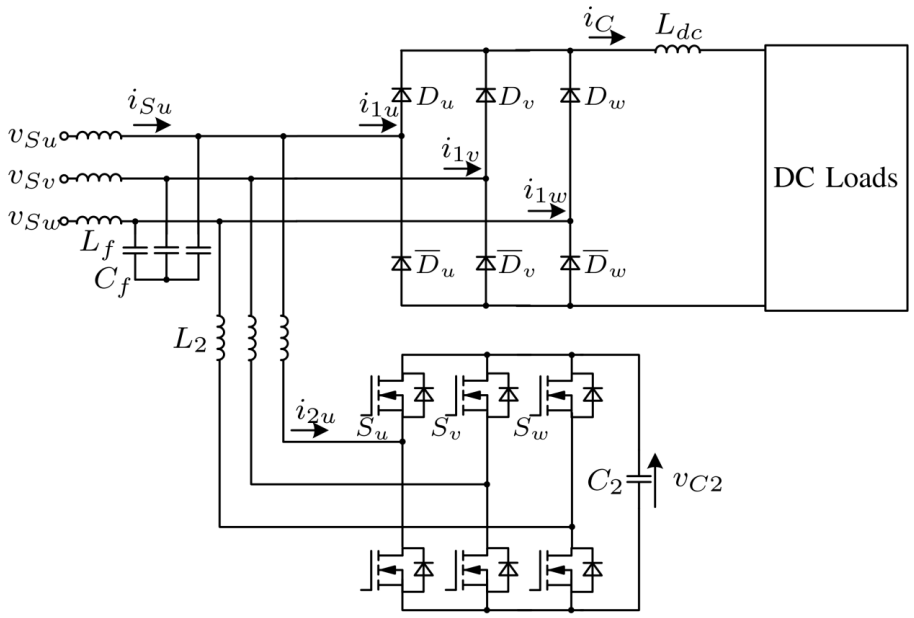

Figure 3.1: Conventional three-phase diode rectifier with smooth inductor (L_{dc}), an active power filter for harmonic current compensation.

about 1/3 of the rectifier rating, and thus, it is expected to reduce the switching power loss in the APF and the volume of the whole system, compared with a conventional PWM rectifier.

On the other hand, it is difficult for APFs to compensate the harmonic current of a diode rectifier with a smoothing capacitor as shown in Figure 3.2. The diode rectifier behaves as a harmonic voltage source with a low impedance due to its large smoothing capacitor [15]. When the APF is operated, the rectifier draws an increased harmonic current into the smoothing capacitor. As a result, the APF requires a large current rating and causes an additional switching and conduction power losses in APF. For this reason, a relatively large ac inductor is often connected to the ac terminals of the rectifier for suppressing the harmonic current drawn from the APF [15].

Figure 3.3 depicts the proposed circuit. The small ac inductor is placed at the ac side of the diode rectifier to increase its impedance, and a small film capacitor is used at the dc-link voltage connecting to a dc/dc converter. When the dc/dc converter controls power to load, the ac current of the diode rectifier is formed

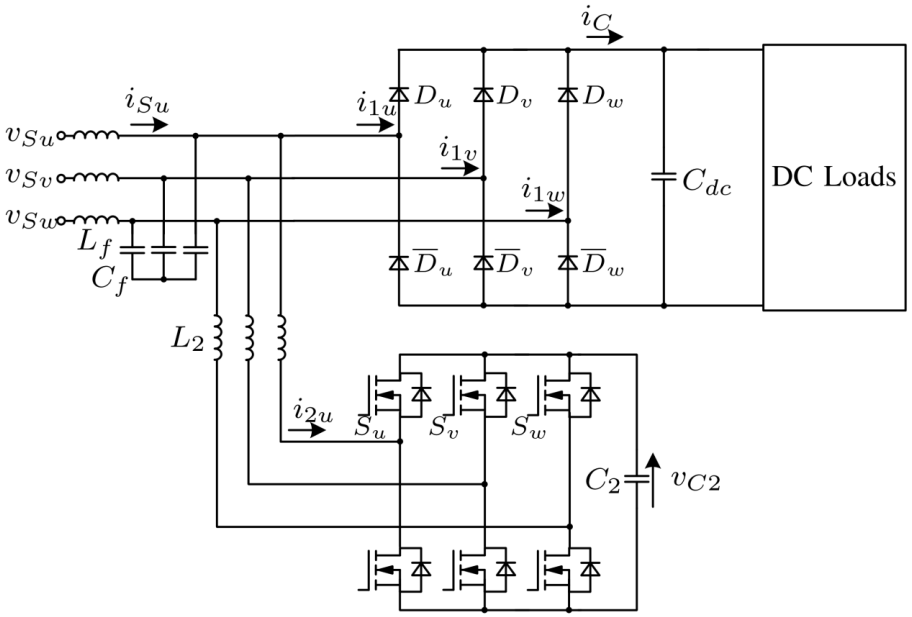

Figure 3.2: Conventional three-phase diode rectifier with smooth capacitor (C_{dc}), an active power filter for harmonic current compensation.

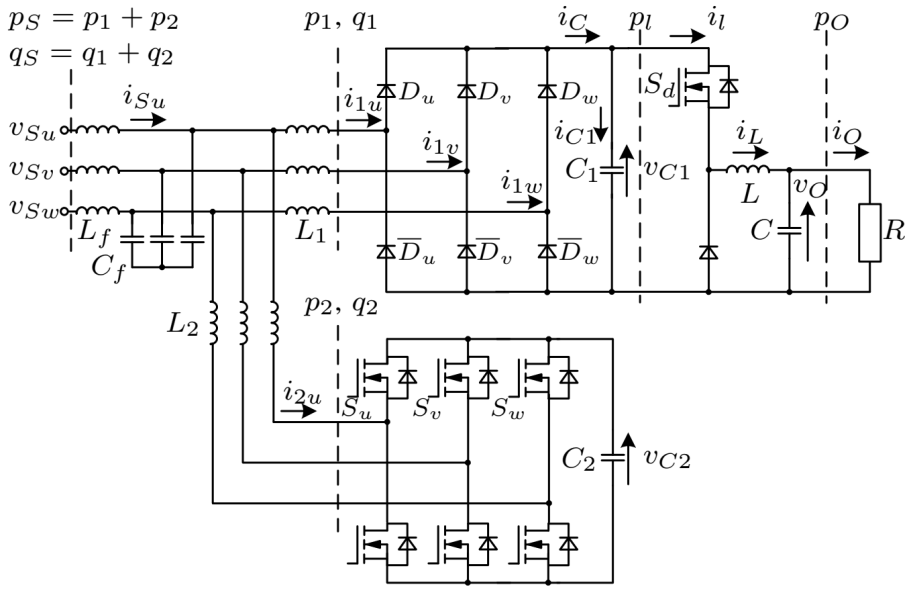

Figure 3.3: Proposed circuit: a three-phase diode rectifier with an IRPC.

as square waveshape that behaves like a harmonic current source. Thus, the IRPC can provide the current around 32% of the grid current rating to suppress the harmonic current of the diode rectifier. This gives an opportunity to reduce a switching and conduction losses of switching devices, and can improve the efficiency and the power density of the system. Moreover, the volume of ac inductor is expected to reduce to of a conventional PWM rectifier.

This thesis presents a new control technique to control the grid current sinusoidal by estimating the instantaneous active and reactive powers of the diode rectifier having two modes such as two-diode and three-diode connections (commutation overlap).

3.2 Circuit Configuration And Difference between Conventional and Proposed Circuit

3.2.1 Circuit Configuration

Figure 3.3 shows the circuit configuration of the combined system of a diode rectifier, a buck converter, and an instantaneous reactive power compensator (IRPC). A small ac inductor L_1 of 80 μH is connected on the ac side of the rectifier, and a film capacitor C_1 of 14 μF is on its dc side. The buck converter is connected to the dc link to regulate its dc output power and ac input of the rectifier at a fixed power.

On the other hand, the IRPC is connected in parallel to the rectifier like a conventional active power filter. The IRPC consists of six Si-MOSFETs (IXFB110N60P3: 600 V, 110 A, IXYS). Its switching frequency was set at 20 kHz in the following experiments. The IRPC equipped with a small film capacitor C_2 of 28 μF on the dc side and an ac inductor L_2 of 390 μH on the ac terminal.

In Table 3.1, the circuit parameters are summarized.

Table 3.1: All parameters of the proposed system

Parameters		Value
Line-to-line grid voltages / grid frequency	V / f_S	200 V / 50 Hz
Inductance of ac filter inductor	L_f	300 μH
Capacitance of ac filter capacitor	C_f	6 μF
Inductance of rectifier inductor	L_1	80 μH
Inductance of compensator inductor	L_2	390 μH
Capacitance of dc-link capacitor	C_1	14 μF
Capacitance of compensator capacitor	C_2	28 μF
Inductance of buck inductor	L	800 μH
Capacitance of buck capacitor	C	14 μF
Resistance of DC load resistor	R	10.5 Ω
Switching frequency	f_{sw}	20 kHz
Output power	P_O	4.5 kW

3.2.2 Difference between Conventional Diode Rectifiers and The Proposed Circuit

Figure 3.1 illustrates the conventional circuit with APF. The dc inductor of L_{dc} is used to suppress the compensating harmonic currents from the APF and to reduce the ripple ac currents of the rectifier which are assumed to be a square waveform without ripple current. The diodes carry ac currents to the dc side depending on the maximum and the minimum voltages of the three-phase voltage source which has a six-stage commutation. Therefore, there are six different circuits of the diode rectifier in a period. For example, the rectifier circuit in the state $n = 2$ when $v_{Su} > v_{Sv} > v_{Sw}$. The diodes D_u and $\overline{D}_w$ contain the currents as shown in Figure 3.4(a). When the three-phase voltage source changes to $v_{Sv} > v_{Su} > v_{Sw}$ in the state $n = 3$, the diode D_u is immediately turned off, whereas the ac current starts flowing into diode D_v to the dc side. This is because the dc-link voltage is higher than the line-to-line grid voltage during changing state of the diode rectifier.

In the proposed circuit as depicts in Figure 3.3 with parameter in Table 3.1, a small ac inductance of L_1 and a small dc capacitance of C_1 are used in the

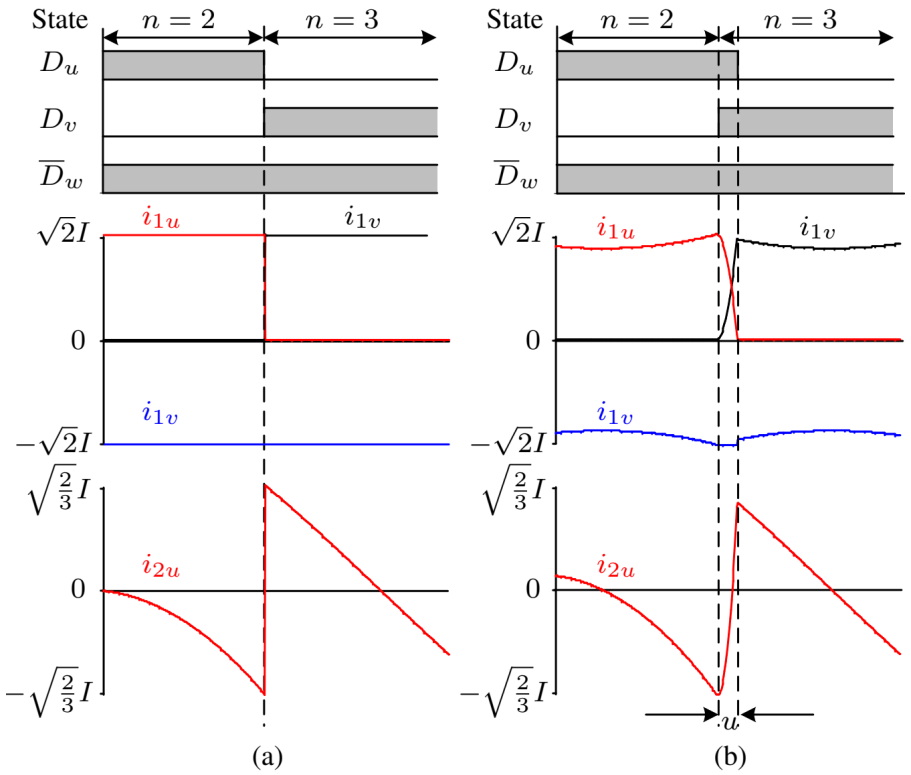

Figure 3.4: Difference of (a) the conventional and (b) proposed circuit when the commutation of diode rectifier changes state from grid voltages $v_{Su} > v_{Sv} > v_{Sw}$ (the state $n = 2$) to $v_{Sv} > v_{Su} > v_{Sw}$ (the state $n = 3$).

circuit, and thus, the dc-link voltage is approximately the same as the line-to-line grid voltage. When the stage changes from $n = 2$ ($v_{Su} > v_{Sv} > v_{Sw}$) to $n = 3$ ($v_{Sv} > v_{Su} > v_{Sw}$), the commutation overlap angle (u) appears in the diodes of D_u, D_v and $\overline{D}_w$ which contain currents in the same time as shown in Fig. 3.4(b). This phenomenon occurs in a short time every the changed state of the diode rectifier according to the grid voltages. The benefit of this method is that the control unit can create the slop for the currents of the IRPC changing from peak to peak. This can reduce the error state in the current controllers.

3.3 Basically Proposed Circuit Operation

Fig. 3.5 shows an equivalent circuit of the harmonic-free rectifier system shown in Fig. 3.3. Here, the current sources i_{2u}, i_{2v}, i_{2w} represent the compensating current injected by the IRPC, and the buck is replaced with a controlled current source i_l which draws the constant output power P_O from the diode rectifier. A balanced three-phase source voltage is also assumed as follows:

$$\begin{bmatrix} v_{Su} \\ v_{Sv} \\ v_{Sw} \end{bmatrix} = \sqrt{\frac{2}{3}} V_S \begin{bmatrix} \sin(\omega t) \\ \sin\left(\omega t - \frac{2\pi}{3}\right) \\ \sin\left(\omega t + \frac{2\pi}{3}\right) \end{bmatrix}, \tag{3.1}$$

when V_S is the rms value of the line-to-line source voltage, ω is the source angular frequency. The filter inductor L_f and capacitor C_f are neglected for the sake of simplicity. The diode rectifier takes one of six conduction states, according to the the three-phase grid voltage v_S. In this paper, the state is defined as $n = \lfloor 3\omega t/\pi + 0.5 \rfloor$. Fig. 3.5 assumes a period $\pi/2 \leq \omega t < 5\pi/6$ or in the state $n = 2$. During $v_{Su} > v_{Sv} \geq v_{Sw}$, the u-phase upper and w-phase diodes are conducting. Fig. 3.6 depicts theoretically operating waveforms. Since a small dc capacitor C_1 is used, the dc capacitor voltage v_{C1} has a three-phase rectified voltage, obtained as

$$v_{C1} = \sqrt{2} V_S \cos\left(\omega t - \frac{n}{3}\pi\right). \tag{3.2}$$

According to the state n, the dc current i_C flows out to the ac side. For example, in state $n = 2$, $i_{1u} = i_C$, $i_{1v} = 0$, and $i_{1w} = -i_C$. Thus, the ac current i_1 has a rectangle waveform as shown in Fig. 3.6. The instantaneous active and reactive power drawn into the rectifier can be calculated as

$$\begin{bmatrix} p_1 \\ q_1 \end{bmatrix} = \begin{bmatrix} v_{S\alpha} & v_{S\beta} \\ -v_{S\beta} & v_{S\alpha} \end{bmatrix} \begin{bmatrix} i_{1\alpha} \\ i_{1\beta} \end{bmatrix}, \tag{3.3}$$

where

$$\begin{bmatrix} v_{S\alpha} \\ v_{S\beta} \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} v_{Su} \\ v_{Sv} \\ v_{Sw} \end{bmatrix} \tag{3.4}$$

$$\begin{bmatrix} i_{1\alpha} \\ i_{1\beta} \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} i_{1u} \\ i_{1v} \\ i_{1w} \end{bmatrix}. \tag{3.5}$$

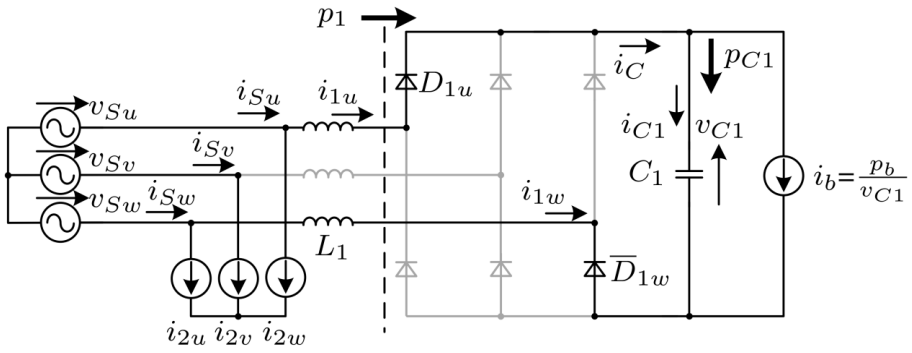

Figure 3.5: Operating circuit of the diode rectifier in the state $n = 2$.

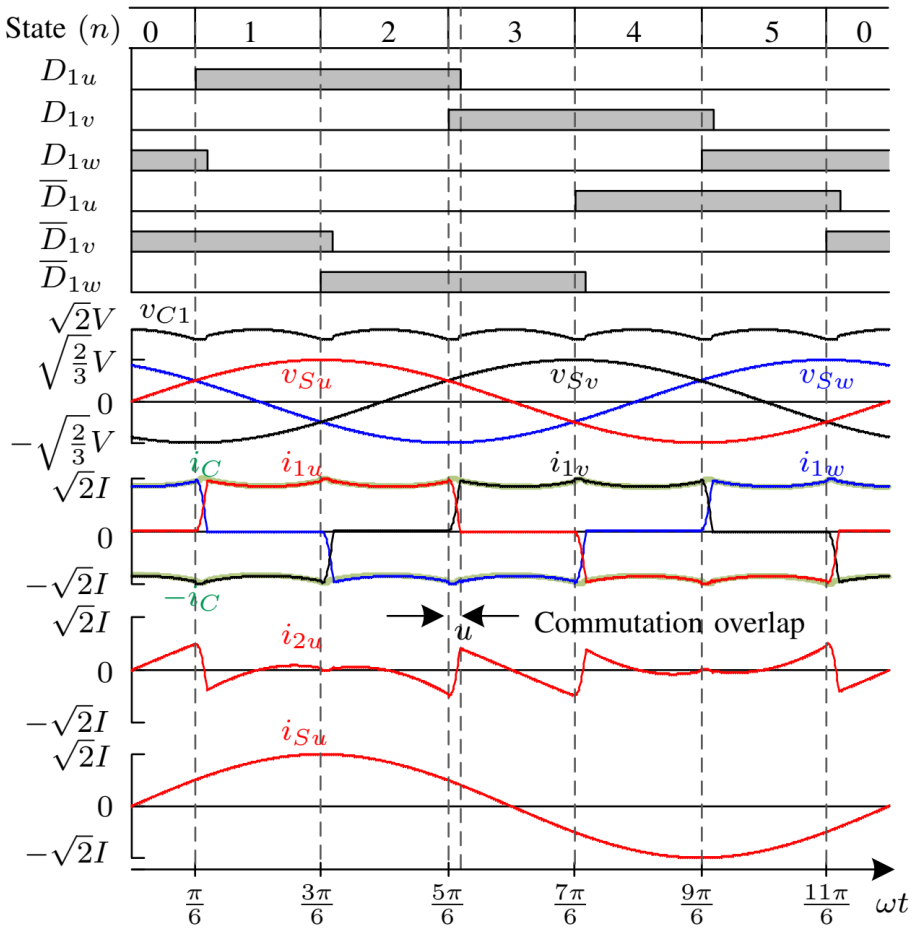

Figure 3.6: Theoretical waveform of the proposed circuit.

Substituting (3.2) into (3.3) yields

$$p_1 = v_{C1} i_C = p_{C1} + p_b, \tag{3.6}$$

$$q_1 = -\sqrt{2} V_S \frac{p_{C1} + p_b}{v_{C1}} \sin\left(\omega t - \frac{n}{3}\pi\right), \tag{3.7}$$

where p_{C1} is the power flowing into C_1 given by

$$\begin{aligned} p_{C1} &= \frac{d}{dt}\left(\frac{C_1 {v_{C1}}^2}{2}\right) \\ &= -\omega C_1 {V_S}^2 \sin\left(2\omega t - \frac{2n}{3}\pi\right). \end{aligned} \tag{3.8}$$

For compensating the grid harmonic current, the ac components in p_1 and q_1 have to be eliminated. Assuming a small C_1 and neglecting p_{C1}, the instantaneous active power approximately equals the constant load power as $p_1 \approx p_b$. The compensator has to cancel the instantaneous reactive power only as ${p_2}^* = 0$ and ${q_2}^* = -q_1$.

The compensating current i_2 can be obtained by using the inverse calculation in [16]. The compensating current i_2 is almost equal to a half of the grid current in peak, and the volume of the inductor L_2 is estimated as 1/4 of the inductor used in a conventional PWM rectifier. On the other hand, the rms current is also reduced to about 1/3, and the conduction losses are expected to be decreased to 1/9.

3.4 Commutation Overlap of Diode Rectifier

Fig. 3.7 depicts a conduction state of the overlap duration of the three-phase diode rectifier at the beginning of state $n = 3$ where $v_{Sv} \geq v_{Su}$. The ac inductor L_1 makes it possible to reduce di_1/dt, and enables the compensating current i_2 to follow the harmonic current reference. However, this causes an overlap duration and affects the rectifier current i_1 and the instantaneous active and reactive power p_1 and q_1. In this overlap duration, the diodes D_{1u} and D_{1v} are conducting at the same time. Thus, the dc voltage is approximately given by

$$v_{C1} = \frac{v_{Su} + v_{Sv}}{2} - v_{Sw}$$

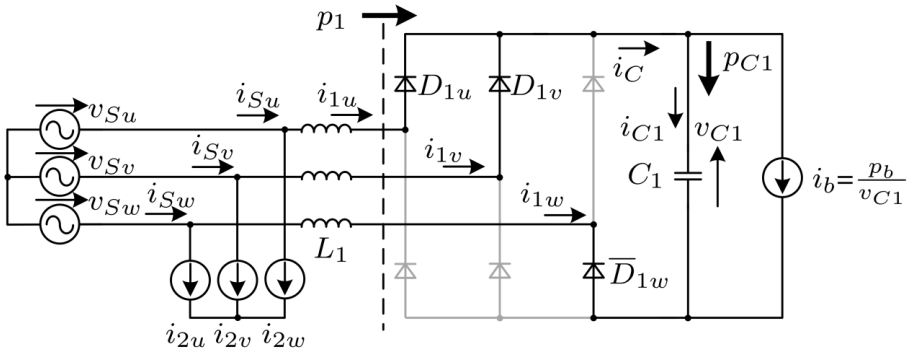

Figure 3.7: Operating circuit of the diode rectifier in the state $n = 3$ during the commutation overlap.

$$= \sqrt{\frac{3}{2}} V_S \sin\left(\omega t - \frac{\pi}{3}\right), \tag{3.9}$$

or

$$v_{C1} = \sqrt{\frac{3}{2}} V_S \sin\left(\omega t - \frac{n-2}{3}\pi\right), \tag{3.10}$$

and the power flowing into the dc capacitor is represented by

$$p_{C1} = -\frac{3\omega C_1 {V_S}^2}{4} \sin\left(2\omega t - \frac{2}{3}\pi\right). \tag{3.11}$$

Since the line-to-line voltage between u and v phases applies across two ac inductors L_1, the v-phase current gradually increases as

$$\frac{di_{1v}}{dt} = \frac{v_{Sv} - v_{Su}}{2L_1} = \frac{V_S}{\sqrt{2}L_1} \sin\left(\omega t - \frac{5}{6}\pi\right), \tag{3.12}$$

and thus,the v-phase current is obtained from (3.12) as

$$i_{1v} = \frac{V_S}{\sqrt{2}\omega L_1}\left[1 - \cos\left(\omega t - \frac{5}{6}\pi\right)\right]. \tag{3.13}$$

The v-phase current i_{1v} meets to the dc current i_C at the end of the overlap duration. Thus, the overlap angle is given by

$$u = \cos^{-1}\left(1 - \frac{\sqrt{2}\omega L_1}{V_S} i_C\right). \tag{3.14}$$

In the overlap duration, the u-phase and w-phase currents are $i_{1u} = i_C - i_{1v}$ and $i_{1w} = -i_C$. From (3.3), the instantaneous active power can be derived as follows:

$$\begin{aligned} p_1 &= (v_{Su} - v_{Sw})i_C + (v_{Sv} - v_{Su})i_{1v} \\ &= v_{C1}i_C + (v_{Sv} - v_{Su})\left(i_{1v} - \frac{i_C}{2}\right). \end{aligned} \tag{3.15}$$

The second term represents the power released from and/or absorbed into the u-phase and v-phase ac inductors L_1, and its average value is zero in the overlap duration. Considering in the v-phase inductor, the power can be given by

$$p_{L1v} = \frac{v_{Svu}}{2} i_{1v}, \tag{3.16}$$

and the inductor power of u-phase can be shown by

$$p_{L1v} = -\frac{v_{Svu}}{2}(i_C - i_{1v}), \tag{3.17}$$

when the direction of the inductor power depends on the polarity of its current. Thus, the total inductor power in this state can be calculated by

$$p_L = p_{L1u} + p_{L1v} = v_{Svu}\left(i_{1v} - \frac{i_C}{2}\right). \tag{3.18}$$

The average total inductor power is zero during the overlap angle u. Substituting (3.18) into (3.15), the output power from the ac side to dc side of the rectifier is equal to

$$P_O = p_1 - p_L = v_{C1}i_C, \tag{3.19}$$

The instantaneous reactive power is also obtained as follows:

$$q_1 = -\sqrt{3}v_{Sv}i_C - \sqrt{3}v_{Sw}i_{1v}. \tag{3.20}$$

From (3.6), (3.7), (3.21), and (3.22), it is possible to summarize the instantaneous active and reactive power in states from $n = 0$ to 5 as follows:

$$p_1 \approx p_{C1} + p_b \tag{3.21}$$

$$q_1 = \begin{cases} \sqrt{2}V_S \frac{p_{C1}+p_b}{v_{C1}} \sin\left(\omega t - \frac{n+2}{3}\pi\right) & \\ \quad + \frac{{V_S}^2}{\omega L_1} S(1-S) & (\omega t - \frac{2n-1}{6}\pi \leq u)\,, \\ -\sqrt{2}V_S \frac{p_{C1}+p_b}{v_{C1}} \sin\left(\omega t - \frac{n}{3}\pi\right) & (u < \omega t - \frac{2n-1}{6}\pi) \end{cases} \tag{3.22}$$

where $S = \sin\left(\omega t - \frac{n-2}{3}\pi\right)$. The active power p_1 can be considered to be almost equal to dc power even in the overlap duration. In other words, the rectifier mainly produces ac components in q_1. Thus, the IRPC can compensate for the harmonic current with a very small capacitor C_2 as an energy storage element.

Figure 3.8 shows the simulation results of the active power p_1 by using the parameters in Table. 3.1 at the power 5 kW. The components of the active power p_1 consist of the output power P_O and the total inductor power of v- and u-phase p_L which has the average value of zero during the commutation overlap.

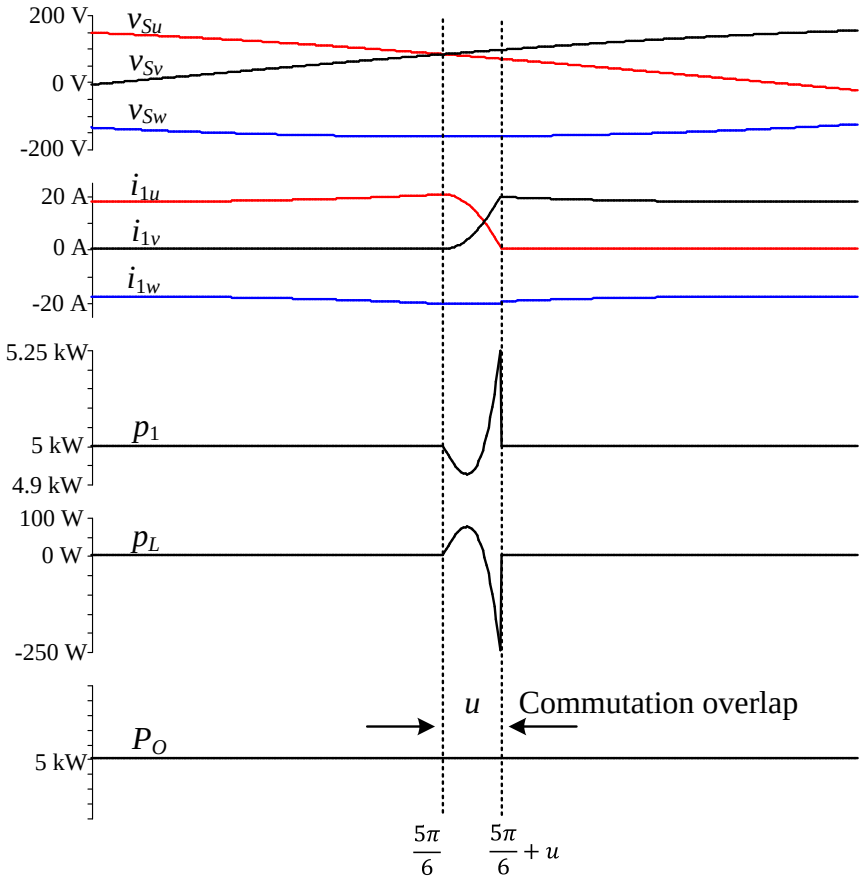

Figure 3.8: Simulation results the instantaneous active power p_1 of the diode rectifier in the state $n = 3$ during the commutation overlap.

It can be seen that the summation between the instantaneous active power and the total inductor power equals to the load power P_O, and thus, the rectifier can pass the load power P_O from the ac side to the dc side as same as the two diode commutation. This can confirm that the IRPC can inject only the reactive power to the grid current.

3.5 Instantaneous Reactive Power Compensator

For compensating the harmonic currents, the ac components in p_1 and q_1 have to be eliminated. Assuming a small C_1 and neglecting the capacitor current i_{C1}, the instantaneous active power approximately equals the constant load power as $p_1 \approx P_O$. The instantaneous active power and reactive power at the grid source voltage are from the summation between powers of the rectifier and the IRPC as expressed by

$$p_S = p_1 + p_2^* = P_O, \text{ and } q_S = q_1 + q_2^* = 0, \tag{3.23}$$

The IRPC has to cancel the instantaneous reactive power only, and its reference is provided as

$$p_2^* = 0, \text{ and } q_2^* = -q_1. \tag{3.24}$$

The compensating current i_2 can be obtained by using the inverse calculation in [16]. It is clearly seen that the IRPC does not provide the active power into the grid system. Thus, a small film capacitor can be used at the dc voltage of the IRPC. From (3.24), the rms current per phase of the IRPC can be calculated by

$$I_2 = I\sqrt{\frac{2\sqrt{3}}{\pi} - 1} \approx 0.32I. \tag{3.25}$$

The compensating current i_2 is almost equal to a half of the grid current in peak, and the volume of the inductor L_2 is estimated as 1/4 of the inductor used in a conventional PWM rectifier. On the other hand, the rms current is also reduced to about 1/3, and the conduction losses are expected to be decreased to 1/9.

Figure 3.9 shows the original concept to find the instantaneous active power and the instantaneous reactive power of the proposed circuit. The buck converter controls the power P_O and the dc-link capacitor power p_{C1} to the load. Because

of this, the dc-link current (i_{C1}) or the dc-link power p_{C1} of the rectifier can be negligible. From the dc-link voltage v_{C1} in either (3.2) or (3.9) depending on the state n and the commutation of the rectifier, the dc-link power p_{C1} can be obtained by $p_{C1} = v_{C1}C_1\frac{dv_{C1}}{dt}$. However, the dc-link power p_{C1} is an ac component included in the power command of the buck converter (P_b^*). This causes the output ripple voltage ($\triangle v_O$) as depicted by

$$\Delta v_O = \frac{1}{C_O}\int_{-\frac{\pi}{3\omega}}^{0}\frac{p_{C1}}{v_O}dt \approx \frac{C_1{V_S}^2}{4C_OV_O}, \tag{3.26}$$

Another method is that including the dc-link power p_{C1} in the instantaneous active power and reactive power of the IRPC. This dc-link power of the rectifier is injected from the dc capacitor of the IRPC to the ac side of the rectifier as shown in Figure (3.10). Therefore, the buck converter controls the constant power to the load. Nevertheless, the dc-link power in p_2^* causes the dc ripple voltage of the IRPC inversely proportion of the dc-link ripple voltage. The dc ripple voltage of the IRPC depends on the dc capacitance of C_2 relating with its energy storage. Thus, the peak-to-peak of v_{C2} can be calculated by

$$\Delta v_{C2} = \frac{1}{C_2}\int_{-\frac{\pi}{3\omega}}^{0}\frac{p_{C1}}{v_{C2}}dt \approx \frac{C_1{V_S}^2}{4C_2V_{C2}}, \tag{3.27}$$

where V_{C2} is the reference dc voltage of IRPC.

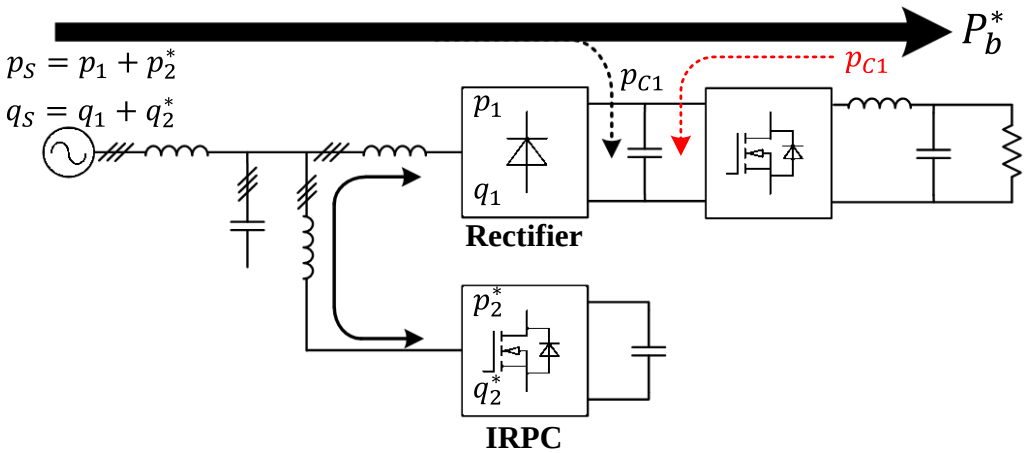

Figure 3.9: The dc-link power p_{C1} compensated by the dc/dc converter.

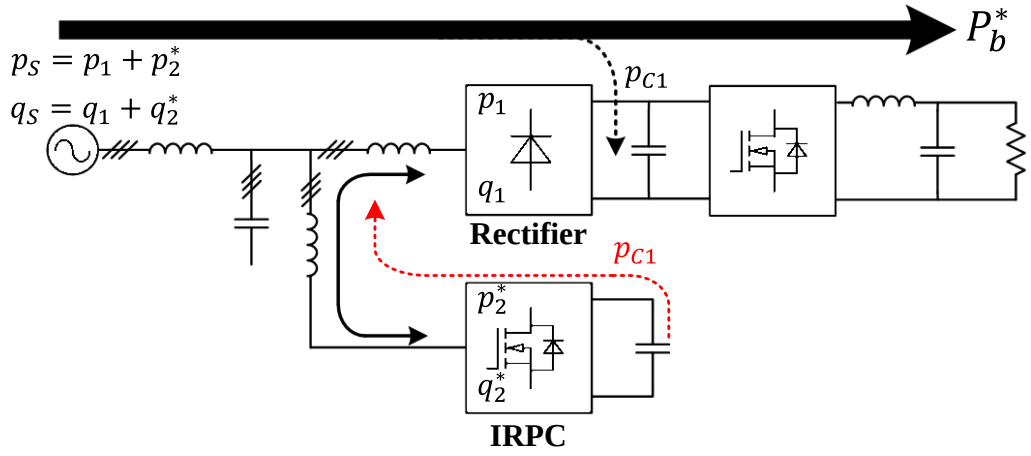

Figure 3.10: The dc-link power p_{C1} compensated by the IRPC.

3.6 Summary

This chapter presents the proposed active front-end based on the three-phase diode rectifier with the IRPC. The diode rectifier behaves as the harmonic current source produces a square waveform for the ac side of the rectifier. The IRPC injects the compensating rms current of 32% to suppress the harmonic current of the rectifier. As a result, the conduction and switching losses of the IRPC are expected to be decreased to 1/9 of a conventional PWM rectifier. Moreover, the compensating current i_2 is almost equal to a half of the grid current in peak, and the volume of the inductor L_2 is estimated as 1/4 of the inductor used in a conventional PWM rectifier.

The active and reactive power of the diode rectifier are estimated based on the instantaneous active and reactive power theory for using to be the power commands for the IRPC. From analysis, the IRPC can produce only the reactive power to eliminate the reactive power of the rectifier, whereas there are a little active power components include in the active power of the IRPC such as the dc-link power compensation and the output power caused by the dc voltage controller using to regulate the IRPC's voltage. The control methods will be present on the next chapter.

3. THREE-PHASE DIDOE RECTIFER WITH AN INSTANTANEOUS REACTIVE POWER COMPENSATOR (IRPC)

Chapter 4

Stability Problem from Resonant Frequency and Control method

In an ac/dc power conversion system, switching devices that are active with a high switching frequency are the main role to control currents/voltages between a three-phase voltage source and dc-link voltage. This causes high switching harmonics flowing into the three-phase voltage source, and it has a chance to generate EMI problems for other equipment [65] - [69]. Thus, LC filters are used to attenuation of the switching harmonic without increasing power losses of a system. Nevertheless, LC components would cause an instability from the resonant frequency. Thus, the damping method is necessary to control the stability of the circuit.

The damping control method has mainly 2 types such as a passive damping and an active damping method [70]. Generally, a passive damping, which adds a resister in the circuit, can effectively eliminate the resonance, but this method causes the increasing power loss in the system. Because of this, the efficiency of the circuit can be reduced [71]. To avoid the power losses, an active damping method is a choice to maintain the stability of the system.

This chapter presents the cause of unstable in the proposed circuit, and discusses the active damping method to control stability of the system. The experimental setup is used to verify the damping control methods and the new control technique.

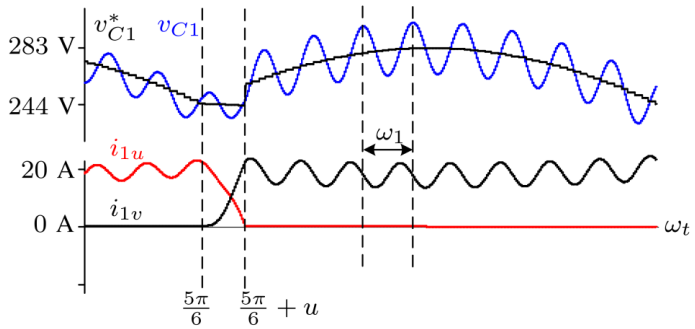

Figure 4.1: Simulation result of resonance in the dc-link voltage v_{C1} by using a current source instead of the buck converter, and neglecting L_f and C_f. during the state $n = 2$ and $n = 3$

Figure 4.1 depicts a simulation waveform of the proposed circuit in Figure 3.3 which is closed up around the overlap duration between states $n = 2$ and 3. The parameter can be shown in Table. 3.1. In this simulation, L_f and C_f at the grid voltage are negligible for a sake of simplify. The overlap starts at $\omega t = \frac{5\pi}{6}$ and finishes at $\omega t = \frac{5\pi}{6} + u$. The dc capacitor voltage v_{C1} includes two different frequency components: one is from the switching component in the current ripple flowing from the buck converter, and the other is from the resonance between the dc capacitor C_1 and the ac inductor L_1. The resonant frequency between C_1 and L_1 is about $\omega_1 = 2.8$ kHz. The switching ripple component in i_{1u} and i_{2u} are not so large because of the impedance of the ac inductor L_1. On the other hand, the resonant current component is much larger than the switching ripple component. Note that the disturbance increases the amplitude of the resonant current component in the dc-link voltage after the end of the overlap duration. A step-change induces the disturbance in the dc-link voltage v_{C1}, which causes the voltage difference between the overlap and the non-overlap as shown in (3.9) and (3.2), respectively. The dc-link voltage can be expressed in the simple equations by

$$v_{C1}(t) = v_{C1}(0) - (i_C(0) - i_l(0))Z_1 \cos(\omega_1 t), \tag{4.1}$$

when ω_1 is the resonant frequency between L_1 and C_1 equal to $\frac{1}{\sqrt{2L_1C_1}}$, and $Z_1 = \sqrt{\frac{2L_1}{C_1}}$ is a characteristic impedance. It can be seen that if the capacitance

of C_1 is decreased, the impedance of Z_1 is high. Because of this, the ripple in the dc-link voltage is higher than the high capacitance of C_1. Therefore, to maintain the system's stability from the resonant frequency, the damping control needs to be used in the control system. In this thesis, the active damping control based on the virtual conductance will be proposed.

4.1 Damping Control Method

4.1.1 Equivalent Circuit at Resonant Frequency

Figure 4.2 shows the operating circuit of the rectifier in the state $n = 2$. At this time, the LC-filter (L_f, C_f) at the ac grid voltage are considered with the diode rectifier, whereas the IRPC currents are negligible because the IRPC can control its currents like a current source which are independent from the resonant frequency in the rectifier circuit. Figure 4.3 illustrates the new drawing circuit of the rectifier. Assuming the impedance of C_f is the same value of each phase. As a result, there is not the v-phase current flowing into the ac grid voltage, and then, the LC-component of v-phase can be ignored. In this circuit, the resonant angular frequency is approximately given by

$$\omega_r = \frac{1}{\sqrt{2(L_f + L_1)C_1}}. \tag{4.2}$$

Considering only the ripple components in Figure 4.3, the grid voltage sources can be negligible. The ac filter inductors and capacitors are considered as the impedance seen from the u- and w-phase terminals of the rectifier as $2L_f$ and $\frac{C_f}{2}$. The current source i_b represents the input current of the buck converter. The input power the buck converter can be given by

$$\begin{aligned} p_b &= v_{C1} i_b, \\ P_b + \Delta p_b &= (V_{C1} + \Delta v_{C1})(I_b + \Delta i_b), \end{aligned} \tag{4.3}$$

when P_b, V_{C1}, I_b are the fundamental signals of the input power of the buck converter, the dc-link voltage and the input current of the buck converter, while Δp_b,

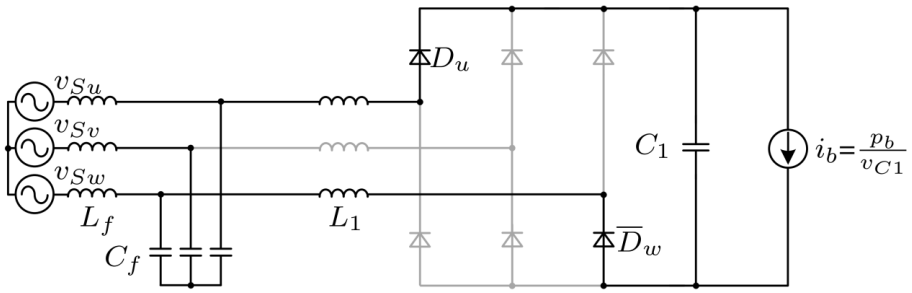

Figure 4.2: The operating circuit of the diode rectifier in Figure 3.3 during the state $n = 2$

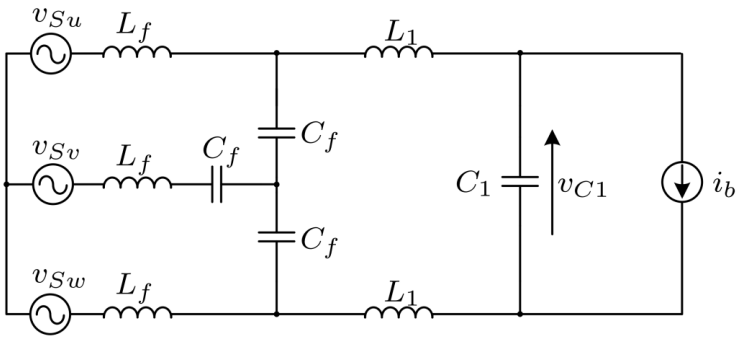

Figure 4.3: The new drawing circuit of Figure 4.2

Δv_{C1}, Δi_b are the ripple components. Neglecting $\Delta v_{C1}\Delta i_b$, an approximation is obtained as

$$\Delta p_b \approx V_{C1}\Delta i_b + \Delta v_{C1} I_b. \tag{4.4}$$

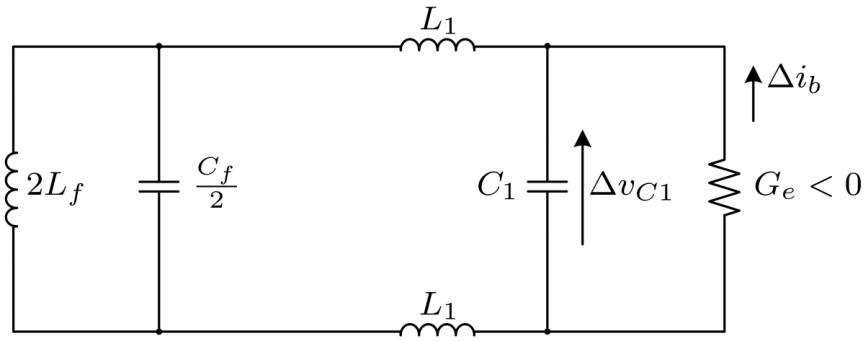

Figure 4.4: The equivalent circuit of the diode rectifier

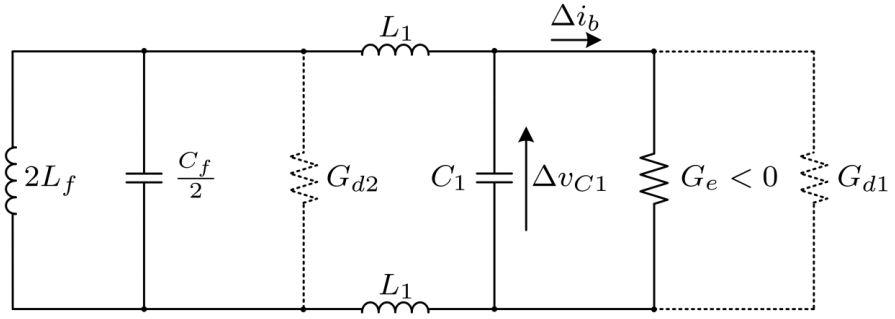

Figure 4.5: Equivalent circuit obtained from small signal analysis.

When the buck converter only provides a constant power P_b to the load, this results in $\Delta p_b = 0$. From (4.4), the equivalent conductance can be derived for the voltage change Δv_{C1} as

$$G_e = \frac{\Delta i_b}{\Delta v_{C1}} = -\frac{I_b}{V_{C1}} = -\frac{P_b}{V_{C1}^2}. \tag{4.5}$$

Figure 4.4 shows the equivalent circuit of the rectifier when the conductance G_e connected to the dc capacitor C_1 represents the behavior of the buck converter against the dc voltage v_{C1}. In this case, the equivalent conductance G_e would make the system unstable because it has a negative value.

4.1.2 Traditional Design

From Figure 4.4, it is possible to add an additional conductance G_{d1} to cancel the current flowing into the negative conductance and to make the system stable. Figure 4.5 depicts an equivalent circuit which has G_{d1} to adjust the total equivalent conductance. For example, an additional positive conductance can be connected in parallel with the negative one G_e to improve the stability as

$$G_{d1} = -G_e. \tag{4.6}$$

Then, i_b can be maintained at the fixed value of I_b, and its change is eliminated as $\Delta i_b = 0$. Instead of installing of a real conductance, a virtual conductance can be implemented in the buck converter control as a damping control method. A

small change is intentionally added to the power reference for the buck converter, p_b^*, as

$$\Delta p_b^* = \Delta p_d = V_{C1} G_{d1} \Delta v_{C1}, \tag{4.7}$$

where G_{d1} [S] is a control gain contributing as a damping conductance. Substituting (4.7) into (4.4) yields

$$\Delta i_b = (G_{d1} + G_e)\Delta v_{C1} \tag{4.8}$$

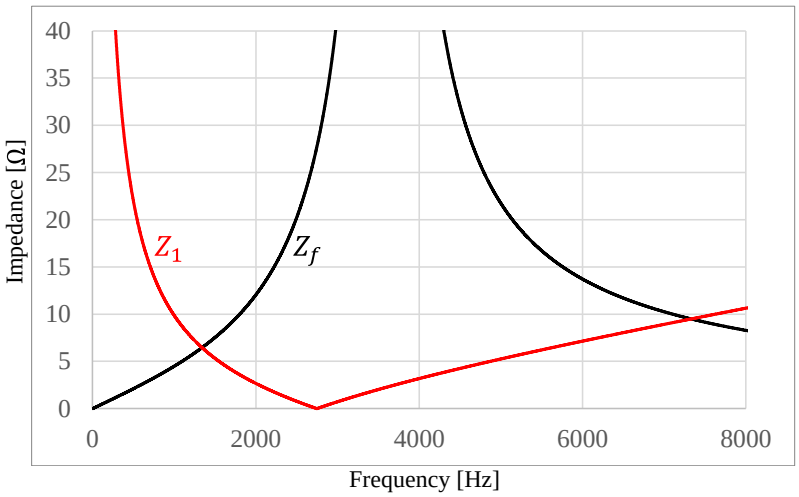

Figure 4.6: LC-impedance of the rectifier side and the LC-filter at grid side by using parameters of Table. 3.1

Moreover, the damping control is also applicable to the IRPC. From Figure (4.5), it can be seen that the LC-filter at the grid voltage (L_f and C_f) are the parallel LC circuit. The impedance of this circuit can be calculated by

$$Z_f = \frac{1}{\sqrt{\left(\frac{1}{X_{Lf}} - \frac{1}{X_{Cf}}\right)^2}}, \tag{4.9}$$

when $X_{Lf} = 2\pi f(2L_f)$, and $X_{Cf} = \frac{1}{2\pi f(C_f/2)}$, and f is frequency. And the LC components of the rectifier is connected like the series LC circuit which can be calculated the impedance by

$$Z_1 = \left(\frac{1}{X_{L1}} - \frac{1}{X_{C1}}\right)^2, \tag{4.10}$$

when $X_{L1} = 2\pi f(2L_1)$, and $X_{C1} = \frac{1}{2\pi f(C_1/2)}$. From the parameters in Table. 3.1, Figure 4.6 depicts the impedance of LC component between the ac side (L_f, C_f) and the rectifier side (L_1, C_1). It can be seen that the rectifier have a lower impedance than the ac filter L_f and C_f at the resonant frequency. Thus, it is possible to add the damping control in the IRPC controller. The following power component should be superposed on the power reference for the IRPC with a gain G_{d2} [S]:

$$\Delta p_d = V_{C1} G_{d2} \Delta v_{C1}, \tag{4.11}$$

Thus, the superposed power Δp_d mainly flows into the dc capacitor C_1 and effectively eliminates the overshoot or ringing in v_{C1}. Note that this damping control method results in a reduced voltage/current ripples at the buck converter output because the power reference p_b can be maintained at a constant power of P_b.

4.1.3 Design Damping Gain

The overlap duration would cause a theoretical disturbance in the system. The theoretical dc voltages in (3.2) and (3.10) have a small difference before and after the overlap end. In other words, a step voltage change is applied across the dc capacitor C_1 at the end of the overlap. This disturbance would induce a non-negligible amount of overshoot and/or ringing in v_{C1} even when G_{d1} is set at a stable conductance in (4.6).

For this problem, the additional conductance can be set to satisfy a critical damping condition with an arbitrary damping factor of ζ. In this case, the conductance has to satisfy the following requirement:

$$G_{d1} = \zeta \sqrt{\frac{2C_1}{L_f + L_1}} - G_e, \tag{4.12}$$

Applying (4.7), the buck converter can eliminate the undesired overshoot or ringing from v_{C1}.

Applying 4.12 into 4.7, the virtual damping conductance can eliminate the undesired overshoot or ringing from v_{C1} when the damping control is operated in the buck converter. On the other hand, the same gain in **??**DampGain) can

be used in 4.11 which is the damping controller of the IRPC. This technique can reduce the output current ripple of the proposed circuit.

4.2 Control Method

4.2.1 Control Block

Figure 4.7 illustrates the control block diagram used in the following experiments. Essentially, the control block adjusts the instantaneous active and reactive power in the IRPC and the buck converter. In Figure 4.7(a), the output current reference i_O^* is calculated from the power reference p_b^*, and provided to a simple current feedback controller with a gain k_O. A feedforward term v_O is added to the voltage reference for the PWM controller.

Similarly, Figure 4.7(b) is the control block diagram of the IRPC. Its input signals is p_2^* and q_2^*. The three-phase current reference i_2^* is obtained by using the inverse calculation of (3.3) and provided to the current feedback and PWM controller. Due to using a small inductance of L_2, the winding resistance is minimal, and it is possible to be negligible. Because of this, the current control transfer function does not have a pole nearly the origin axis causing a slow response for the control system. Thus, a P controller and the three-phase voltage feedforward are enough to control the performance of the IRPC. The critical proportional gain k_C can be given by $\frac{L_2}{4T_s}$ when T_s is the sampling time of the controller.

In the dc voltage controller, since the dc capacitor C_2 is only connected to the dc side of the IRPC, dc voltage v_{C2} has to be regulated at a specific voltage. Thus, voltage feedback control term is added to p_2^*, which is calculated from the dc voltage v_{C2} and its reference v_{C2}^* by using a proportional and integral gains.

A phase lock loop (PLL) is used to detect the phase angle information ωt. The dead-time compensation and the third harmonic injection are also implemented in the PWM controllers to improve the accuracy and controllability.

4.2.2 Control Strategy

Three references p_b^*, p_2^*, and q_2^* should be provided to the control block in Figure 4.7. Aforementioned, the IRPC should compensate for the instantaneous reactive

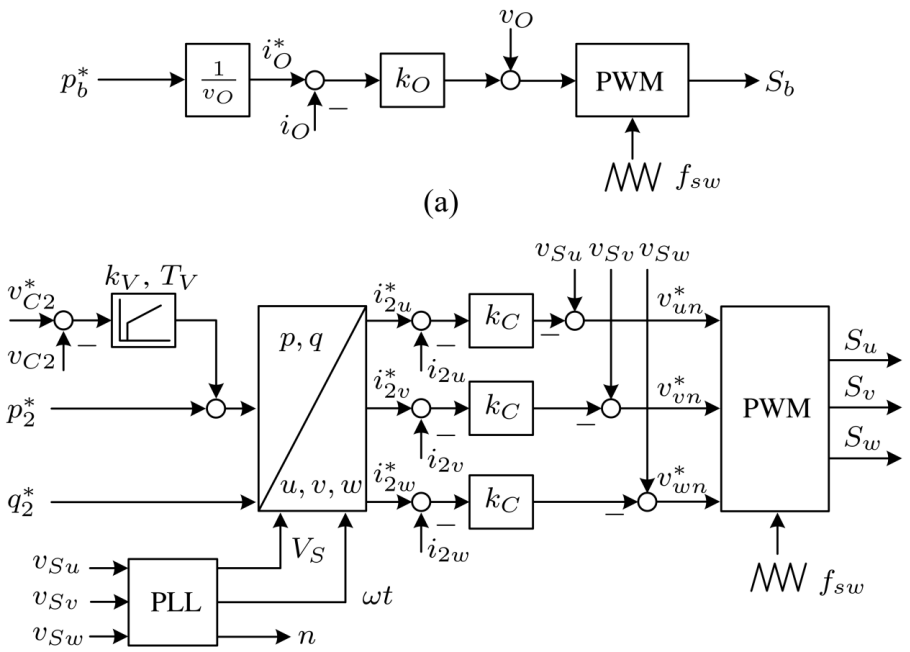

Figure 4.7: Control block diagram for (a) the buck converter and (b) the IRPC.

power produced by the rectifier. Therefore, the reference should be set as

$$q_2^* = -q_1, \tag{4.13}$$

There are four possible combinations in the control method of p_b^* and p_2^* to perform the damping control Δp_d and to compensate for p_{C1}.

- Method 1

$$p_b^* = P_O^* - p_{C1} + \Delta p_d \tag{4.14}$$

$$p_2^* = 0 \tag{4.15}$$

- Method 2

$$p_b^* = P_O^* - p_{C1} \tag{4.16}$$

$$p_2^* = \Delta p_d \tag{4.17}$$

- Method 3

$$p_b^* = P_O^* + \Delta p_d \tag{4.18}$$

$$p_2^* = -p_{C1} \tag{4.19}$$

- Method 4

$$p_b^* = P_O^* \tag{4.20}$$

$$p_2^* = -p_{C1} + \Delta p_d \tag{4.21}$$

In methods 1 and 2, the buck converter compensates for p_{C1} which is the power flowing into C_1 due to the voltage ripple in v_{C1}. This causes a ripple in the load voltage v_O. From (3.8), the peak-to-peak load voltage ripple is obtained as

$$\Delta v_O = \frac{1}{C_O}\int_{-\frac{\pi}{3\omega}}^{0} \frac{p_{C1}}{v_O} dt \approx \frac{C_1 {V_S}^2}{4 C_O V_O}, \tag{4.22}$$

where V_O is the average value of the load voltage v_O. The power p_{C1} is compensated by the IRPC, and causes a voltage ripple in v_{C2} in methods 3 and 4. The peak-to-peak voltage ripples can be expressed by

$$\Delta v_{C2} = \frac{1}{C_2}\int_{-\frac{\pi}{3\omega}}^{0} \frac{p_{C1}}{v_{C2}} dt \approx \frac{C_1 {V_S}^2}{4 C_2 V_{C2}}, \tag{4.23}$$

where V_{C2} is the average voltage of v_{C2}.

On the other hand, Δp_d is compensated by the buck converter in methods 1 and 3. The power Δp_d charges the C_1 at the end of the overlap from the voltage in (3.10) to that in (3.2). Therefore, the peak-to-peak voltage ripple in v_O is obtained as

$$\begin{aligned}\Delta v_O &= \frac{C_1}{C_O}\left[v_{C1}\left(u_+ - \frac{\pi}{6}\right) - v_{C1}\left(u_- - \frac{\pi}{6}\right)\right] \\ &= \frac{C_1 V_S}{\sqrt{2} C_O}\sin(u),\end{aligned} \tag{4.24}$$

where u_- and u_+ are the angles just before and after the overlap angel u. Similarly, the peak-to-peak voltage ripple in methods 2 and 4 is obtained as

$$\Delta v_{C2} = \frac{C_1 V_S}{\sqrt{2} C_2}\sin(u). \tag{4.25}$$

Methods 2 to 4 compensate for p_{C1} and/or Δp_d by controlling a small instantaneous active power in the IRPC. Thus, these methods cause an increased voltage ripples in v_{C1} or require an increased capacitance in C_1. Methods 1 to 3 p_{C1} and/or Δp_d result in an amount of voltage/current ripples across the load.

Note that the buck converter can be changed to other topologies depending on load requirements. Thus, method 1 is useful for the load accepting the ripples. For example, the output voltage v_C1 can be connected to a motor-drive inverter system which is expected to absorb the ripples in the inertia. On the other hand, method 4 might be suitable for the load, which requires a constant current and voltage, such as a battery charger system that can avoid the charging current ripples and the heat of a battery.

4.3 Experimental Results

The circuit configuration of the experimental setup has been already shown in Figure 3.3, and Table 3.1 showed the parameters of them. The proposed circuit was used to control the active power from the three-phase grid voltage to the dc load with the power rating 4.5 kW. Thus, the power factor was nearly 1.0. The proportional gains of the current controllers of the buck converter and the IRPC (k_O and k_C) were 6 A/V and 8 A/V, which were the critical value of each circuit. In the voltage controller of the IRPC, the dc voltage reference v^*_{C2} was set to 320 V with the proportional gain k_V and the integral time T_i of 0.2 W/V and 10 msec, respectively. The output power of this voltage controller p_{C2} was nearly zero. The damping conductance gain G_{d1} and G_{d2} was set to 0.5 S.

4.3.1 Effect of Commutation Overlap

Figure 4.8 shows the experimental results to demonstrate the overlap compensation. The dc voltage v_{C1} and reactive power q_1 were calculated in the control block by using (3.2) and (3.7) before start of the overlap compensation, which v_{C1} and q_1 were replaced to (3.10) and (3.22). In this experiment, method 1 was used and the load power was reduced to $P_O = 3$ kW because relatively large ringings were observed in the rectifier current i_1 and the grid current i_S before start. These ringings were induced by current error between i_{1u} and i_{2u}, because the overlap was not considered in the reference ${i_2}^*$ before start. In addition, the voltage reference ${v_{2u}}^*$ exceeded the dc voltage v_{C2} at the commutation in the rec-

tifier. After start, no saturation occurred in ${v_{2u}}^*$ and the ringings were effectively eliminated from i_{Su} and i_{1u}.

4.3.2 Effect of Damping Control

Figure 4.9 is the experimental results to confirm the damping control. In the control block, method 1 was used and the damping gain was changed from $G_{d1} = 0$ to 0.14 S at the starting of the damping control. The rectifier current i_{1u} was distorted due to the resonance between L_1 and C_1, and the resonant current also flowed out to the grid. After starting the damping control, the distortion was suppressed in i_{1u} and the grid current i_{Su} became sinusoidal.

4.3.3 Discussion Results of Control Method 1, 2 and 4

Figures 4.11-4.12 compare the experimental results of methods 1, 2, and 4. In these experiments, the load was adjusted at the rated power of 4.5 kW, and the damping gain was set to $G_d = 0.16$ S which is the gain to make the damping factor of $\zeta = 0.5$ in (4.12).

The grid current i_{Su} became sinusoidal in all three cases. As shown in Fig. 4.11, the dc capacitor voltage v_{C2} is almost constant in method 1, because the IRPC provided only reactive power. Method 2 had an increased voltage ripple of $\Delta v_{C2} = 16$ V, while it was $\Delta v_{C2} = 17$ V in method 4. Thus, compensation of Δp_d has a relatively small impact on v_{C2}.

On the other hand, method 1 had the largest output current ripple of $\Delta i_O = 2.7$ A. Method 4 can effectively reduce the ripple to $\Delta i_O = 0.5$ A, because both p_{C1} and Δp_d was compensated by the IRPC and then, the buck converter reference was maintained at a constant power of P_O. However, the THD was 3.8% in method 4, and method 2 achieved the smallest THD of 2.3%, which is slightly smaller than that in method 1.

Figure 4.13 depicts the experimental results when the damping powers were generated from both the buck converter and the IRPC, and the dc-link power p_{C1} was operated by the IRPC. The damping gains G_{d1} and G_{d2} were set to 0.25 Ω^{-1} which was a half of the previous experiment results. From this method, the voltage ripple of the dc voltage v_{C2} was able to be reduced because the buck

converter shared its power to maintain the stability of the system. The current ripple of the output current i_O was still less than 0.5 A with the THDi_u of 3.56%.

4.3.4 Efficiency

Figure 4.14 expresses the block diagram of the power losses of the components from the ac grid voltage source to the dc-link voltage between the conventional three-phase boost rectifier in Figure 4.14 (a) and the proposed circuit in Figure 4.14 (b) when the grid power p_S is varied from 0 W to 4.5 kW. The ac inductor L_1 and the dc-link capacitor C_1 of the three-phase boost was set to 800 μH and 1000 μF, respectively. And the parameters of the proposed circuit, which was controlled by the control method 2, can be show in Table I. The switching devices of the three-phase boost rectifier and the IRPC are MOSFETs by using the Si-based devices with the part number IXFB110N60P3, 600 V, 110 A. The real power losses measurement of the both systems can be shown in Figure 4.15 (a) and Figure 4.15 (b). It can be seen that the total power loss of the proposed circuit can be reduced by more than 80% of the conventional circuit.

Figure 4.15 (c) depicts the power losses in the MOSFETs (p_M) of the both circuits at the power rating 4.5 kW. The power losses in p_M consists of the conduction loss (p_{cond}) and the switching loss (p_{sw}). In the three-phase boost rectifier, because the main current flowed into the MOSFETs, the total power p_M was around 135.8 W which were 29.6 W of p_{cond} and 106.2 W of p_{sw}. In the proposed circuit, the current flowing into the MOSFETs of IRPC was 0.32 % of the grid current per phase, p_{cond} and p_{sw} could be significantly reduced to 2.7 W and 25.9 W, respectively. Therefore, the proposed circuit can be improved the efficiency higher around 2% than the conventional circuit of which the efficiency was 96% at 4.5 kW. The real measurement of the efficiency between the grid voltage source and the dc-link voltage of the both circuits can be shown in Figure 4.15 (d).

4.4 Summary

This chapter has proposed an ac/dc converter which consists of a three-phase diode rectifier equipped with an instantaneous reactive power compensator. The proposed circuit can eliminate bulky energy storage such as electrolytic capacitors. Moreover, as the ac current flowing into the IRPC is around 30% per phase, thus, it can reduce the switching loss and the power losses in ac inductors which the volume can be decreased around one-ninth when compared with the conventional three-phase boost rectifier. This paper also proposes the control techniques, such as the harmonic reduction techniques and the damping controller, to create sinusoidal grid currents and to maintain the stability of the system. A 4.5-kW experimental setup is used to verify the control performance and the efficiency. As a result, the proposed circuit can control the sinusoidal grid current waveform with the THD 2.27% and the efficiency 98.2% based on the silicon devices of the instantaneous reactive power compensator.

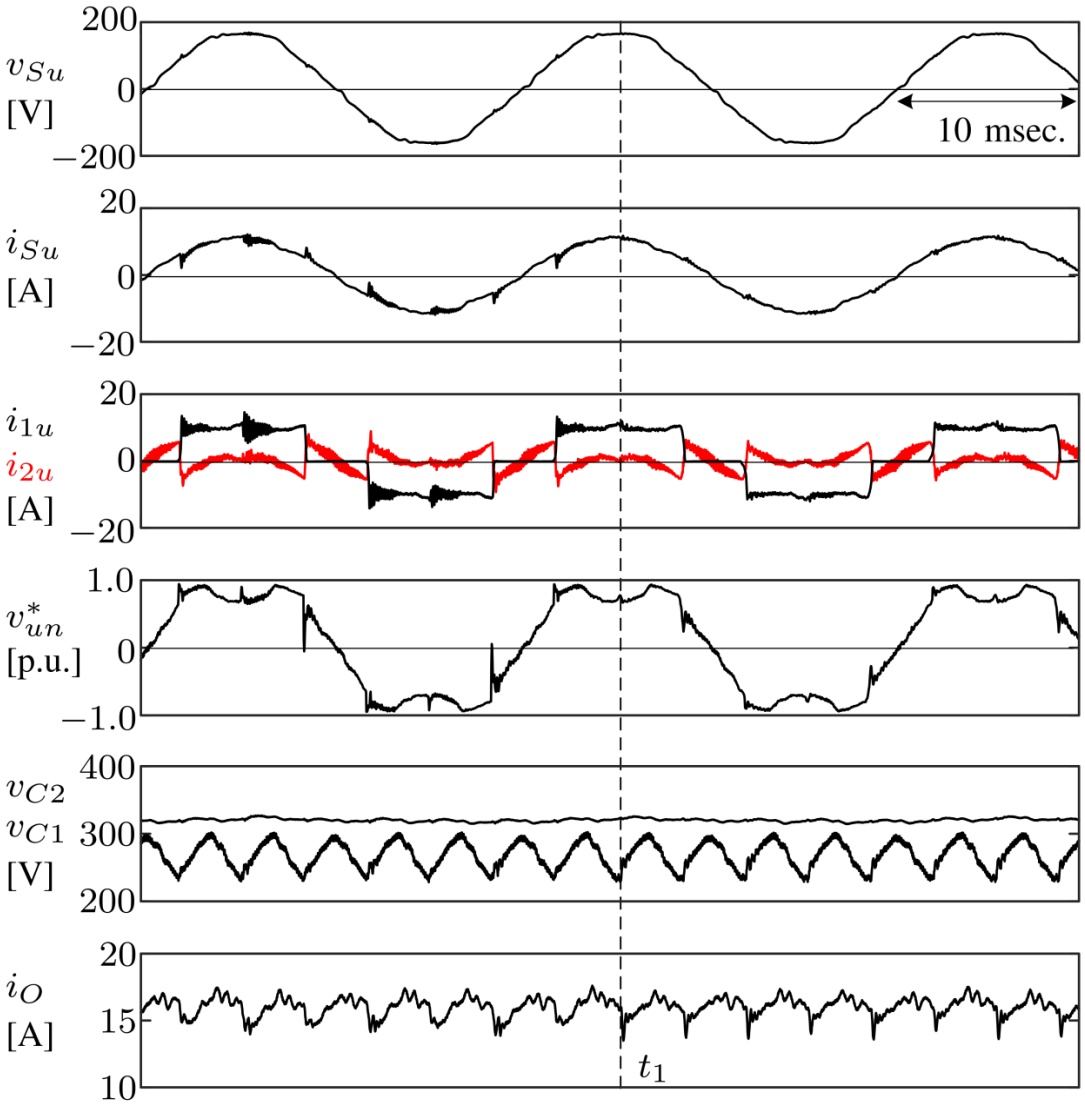

Figure 4.8: The effect of the proposed system controlled by the control method 2 at the power 3 kW when the commutation overlap was enable at t_1.

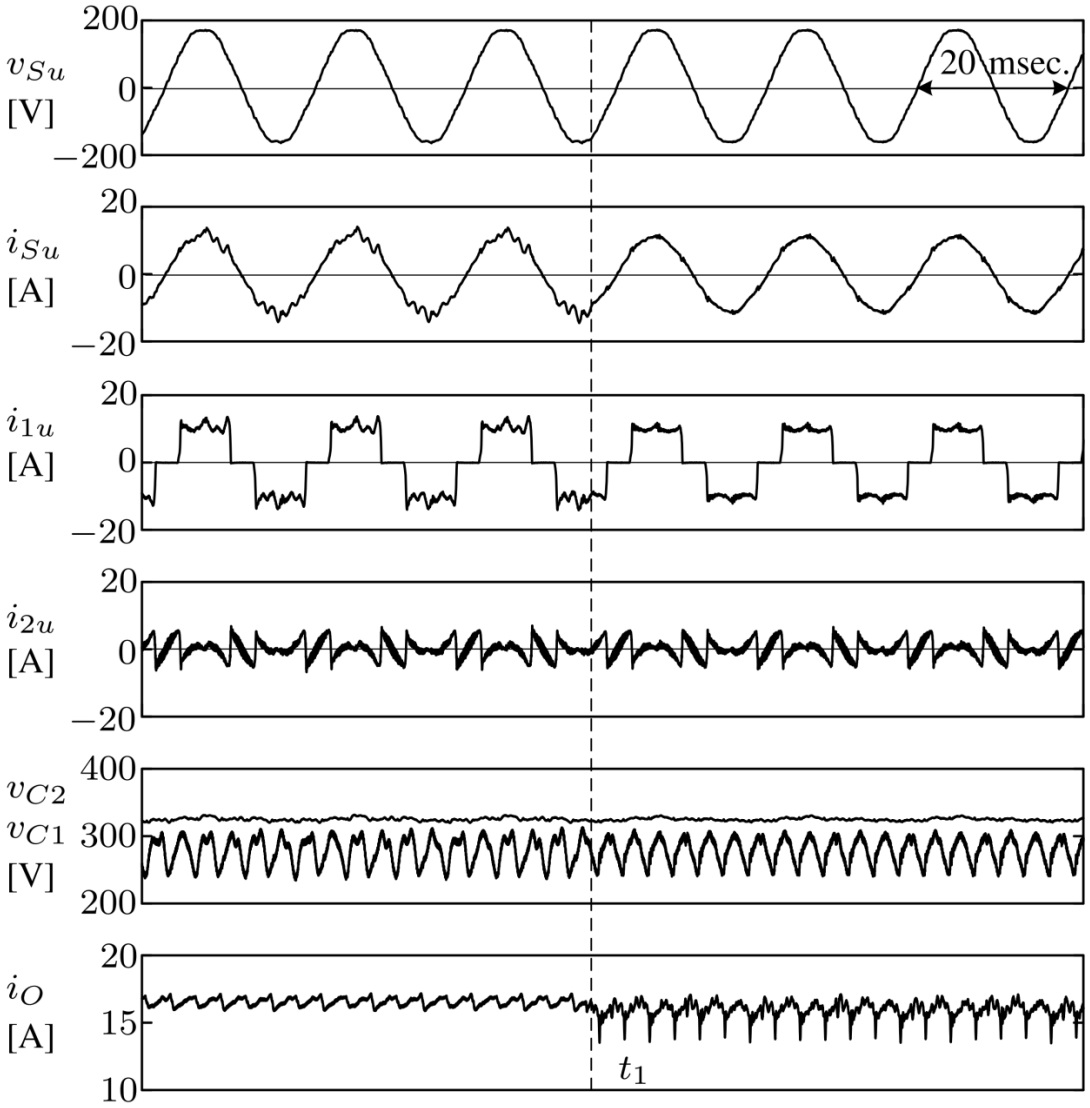

Figure 4.9: The operating damping control in the control method 2 at the power 3 kW when the damping control was enable at t_1.

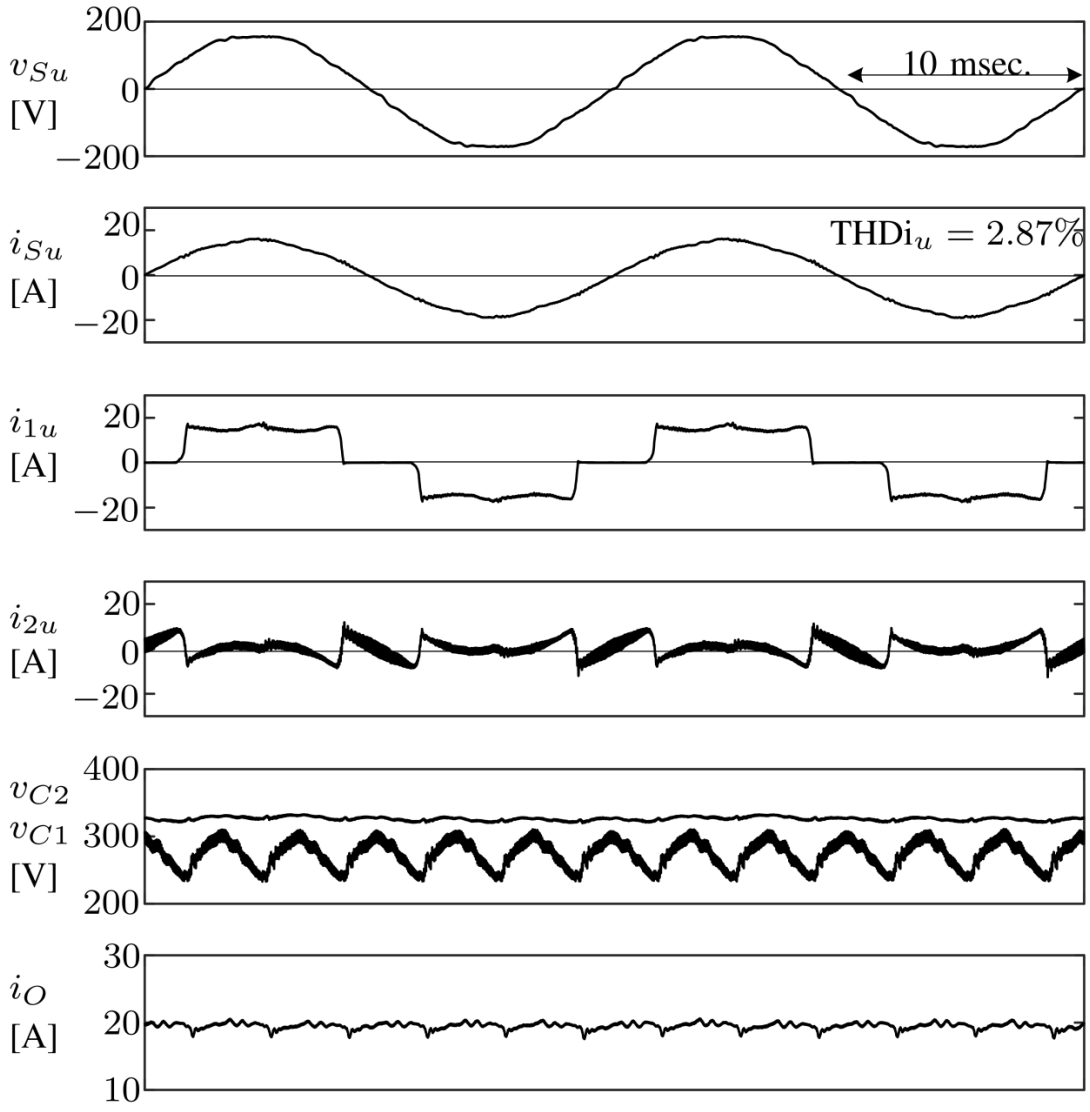

Figure 4.10: The experimental results of the control method 1.

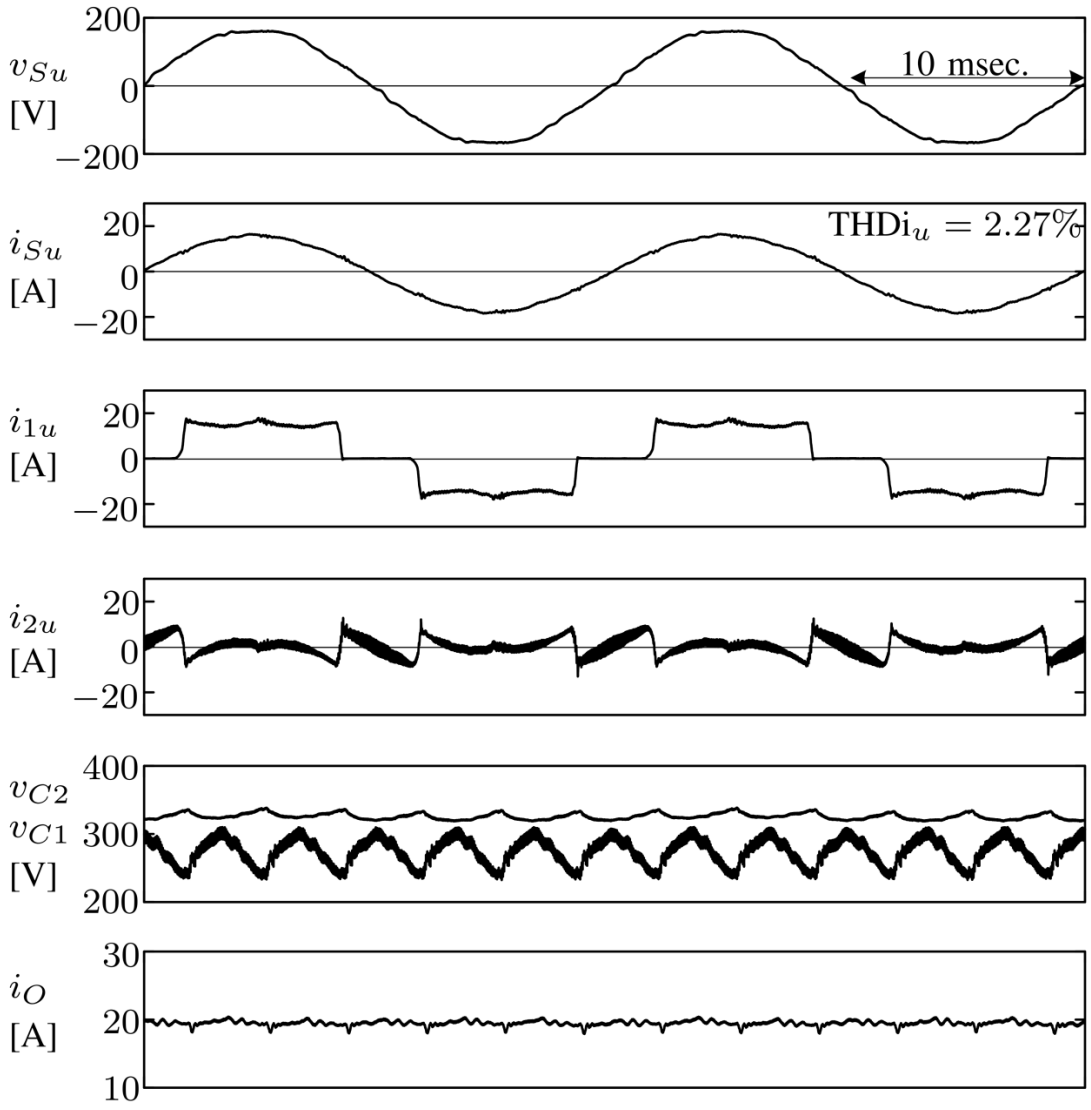

Figure 4.11: The experimental results of the control method 2.

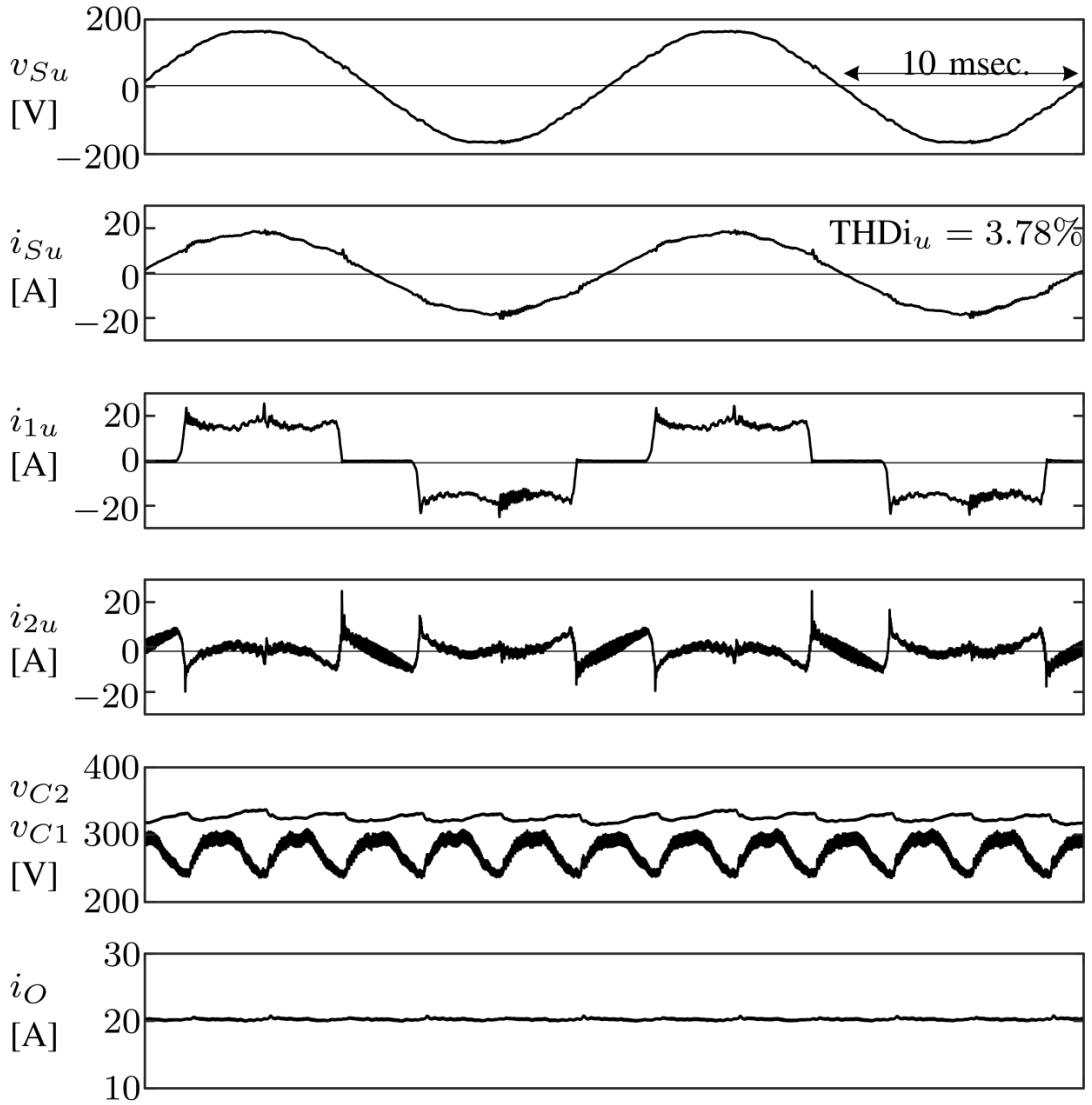

Figure 4.12: The experimental results of the control method 4.

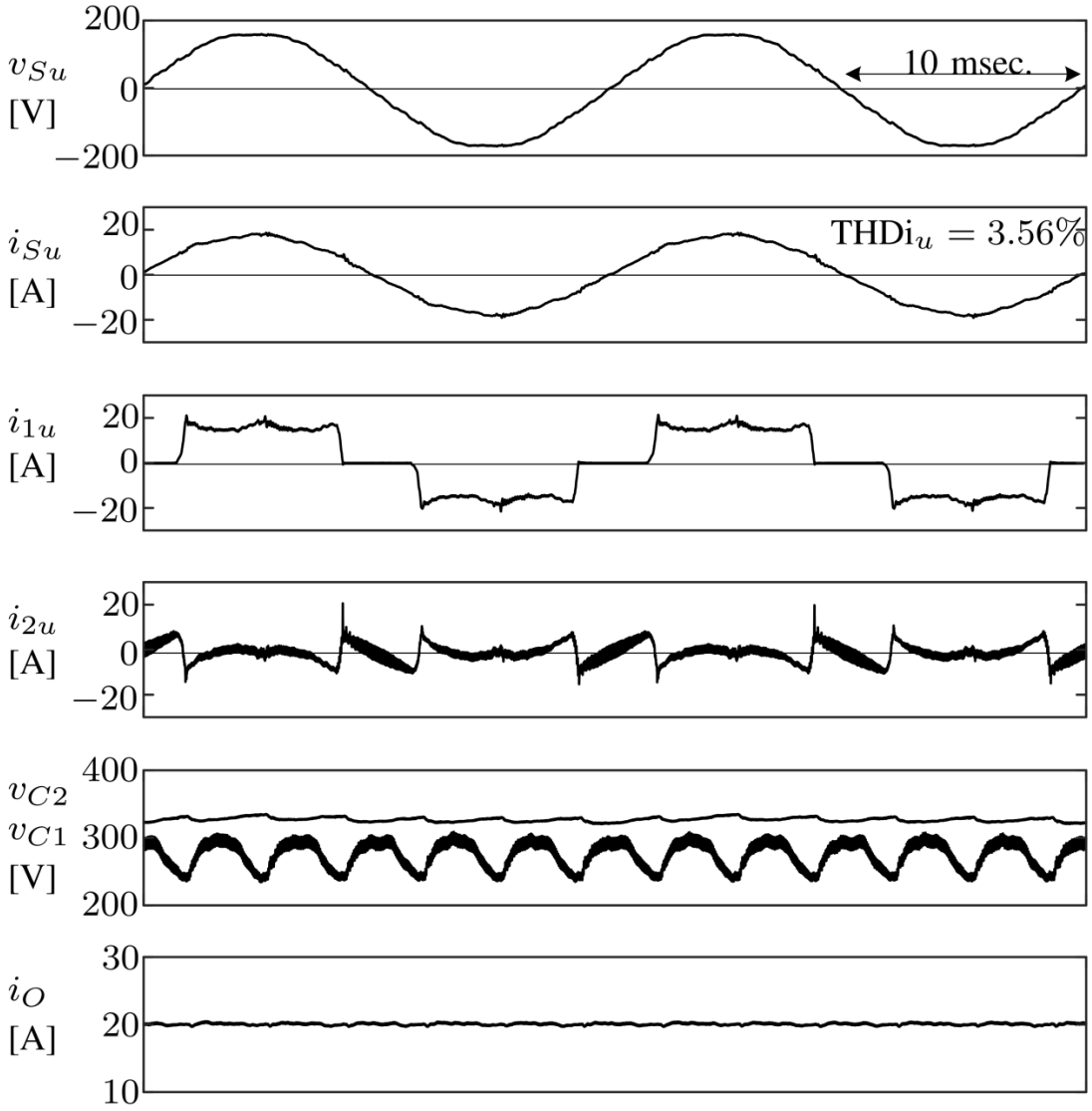

Figure 4.13: The experimental results when the damping control operated in both the buck converter and the IRPC with the damping gain G_{dc} and G_{d2} were set to 0.5 S..

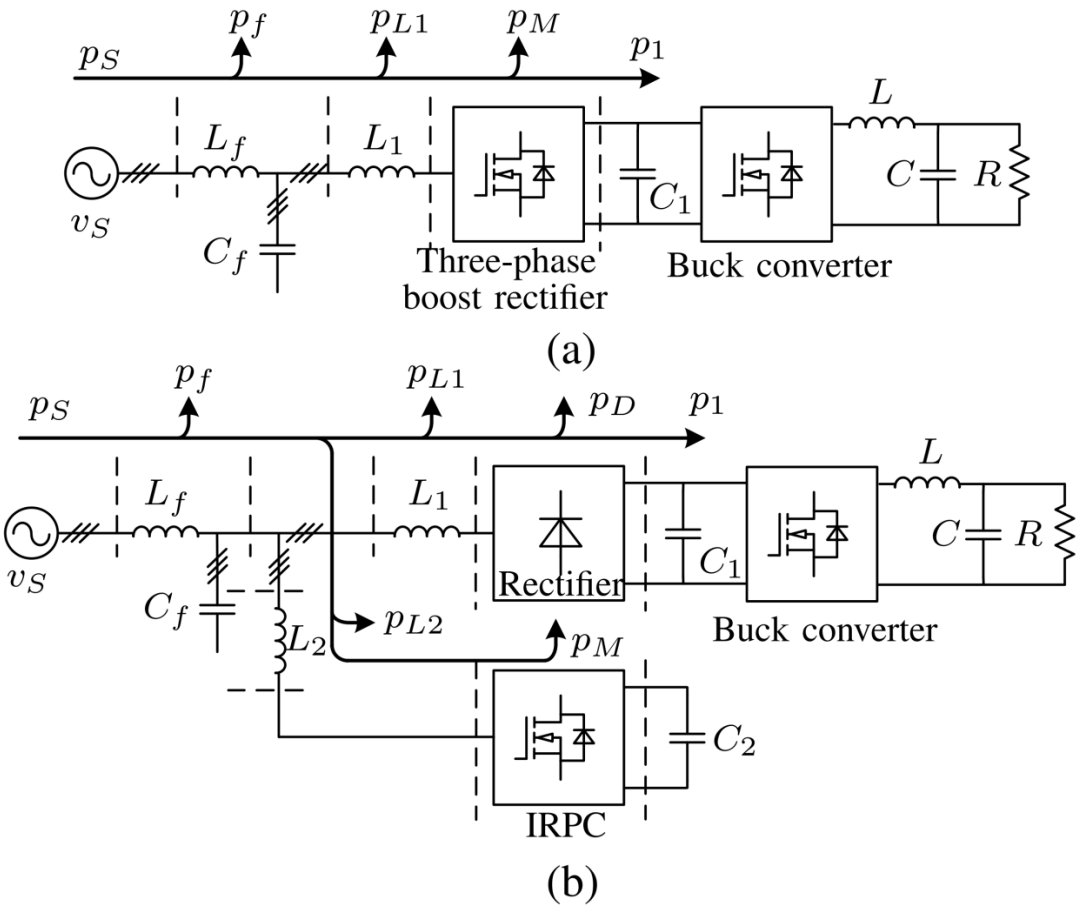

Figure 4.14: Power loss measurement block diagrams of (a) the three-phase boost rectifier, and (b) the proposed system.

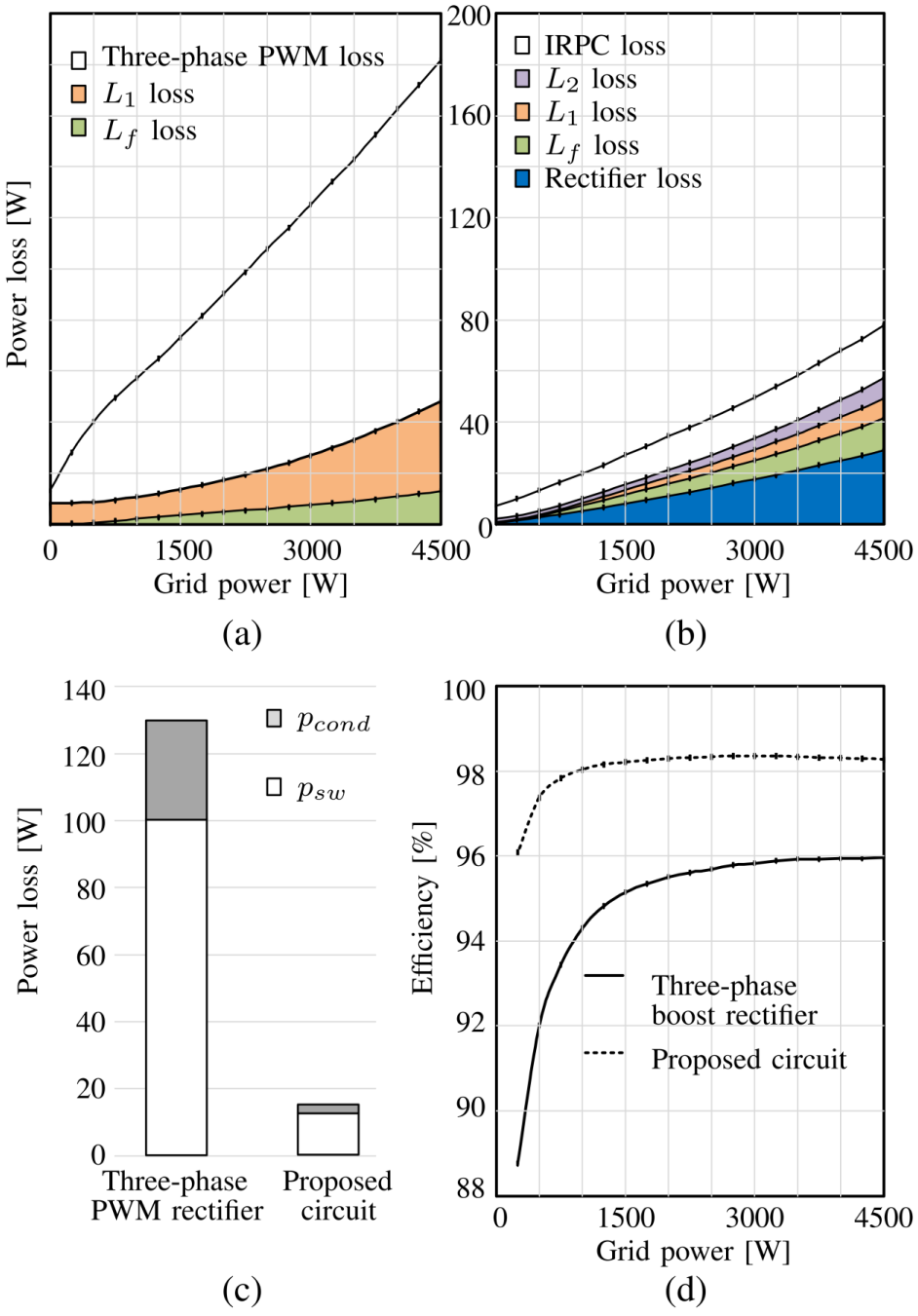

Figure 4.15: Power loss breakdowns of (a) the three-phase boost rectifier, (b) the proposed system. (c) The comparisons of the power in MOSFETs at 4.5 kW, and (d) the efficiency of the both system.

Chapter 5

Combination Zero-Voltage Switching and Discontinuous Pulse-Width Techniques for Three-Phase Didoe Rectifer with an Instantaneous Reactive Power Compensator

This chapter expresses the combination between the zero-voltage switching and discontinuous pulse-width modulation (DPWM) techniques for reducing the switching losses of the IRPC. These techniques, including the relationship of SV-PWM, CB-PWM, and DPWM, the designed ac inductance to achieve ZVS operation, the dead-time compensation for DPWM, are described in detail. The proposed method is verified by using the experimental setup of the three-phase rectifier with the IRPC comparing the power loss breakdowns between using the conventional PWM and the proposed technique for the IRPC circuit.

5.1 Discontinuous Pulse-Width Modulation and Zero-Voltage Switching Technique

5.1.1 Conventional and Discontinuous Pulse-Width Modulation

Figure 5.1 illustrates the basic space vector PWM for a three-phase inverter. Figure 5.1(a) shows the equivalent circuit of a three-phase inverter which creates the three-phase voltage at the ac terminal. The switch devices in the v-phase and w-phase are replaced by the equivalent switching device similar to the switching devices in the u-phase leg. When S_u is equal to 1 and 0, the terminal u connects to the positive and the negative bus of the dc-link voltage, respectively. The switching devices in other phases are the same operation as the switching devices of the u-phase.

Figure 5.1(b) depicts the switching state for the three-phase inverter, which has eight vectors to generate ac voltage to the ac terminal covering the sector n = 0 to 5. The zero vectors $\overrightarrow{V_0}$ and $\overrightarrow{V_7}$ can not generate the ac voltages to the ac terminals because all of the switching devices S_u, S_v, and S_w connect to the positive bus, and the negative bus of dc-link voltage.

Figure 5.1(c) illustrates the example of the switching signals S_u, S_v, and S_w in the sector 2 consisting of the 4-state switching vectors within the half switching frequency $\frac{t_{SW}}{2}$. The time T_0, T_1 and T_2 of the $\overrightarrow{V_0}$, $\overrightarrow{V_1}$, $\overrightarrow{V_2}$, and $\overrightarrow{V_7}$ calculated from the space-vector PWM as presented in [72]. In case of the conventional PWM, the time of $\overrightarrow{V_0}$ is equal to the time of $\overrightarrow{V_7}$. Thus, k_0 is equal to 0.5. During changing of the switching state, it is posible to produce the switching losses in the circuit.

The paper [81] has been proposed the modified PWM technique, which explained the relationship between the calculated times in the space-vector PWM to the voltage commands for comparing with triangular carrier based on microcontrollers and FPGAs. The voltage command v_x^* can be shown as follows:

$$v_x^* = v_x - (1 - 2k_0) - k_0 v_{max} - (1 - k_0) v_{min} \tag{5.1}$$

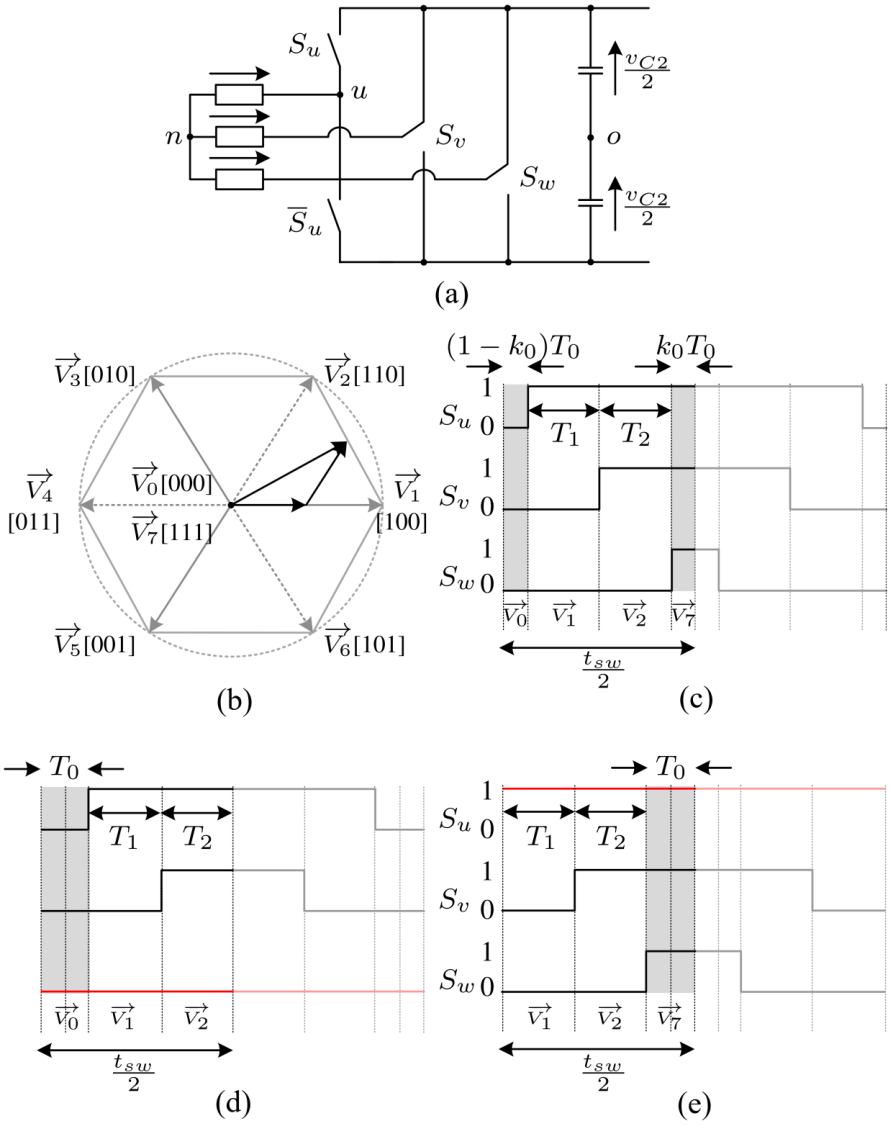

Figure 5.1: Principle of the three-phase PWM (a) the equivalent circuit, (b) the switching vectors, (c) the switching pattern of the conventional PWM $k_0 = 0.5$, (d) DPWM when $k_0 = 0$, (e) DPWM when $k_0 = 1$ during the state $n = 2$

when v_x is the voltages v_u, v_v, and v_w from the output of the current controller, and k_0 is 0.5 in case the conventional PWM. The voltages v_{max} and v_{min} can be shown as follows:

$$v_{max} = \begin{cases} v_w & \text{, when } 0 \leq \omega t < \frac{\pi}{6} \\ v_u & \text{, when } \frac{\pi}{6} \leq \omega t < \frac{5\pi}{6} \\ v_v & \text{, when } \frac{5\pi}{6} \leq \omega t < \frac{9\pi}{6} \\ v_w & \text{, when } \frac{9\pi}{6} \leq \omega t < 2\pi, \end{cases} \tag{5.2}$$

$$v_{min} = \begin{cases} v_v & \text{, when } 0 \leq \omega t < \frac{3\pi}{6} \\ v_w & \text{, when } \frac{3\pi}{6} \leq \omega t < \frac{7\pi}{6} \\ v_u & \text{, when } \frac{7\pi}{6} \leq \omega t < \frac{11\pi}{6} \\ v_v & \text{, when } \frac{11\pi}{6} \leq \omega t < 2\pi. \end{cases} \tag{5.3}$$

In case discontinuous PWM (DPWM), the switching losses of the switching devices can be reduced to one-third of the conventional PWM because one phase leg of the switching devices is not active of each sector n. Figure 5.1(d) and (e) show DPWM during the sector $n = 2$ when the time of the zero-vector is operated in $\overrightarrow{V_0}$ and $\overrightarrow{V_7}$ by adjusting $k_0 = 1$ and 0, whereas the other switching vectors $\overrightarrow{V_1}$ and $\overrightarrow{V_2}$ can be operated in the same time. There are many types of DPWM. The DPWM is designed to stop PWM at the peak of the current depending on its power factor because the circuit produces the highest switching losses from a conventional PWM rectifier. In the case of a conventional active power filter, DPWM is very difficult to use in this system because it is hard to predict the peak of compensating current. For the proposed circuit, the IRPC generates the reactive power to suppress the reactive power of the rectifier. The peak current does not vary like the conventional active power filter, and thus, the DPWM type 3 (DPWM3) is a suitable choice for the proposed IRPC. To generate DPWM3, k_0 is varied by

$$k_0 = \begin{cases} 1 & : 0 \leq \omega t < \frac{2\pi}{6}, \frac{4\pi}{6} \leq \omega t < \pi \\ & \text{, and } \frac{8\pi}{6} \leq \omega t < \frac{10\pi}{6} \\ 0 & : \frac{2\pi}{6} \leq \omega t < \frac{4\pi}{6}, \pi \leq \omega t < \frac{8\pi}{6} \\ & \text{, and } \frac{10\pi}{6} \leq \omega t < 2\pi. \end{cases} \tag{5.4}$$

The simulation results of DPWM3 can be shown in Figure 5.2. The voltage commands v_u, v_v, and v_w are transferred in the per unit before changing to the voltage commands v_u^*, v_v^*, and v_w^* by using (5.1) to (5.4). It can be seen that when the voltage commands reaches to 1 or -1, the PWM of the switching signal S_u^* is stopped at the peak current of the IRPC's current command i_{2u}^*. Thus, the switching loss of the switching device can be reduced more than 50% of the conventional PWM. However, the other areas still have the switch loss. To reduced the switching losses, the zero-voltage switching (ZVS) technique is used in this paper.

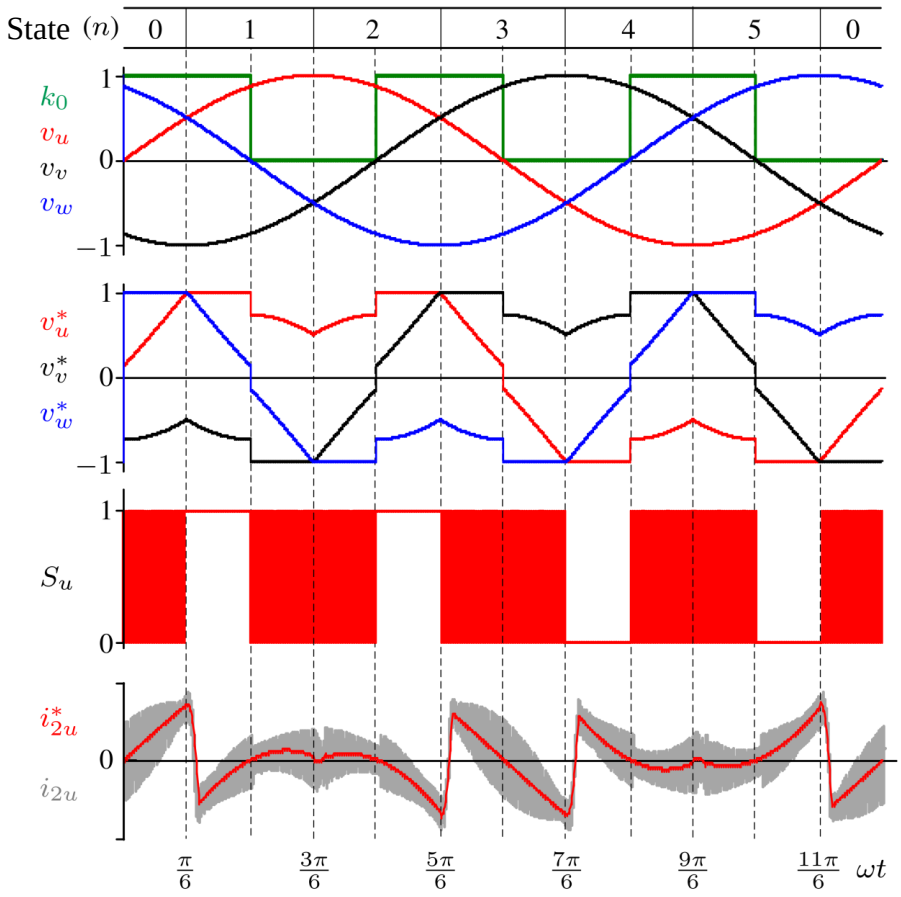

Figure 5.2: DPWM3 for the IRPC.

5.1.2 Zero-Voltage Switching Technique

When the current ripple is increased until opposite the polarity, the switching device can automatically achieve the ZVS operation as presented in the paper [13]. However, even though the turn-on loss is low, the on-stage is the main power loss for switching devices. Thus, this technique is unsuitable for high-power applications based on a PWM rectifier.

In the proposed circuit, the IRPC produces the peak current around 1/2 of the grid current. The current ripple of i_{2u} can be designed to start the ZVS operation at 1/2 of the IRPC current, which can limit the on-stage power losses for the switching devices, as well as the size of the inductor L_2 from the high peak current ripple.

Fig. 5.3 shows the simulation results of the switching signals in the u-phase of the IRPC circuit. The waveform is closed up during the state $n = 3$, where the IRPC is operating in the ZVS mode. Each waveform consists of the switching signals S_u, $\overline{S}_u$, the voltage across of each switch (v_u, $\overline{v}_u$), and the drain-to-source currents of the upper switch i_u and lower switch $\bar{i}_u$. The summation between i_u and $\bar{i}_u$ equals to the ac current i_{2u}.

Fig. 5.4 depicts the operating IRPC circuit during the turn-on transition of the switch $\overline{S}_u$. At $\omega t < t_A$, the initial status of the switch S_u and $\overline{S}_u$ are on and off, respectively, and the current i_{2u} is in a negative value. At the beginning of $t_A \leqslant \omega t < t_B$, the switch S_u is turned off. The drain-to-source currents i_u and $\bar{i}_u$, which are the half value of the current i_{2u}, charge and discharge the output capacitor of the upper and the lower switches. Then, the voltage of the lower switch $\overline{v}_u$ reduces to zero at t_B. After that, the diode of $\overline{S}_u$ contains the current at the beginning of $t_B \leqslant \omega t < t_C$. Thus, the switch $\overline{S}_u$ can be turned on in the ZVS condition at the end of the dead-time t_d.

Fig. 5.5 illustrates the turn-off transition of $\overline{S}_u$. At $\omega t < t_D$, the current i_{2u} is positive, and the switch $\overline{S}_u$ is turned off at the beginning of $t_D \leqslant \omega t < t_E$. After that, the large drain-to-source currents i_u and $\bar{i}_u$ rapidly discharge and charge the output capacitor of each switch to be 320 V and 0 V, respectively, and the freewheeling diode starts containing the ac current to the dc capacitor C_2 from t_E to t_F. At $\omega t = t_F$, the upper switch S_u can be turned on in the ZVS condition.

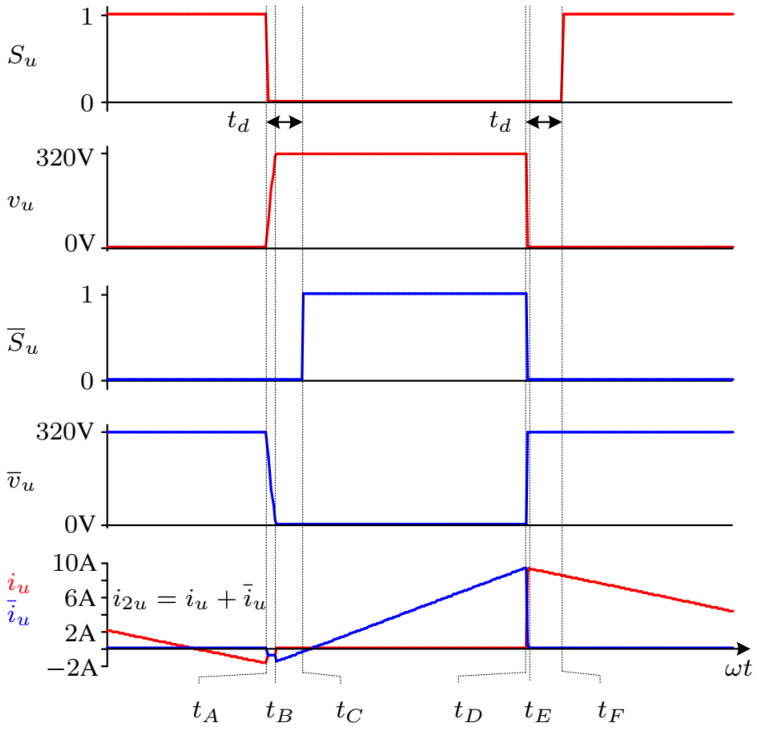

Figure 5.3: Simulation waveform of the switching signals in the u-phase leg of the IRPC during the ZVS operation ($\omega t \approx \frac{11\pi}{12}$).

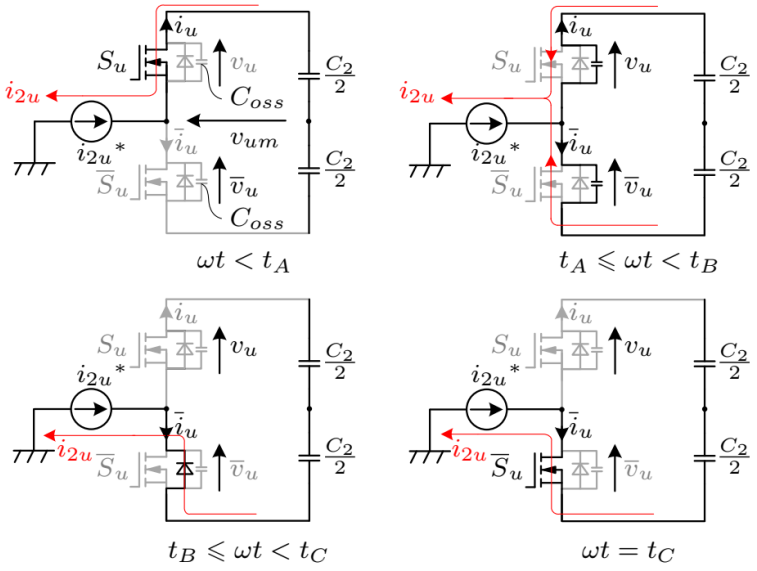

Figure 5.4: Operating IRPC circuit of the u-phase between t_A and t_C.

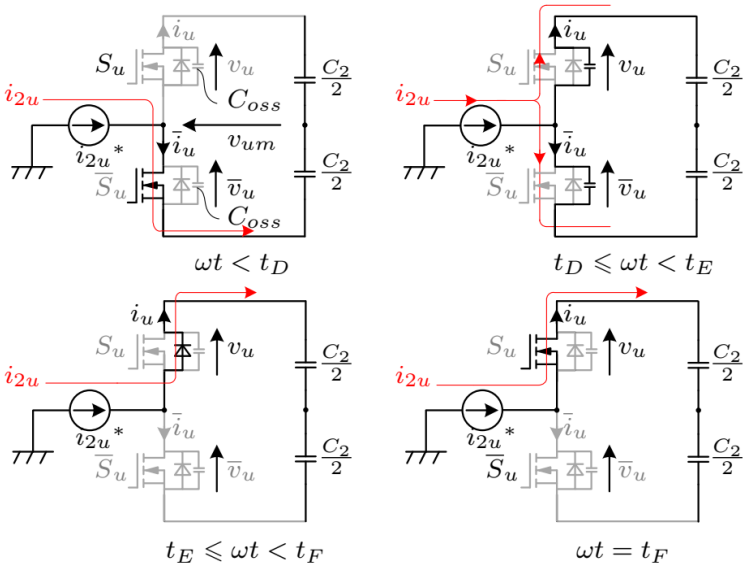

Figure 5.5: Operating IRPC circuit of the u-phase between t_A and t_C.

To completed ZVS operation regions, the current ripple has to be higher than two times of its average current. However, this method generate high rms current causing high conduction losses. In this thesis, the ac inductance of L_2 is designed to start the ZVS operation at $\omega t = \frac{11\pi}{12}$ or a half rating current in peak of i_{2u}^*. The relationship of the switching signals (S_u, S_v, S_w), the current i_{2u}, and the ac inductor voltage in u-phase (v_{L2u}) at $\omega t = \frac{11\pi}{12}$ can be shown in Figure 5.6. It can be seen that the current ripple of i_{2u} can be calculated during the turned-off duration (T_1) of the switch S_u. Thus the ac inductance of L_2 can be calculated by

$$\begin{aligned} L_2 &= \left| \frac{v_{Lu}}{\triangle i_{2u}} \right| T_1, \\ &= \left| \frac{v_{Su} - v_{un}}{\triangle i_{2u}} \right| \left(\frac{t_{sw}}{2}(1 - v_u^*) \right), \end{aligned} \tag{5.5}$$

when v_{un} is the line-to-neutral voltage at the ac terminal of the u-phase leg in the IRPC circuit. The ac terminal voltages of the IRPC of each phase can be

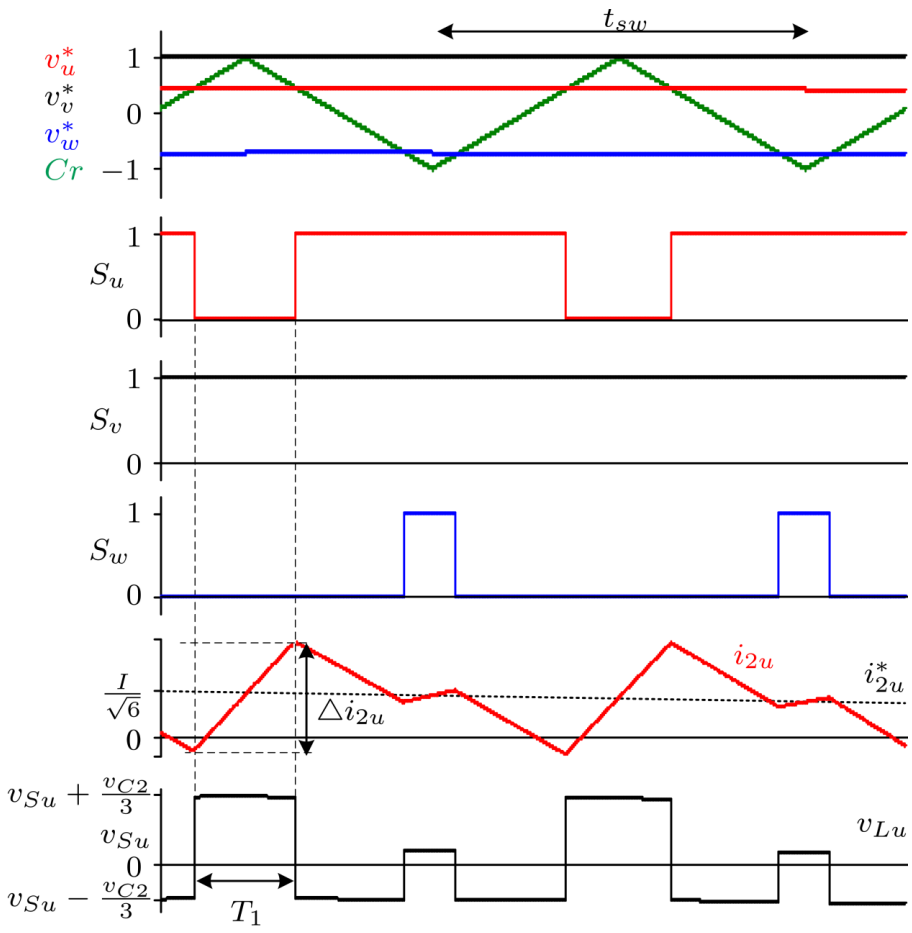

Figure 5.6: Ripple current of the IRPC when modulated by DPWM3 at $\omega t = \frac{11\pi}{12}$.

calculated by

$$\begin{cases} v_{un} = \frac{v_{C2}}{3}\left(2S_u - S_v - S_w\right), \\ v_{vn} = \frac{v_{C2}}{3}\left(2S_v - S_u - S_w\right), \\ v_{wn} = \frac{v_{C2}}{3}\left(2S_w - S_u - S_v\right). \end{cases} \tag{5.6}$$

The voltage command v_u^* is calculated from (5.1) when $k_0 = 1$, and the output voltages of the current controller is approximately equal to the grid voltages at $\omega t = \frac{11\pi}{12}$. Hence, The voltage command v_u^* can be estimated by

$$v_u^* = \frac{2v_{Su}}{v_{C2}^*} + 1 - \frac{2v_{Sv}}{v_{C2}^*}, \tag{5.7}$$

when v_{C2}^* is the dc voltage reference in the voltage controller of the IRPC.

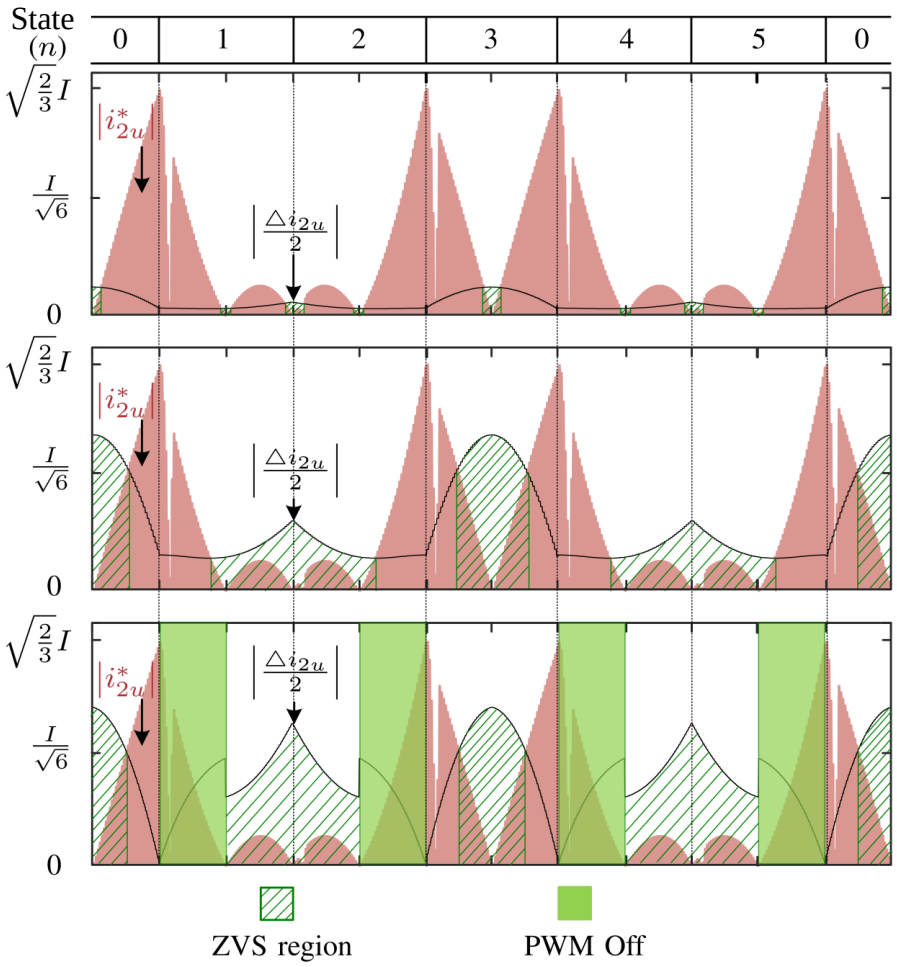

Figure 5.7: Comparison of the ripple current of IRPC in u-phase by using the conventional PWM with $L_2 = 800$ μH (top), the conventional PWM with $L_2 = 185$ μH (middle), and the DPWM3 with $L_2 = 185$ μH (below).

Figure 5.7 shows the 4.5-kW, 20-kHz simulation results of the proposed circuit consisting of the absolute value of the current references ($|i^*_{2u}|$) and a half current ripple ($\left|\frac{\triangle i_{2u}}{2}\right|$) of the u-phase when the IRPC is controlled by the conventional PWM with $L_2 = 800$ μH (top), and with $L_2 = 185$ μH (middle), and the DPWM3 with $L_2 = 185$ μH (below). The ZVS condition of this circuit is that a current ripple should be higher than the current reference ($\left|\frac{\triangle i_{2u}}{2}\right| > |i^*_{2u}| + I_{min}$), when

I_{min} calculated from

$$I_{min} = \frac{2C_{oss}v_{C2}}{t_d}, \tag{5.8}$$

In the top Figure 5.7, the small current ripple causes the small ZVS region. Because of this, the switching losses of the IRPC are high. To reduce the switching loss, the increase of the current ripple of the IRPC can extend the ZVS region as shown in the middle Figure 5.7. However, the large current ripple causes the increase of rms currents, which significantly increases the conduction losses of the circuit. Moreover, if the ac inductance of L_2 is reduced, the IRPC can not control the dc voltage. Hence, the middle figure of Figure 5.7 still has the switching losses in the IRPC circuit, especially at the peak of the IRPC's current. In the below figure, the DPWM3 can stop the PWM at the peak of the current i^*_{2u}. As a result, the switching loss in the MOSFETs can be reduced by more than 50% of the conventional PWM.

From the simulation in Fig. 5.3, when the current is around zero and the switch S_u is turned off, there is the delay time in the voltages v_u and $\overline{v}_u$ causing the voltage error at the ac terminal of the IRPC. As a result, the IRPC cannot ultimately generate the current to inject the harmonic current of the rectifier. For this reason, dead-time compensation is necessary to compensate the error voltage. Therefore, the next section will be the proposed dead-time compensation by estimating the current ripple of the IRPC based on DPWM3.

5.2 Dead-Time Compensation by Estimated Current Ripple of IRPC

The dead-time is very important for half-bridge and full-bridge converters to protect the short-circuit of each phase leg. However, the dead-time causes the converter voltage error, which affects the quality of the output voltages and currents, especially in high-switching frequency applications.

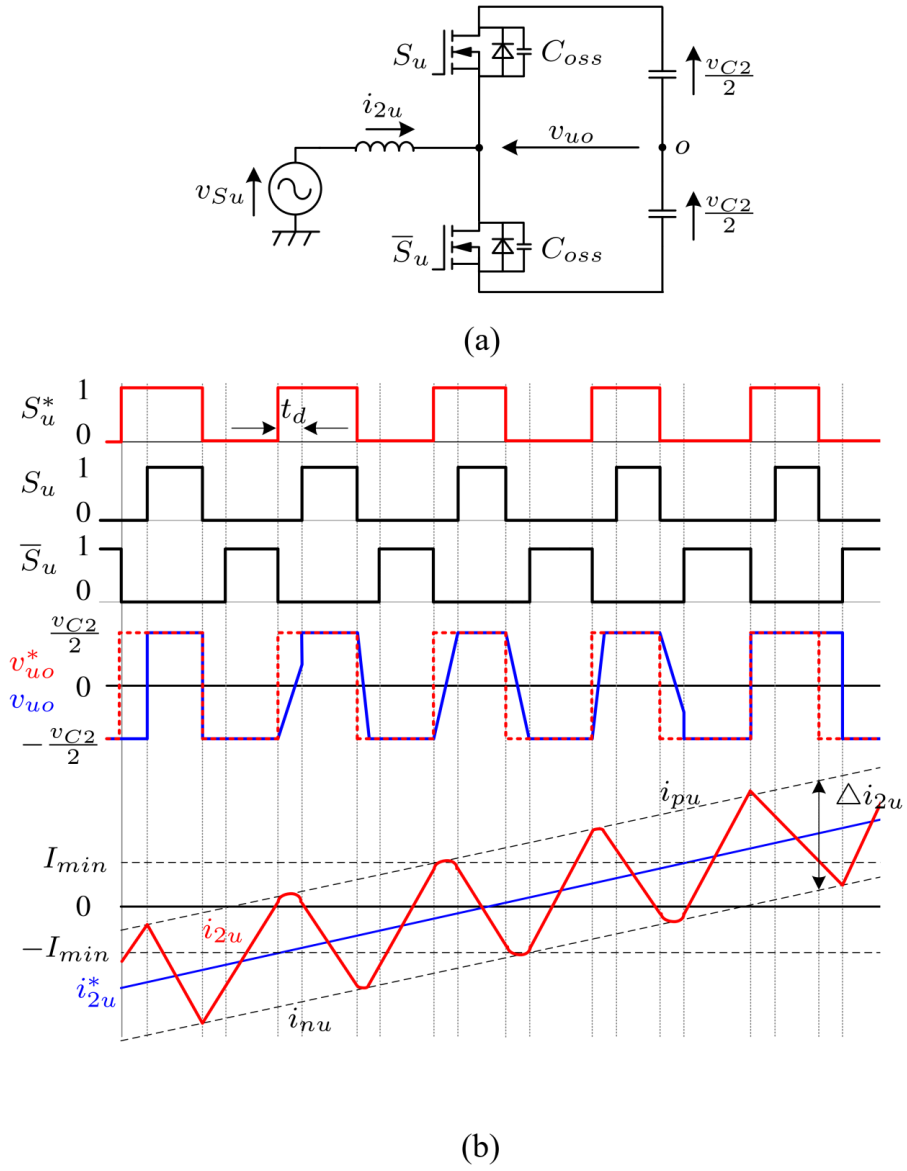

Figure 5.8: The voltage error caused by the dead-time in u-phase of (a) half-bridge converter, and (b) theoretical waveform of the circuit.

5.2.1 Voltage Error of IRPC Caused by Dead-Time

Fig. 5.8(a) depicts an example half-bridge converter circuit, which connects to the ac inductor and the ac grid voltage source in the u-phase. The switching devices, which are MOSFETs, have the output capacitance C_{oss} connected between the

drain-to-source terminals. Fig. 5.8(b) shows the theoretical waveform when the ac current i_{2u} is passing the zero-crossing according to its reference i_{2u}^*. The upper and lower ripple currents can be shown in i_{pu} and i_{nu}, respectively. The switching command reference S_u^*, which is the output signal after the voltage command compared with the triangular carrier to generate PWM, is delayed with the time t_d to create the dead-time for the upper and lower switching commands (S_u, $\overline{S}_u$). The switching commands S_u, $\overline{S}_u$ are used to control the switching devices of the half-bridge converter, which generate the ac voltage v_{uo}. Due to the dead-time t_d, the ac voltage v_{uo} is different from the ac voltage reference v_{uo}^*. It can be seen that there is the delay-time in the ac voltage v_{uo} depending on the ac current i_{2u} where each switching device is turned off. This causes the voltage error in v_{uo}. From this voltage error, the converter cannot control the ac current following its reference causing the distortion in the grid currents. Paper [80] has been proposed the calculated average voltage error from the dead-time which relates with the dc voltage v_{C2}, the minimum current I_{min}, and the current ripples i_{pu}, i_{nu} during the dead-time t_d.

When the lower switching command $\overline{S}_u$ is turned-off at the upper ripple current $i_{pu} < 0$, the current still flows though its diode. The ac voltage v_{uo} is equal to $-\frac{v_{C2}}{2}$ during the dead time. The average voltage error can be shown by

$$v_{erpu} = \frac{v_{C2} t_d}{t_{SW}}. \tag{5.9}$$

In the case of $I_{min} \geq i_{pu} \geq 0$, when the switch $\overline{S}_u$ is turned off, there is a current flowing to discharge the voltage across C_{oss} of the upper switch. However, the voltage across the upper switch cannot completely discharged until the switch $\overline{S}_u$ is turned off at $i_{pu} = I_{min}$. The average voltage error during the dead-time t_d can be calculated by

$$v_{erpu} = \frac{v_{C2} t_d}{t_{SW}} \left(1 - \frac{i_{pu}}{2I_{min}}\right). \tag{5.10}$$

When the switch $\overline{S}_u$ is turned off after $i_{pu} > I_{min}$, the voltage across the upper switch is discharged to zero until the freewheeling diode can contain the current during the dead-time. Moreover, if the current i_{pu} is remarkably higher than I_{min}, the ac voltage v_{uo} will be immediately increased to $\frac{v_{C2}}{2}$, and the voltage error will

reduce to zero. It can be seen that the rising edge of the ac voltage v_{uo} is similar to its voltage reference v_{uo}^{*}. The average error voltage can be expressed by

$$v_{erpu} = \frac{v_{C2} t_d}{t_{SW}} \frac{I_{min}}{i_{pu}}. \tag{5.11}$$

On the other hand, the average voltage error caused by the lower current ripple i_{nu} is similar to the analysis of the upper current ripple i_{pu}. However, this average voltage error has a negative value because the ac voltage v_{uo} is higher than the ac voltage reference v_{uo}^{*}.

Thus, the equations (5.12) and (5.13) can be used to sum up the average voltage error caused by the upper and lower current ripple, respectively.

$$v_{erpu} = \begin{cases} \frac{v_{C2} t_d}{t_{SW}} & : (i_{pu} < 0) \\ \frac{v_{C2} t_d}{t_{SW}} \left(1 - \frac{i_{pu}}{2I_{min}}\right) & : (I_{min} \geq i_{pu} \geq 0) \\ \frac{v_{C2} t_d}{t_{SW}} \frac{I_{min}}{i_{pu}} & : (i_{pu} > I_{min}). \end{cases} \tag{5.12}$$

$$v_{ernu} = \begin{cases} -\frac{v_{C2} t_d}{t_{SW}} & : (i_{nu} < 0) \\ -\frac{v_{C2} t_d}{t_{SW}} \left(1 - \frac{i_{nu}}{2I_{min}}\right) & : (0 \geq i_{nu} \geq -I_{min}) \\ \frac{v_{C2} t_d}{t_{SW}} \frac{I_{min}}{i_{nu}} & : (i_{nu} < -I_{min}). \end{cases} \tag{5.13}$$

The total error voltage can be calculated by

$$v_{uDT} = v_{erpu} + v_{ernu}. \tag{5.14}$$

This voltage is used to compensate the voltage error by adding in the voltage command as depicted by

$$v_u^{**} = v_u^{*} + \frac{2 v_{uDT}}{v_{C2}} = v_u^{*} + v_{eru}, \tag{5.15}$$

when v_u^{**} is the new voltage reference in u-phase for comparing with the triangular carrier C_r. However, this method needs to know the ripple currents of each phase.

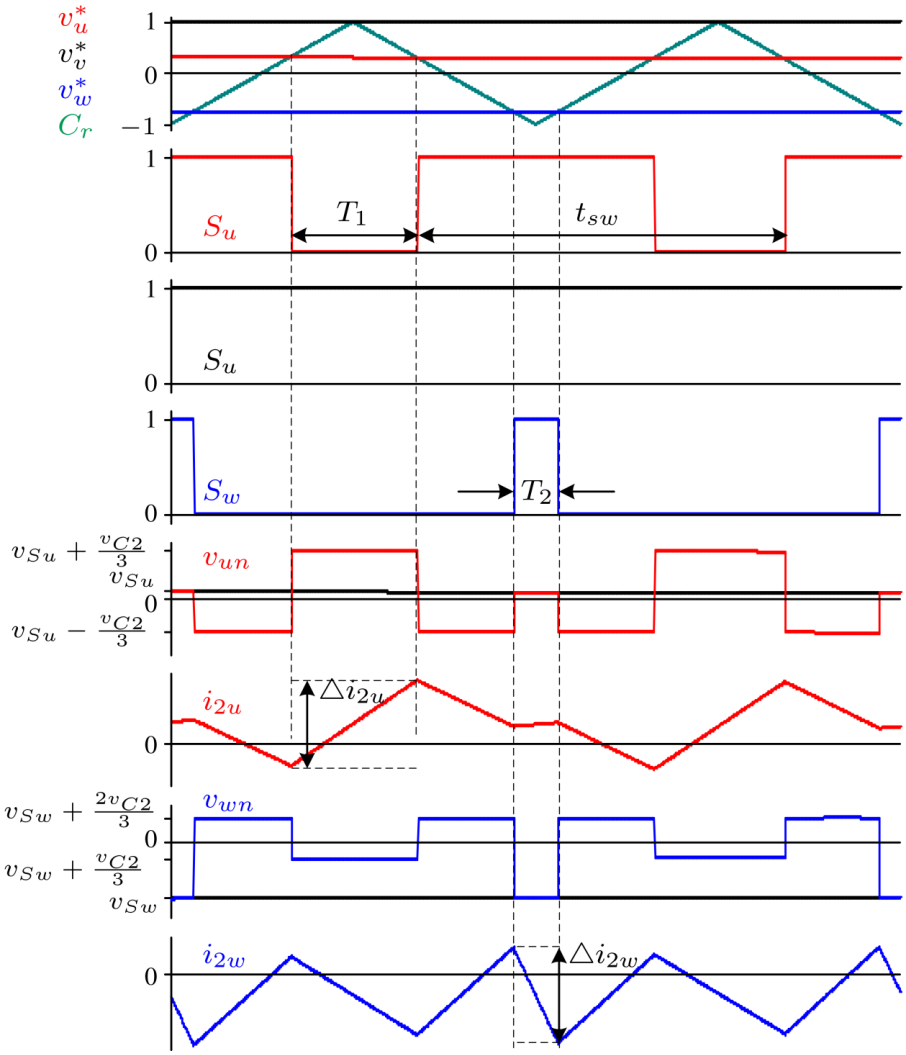

Figure 5.9: The relationship between the switching commands (S_u, S_v, S_w), the voltage drops of ac inductors (v_{Lu} and v_{Lw}) and the ripple currents of u-phase and w-phase during the sector 3 when $k_1 = 0$.

5.2.2 Current Ripple Estimation of DPWM3

Figure 5.9 shows the simulation waveform of the IRPC circuit when controlled by DPWM3 at the sector $n = 3$ and $k_0 = 1$. At this time, the switching device of the v-phase is clamped to the positive dc voltage because the voltage reference v_v^* is equal to 1. Hence, the voltage error of the v-phase can be neglected, and it

does not need to find the current ripple. The peak current of the u-phase can be calculated during the turned-off duration of S_u in the switching state $[S_u S_v S_w] = [010]$, which the ac terminal voltage of the u-phase can be obtained by (5.6) with the time T_1. The relationship between the voltage command v_u^* and the time T_1 can be expressed by

$$\begin{aligned} T_1 &= t_{sw} - \left(\frac{t_{sw}}{2}(1+v_u^*)\right), \\ &= \frac{t_{sw}}{2}(1-v_u^*). \end{aligned} \tag{5.16}$$

From the calculated ac inductance in (5.5), the current ripple of the u-phase can be obtained by

$$\triangle i_{2u} = \left|\frac{v_{Su} + \frac{v_{C2}^*}{3}}{L_2}\right| \left(\frac{t_{sw}}{2}(1-v_u^*)\right). \tag{5.17}$$

Moving onto the current ripple in the w-phase, the peak current is in during $[S_u S_v S_w] = [111]$ or the zero-vector. This peak current is operated in the turned-on transition of the switch S_w. The relationship between the turned-on time T_2 and the voltage command v_w^* can be found as follows:

$$T_2 = \frac{t_{sw}}{2}(1+v_w^*). \tag{5.18}$$

Hence, the current ripple in the w-phase can be shown by

$$\begin{aligned} \triangle i_{2w} &= \left|\frac{v_{Lw}}{L_2}\right| T_2, \\ &= \left|\frac{v_{Sw} - v_{wn}}{\triangle i_{2w}}\right| T_2, \\ &= \left|\frac{v_{Sw}}{L_2}\right| \left(\frac{t_{sw}}{2}(1+v_w^*)\right). \end{aligned} \tag{5.19}$$

The current ripples can be calculated in a similar pattern of each sector which needs to know the voltage vector and the duration of the peak currents. The DPWM3 has a 12-voltage sector. The switching device is clamped to the positive and the negative dc voltage when voltage reference saturates at 1 and -1, respectively. Thus, the voltage error and current ripple in that phase do not need to

Table 5.1: Summary ac current ripples of the IRPC when modulated by DPWM3

Sector n (k_0)	$\triangle i_{2u}$	$\triangle i_{2v}$	$\triangle i_{2w}$
1 ($k_0 = 1$)	–	$\frac{v_{Sv}}{L_2}$ $\frac{t_{sw}}{2}(1 + v_v^*)$	$\frac{v_{Sw}+\frac{v_{C2}}{3}}{L_2}$ $\frac{t_{sw}}{2}(1 - v_w^*)$
1 ($k_0 = 0$)	$\frac{v_{Su}}{L_2}$ $\frac{t_{sw}}{2}(1 - v_u^*)$	–	$\frac{v_{Sw}-\frac{v_{C2}}{3}}{L_2}$ $\frac{t_{sw}}{2}(1 + v_w^*)$
2 ($k_0 = 0$)	$\frac{v_{Su}}{L_2}$ $\frac{t_{sw}}{2}(1 - v_u^*)$	$\frac{v_{Sv}-\frac{v_{C2}}{3}}{L_2}$ $\frac{t_{sw}}{2}(1 + v_v^*)$	–
2 ($k_0 = 1$)	–	$\frac{v_{Sv}+\frac{v_{C2}}{3}}{L_2}$ $\frac{t_{sw}}{2}(1 - v_v^*)$	$\frac{v_{Sw}}{L_2}$ $\frac{t_{sw}}{2}(1 + v_w^*)$
3 ($k_0 = 1$)	$\frac{v_{Su}+\frac{v_{C2}}{3}}{L_2}$ $\frac{t_{sw}}{2}(1 - v_u^*)$	–	$\frac{v_{Sw}}{L_2}$ $\frac{t_{sw}}{2}(1 + v_w^*)$
3 ($k_0 = 0$)	$\frac{v_{Su}-\frac{v_{C2}}{3}}{L_2}$ $\frac{t_{sw}}{2}(1 + v_u^*)$	$\frac{v_{Sv}}{L_2}$ $\frac{t_{sw}}{2}(1 - v_v^*)$	–
4 ($k_0 = 0$)	–	$\frac{v_{Sv}}{L_2}$ $\frac{t_{sw}}{2}(1 - v_v^*)$	$\frac{v_{Sw}-\frac{v_{C2}}{3}}{L_2}$ $\frac{t_{sw}}{2}(1 + v_w^*)$
4 ($k_0 = 1$)	$\frac{v_{Su}}{L_2}$ $\frac{t_{sw}}{2}(1 + v_u^*)$	–	$\frac{v_{Sw}+\frac{v_{C2}}{3}}{L_2}$ $\frac{t_{sw}}{2}(1 - v_w^*)$
5 ($k_0 = 1$)	$\frac{v_{Su}}{L_2}$ $\frac{t_{sw}}{2}(1 + v_u^*)$	$\frac{v_{Sv}+\frac{v_{C2}}{3}}{L_2}$ $\frac{t_{sw}}{2}(1 - v_v^*)$	–
5 ($k_0 = 0$)	–	$\frac{v_{Sv}-\frac{v_{C2}}{3}}{L_2}$ $\frac{t_{sw}}{2}(1 + v_v^*)$	$\frac{v_{Sw}}{L_2}$ $\frac{t_{sw}}{2}(1 - v_w^*)$
0 ($k_0 = 0$)	$\frac{v_{Su}-\frac{v_{C2}}{3}}{L_2}$ $\frac{t_{sw}}{2}(1 + v_u^*)$	–	$\frac{v_{Sw}}{L_2}$ $\frac{t_{sw}}{2}(1 - v_w^*)$
0 ($k_0 = 1$)	$\frac{v_{Su}+\frac{v_{C2}}{3}}{L_2}$ $\frac{t_{sw}}{2}(1 - v_u^*)$	$\frac{v_{Sv}}{L_2}$ $\frac{t_{sw}}{2}(1 + v_v^*)$	–

be calculated. Table 5.1 summaries the current ripples of the 12-voltage sector. From the current ripples, the estimated upper and lower current ripple i_{px} and i_{nx} of each phase can be calculated by

$$\begin{bmatrix} i_{2u}^* \\ i_{2v}^* \\ i_{2w}^* \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} \sin(\omega t) & \cos(\omega t) \\ \sin\left(\omega t - \frac{2\pi}{3}\right) & \cos\left(\omega t - \frac{2\pi}{3}\right) \\ \sin\left(\omega t + \frac{2\pi}{3}\right) & \cos\left(\omega t + \frac{2\pi}{3}\right) \end{bmatrix} \begin{bmatrix} i_{2d}^* \\ i_{2q}^* \end{bmatrix}, \tag{5.20}$$

$$\begin{cases} i_{px} & = i_{2x}^* + \frac{\triangle i_{2x}}{2}, \\ i_{nx} & = i_{2x}^* - \frac{\triangle i_{2x}}{2}, \end{cases} \tag{5.21}$$

when x is u-, v-, and w-phase. These current ripples are used to find the dead-time compensation from the equations(5.12) to (5.15).

Table 5.2: All parameters of the proposed system when IRPC controlled by the conventional PWM and DPWM3

Parameters		Value
Line-to-line grid voltages / grid frequency	V / f_S	200 V / 50 Hz
Inductance of ac filter inductor	L_f	300 μH
Capacitance of ac filter capacitor	C_f	6 μF
Inductance of rectifier inductor	L_1	80 μH
AC inductance of IRPC when IRPC modulated by conventional PWM IRPC modulated by DPWM3	L_2	 800 μH 185 μH
Capacitance of dc-link capacitor	C_1	14 μF
Capacitance of compensator capacitor	C_2	28 μF
Inductance of buck inductor	L	800 μH
Capacitance of buck capacitor	C	14 μF
Resistance of DC load resistor	R	10.5 Ω
Switching frequency	f_{sw}	20 kHz
Output power	P_{dc}	4.5 kW

5.3 Experimental Verification

Figure 3.3 shows the proposed circuit configuration for the experimental setup in the laboratory, which was operated at the rating power 4.5 kW by using the parameters in Table 5.2. The control block diagrams as shown in Figure 5.10 was used to control the IRPC and the buck converter. The constant load power, the damping control, and the dc-link power compensation were operated by the dc/dc converter, whereas the IRPC was used to generate the harmonic currents by using the q-axis current to eliminate the harmonic current of the rectifier. The operating waveform, power losses of each component, the EMIs of the conventional three-phase boost rectifier, and the proposed circuit of each control technique were compared and discussed in this paper.

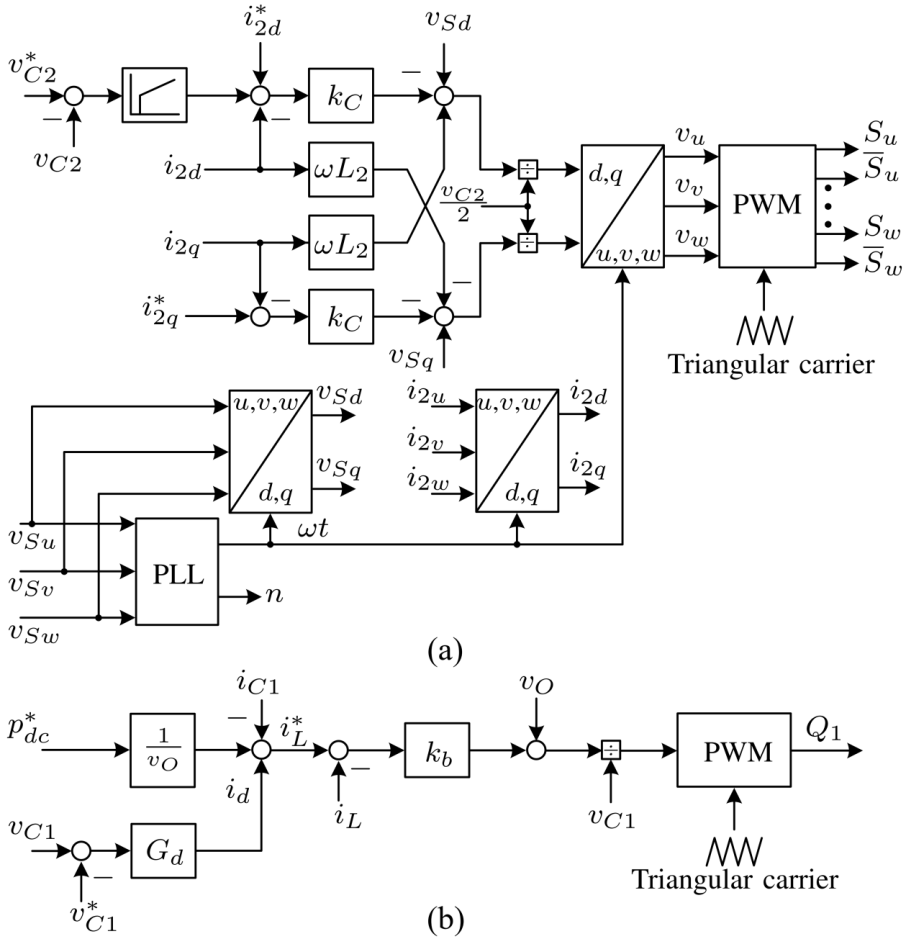

Figure 5.10: Control block diagrams of (a) the IRPC, and (b) the buck converter.

5.3.1 Dead-time Compensation of DPWM3

In the control block diagram of Figure 5.10, the output voltages (v_u, v_v, v_w) of the current current controller flowed into the PWM block to find the voltage references (v^*_u, v^*_v, v^*_w) by substituting the equations from (5.2) to (5.4) into (5.1). These voltage references were compared with the triangular carrier to generate the switching references S^*_u, S^*_v, and S^*_w. After that, the dead-time of the IRPC was set to 2 μsec to provide switching signals S_u, $\overline{S}_u$, S_v, $\overline{S}_v$, S_w, and $\overline{S}_w$ for the gate driver of the IRPC. Due to the dead-time, there are error voltages at the ac voltage of the IRPC. This causes the distortion in the ac currents of the

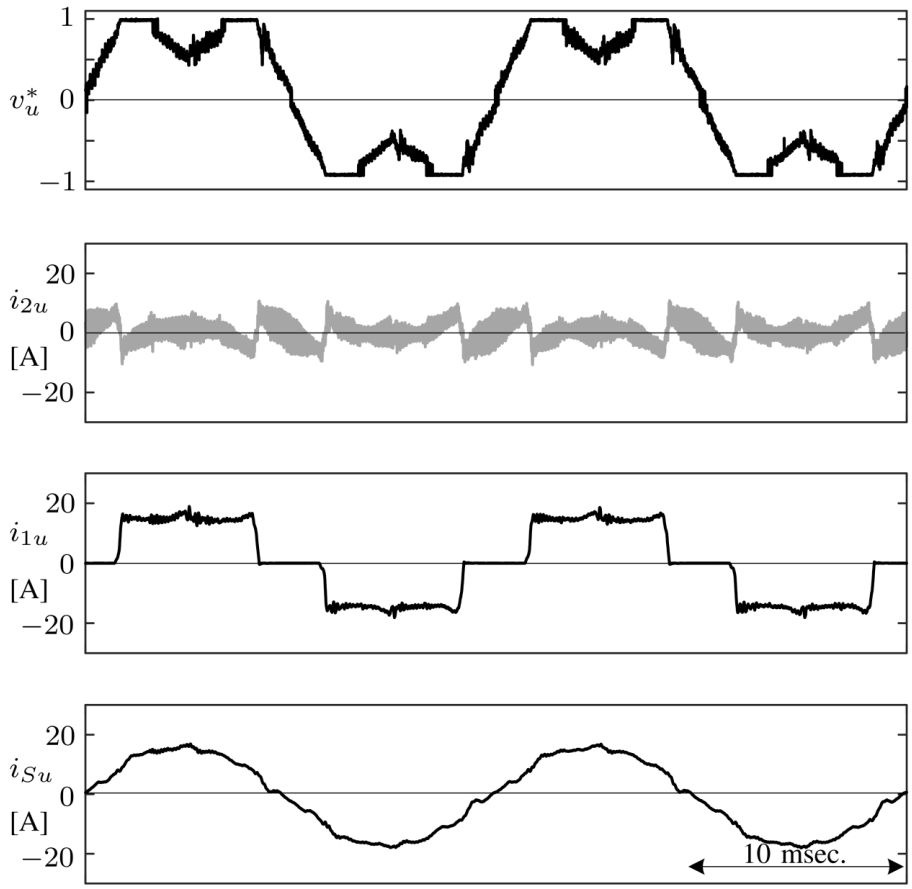

Figure 5.11: The experimental results of the proposed circuit when the IRPC modulated by DPWM3 and using the ac inductance of $L_2 = 185\mu$H without considering the dead-time compensation.

IRPC as shown the waveform of u-phase in Figure 5.11. This waveform consists of the voltage reference v_u^*, the ac current of the IRPC i_{2u}, the ac current of the rectifier i_{1u}, and the grid current i_{Su} of the u-phase. The voltage reference v_u^* was measured by the digital-to-analog of the control system and scaling to very between 1 and -1. It can be seen that the IRPC could not correctly generate the harmonic current of i_{2u} to cancel the harmonic current of the rectifier i_{1u}, which distorts the grid current i_{Su}. The total harmonic of i_{Su} was 6.55%.

Figure 5.12 illustrates the dead-time compensation by estimating the current ripple of the IRPC as shown in Table 5.1. The estimated current ripples of the u-

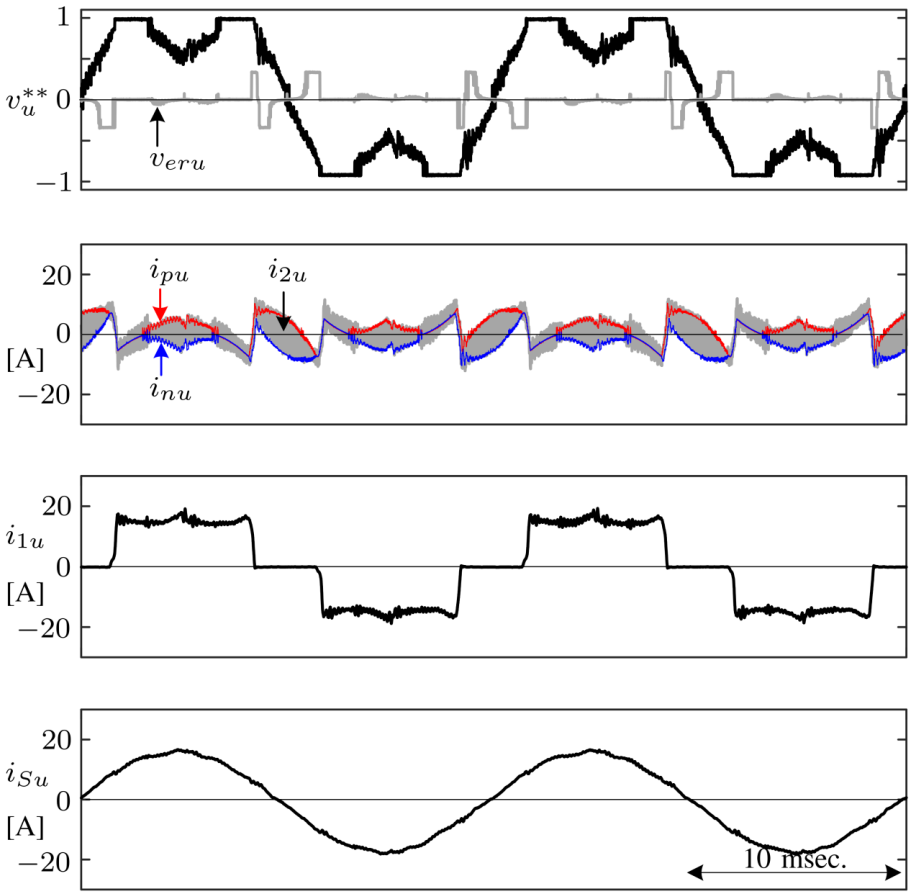

Figure 5.12: The experimental results of the proposed circuit when the IRPC modulated by DPWM3 and using the ac inductance of $L_2 = 185\mu$H with considering the dead-time compensation.

phase (i_{pu} and i_{nu}) were used to find the voltage error by using the equations from (5.12) to (5.14) which was depicted in the voltage error in v_{eru}. The estimated current ripples i_{pu} and i_{nu}, and the voltage error v_{eru} were measured by the digital-to-analog of the control system. When the voltage error v_{eru} was included in the voltage reference v_u^*, the new voltage reference v_u^{**} was used to compare with the triangular carrier to generate the switching signals. It can be seen that the IRPC could produce the current i_{2u} to eliminate the harmonic current of i_{1u}, and the proposed circuit could control the grid current sinusoidal. This can confirm that the dead-time compensation is significant to control the quality of

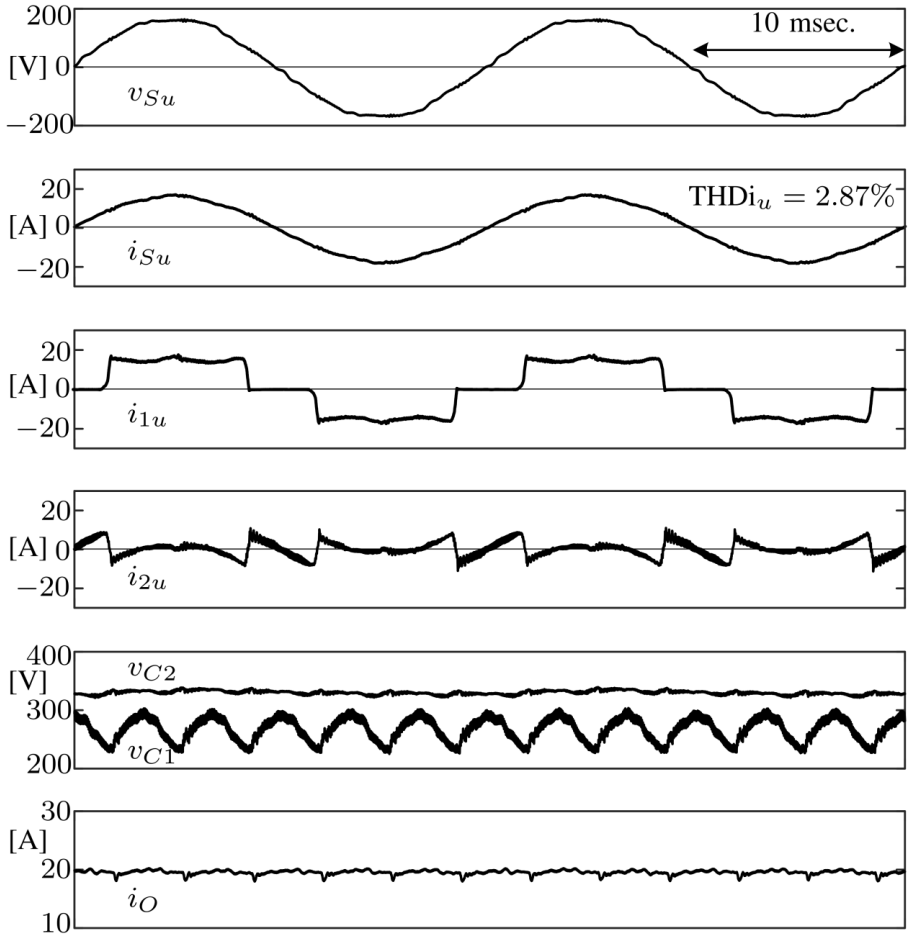

Figure 5.13: The experimental results of the proposed circuit when the IRPC modulated by using the conventional PWM with the ac inductance of $L_2 = 800\mu$H.

the grid currents. Moreover, this method is very simple and suitable for general micro-controllers or DSPs.

5.3.2 Operating IRPC by using Conventional PWM and DPWM3

Figure 5.13 to Figure 5.15 show the experimental results of the proposed circuit when the IRPC controllrf by the conventional PWM with $L_2 = 800\mu$H which provided the current ripples of 30%, the conventional PWM with $L_2 = 185\mu$H, and the DPWM3 with $L_2 = 185\mu$H which provided the current ripples of 100% of

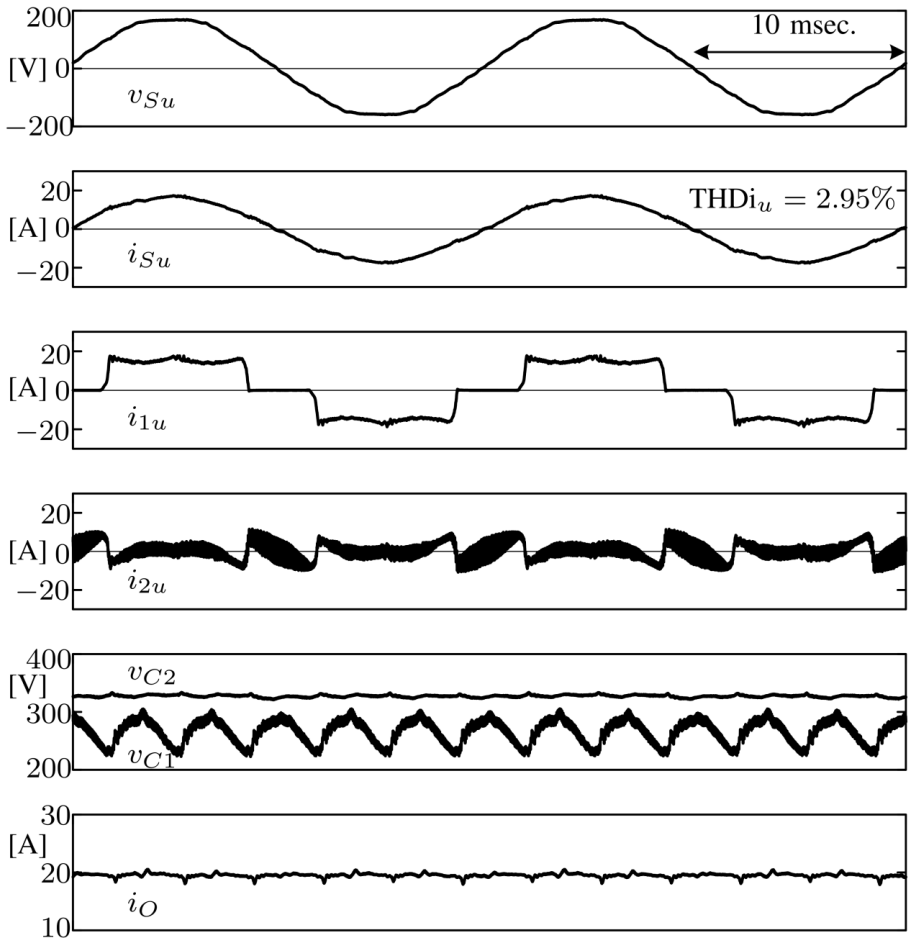

Figure 5.14: The experimental results of the proposed circuit when the IRPC modulated by using the conventional PWM with the ac inductance of $L_2 = 800\mu$H.

the peak current reference i^*_{2u}. Each waveform consists of the grid voltage v_{Su}, the grid current i_{Su}, the rectifier current i_{1u}, the IRPC current i_{2u}, the dc-link voltage v_{C1}, the dc voltage of the IRPC v_{C2}, and the output current of the dc/dc converter i_o at the rated power 4.5kW. Because of the voltage ripple in v_{C1}, there was the absorbed current in the dc-link capacitor before flowing to the dc/dc converter. Thus, the dc-link power compensation needed to be compensated by using the dc/dc converter. Moreover, the dc/dc converter had to control the damping power to maintain the system's stability. As a result, there was a ripple in the output current of the dc/dc converter i_o. The IRPC was able to generate the current i_{2u} to eliminate the harmonic current of the rectifier i_{1u} which provided the sinusoidal

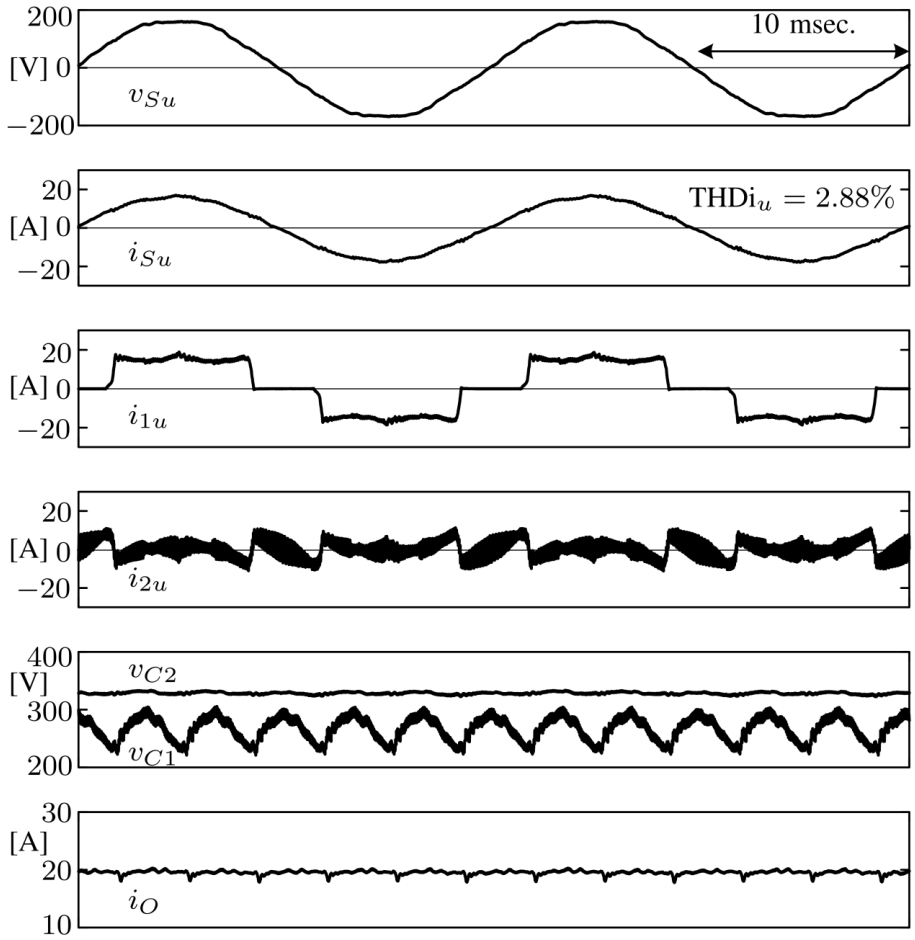

Figure 5.15: The experimental results of the proposed circuit when the IRPC modulated by using the DPWM3 with the ac inductance of $L_2 = 185\mu$H.

waveform for the grid current i_{Su} with the total harmonic distortion lower than 3%.

5.3.3 Efficiency and EMI Measurement

Figure 5.16 depicts the power loss breakdown based on measurement from the ac grid voltage source to the dc-link voltage. The switching devices of the three-phase diode rectifier and the IRPC are the Si-based devices, 600V, 100A MOSFETs (IXFB110N60P3). Figure 5.16(a) shows the several points to measure power losses. The grid power (p_S) was varied from 0 to 4.5 kW. The power losses

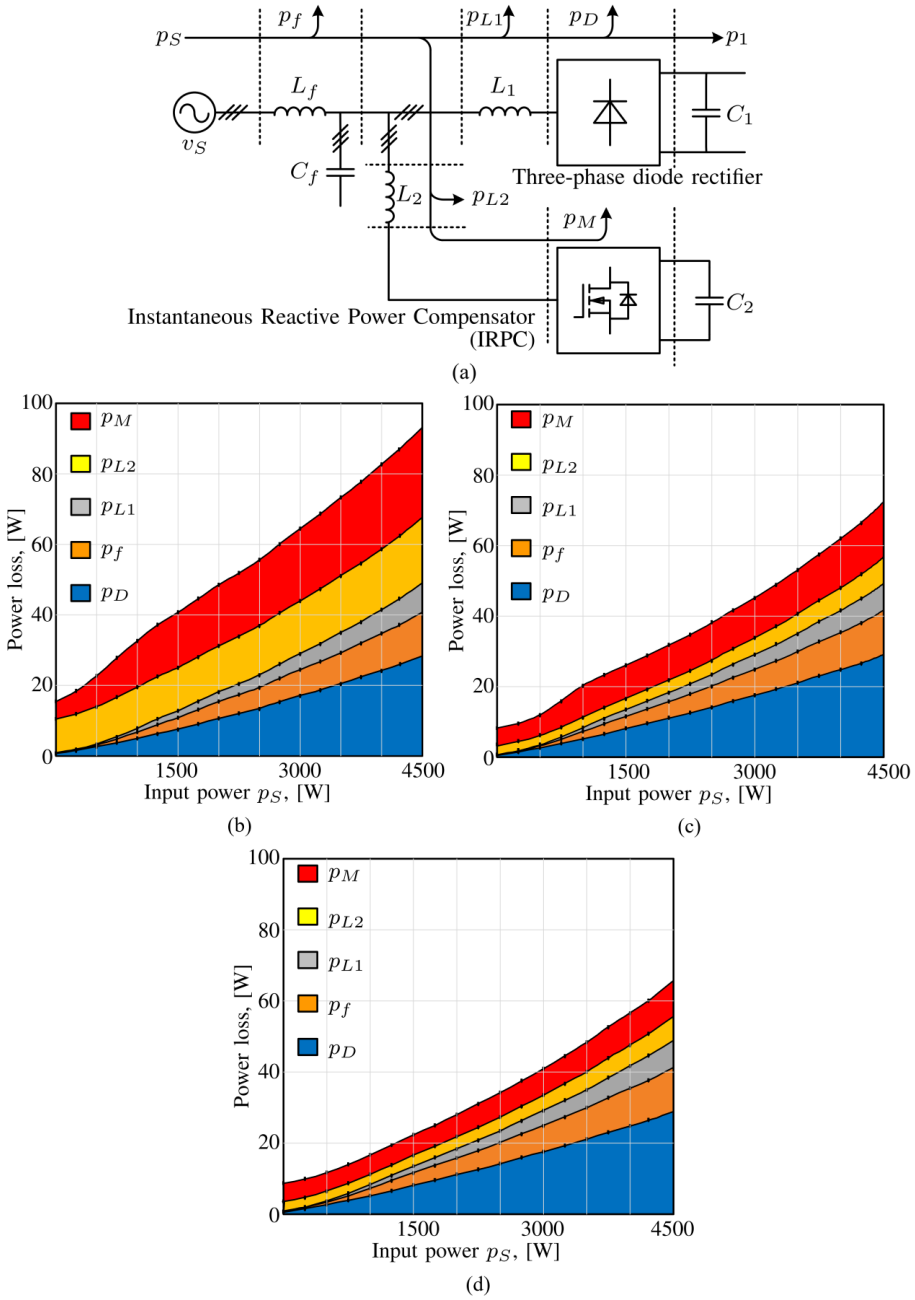

Figure 5.16: The block diagram of the proposed circuit and the power loss breakdown (a) the block diagram for measuring the power losses from the ac grid voltage source to the dc-link voltage, the power loss breakdown of the proposed circuit when the IRPC was modulated by the conventional PWM with $L_2 = 800\mu$H as shown in (b), and with $L_2 = 185\mu$H as shown in (c), and (d) the proposed circuit when IRPC was modulated by the DPWM3 with $L_2 = 185\mu$H.

consist of the power loss in the LC-filter at the ac side (p_f), the power loss in the ac inductors at the rectifier (p_{L1}), the power loss in the ac inductors at the IRPC (p_{L2}), the power loss in the diode rectifier (p_D), and the power loss in the IRPC (p_M). The power loss in the IRPC included the conduction and switching losses.

Figure 5.16(b) illustrates the power loss breakdown of the proposed circuit when the conventional PWM controlled the IRPC with $L_2 = 800\mu$H, which using the toroid core and $N = 50$ turns. Due to the small ripple current, there were many hard-switching areas, as shown in the top figure of Fig 5.7.

When the ac current ripples of the IRPC was increased to 100% of the peak current by reducing the ac inductance of L_2 to 185 μH, using the ferrite core with PQ 40/40 and $N = 23$ turns. The power loss p_M could be reduced to around 50% as shown in Fig. 5.16(c) as well as the power loss of p_{L2}.

Figure 5.16(d) depicts the power losses of the proposed circuit when the IRPC was controlled by the DPWM3 which the PWM was stopped at the peak of the IRPC current. As mentioned in the bellow figure in Fig. 5.7, the power loss p_M could be reduced around 70% of the conventional method because of the combination between the stopped PWM and the extension of the soft-switching regions.

The power losses of p_M in Figures 5.16(b) to 5.16(c) consist of the conduction loss and the switching losses. The conduction loss of the MOSFETS can be calculated by

$$p_{cond} = 3i_{2u(rms)}^2 R_{DS(on)}, \tag{5.22}$$

when $R_{DS(on)}$ of MOSFETs (IXFB110N60P3) was 56 mΩ. Hence, the switching loss can be given by

$$p_{sw} = p_M - p_{cond}. \tag{5.23}$$

It can be seen that the power losses of p_M in (i) and (ii) were very low at the input power p_S nearly 0 because the switching device could be operated in the ZVS region. However, when p_S was increased from 1kW to 4.5kW, the power losses p_M of (i) and (ii) were significantly increased since the ac currents were higher than 0A which was operated in the hard-switching regions. Excepting

Table 5.3: Summary the conduction loss and the switching loss of the IRPC at power 4.5 kW

PWM / L_2	p_M	$i_{2u(rms)}$	p_{cond}	p_{sw}
Convetional PWM /800 μH	25.6 W	4.025 A	2.72 W	22.88 W
Convetional PWM /185 μH	16.15 W	4.5 A	3.4 W	12.75 W
DPWM3 /185 μH	10.3 W	4.51 A	3.42 W	6.88 W

(iii), the PWM was stopped at the peak ac current, and the switching device could be operated in the ZVS region. Because of this, the power loss p_M of (iii) was lower than the other methods.

Table 5.3 summarizes the power losses in the IRPC at the grid power p_S 4.5 kW including the conduction loss (p_{cond}) and the switching loss (p_{sw}) as obtained by (5.22) and (5.23). It can be seen that the DPWM3 could reduce the switching loss to 6.88 W although the conduction loss was increased from the raised current ripple.

Fig. 5.17 shows the efficiency of the proposed circuit when varies the conventional PWM and DPWM3 and L_2 from the power loss breakdown in Fig. 5.16. It can been seen that the combination between DPWM and the ZVS operation, as shown in (iii), has the highest efficiency at around 98.5% at 4.5kW because of the significant reduction in the switching loss.

Fig. 5.18 shows the comparison of the conducted EMIs of the four cases when the switching frequency of each circuit was set to 20 kHz. The Line Impedance Stabilization Network (LISN), which connected between the ac grid voltage source and the circuit without an EMI filter, was used to measure the conducted EMIs of each circuit. The RIGOL DSA815 Spectrum Analyzer was used to analyze the signal from LISN by setting RWB to 9 kHz and display the signal in average value from 150 kHz to 30 MHz. The line (v) shown the limitation standard of CISPR 11 class A group 2 in the average value for industrial equipment. The first case as shown in (i) was the proposed circuit when the switching devices of the

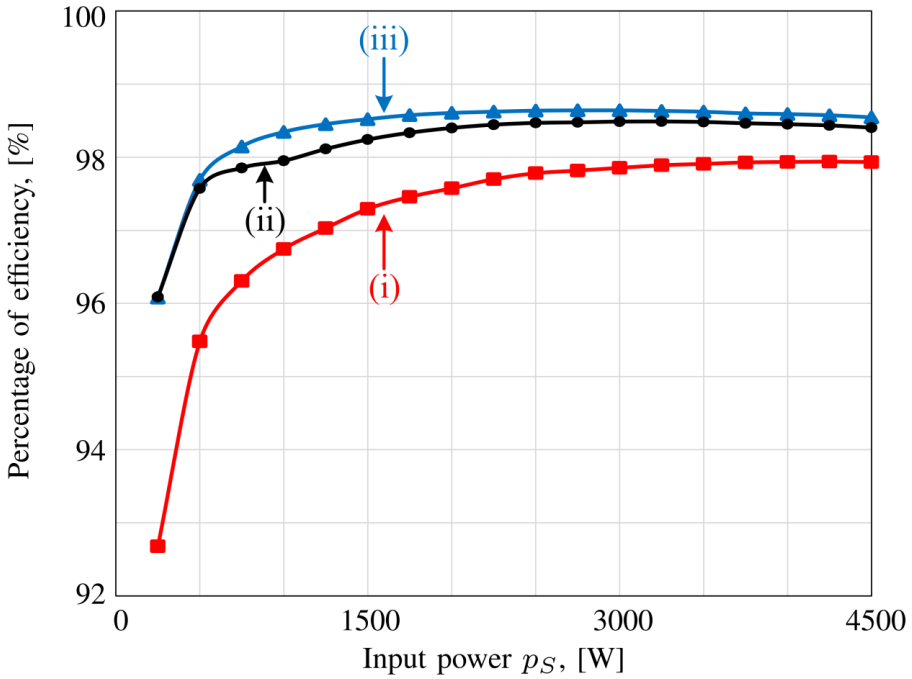

Figure 5.17: Efficiency of Circuits when (i) the IRPC was controlled by the conventional PWM with $L_2 = 800\mu$H, (ii) the IRPC was controlled by the conventional PWM with $L_2 = 185\mu$H, and the IRPC was controlled by the DPWM3 with $L_2 = 185\mu$H.

IRPC were disabled. The dominant noises, which were occurred from the dc/dc converter, was around 2MHz, 4MHz, 8MHz and 16MHz. The line (ii) was the proposed circuit when the IRPC was controlled by the conventional PWM with $L_2 = 800\mu$H. It can be seen that the switching noise from the IRPC was dominant at around 8MHz which was closely the limitation standard line. However, when the IRPC was modulated by the DPWM3 with $L_2 = 185\mu$H as shown in (iii), the amplitude of noise from 8 MHz 15 MHz was reduced and lower than (ii). This can confirm that the DPWM and soft-switching mode of the IRPC produced the noise lower than the hard-switching mode, as shown in the line (ii).

The line (iv) of Fig. 5.18 depicts the conducted EMI of the conventional three-phase PWM rectifier which was modified the circuit from the IRPC. The dc voltage of the IRPC was connected to the dc/dc converter by changing the dc capacitance of C_2 and ac inductance of L_2 to 1000 μF and 600 μH, respectively.

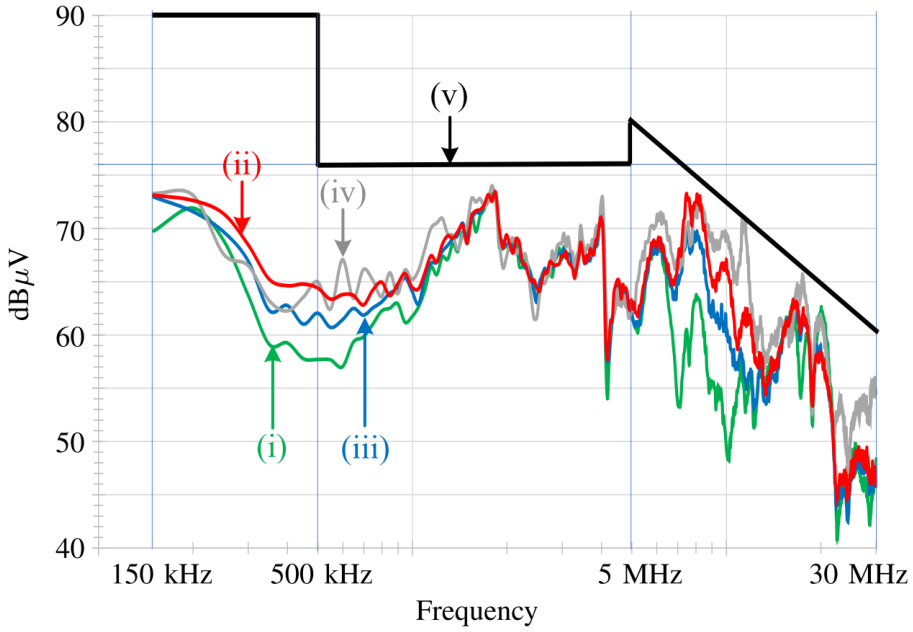

Figure 5.18: The conducted EMIs of (i) the dc/dc converter when the switching devices of the IRPC were turned-off, (ii) the proposed circuit when the IRPC was controlled by the conventional PWM with $L_2 = 800\mu$H, (iii) the proposed circuit when IRPC was controlled by the DPWM3 with $L_2 = 185\mu$H, (iv) the conventional three-phase PWM rectifier with the dc/dc converter, and (v) the EMI limitation standard of CISPR 11.

The ac inductor L_2 and the three-phase diode rectifier were disconnected from the circuit. It can be seen that the amplitude of noise at around 8MHz was equal to the line (ii). However, the amplitudes of noise at around 12 MHz to 16 MHz were increased to the limitation of the standard line (v). That was because the switching devices of the three-phase PWM rectifier circuit operated in the hard-switching mode causing the relative large ringing from the switching devices at the higher ac currents.

5.4 Summary

This Chapter has presented the combination of the DPWM3 and ZVS techniques to reduce the switching loss in the IRPC for a three-phase rectifier system.

DPWM3 can be inactive the switching devices at the peak currents, and thus, it is possible to reduce the switching loss. Moreover, increasing the current ripple until the opposite polarity within one switching cycle can achieve ZVS operation in other areas. Thus, the switching loss in the IRPC significantly reduces more than using CPWM with the same ac inductance. This paper derives the dead-time compensation of DPWM3 based on the estimated current ripples for the IRPC. The switching losses of three different modulations and inductance are compared.

The 4.5-kW experimental setup was used to confirm the theory developed in this paper. As a result, each technique could achieve a sinusoidal grid current with the THD lower than 3%. Furthermore, the combination of the DPWM3 and ZVS techniques could reduce the switching loss to 6.9W at the output power of 4.5kW. The system reached the highest efficiency of 98.5% at the output power of 4.5kW. From these techniques, the switching losses could be reduced more than 70% of the IRPC modulated by the conventional PWM with the same value of the ac inductance of L_2. Moreover, the conducted EMI of the proposed circuit could be reduced without using the EMI filter at the input ac voltage of the circuit.

Chapter 6

Switching Loss Estimation in an Instantaneous Reactive Power Compensator

From the experimental result in Chapter 5, the current ripple mainly affects the power losses in the IRPC. The conduction loss of the IRPC is very small because the current around 32% flows into the IRPC. However, the switching loss is the dominant power loss in the IRPC circuit. The switching losses occur during the turn-on and the turn-off transitions of the MOSFETs, and these power losses are different between the hard-switching and soft-switching modes. Here, the relationship between the current ripple and the switching losses are investigated in this Chapter.

6.1 IRPC Circuit Configuration for Switching Loss Investigation

Figure 6.1 illustrates the three-phase IRPC circuit to measure the switching loss. The circuit consists of the dc capacitor (C_2), the switching devices, and the ac inductor (L_2) connecting with the LC-filter (L_f, C_f) at the grid side. The IRPC is controlled to produce only the reactive power between the dc capacitor C_2 and the ac side of the circuit. In contrast, the active power is used to regulate the

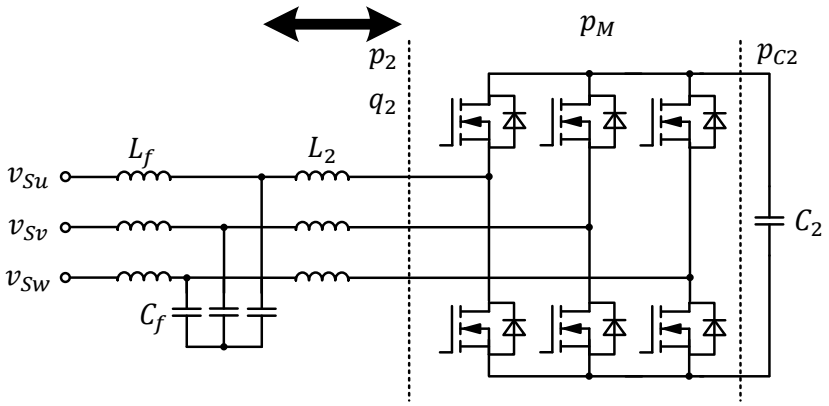

Figure 6.1: The IRPC current.

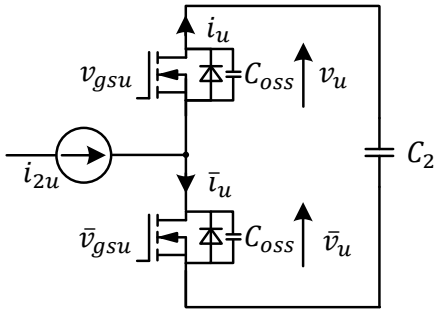

Figure 6.2: The u-phase of the IRPC.

dc voltage v_{C2}. The active power of IRPC is nearly zero because of no dc load connected to the dc capacitor C_2. The power meter (HIOKI: PW6001) is used to measure the input power (p_2) and the output power (p_{C2}) to find the total power loss of the IRPC ($p_M = p_2 - p_{C2}$) which is displayed in the active power of the power meter.

Figure 6.2 shows the u-phase leg of the IRPC circuit, and expresses the direction/position of the current probes (i_u, $\bar{i}_u$) and voltage probes (v_u, $\overline{v}_u$) for measuring the drain-to-source currents and voltage of each MOSFETs. The current source i_{2u} represents the ac current of the u-phase.

Figure 6.3 demonstrates the drain-to-source voltages across each MOSFETs

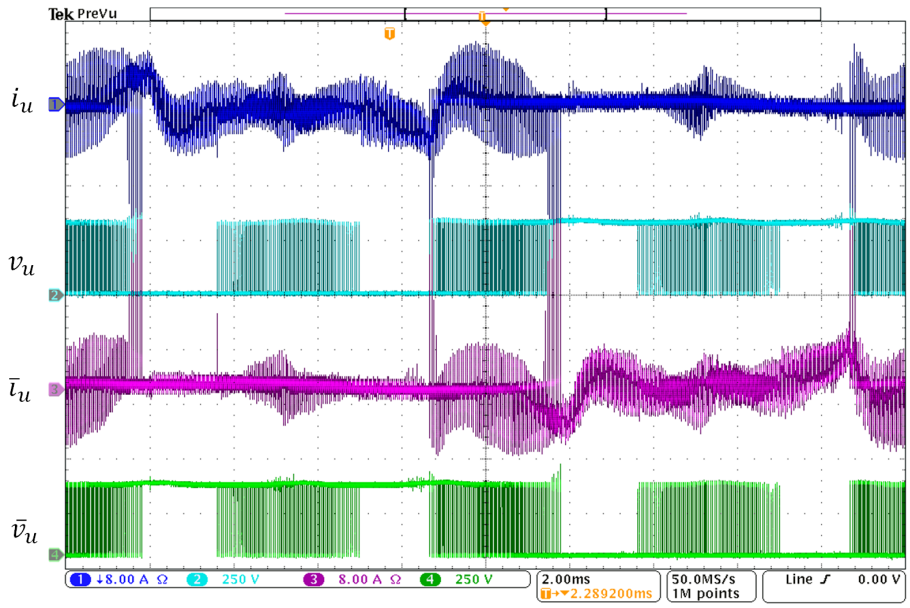

Figure 6.3: The drain-source voltages and currents waveform of the MOSFETs in the u-phase leg.

(v_u, $\overline{v}_u$) and its drain-to-source currents (i_u, $\bar{i}_u$) when the IRPC is controlled by using DPWM3 with the ac inductance of $L_2 = 185\mu$H at the reactive power 1.5 kVar. It can be seen that the operation of each MOSFETs can be divided to 3 states.

The first state is the hard-switching mode which has a lot of noise, as shown in the drain-to-source currents i_u and $\bar{i}_u$ because of the reverse recovery charge from the freewheeling diode resulting in the high-switching loss in the IRPC circuit.

the second state is the soft-switch mode. In this state the current ripple varies in both a positive and a negative polarity within one cycle of the switching frequency. This mode can achieve ZVS operation for the switching devices in the IRPC circuit. It can be seen that the relatively large noise is disappeared in these regions. So, the switching loss in the IRPC is very small. However, the main of the power loss in this duration is from the turn-off transition.

The last state is the PWM-off mode. It can be seen from Figure 6.3 that the drain-to-source voltages v_u, $\overline{v}_u$ were equal to the dc voltage or zero. The currents i_u and $\bar{i}_u$ were able to flow only the turn-on regions. Therefore, the turn-on and

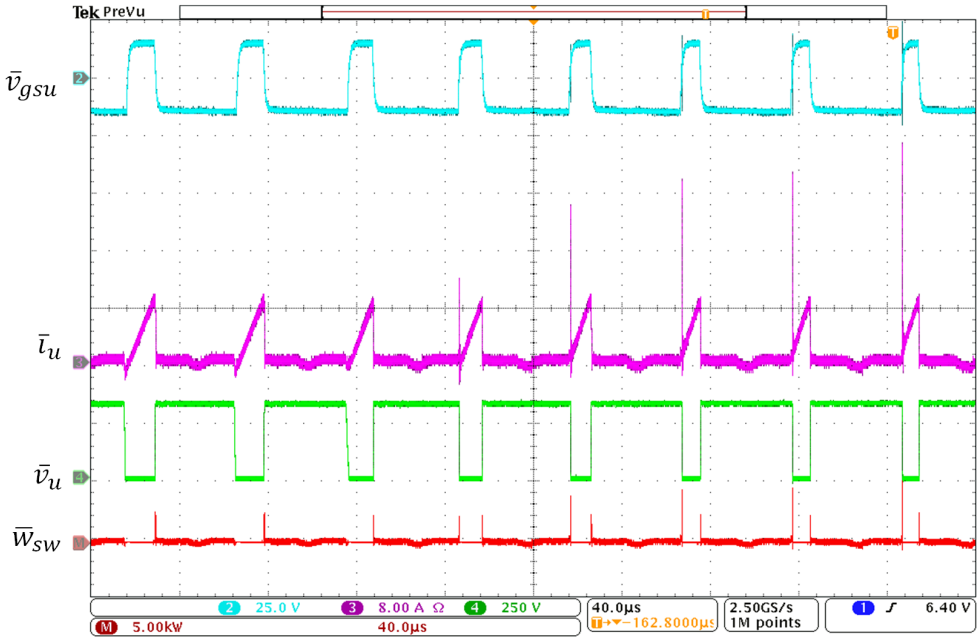

Figure 6.4: The switching waveform of the lower switch of u-phase during the transition changing from the soft- to hard-switching mode.

turn-off losses are eliminated in these regions.

Paper [73] has already been presented the method for estimating the switching loss in a three-phase grid connection circuit in which the current ripple at the ac side is very small. So, the power loss during turn-on and turn-off transition can be calculated in the same current value of each active switching state. From the experiment result in Figure 5.17 clearly expresses that the large current ripples can product a smaller switching loss in the converter circuit. Therefore, in the next section the power losses during the hard-switching and soft-switching mode will be investigated in order to calculate the switching loss when the current ripple is considered in a large value.

6.2 Switching Modes

Figure 6.4 shows the waveform of the lower switch of u-phase changing from the soft-switching mode to hard-switching mode. It consists of the gate-to-source

voltage ($\overline{v}_{gsu}$), the drain-to-source current ($\bar{i}_u$), the drain-to-source voltage ($\overline{v}_u$), and the energy consumption ($\overline{w}_{sw} = \overline{v}_u \times \bar{i}_u$) calculated from the multiple function in the oscilloscope. It is clearly seen that in the soft switching mode the power loss during turn-on disappeared from $\overline{w}_{sw}$, and it remained only the turned-off state loss. On the other-hand, when the current $\bar{i}_u$ varied to the positive value, the noise from the recovery current diode appeared at the on-state of $\overline{v}_{gs}$ which causes a high-switching loss in the circuit. The operating circuit and the switching loss analysis can be explained as follows.

6.2.1 Hard-Switching Mode

In this mode, the switching losses occur from a large reverse recovery current as shown in Figure 6.5. Figure 6.6 demonstrates the operating circuit during turn-on transition (from t_a to t_c) which is explained as follow:

Before t_a, the initial status of the switch S_u was on-state, the switch $\overline{S}_u$ was off, and the initial current i_{2u} was a positive value which flowed from the ac side to C_2 as shown in Figure 6.6(a).

At t_a, the switch S_u was turned off, whereas the current i_u was in a positive value and flowed into the freewheeling diode of the switch S_u as depicted in Figure 6.6(b).

At the time t_b, the lower switch $\overline{S}_u$ began turned on as depicted in Figure 6.6(c). At this time, the current passing the switch $\overline{S}_u$ was shapely increased to the i_{2u}, while the current flowing into the freewheeling diode of the switch S_u was rapidly decreased to the negative value because the freewheeling diode was temporarily conducted in the reverse direction. The reverse recovery current flew into the lower switch $\bar{i}_u$, and this current summed with the current of the lower switch $\bar{i}_u$. As a result, the current $\bar{i}_u$ increased significantly, and thus, the lower switch had a relatively large power loss. After that, the reverse recovery current was reduced and oscillated around zero at t_c that was its ringing. After this time, the upper diode completely turned off, and the lower switch $\overline{S}_u$ carried the current i_{2u} into the negative bus of the IRPC as depicted in Figure 6.6(d).

On the other-hand, when the switching was turned off as shown in Figure 6.5 between the time i_d and t_f, the noise of the switching currents were disappeared

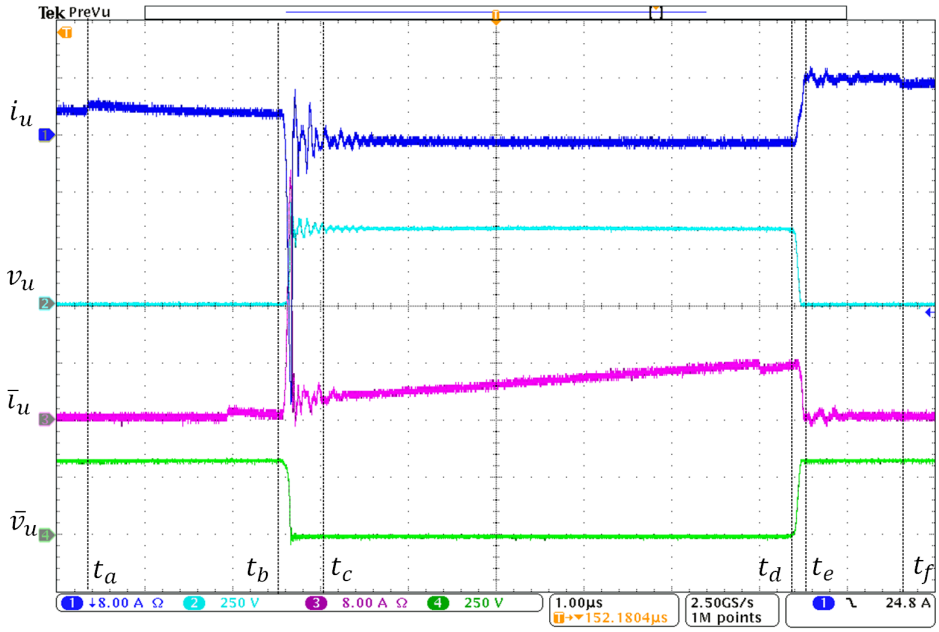

Figure 6.5: The drain-source voltages (v_u, $\bar{v}_u$) and currents (i_u, $\bar{i}_u$) of the MOSFETs in the u-phase leg of the hard-switching mode.

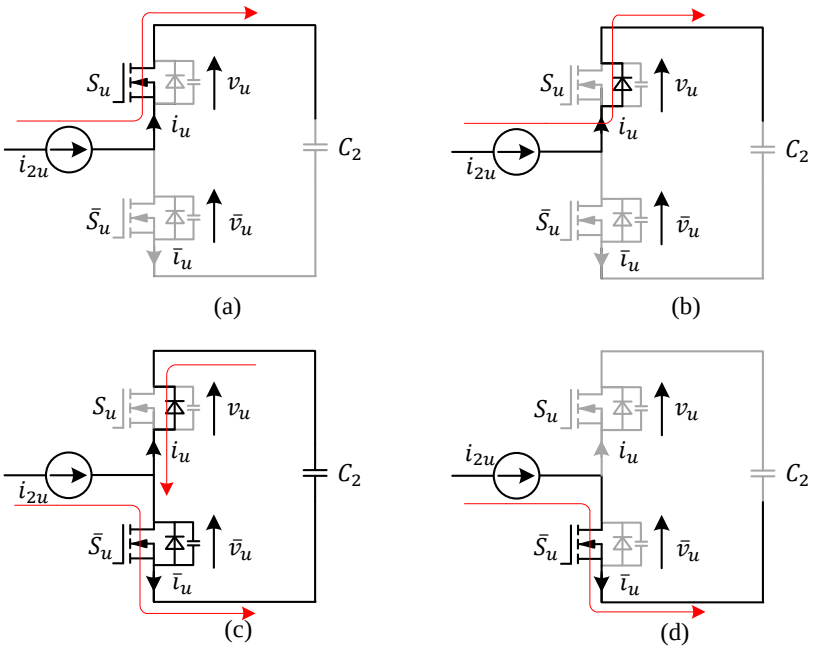

Figure 6.6: Operating circuit of Fig. 6.5 between t_a and t_c.

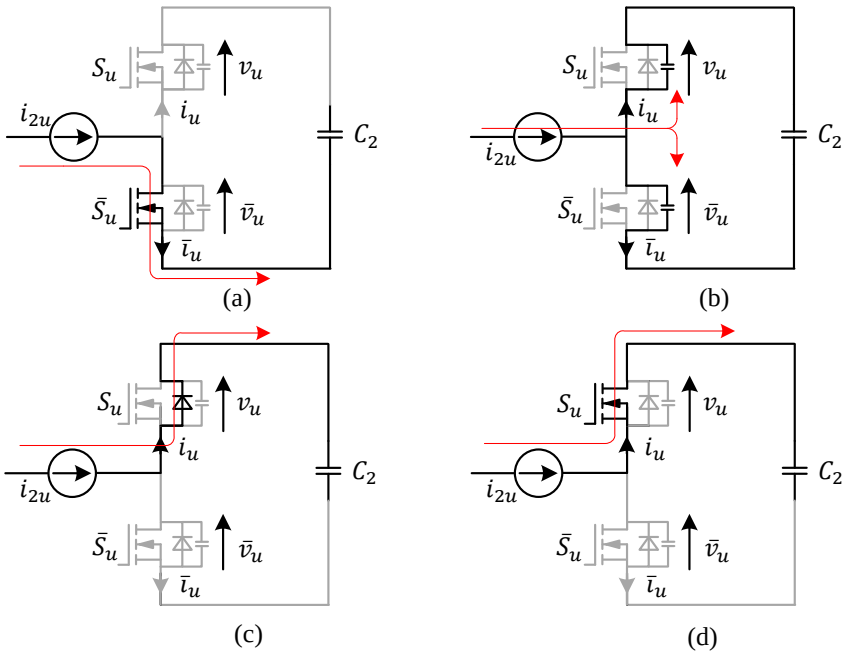

Figure 6.7: Operating circuit of Fig. 6.5 between t_d and t_f.

from the graph. This is because the upper switch of u-phase operated in the soft-switching mode. Figure 6.7 expressed the basic operation during the lower switch $\overline{S}_u$ off which can be explained as follows:

Before the time t_d, Figure 6.7(a) shows the initial state of the switches (S_u and $\overline{S}_u$ were off and on), and the current i_{2u}, which is a positive value, flowed into the negative terminal of C_2.

At the time t_e as shown in Figure 6.7(b), the switch $\overline{S}_u$ was turned off, and then the current i_{2u} flowed to discharge and charge the output capacitor (C_{oss}) of the MOSFETs S_u and $\overline{S}_u$, respectively. Because of this, the voltage v_u of the upper switch was reduced to zero, and its freewheeling diode carried the current i_{2u} to the positive terminal of C_2 as depicted in Figure 6.7(c). Therefore, the upper switch S_u was be able to turn on under the ZVS operation after the time t_f as shown in Figure 6.7(d). During the turned off transition, the power loss of the switching device would come from the lower switch $\overline{S}_u$ which behaves the resistance characteristic in the turn-off duration. The details of the switching loss calculation can be explained as follows:

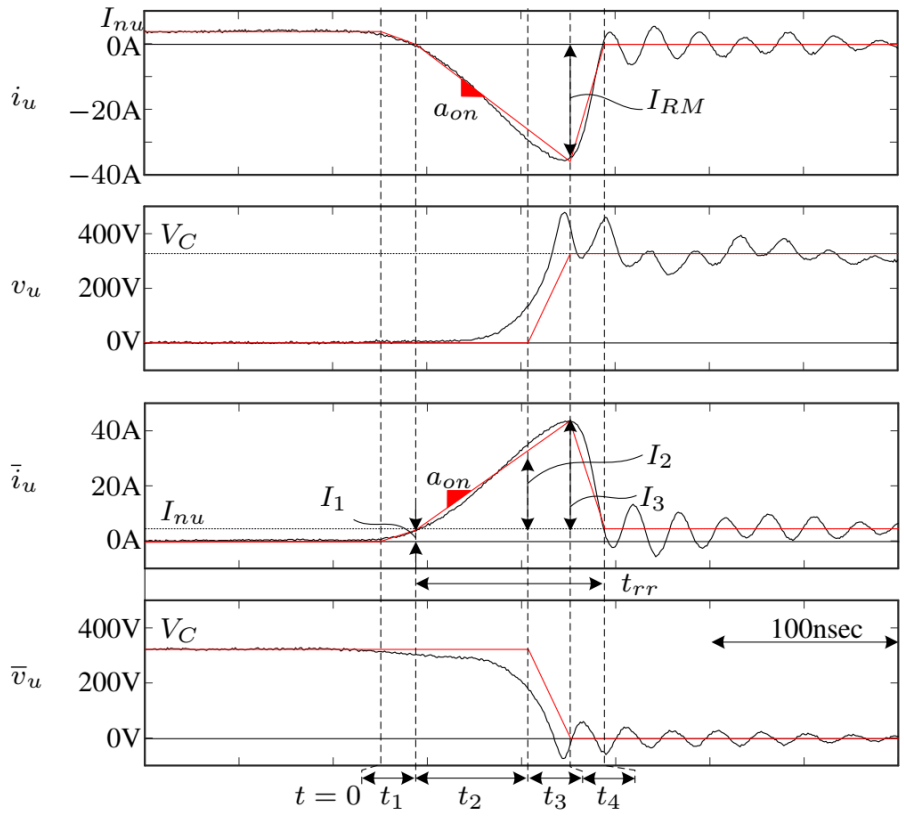

Figure 6.8: Experimental and ideal current and voltage waveform of the u-phase switching devices during diode turn off and MOSFET turn on.

Figure 6.8 shows the closed-up experiment waveform and ideal waveform where the upper diode of MOSFET was in the turn-off transition, and the lower MOSFET was in the turn-on duration. During this procedure, the energies coming from the turn-off transition of diode and the turn-on MOSFET can be estimated by using the ideal waveform as follows:

$$W_1(i_{pu}, i_{nu}) = \int_{t=t_2}^{t_3+t_4} v_u i_u dt + \int_{t=0}^{t_1+t_2+t_3+t_4} \overline{v}_u \bar{i}_u dt,$$
$$= \frac{V_C I_{nu}}{2}(t_1 + 2t_2 + \frac{t_3}{2}) + \frac{V_C I_{RM}}{2}(t_2 + \frac{t_3}{2} + 2t_4) - \frac{V_C a_{on}}{2}(t_2 + t_3)t_3, \qquad (6.1)$$

when $t_1 = t_r$ is the raise time to reach the current $I_1 = I_{nu}$. t_r is nearly the same value in the datasheet at 30 nsec. t_2 is the time duration when the reverse recovery current increases from I_1 to the current I_2 until the voltage $\overline{v}_u$ starts

decreasing. t_3 is Miller effect time duration when the voltage v_u increases to $V_C = v_{C2}{}^*$, while the voltage $\overline{v}_u = V_C - v_u$. This time can be calculated from the gate resistance ($R_g = 30\ \Omega$ in the gate-driver circuit). Thus, the time t_3 is around 25 nsec. At the end of t_3, the currents i_u and $\overline{i}_u$ reach to the maximum current with a slope a_{on} at $I_{nu} + I_{RM}$, and I_{RM} which is the maximum reverse recovery current, respectively. From the measurement between t_2 and t_3, the calculated slope of a_{on} is equal to $\frac{di_u}{dt} = 456$ A/μsec, and thus, it is possible to calculate the time t_2 which can be expressed by $\frac{I_{RM}}{a_{on}} - t_3$. The time t_4, is the decreasing current duration from the maximum current to zero, is equal to $t_{rr} - t_2 - t_4$. Based on the measurement, the t_{rr} equals to 110 nsec.

After t_4, the lower MOSFET contained the current $\overline{i}_u$ which increased to the current I_{pu} as shown in Figure 6.9 before the lower switch was turned off at the beginning of t_5. The current i_{2u} from the ac side was divided into two parts. The first part was the current i_u flowing to the upper switch and the second part is the current $\overline{i}_u$ flowing to the lower switch. The output capacitance C_{oss} had a non-linear characteristic depending on the drain-to-source voltage of each MOSFET. Because of this, the currents flowing to the output capacitor had a slope a_{off}. These currents could charge and discharge the output capacitor of the upper and lower switch to 0 V and V_C at the end of t_5. However, the current of the lower switch $\overline{i}_u$ was higher than the charging output capacitor current (blue line) because the gate-to-source voltage was nearly between the threshold voltage and 0 V. As a result, the lower MOSFET behaved like a varied resistor. When the drain-to-source voltage was increased, the current passed through the resistor, causing the energy loss in the MOSFET during the turn-off transition. Neglecting the loss in t_6, the consumed energies during the turn-off transition can be approximated from the ideal voltage and current during the time t_5 as shown by

$$W_{off}(i_{pu}, i_{nu}) = \int_{t=0}^{t_5} \overline{v}_u \overline{i}_R dt = \int_{t=0}^{t_5} \overline{v}_u (\overline{i}_u + \overline{i}_C) dt, \tag{6.2}$$

when $\overline{i}_u = I_{pu}$ at $t = 0$. Thus, the current flows into a resistor of the MOSFET can be given by

$$\overline{i}_R = I_{pu} + \overline{i}_C = I_{pu} + a_{off} t, \tag{6.3}$$

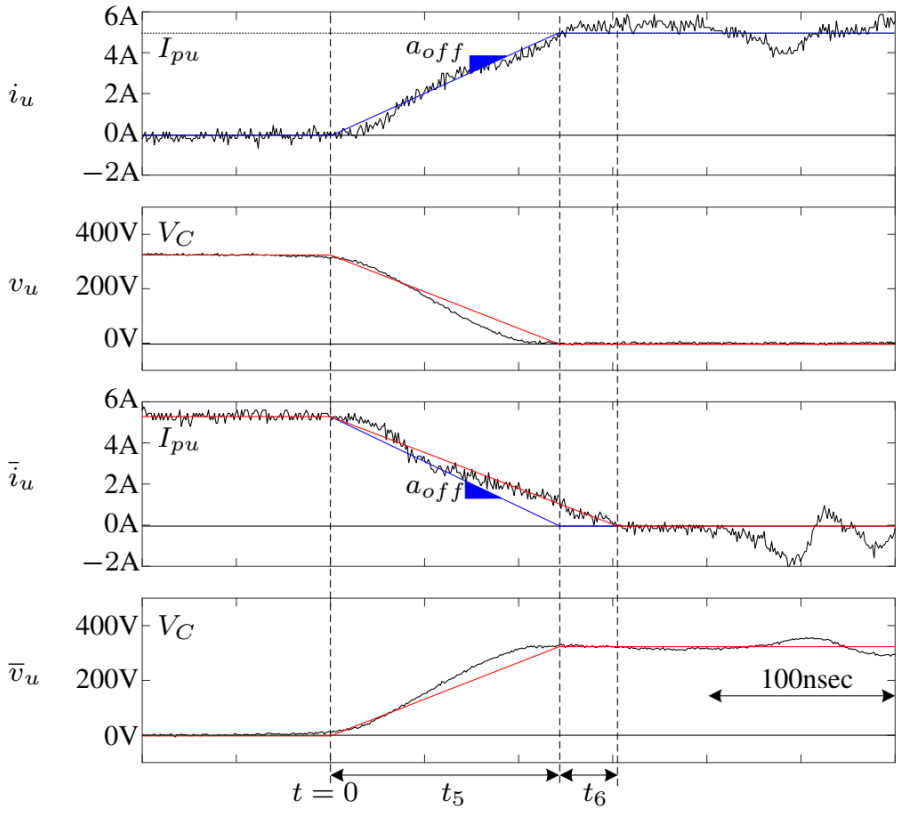

Figure 6.9: Experimental and ideal current and voltage waveform of the u-phase switching devices during the voltage across upper MOSFET discharge and lower MOSFET turn off.

The slope a_{off} is a negative value which equal to $-a_{off} = \frac{I_{pu}}{t_5}$, and $t_5 = \frac{C_{oss}V_C}{I_{pu}} = -\frac{I_{pu}}{a_{off}}$. Thus, the current $\bar{i}_C = -a_{off}t$ flows to charge the output capacitor C_{oss} of the lower switch and the voltage $\overline{v}_u$ reaches to V_C at the end of t_5. Therefore, the voltage $\overline{v}_u$ can be given by

$$\overline{v}_u = \frac{1}{C_{oss}} \int_{t=0}^{t_5} \bar{i}_C dt = \frac{-1}{C_{oss}} \int_{t=0}^{t_5} a_{off} t dt = \frac{-a_{off}}{2C_{oss}} t^2. \tag{6.4}$$

From the experimental results in Fig. 6.9, the average capacitance can be calculated by $C_{oss} = \frac{I_{pu}t_5}{V_C} = 1.4\text{nF}$. It supposes that the output capacitance C_{oss} of the upper switch equals to the lower switch. Substituting $\bar{i}_R$, $\overline{v}_u$ and t_5 into (6.2), the energy loss in the resistor can be obtained by

$$W_{off}(i_{pu}, i_{nu}) = \frac{{I_{pu}}^4}{24C_{oss}{a_{off}}^2}. \tag{6.5}$$

Therefore, the total consumed energy of the switch in the hard-switching mode can be given by

$$W_H(i_{pu}, i_{nu}) = W_1(i_{pu}, i_{nu}) + W_{off}(i_{pu}, i_{nu}). \tag{6.6}$$

6.2.2 Soft-switching Mode

In the soft-switching mode operation, the voltage across the switching device reduces to zero before that switch is turned on. Thus, it does not have the reverse recovery current like the hard switching mode. As a result, the turn-off diode loss and the turn-on switching loss disappear from the soft-switching mode resulting in the significant reduction of the power losses for the switching devices.

The soft-switching mode can consider from the relationship between the current ripples, the current I_{min} as shown in (5.8), and the polarity of the average current ${i_{2x}}^*$. For example, in the u-phase leg of the IRPC circuit, if the average current ${i_{2u}}^*$ is a positive value, the current ripple i_{pu} must be higher than the current I_{min} to achieve the ZVS. On the other hand, the current ripple i_{nu} must be less than the current $-I_{min}$ to achieve the ZVS operation whenever the average current ${i_{2u}}^*$ is negative.

From the operating waveform and circuit in Figures 5.3 to 5.5 where the average current ${i_{2u}}^*$ is positive, the turn-off losses occur twice time per the switching frequency. Thus, the consumed energies can be obtained by

$$W_S(i_{pu}, i_{nu}) = \frac{{I_{pu}}^4}{24 C_{oss} {a_{offp}}^2} + \frac{{I_{nu}}^4}{24 C_{oss} {a_{offn}}^2}, \tag{6.7}$$

when a_{offp} and a_{offn} are the slope currents where the switching devices were turned off at the current ripples i_{pu} and i_{nu}, respectively. These slopes can be calculated the same way from the turn-off transition in the hard-switching mode.

It can be seen that the energies in (6.6) and (6.7) are the function of the current ripples i_{px} and i_{nx} which can be obtained by [80] for the IRPC modulated by CPWM and Table. 5.1 for the IRPC modulated by DPWM3. Therefore, it is possible to estimate the average switching power loss for the three-phase IRPC modulated by CPWM as follows:

$$P_{sw}^{\text{CPWM}} = \frac{3}{T} \int_0^T \left(W_H(i_{pu}, i_{nu}) + W_S(i_{pu}, i_{nu}) \right) f_{sw} dt, \tag{6.8}$$

when T is the number of the sampling point in the grid frequency 50 Hz. In case of the IRPC modulated by DPWM3, the average switching loss can be calculated by

$$P_{sw}^{\text{DPWM3}} = \frac{3}{T}\frac{2}{3}\int_0^T \left(W_H(i_{pu}, i_{nu}) + W_S(i_{pu}, i_{nu})\right) f_{sw} dt, \tag{6.9}$$

when 2/3 represents the factor of DPWM3. The estimated switching loss method are assumed that the switching losses of each phase are balance.

Figure 6.10 shows the 5-kW simulation result for the switching loss of the IRPC in the u-phase leg when the conventional PWM controls the IRPC with $L_2 = 185$ μH. The current ripples can be estimated by using the proposed technique in paper [80]. It can be seen that there are a lot of hard-switching regions

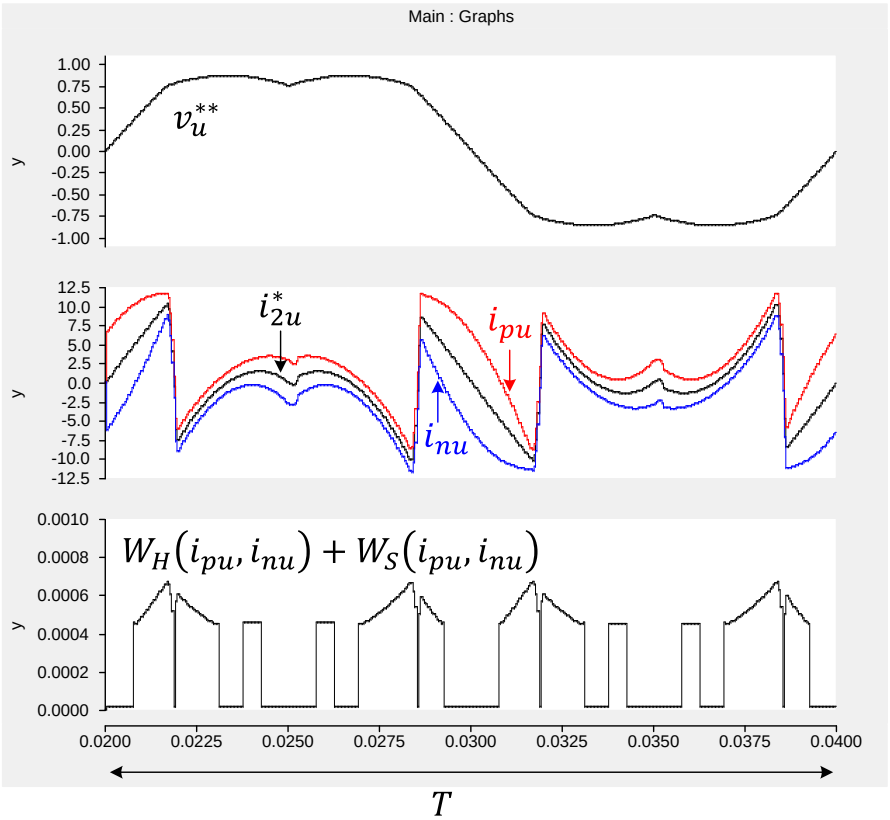

Figure 6.10: Simulation result of energy loss in the u-phase leg of the IRPC circuit controlled by the conventional PWM with $L_2 = 185\mu$H.

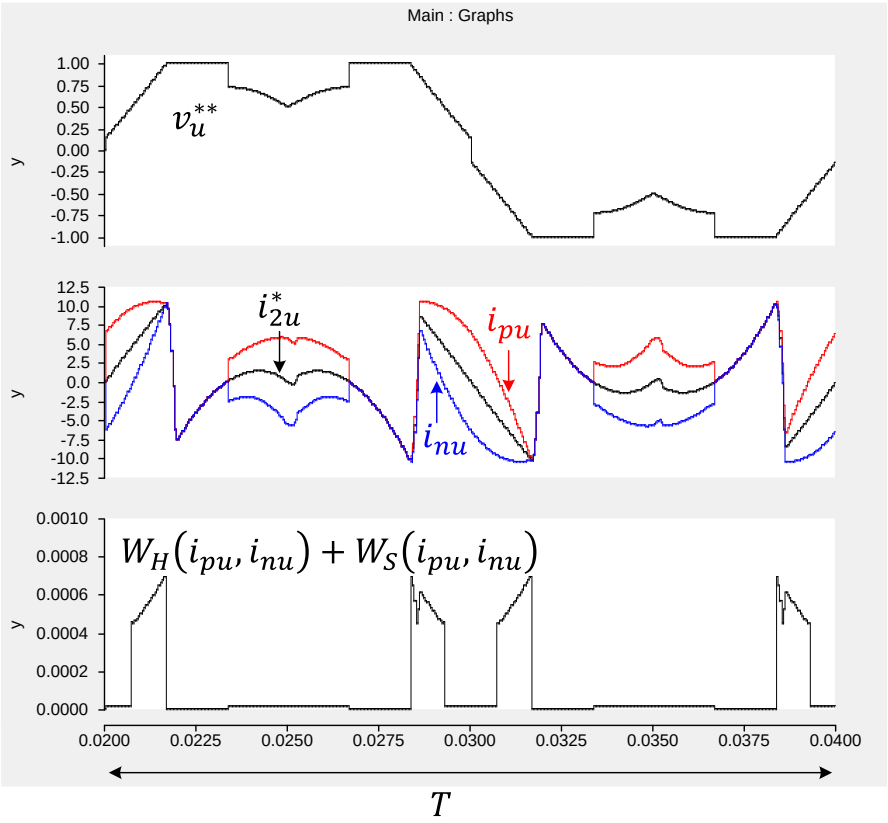

Figure 6.11: Simulation result of energy loss in the u-phase leg of the IRPC circuit controlled by DPWM3 with $L_2 = 185\mu$H.

to generate the high energy loss for the switching devices, especially at the peak current of i_{2u}^*.

Figure 6.11 depicts the simulation result of the u-phase leg of the IRPC circuit at the output power of 5 kW. DPWM3 with $L_2 = 185$ μH is used to control the IRPC. The current ripples can be calculated from Table 5.1 to find the energy consumption. It can be seen that the energy losses are disappeared at the peak current. Moreover, when the voltage modulation ${v_u}^{**}$ is saturated at 1 and -1, the energy loss is zero because of no PWM in these regions. As a result, the energy consumption of this technique is significantly decreased when compared with the convention PWM with the same inductance of L_2.

Figure 6.12 shows the switching losses of the IRPC based on the measurement compared with the simulation. The high inductance of $L_2 = 390$ μH could

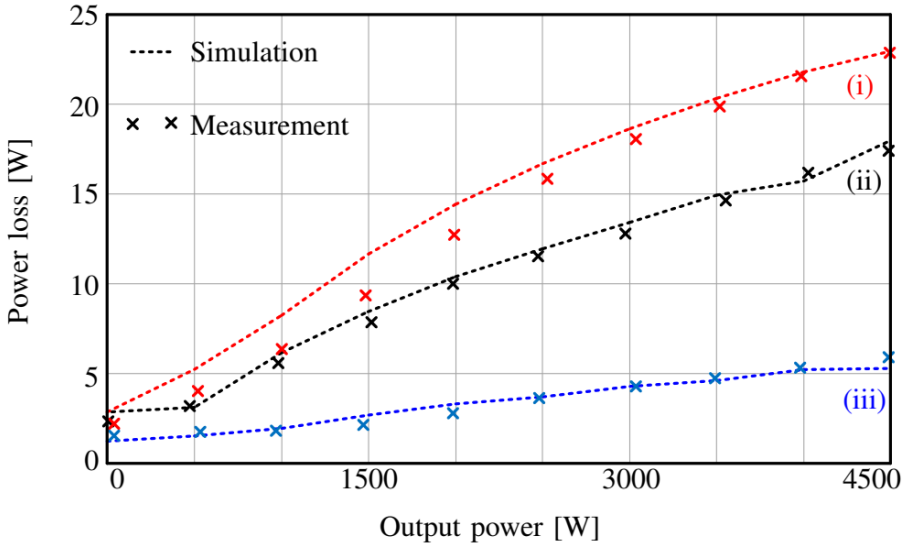

Figure 6.12: The switching loss based on simulation and measurement of the IRPC when controlled by (i) CPWM with $L_2 = 390\mu$H, (ii) CPWM with $L_2 = 185\mu$H and (iii) DPWM3 with $L_2 = 185\mu$H.

produce the highest switching loss around 24 W at the output power of 4.5 kW. During the hard-switching region, the main power loss was from the high reverse recovery current diode. When the inductance of L_2 was reduced to 185 μH, the currents of the IRPC were possible to achieve ZVS, excepting around the peak current, which could produce a high switching loss. The switching loss was slightly reduced by 5 W of the high inductance. In the case of DPWM3, the switching devices were inactive at peak currents. Therefore, from the soft-switching areas and DPWM3, the switching loss significantly decreased to 5.5 W at the output power of 4.5 kW. The dotted lines show the simulated switching loss by integrating the energy losses as shown in (6.8) for the conventional PWM and (6.9) for the DPWM3. As a result, the estimated switching losses were closed to the measurement. Therefore, this technique can estimate the switching loss for the IRPC circuit.

6.3 Summary

This Chapter has presented the behavior of the hard-switching mode and the soft-switching mode in an instantaneous reactive power compensator (IRPC). The hard-switching mode can produce a high switching loss for the system because of the reverse recovery current charge depending on switching devices' characteristics. Thus, the power loss of the hard-switching mode occurs from the turn-on duration and the turn-off transition.

In the soft-switching mode, the ZVS operation makes it possible to eliminate the turn-on losses for the switching device. As a result, the total consumed energy can be reduced significantly because the turn-off losses are smaller than the turn-on losses. The peak current of the IRPC would be able to operate in the hard-switching mode, which degrades the system's efficiency. DPWM3 is proposed to control the IRPC, which can temporarily stop PWM at the peak current, resulting in a significant switching loss reduction. From analysis in this Chapter, the switching loss estimation technique can be used to calculate the switching loss in the IRPC, which is nearly close to the experimental results.

6. SWITCHING LOSS ESTIMATION IN AN INSTANTANEOUS REACTIVE POWER COMPENSATOR

Chapter 7

Conclusions and Future Research

7.1 Conclusions

This doctoral dissertation has introduced an ac/dc power conversion system by using a three-phase diode rectifier with an instantaneous reactive power compensator (IRPC) which has the capability to control the grid current sinusoidal. The proposed circuit can use small film capacitors instead of electrolytic capacitors at the dc-link voltage and the dc voltage of the instantaneous reactive power compensator. These effectively improve the power density and its lifetime problem from an electrolytic capacitor. Furthermore, the small ac inductor is placed at the ac side of the diode rectifier to reduce a small current drawn into the dc-link capacitor. When the dc/dc converter controls power to load, the ac current of the diode rectifier is formed as a square waveshape that behaves like a harmonic current source. Thus, the IRPC can provide the current around 32% of the grid current rating to suppress the harmonic current of the diode rectifier. This gives an opportunity to reduce switching and conduction losses of switching devices and improve the efficiency and the power density of the system. Moreover, the volume of the ac inductor is expected to reduce to $\frac{1}{4}$ of a conventional PWM rectifier.

In Chapter 2, state-of-the-art and literature review of electric vehicle charging systems have been described. In electric vehicle charging systems, an active front-end rectifier is an important ac/dc power conversion to provide a dc voltage for

a dc/dc converter and to control the quality of grid currents with unity power factor. Many active front-end rectifier topologies are reviewed in this section.

In Chapter 3, an analysis of a three-phase diode rectifier with an instantaneous reactive power compensator has been introduced in this section. Due to small ac inductors, the diode rectifier has two operating modes of each state such as the non overlap (two-diode connection) and the overlap commutation (three-diode connection). The advantage of the overlap commutation is that the IRPC current has the overlap time during changing its current from peak-to-peak. This can effectively reduce the error state in the current controller of the IRPC. From the analysis, the instantaneous active power and the instantaneous reactive power of the diode rectifier can be calculated from the output power and the dc-link power, and thus, the IRPC controller does not need to detect harmonic currents for injecting the currents of the diode rectifier. Because of this, the number of the current sensors is the same as a conventional PWM rectifier.

In Chapter 4, the cause of an unstable in the proposed circuit has been analyzed. As a result, the dc/dc converter behaves as the negative conductance connected in parallel with the dc-link capacitor when the dc/dc converter controls a constant power to the load. Thus, the damping control is proposed to eliminate the effect of this negative conductance. The damping control is like a virtual conductance that is operated in the current controller of the control system. In the conventional method, the damping control is in the current controller of the dc/dc converter causing a large current ripple. On the other hand, due to a small inductance used for the ac inductors at the rectifier side, the damping control is possible to operate in the current controller the IRPC that can effectively reduce the output current ripple of the system. The 4.5-kW experimental setup was used to verify the new control method and the damping control of the proposed circuit.

In Chapter 5, the combination between the discontinuous pulse-width modulation (DPWM) and the zero-voltage switching techniques are presented to reduce the switching loss of the instantaneous reactive power compensator. The DPWM3 is suitable for the proposed circuit because the PWM signals are stopped at the peak currents which can effectively reduce the switching losses of the proposed circuit. Moreover, to extend the soft switching area, the increase of the current

ripple is the way to achieve the ZVS operation which is designed to start ZVS at the half of IRPC currents in peak (at 4.5 kW). This is possible to limit the conduction loss in the IRPC circuit. Thus, the switching losses of the proposed circuit can be significantly reduced even though using general Si-MOSFETs.

In Chapter 6, the switching loss approximation for the IRPC circuit is proposed. The IRPC has two mode operation, such as the hard-switching mode and the soft-switching mode. The hard-switching mode can produce a high switching loss because of the reverse recovery current charge in MOSFETs. The power loss of the hard-switching mode occurs from the turn-on duration and the turn-off transition. In the soft-switching mode, the ZVS operation makes it possible to eliminate the turn-on losses for the switching device. As a result, the total consumed energy can be reduced significantly.

7.2 Future research

In this dissertation, a three-phase diode rectifier with an instantaneous reactive power compensator has been discussed in the theoretical and verified by using the experimental setup. Furthermore, the discontinuous pulse-width modulation and the zero-voltage switching technique have been proposed to reduce the switching losses of the compensator. The conduction loss of the diode rectifier was the main power loss in this system; however, it can be easily decreased by using MOSFETs instead of diodes. This technique has the additional capability to improve the efficiency and enable the bidirectional power flow in the system which is suitable for many applications such as vehicle-to-grid, battery energy storage systems, and so on. Note that, when the rectifier is operated in the inverting mode, the commutation overlap is unlike the proposed circuit because the current does not flow through the body diode of the MOSFETs and the dc-link voltage is a little bit higher than the line-to-line grid voltage. Therefore, the overlap time operation should be considered by using the technique of Dr. Kazuto Takagi as presented in [17].

For the vision of the author, the proposed circuit has the opportunity to develop in the future as follows:

- Due to the low switching loss, the increasing switching frequency of the compensator is the way to reduce the size of the inductor and can study the effect of EMI in the ac/dc power conversion system,
- An increasing current ripple can make the compensator operating in the zero-voltage switching condition but it has a large current flowing into a film capacitor which causing the current stress in a capacitor. An interleave compensator technique is possible to solve this problem and make a opportunity to increase the power of the system.
- The damping control can be operated in the compensator, and thus, the dc/dc converter can be changed to other high-efficiency circuits such as a dual active bridge converter.

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Publications

List of Publications related to the dissertation

Journal Papers

1. N. Surasak and H. Fujita, "Current Ripple Reduction Method in a Three-Phase Diode Rectifier with an Instantaneous Reactive Power Compensator," IEEE Transaction on Industrial Applications, VOL. 58, NO. 3, pp. 3808-3818, May-June 2022.

2. N. Surasak and H. Fujita, "Switching Loss Reduction Method for Instantaneous Reactive Power Compensator in Three-Phase Rectifier System," IEEE Journal of Emerging and Selected Topics in Power Electronics, 2022, doi: 10.1109/JESTPE.2022.3216954 (early access).

International Conference Papers

1. N. Surasak and H. Fujita, "Control of A Three-Phase Diode Rectifier with An Instantaneous Reactive Power Compensator," 2020 IEEE Energy Conversion Congress and Exposition (ECCE), Detroit, MI, USA, 2020, pp. 4579-4586.

2. N. Surasak and H. Fujita, "Switching Loss Evaluation in a Three-Phase Diode Rectifier with an Instantaneous Reactive Power Compensator," 2022 International Conference on Electrical Machines and Systems (ICEMS), Chiang Mai, Thailand, 2022.