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論文 / 著書情報
Article / Book Information

題目(和文)	
Title(English)	1T1C FeRAM memory array with Hf0.5Zr0.5O2-based ferroelectric film
著者(和文)	奥野潤
Author(English)	Jun Okuno
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学位種別(和文)	博士論文
Category(English)	Doctoral Thesis
種別(和文)	論文要旨
Type(English)	Summary

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（博士課程）
Doctoral Program

論 文 要 旨

THESIS SUMMARY

系・コース： Department of, Graduate major in	電気電子 系 電気電子 コース	申請学位（専攻分野）： Academic Degree Requested	博士 （工学） Doctor of Engineering
学生氏名： Student's Name	奥野 潤	指導教員（主）： Academic Supervisor(main)	若林 整 教授
		指導教員（副）： Academic Supervisor(sub)	

要旨（英文 800 語程度）
Thesis Summary（approx.800 English Words ）

Since ferroelectric $HfSiO_2$ material was reported in 2011, there has been much discussion about its application to 1T1C FeRAM. However, the feasibility under practical memory array operation using 1T1C memory cell structures has never been discussed. In the conventional method, a large area around 100 μm² of Metal/Ferroelectric/Metal (MFM) capacitor has been commonly used to amplify small displacement current, resulting in unrealistic memory cell structure with limitation of operating condition due to RC delay. In this thesis, a 64 kbits 1T1C FeRAM memory array with $Hf_{0.5}Zr_{0.5}O_2$-based film using dedicated CMOS logic circuits was integrated into 130 nm CMOS technology node and demonstrated the memory array operation for the first time.

In Chapter 2, materials used in the 1T1C FeRAM were mentioned. $Hf_{0.5}Zr_{0.5}O_2$ was chosen as a ferroelectric material from large concentration window and CMOS process compatibility point of view. The atomic layer deposition process using TEMAHf and ZyALD as metal precursors and oxidizer were optimized to obtain higher remanent polarization considering limitation of thermal budget.

In Chapter 3, experimental of the process integration and design of $Hf_{0.5}Zr_{0.5}O_2$-based 1T1C FeRAM were mentioned. The 64 kbits of MFM capacitors with $Hf_{0.5}Zr_{0.5}O_2$-based material were implemented into 130 nm CMOS technology with capacitor under bitline structure. A dedicated sense amplifier for destructive read scheme was designed in the circuit. The change in bitline voltage (ΔV_{BL}) that occurs during read operation can be compared with reference voltage (V_{REF}) generated from a reference capacitor (C_{REF}) or an externally applied voltage.

In Chapter 4, the memory array operation of 64 kbits $Hf_{0.5}Zr_{0.5}O_2$-based 1T1C FeRAM were investigated. First, the simulation result of the designed circuit reveled that it allows the 1T1C FeRAM to apply pulse width with less than 10 ns and the behavior of ΔV_{BL} during read operation for data0 and data1 were experimentally confirmed. The memory array performance with write and sense voltages of 2.5 V and operation speed of 10 ns or less were verified by investigating a shmoo plot and found to be in good agreement with the ferroelectric switching kinetics of the Nucleation Limited Switching model.

In Chapter 5, memory window analysis of the 64 kbits 1T1C FeRAM were performed. A perfect yield and a large memory window were obtained at the capacitor area of 0.4 μm², revealing good uniformity or the film. Memory window at median value in the 64 kbits 1T1C

FeRAM was discussed by the size dependence of MFM, and sufficient read voltage margin will be obtained at 0.065 μm^2 capacitor area, which is good agreement with the estimation. Finally, to investigate the feasibility of a memory window that accounts for the capacitance distribution of the MFM, Monte Carlo simulations was applied for the experimental results to estimate a memory window in Mbits at the 40 nm CMOS technology node. As a result, more than 140 mV of memory window can be achieved by MFM area between 0.11 to 0.14 μm^2.

In Chapter 6, the dependence of reliability on the $Hf_{0.5}Zr_{0.5}O_2$ thickness was investigated to improve the cycling tolerance of hard breakdown and reduce an operating voltage using 1T1C FeRAM for the first time. Furthermore, fatigue and its recovery of the 1T1C FeRAM memory were investigated to confirm the uniformity under practical memory array operation. Fundamental study for the ferroelectric and dielectric properties between 5, 8 and 10 nm thick $Hf_{0.5}Zr_{0.5}O_2$ were investigated using large single capacitor, indicating that 8 nm thick sample had the largest remanent polarization and higher breakdown voltage with low leakage in three samples. Memory array performance of the 64 kbits 1T1C FeRAM with 8 nm thick $Hf_{0.5}Zr_{0.5}O_2$ was confirmed that array operation at 2.0 V and 16 ns were demonstrated experimentally, which was lower than 10 nm thick HZO. Cycling tolerance of hard breakdown of the 1T1C FeRAM memory array revealed no bit error count during 10^8 cycles at an accelerated operating voltage of 3.5 V and an operating speed of 100 ns. The 1 ppm Raw Bit Error Rate at 2.0 V, 100 ns, and 85° C operation was predicted to be > 10^{15} cycles, based on the dependence of time to breakdown on the applied voltage. Fatigue and recovery operations of the 1T1C FeRAM memory array were investigated for the first time. The memory window was decreased post 2.0 V,100 ns for 10^8 cycles, but was recovered by applying higher stress at 2.8 V,100 ns for 10^8 cycles. During fatigue and recovery phases, no degradation of the ΔV_{BL} distributions was obtained, indicating that charge trapping and domain de-pinning in HZO was uniformly occurred.

In conclusion, this technology with planer-type capacitor under bitline structured 1T1C FeRAM can be a candidate for edge IoT application for advance technology node and should encourage the mass production of HfO_2-based 1T1C FeRAM, which has been at the research level until now.

備考 ： 論文要旨は、和文 2000 字と英文 300 語を 1 部ずつ提出するか、もしくは英文 800 語を 1 部提出してください。

Note : Thesis Summary should be submitted in either a copy of 2000 Japanese Characters and 300 Words (English) or 1copy of 800 Words (English).

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