論文 / 著書情報
Article / Book Information

題目(和文)	
Title(English)	Area-Efficient and Power-Efficient CMOS Phased-Array Beamformers for High-Data-Rate Communications
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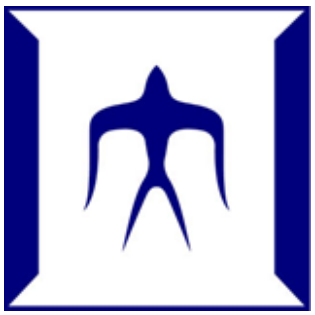
出典(和文)	学位:博士(学術), 学位授与機関:東京工業大学, 報告番号:甲第12500号, 授与年月日:2023年6月30日, 学位の種別:課程博士, 審査員:岡田 健一,廣川 二郎,阪口 啓,伊藤 浩之,白根 篤史,山尾 泰
Citation(English)	Degree:Doctor (Academic), Conferring organization: Tokyo Institute of Technology, Report number:甲第12500号, Conferred date:2023/6/30, Degree Type:Course doctor, Examiner:,,,,,
学位種別(和文)	博士論文
Type(English)	Doctoral Thesis



Area-Efficient and Power-Efficient CMOS Phased-Array Beamformers for High-Data-Rate Communications

by

Zheng Li

A Ph.D. dissertation submitted in partial satisfaction of the requirements for the degree of

Doctor of Philosophy

in

Department of Electrical and Electronic Engineering

in the

Graduate School of Engineering

of

Tokyo Institute of Technology

Supervised by

Prof. Kenichi Okada

Summer 2023

To my family,

Acknowledgment

The five and half years doctoral career at Tokyo Tech has been an incredible journey and a precious treasure. Pursuing a Ph.D. can be very challenging. This thesis not only stands on my effort for hard work but also represents the generous help and support from so many people. I am very grateful and honored to be a member of Okada Lab. I would like to express my gratitude to each of them with my sincerest thanks.

First of all, I would like to thank my supervisor Prof. Kenichi Okada. This work would not be possible without his support and guidance. The research is not always achieved smoothly, and the failure can sometimes be frustrating. Prof. Okada always encourages me and inspires me during discussions, even though he has a tough schedule. He is full of knowledge and passion for both scientific research and life. I would like to thank Prof. Okada for being my navigator and allowing me to seize my career direction.

I would also like to thank Prof. Akira Matsuzawa. Prof. Matsuzawa is stringent in seminars and academic discussions. His comments are always sharp and helpful, and he can point out the core issues. At the same time, he is very gentle and amiable in daily life. Even though I didn't spend a long time working with Prof. Matsuzawa due to his retirement, I was still invited together with the lab members to enjoy the friendly parties in his house. He is lovely and willing to share interesting sees and hears, which broaden our horizons and bring more fun.

I would like to say thanks to Prof. Atsushi Shirane. Prof. Shirane is very easy going, and the conversations with him are always happy and relaxing. He is also in charge of the tape out and measurement plans for the whole lab. Thanks for his contribution to the lab.

Special thanks to Prof. Jian Pang, the 5G group leader. We have worked together for over five years and spent too many sleepless nights for the tape out. He is a very talented researcher and can often put up with some genius ideas. The technical discussions with him are productive and valuable.

I would like to express my gratitude to the Ph.D. defense committee members: Prof. Jiro Hirokawa, Prof. Kei Sakaguchi, Prof. Hiroyuki Ito, and Prof. Yasushi Yamao for spending their precious time examining my dissertation and taking part in my final presentation. Sincerely thank them for their valuable comments and suggestions to make this

thesis more substantial and meaningful.

I would like to say thanks to our secretaries team: Yoshino Kasuga, Makiko Tsunashima, Ayumi Okubo, and Prof. Hiroyuki Sakai. They are the indispensable characters of the lab and keep the lab operating in order. Their jobs cover the routines and trifles of our daily life. Their patient explanations and reminders greatly facilitate our study and life. Thanks for their constant help.

I would like to appreciate the help from my seniors and researchers: Zheng Sun, Rui Wu, Yun Wang, Bangan Liu, Hanli Liu, Yuncheng Zhang, Wei Deng, Ning Li, and Kiyoshi Yanagisawa. Both of them are full of experience, whether in circuit design or measurement. The talk with them can inspire me to find different thinking perspectives. The time spent with them was enjoyable, greatly enriching my life in Japan.

Also, I would like to thank our 5G group members: Yi Zhang, Zixin Chen, Zhongliang Huang, Xueting Luo, Xiaofan Gu, Joshua Alvin, Weichu Chen, Yamazaki Yudai, Qiaoyu Wang, Peng Luo, MinZhe Tang, Yijing Liao. This work has brought together the efforts of everyone, and I really enjoy the team's cooperation with them. Thanks for sharing their time with me, and I hope they all have a bright future. Besides, I want to thank all the lab members for their companionship over these five and half years. All of them make life more vigorous and fantastic.

Finally, I would like to express my sincerest thanks to my parents. Their love and support will always be my strongest motivation.

Abstract

The 5G and next-generation wireless communications, taking advantage of tremendous millimeter-wave band resources, bring in extremely high data rate with ultra-low latency. The increased free-space path loss and high peak-to-power ratio modulated signals demand high-performance phased-array systems. This thesis focuses on the design of area-efficient and power-efficient CMOS phased-array beamformers for high-data-rate communications. The neutralized bi-directional technique is utilized to realize the area-efficient element design. The phased-array system with the cross-polarization leakage canceller is configured in dual-polarized multiple-in-multiple-out to improve the data rate. Both the digital pre-distortion and Doherty techniques are applied in the phased-array to improve power efficiency. While the inter-element mismatches introduced by the Doherty technique due to the PVT variations limit the efficiency enhancement. An inter-element mismatch compensation technique with the shared lookup table is proposed for improving the DPD performance in Doherty phased-array systems. Around 3-dB improvement is achieved for both Error Vector Magnitudes and Adjacent Channel Leakage Ratios with the proposed compensation.

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Chapter 1

Introduction

1.1 Evolution of Cellular Technologies

During the past decades, wireless communication technology has experienced rapid development and truly changed the method of information transfer in the world. Fig. 1.1 illustrates the evolution of cellular technologies since the first-generation (1G) cellular was adopted. The 1G was first deployed in 1981 based on the analog frequency-modulated (FM) technique, supporting only voice communications. The digital modulation technique was implemented in the second generation (2G) cellular systems in 1990, and the essential short message service (SMS) emerged. Since the first demonstration of the third-generation (3G) cellular in 2001, wireless communication has ushered in explosive development with various data services. According to this trend, a new mobile generation is almost proposed every ten years. Wireless communication has become an indispensable part of people's lives; even a distance of thousands of miles is no longer a barrier. At the same time, the number of wireless devices is still growing significantly, which results in ever-increasing data traffic. The exploration for extremely high data-rate wireless communication with ultra-low latency remains an endless desire. The fifth-generation (5G) new radio (NR) operation frequency is extended towards the millimeter-wave (mm-wave) bands. Substantial bandwidth resources are available at the mm-wave bands, which means a higher communication speed than the sub-6-GHz bands. Now we are in the era of 5G, the study of this thesis focuses on new opportunities and challenges.

1.2 Trend of mm-wave Process

The appropriate manufacturing process is indispensable for realizing mm-wave communications. The evolution of the mm-wave process is briefly summarized in Fig. 1.2. In

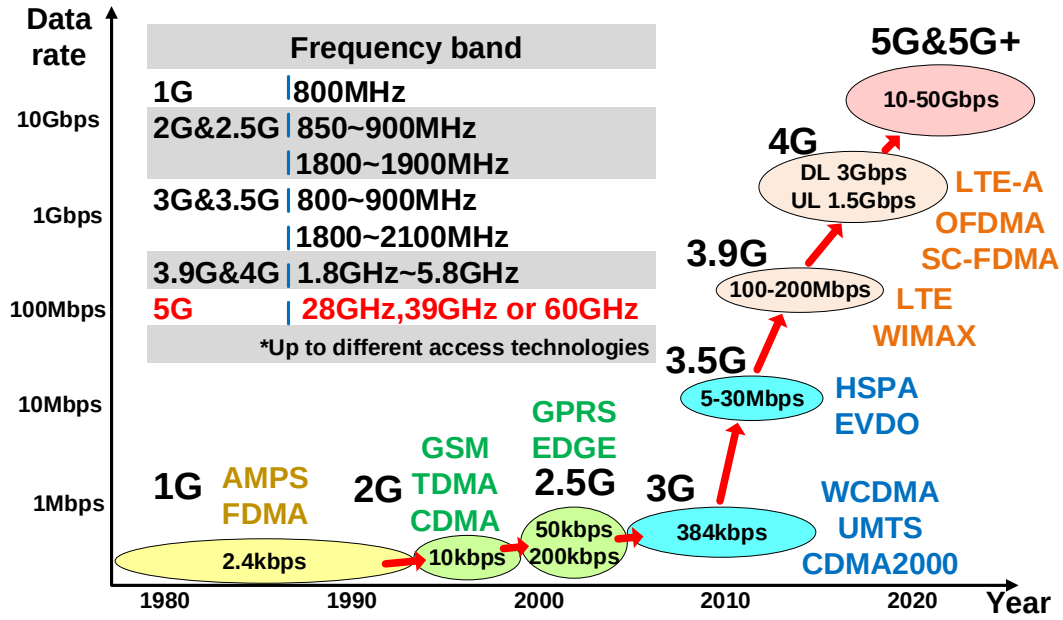

Figure 1.1: Evolution of Cellular Technologies.

1959, Jack Kilby of Texas Instruments invented and manufactured the world's first integrated circuit (IC). The reported IC was manufactured by photolithography technology so that numerous devices and metal interconnections could be fabricated after precisely controlled process steps and transferred onto the surface of a single semiconductor material substrate [1, 2]. This means that the electronics industry can manufacture complex circuits economically and reliably and marks the beginning of the integrated circuit era. In 1976, R. S. Pengelly and J. A. Turner reported the first GaAs monolithic microwave integrated circuit (MMIC) amplifier. The single-stage amplifier in a gallium arsenide (GaAs) metal–semiconductor field-effect transistor (MESFET) with a gate length of 1 μm obtained a gain of 7-12dB in the X-band [3]. As the first MMIC circuit in the history of integrated circuits, it has dramatically stimulated the development of GaAs and also the III-V MMIC industries on a global scale. The gallium nitride (GaN) is more suitable for high-power scenarios with limited high-frequency performance. The indium phosphide (InP) process promises excellent high-frequency features with extremely high gain cut-off frequency f_{max}. Compared with silicon-based technologies, the III-V process is still at a high manufacturing cost, and the incompatibility with the silicon-based digital block is also a drawback.

The silicon-based complementary metal–oxide–semiconductor (CMOS) process scaling, along with Moore's Law, allows the use of high-performance mm-wave IC. Designing mm-wave front ends in the CMOS process has many advantages. The high integration

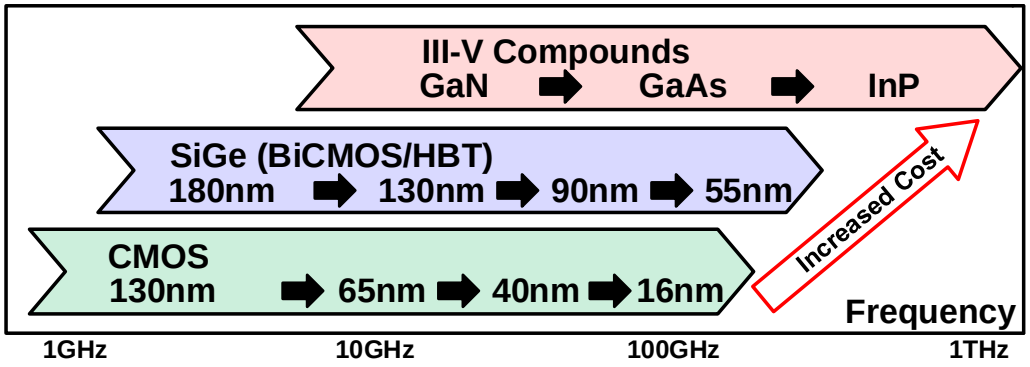

Figure 1.2: Evolution of mm-wave process.

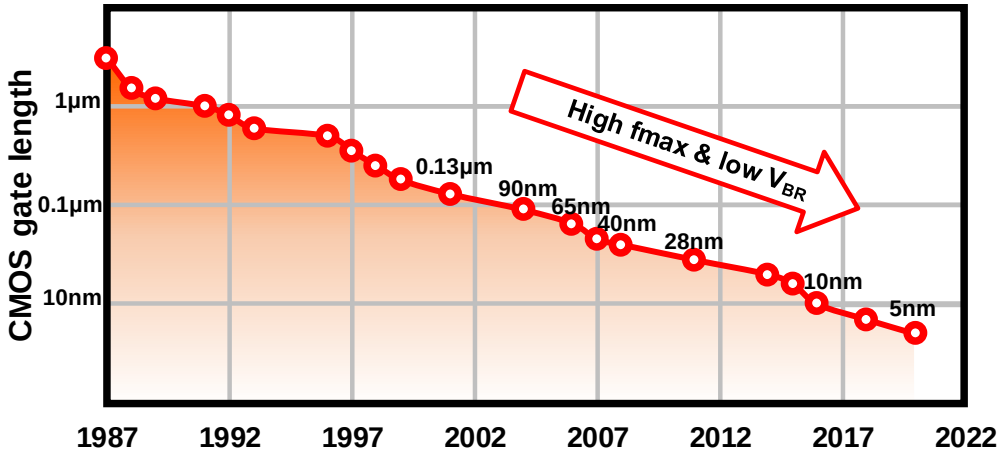

Figure 1.3: Scaling trend of CMOS technology.

with digital processing circuits enables the design of novel mm-wave transceivers with direct digital modulation schemes. This reduces system complexity and power consumption and avoids high-speed digital interfaces between digital chips and front-end chips implemented with III-V technology. The CMOS platform also features a low manufacturing cost, which is well suited for the exponential growth of the wireless communication market for consumer applications. In Fig. 1.3, the scaling trend of CMOS technology is introduced [4]. Its f_{max} is increased along with the process scaling. However, the transistor breakdown voltage is gradually decreased. This thesis selects the cost-effective 65-nm CMOS with more than 300-GHz f_{max} for the following phased-array system design.

1.3 Overview of the Thesis

This thesis mainly discusses the mm-wave CMOS phased-array beamformer designs for low-cost high-data-rate communications. Aiming for the 5G and the next-generation communication requirements, several novel techniques for both building blocks and system architectures are proposed. The proposed phased-array beamformers in this thesis fulfill the targets for area-efficient and power-efficient design. This thesis is structured as follows.

Chapter 2 mainly presents the 5G standard and the related design parameters. Some fundamental knowledge of the phased-array theory and basics is also provided. Along with this, the consideration and requirements for 5G and next-generation communications are well discussed. The prior arts of the phased-array architecture or key components with state-of-art performance are briefly reviewed. The limitation of the existing techniques towards the design challenges is analyzed, which is the critical point of this thesis.

Chapter 3 presents the proposed high-performance bi-directional circuits. These building blocks are the essential parts in the area-efficient beamformer design. The bi-directional core is analyzed from the differential capacitive neutralized PA architecture. The unbalanced neutralized bi-directional PA-LNA serves as the first stage of the front end, realizing a high power-added efficiency (PAE) with a half-reduced chip size. The Doherty technique combines the bi-directional technique to enhance the back-off power efficiency further. To minimize the package capacitive loss, a wafer-level chip scale package is co-designed with the bi-directional Doherty PA-LNA. Besides, the dual-polarized aperture-coupled antenna is implemented, fitting the narrowed antenna pitch and the increased operating frequency. The updated active phase shifter (PS) utilizing the bi-directional core is also introduced, which provides better PVT characteristics. A passive mixed-type PS is demonstrated at the end of this chapter.

Chapter 4 presents the proposed phased-array beamformer designs. The proposed beamformers are configured in DP-MIMO architecture to improve the data rate. A cross-polarization cancellation technique is introduced to minimize the performance degradation of the cross-polarization leakage.

Chapter 4 also analyzes the implementation of digital pre-distortion (DPD) in phased-array systems. The influence of inter-element mismatch on the DPD linearization degradation is discussed. An inter-element mismatch compensation technique improves the DPD performance over PVT variations. The inter-element mismatch compensation proves significant through simulation and measurement, especially with the Doherty technique. The 64-element 16-IC beamformer module is demonstrated at the end of this chapter. With the proposed techniques, excellent array performance is achieved.

Finally, the conclusion and future work of this research are presented in chapter 5.

Chapter 2

CMOS Phased-Array Design Challenges

2.1 Introduction

The 5G technology has three sets of use cases defined as enhanced mobile broadband (eMBB), ultra-reliable and low latency communication (URLLC), and massive machine type communication (mMTC). In recent years, with the rapid development of mobile communications, 5G frequency range 1 (FR1) frequency band resources located at sub-6-GHz bands are extremely congested, together with the existing 3G, 4G, Wifi, and Bluetooth bands [5]. With the merit of abundant frequency resources in millimeter-wave bands, 5G new radio (NR) Frequency Range 2 (FR2) promises a high data rate and low communication latency. As shown in Fig. 2.1, the 5G enhanced Mobile Broadband (eMBB) scenario even supports over 10-Gb/s throughput among massive wireless terminals [6]. The 5G NR FR2 spectrum allocation is illustrated in Fig. 2.2. In this thesis, the phased-array beamformer designs are based on the 5G NR 28GHz n257 (26.5GHz-29.5GHz) and 39GHz n259 (39.5GHz-43.5GHz) and n260 (37.0GHz-40.0GHz) bands. The following part of this chapter will introduce the requirement for the 5G standard and also the challenges for phased-array design. This chapter will also elaborate on some fundamental knowledge of the phased-array theory and basics for a better understanding of the following discussions. A brief description of the previously reported techniques will be given at the end, together with the existing issues.

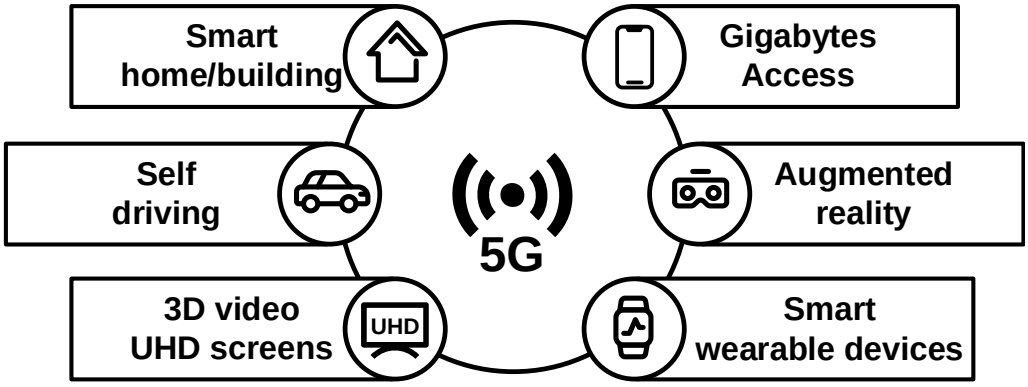

Figure 2.1: 5G enhanced mobile broadband usage scenarios.

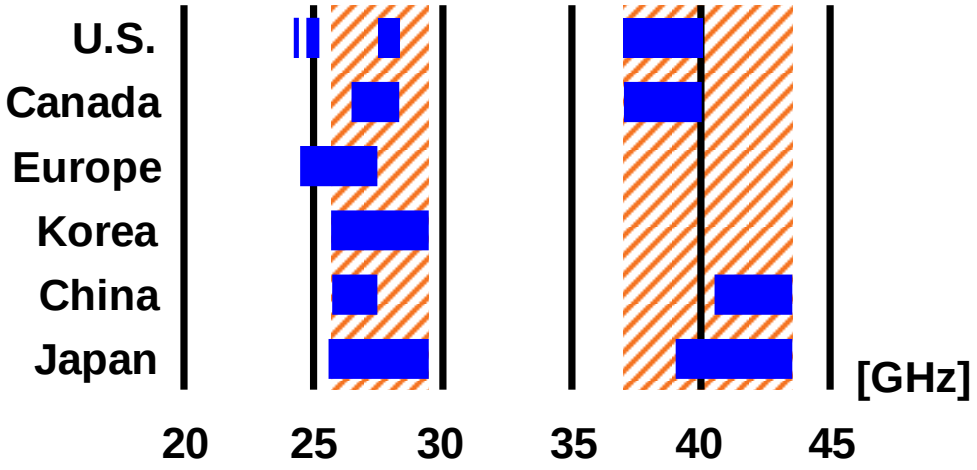

Figure 2.2: 5G NR FR2 Spectrum Allocation.

2.2 Features of 5G NR Cellular Network

2.2.1 Beamforming for Free-Space Path Loss

As mentioned at the beginning of this chapter, the 5G NR communication takes advantage of the extension towards the millimeter-wave band. In return, it will also suffer from the intrinsic shortcoming of the millimeter-wave band. Compared with the sub-6-GHz bands, the over-the-air propagation loss of the 5G FR2 bands is drastically increased. The free-space path loss (FSPL) is used to define the propagation loss, and it can be calculated in decibels by the following equation

$$FSPL(\text{dB}) = 20\log_{10}(d) + 20\log_{10}(f) + 20\log_{10}(\frac{4\pi}{c}) \tag{2.1}$$

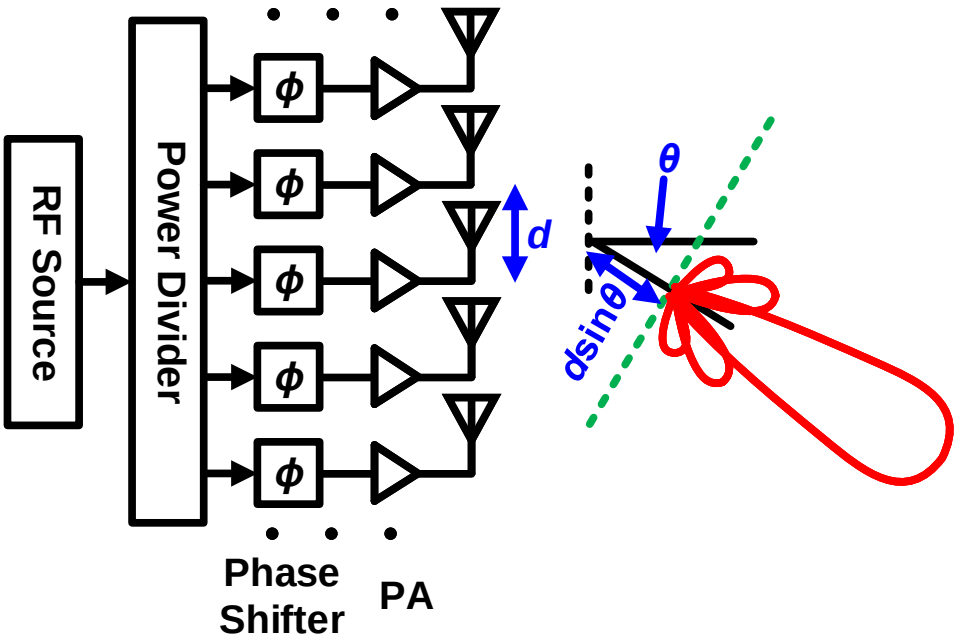

Figure 2.3: Uniform linear TX-mode phased-array system.

where d, f, and c represent the communication distance, operation frequency, and the speed of light, respectively. It's easier to calculate that a 100-m electromagnetic broadcasting will suffer from over 100-dB FSPL at 28GHz. And a 3-dB more FSPL increases at 39GHz compared with the 28-GHz case.

Limited by the increased FSPL, the beamforming technique based on large-scale phased-arrays is mandatory to reach a better signal-to-noise ratio (SNR) over long-distance communication. A phased-array system is composed of multiple beamformer elements. Each beamformer element has its antenna and PS to control the phase of the input or output signal independently. Antennas are placed in various array patterns, the linear arrays and rectangular arrays are commonly used for simplicity. A typical $\lambda/2$ antenna pitch is placed to realize the Nyquist sampling [7]. Fig. 2.3 illustrates the basic principle of a linear phased-array system. Considering only the adjacent two transmitters (TXs) for simplicity, each antenna radiates the individual signal. In an arbitrary direction θ, due to the physical distance between these two antennas, a phase difference between signals from these two elements occurs. At the far-field area, the phase difference can be approximated as follows

$$\phi = \frac{2\pi d}{\lambda}\sin\theta \tag{2.2}$$

where d and λ denote the distance between elements and the wavelength, respectively.

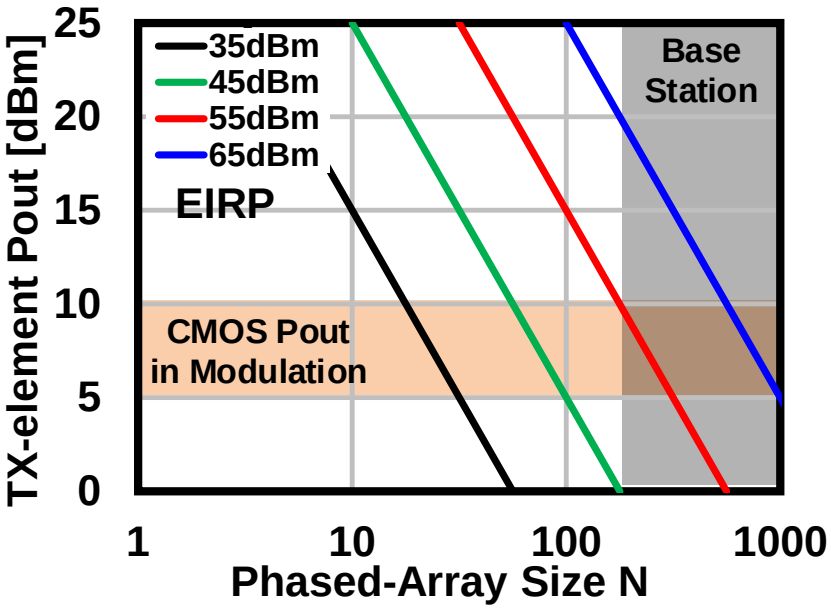

Figure 2.4: EIRP calculation based on TX-element Pout and the number of elements.

Due to this phase difference, if the antennas are driven with the same phase, the electronic field generated by these two antennas is not added in phase in this direction, resulting in a degraded amplitude. However, phase shifters within the TX can easily compensate for this phase difference, generating the output signals with a phase difference of $-\phi$. The in-phase spatial combining with a beam angle of θ twice the magnitude compared with a single TX. Because energy is proportional to the square of the electronic-field amplitude, the energy delivered in this direction is boosted by a factor of 4, which means 6-dB larger than a single TX case. This conclusion can be extended to the N_{TX}-element phased-array system, the far-field energy at the beam pointing direction is increased by N_{TX}^2. The corrsponding array gain $G_{\mathrm{TX\_ARR}}$ in decibel is equal to $20\log_{10}N_{\mathrm{TX}}$. Similar to the TX array, multiple receivers (RXs) can also be configured into the N_{RX}-element RX array to achieve an array gain of $G_{\mathrm{RX\_ARR}}$.

By utilizing the beamforming technique, mm-wave communication is capable of covering a long distance with better SNR. The evaluated the radiated power level of the phased-array, the effective isotropic radiated power (EIRP). As for an ideal phased-array, EIRP can be calculated by the following equation

$$EIRP(\mathrm{dBm}) = P_{\mathrm{TX}}(\mathrm{dBm}) + G_{\mathrm{TX\_ANT}}(\mathrm{dB}) + G_{\mathrm{TX\_ARR}}(\mathrm{dB}) \tag{2.3}$$

The parameters P_{TX} and $G_{\mathrm{TX\_ANT}}$ represent the single element output power and the antenna gain, respectively. Fig. 2.4 shows the calculated EIRP based on the generalized 5G

single beamformer element output power satisfying the SNR requirement. The required SNR_{Required} limits the achievable output power as demonstrated below

$$\begin{aligned} P_{\text{TX}}(\text{dBm}) > SNR_{\text{Required}}(\text{dB}) - G_{\text{TX\_ANT}}(\text{dB}) - G_{\text{TX\_ARR}}(\text{dB}) - G_{\text{RX\_ANT}}(\text{dB}) \\ -G_{\text{RX\_ARR}}(\text{dB}) + FSPL(\text{dB}) + NoiseFloor(\text{dBm}) \end{aligned} \tag{2.4}$$

where the $G_{\text{RX\_ARR}}$ represents the RX array gain. According to this equation, to cover a 300-m communication distance, over 256-element phased-array is required with a higher than 55-dBm EIRP. The large-scale array size not only increases the total system power consumption but also means a huge manufacturing cost. Furthermore, a complicated system design is inevitable, such as a high-order power divider and combiner, a digital block with massive controlling registers, and well-designed power supply paths. The area-efficient design is an attractive research topic for reducing system complexity and cost.

2.2.2 Phased Array Implementation

As mentioned in section 2.2.1, 5G phased-array systems require high-density antenna arrays for beamforming, which can pose challenges in size and cost. One way to address this is to scale down the antenna pitch, which refers to the spacing between individual antenna elements, to achieve higher antenna density in a given area. Scaling down the antenna pitch allows more antennas to be packed into a smaller area, leading to higher spatial resolution and better beamforming performance. However, there are also some challenges associated with this approach. One potential issue is the increased complexity of the antenna design and fabrication process, which can increase the cost and time required for manufacturing. Another important issue to consider is that implementing a phased-array module becomes more challenging as the antenna pitch is scaled down closer to the size of the chip. Fig. 2.5 shows the antenna pitch scaling down with the increasing operating frequency. The typical $\lambda/2$ antenna pitch for 28GHz and 39GHz bands are 5mm and 4mm, respectively. Thus, the antenna pitch limits the beamformer chip size, so area-efficient beamformer design is in urgent demand. Fig. 2.6 demonstrates the prototype of the 5G NR phased-array implementations. The single-polarized phased-array module can be referred to Fig. 2.6(a), where the ICs are mounted with the spacing of typical $\lambda/2$ antenna pitch and the symmetrical RF power divider is required. While the dual-polarized phased-array shown in Fig. 2.6(b) is more complicated than the single-polarized case, two pairs of the dedicated designed RF dividers are mandatory, and the spacing for the RF divider interconnections become a constraint issue.

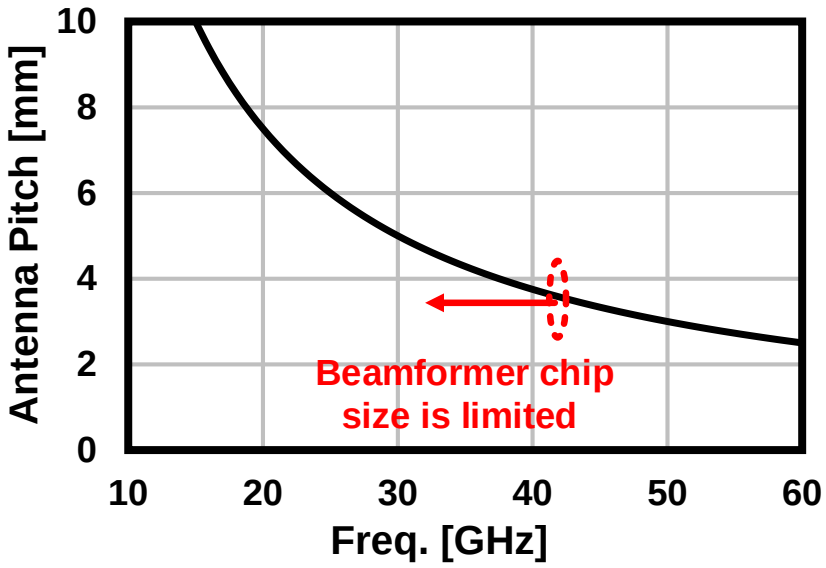

Figure 2.5: Antenna pitch scaling down with the increasing operation frequency.

2.2.3 High-Order High-PAPR 5G Signals

The 5G-compliant signals are modulated in Orthogonal Frequency Division Multiple Access (OFDMA) modes. The OFDMA featured in the robust communication wireless scheme for multiple users derives from the Orthogonal Frequency Division Multiple (OFDM). The OFDMA presents a good performance in the presence of multipath due to its multi-tone carriers and synchronization prefix.

Quadrature Amplitude Modulation (QAM) is also utilized to enhance the data rate. The QPSK, 16-QAM, 64-QAM, and 256-QAM represent the 2-bit, 4-bit, 6-bit, and 8-bit amplitude modulation. The high-order modulation brings in a high data rate and suffers from severe nonlinearity degradation. The higher TX linearity means the higher available EIRP. As shown in Table 2.1, The Third Generation Partnership Project (3GPP) has stipulated the requirement for Error Vector Magnitude in specification 38.101-1 [8].

Furthermore, the 5G OFDMA-modulated signals also perform a higher peak-to-average power ratio (PAPR). Fig. 2.7 shows the concept of PAPR, which is defined as the relation between the signal maximum power P_{PEAK} and its average power P_{AVG}. For an $s(t)$ signal inside a period T, the PAPR can be derived from the following equation

$$PAPR = \frac{P_{\mathrm{PEAK}}}{P_{\mathrm{AVG}}} = \frac{max_{[0,\mathrm{T}]}|s(t)|^2}{\frac{1}{T}\int_0^{\mathrm{T}}|s(t)|^2 dt} \tag{2.5}$$

The PAPR of cellular standards is given in Table 2.2. The 5G OFDMA-mode 64-QAM

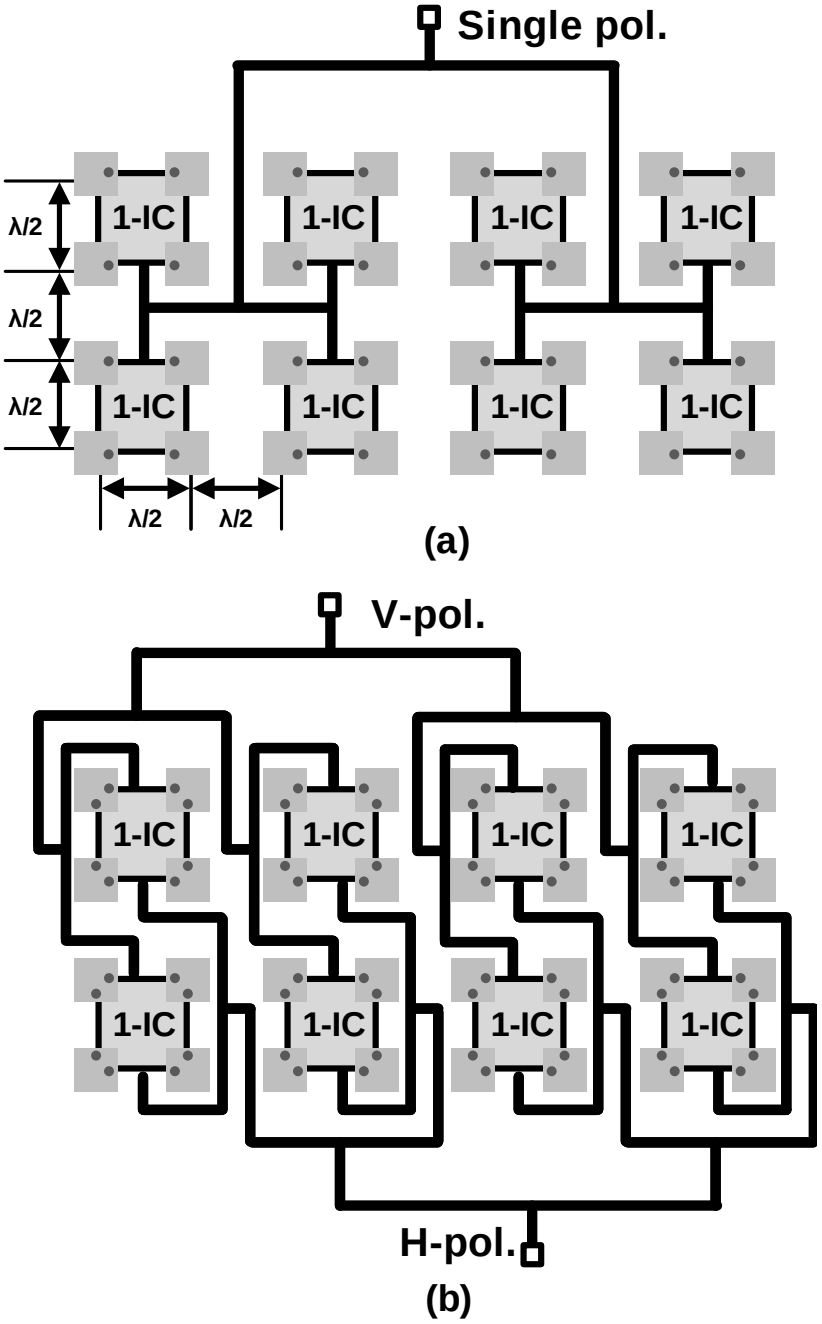

Figure 2.6: 5G NR phased-array implementations: (a) single-polarized phased-array module and (b) dual-polarized phased-array module.

signal reaches an 11.2-dB PAPR, large power back-off (PBO) from the saturated output power (Psat) point is required. However, the conventional power amplifier (PA) in the phased-array presents a maximum power-added efficiency (PAE) performance only on the maximum input or output power level. While the PAE at more than 6-dB PBO region

Table 2.1: Requirement for Error Vector Magnitude

Modulation scheme for PDSCH	Required EVM
QPSK	17.5%
16QAM	12.5%
64QAM	8%
256QAM	3.5%

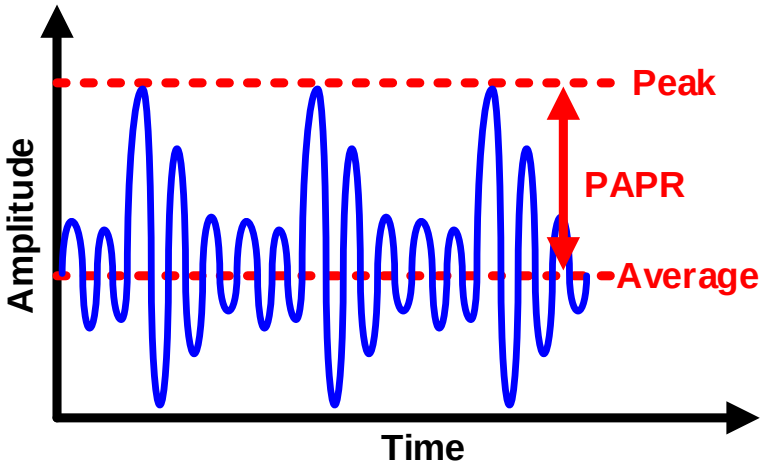

Figure 2.7: Peak-to-average power ratio.

is degraded quickly, severely reducing the system power efficiency.

In a word, the desired phased-array beamformer requires a power-efficient design with high PBO efficiency and linearization techniques.

Table 2.2: Peak-to-Average Power Ratio of cellular standards

Cellular Standard	PAPR
3G WCDMA	3dB
3G HSPA	5-7dB
4G LTE SC-FDMA	6-8dB
5G OFDMA 64QAM	11.2dB

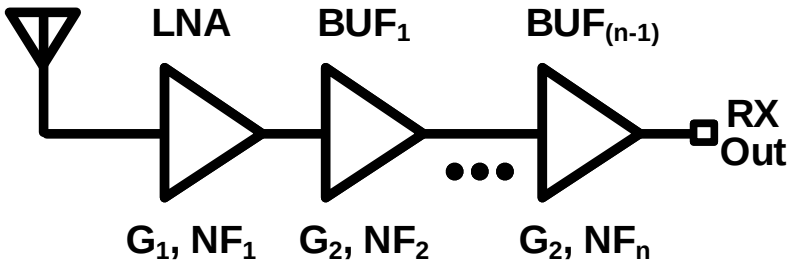

Figure 2.8: Antenna followed by LNA and RF buffer chains.

2.3 5G Phased-Array System Considerations

To meet the 5G NR cellular network's new features, dedicated design and system considerations of the phased-array systems are required. Similar to the commonly used sub-6-GHz transceivers, the PA and LNA serve as the first stage of the mm-wave front end, directly connecting with the antenna port. The performance of PA and LNA almost determines the whole beamformer system performance. To deliver sufficient output power to the antenna port and compensate for RF power divider distribution loss in the beamformer chip, the cascaded buffer and VGA stages are mandatory. Several design parameters can be a bottleneck of the following system design. As a result, we focus on the most important part of them. Excellent RX noise figure (NF) and TX linearity are desired to achieve the best communication quality.

2.3.1 Front-End Design Parameters

In RX mode, NF and SNR are critical parameters that determine the quality of the received signal. NF represents the amount of noise the RX adds to the received signal. At the same time, SNR measures the signal's strength compared to the background noise level. A lower NF and higher SNR result in a better-quality signal, allowing for more reliable and accurate communication. Therefore, understanding these parameters' concepts and how to measure and optimize them is crucial for designing and operating effective wireless communication systems. To quantify how noisy the circuit is, the NF can be defined as follows

$$NF = \frac{SNR_{\text{in}}}{SNR_{\text{out}}} \tag{2.6}$$

which can be rewritten as

$$NF[dB] = 10log_{10}(NF) \tag{2.7}$$

As for a noiseless circuit, the output SNR should equal the input SNR, meaning NF is 0dB in the ideal case. While due to the non-ideal characteristics of the transistors and lossy matching networks, the NF for 5G phased-array systems is usually around 5dB. Considering the NF with many cascaded stages in the RX chain, as shown in Fig. 2.8, the total NF can be calculated as

$$NF_{\text{total}} = 1 + (NF_1 - 1) + \frac{NF_2 - 1}{G_1} + \frac{NF_2 - 1}{G_1 G_2} + \cdots + \frac{NF_{\text{n}}}{G_1 G_2 \cdots G_{\text{n}}} \tag{2.8}$$

where NF_{m} means the NF of the m^{th} amplifier and G_{m} means the available power gain of the m^{th} amplifier, respectively.

While as for the TX mode, linearity is a crucial parameter that directly impacts the quality and reliability of the transmitted signal. TX linearity measures how accurately the transmitter converts the input signal to output without introducing distortion or non-linearities. If the transmitter introduces non-linearities or distortion, the transmitted signal can interfere with other signals, creating noise or reducing the system's overall performance. Furthermore, non-linearities in the transmitter can cause intermodulation distortion, which can create unwanted signals that can interfere with other signals in the communication system. To define the harmonic distortion of a nonlinear system, as shown in Fig. 2.9(a), a single-tone test signal $x(t) = A\cos\omega t$ is applied to the simplified memoryless systems

$$y(t) = \alpha_1 x(t) + \alpha_2 x^2(t) + \alpha_3 x^3(t) + \cdots \tag{2.9}$$

with the single-tone input, the output can be expressed as

$$y(t) = \alpha_1 A\cos\omega t + \alpha_2 A^2\cos^2\omega t + \alpha_3 A^3\cos^3\omega t + \cdots \tag{2.10}$$

$$= \alpha_1 A\cos\omega t + \frac{\alpha_2 A^2}{2}(1 + \cos 2\omega t) + \frac{\alpha_3 A^3}{4}(3\cos\omega t + \cos 3\omega t) + \cdots \tag{2.11}$$

$$= \frac{\alpha_2 A^2}{2} + (\alpha_1 A + \frac{\alpha_3 A^3}{4})\cos\omega t + \frac{\alpha_2 A^2}{2}\cos 2\omega t + \frac{\alpha_3 A^3}{4}\cos 3\omega t + \cdots \tag{2.12}$$

The obtained result comprises several essential components. Firstly, the output contains signals that are the harmonics of the input signal frequency, with amplitudes proportional to the input signal's amplitude raised to the corresponding power. When the input frequency is high, it is easier to suppress these harmonics due to the larger frequency difference between them and the desired signal. Secondly, the fundamental gain is altered by $\alpha_1 A + \alpha_3 A^3/4$. In the CMOS process, where $\alpha_1\alpha_3 < 0$, high input signal amplitudes lead to compression of the fundamental gain. The linearity of system components can be

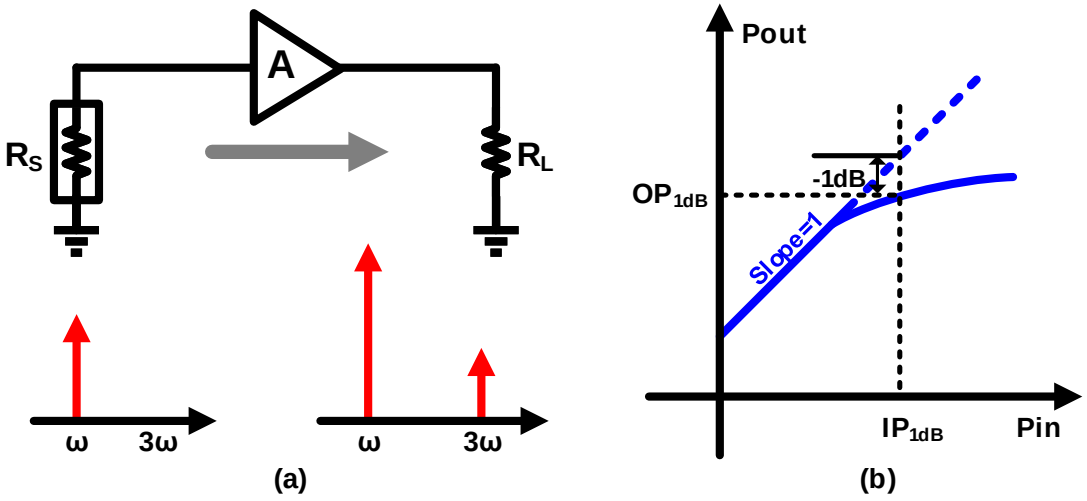

Figure 2.9: (a) Simplified memory-less nonlinear model for single-tone test and (b) its gain compression response.

evaluated using the 1-dB compression point as given in Fig. 2.9, which is the point at which the gain is compressed by 1dB compared to the small signal gain.

The value of the 1-dB compression point can be calculated theoretically by utilizing the coefficients in the above equation. This calculation equates the gain to 1dB less than the ideal linear gain α_1. Thus, the following equation can be used to calculate the 1dB compression point

$$A_{1\text{dB}} = \sqrt{0.145\left|\frac{\alpha_1}{\alpha_3}\right|} \tag{2.13}$$

In more complex application scenarios, a frequency-spanning modulated signal is often used for data streaming. This modulated signal can be considered a collection of multiple tones, which can cause intermodulation effects within the system. Intermodulation occurs when two or more signals with different frequencies are combined in a non-linear system, creating additional frequencies known as intermodulation products. To evaluate a modulated signal, it is important to analyze the intermodulation products and identify sources of distortion that may degrade signal quality. By simply applying the two-tone input signals with a given frequency spacing and measuring the resulting intermodulation products, it is possible to obtain insights into the system's linearity and distortion characteristics, which can be used to optimize performance and improve signal quality. As demonstrated in Fig. 2.10(a), by replacing the two-tone signal $x(t) = A_1\cos\omega_1 t + A_2\cos\omega_2 t$ into the Equation 2.9, the output results can be derived as follows

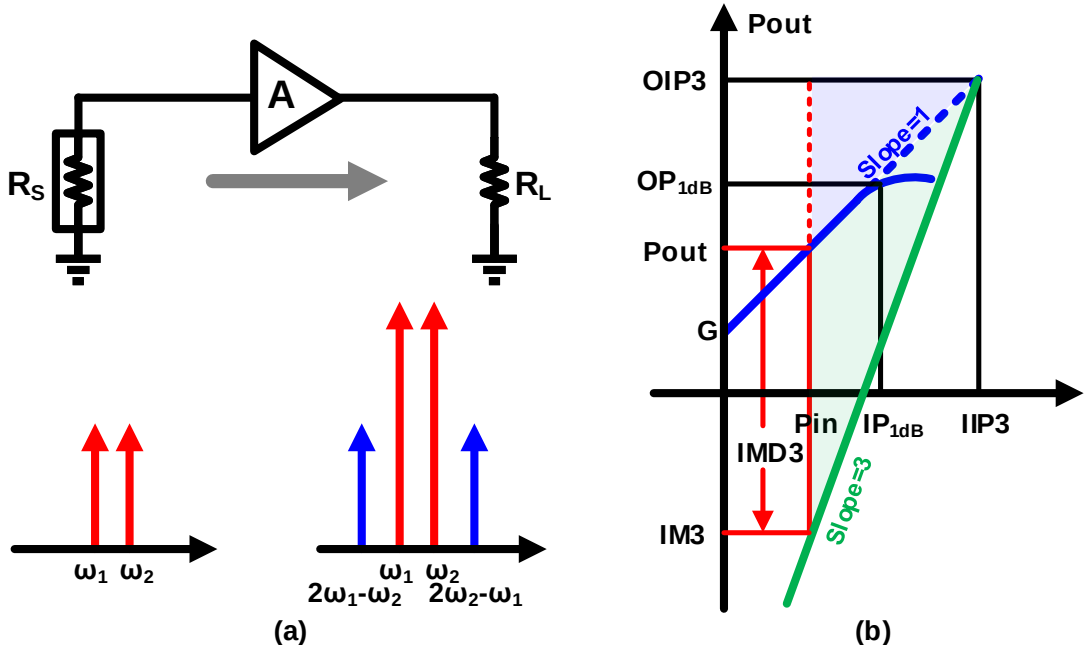

Figure 2.10: (a) Simplified memory-less nonlinear model for two-tone test and (b) its intermodulation response.

$$y(t) = \alpha_1(A_1\cos\omega_1 t + A_2\cos\omega_2 t) \tag{2.14}$$

$$+ \alpha_2(A_1\cos\omega_1 t + A_2\cos\omega_2 t)^2 \tag{2.15}$$

$$+ \alpha_3(A_1\cos\omega_1 t + A_2\cos\omega_2 t)^3 + \cdots \tag{2.16}$$

through the use of standard trigonometric identities, the two relevant distortion terms with frequencies near ω_1 and ω_2, that is

$$\frac{3\alpha_3 A_1^2 A_2}{4}\cos(2\omega_1 - \omega_2)t \tag{2.17}$$

and

$$\frac{3\alpha_3 A_1 A_2^2}{4}\cos(2\omega_2 - \omega_1)t \tag{2.18}$$

These two terms are defined as third-order intermodulation (IM3) products. All other terms are irrelevant, as they have frequencies far from ω_1 and ω_2. In practice, they would be suppressed by the transmit antenna frequency response and, therefore, effectively not transmitted. The IM3 is commonly referred to as the third-order intermodulation dis-

tortion (IMD3). The IMD3 is highly related to the system adjacent channel leakage ratio (ACLR) performance. The IM3 and IMD3 are demonstrated conceptually in Fig. 2.10(b). The third-order intercept point (IP_3) is defined as the cross-point of the linear extension of the fundamental output and IM3 product. And the IIP_3 can be calculated by equating the fundamental and IM3 amplitudes

$$|\alpha_1 A_{\text{IIP3}}| = \left|\frac{3}{4}\alpha_3 A_{\text{IIP3}}^3\right| \tag{2.19}$$

thus

$$A_{\text{IIP3}} = \sqrt{\frac{4}{3}\left|\frac{\alpha_1}{\alpha_3}\right|} \tag{2.20}$$

an important relationship between IIP_3 and P1dB can be derived from the follows, which is useful in the ACLR analysis in Section 4.2

$$\frac{A_{\text{IIP3}}}{A_{\text{1dB}}} = \sqrt{\frac{4}{0.435}} \tag{2.21}$$

$$\approx 9.6dB \tag{2.22}$$

Up to now, the key RF front-end design parameters are introduced and analyzed for The key RF front-end design parameters are now introduced and analyzed for RX-mode and TX-mode considerations. These design parameters are extremely useful for the following understanding and system design.

2.3.2 Error Vector Magnitude

Error Vector Magnitude (EVM) is the root mean square (rms) of the error vectors computed and expressed as a percentage of the EVM Normalization Reference. The error vector magnitude is the length of the vector—at the detected symbol location—which connects the I/Q reference-signal vector to the I/Q measured-signal vector. Fig. 2.11(a) shows the calculation of the EVM metric as well as a diagram showing how a single error vector is calculated. According to Fig. 2.11(a), EVM can be calculated by

$$EVM(\%) = 100\% \times \frac{\sqrt{\frac{1}{N}\sum_{n=0}^{N-1} I_{\text{err}}[n]^2 + Q_{\text{err}}[n]^2}}{EVM\ Normalization\ Reference} \tag{2.23}$$

where n and N represent the symbol index and the number of symbols, respectively. I_{err} and Q_{err} are calculated by $I_{\text{ref}} - I_{\text{meas}}$ and $Q_{\text{ref}} - Q_{\text{meas}}$, respectively.

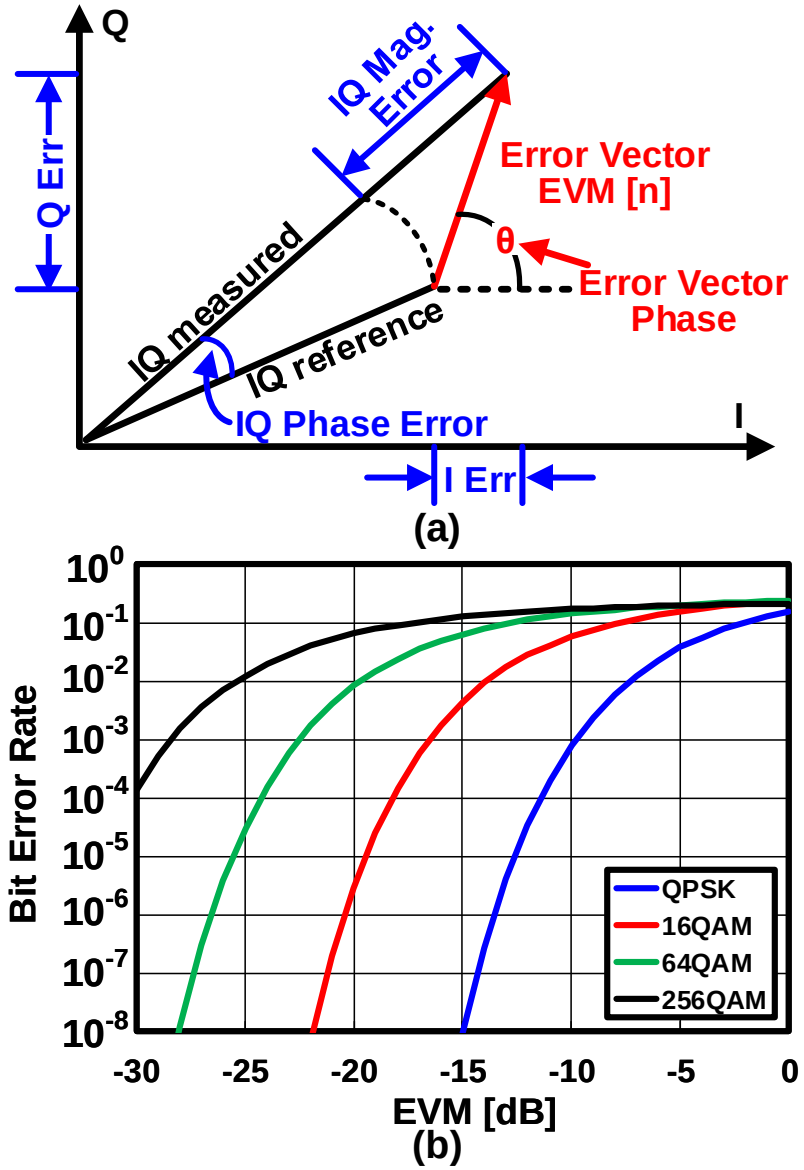

Figure 2.11: (a)The definition of EVM and (b) Required EVM against BER with different modulation schemes.

Considerable spectrum resources could be utilized in the millimeter-wave band to improve the wireless capacity. Complex modulation schemes with higher order, such as 64-QAM and 128-QAM, will also be employed. However, a small enough error vector magnitude (EVM) should be maintained from the transmitter to the receiver for such modulation schemes after the demodulation. Thus, improving the system EVM is one of the most important design challenges for mm-wave transceivers. Increasing the modulation order requires an improvement to the system EVM. Fig. 2.11(b) shows the EVM require-

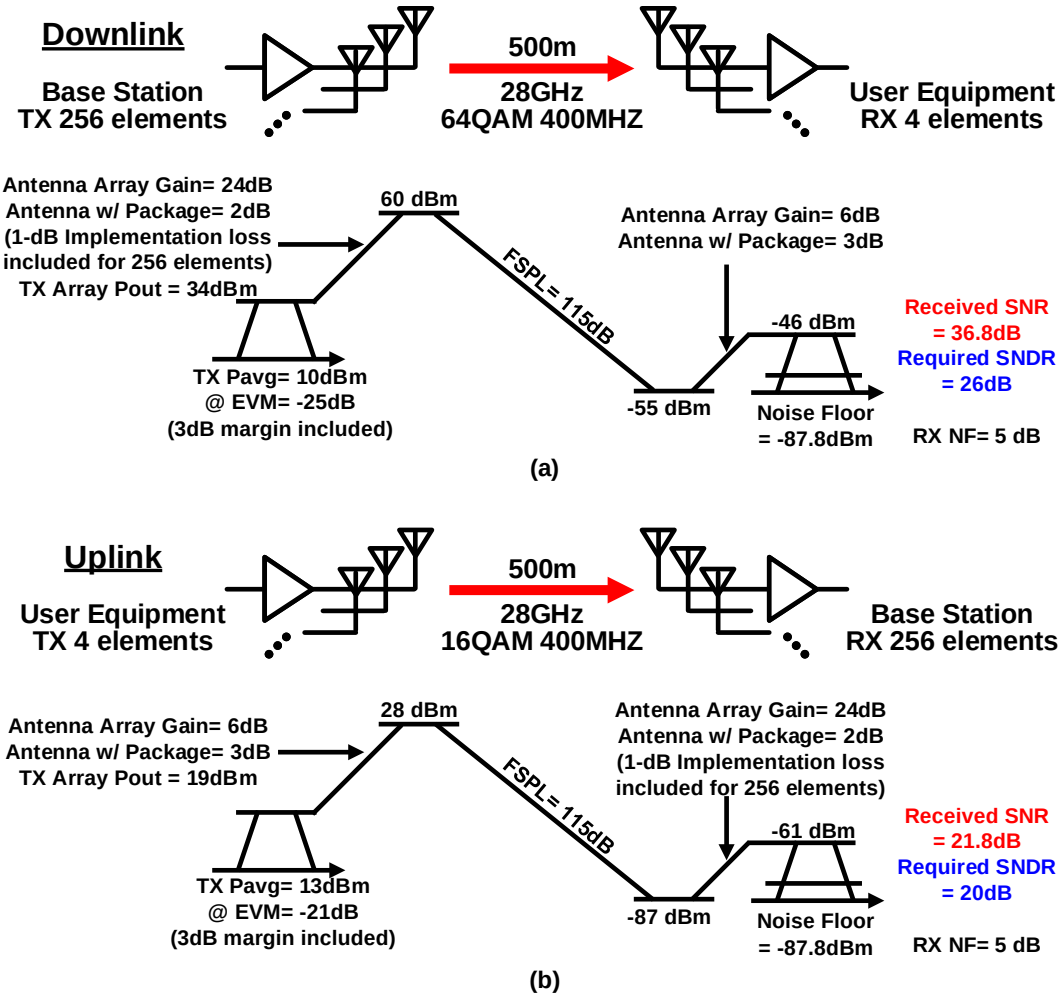

Figure 2.12: Link budget examples for (a) 5G downlink and (b) 5G uplink.

ment against the bit error rate (BER) regarding different modulation schemes. To realize a BER of 10^{-3}, EVMs of -22.5 dB, -25.5 dB and -28.4 dB are required for 64-QAM, 128-QAM and 256-QAM, respectively, through the transmitter to the receiver. Due to limited power and cost budgets, the transceiver design progress becomes extremely challenging. In recent years, the direct-conversion architecture has been widely adopted for mm-wave transceivers. The reduced number of building blocks due to the system's simplicity helps to achieve a compact and low-power system.

System SNDR optimization is very important to millimeter-wave transceivers. The much wider channel bandwidth significantly increases the input noise floor. Taking the 5G NR application mentioned in Chapter 1, for example, a 6-dB noise floor increase could be calculated regarding the 100-MHz channel bandwidth in FR1 and the 400-MHz channel bandwidth in FR2. As a result, to maintain enough transceiver EVM, careful

design considerations and evaluations will be required for the gain level, linearity, and noise figure.

Moreover, the increased requirement on EVM will demand a lower phase noise of the RF phase-locked loop. Usually, baseband carrier tracking circuits can suppress the influence of phase noise. However, the carrier tracking bandwidth will be limited by the sub-carrier spacing for OFDM-mode data transmission. Therefore, stringent phase noise requirements still need to be satisfied. While on the other hand, the phase noise requirement for single-carrier (SC) mode data transmission can be relaxed due to the wider carrier tracking bandwidth.

2.3.3 5G NR Communication Link Budget

The 5G communication link budget is a tool used to determine the minimum power required to achieve the desired level of performance in a wireless communication system. It considers factors such as transmitted power, antenna gain, FSPL, and noise to optimize the network's performance. Higher frequencies used in 5G networks result in higher path loss and more susceptibility to attenuation by obstacles, so higher transmitted power is required. To obtain sufficient 5G communication distance, a large array size is required for a 5G base station (BS) using a CMOS millimeter-wave phased-array transceiver. The 5G NR standard allows a maximum EIRP of 75 dBm100 MHz to the base station and 43 dBm to user equipment (UE). Fig. 2.12 shows link budget examples for a 400-MHz downlink in 64-QAM and a 400-MHz uplink in 16-QAM. The array sizes are 256 for the BS and 4 for the UE. The communication distance is 500 m, corresponding to a line-of-sight (LOS) FSPL of 115 dB at 28 GHz. Usually, the differential topology PA is adopted in the 5G transmitter for larger power delivery.

Within a reasonable power consumption, a single-element transmitter output power of around 10 dBm can be realized for the 64-QAM modulation scheme in the CMOS process. Thus, an array size of over 256 will be required to realize a 60-dBm EIRP. The 60-dBm EIRP is calculated based on the 30-dBm TX array output, 24-dB antenna array gain, and 2-dB single antenna gain with the package, including the implementation loss. In this case, 1-dB implementation loss caused by a 256-element non-ideal antenna array is considered in calculating equivalent single antenna gain. After receiving, assuming a 5-dB RX NF, the downlink maintains SNR over 26 dB with a 10.8-dB margin for the down-conversion and demodulation. Similarly, the uplink from UE to BS can be referred to in Fig. 2.12(b). The 4-element TX EIRP is around 28dBm, with the 13-dBm single-element output power in 16-QAM. Also, the antenna gain with the package, including implementation loss, is around 3 dB due to the much smaller array size. The calculated

SNR of the uplink is over 20 dB, and a 1.8-dB margin is left.

2.3.4 PVT Issue of Phased-Array

Phased-array systems are susceptible to a phenomenon known as the PVT (Process, Voltage, Temperature) issue, which can cause the system to experience errors in beamforming and image quality. The PVT issue arises due to variations in the electronic components of the system, which can lead to variations in the system's phase, voltage, and temperature. In order to make the chip work after fabrication in all the possible conditions, we simulate it at different PVT corners. There are many transistors on the single chip as we are going to lower nodes, and all the transistors in a chip cannot have the same properties. Process variation is the deviation in the parameters of the transistor during the fabrication. During manufacturing a die, the area at the center and the boundary will have different process variations. This happens because layers that will be fabricated cannot be uniform all over the die.

Below are a few important factors that can cause the process variation: the wavelength of the UV light, manufacturing defects, oxide thickness variation, dopant and mobility fluctuation, transistor width, RC variation, channel length, doping concentration, metal thickness, impurity concentration densities, diffusion depths, imperfections in the manufacturing process like mask print and etching. These variations will cause parameters like threshold voltage and threshold voltage depending on parameters like doping concentration, surface potential, channel length, oxide thickness, temperature, source-to-body voltage, and implant impurities.

As we go to the lower process nodes, the supply voltage for a chip will also be less. Let us say the chip is operating at 1.0V. So, this voltage may vary in certain instances. It can go to 1.2V or 0.8V. To take care of this scenario, we consider voltage variation. There are multiple reasons for voltage variation. The current flow over the power grid network causes an IR drop–the Supply noise caused by parasitic inductance in combination with resistance and capacitance. When the current flow through parasitic inductance, it causes the voltage to bounce. The supply voltage is given to any chip externally from the DC source or some voltage regulator. The voltage regulator will not give the same voltage all the time. It can go above or below the expected voltage. Hence, if the voltage changes, it will change the current, making the circuit slower or faster.

The transistor density is not uniform throughout the chip. Some regions of the chip have higher density and switching, resulting in higher power dissipation. Some regions of the chip have lower density and switching, resulting in lower power dissipation. Hence the junction temperature at these regions may be higher or lower depending upon the

density of transistors. Because of the variation in temperature across the chip, it introduces different delays across all the transistors.

The temperature variation concerns the junction and not the ambient temperature. The temperature at the junction inside the chip can vary within a big range, which is why temperature variation must be considered. The delay of a cell increases with an increase in temperature. Nevertheless, this is only true for some technology nodes. For deep submicron technologies, this behavior is contrary. This phenomenon is called a temperature inversion.

The accuracy of phase and gain are essential in controlling the beam direction and suppressing the side lobes. However, these can be affected by the process, the environmental temperature, and the control voltage fluctuation. These factors can cause phase-shift inaccuracy and gain fluctuation and thus leads to the unstable performance of phase shifters. These factors must be considered carefully in the design of the phase shifter. Besides, considering the integration of the multi-path power-combined PAs in the beamformer, the PVT issue will become more severely. The analysis and proposed solution will be illustrated in Chapter 4.

2.4 Prior Arts of 5G Phased-Array Beamformers

Widespread research has been focused on the 5G mm-wave phased-arrays in the past few years [9–30]. The high-performance phased-array system should feature high EIRP for maintaining the link budget and compact system design to adapt to the narrowed antenna pitch.

2.4.1 Antenna Sharing with TRX Switch

One popular solution to reduce the phased-array complexity is to share the same antenna port between the TX and RX paths, as shown in Fig. 2.13. An additional transceiver (TRX) switch is inserted between the antenna port and the PA's output (i.e., LNA's input). The TRX switch is usually realized by $\lambda/4$ transmission lines (TLs) together with the shunt transistors. Some TRX switches were reported with the same principles as the TL-based switch. The TL-based TRX switch is bulky and lossy even at the millimeter-wave band. In general, its insertion loss is high than 1.5dB. This insertion loss directly degrades the TX-mode output power and the RX-mode noise figure (NF).

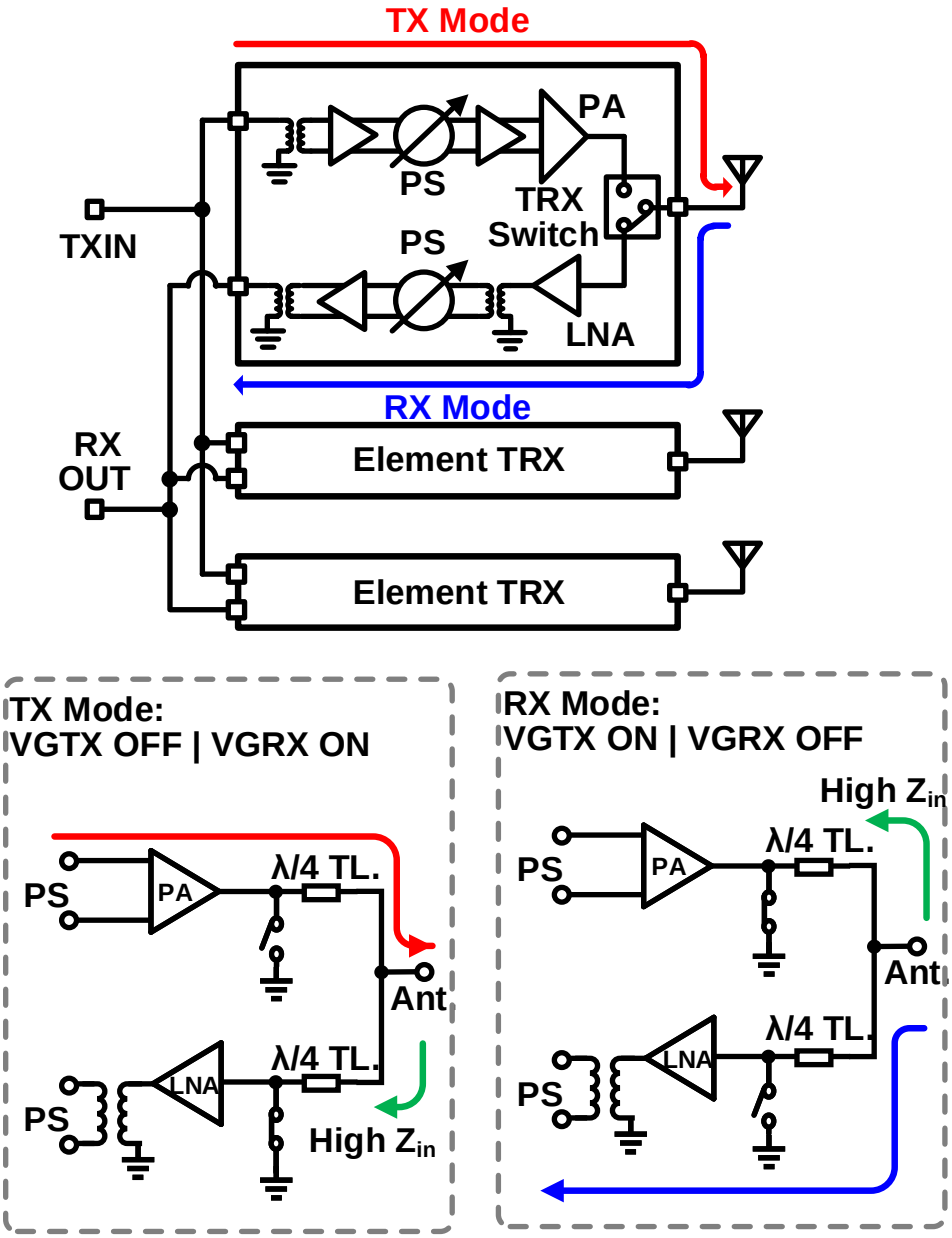

Figure 2.13: Conventional phased-array architecture with antenna sharing.

2.4.2 DP-MIMO Configuration

The multiple-input-multiple-output (MIMO) configuration is also widely utilized, especially in sub-6-GHz communication scenarios. The basic topology of the MIMO system is given in Fig. 2.14. The channel capacity C for ideal MIMO is defined by [31]

$$C = nBW\log_2(1 + SNR/n) \tag{2.24}$$

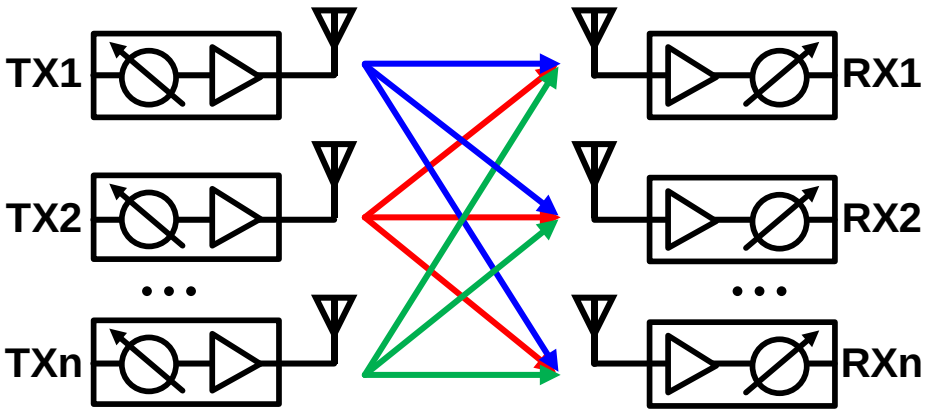

Figure 2.14: Multiple-input-multiple-output configuration.

in this equation, the n is the number of the different data streams, and BW is the available bandwidth of the streaming signal. By transmitting only 2 data streams, the dual-polarized MIMO (DP-MIMO) can be realized together with the dual-polarized antenna. The miniaturized dual-polarized patch antenna is suitable for phased-array integration. The phased-array beamform elements can share an identical design with the orthogonal vertical-polarized (V-pol.) and horizontal-polarized (H-pol.) directions. Like the MIMO system, the DP-MIMO can improve the data rate and reduce the module cost. However, it suffers from channel correlation and desires high channel isolation.

2.5 Power-Efficient Power Amplifiers

In conventional phased-array beamformer designs, the differential PA is a better choice than the two-way single-ended in-phase-combined PA for additional common-mode rejection [32–37]. The biases are usually optimized at class-AB to enhance the AM-AM linearity. The optimization of the class-AB PA is mainly focused on the transformer-based matching networks and the passive power-combiners, improving only the peak power efficiency performance.

As mentioned at the beginning of this chapter, due to the high PAPR of 5G-standard OFDMA-mode modulated signals, the power efficiency of phased-array beamformers is easily degraded in the deep PBO region. The extra energy dissipation will bring in a severe thermal issue, especially in large-scale phased-arrays. In order to further enhance the output power as well as the PAE at deep PBO regions, several solutions are available for mm-wave PA design, such as mixed-signal PAs, out-phasing PAs, envelope-tracking PAs, and Doherty PAs. The mixed-signal PAs need external digital controls [38–40] which

increases the system control cost. The outphasing PA as shown in Fig. 2.15(a) consists of two or more PAs, which are driven by a signal that is phase-modulated to produce an output signal that is a combination of the amplified outputs of the PAs [41]. The main advantages of outphasing PAs are high power efficiency. However, there are also some drawbacks to this technology. One of the main drawbacks is the need for accurate phase and amplitude control of the individual PAs, which can be challenging to achieve in practice. Any errors in the phase or amplitude control can lead to distortions in the output signal, which can cause interference with other communication channels. Besides, outphasing PAs are sensitive to variations in the input signal amplitude and phase, which means backend overhead is required to generate the outphasing signals [42–45].

As the other PBO efficiency enhancement technique, the envelope-tracking PA is shown in Fig. 2.15(b). The envelope-tracking PAs save the PA DC power consumption in PBO by a dynamic power supply. This methodology can achieve peak PAE at multiple input power levels. By having the supply voltage tracks the input power of the amplifier, the following PAE curves can be seen relative to the back-off power of the signal. However, the analog supply modulator often presents tough design trade-offs among its efficiency, dynamic range, and speed. This becomes particularly challenging for signals with large PAPRs and high modulation rates. Modulating a supply voltage can cause issues with linearity normally overlooked and assumed to be solved with digital pre-distortion.

As for Doherty PAs, the $\lambda/4$ TL-based impedance inverter load modulation network has been widely used [46–52]. Fig. 2.16(a) demonstrates the basic topology of the parallel Doherty PA. Unlike the conventional power combining of two identical PA paths, the Doherty PA comprises the main PA path and the auxiliary PA path. The main PA stage biased in class-AB mode is always on from the small signal power region to the saturated power region. In contrast, the auxiliary PA stage is biased in class-C mode, which is turned off at higher than 6-dB PBO and is gradually opened when the PBO is less than 6dB. The $\lambda/4$ TL-based impedance inverter is designed with a characteristic impedance of R_{opt}. The load modulation for the main PA path is adjusted by the variant output impedance of the auxiliary PA path. Fig. 2.16(b) compares concept efficiency with the class-AB PA.

Nowadays, instead of the bulky and lossy $\lambda/4$ TL, as shown in Fig. 2.17(a), the transformer-based passive networks are selected together with the capacitors to realize both impedance matching and load modulation. This impedance inverter can be substituted by the π-shaped C-L-C equivalent model in the mm-wave band, as shown in Fig. 2.17(b). By reorganizing the positions of inductors and capacitors toward the output balun demonstrated in Fig. 2.17(c), the inductors can be absorbed into the balun as a part of the leakage inductance [53]. Thus the chip area can be further reduced. Fig. 2.17(d) and Fig.

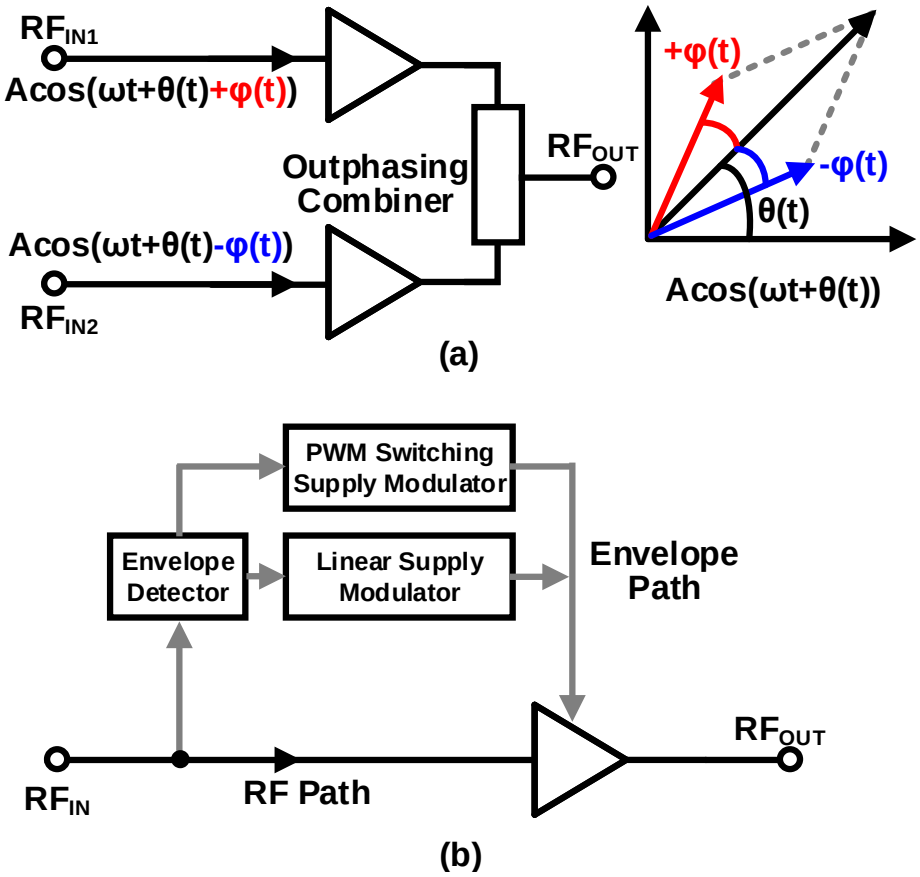

Figure 2.15: Concept of the (a) basic out-phasing PA and (b) envelope-tracking PA.

2.17(e) show the topology of the compact transformer-based output combiner with its EM model. As a promising solution for improving PBO efficiency, many high-performance stand-alone Doherty PAs have been demonstrated for 5G applications so far [53–62]. However, the integration of the Doherty technique in phased-arrays is still not well studied yet. The reported Doherty PAs are usually bulky and cannot fit the antenna pitch for mm-wave beamformer design.

2.6 Linearization Techniques for 5G Systems

2.6.1 Power Amplifier Linearization Techniques

At the transmitter side, the PA is the bottleneck for the distortion of the whole system. The effect of distortion can be decomposed into two parts: 1) the effect on the amplitude referred to as amplitude to amplitude (AM-AM) and 2) the effect on the phase referred

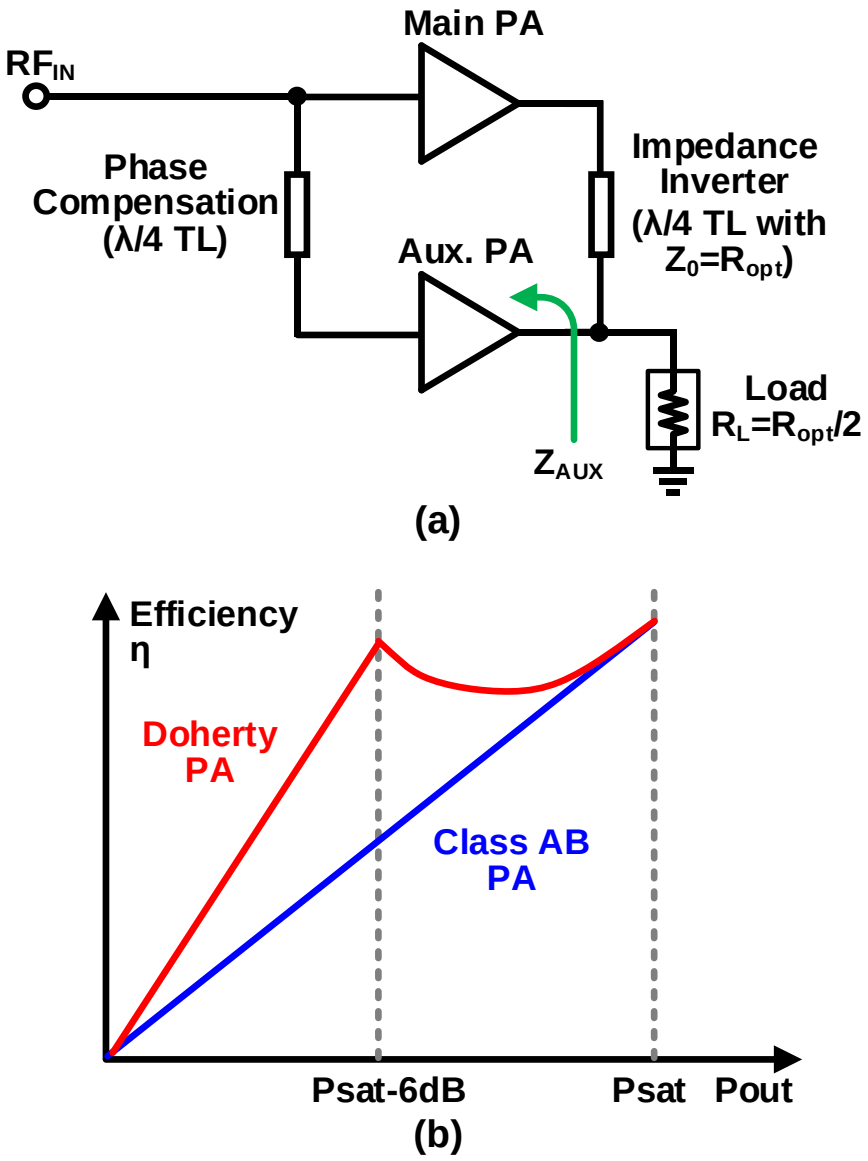

Figure 2.16: (a) Concept of the basic parallel Doherty PA with (b) its efficiency compared with class-AB PA.

to as amplitude to phase (AM-PM). PAs intended for complex modulation are often operated in class-AB mode to meet simultaneous requirements for high efficiency and reasonable linearity. Nonetheless, the class-AB biasing leads to additional AM-PM distortion [63, 64]. Consequently, it degrades linearity metrics, such as EVM and ACLR, in complex-modulation systems. This motivates significant research efforts on the sources of AM–PM distortion [65, 66] and the implementations of class-AB PAs with mitigated AM–PM distortion [67–70]. The reported AM-PM linearization techniques mainly comprise the PMOS varactor-based compensation, second harmonic trap, and transformer-

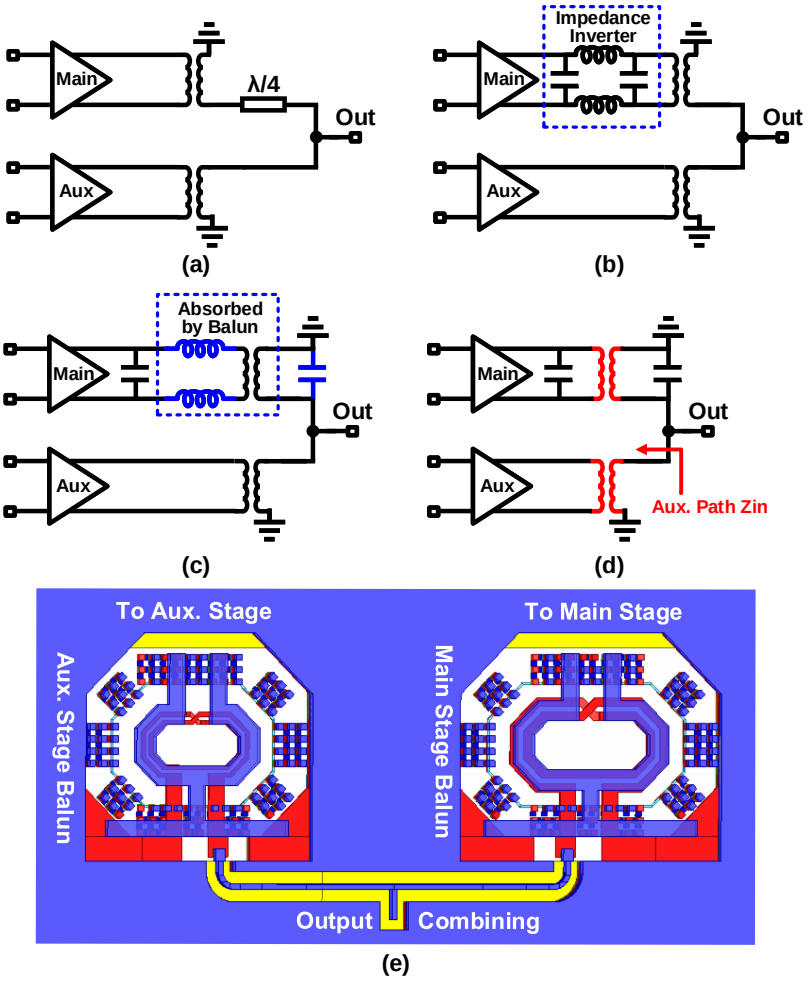

Figure 2.17: (a) Conventional output combiner with $\lambda/4$ transmission line. (b) Output combiner with equivalent π-shaped C-L-C impedance inverter and the (c) reorganized model together with balun. (d) Inductors absorbed into the balun as a part of the leakage inductance. (e) EM model of the compact transformer-based output combiner.

based feedback correction. Besides, as for the power-combined PAs, especially the Doherty PAs. The class-C biased auxiliary path will bring in more AM-AM and AM-PM issues. The linearity correction for Doherty PAs is mainly through the adaptive bias network (ABN). The ABN adjusts the class-C stage bias according to the detected input swing envelope. With the dedicated optimization, the AM-AM distortion can be significantly compensated [56, 71–73].

Well, the mentioned linearization techniques mainly focus on stand-alone PA designs. The linearization improvement will suffer from the PVT variations when integrated into the phased-array systems.

2.6.2 Digital Pre-Distortion

As another cost-effective linearization solution, the digital pre-distortion (DPD) technique can also be applied to correct the distortion introduced by the PA nonlinearity in the baseband [74, 75]. Recently, there have been more and more demonstrations of the phased-array DPD strategies [76–90]. Fig. 2.18(a) shows a simplified DPD-PA cascade system. The DPD features an excellent linearization capability and the ability to preserve overall efficiency. It takes full advantage of advances in digital signal processors and A/D converters. The technique adds an expanding inverse nonlinearity in the baseband that complements the compressing characteristic of the power amplifier. Ideally, the cascade of the pre-distorter and the power amplifier becomes linear, and the original input is amplified by a constant gain. With the pre-distorter, the power amplifier can be utilized up to its saturation point while maintaining good linearity, significantly increasing its efficiency. The DPD algorithm needs to model the PA behavior accurately and efficiently for successful DPD deployment.

DPD implementations can be classified into memoryless models and models with memory. Memoryless models focus on the power amplifier that has a memoryless nonlinearity. The current output depends only on the current input through a nonlinear mechanism. This instantaneous non-linearity is usually characterized by the AM/AM and AM/PM responses of the power amplifier, where the output signal amplitude and phase deviation of the power amplifier output are given as functions of the amplitude of its current input. Memoryless polynomial and look-up table (LUT) based algorithms are two key algorithms for memoryless models. The memory model is commonly used as the signal bandwidth becomes broadened. Power amplifiers exhibit memory effects for wider bandwidth due to the different PA non-linearity frequency responses. This is especially true for those high-power amplifiers used in wireless base stations. Besides the wideband frequency memory effect, the causes of the memory effects can be attributed to components in the biasing network or the power supply that have frequency-dependent behaviors or thermal constants of the active devices. As a result, the current output of the power amplifier depends not only on the current input but also on the past input values. In other words, the power amplifier becomes a nonlinear system with memory.

Memoryless pre-distortion can achieve only very limited linearization performance for such a power amplifier. Therefore, digital pre-distorters must have memory structures. The most important algorithm for models with memory for Digital pre-distortion implementation is the Volterra series and its derivatives. The most general way to introduce memory is to use the Volterra series. However, the large number of coefficients of the Volterra series makes it unattractive for practical applications. This thesis uses the

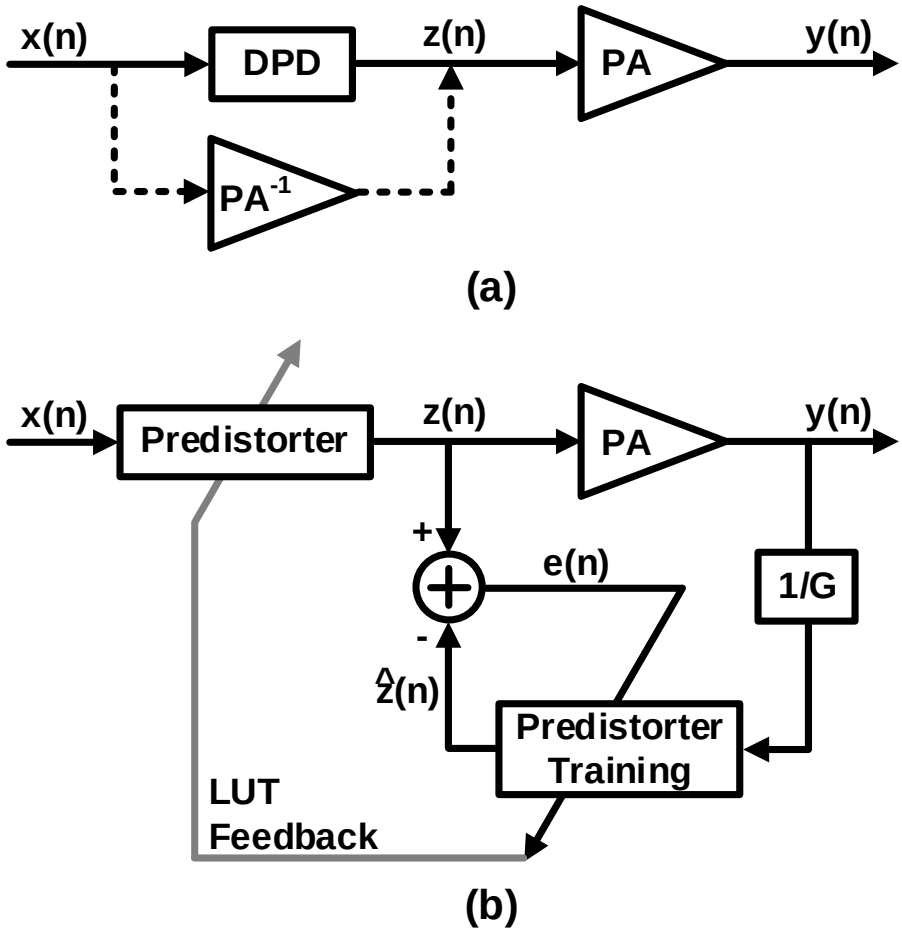

Figure 2.18: (a) The inverse nonlinear operation of the DPD; (b) Predistorter with memory model.

memory polynomial model derived from the Volterra series with compact memory length and depth. Fig. 2.18(b) demonstrates the indirect learning architecture for the digital pre-distorter [91].

The discussion above about the DPD technique is limited to single PA or TRX cases. Considering the DPD implementation applications in phased-array systems with multiple beamformer elements, the linearity improvement can be limited due to the different beamformer characteristics. This issue will be analyzed in detail in Chapter 4, with a possible solution proposed.

2.7 Summary

In this chapter, the main concepts and standards for 5G NR FR2 networks are introduced, followed by the challenges facing the design of millimeter-wave CMOS transceivers. Besides, the most important challenges and requirements of the phased-array systems are discussed. The design limitations and existing techniques for the area- and power-efficient systems are further explored. Beamforming importance and realization conditions are also explained in this chapter.

Chapter 3

Area-Efficient Bi-Directional Technique

3.1 Introduction

The phased-array system plays a very important role in millimeter-wave communications. A large-scale array size is necessary for a sufficient EIRP to maintain the long communication distance. The area-efficient technique is desired to reduce the whole system's physical size and manufacturing cost. The importance of area efficiency has been mentioned in Chapter 2. The detailed analysis of the proposed area-efficient technique with be discussed in this chapter. The proposed bi-directional technique is derived from the conventional capacitive neutralization technique. The Doherty technique is then implemented with the bi-directional core to enhance the PBO efficiency with less die area penalty. After that, the active vector-summing phase shifter (VSPS) utilizing the proposed bi-directional core is demonstrated. A bi-directional passive mixed-type phase shifter (MTPS) is also designed for better PVT characteristics than active PSs. The single-ended bi-directional variable gain amplifier (VGA) is given at the end.

3.2 Neutralized Bi-Directional Technique

3.2.1 Conventional Capacitive Neutralization

The capacitive neutralization is a popular PA structure, as shown in Fig. 3.1(a). Common-source differential pair is used for the largest output swing from each PA stage at low supply. Stability and isolation of the PA are simultaneously achieved by neutralizing each stage using cross-coupled drain-gate feedback capacitors. Neutralization increases the gain with no penalty in power consumption. Unconditional stability results from the near unilateral behavior of each stage, which permits simplified inter-stage matching with on-

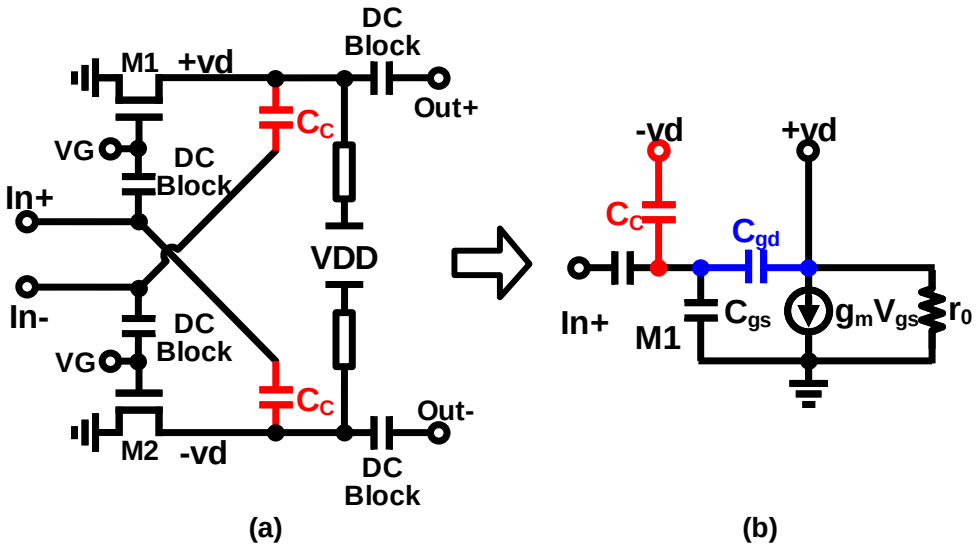

Figure 3.1: (a) Conventional differential PA core with capacitive neutralization and (b) its equivalent model for the PA transistor.

chip coupling transformers [32, 92, 93]. As shown in Fig. 3.1(b), the Miller effect of the PA transistor can be analyzed for its equivalent model. Assuming a positive voltage gain of A_V, the voltage gains for OUT− to IN+ and for OUT+ to IN+ can be written as A_V and $-A_V$. Thus, the total Miller capacitance C_M from OUT− and OUT+ are equal to

$$C_M = C_{gd}(1 - A_V) + C_C(1 + A_V) \tag{3.1}$$

Suppose the gain A_V is much greater than 1, the Miller capacitance C_M can be simplified as

$$C_M = (C_C - C_{gd})A_V C_C - C_{gd} \tag{3.2}$$

The C_M can be fully neutralized when choosing $C_C = C_{gd}$.

3.2.2 Neutralized Bi-Directional Core

The proposed neutralized bi-directional core is realized by replacing the C_C pair in Fig. 3.1 with the other transistor pair severed as LNA-mode transistors. Fig. 3.2 (a) shows the circuit schematic of the bi-directional gain amplifier. Two differential pairs in cross-coupling connection are included in the neutralized bi-directional core. The mode selection of the core is realized by switching the tail transistors M3 and M6. Fig. 3.2 (b) and (c) further explain the TX-mode and RX-mode core operations. By selecting the same tran-

sistor size among M1, M2, M4, and M5, the gate-drain capacitance neutralization could be maintained in both operating modes. Improved amplifier gain and reverse isolation are achieved. Moreover, to minimize the required chip area, the TL-based passive matching components for the gain amplifier are shared between TX mode and RX mode. In millimeter-wave frequencies, the required matching conditions for the proposed core will not change dramatically during the mode switching. Therefore, properly-sized TLs could be selected to achieve low-loss matching in both TX and RX modes. High-performance and area-efficient bi-directional amplifiers could be realized.

Fig. 3.3 (a) and (b) show the simulated performance of the bi-directional gain amplifier. The achieved TX-mode and RX-mode gain are around 8 dB and 10 dB, respectively. Within 26.5 GHz to 29.5 GHz, the return losses are always better than -8 dB. The power consumptions are 9 mW in TX mode and 10 mW in RX mode. Furthermore, orthogonal gain and phase tuning is always demanded by millimeter-wave beamformers for a simple control algorithm and fast calibration. In this work, the TX-mode amplifier is further reused as the VGA in each beamformer path. The tail bias is controlled by the high-resolution DACs for providing the fine gain tuning. Fig. 3.3 (c) and (d) demonstrate the VGA performance. The simulated gain coverage with transistor process corners is also shown in the figure. Thanks to the neutralized bi-directional technique, the phase variation during the gain tuning is suppressed by the gate-drain capacitance neutralization. As shown in Fig. 3.3 (d), within 8-dB gain tuning range, the phase variation is less than 2.5° at 28 GHz.

3.2.3 Class-AB PA-LNA

In RF front-end design, the PA, LNA, and antenna interface almost dominate the system performance. The low-loss antenna interface is attractive for maintaining TX output power level and reducing RX NF. Also, the $\lambda/2$ antenna pitch is scaling down along with the increasing operation frequency, less than 5-mm antenna pitch is available when operating at 28GHz or even higher frequency band. Thus, compact packaging method is desired. The PA power delivery and LNA NF are required to be optimized together with the TRX switch considering the insertion loss and chip area.

Fig. 3.4 shows the circuit schematic of the PA-LNA along with the packaging connection. To minimize the chip area cost, the unbalanced neutralized bi-directional technique is adopted in this work. Compared with the neutralized bi-directional technique mentioned in Chapter 3.2.2, two extra capacitors C_{comp} are attached to the LNA transistors for compensating the extra gate-drain capacitance from the PA transistors. Therefore, even with different transistor sizes, the unbalanced neutralized bi-directional core could still

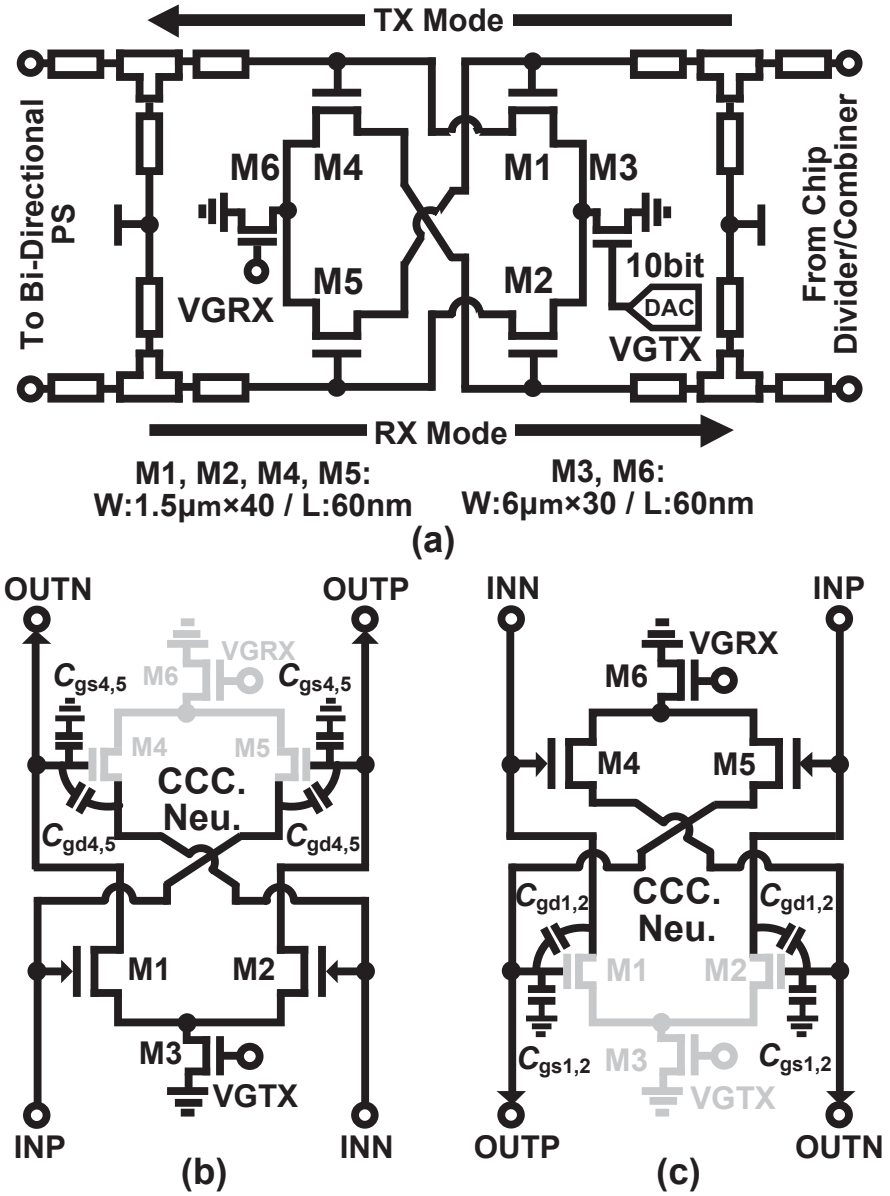

Figure 3.2: (a) Circuit schematic of the neutralized bi-directional gain amplifier. Equivalent circuits of the proposed neutralized bi-directional core in (b) TX mode and (c) RX mode.

maintain the gate-drain capacitance neutralization in both PA mode and LNA mode. Fig. 3.5 shows the layout optimization of unbalanced neutralized PA-LNA cores. The first version of the PA-LNA core is shown in Fig. 3.5(a), where the larger interconnection loss exists for both LNA mode and PA mode. Besides, the achievable PAE is relatively low due to the only tail bias control in the PA mode. While the updated version of the PA-LNA core, as shown in Fig. 3.5(b), provides individual PA biases by inserting additional

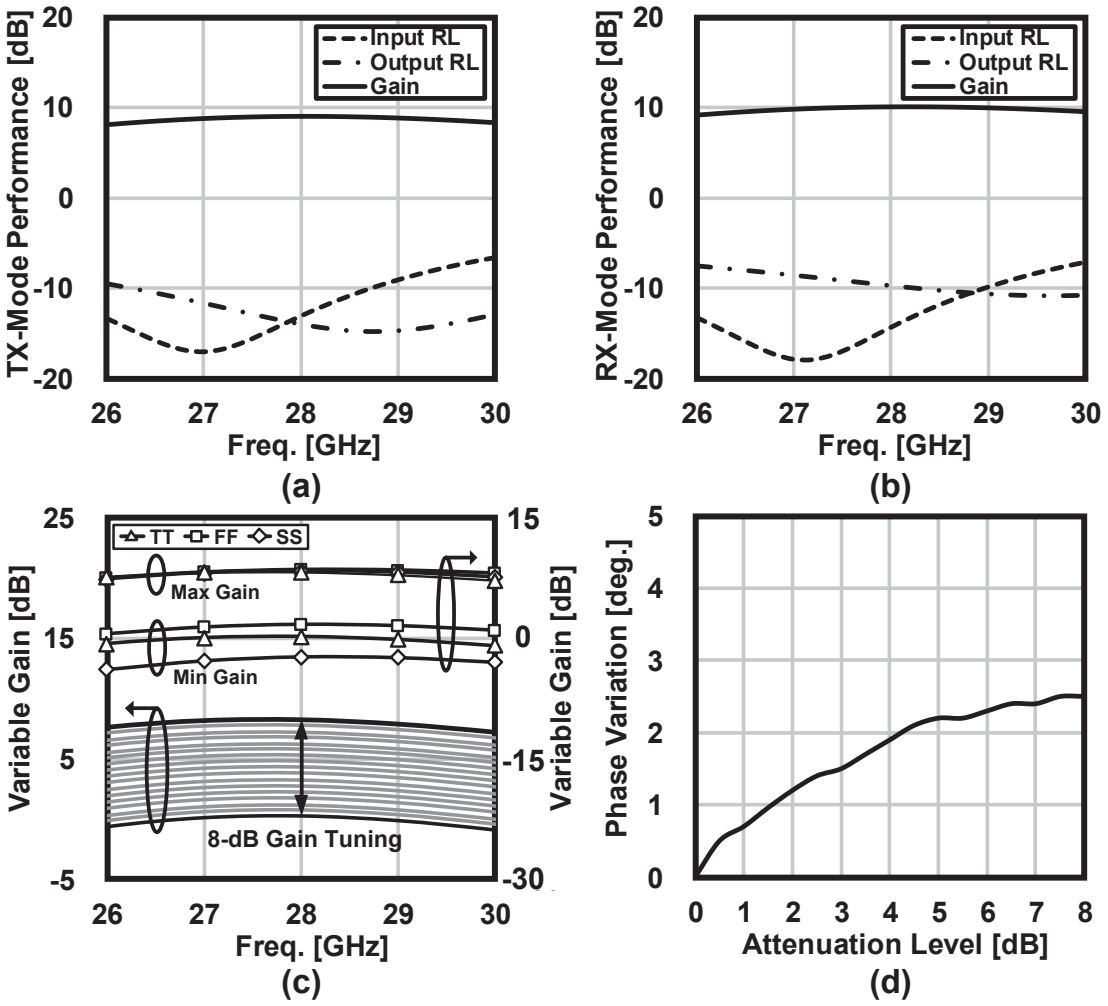

Figure 3.3: Simulated S parameters of the gain amplifier in (a) TX mode and (b) RX mode. Simulated (c) variable gain of the TX-mode amplifier and (b) the corresponding phase variation at 28 GHz.

DC-block capacitors to enhance the PA PAE. At the same time, the PA-mode parasitic inductance is still higher because of the long interconnection path between the PA transistors' drain and the output transformer-based matching network. The updated version of the PA-LNA core is used in the 28-GHz PA-LNA designs. While for the following 39-GHz PA-LNA research, the compact PA-LNA core with minimized PA-mode parasitic inductance is required due to the more severe parasitic influence of high operation frequency. It can be demonstrated in the final version of the PA-LNA core as shown in Fig. 3.5(c). The further narrowed core size provides higher PA-mode saturated output power and peak PAE.

The matching network towards the antenna port is configurable with a switching tran-

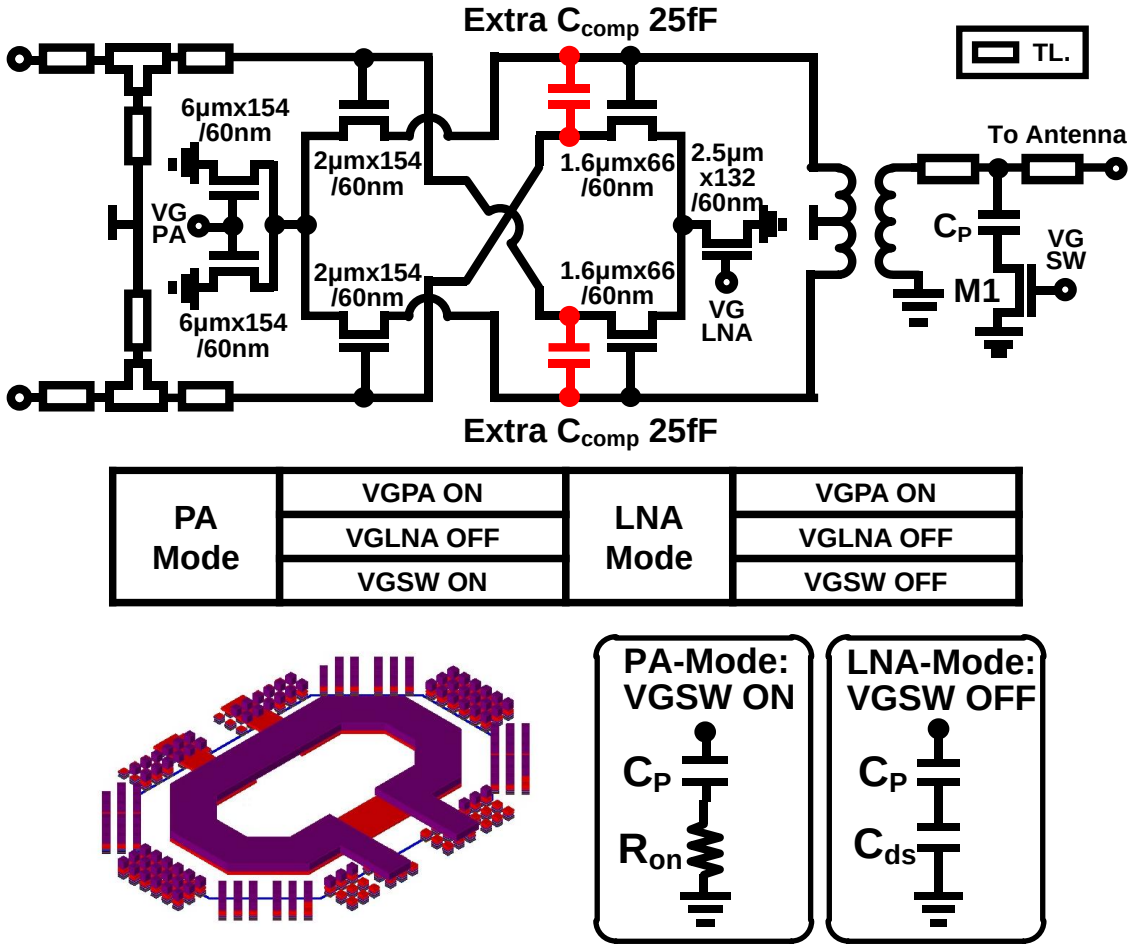

Figure 3.4: Circuit schematic of the proposed PA-LNA with antenna sharing.

sistor M1. By switching the on/off state through the bias VGSW, the matching point can be closer for both the load-pull optimum impedance in PA mode and the optimum noise figure impedance in LNA mode. The proposed PA is biased in class AB condition to improve the PA-mode power efficiency at the deep PBO region. An adaptive antenna-sharing network is co-designed with the core circuits to improve the PA-mode power delivery and LNA-mode NF. At 28 GHz, the simulated insertion loss of the antenna-sharing network is 0.5dB in PA mode and 1.5dB in LNA mode.

To evaluate the performance of the PA-LNA, a standalone PA-LNA is fabricated for on-wafer measurement. Fig. 3.6 (a) presents the measured PA-mode linearity. The achieved saturated output power is 16.2dBm and the output P_{1dB} is 13.4dBm. Fig. 3.6 (b) demonstrates the corresponding power-added efficiency (PAE). The proposed PA reports a maximum PAE of 30.7%, including the TRX switch. Thanks to the class AB bias condition, the maintained PAE at 6-dB PBO is 11.5%. The measured LNA-mode NF is

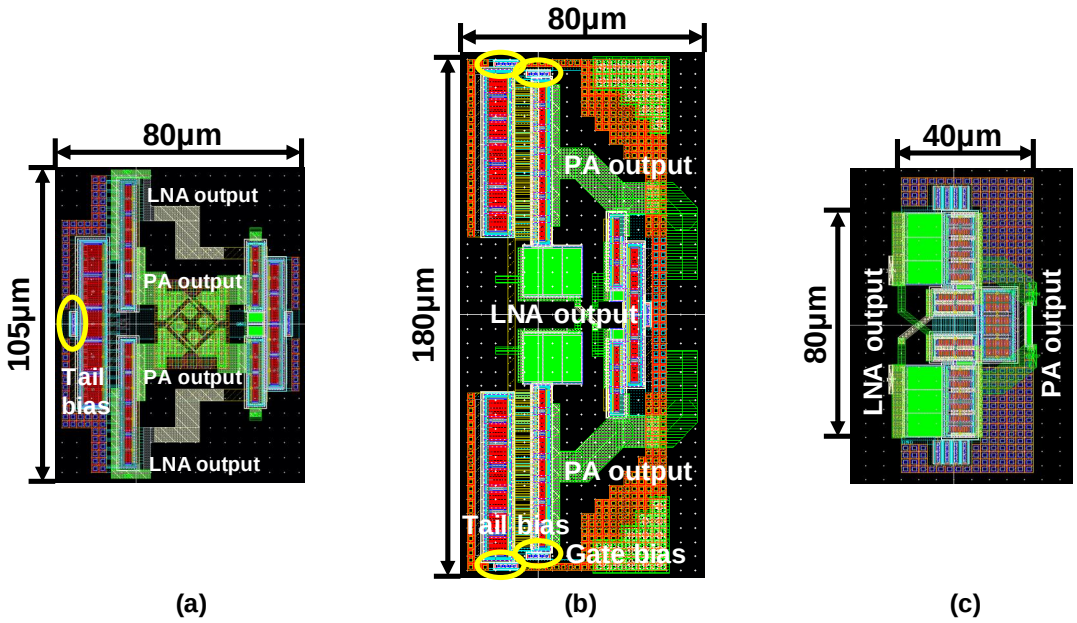

Figure 3.5: The layout optimization of unbalanced neutralized PA-LNA cores

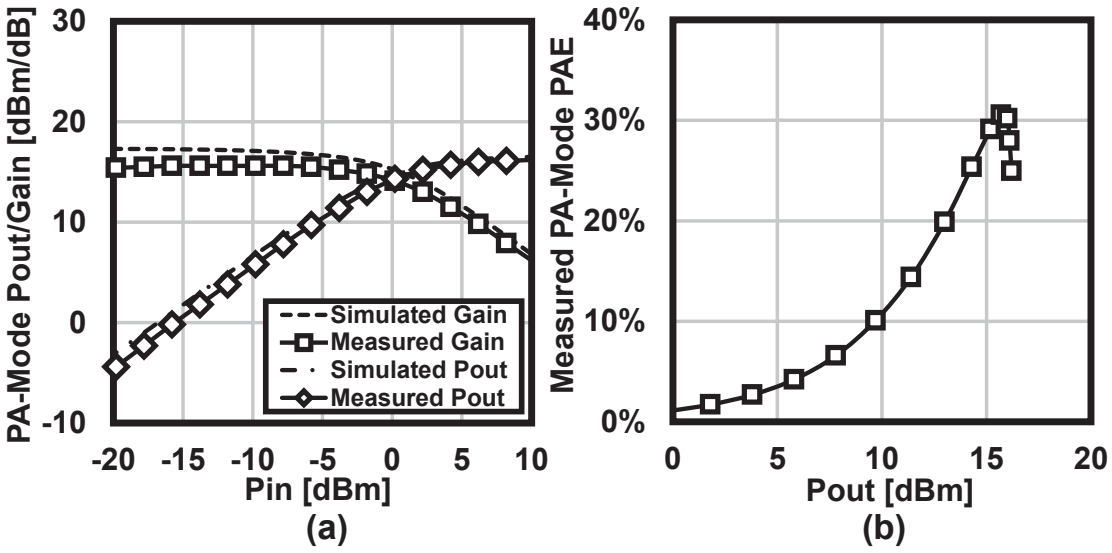

Figure 3.6: (a) Measured PA-mode linearity and (b) the corresponding PAE.

further shown in Fig. 3.7. Keysight PNA-X N5247A and the cold-source method are used for the NF measurement. Within the frequency range of 26.5GHz to 29.5GHz, the NF is from 4.3dB to 5.3dB.

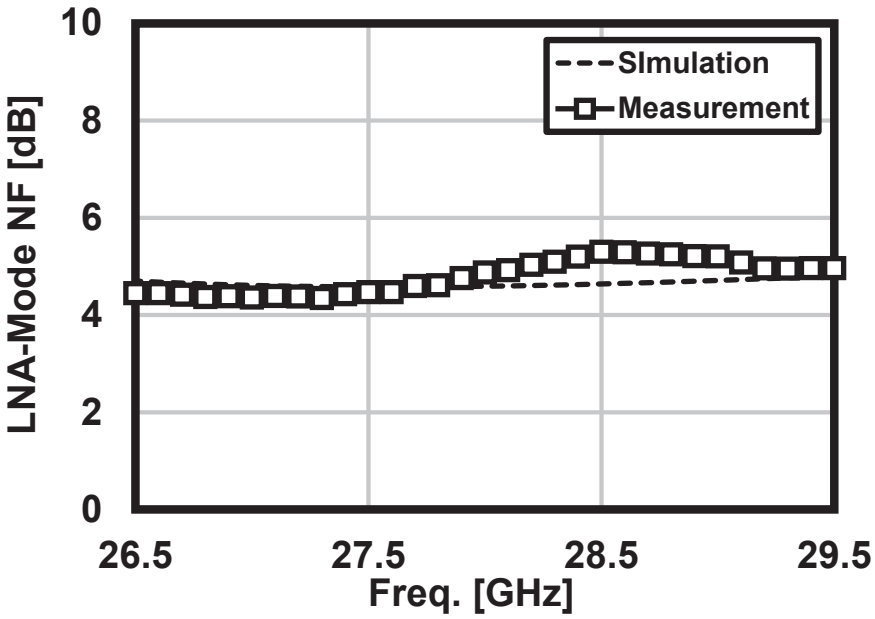

Figure 3.7: Measured LNA-mode noise figure (NF).

3.3 Bi-Directional Doherty PA-LNA with WLCSP

Facing the complex modulated signals in 5G, the PA efficiency in the deep PBO region also demands further improvement. Moreover, the packaging design is critical to the overall performance of 5G millimeter-wave phased-array systems. Accurate package modeling and optimizations are required to decrease the insertion loss. In this work, a bi-directional Doherty PA-LNA is proposed and co-designed with WLCSP. The TX back-off power efficiency can be enhanced by utilizing the Doherty technique. Meanwhile, a larger TX output power is realized through the combined output, which is good for reducing the array size.

3.3.1 Doherty PA-LNA

Fig. 3.8(a) and Fig. 3.9(a) show the bi-directional Doherty PA-LNA in PA mode and LNA mode, respectively. It consists of a 90° hybrid coupler, a main PA path with LNA, and an auxiliary PA path for Doherty operation. The main PA path with LNA is designed based on an unbalanced neutralized bi-directional technique [9, 10]. A minimized on-chip area could be realized by the shared inter-stage passives between PA and LNA. When the Doherty PA-LNA operates in PA mode, the main PA path is biased at class-AB while the auxiliary PA path is biased at class-C to perform the Doherty load modulation. The same driver stages are applied for both the main and auxiliary PA paths to minimize the

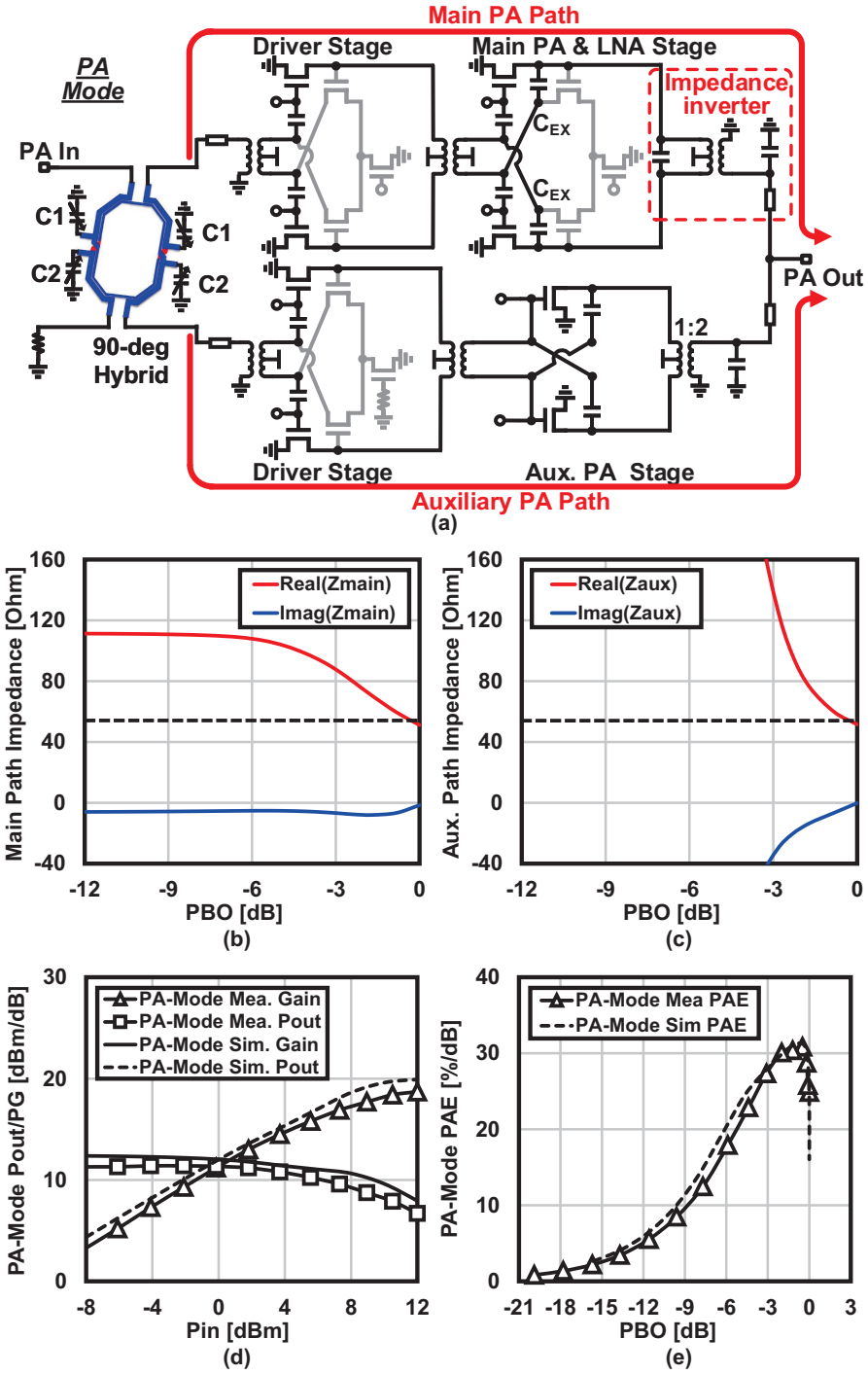

Figure 3.8: (a) Proposed bi-directional Doherty PA-LNA in PA mode. Simulated PA-mode Doherty load modulation characteristics of (b) main PA path and (c) auxiliary PA path, measured results of the stand-alone bi-directional Doherty PA-LNA TEG (d) PA-mode power gain and output power, and (e) PA-mode PAE vs. power back-off.

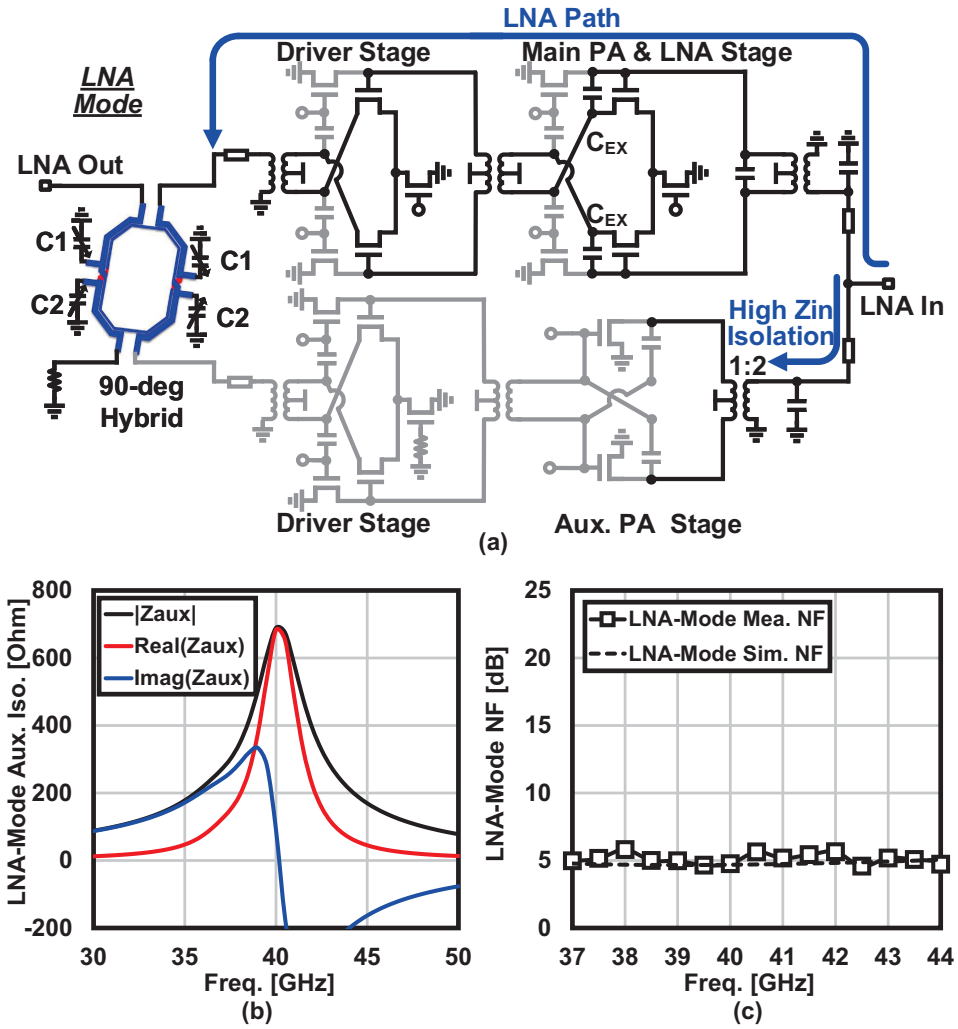

Figure 3.9: (a) Proposed bi-directional Doherty PA-LNA in LNA mode. (b) Simulated LNA-mode auxiliary path isolation, (c) measured result of the stand-alone bi-directional Doherty PA-LNA TEG LNA-mode noise figure.

output combining mismatch. Fig. 3.8(b) and (c) demonstrate the simulated Doherty load modulation characteristics of the main PA path and auxiliary PA path, respectively. The auxiliary PA path is gradually turned on from the 6-dB PBO point, and the load impedance seen into the main PA path is slowly descending at the same time. Until the saturation region, the same load impedance is reached for both the main PA path and the auxiliary PA path. Fig. 3.8(d) and (e) show the measured PA-mode results compared with its simulated results. To minimize the degradation between the measured results and simulated results, the transistor cores are modeled with EMX and the passives are modeled by Ansys HFSS during the post-simulation. In measurement, a standalone bi-directional Doherty PA-LNA achieves an 18.9-dBm Psat and a 30.4% peak PAE in PA mode with a 1-V supply voltage.

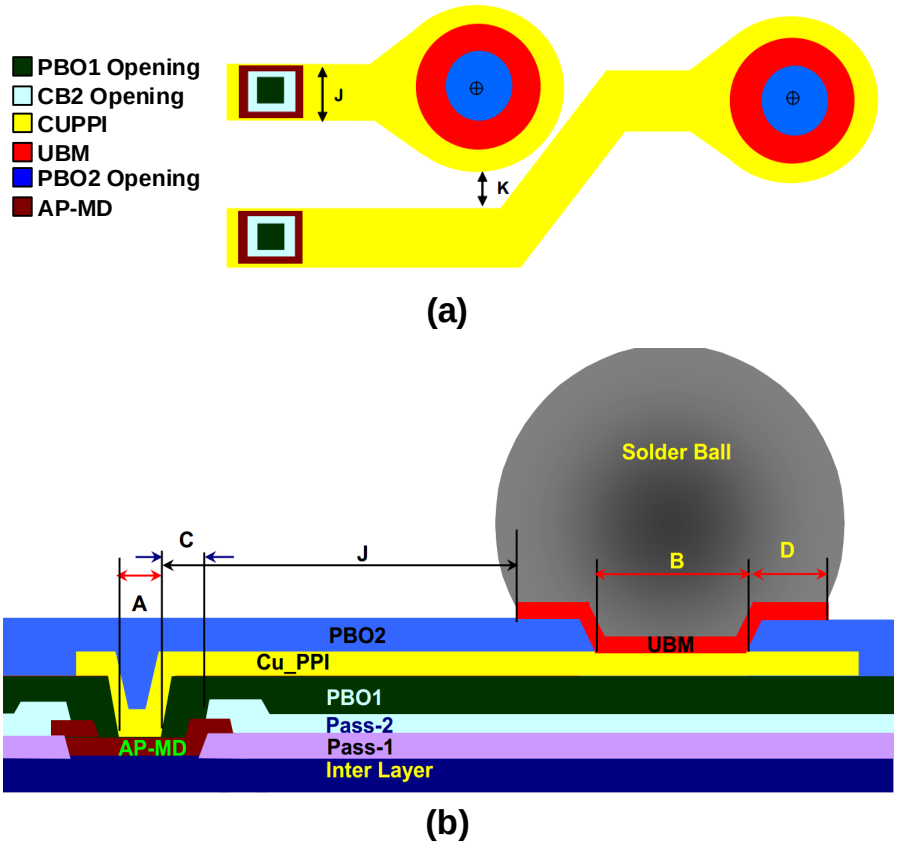

Figure 3.10: (a) The top view and (b) cross-sectional view of the dual-passivation WLCSP process.

The measured PAE at 6-dB and 8-dB PBO are 17.8% and 12.0%, respectively.

In LNA mode, the 1:2 balun at the auxiliary PA stage is capable of providing an impedance up-scaling to isolate the auxiliary path and suppress the loading effect. The simulated impedance seen from LNA input to the off-state PA auxiliary path is shown in Fig. 3.9(b). The extra capacitor C_{EX} is designed to be neutralized by the C_{gd} of the PA-mode transistors along with the C_{gd} of the LNA-mode transistors. Therefore, the Miller effect is minimized and the LNA-mode stability is also enhanced. The NF is measured by Keysight PNA-X N5274B network analyzer. The Noise Figure Cold Source option is selected with the Scalar Noise calibration. Fig. 3.9(c) presents the measured LNA-mode NF, a 4.8-dB NF at 40GHz and a less than 5.8-dB in-band NF are obtained in LNA mode.

3.3.2 Package and Antenna Design

Wafer Level Chip Scale Package (WLCSP) refers to the technology of packaging an integrated circuit at the wafer level instead of the traditional process of assembling individual

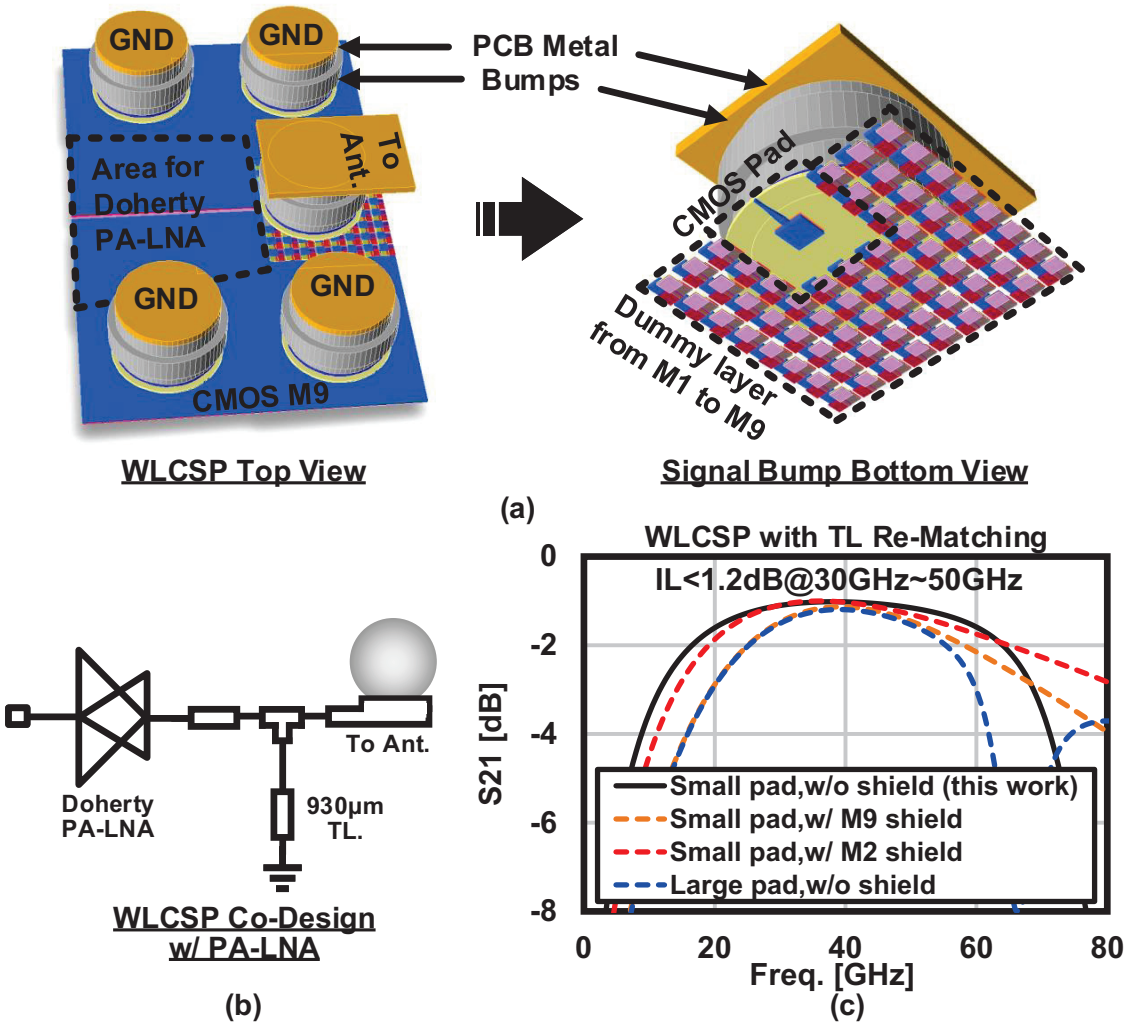

Figure 3.11: (a) Optimized 3D WLCSP EM model at the antenna port, (b) proposed bi-directional Doherty PA-LNA with WLCSP co-design, (c) simulated packaging insertion loss with the transmission-line rematching network.

units in packages after dicing them from a wafer. This process is an extension of the wafer Fab process, where the device interconnects and protection is accomplished using the traditional fab processes and tools. In the final form, the device is a die with an array pattern of bumps or solder balls attached at an I/O pitch that is compatible with traditional circuit board assembly processes. WLCSP is a true chip-scale packaging (CSP) technology, since the resulting package is the same size as the die. WLCSP technology differs from other ball-grid arrays (BGAs) and laminate-based CSPs in that no bond wires or interposer connections are required. The key advantages of the WLCSP are minimized die-to-PCB inductance, reduced package size, and enhanced thermal conduction characteristics. The Cuppi layer is used as RDL and isolated by two dielectric layers PBO1 and

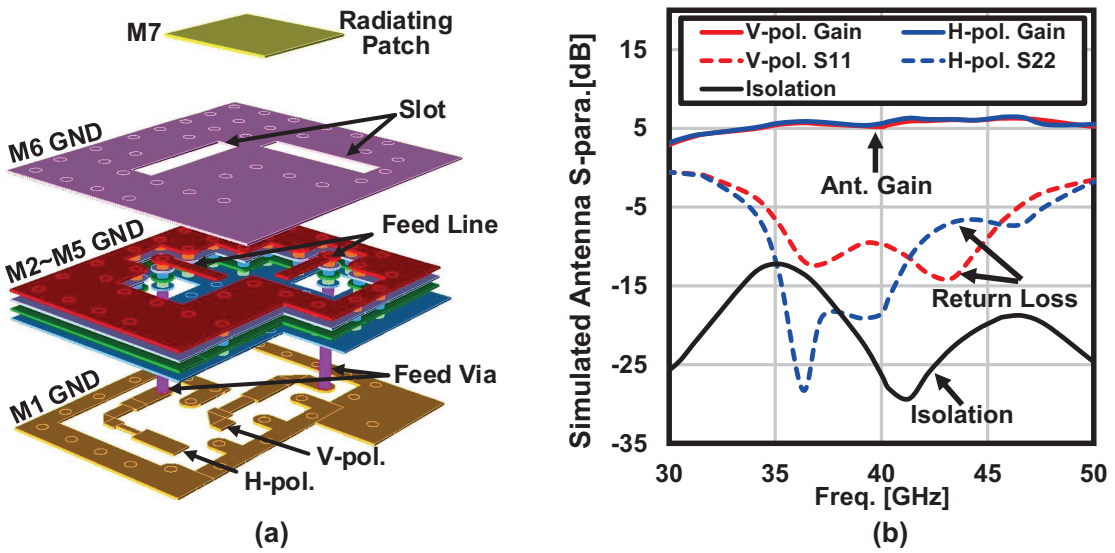

Figure 3.12: (a) The 3D EM model of the dual-polarized aperture-coupled antenna with offset slots in Γ-type configuration and (b) the simulated antenna performance.

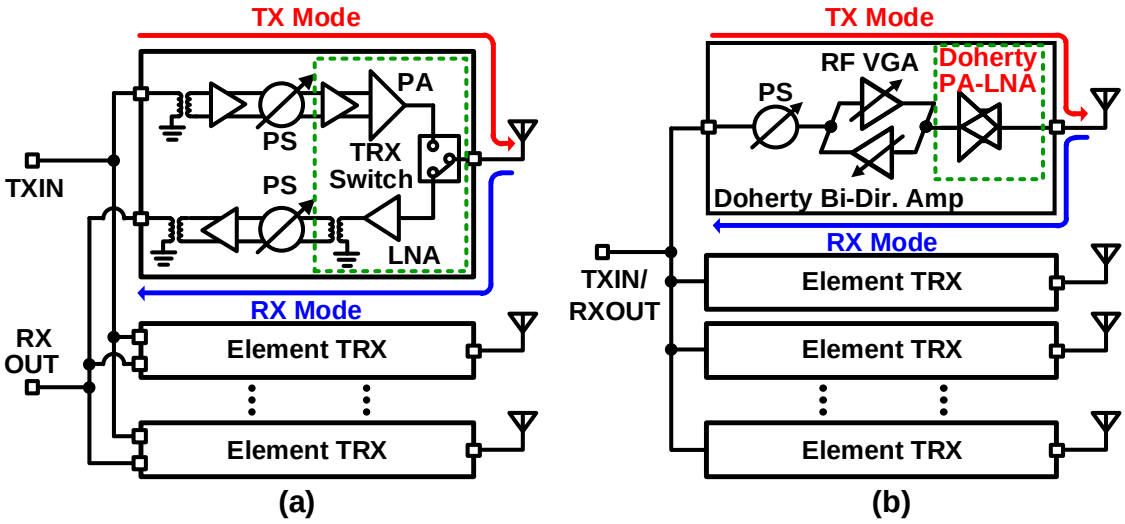

Figure 3.13: (a) Conventional phased-array architecture with antenna sharing. (b) Proposed phased-array architecture in bi-directional technique.

PBO2.

Fig. 3.11(a) shows the WLCSP 3D EM model for antenna and IC interconnection. In order to minimize the package capacitive loss and improve the bandwidth, the RF pad size is minimized and the ground shield under the signal bump is removed. The additional metal-to-substrate loss of the signal bump from the P-doped substrate is smaller than the capacitive loss introduced by the ground shield [94]. A transmission lines (TLs) rematching network is inserted between PA-LNA and the WLCSP model, as shown in Fig.

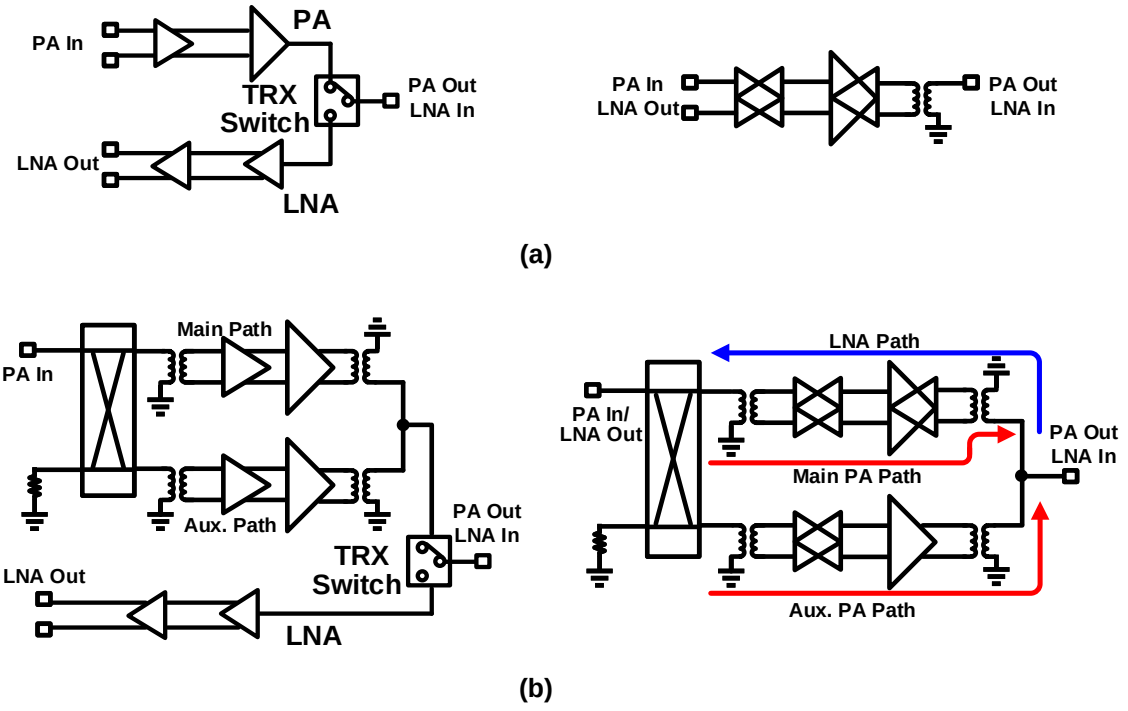

Figure 3.14: (a) Comparison between the conventional PA, LNA, and TRX switch with PA-LNA, and (b) comparison between the conventional Doherty PA, LNA, and TRX switch with Doherty PA-LNA

3.11(b). The TL stub is shared with the calibration path to save the chip area and further reduce insertion loss. Fig. 3.11(c) shows the WLCSP EM simulated results with TL re-matching network, a less than 1.2-dB insertion loss is realized from 30GHz to 50GHz.

The dual-pol. aperture-coupled structure is selected and optimized for the wide-band gain feature [95–97]. Its 3D EM model is given by Fig. 3.12(a) in Γ-type slot configuration. As shown in Fig. 3.12(b), a higher than 5-dB single-element wide-band antenna gain with larger than 25-dB isolation at 40GHz is realized according to the antenna simulated results.

3.3.3 PA-LNA Area-Power-Efficiency Analysis

This section will discuss the area and power efficiency of the proposed class-AB PA-LNA and Doherty PA-LNA at the system level. The comparison with state-of-the-art stand-alone PAs will also be demonstrated.

The conventional and proposed phased-array architectures with antenna sharing are depicted in Fig. 3.13(a) and Fig. 3.13(b), respectively. By employing the bi-directional technique, the PA-LNA block can replace the PA, LNA, and TRX switch of the conventional phased-array architecture, resulting in less overhead area for LNA and TRX

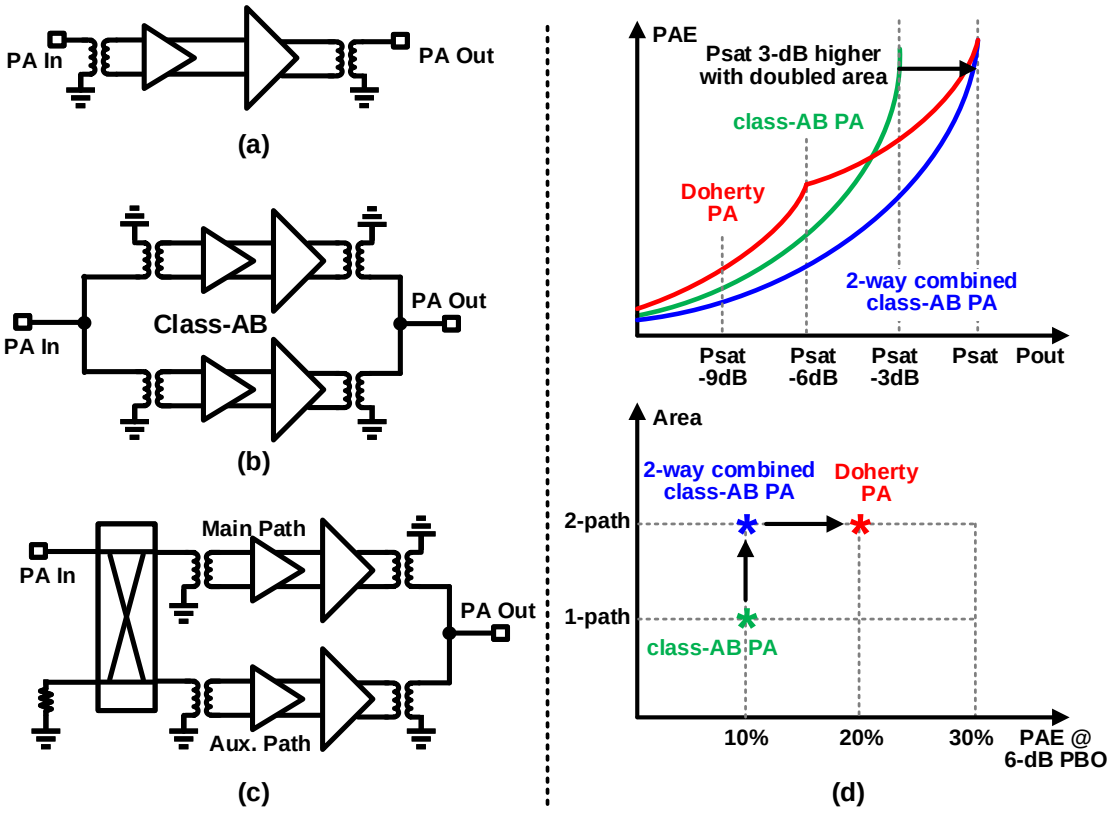

Figure 3.15: The two-stage topologies of (a) class-AB PA. (b) two-way power-combined class-AB PA and (c) Doherty PA. (d) Conceptual power-efficiency and area-efficiency comparison.

switches, thus achieving higher area efficiency. Additionally, the PA-mode Psat and PAE of the proposed PA-LNAs include the TRX-mode switching loss. In contrast, a TRX switch loss of around 1.5 dB must be accounted for in stand-alone PAs, making this work more power-efficient. To further demonstrate the area-efficiency of this work, a comparison between the conventional PA, LNA, and TRX switch with PA-LNA, and a comparison between the conventional Doherty PA, LNA, and TRX switch with Doherty PA-LNA are presented in Fig. 3.14(a) and Fig. 3.14(b), respectively. Assuming that each path occupies the same area and excludes the additional area for the TRX switch, it is evident that only 50% and 66.7% of the area are required for the PA-LNA and Doherty PA-LNA, respectively. In other words, compared with the stand-alone PAs, the PA-LNA and Doherty PA-LNA only occupy 50% and 66.7% equivalent areas in PA mode.

As for the Doherty PA in Fig. 3.15(c), it doubles the output power compared with class-AB PA as shown in Fig. 3.15(a), similar to the two-way power-combined class-AB PA in Fig. 3.15(b). Assuming no combiner loss, the 6-dB PBO efficiency of the Doherty PA is around two times compared with class-AB PAs. From Fig. 3.15(d), it is

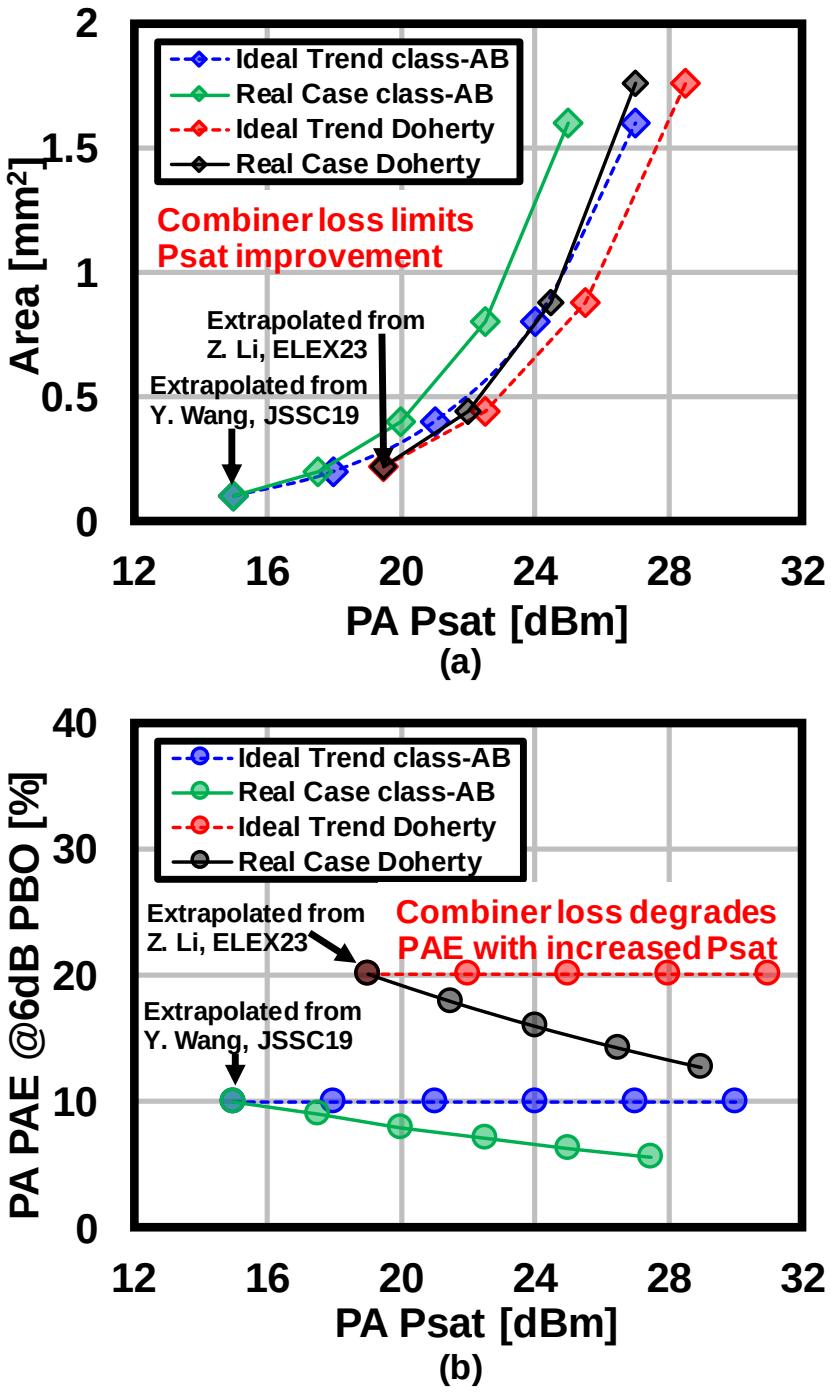

Figure 3.16: (a) The trend of area versus. Psat by power-combining and (b) the trend of backoff PAE versus. Psat by power-combining.

easy to find that the Doherty technique enhances the PBO efficiency while maintaining the same area efficiency. The power-combining technique effectively improves output power, and its insertion loss directly determines the PA performance. Extrapolated from the

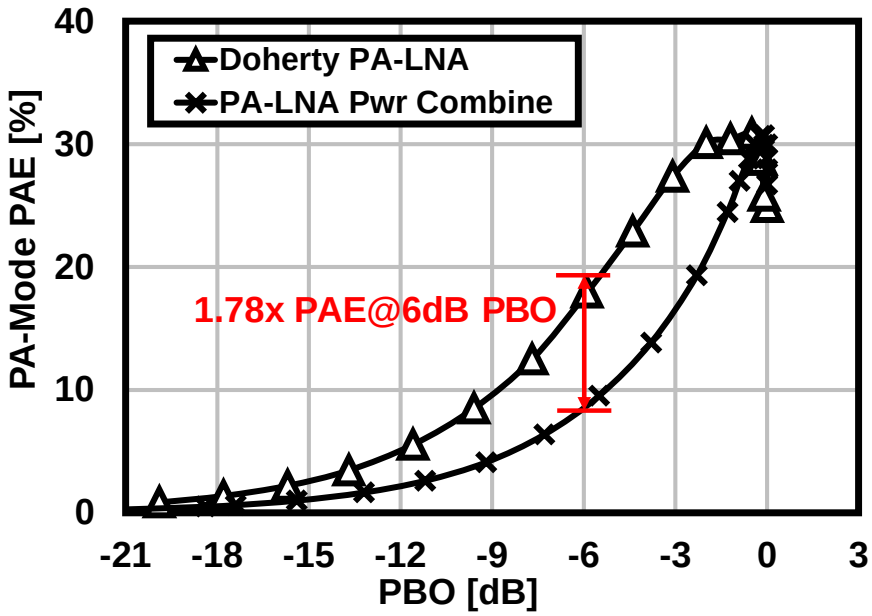

Figure 3.17: Doherty PA back-off PAE enhancement compared with the power-combining PA

reported papers, the area and PAE trends versus Psat with multi-stage RF combiners can be depicted as Fig. 3.16(a) and Fig. 3.16(b), respectively. As for the ideal trends without power-combining loss in dotted lines, every two times of area with lead to doubled Psat, while the PAE keeps same. However, in practice, around 0.5-dB power-combining loss should be considered. Thus as for real cases in solid lines, the area is doubled but results in less than doubled Psat, degrading the PAE performance.

According to the above analysis, as proof of PBO efficiency enhancement by the Doherty technique, Fig. 3.17 compares the Doherty PA-LNA compared with a two-way symmetrical power-combined PA-LNA, 1.78 times PAE improvement is obtained at 6-dB PBO region.

To further demonstrated the advantages of the proposed PA-LNA, the comparison of the state-of-the-art PAs from 20GHz to 50GHz are given in Fig. 3.18. From Fig. 3.18(a), the proposed PA-LNAs proved area-efficient in this work by fully absorbing the chip area for LNA. The compact size with a 1-V power supply is compatible with scaling down phased-array applications. Furthermore, good power efficiency performance is obtained based on the 65nm CMOS technology in Fig. 3.18(b). Due to the switchless bi-directional operation, this work suffers from no additional saturated output power and PAE degradations. As mentioned above, the equivalent PA-mode area equals 50% and 66.7% for PA-LNA and Doherty PA-LNA, respectively. Furthermore, a general 1.5-dB TRX switch loss should be compensated during the comparison with stand-alone PAs. Thus, demon-

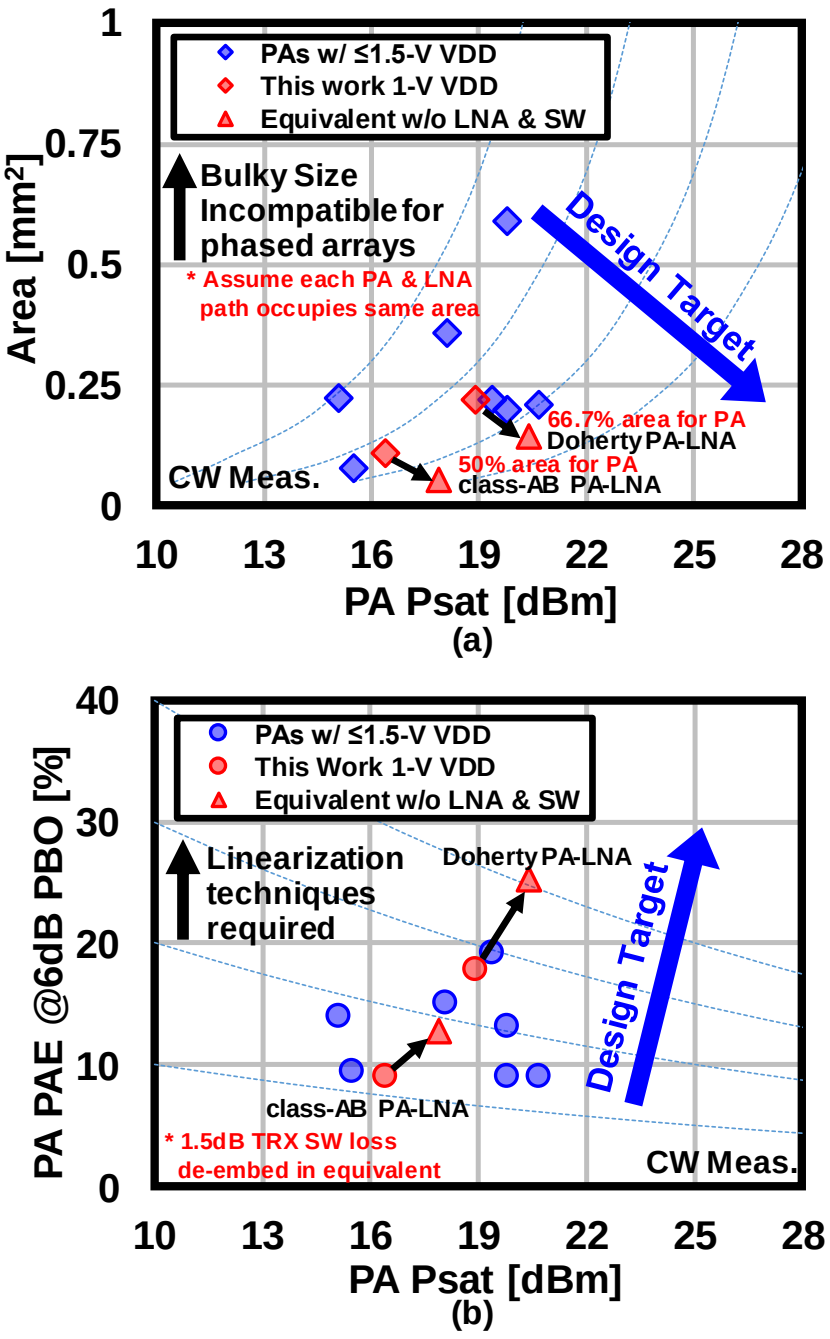

Figure 3.18: Comparison of the state-of-the-art PAs for 5G applications from 20GHz to 50GHz bands: (a) area efficiency performance and (b) power efficiency performance.

strated in the red triangle markers, this work performs excellent area-power-efficiency, which makes this work more attractive for 5G phased-array applications.

3.4 Bi-Directional Building Blocks

3.4.1 RF Phase Shifter Considerations

As the key component of the phased-array system, RF phase shifters (PS) with high phase shifting resolution can suppress the side lobes and minimize the beam-pointing error. Aiming for the increasing carrier frequency bands and beamformer integration level, compact PS designs supporting bi-directional operation are desired. The design considerations for the 5G NR and next-generation PSs are illustrated in Fig. 3.19, where the pros and cons of the three popular bi-directional PS architectures are demonstrated. The active vector-summing phase shifter (VSPS), which is composed of a vector-summing poly-phase filter (PPF) or quadrature all-pass filter (QAF) together with the VGA stage, is able to perform phase shifting while maintaining a relatively smaller insertion loss. The bi-directional VSPS reported in [9] is designed with the bi-directional core. Thus, the area of the beamformer element can be further shrunk down. However, the linearity degradation introduced by PVT variations and the additional power consumption limit its usage. Moreover, precise calibration is required to compensate for the I/Q imperfection. The path-to-path mismatches make the calibration more complicated, which means dedicated LUTs for each element are necessary, tremendously increasing the controlling cost for large array systems. Compared with the active VSPS, the passive VSPS based on the hybrid coupler with a bi-phase vector modulator requires no additional power consumption and provides better PVT features due to the lack of active VGA stages. However, like the active VSPS, the passive VSPS also requires the frequency response of the passive I/Q generation components and limits symmetrical layout design for the I/Q vector summing and the bandwidth. The passive reflection-type phase shifters (RTPSs) based on the 90° directional hybrids have also been reported in [98–100]. The RTPS can provide not only high-resolution phase shifting by tuning the reflection load but also better linearity compared with the VSPS. However, the operating bandwidth for RTPS is limited by the 90° directional hybrid's intrinsic frequency feature. Besides, multiple DACs are mandatory for the precise bias control of such RTPS. To mitigate such drawbacks, the passive mixed-type phase shifter (MTPS) is proposed by combining the switch-type phase shifter (STPS) and RTPS, where the RTPS serves as the fine-tuning stage for higher PS resolution requirements. The MTPS desires a dedicated design for each phase-shifting stage and needs an additional 180° phase-shifting stage. However, it can provide relatively wide bandwidth by optimizing each stage and the additional techniques to compensate for the switch transistors' frequency response, which can be a good candidate for next-generation communications with a simple digital control algorithm.

	Active Vector-Summing PS	Passive Vector-Summing PS	Passive Mixed-Type PS
Architecture	PPF/QAF * w/ VGA	Hybrid CPL w/ Bi-Phase Modulator	Combination of STPS and RTPS
☺ Pros	• Additional RF Gain	• No Pdc	• No Pdc • Better PVT features • Wide BW
☹ Cons	• Bi-dir. cores required • Symmetrical Layout • Multiple VGAs • Limited BW	• Symmetrical Layout • Limited BW	• Dedicated design for each stage • Need 0/180-deg flip

* PPF: Poly-Phase Filter
QAF: Quadrature All-Pass Filter

Figure 3.19: Summary of phase shifter architectures.

3.4.2 28-GHz Balanced Active Bi-Directional Phase Shifter

The usage of active phase shifters further helps the bi-directional beamformers to shrink in size [9]. The area consumption overhead for gain compensation, which is required in beamformers with passive phase shifting solutions, can be removed. However, conventional bi-directional active vector-summing phase shifters (VSPS) (Fig. 3.20 (a)) based on the switchable poly-phase filters (PPFs) suffer from imperfect switching operation. The parasitic resistance of switches introduces unbalanced vector summing. Complicated control tables are required for compensating the magnitude and phase errors. Additionally, the overall achievable RF-path gain is degraded by using multiple switchable PPFs.

To address these issues, Fig. 3.20 (b) presents the balanced active bi-directional phase shifter in this work. The proposed phase shifter consists of a non-switchable PPF, bi-directional VGAs A1 and A3 for the I path and bi-directional VGAs A2 and A4 for the Q path. The VGA circuits for A1 to A4 are similar to the neutralized bi-directional gain amplifier. Two bi-directional cores with flipped output are included for covering the complete 360° phase shifting in vector-summing operation. Fig. 3.20 (c) and (d) further explain the TX-mode and RX-mode operations, respectively. In TX mode, the generated I/Q signals by the PPF are first sent to A1 and A2. Due to their constant input impedance, A1 and A2 will directly function as the I/Q VGAs. In this condition, A3 and A4 will be set with fixed gain and serve as another driving stage for the PA. Balanced I/Q summing and improved linearity over phase shifting could be achieved in TX mode. In RX mode, the PPF can operate as the quadrature adder with its reciprocal characteristic. However, the orthogonality of PPF is sensitive to the mismatch between the I/Q input impedances. Therefore, A3 and A4 in RX mode will function as the I/Q VGAs, while A1 and A2 with

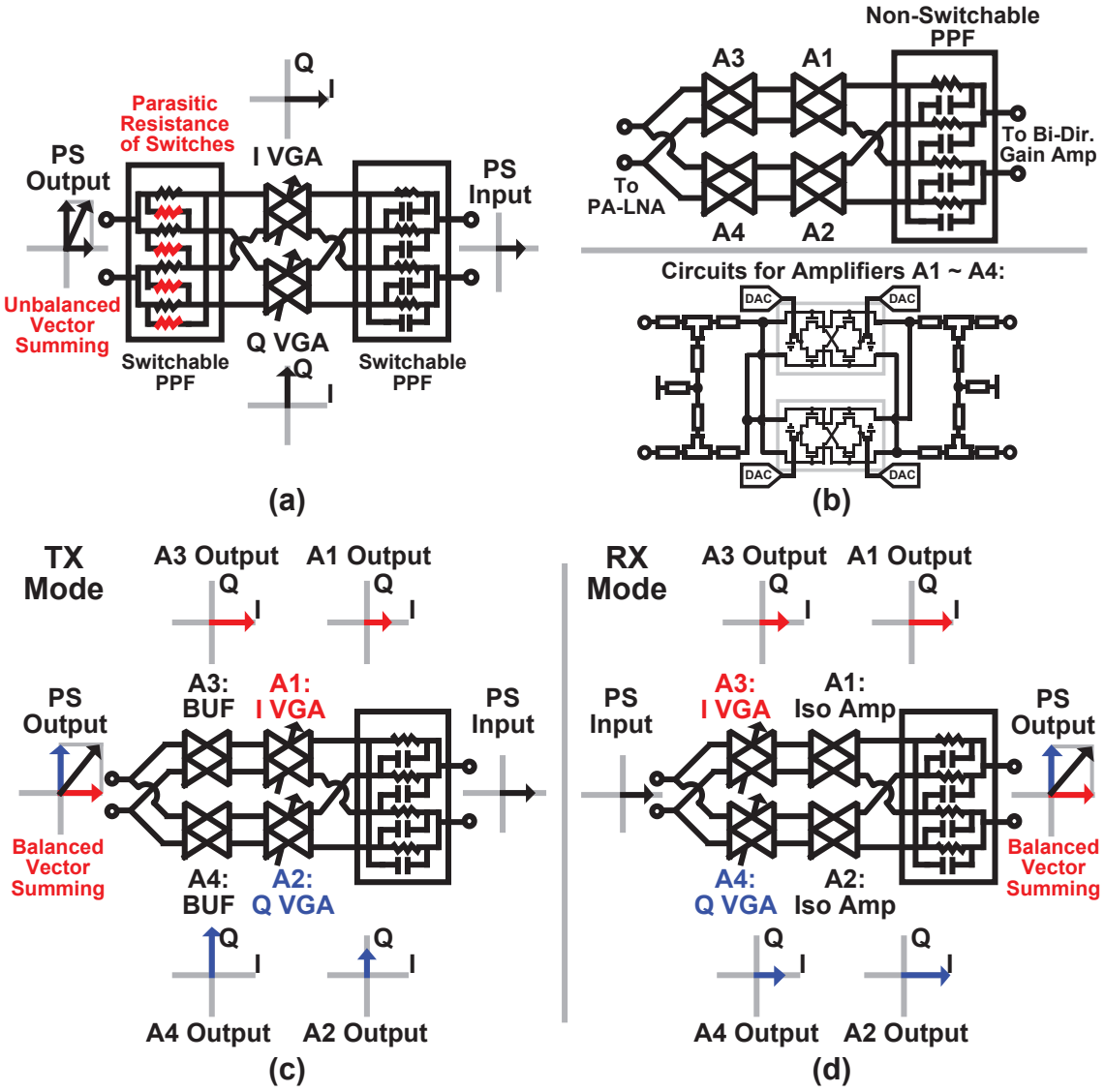

Figure 3.20: Block diagrams of (a) conventional active bi-directional phase shifter and (b) proposed balanced active bi-directional phase shifter. Operations of proposed phase shifter in (c) TX mode and (d) RX mode.

fixed gain will serve as the isolation buffers. Identical I/Q input impedances could be provided to the PPF and balanced vector summing could also be realized in RX mode. Moreover, the overall gain performance of the proposed phase shifter is improved due to the usage of one single non-switchable PPF.

The non-switchable PPF used in this work is designed with tunable capacitance. It can be configured for different operating center frequencies. The frequency band from 26.5 GHz to 29.5 GHz is covered by the PPF. The I/Q imbalance caused by the process variation could also be compensated by the tunable capacitance through calibration. Fig.

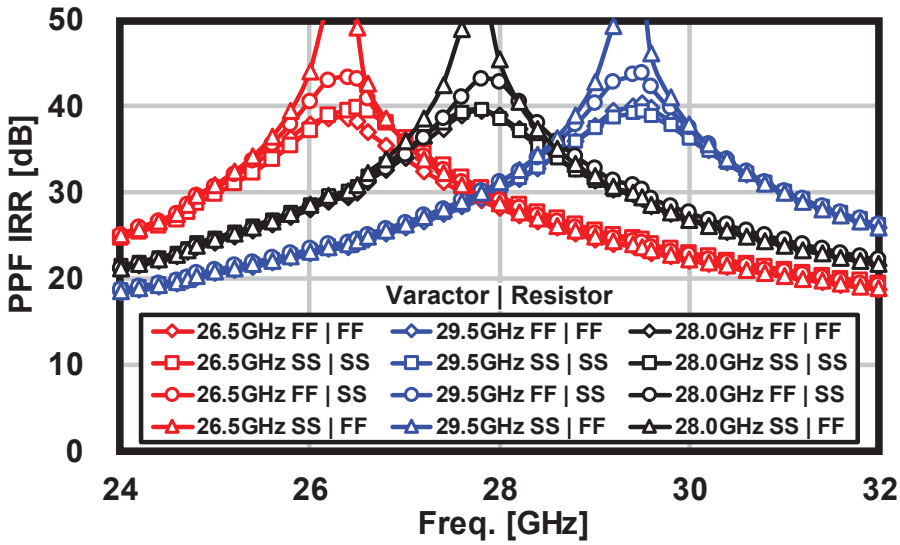

Figure 3.21: Simulated image rejection ratio of poly-phase filter over process corners after compensation.

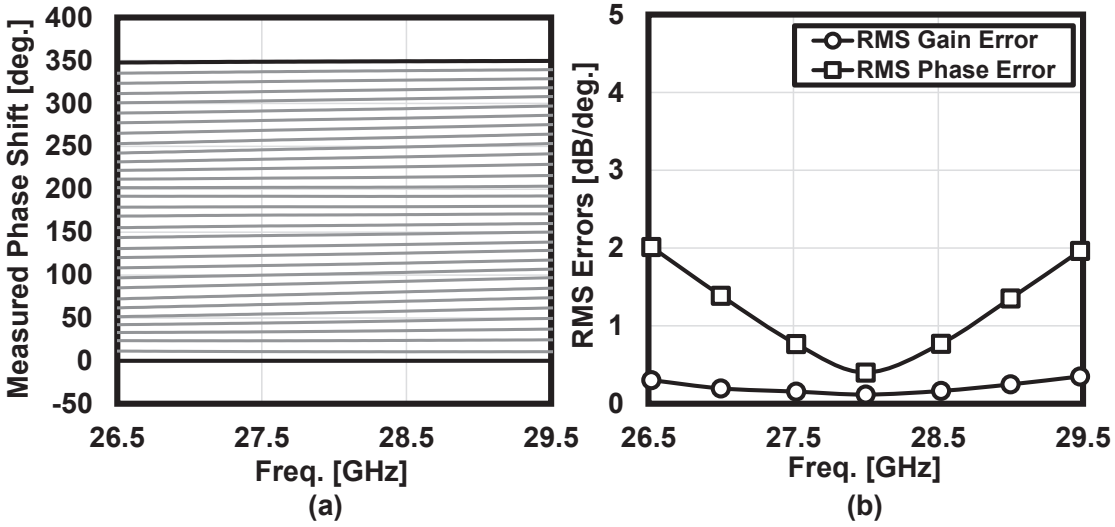

Figure 3.22: Measured (a) phase shifting and (b) RMS gain and phase errors for the proposed beamformer.

3.21 shows the simulated image rejection ratio (IRR) of the PPF in corner conditions after the compensation. Process corners of the varactors and resistors are considered in this simulation. Considering the 400-MHz channel bandwidth defined in 5G NR standard, the simulated IRRs are always better than 37.1 dB.

Fig. 3.22 demonstrates the measured phase shifting performance of the proposed beamformer. The PPF setting is fixed in this measurement. This work covers 360° phase

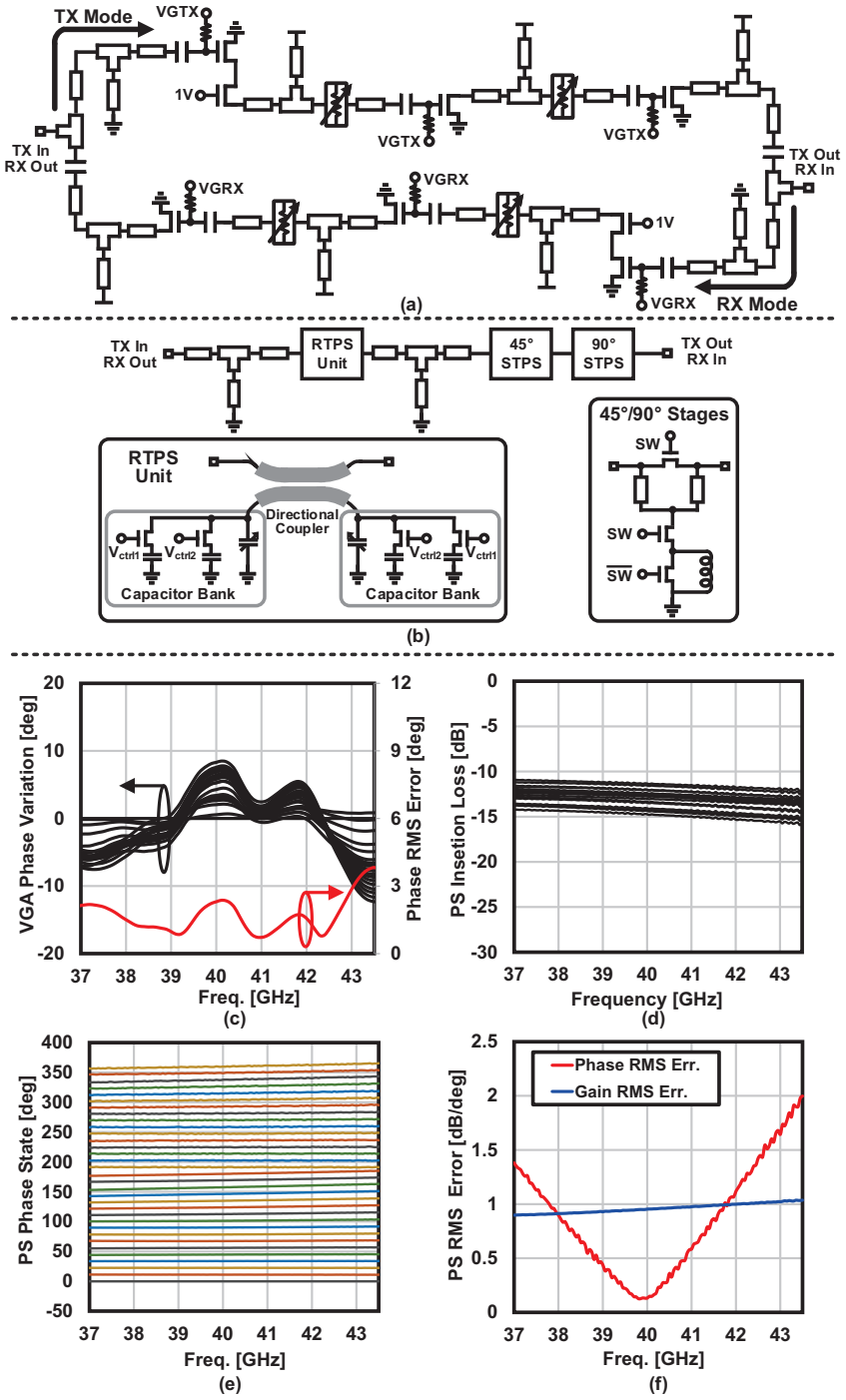

Figure 3.23: (a) Circuit schematics of single-ended three-stage bi-directional RF VGA. (b) Mixed-type RF phase shifter topology with (d) the measured insertion loss. Measured results of the single TX-mode beamformer element: (c) VGA additive phase variations, (e) phase-shifting coverage with the corresponding (f) phase and gain rms errors.

shifting. From 26.5 GHz to 29.5 GHz, the introduced RMS phase error and RMS gain error are less than 2° and 0.4 dB, respectively, without any compensation tables. The proposed phase shifter also realizes a 13-dB gain in TX mode and a 10-dB gain in RX mode. The PA could be directly driven by the phase shifter in this work. The area and power efficiencies of the proposed beamformer are further improved.

3.4.3 39-GHz Bi-directional VGA and Mixed-type Phase Shifter

A three-stage single-ended bi-directional VGA with attenuators is presented in Fig. 3.23(a). Two single-direction VGAs are connected end-to-end and controlled by mode-switching bias. The bi-directional operation is supported by limited power consumption. The single-ended topology is also convenient to fit the irregular layout shape. Fig. 3.23(b) shows the mixed-type RF phase shifter, composed of a reflection-type phase shifter (RTPS), a 45° switch-type phase shifter (STPS), and a 90° STPS. The 45° stage and 90° stage are both designed in a bridged-T type low-pass structure [101]. A 90° directional coupler with around 25-Ohm characteristic impedance is implemented in RTPS to enlarge the phase shift coverage. The tunable capacitive reflection load is designed with two switching capacitors and a varactor, realizing the fine phase-tuning function. The 180° phase shift is fulfilled by swapping the outputs of the following differential stages. The measured insertion loss of the mixed-type PS is shown in Fig. 3.23(d). The Measurement results shown in Fig. 3.23(c,e,f) are based on the single TX-mode beamformer element. The additive phase variation introduced by the bi-directional VGA is demonstrated in Fig. 3.23(c) with the calculated phase rms error. Fig. 3.23(e) and (f) perform the measured beamformer phase coverage with the corresponding phase and gain rms error. 360° phase coverage is achieved from 37-GHz to 43.5-GHz band, less than 2.00° phase rms error and less than 1.03-dB gain rms error are obtained within the targeted 39-GHz band.

3.5 Summary

In this chapter, the element-beamformer building blocks are designed based on the neutralized bi-directional architecture for saving chip area and manufacturing costs. The bi-directional technique could reduce the occupied on-chip area for each beamformer. The stand-alone 28-GHz PA-LNA realizes 16.4-dBm saturated output power with a 32% peak PAE in PA mode. It also achieves good linearity with a 14.9-dBm P_{1dB}. In LNA-mode, 4.4-dB~5.3-dB NF is realized from 26.5GHz to 29.5GHz band. A 39-GHz bi-directional Doherty PA-LNA is proposed to enhance the power PBO efficiency regarding the high PAPR 5G signals, meanwhile costing down the system by the unbalanced neutralized

Table 3.1: Summary of the bi-directional PA-LNA design history

Year	2018*	2019*	2018#	2019*	2020*	2021*
Ref.	[9] JSSC2020	[10] JSSC2021	[34] RFIT2018	-	[102] ELEX2023	[103] JSSC2023
Topology	PA-LNA Core v1	PA-LNA Core v2	Diff. PA	PA-LNA Core v2	Doherty PA	Doherty PA-LNA Core v3
Freq. [GHz]	28	28	39	39	41	39
Psat [dBm]	15.4	16.4	16.3	16.2	19.4	18.9
OP1dB [dBm]	13.0	14.9	14.9	13.9	18.6	17.0
PAE_{PEAK} [%]	20	32	30.3	26.5	30.4	30.4
PAE @6-dB PBO [%]	4	9	-	8.2	19.2	17.8
NF [dB]	4.6	<5.3	-	5.1	-	4.8
Core Chip Area [mm^2]	0.11	0.11	0.08	0.11	0.22	0.22

* My own work.

Previous work in our lab.

bi-directional operation. The measured stand-alone Doherty PA-LNA achieves 18.9-dBm saturated output power with 17.8% PAE at 6-dB PBO in PA mode and obtains a 4.8-dB NF at 40GHz in LNA mode. Table 3.1 summarizes the design history of the bi-directional PA-LNA. Based on the optimized final version of the unbalanced neutralized bi-directional PA-LNA core, the bi-directional Doherty PA-LNA achieves closer performance towards the stand-alone Doherty PA.

The area-efficient bi-directional PSs are also proposed with 360° phase coverage. The measured rms phase and rms gain errors are less than 2° and 1.1dB, respectively. Table 3.2 compares the phase shifters for 5G applications with the proposed phase shifters in this thesis. The research demonstrated in this chapter is the foundation for the phased-array system designs.

Table 3.2: Comparison of the phase shifters for 5G applications

	This Work		[104] IEICE2020	[105] ICTA2020	[106] RFIC2020
Architecture	Active VSPS	MTPS	Active VSPS	STPS	Passive VSPS
Freq. [GHz]	28	39	28	39	39
$Gain_{avg}$ [dB]	10	-13	3.7	-11.6	-17.8
Coverage [°]	360	180	360	180	360
Gain Err_{rms} [dB]	<0.4	<1.03	<0.2	<0.4	<0.28
Phase Err_{rms} [°]	<2	<2	<1.2	<3.1	<1.1
P_{DC} [mW]	20	0	25.2	0	0
Core Chip Area [mm^2]	0.27	0.17	0.32	0.15	0.14

Chapter 4

Power-Efficient Phased-Array DP-MIMO System

4.1 Introduction

Based on the 5G requirement introduction in Chapter 2 and the beamformer-element building blocks designed in Chapter 3, this chapter focuses on the system challenges and targets for the high-data-rate power-efficient phased-array beamformer designs. This chapter mainly comprises two key ideas: the cross-polarization cancellation to support DP-MIMO better and the inter-element mismatch compensation to improve the DPD performance in phased-array applications. Both the proposed techniques enhance the available EIRP and system power efficiency.

4.2 Cross-Polarization Leakage Cancellation

4.2.1 Millimeter-Wave DP-MIMO Communications

As demonstrated in Fig. 4.1(a), 5G millimeter-wave DP-MIMO systems utilize the cross-pol. isolation between H-pol. and V-pol. to simultaneously transmit two data streams. To evaluate the performance of the idea DP-MIMO systems, the channel capacity under 2×2 DP-MIMO configuration could be represented with Eq. (4.1) [31, 107].

$$C = B\log_2\left[\det\left(\boldsymbol{I} + \frac{\gamma_0}{\mathrm{n}}\boldsymbol{H}^{\mathrm{H}}\boldsymbol{H}\right)\right] \tag{4.1}$$

In this equation, B is the channel bandwidth and γ_0 is the signal-to-noise ratio (SNR). n = 2 is selected here to keep the total transmitted power constant in DP-MIMO. The channel information is included in the 2×2 channel matrix $\boldsymbol{H}$. For ideal line-of-sight (LOS) DP-

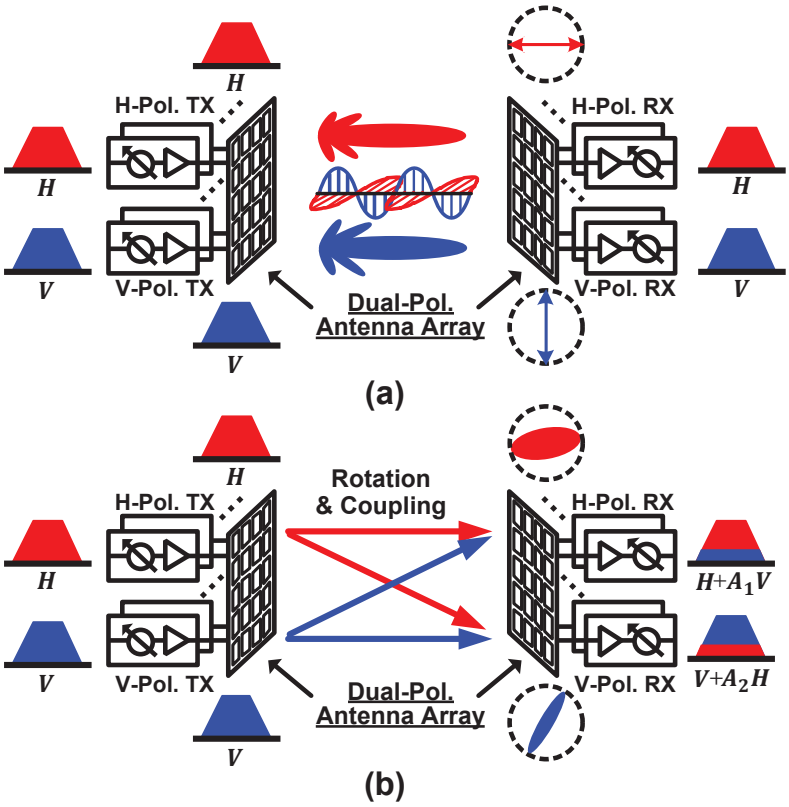

Figure 4.1: (a) Ideal dual-polarized multiple-in-multiple-out (DP-MIMO) operation. (b) DP-MIMO operation with rotation and coupling during propagation.

MIMO operation, the H-pol. and V-pol. signals are completely isolated. Therefore, the channel matrix $\boldsymbol{H}_{\text{ideal}}$ could be represented as follows

$$\boldsymbol{H}_{\text{ideal}} = \begin{bmatrix} e^{j\varphi_{11}} & 0 \\ 0 & e^{j\varphi_{22}} \end{bmatrix} \tag{4.2}$$

In $\boldsymbol{H}_{\text{ideal}}$, φ_{11} and φ_{22} denote the phase shifting caused by propagation. Considering a communication distance of d, φ_{11} and φ_{22} could be derived with $2\pi\frac{d}{\lambda}$. By applying $\boldsymbol{H}_{\text{ideal}}$ to Eq. (4.1), the ideal DP-MIMO channel capacity could be calculated with Eq. (4.3).

$$C_{\text{ideal}} = B\log_2\left(1 + \frac{\gamma_0}{2}\right)^2 \tag{4.3}$$

From Eq. (4.3), we can find that using DP-MIMO in ideal conditions significantly boosts the channel capacity. While in the real case, the rise of cross-pol. leakage will always limit the achievable DP-MIMO capacity. As shown in Fig. 4.1(b), both the coupling from the antenna and the polarization rotation due to module placement can generate such

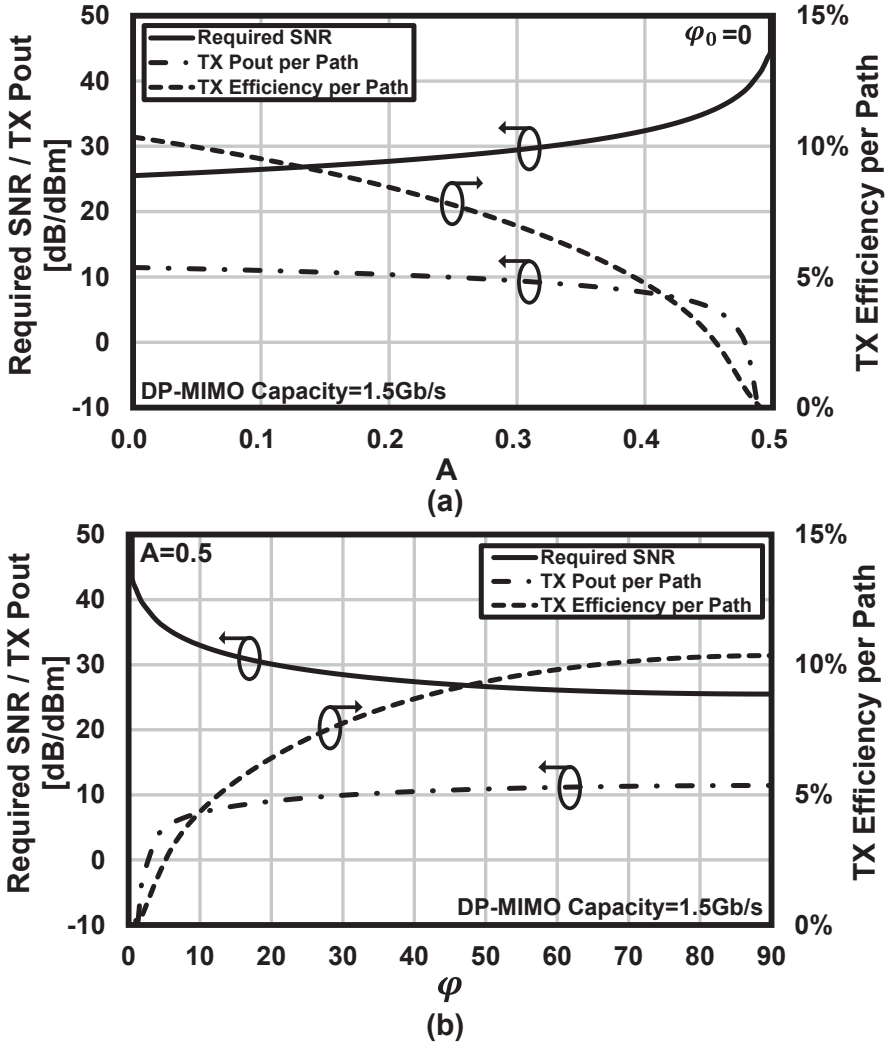

Figure 4.2: Calculated required SNR, available TX output power, and TX efficiency against (a) A and (b) φ_0.

leakages. To explore their influence on channel capacity, the channel matrix $\boldsymbol{H}_{\text{leak}}$ under leakage condition could be represented as follows

$$\boldsymbol{H}_{\text{leak}} = \begin{bmatrix} \sqrt{1-\alpha}e^{j\varphi_{11}} & \sqrt{\beta}e^{j\varphi_{21}} \\ \sqrt{\alpha}e^{j\varphi_{12}} & \sqrt{1-\beta}e^{j\varphi_{22}} \end{bmatrix} \tag{4.4}$$

Here, $\sqrt{\alpha}$ and $\sqrt{\beta}$ are the magnitudes of the cross-pol. leakage components, where $0 \leq \alpha \leq 1$ and $0 \leq \beta \leq 1$. The phase of the leakages are denoted with φ_{12} and φ_{21}. The corresponding channel capacity C_{leak} could be derived by applying $\boldsymbol{H}_{\text{leak}}$ to Eq. (4.1). The calculated result is shown in Eq. (4.5) (the bottom of the next page). If we assume $\alpha = \beta = A$ and $\varphi_{21} - \varphi_{11} = \varphi_{12} - \varphi_{22} = \varphi$, the channel capacity under leakage condition

could be further simplified with Eq. (4.6).

$$C'_{\text{leak}} = B\log_2\left[\left(1+\frac{\gamma_0}{2}\right)^2 - \frac{\gamma_0}{2}A(1-A)(\cos 2\varphi + 1)\right] \tag{4.6}$$

From Eq. (4.6), we can find the first term inside the brackets of C'_{leak} is the same as the one inside C_{ideal}. While the second term, which is always negative, represents the capacity degradation caused by the cross-pol. leakages. The worst condition is obtained when A=0.5 and φ=0°. The corresponding channel capacity C''_{leak} could be represented with Eq. (4.7), which is the channel capacity for a single-in-single-out (SISO) scenario.

$$C''_{\text{leak}} = B\log_2(1+\gamma_0) \tag{4.7}$$

To compensate for the degradation caused by the cross-pol. leakage, the channel SNR γ_0 is required to be improved. Fig. 4.2(a) and (b) demonstrate the required γ_0 against A and φ, respectively. The DP-MIMO capacity is fixed at 1.5 Gb/s in this calculation, and the channel bandwidth is 100 MHz. In 5G millimeter-wave transceivers, the channel SNR γ_0 is usually dominated by the transmitter side. The transmitter will require additional power back-off (PBO) to improve γ_0. Thus, the system power efficiency will be in turn degraded. An example for explaining the efficiency degradation is also presented in Fig. 4.2.

As shown in Fig. 4.3(c) and (d), conventional 5G MIMO operation usually relies on the receiver digital baseband (DBB) or an analog-domain leakage cancellation. However, the channel capacity cannot be recovered regarding severely-coupled MIMO channels and the TRX nonlinearity. In DP-MIMO, this situation becomes even worse because of the H-pol. and V-pol. streams usually come from the same directions. The cross-pol. leakage before the receiver DBB or the leakage cancellation worsens the TX-to-RX linearity. In this condition, the transmitter EVM must be further improved, leading to larger PBO and lower power efficiency, as mentioned previously. To improve the DP-MIMO capacity without sacrificing power efficiency, the cross-pol. leakage cancellation is required to be performed at the transmitter side. This function could be realized at the transmitter digital baseband as shown in Fig. 4.3(a) and (e). However, the digital processing regarding the multi-Gb/s data rate in 5G is power-hungry. An additional resolution will also be required for the digital-to-analog converters (DACs) to support accurate cancellation, which

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$$C_{\text{leak}} = B\log_2\left[\left(1+\frac{\gamma_0}{2}\right)^2 - \frac{\gamma_0^2}{4}(\alpha+\beta-2\alpha\beta+2\sqrt{\alpha\beta(1-\alpha)(1-\beta)}\cos(\varphi_{12}+\varphi_{21}-\varphi_{11}-\varphi_{22})\right] \tag{4.5}$$

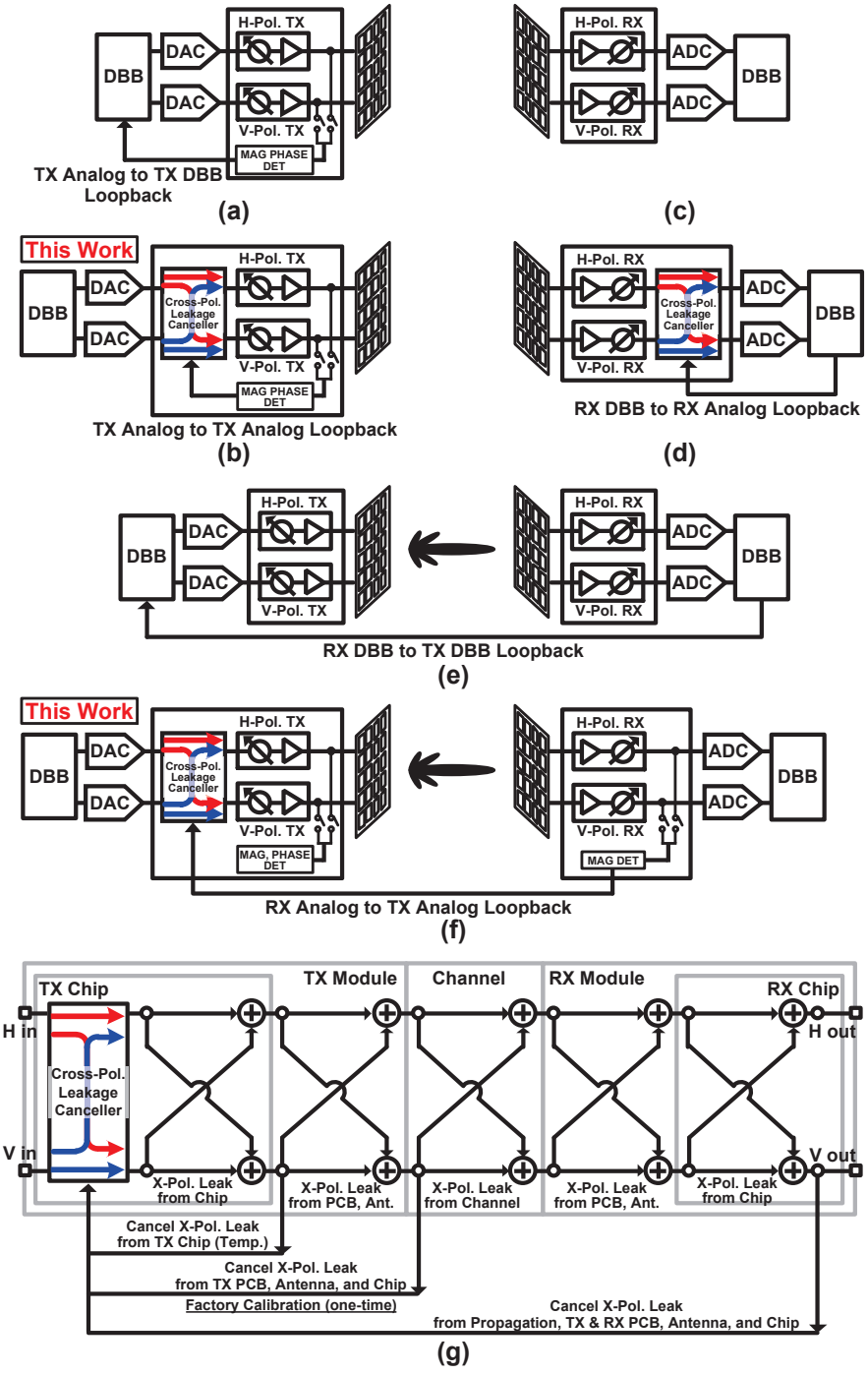


Figure 4.3: Cross-pol. leakage cancellations with (a) TX analog to TX digital baseband (DBB) loopback, (b) TX analog to TX analog loopback, (c) RX DBB, (d) RX DBB to RX analog loopback, (e) RX DBB to TX DBB loopback, and (f) RX analog to TX analog loopback. (g) Signal flow chart for the proposed cancellation technique.

is power-consuming. Therefore, a power-efficient analog-assisted cross-pol. leakage cancellation technique is introduced in this work. Fig. 4.3(b) shows the operation of the proposed technique. A cross-pol. leakage canceller is utilized for generating the cancellation signals. This TX analog loopback cancellation is suitable for communications with multiple user equipment. The calibration signal can be a single tone or modulated signal in the real use case, while the ERIP must obey the limitation of no more than 55-dBmMHz. The envelop detector is required when using a modulated signal as the calibration signal. Fig. 4.3(g) shows the signal flow chart of the proposed cancellation. A one-time factory calibration could initially decide the settings of the canceller. During the transmitter operation, a magnitude and phase loopback calibration could be performed to compensate for the temperature variation. Regarding severely-coupled DP-MIMO channels, a receiver-to-transmitter loopback cancellation, similar to precoding, could be further performed as shown in Fig. 4.3(f). If the latency requirement is relaxed, the strength of the leakage signals could be detected at the receiver side and sent back to the transmitter for this cancellation. The cross-pol. leakages introduced from the transmitter to the receiver could be cancelled by the proposed cancellation technique in this condition.

The proposed canceller is designed based on the vector modulator. Regarding a leakage component $A_L e^{j\varphi_L}$, the achievable suppression ratio with a cancellation signal $A_C e^{j\varphi_C}$ could be calculated with the following equation

$$\begin{aligned} LeakageSupp. &= \frac{|A_L e^{j\varphi_L}|}{|A_L e^{j\varphi_L} + A_C e^{j\varphi_C}|} \\ &= 20\log\frac{1}{\sqrt{\Delta A^2 + 2\Delta A\cos\Delta\varphi + 1}}(dB) \end{aligned} \tag{4.8}$$

In this equation, $\Delta A = \frac{A_C}{A_L}$ is the magnitude error and $\Delta\varphi = \varphi_C - \varphi_L$ is the phase error. Fig. 4.4 presents the calculated suppression ratio against the corresponding ΔA and $\Delta\varphi$. To maintain an over 40-dB cross-pol. leakage suppression ratio, ΔA should be less than 0.3dB and $\Delta\varphi$ should be less than 1.8°. The proposed canceller is therefore designed with fine-grained phase tuning and magnitude tuning for a high-accuracy and fast cancellation.

4.2.2 Cross-Pol. Leakage Canceller

To improve the DP-MIMO EVMs and the corresponding system power efficiency, a high-accuracy cross-pol. leakage cancellation circuit is introduced in this work. Fig. 4.5 shows the block diagram of the proposed cross-pol. leakage canceller. It comprises two bi-directional variable gain amplifiers (VGAs) and two cross-pol. leakage cancellation paths. The proposed canceller can be configured into three operating modes. In normal TX mode, the H/V bi-directional VGAs operate in TX mode and the H/V cancellation

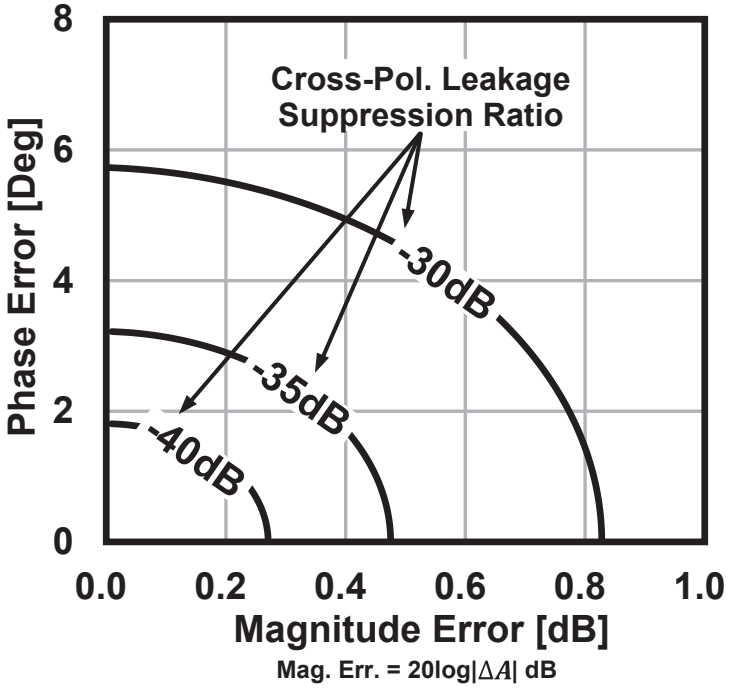


Figure 4.4: Calculated cross-pol. leakage suppression ratio against ΔA and $\Delta\varphi$.

paths are disabled. The RX mode operation is similar to the normal TX mode. Only the RX-mode H/V bi-directional VGAs are turned on to support the bi-directional operation. In cross-pol. leakage cancellation mode, the cancellation paths are operating together with the TX-mode H/V bi-directional VGAs. The required H-to-V and V-to-H cancellation signals are created by the magnitude and phase control circuits along the cancellation paths.

The cancellation path in this work is designed to realize high-resolution and orthogonal magnitude and phase tunings. Each cancellation path includes two VGAs and a phase shifter. Fig. 4.6(a) shows the circuit schematic of the VGA. The VGA is designed with a cascode stage, a common-source stage and an adjustable attenuator. The passive components for matching are designed based on the low-loss and configurable transmission lines (TLs). To realize high-resolution magnitude tuning, a 10-bit DAC is utilized to control the adjustable attenuator. A shunt TL stub is connected to the attenuator to compensate for the parasitic capacitance and suppress the phase variation.

Fig. 4.6(b) shows the circuit schematic for the cancellation phase shifter. The reflection-type phase shifter is selected here to achieve fine phase shifting with minimized insertion loss and area [100, 108]. The 90° directional coupler is realized with two top-thick metal layers. The phase difference between the through port and the coupling port is optimized in electromagnetic (EM) simulations. The reflection load in this work includes two se-

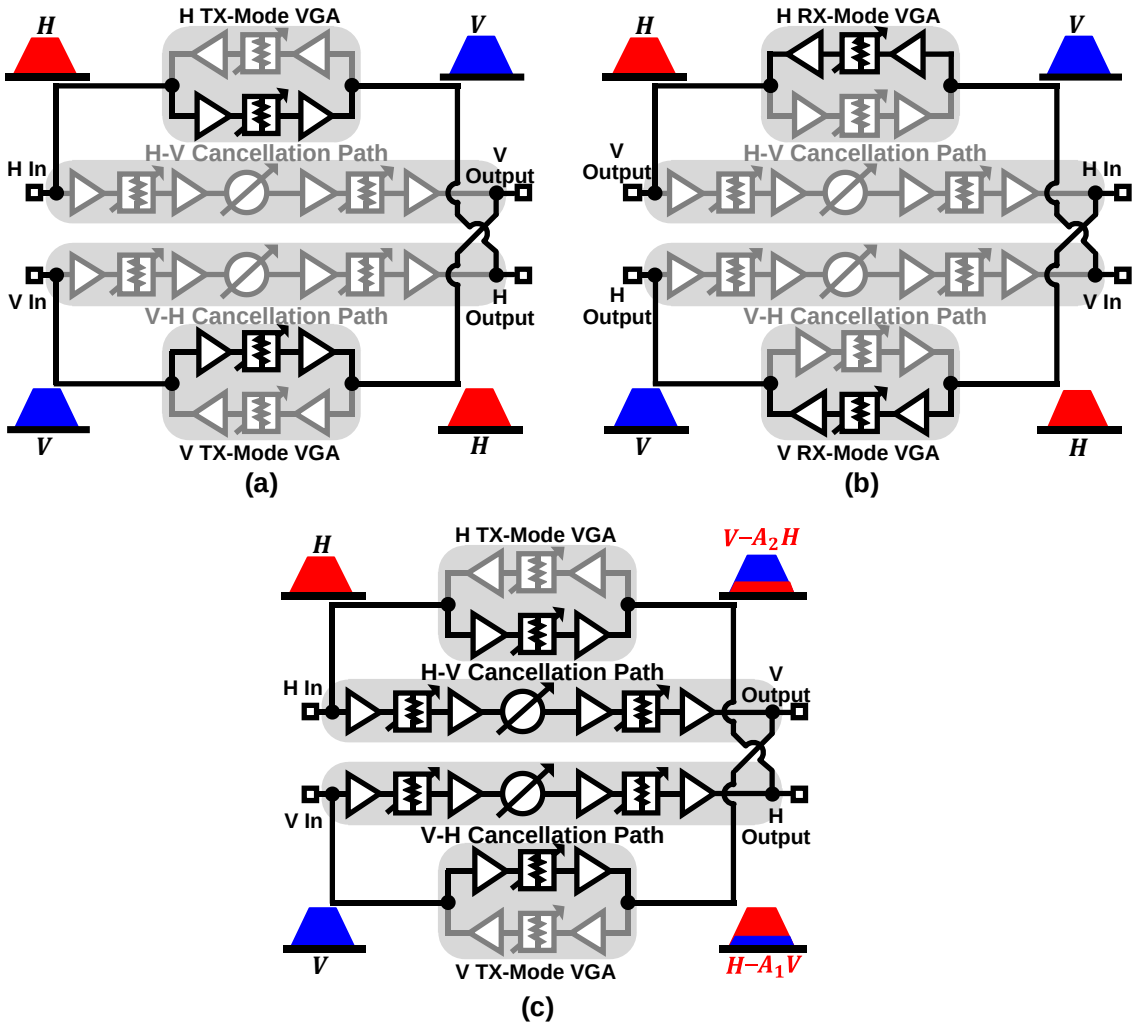


Figure 4.5: Block diagrams of proposed cross-pol. leakage canceller in (a) TX mode, (b) RX mode, and (c) cross-pol. leakage cancellation mode.

ries of LC resonators with different resonating points. 360° gain-invariant phase shifting could be obtained with the dual-voltage control. The occupied area for the phase shifter is 0.16mm^2. Further area reduction could be realized using switch-type phase shifters and the resonator-based fine-tuning stage.

Fig. 4.6(c) presents the circuit schematic of the H/V single-ended bi-directional VGAs. Two single-direction VGA chains are directly combined to support the bi-directional operation with a minimized area. The mode selection is realized by switching the bias.

Fig. 4.7(a) and (b) summarize the measured variable gain performance of the cancellation path with a 2-dB tuning step. The simulated single-stage VGA performance with transistor process corners is also included. Two VGAs in this work provide a 32-dB gain tuning range. The achieved tuning resolution is less than 0.2dB with the help of the high-

resolution DACs. Furthermore, the measured phase variation overall gain tuning states is less than 2.3° at 28GHz. Phase-invariant gain tuning is obtained by the cancellation path. Fig. 4.7(c) and (d) present the phase-shifting performance of the cancellation path. The simulated phase coverage over process corners of the varactor and MOM capacitor are also included. 360-degree phase shifting could always be achieved from 26.5GHz to 29.5GHz in both simulation and measurement. The corresponding RMS gain error over the whole 5G 28-GHz band is less than 0.98dB.

The cancellation performance in this work is further evaluated over temperature and supply voltage. Four H-pol. and four V-pol. transmitters along with the cancellation circuits are utilized for this simulation. The outputs of H-pol. transmitters and V-pol. transmitters are ideally combined, respectively. Before the cancellation, around -10-dB cross-pol. coupling is manually added between the output nodes of H-pol. and V-pol. transmitters. Fig. 4.8(a) demonstrates the H-to-V isolations with different cancellation temperatures. With a cancellation at 27°C, the cross-pol. isolation is always better than 20dB from -40°C to 120°C. Within 0°C to 60°C, the cross-pol. isolation is better than 30dB. Fig. 4.8(b) presents the H-to-V isolations over different supply voltages. With a cancellation at 1-V, the cross-pol. isolation is always better than 23dB considering ±5% supply voltage variation.

4.2.3 28-GHz Phased-Array Beamformer

Fig. 4.9 shows the block diagram of the proposed 28GHz beamformer chip. Area-efficient neutralized bi-directional architecture is employed to share the same signal chain between the TX and RX [9]. Totally eight element-beamformers (4H+4V) are integrated to support the DP-MIMO. In this work, the magnitude and phase detection circuits along with on-chip coupling networks are implemented to the chip. The output signals from each element-transmitter could be selected and distributed to the on-chip detection block through the coupling network. The signals will be down-converted to a much lower frequency for accurate detection. A cross-pol. leakage canceller mentioned in the previous section is also inserted at the H/V combining port for suppressing the cross-pol. leakage introduced from the polarization coupling and rotation. This work could maintain low-cost, power-efficient and high-performance 5G DP-MIMO systems.

4.2.4 Measurements

The proposed phased-array beamformer chip is fabricated in a 65-nm CMOS process with WLCSP. Fig. 4.10 shows the chip micrograph, including the package. The chip size is 4mm × 4mm. Table 4.1 summarizes the core area consumption breakdown for

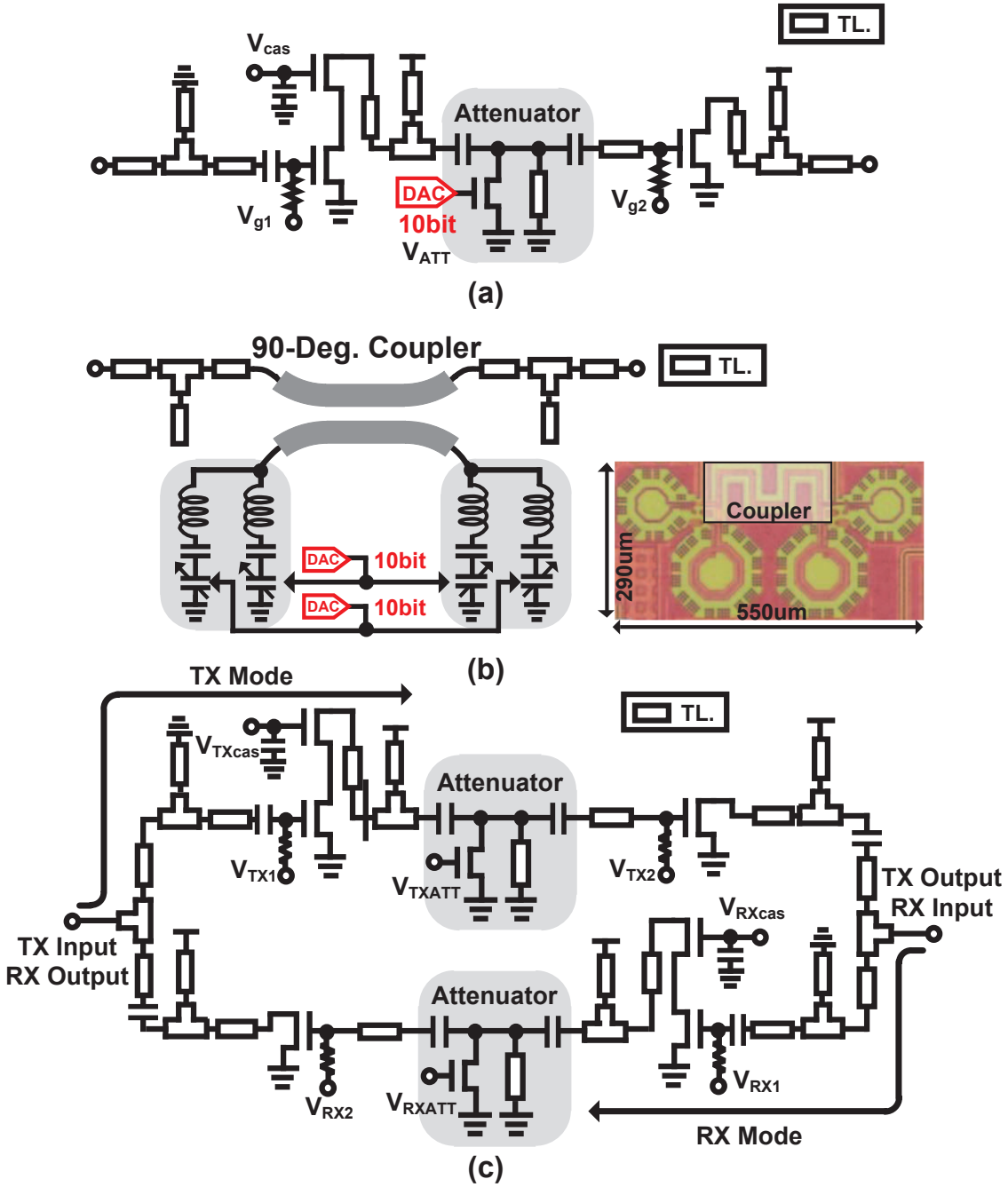


Figure 4.6: Circuit schematics of (a) single-ended variable gain amplifier (VGA), (b) reflection-type phase shifter in cancellation path, (c) and single-ended bi-directional variable gain amplifier.

the whole chip. Based on the compact neutralized bi-directional architecture, the proposed element-beamformer occupies only 0.48-mm^2 on-chip area. Table 4.1 also shows the power consumption breakdown. The proposed chip consumes 745mW in TX mode

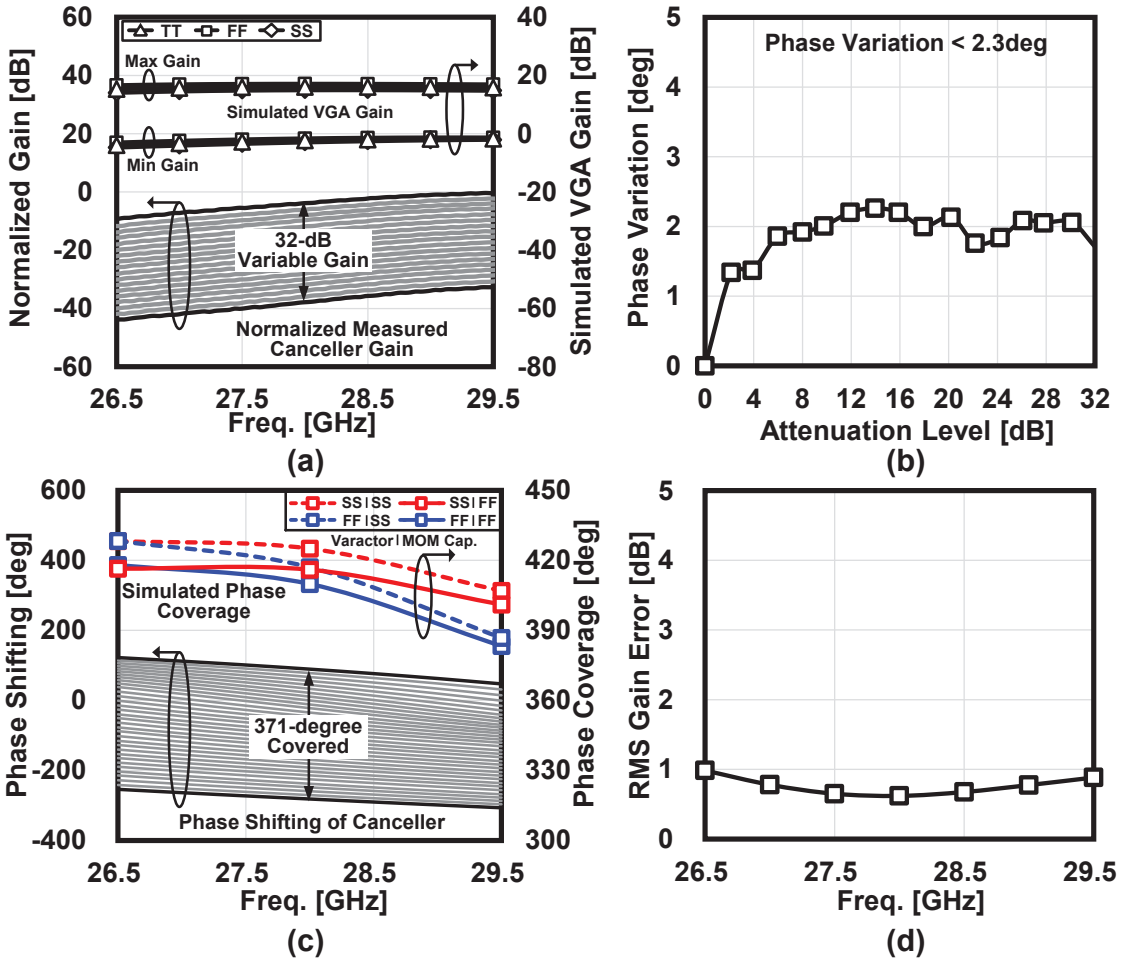


Figure 4.7: (a) Measured variable gain of the cancellation path and simulated tuning range of a single-stage VGA. (b) Phase variation of the cancellation path during gain tuning. (c) Phase shifting coverage and (d) the corresponding RMS gain error of the cancellation path.

and 352mW in RX mode for each polarization. Thus, the power consumption for each element-beamformer is 186mW in TX mode and 88mW in RX mode. The cancellation path introduced in this work only consumes 10mW. Thanks to the power-efficient circuits introduced in this work, a peak TX-mode efficiency of 22% per antenna path is achieved. High-efficiency and low-cost 5G millimeter-wave DP-MIMO systems could be realized by the proposed chip.

The on-wafer characteristics of the proposed chip are first evaluated. Fig. 4.11 summarizes the on-wafer measured performance of the single-path element-beamformer. The simulated performance with different temperatures is also provided. Fig. 4.11(a) and (c) show the measured TX-mode and RX-mode frequency responses. Within 26.5GHz to

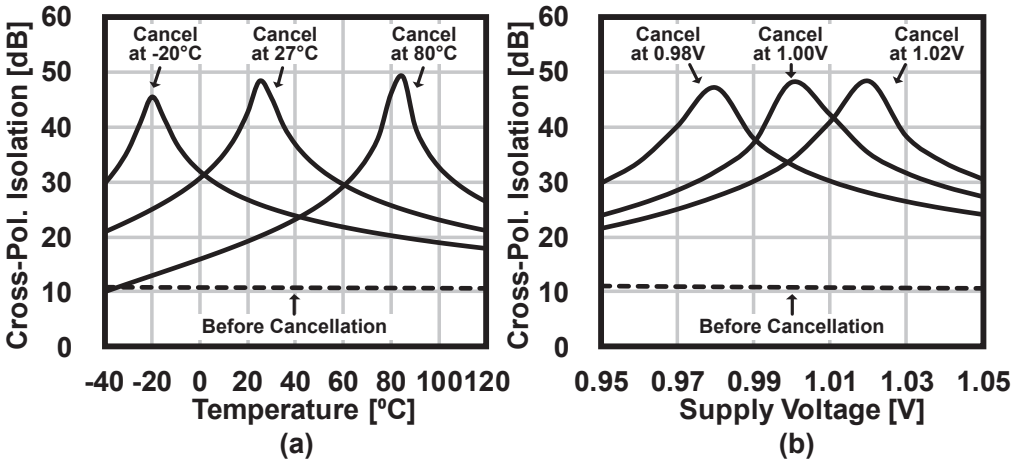


Figure 4.8: Simulated cross-pol. isolation against (a) the temperature and (b) the supply voltage.

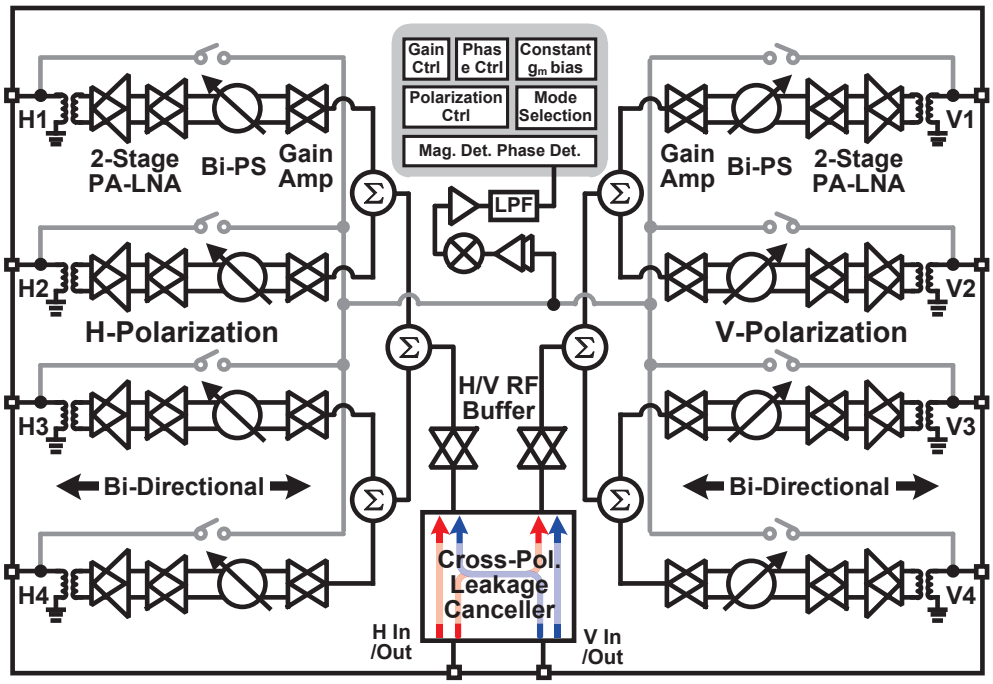


Figure 4.9: Block diagram of proposed bi-directional phased-array beamformer chip with cross-pol. leakage cancellation.

30.5GHz, the proposed beamformer achieves around 25-dB gain in TX mode and around 18-dB gain in RX mode. Fig. 4.11(b) presents the TX-mode linearity. The measured on-wafer saturated output power is 16.1dBm at 28GHz. The corresponding output P_{1dB} is 13.7dBm. Fig. 4.11(d) demonstrates the measured RX-mode NF. At 28GHz, the achieved

Table 4.1: Core Area and Power Consumption Breakdowns

Block		Sub-Block	Core Area [mm^2]	PDC [mW]	
Element Beamformer		PA-LNA	0.11	PA	132
				LNA	50
		Bi-Dir. Phase Shifter	0.27	TX	39
				RX	19
		Isolation Buffer	0.10	TX	10
				RX	11
Comb. Path		RF Buffer & VGAs	0.30	TX	21
				RX	32
		Canceller	0.42	10×2	

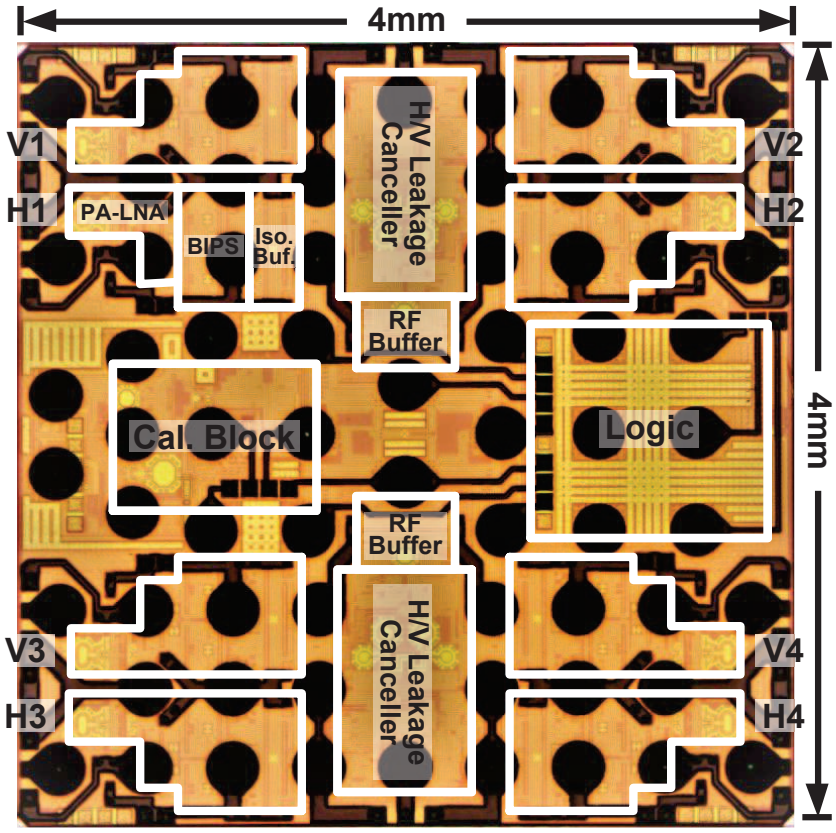


Figure 4.10: Die micrograph of the proposed 28-GHz beamformer chip.

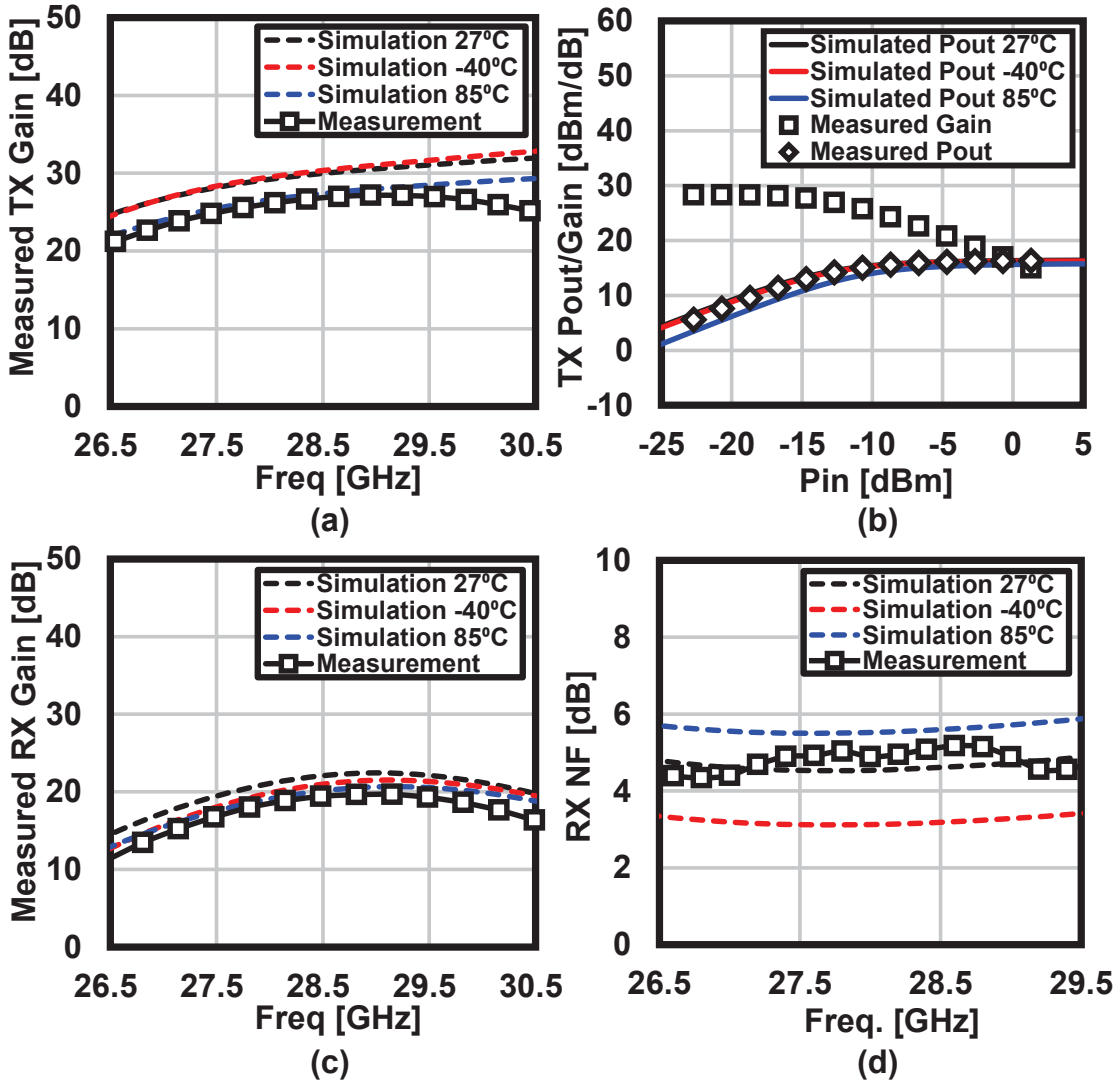


Figure 4.11: Simulated and measured (a) TX-mode gain, (b) TX-mode linearity, (c) RX-mode gain, and (d) RX-mode NF.

NF is 4.9dB.

The TX-mode beamformer is further evaluated with the modulated signals. Single-carrier-mode (SC-mode) and standard-compliant 5G NR OFDMA-mode signals are utilized in this measurement. Fig. 4.12(a) and (b) present the measured OFDMA-mode EVMs with 100-MHz and 400-MHz channel bandwidths, respectively. The measured EVMs are normalized to the RMS magnitude of the constellations. The peak-to-average power ratio (PAPR) for 400-MHz 64-QAM OFDMA-mode modulated signal is 11.6dB. When the output power P_{out} is low, the EVMs are dominated by the output noise floor. Therefore, in this region, the measured EVMs with 100-MHz bandwidth are better than the ones with 400-MHz bandwidth. When the P_{out} is large, the nonlinearity of the TX-

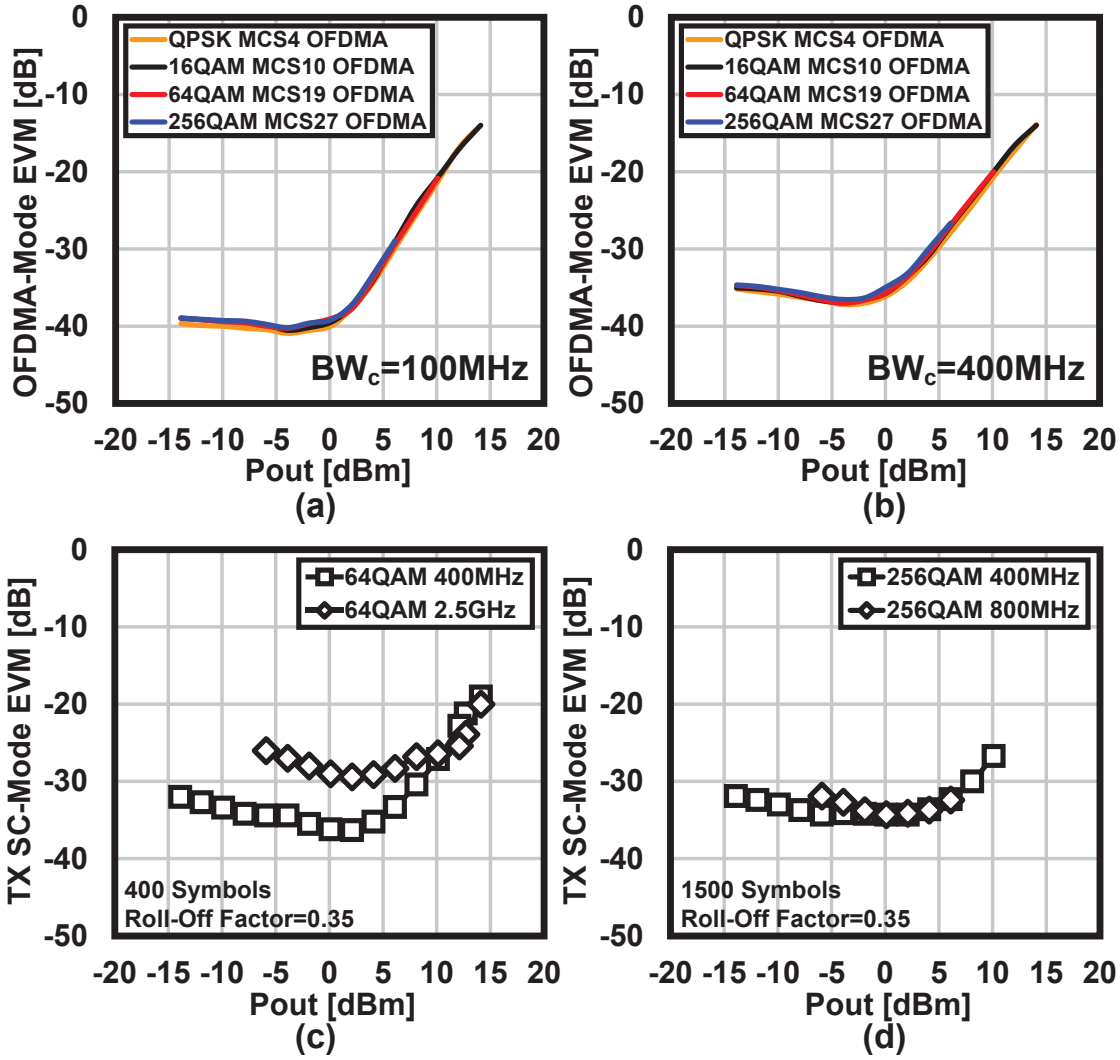


Figure 4.12: Measured OFDMA-mode EVMs with (a) 100-MHz bandwidth and (b) 400-MHz bandwidth for TX-mode beamformer. 5G NR MCS index table 2 for PDSCH is applied (Table 5.1.3.1-2 in 3GPP TS 38.214 V16.1.0.) Measured SC-mode EVMs (c) in 64-QAM and (d) in 256-QAM for TX-mode beamformer.

mode beamformer mainly decides the achievable EVMs. Thus, the measured EVMs are almost the same between Fig. 4.12(a) and (b) in large P_{out} region. This work achieves minimum 64-QAM EVMs of -40.3dB with 100-MHz bandwidth and -37.0dB with 400-MHz bandwidth. The measured 64-QAM output power is 7.1dBm, with an EVM of -25dB. A 256-QAM output power of 2.5dBm is also maintained with -32-dB EVM. Fig. 4.12(c) and (d) further demonstrate the measured EVMs with SC-mode modulated signals against the output power. Compared with the 5G NR OFDMA-mode signals, the SC-mode modulated signals have lower PAPRs (7.7dB for 64-QAM and 8.2dB for 256-

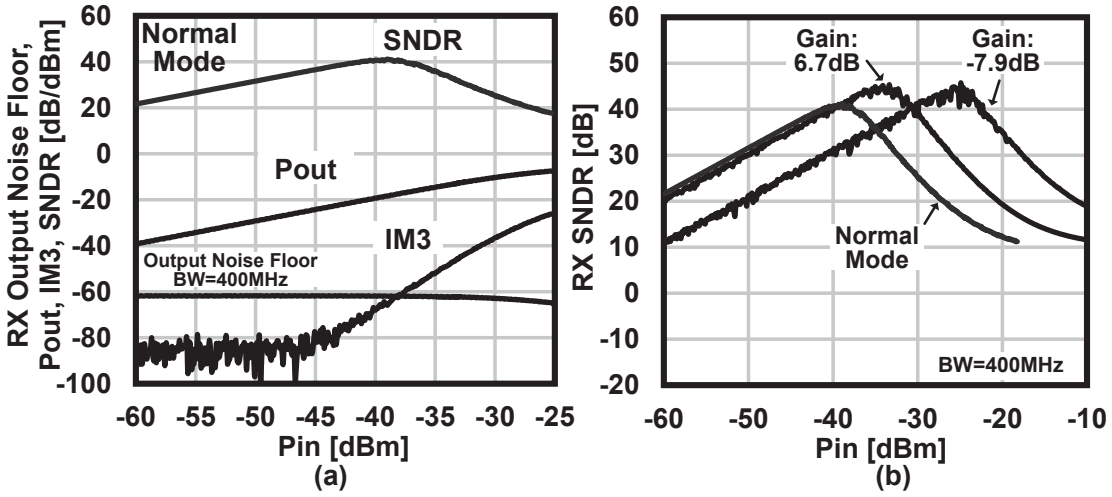


Figure 4.13: (a) Measured output power, output noise floor, IM3, and SNDR for RX-mode beamformer in normal-gain mode. (b) Measured RX-mode SNDRs with different gain settings.

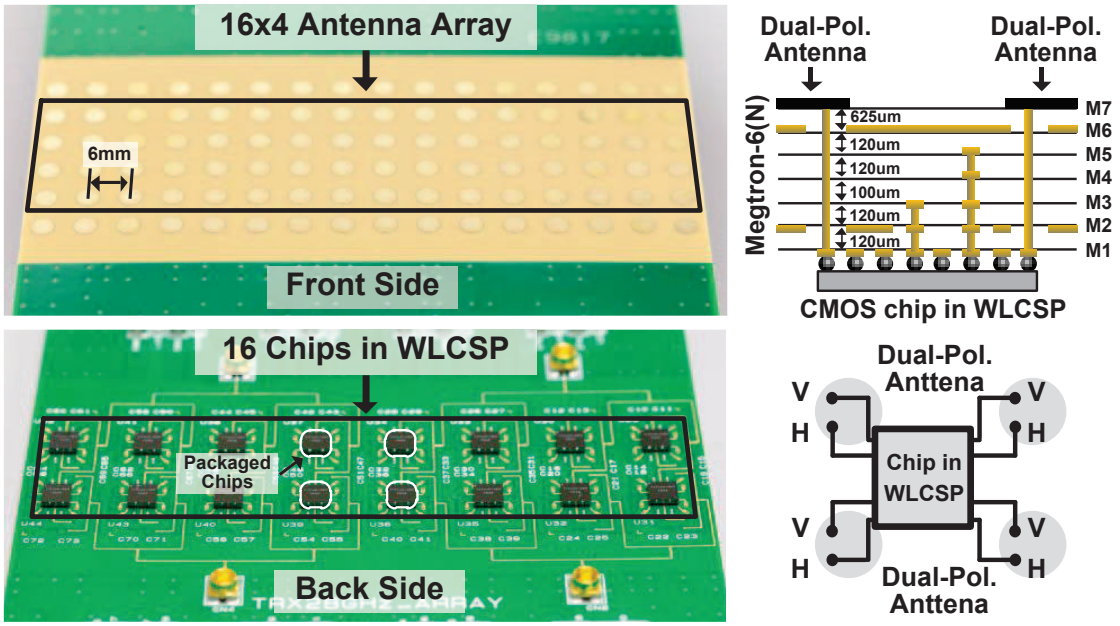


Figure 4.14: Photograph of proposed 64H+64V phased-array module.

QAM). Therefore, the EVMs of the TX-mode beamformer at large output power regions are improved. With 400-MHz channel bandwidth, the TX-mode beamformer in this work can deliver 11-dBm SC-mode output power in 64-QAM with -25-dB EVM. 6.1-dBm output power can also be supported in 256-QAM with -32.4-dB EVM.

Fig. 4.13(a) demonstrates the measured performance of the RX-mode beamformer.

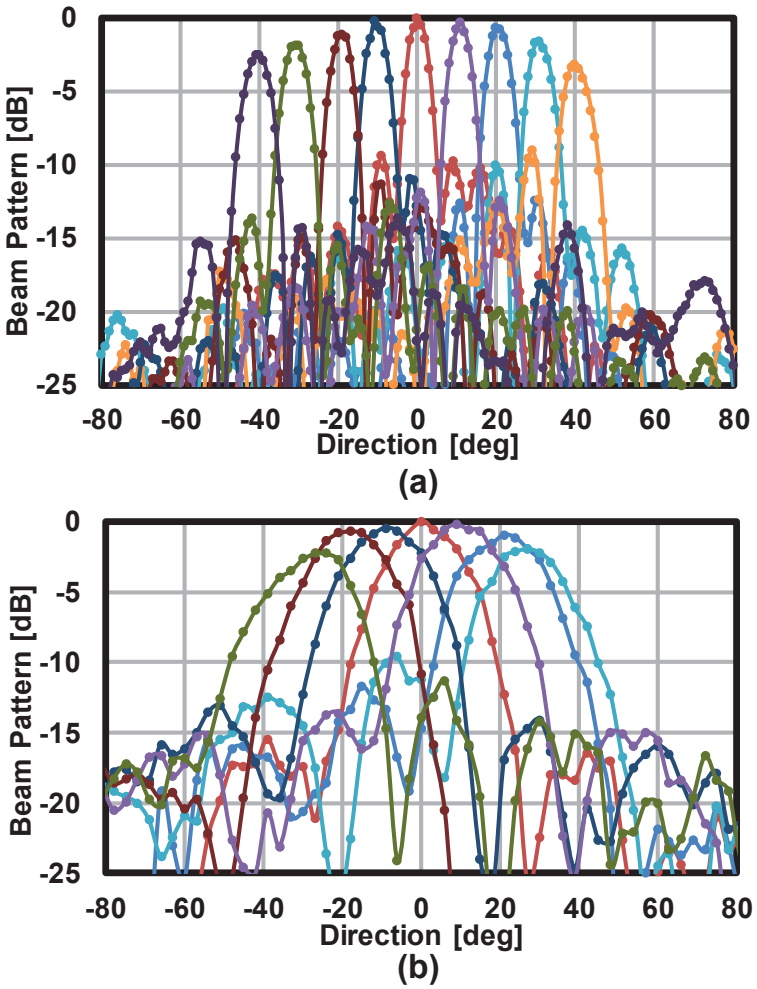


Figure 4.15: Measured beam patterns in (a) azimuth plane and (b) elevation plane.

The output power, output noise floor and IM3 are measured at 28GHz against the input power. The input P_{1dB} is -29dBm. The corresponding signal-to-noise-and-distortion ratio (SNDR) is calculated with 400-MHz channel bandwidth. In this work, the RX-mode beamformer achieves a peak SNDR of 41.2dB. The measured dynamic range regarding a 25-dB SNDR is from -57dBm to -30dBm. The SNDR at a high input power region could be further improved by reducing the RX-mode gain. Fig. 4.13(b) shows the RX SNDRs with different gain settings. With -6.9-dB gain, the measured NF of the RX-mode beamformer is 16.3dB at 28GHz. The achieved SNDR is improved to -35.4dB regarding an input power of -20dBm.

To evaluate the OTA performance of this work, the packaged chips are further implemented into the 64H+64V dual-polarized phased-array transceiver modules. Fig. 4.14 shows the photograph. Sixteen of the packaged chips are mounted to the backside of the

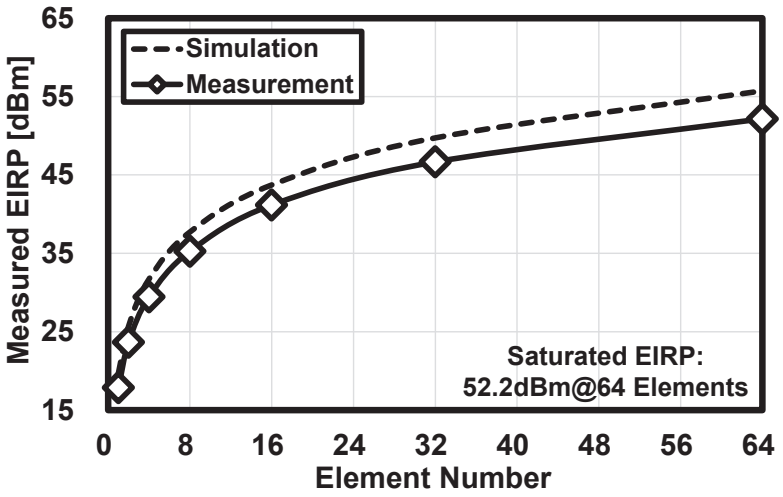
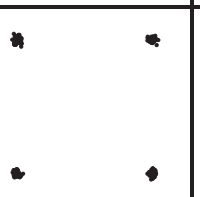
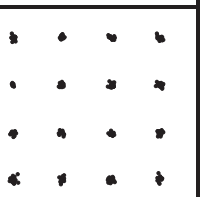
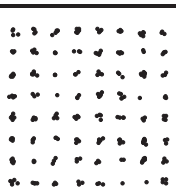
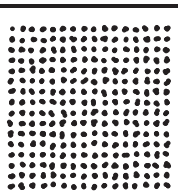


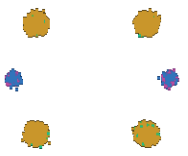
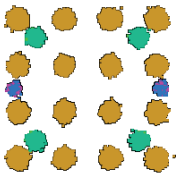
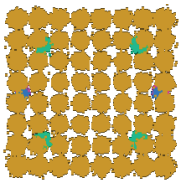
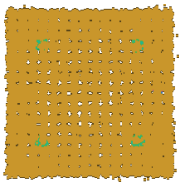
Figure 4.16: Measured effective isotropic radiated powers (EIRPs) against the number of TX-mode beamformers.

module. Each chip has eight antenna ports and is connected to the 2×2 dual-polarized antenna array in frontside through the PCB vias. For distributing H-pol. and V-pol. signals among the chips, totally four 1-to-8 dividers/combiners are utilized on the PCB. To improve the cross-pol. isolation of the H/V signal distribution network, the ground-wall shieldings are included between the distributions. The simulated cross-pol. isolation for the H/V signal distribution network on the PCB is better than 37dB from 26.5GHz to 29.5GHz. On the front side of the module, a 16×4 dual-polarized antenna array is implemented.

Fig. 4.15(a) demonstrates the measured V-pol. beam patterns in the azimuth plane for the proposed phased-array module. The proposed module is capable of scanning the beam from -40° to +40°. The measured sidelobe level is always less than -9dB without any amplitude tapering. The observed asymmetry of the beam patterns is possibly caused by the element pattern and the imperfections during the measurement. Fig. 4.15(b) presents the measured elevation-plane beam patterns within ±30°. A 2×4 array is used in this measurement. The sidelobe level is always less than -9.6dB. Fig. 4.16 shows the measured V-pol. EIRP against the activated element number. The saturated EIRP realized by 64 TX-mode beamformers is 52.2dBm.

Two of the 64-element phased-array transceiver modules are evaluated in a SISO scenario with modulated signals. In this measurement, one phased-array module is operating in TX mode, while the other one is operating in RX mode. The communication distance is 1 meter, which is limited by the size of microwave anechoic chamber. The beam direction is fixed with 0°. The SC-mode and OFDMA-mode modulated signals for the TX-mode

Modulation	QPSK	16QAM	64QAM	256QAM
Mode	Single-Carrier SISO	Single-Carrier SISO	Single-Carrier SISO	Single-Carrier SISO
Symbol rate	2.5GSymbol/s	2.5GSymbol/s	2.5GSymbol/s	0.8GSymbol/s
Data rate/BW_c	5Gb/s	10Gb/s	15Gb/s	6.4Gb/s
TX Constellation				
TX EIRP	31.0dBm	28.3dBm	27.9dBm	21.2dBm
TX EVM (RMS)	-30.0dB	-29.3dB	-29.4dB	-34.3dB
TX-to-RX EVM (RMS)	-22.5dB	-22.2dB	-22.3dB	-28.4dB

Modulation	QPSK	16QAM	64QAM	256QAM
Mode	OFDMA SISO	OFDMA SISO	OFDMA SISO	OFDMA SISO
MCS*	5G NR MCS4	5G NR MCS10	5G NR MCS19	5G NR MCS27
BW_c	400MHz	400MHz	400MHz	400MHz
TX Constellation				
TX EIRP	43.2dBm	42.8dBm	42.8dBm	40.2dBm
TX EVM (RMS)	-26.2dB(4.9%)	-26.0dB(5.1%)	-25.8dB(5.2%)	-29.9dB(3.2%)
TX-to-RX EVM (RMS)	-25.8dB(5.2%)	-25.5dB(5.3%)	-25.3dB(5.4%)	-29.8dB(3.3%)

*5G NR MCS index table 2 for PDSCH is used. (Table 5.1.3.1-2 in 3GPP TS 38.214 V16.1.0).
**For OFDMA-mode measurement, 64-element array transmitter is used. For SC-mode measurement, 8-element array transmitter is used.

Figure 4.17: Measured constellations and EVMs in single-in-single-out (SISO) scenario.

module are generated by the Keysight arbitrary waveform generator (AWG) M8195A along with an up-conversion mixer. The LO for the up-conversion mixer is generated by the Keysight signal generator N5183B. The phase noise is low enough, which will not influence the measured EVMs. The received signals from the RX-mode module are directly analyzed by the Keysight real-time oscilloscope UXR0334A. The upper side of Fig. 4.17 presents the measured SC-mode constellations and EVMs. In SC-mode measurement, eight TX-mode beamformers and four RX-mode beamformers are activated. As shown in Fig. 4.17, the proposed module is capable of supporting maximum data rates of 5Gb/s in QPSK, 10Gb/s in 16-QAM, 15Gb/s in 64-QAM, and 6.4Gb/s in 256-QAM. The cor-

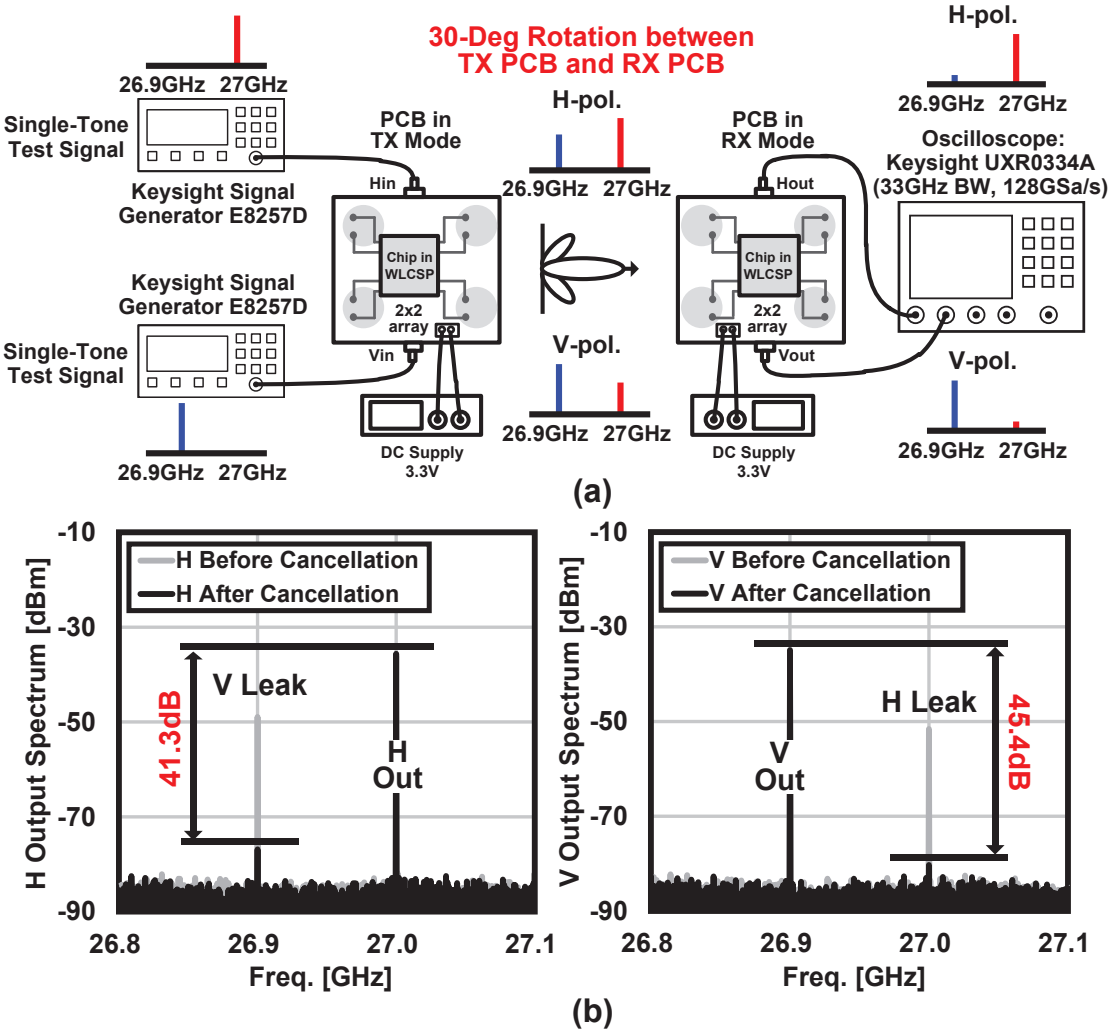
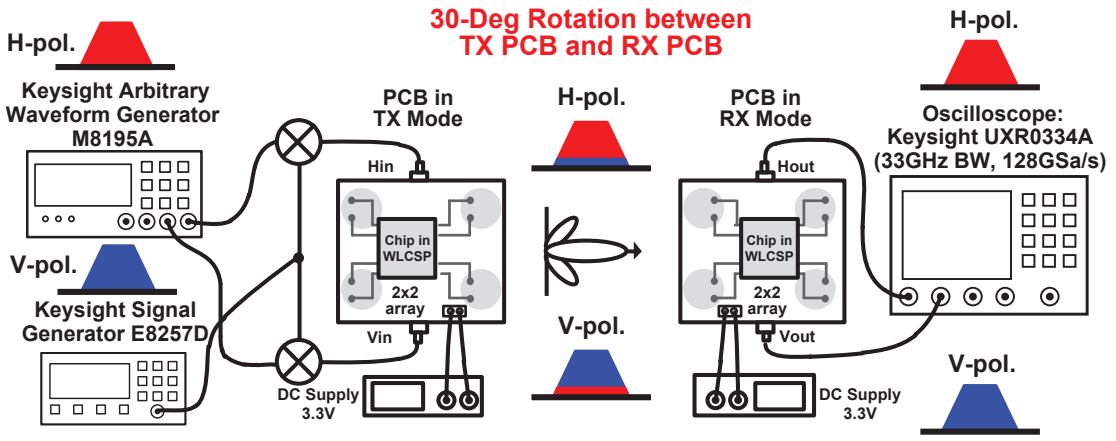
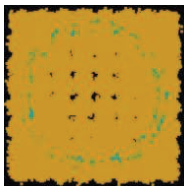
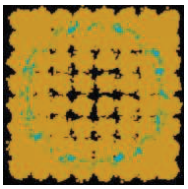


Figure 4.18: (a) Equipment setup for cross-pol. leakage cancellation and (b) measured output spectra for H- and V-polarizations.

responding TX-to-RX EVMs are -22.5dB, -22.2dB, -22.3dB, and -28.4dB for QPSK, 16-QAM, 64-QAM, and 256-QAM, respectively. The bottom side of Fig. 4.17 demonstrates the measured constellations and EVMs with standard-complaint 5G NR OFDMA-mode signals. Sixty-four TX-mode beamformers and four RX-mode beamformers are utilized in this measurement. The PBO of the TX-mode module is reduced for improving both the EIRP level and the transmitter power efficiency. Considering the increased EIRP from the TX side, the RX-mode beamformer in low-gain mode is used in this measurement for improving the input-referred linearity. As shown in Fig. 4.17, the 64-element TX-mode module is capable of delivering 43.2-dBm EIRP in QPSK with -26.2-dB TX EVM, 42.8-dBm EIRP in 16-QAM with -26.0-dB TX EVM, 42.8-dBm EIRP in 64-QAM



(a)

2x2 DP-MIMO Measurement**					
Modulation	64QAM				
Uplink BW_c	400MHz				
Cancellation	No		Yes		
EIRP	V: 19.5dBm	H: 18.7dBm	V: 19.4dBm	H: 19.1dBm	
TX-to-RX Constellation for DP-MIMO*					
TX-to-RX EVM for DP-MIMO*	-22.7dB (7.3%)		-25.1dB (5.6%)		

*TX-to-RX constellation and EVM in DP-MIMO measurement are shown for H and V streams together.
**4H+4V TX-mode beamformers and 4H+4V RX-mode beamformers are used for this measurement.

(b)

Figure 4.19: (a) Equipment setup for DP-MIMO measurement and (b) performance summary before and after proposed cancellation.

with -25.8-dB TX EVM, and 40.2-dBm EIRP in 256-QAM with -29.9-dB TX EVM. By de-embedding the ideal array gain (36.1dB) and the simulated antenna gain (4.9dB), the average TX output power including the packaging and implementation loss is 1.8dBm per path in 64-QAM. The measured TX-to-RX EVMs are -25.8dB in QPSK, -25.5dB in 16-QAM, -25.3dB in 64-QAM, and -29.8dB in 256-QAM.

As mentioned in chapter 4.2.1, the cross-pol. leakage introduced from the PCB and propagation will degrade the channel capacity of DP-MIMO systems. An analog-assisted cross-pol. leakage cancellation technique is proposed in this work to improve both the DP-MIMO EVM and the transmitter power efficiency. Fig. 4.18(a) demonstrates the equipment setup and the cancellation procedure. In this measurement, 4H+4V TX-mode beamformers and 4H+4V RX-mode beamformers are adopted. To verify the cancellation

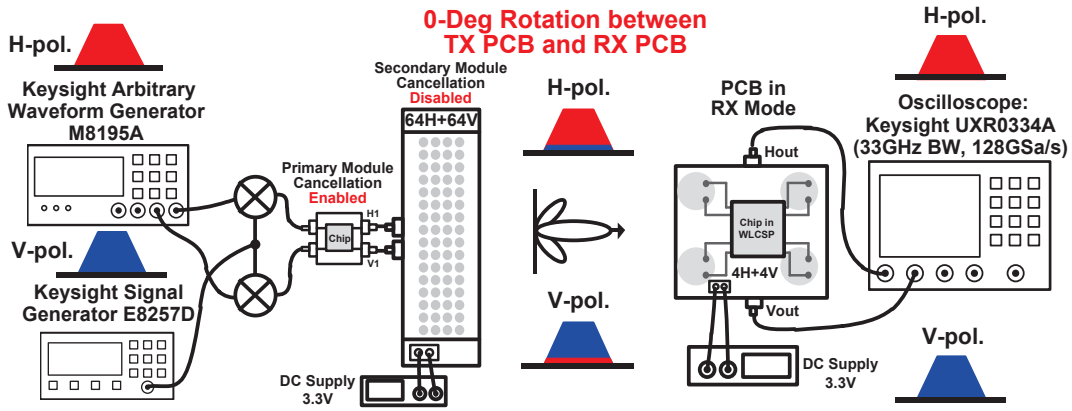
performance over propagation, the TX-mode and RX-mode modules are placed with 30° rotation. Single-tone test signals with frequencies of 27.0GHz and 26.9GHz are firstly sent to the H-pol. and V-pol. of the TX-mode module, respectively. At the RX side, the cross-pol. leakage could be observed from the H-pol. and V-pol. output spectra. According to the leakage observed at the RX side, the canceller at the TX side is activated and configured to suppress the cross-pol. leakage. Fig. 4.18(b) shows the output spectra for the RX-mode module before and after the cancellation. Before the cancellation, around -15-dB cross-pol. leakage could be observed for both H-pol. and V-pol. output spectra due to the rotation and coupling. After the cancellation, the V-to-H leakage is suppressed to -41.3dB, while the H-to-V leakage is suppressed to -45.4dB. The DP-MIMO performance before and after the cross-pol. leakage cancellation is also evaluated. Fig. 4.19(a) demonstrates the equipment setup. The settings for the TX-mode and RX-mode modules are kept the same with the ones used in Fig. 4.18. The rotation between the modules is also 30°. Two-stream 400-MHz standard-compliant 5G NR modulated signals in SC-FDMA mode are generated simultaneously from the Keysight AWG M8195A. The data patterns are fully independent between these two data streams. The generated data streams are up-converted by two external mixers for the TX-mode module. The H-pol. and V-pol. output signals of the RX-mode module are directly analyzed by the Keysight real-time oscilloscope UXR0334A. Fig. 4.19(b) summarizes the measured TX-to-RX constellations and EVMs before and after the proposed cancellation. The output EIRPs for H- and V-pol. signals are kept the same for comparison. The achieved TX-to-RX EVM is improved from -22.7dB to -25.1dB in 64-QAM. The DP-MIMO EVMs including the coupling and rotation are improved with the help of the cross-pol. leakage cancellation technique.

To perform the cross-pol. leakage cancellation for 64H+64V TX-mode beamformers, the designed chip can operate in a primary-secondary configuration. As shown in Fig. 4.20(a), a 4H+4V transceiver module with a coaxial connector interface in this work could be utilized as the primary transceiver. It could provide cross-pol. cancellation function and input signal buffering for the secondary 64H+64V TX-mode module. In this condition, the secondary 64H+64V TX-mode transceiver module will bypass the cancellation function and operates in normal TX mode. Fig. 4.20(b) demonstrates the measured DP-MIMO constellations and TX-to-RX EVMs for 64H+64V TX-mode beamformers and 4H+4V RX-mode beamformers. With 100-MHz channel bandwidth, the measured TX-to-RX EVMs are -34.3dB in QPSK, -33.3dB in 16-QAM, -32.9dB in 64-QAM, and -32.9dB in 256-QAM. With 400-MHz, the achieved TX-to-RX EVMs for QPSK, 16-QAM, 64-QAM, and 256-QAM are -30.4dB, -29.6dB, -29.4dB, and -29.4dB, respectively. The measured V-pol. and H-pol. EIRPs in 64-QAM with 400-MHz bandwidth are 38.4dBm and38.6 dBm, respectively.

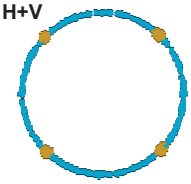
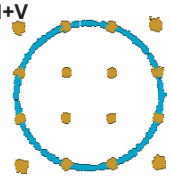
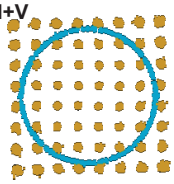
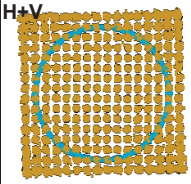
Table 4.2: Performance Comparison of 28-GHz Phased-Array Transceivers Supporting DP-MIMO

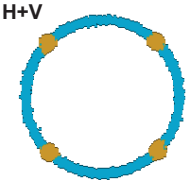
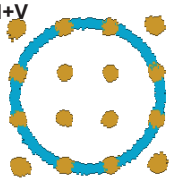
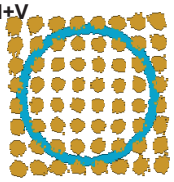
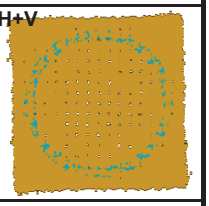
	This work		Qualcomm [13]	IBM [12]	UCSD [14]	Tokyo Tech [9]
Process	65nm CMOS		28nm CMOS	0.13μm SiGe	0.18μm SiGe	65nm CMOS
Carrier Frequency	28GHz (n257)		28GHz (n257)	28GHz	29GHz	28GHz (n257)
TX P1dB/path	13.7dBm		12.0dBm	14.0dBm	12.0dBm	11.3dBm
TX Psat/path	16.1dBm		14.0dBm	16.4dBm	N/A	15.1dBm
Saturated EIRP	52.2dBm (64 elements)		35.0dBm (8 elements)	54.0dBm (64 elements)	26.5dBm@P_{1dB} (4 elements)	45.6dBm (32 elements)
RX NF	4.9dB@28GHz		4.4~4.7dB	6.0dB@28GHz	4.8dB	4.2~5.0dB
RMS Gain Error	0.12dB@28GHz		N/A	Gain Var.< 1.5dB	0.6dB	0.2dB@28GHz
RMS Phase Error	0.4°@28GHz		N/A	< 1°@28GHz	< 4°	0.4°@28GHz
Integration/chip	4×H-Beamformer, 4×V-Beamformer		24×TRX, IF, LO	16×H-TRX, 16×V-TRX, IF, LO (w/o PLL)	4×H-Beamformer, 4×V-Beamformer	4×H-Beamformer, 4×V-Beamformer
PDC/path	TX:186mW @16.1dBm/path RX:88mW		TX:119mW(P_{1dB}) @11dBm/path RX:42mW	TX:319mW @16.4dBm/path RX:206mW	TX:220mW RX:150mW	TX:232mW @15.1dBm/path RX:112mW
Area/path	0.48mm^2		0.68mm^{2*}	2.55mm^{2*}	1.62mm^{2*}	0.58mm^2
5G NR SISO Modulation Supported	QPSK, 16-QAM, 64-QAM, 256-QAM OFDMA-Mode		QPSK, 16-QAM, 64-QAM OFDMA-Mode	N/A	N/A	QPSK, 16-QAM, 64-QAM, 256-QAM OFDMA-Mode
Cross-Pol. Leak Cancel	Yes		No	No	No	No
Rotation btw. TX & RX	Yes		No	No	No	No
Cross-Pol. Isolation	41.3dB for V 45.4dB for H (from TX to RX)		N/A	N/A	36dB for V 27dB for H (TX only)	20.2dB (TX only)
5G NR	64-QAM	256-QAM	N/A	N/A	64-QAM(SC-Mode)	64-QAM
2x2 DP-MIMO	EVM=3.4%	EVM=3.4%			EVM=5.0%	EVM=4.9%

* Estimated from paper.



(a)

Modulation	QPSK	16QAM	64QAM	256QAM
Mode	SC-FDMA DP-MIMO	SC-FDMA DP-MIMO	SC-FDMA DP-MIMO	SC-FDMA DP-MIMO
MCS	5G NR MCS9*	5G NR MCS16*	5G NR MCS27*	5G NR MCS27**
BW_c	100MHz	100MHz	100MHz	100MHz
TX-to-RX Constellation	H+V 	H+V 	H+V 	H+V 
TX-to-RX EVM (RMS)	-34.3dB(1.9%)	-33.3dB(2.2%)	-32.9dB(2.3%)	-32.9dB(2.3%)

Modulation	QPSK	16QAM	64QAM	256QAM
Mode	SC-FDMA DP-MIMO	SC-FDMA DP-MIMO	SC-FDMA DP-MIMO	SC-FDMA DP-MIMO
MCS	5G NR MCS9*	5G NR MCS16*	5G NR MCS27*	5G NR MCS27**
BW_c	400MHz	400MHz	400MHz	400MHz
TX-to-RX Constellation	H+V 	H+V 	H+V 	H+V 
TX-to-RX EVM (RMS)	-30.4dB(3.0%)	-29.6dB(3.3%)	-29.4dB(3.4%)	-29.4dB(3.4%)

*5G NR MCS index table 1 for PDSCH is used. (Table 5.1.3.1-1 in 3GPP TS 38.214 V16.1.0).
**5G NR MCS index table 2 for PDSCH is used. (Table 5.1.3.1-2 in 3GPP TS 38.214 V16.1.0).
***64H+64V TX-mode beamformers and 4H+4V RX-mode beamformers are used.

(b)

Figure 4.20: (a) Equipment setup for primary-secondary DP-MIMO operation. (b) Measured DP-MIMO constellations and EVMs for 64H+64V array module.

Table 4.2 compares this work with several state-of-the-art 28-GHz phased-array transceivers supporting DP-MIMO. With the proposed analog-assisted cross-pol. leakage cancellation technique, this work achieves over 40-dB cross-pol. isolation. The 64H+64V phased-array transceiver modules in this work could support 2×2 DP-MIMO communications. Moreover, the area-efficient neutralized bi-directional beamformer achieves 16.1-dBm TX-mode saturated output power and 22% per path peak TX-mode efficiency. The measured RX-mode NF is 4.9dB at 28GHz. The occupied on-chip area for each beamformer is only 0.48mm^2 due to the completely shared circuits between TX and RX modes. Low-cost and power-efficient millimeter-wave DP-MIMO systems could be supported by this work for the 5G NR.

4.2.5 Summary

In this work, an analog-assisted cross-pol. leakage cancellation technique is utilized for the 28-GHz DP-MIMO systems to improve the DP-MIMO EVMs and efficiency. Over 40-dB cross-pol. isolation is achieved after the proposed high-accuracy cancellation. The element-beamformer in this work maintains low-cost and high-efficiency features with the neutralized bi-directional architecture. 16.1-dBm TX-mode saturated output power along with a 22% maximum TX-mode efficiency is realized with 0.48mm^2 on-chip area. The proposed 64H+64V array modules achieve 3.4% EVM with standard-compliant DP-MIMO signals in 256-QAM. Low-cost and high-efficiency 5G NR millimeter-wave DP-MIMO systems could be realized.

4.3 Inter-Element Mismatch Compensation for Shared-LUT DPD

4.3.1 DPD Architecture in Phased-Array System

As mentioned in Chapter 2, DPD is essential to suppress the nonlinearity and enlarge the output power for 5G mm-wave phased-array beamformers. In this section, as shown in Fig. 4.21, the concept of the shared-LUT DPD with inter-element mismatch compensation is discussed and contrasted with the conventional phased-array DPD strategies. The prefix “single”, “combined” and “shared” are defined by the different approaches of the LUT generation and are not related to the LUT structure itself. Only one LUT is commonly applied for the phased-array system to simplify the baseband. In general, DPD captures the beamformer element output and applies inverse nonlinear operation upon the

input. Based on a widely-used memory polynomial model [74], the pre-distorted input signal of a uniform linear array (ULA) can be expressed as

$$z_{\mathrm{m}}(n) = \sum_{k=0}^{K-1} \sum_{q=0}^{Q-1} a_{\mathrm{kq}}^{\mathrm{m}} x_{\mathrm{m}}(n-q)|x(n-q)|^{\mathrm{k}} \tag{4.9}$$

where $x_{\mathrm{m}}(n)$ is the m^{th} baseband input signal, $z_{\mathrm{m}}(n)$ is the m^{th} pre-distorted signal. The maximum nonlinear order K, maximum memory depth Q and DPD coefficients $a_{\mathrm{kq}}^{\mathrm{m}}$ define the memory polynomial model together. Thus, the corresponding m^{th} element output $y_{\mathrm{m}}(n)$ can be denoted as

$$y_{\mathrm{m}}(n) = z_{\mathrm{m}}(n) e^{j\varphi_{\mathrm{m}}} A_{\mathrm{m}} \tag{4.10}$$

where $e^{j\varphi_{\mathrm{m}}}$ is the m^{th} phase shift and A_{m} is the m^{th} PA gain. This DPD strategy requires individual basebands for each phased-array element, which is impractical. In hybrid beamforming systems, the DPD LUT has to be shared among all the elements and ICs. Therefore, the linearity improvement achieved by DPD is sensitive to the path-to-path AM-AM and AM-PM mismatches caused by the PVT variations. To demonstrate this issue, as a simplified strategy, the single-LUT DPD is shown in Fig. 4.21(a) [76]. The single-LUT DPD captures the response from a single path, assuming the DPD extracted from an arbitrary element m_0, the output mismatch between this element and m^{th} element is given by

$$E_{\mathrm{single}}(n) = z_{\mathrm{m_0}}(n)(e^{j\varphi_{\mathrm{m}}} A_{\mathrm{m}} - e^{j\varphi_{\mathrm{m_0}}} A_{\mathrm{m_0}}) \tag{4.11}$$

where $z_{\mathrm{m_0}}(n)$ is the pre-distorted signal generated by the arbitrary element m_0, which is a constant matrix. The linearity improvement is degraded by the existence of $E_{\mathrm{single}}(n)$. And the error is also subject to change with the different paths, which brings in more uncertainty. While, the conventional combined-LUT DPD in Fig. 4.21(b) captures the responses from all paths and minimizes the errors by digital-domain response combining [77–80]. The digital-domain computational complexity can be relieved by the approach of far-field combining as shown in Fig. 4.21(c), while additional calibration antenna and timing alignment are required to synchronize with the source signal [81–90]. Besides, along with the increasing operation frequency and phased-array size, the narrowed beamwidth makes it difficult to conduct the comined-LUT in far-field, which means the receiver lo-

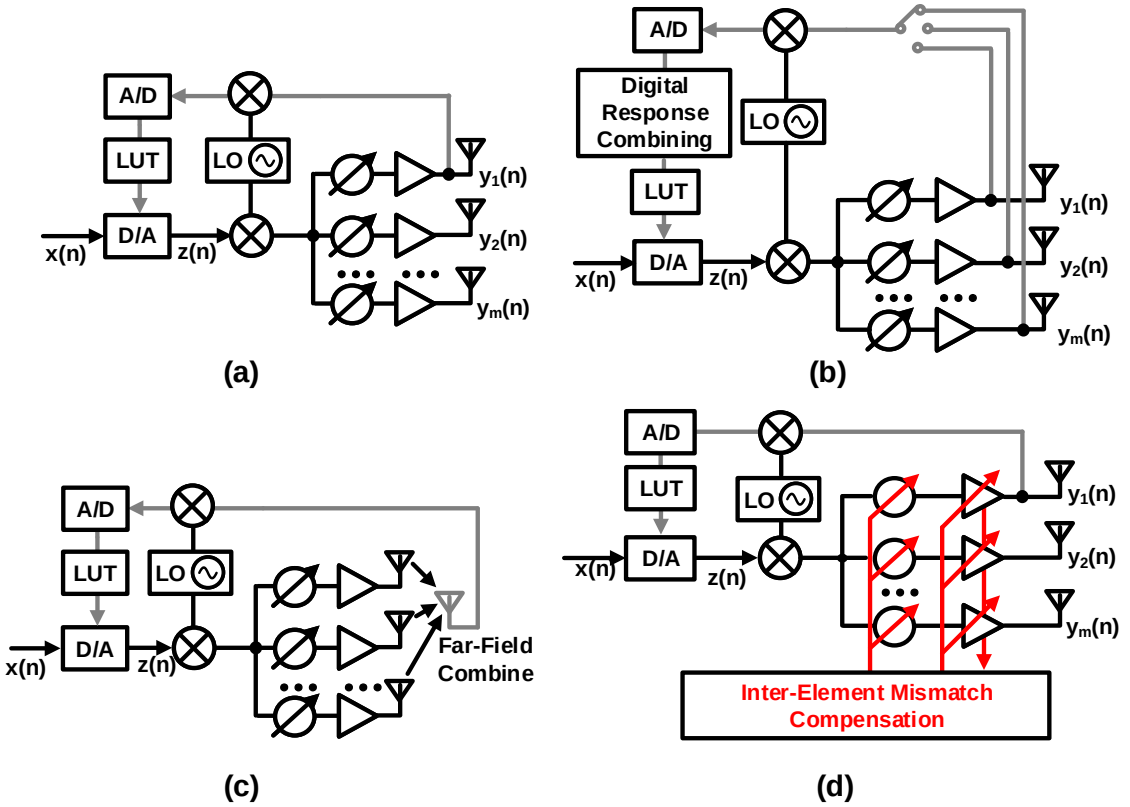


Figure 4.21: DPD strategies for phased-arrays: (a) conventional single-LUT DPD, conventional combined-LUT DPD (b) with digital response combining and (c) with far-field combining, and (d) proposed shared-LUT DPD with inter-element mismatch compensation.

cation and accurate beam direction are required in advance. The combined-LUT DPD output $y_{\text{opt}}(n)$ and the optimized coefficient $z_{\text{opt}}(n)$ can be represented as follows

$$y_{\text{opt}}(n) = \frac{1}{\text{M}} \sum_{\text{m}=1}^{\text{M}} z_{\text{m}}(n) e^{j\varphi_{\text{m}}} A_{\text{m}} \tag{4.12}$$

$$z_{\text{opt}}(n) = \frac{y_{\text{opt}}(n)}{e^{j\varphi_{\text{opt}}} A_{\text{opt}}} \tag{4.13}$$

where $e^{j\varphi_{\text{opt}}}$ is the optimized phase shift and A_{opt} is the optimized PA gain. The output mismatch can be expressed as

$$E_{\text{combine}}(n) = z_{\text{opt}}(n)(e^{j\varphi_{\text{m}}} A_{\text{m}} - e^{j\varphi_{\text{opt}}} A_{\text{opt}}) \tag{4.14}$$

Thus, the achievable linearity improvement could be better than the single-LUT DPD but

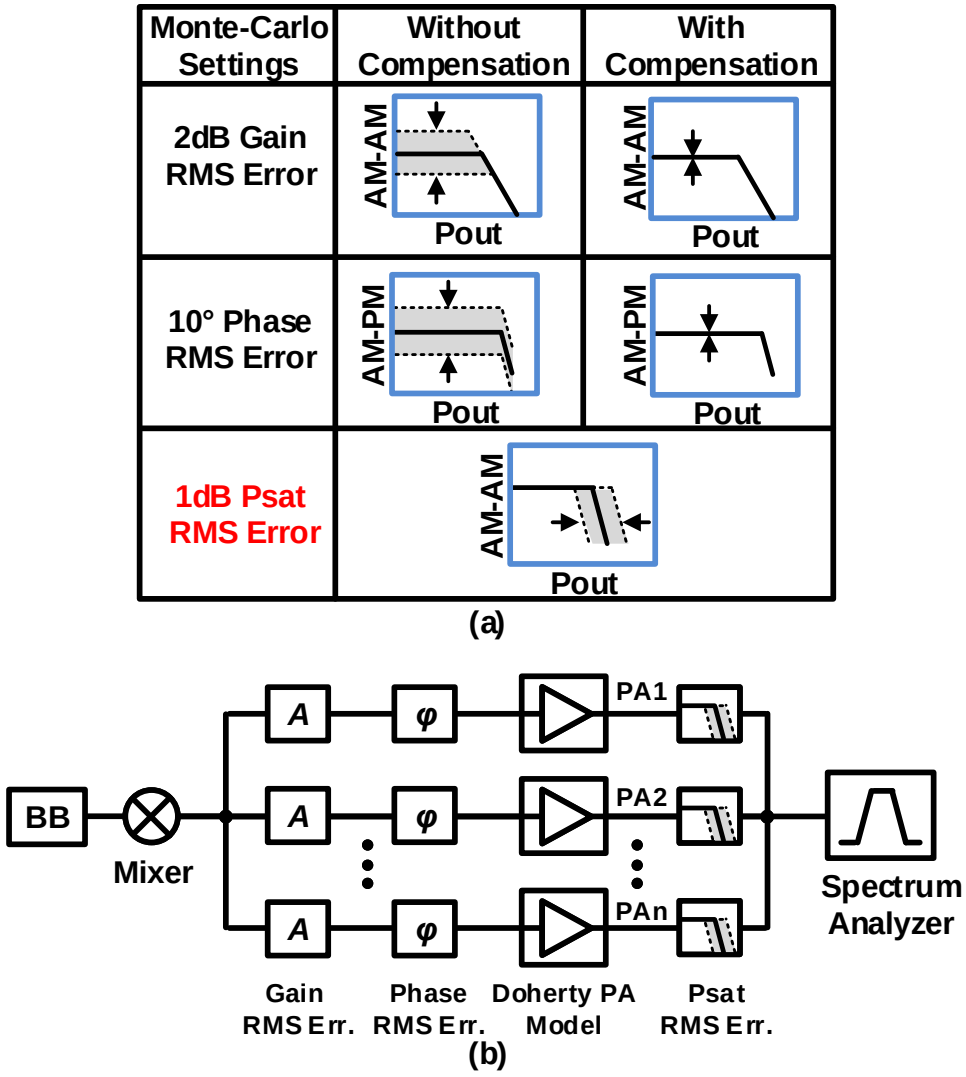


Figure 4.22: The Monte-Carlo simulation of a 16-element ULA with different DPD strategies: (a) offset-mismatch settings with given gain and phase rms errors, and (b) the simplified simulation testbench.

is still limited by the AM-AM and AM-PM mismatches among different elements.

As illustrated in Fig. 4.21(d), this work introduces a shared-LUT DPD with the inter-element mismatch compensation technique to further improve DPD performance in 5G hybrid beamforming systems. Before DPD LUT extraction, the path-to-path AM-AM and AM-PM mismatches are corrected through the inter-element mismatch compensation system. In this way, the errors could be minimized after compensation, which provides a prerequisite for sharing the same DPD LUT among the entire phased-array without compromising DPD performance.

To demonstrate the performance with the conventional and proposed DPD strategies,

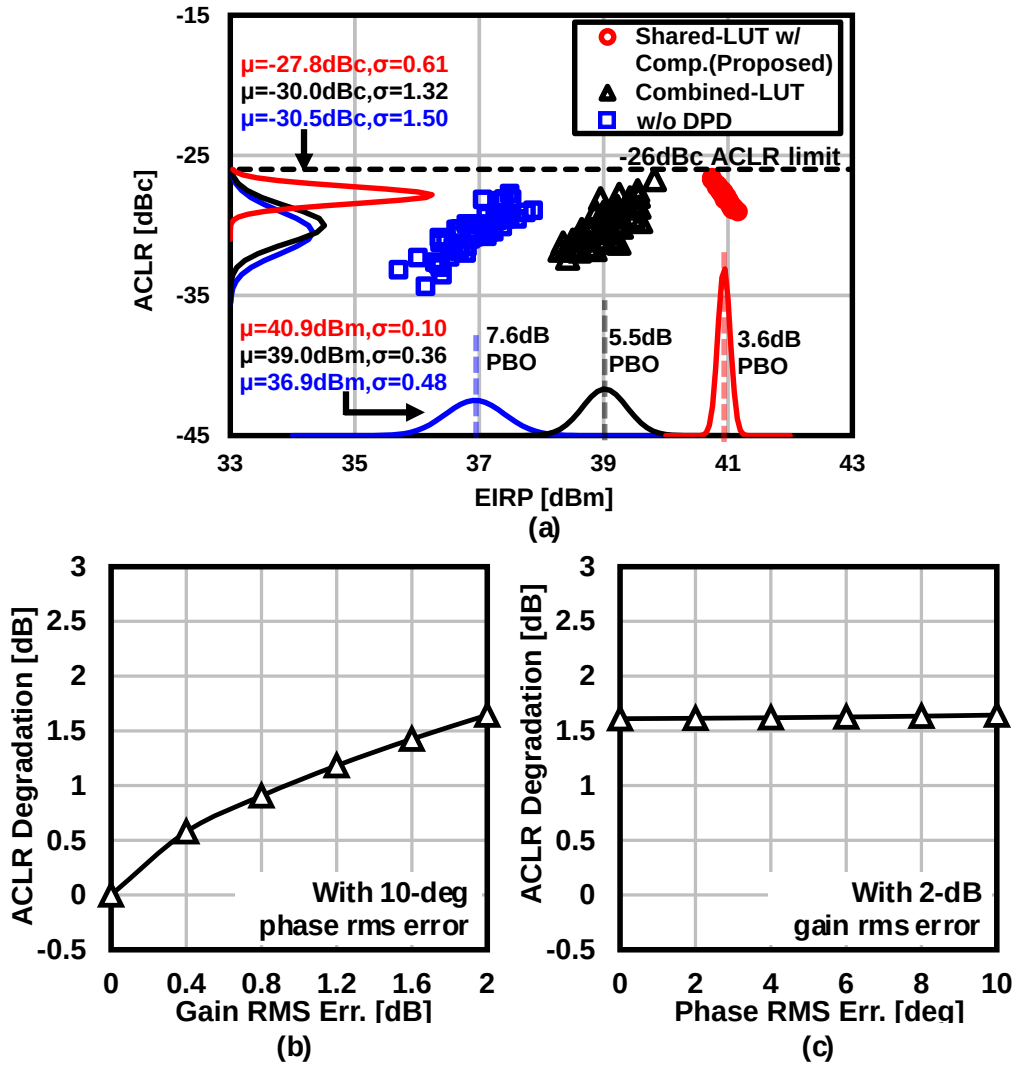


Figure 4.23: The Monte-Carlo simulation of a 16-element ULA with different DPD strategies: (a) the simulated ACLR vs. EIRP performance. The 16-element ULA simulated (b) ACLR vs. gain rms error and (c) ACLR vs. phase rms error.

an ACLR versus EIRP simulation of a 16-element ULA is conducted using Keysight SystemVue software in Fig. 4.22. The simulation condition and a simplified testbench are also shown in Fig. 4.22(a) and Fig. 4.22(b), respectively. 2-dB gain offset rms error and 10° phase offset rms error are assigned by the Monte-Carlo setup. Besides, an additional 1-dB saturated output power offset rms error is also assigned to demonstrate the process variation due to the different manufacturing lots and implementation mismatches. The AM-AM and AM-PM characteristics of a Doherty PA are extracted and applied to the ACLR simulation. All samples are simulated at the same input power level. Each

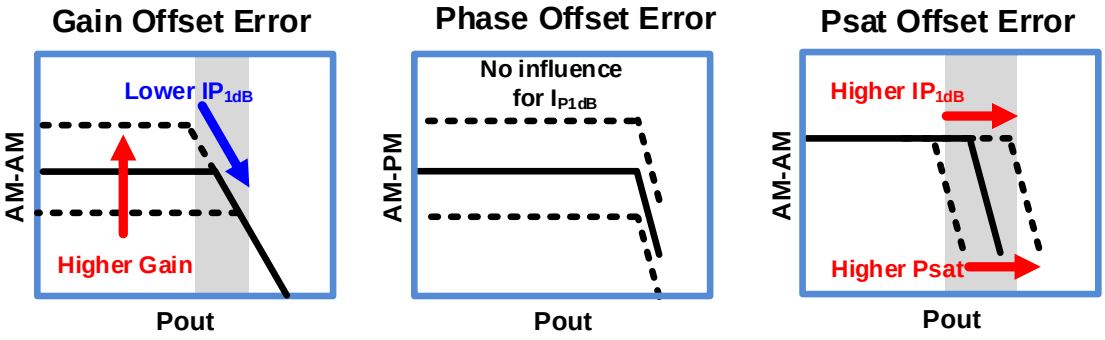


Figure 4.24: The influence of gain offset error, phase offset error and Psat offset error towards IP_{1dB}.

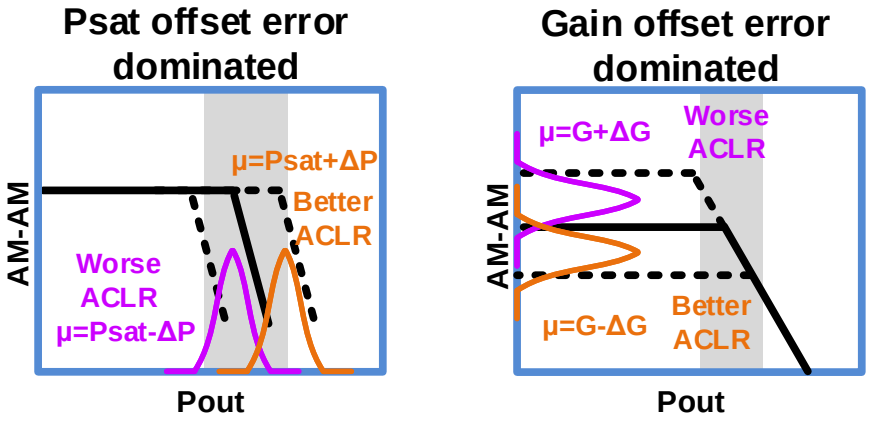


Figure 4.25: The ACLR vs. EIRP variation due to the random Pout probability distribution of samples.

PBO point is adjusted so the $+3\sigma$ worst-case ACLR becomes less than the required -26-dBc level. By means of the proposed shared-LUT DPD with the inter-element mismatch compensation technique, the average value and the standard deviation of the simulated ACLR can be improved, as shown in Fig. 4.23(a). The proposed technique can realize the smallest PBO and the highest EIRP characteristics. To evaluate the required calibration resolution, the 16-element ULA ACLR vs. gain and phase rms errors are performed as shown in Fig. 4.23(b) and Fig. 4.23(c), respectively. In order to minimize the calibrated ACLR degradation below 0.5dB, the 0.4-dB gain rms error is required for the VGA resolution, which means a finer resolution is required for amplitude detection. The ACLR degradation will in return cost more power back-off for EIRP. While the phase rms error mainly degrades the side lobes of the beampattern, the non-linearity contribution is not obvious.

It is worth noticing that the ACLR versus EIRP tendency of the proposed shared-LUT

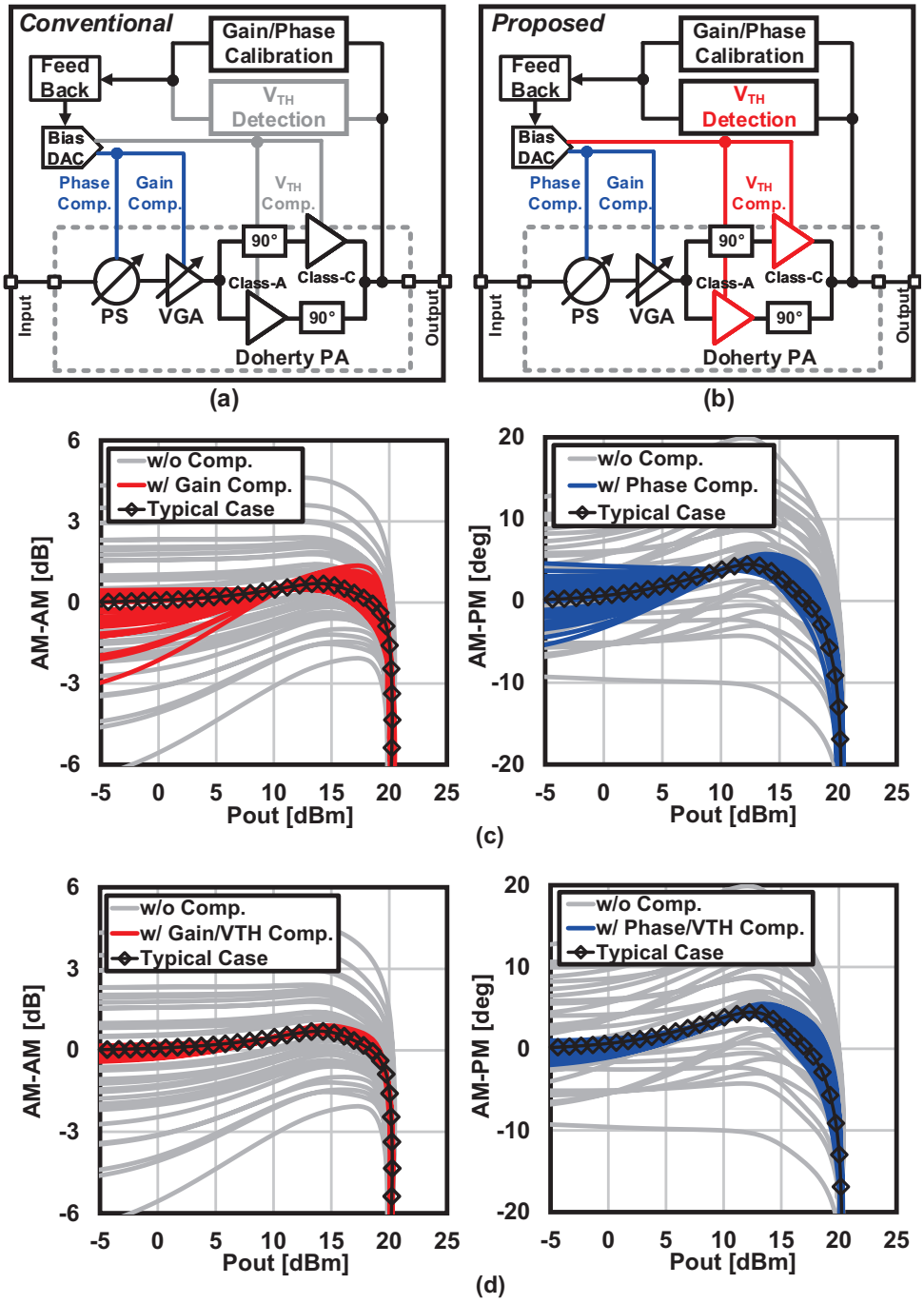


Figure 4.26: (a) The concept of gain and phase compensation and (b) the proposed Vth, gain and phase compensation. Monte-Carlo simulation over process variations of (c) AM-AM and AM-PM with gain/phase compensation only, and (d) AM-AM and AM-PM with gain/phase/Vth compensation method.

DPD with compensation is opposite with the combined-LUT DPD and without DPD cases in Fig. 4.23(a). To make a reasonable explanation, the influence factor of the ACLR will

be introduced first. The ACLR of the RF devices is frequently dominated by the 3rd-order intermodulation distortion (IMD3) of the device. The ACLR of a wideband carrier can be related to the two-tone IMD3 performance by a correction factor. This correction is due to the fact that the ACLR performance is degraded by the IMD3 performance. This degradation is due to the effects of the various intermodulation products that form from the spectral density of the spread-spectrum carrier. A useful relationship for ACLR to IMD3 is as follows [109, 110]

$$ACLR = IMD3 + C_{\mathrm{n}} \tag{4.15}$$

where C_{n} is the correction factor related to the number of subcarriers. For the two-tone test, as mentioned in Section 2.3.1, it is easily to find the relationship below

$$IMD3 = IM3 - Pout = IM3 - Pin - G \tag{4.16}$$

$$IM3 = 3Pin + G - 2IIP3 = 3Pin + G - 2IP_{1\mathrm{dB}} - 19.2dB \tag{4.17}$$

where Pout and Pin represent the output power and input power of the device, respectively. IM3 is the 3rd-order intermodulation product and G means the linear power gain. Thus, IMD3 can be referred to $\mathrm{IP}_{1\mathrm{dB}}$ as follows

$$IMD3 = 2Pin - 2IP_{1\mathrm{dB}} - 19.2dB \tag{4.18}$$

which means ACLR is dominated by $\mathrm{IP}_{1\mathrm{dB}}$ at a given input power level. The higher $\mathrm{IP}_{1\mathrm{dB}}$ brings a better ACLR. Based on this conclusion, the single-element ACLR tendency can be analyzed as shown in Fig. 4.24. It is evident that phase offset error does not influence $\mathrm{IP}_{1\mathrm{dB}}$, resulting in no change of ACLR. This also corresponds to the result in Fig. 4.23(c). As for the gain offset error case, the PA saturates in advance and $\mathrm{IP}_{1\mathrm{dB}}$ becomes lower when a higher gain occurs. This means a degraded ACLR with a larger Pout and vice versa. On the contrary, when the Psat offset error generates a higher Psat, the gain remains constant, which leads to a larger $\mathrm{IP}_{1\mathrm{dB}}$. Thus the larger Pout means a better ACLR in the Psat offset error case. During the Monte-Carlo simulation in Fig. 4.22(a), the EIRP variation due to the random Pout probability distribution of samples can be represented by Fig. 4.25. When the dominant error is the Psat offset, a higher average Pout results in a higher EIRP and, therefore a better ALCR. Conversely, a lower average Pout will lead to a lower EIRP and a worse ALCR. On the other hand, when the dominant error is the

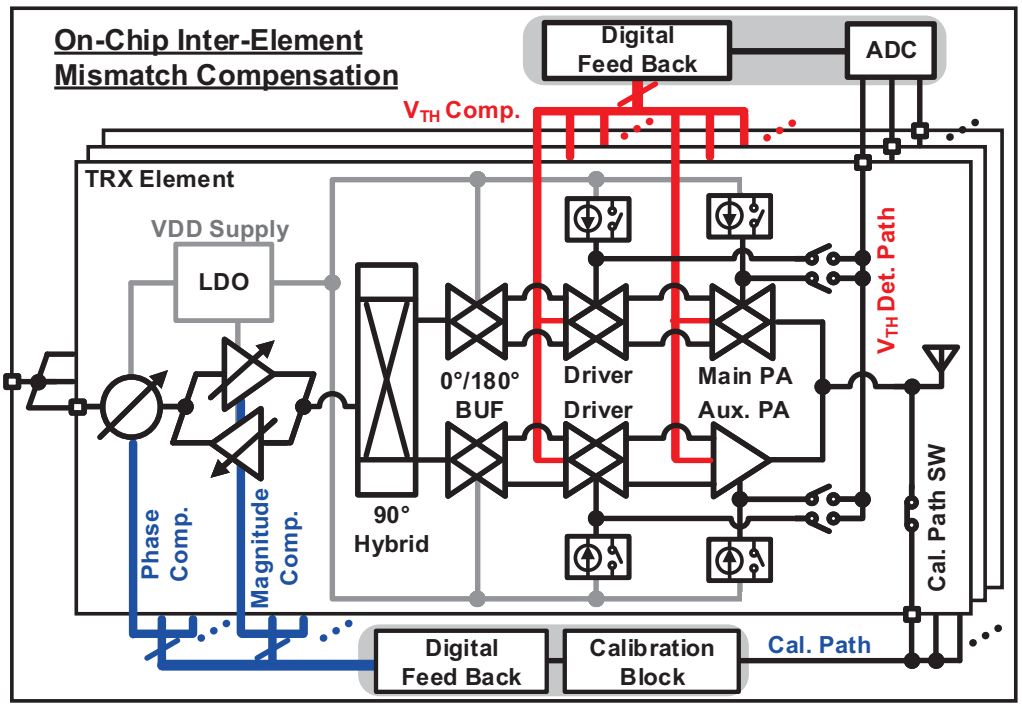


Figure 4.27: System block diagram of the proposed inter-element mismatch compensation.

gain offset, a lower average Pout will result in a better ACLR, and conversely, a higher average Pout will result in a degraded ACLR. The ACLR distributions are related to the IP_{1dB} variations of all the samples.

To draw a conclusion, the gain and Psat offset rms errors contribute to different ACLR trends. The ACLR is fully dominated by the Psat offset error in the proposed shared-LUT DPD with compensation case and mainly dominated by the larger gain offset error in the combined-LUT DPD and without DPD cases.

The gain and phase offset calibration is applied for accurate beamforming in a phased-array system, which can mitigate AM-AM and AM-PM offset mismatches over the phased-array elements. However, the strong nonlinearity of Doherty PA cannot be compensated by the simple gain and phase offset compensation since the class-C biased amplifier is very sensitive to the transistor threshold voltage (Vth) variation. Thus, as shown in Fig. 4.26(b), Vth mismatch compensation is mandatorily required for a phased-array beamformer using Doherty PA for optimizing array EVM and ACLR characteristics. To verify the difference towards the conventional gain/phase compensation in Fig. 4.26(a), a Monte-Carlo simulation about AM-AM and AM-PM of the single TX element with Doherty PA is conducted, where the same simulation samples are used for two compensation methods. The gain/phase compensation and the proposed gain/phase/Vth compensation results are

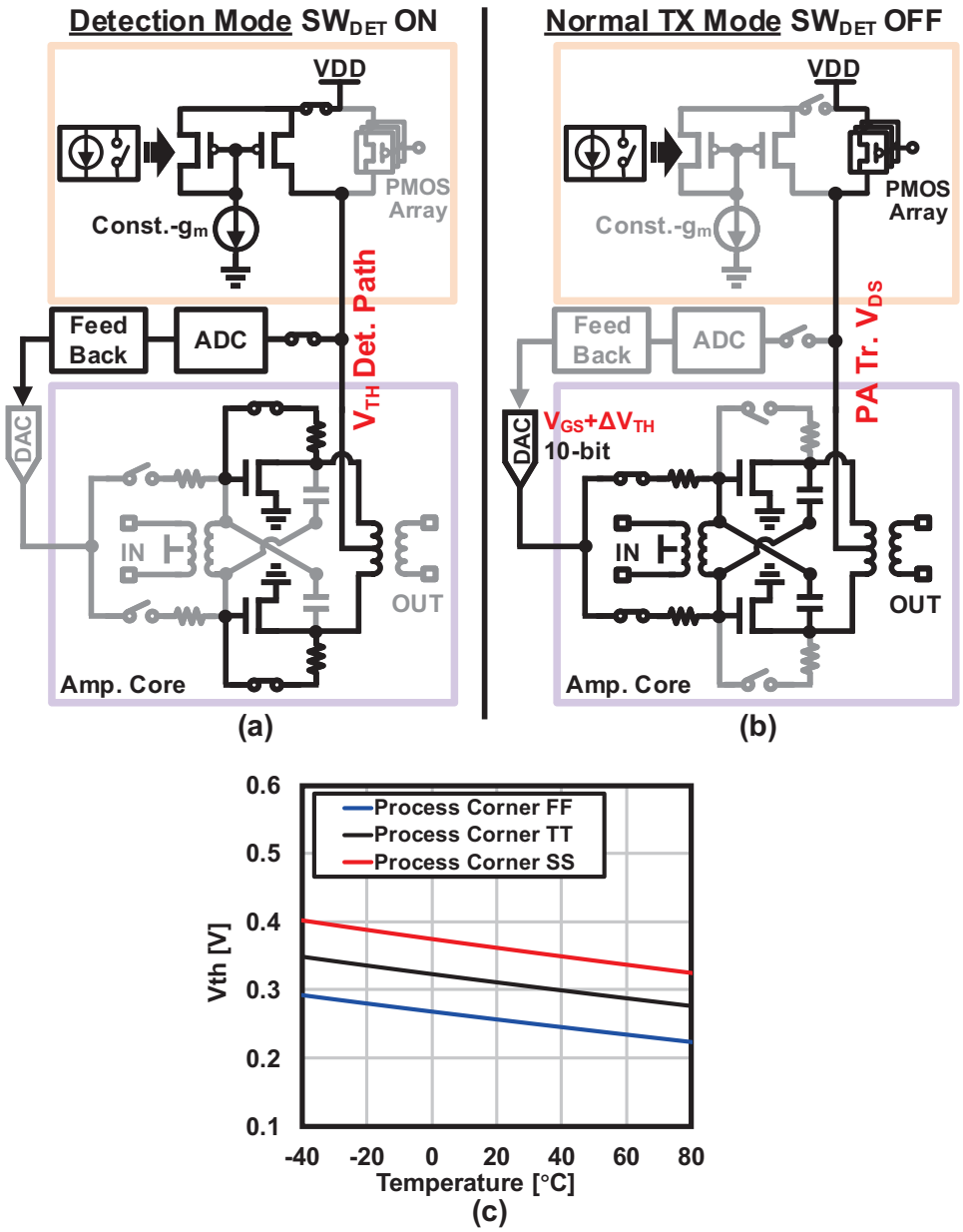


Figure 4.28: Schematic of the proposed Vth detection circuit in (a) Vth detection mode and (b) normal TX operation mode. And (c) the simulated Vth detection varies with the temperature variations at different process corner conditions.

shown in Fig. 4.26(c) and Fig. 4.26(d), respectively. Obviously, with the gain/phase offset compensation, the large mismatch remains in both AM-AM and AM-PM characteristics. While the AM-AM and AM-PM can be compensated from the back-off power level along to the peak power level by using the gain/phase/Vth method.

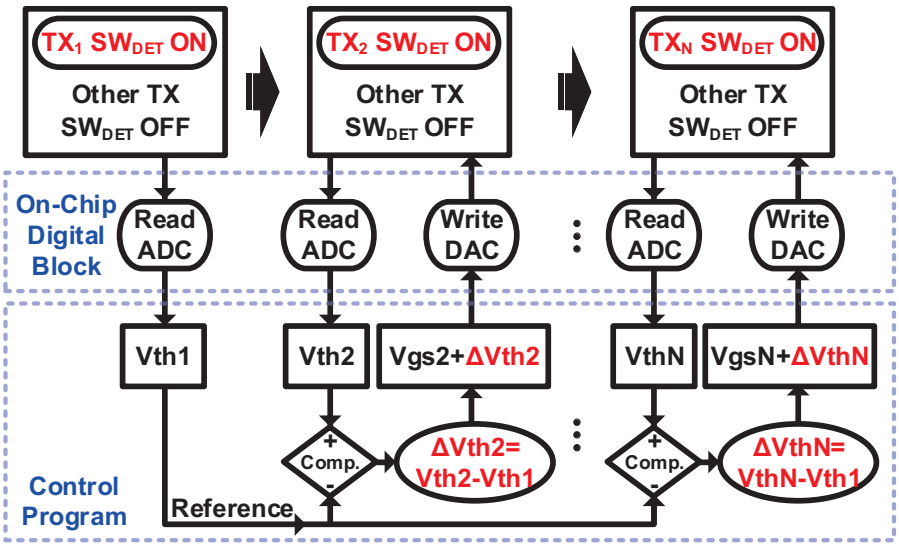


Figure 4.29: Measurement flow diagram of the proposed Vth detection and compensation.

4.3.2 Inter-Element Mismatch Compensation

Fig. 4.27 shows the detailed implementation of the proposed on-chip inter-element compensation system, the AM-AM and AM-PM mismatches are detected by em-bedded self-test circuitry and compensated over inter-element and inter-chip. Therefore, the nonlinearity characteristics at the TX operating points between different elements are minimized and a shared-LUT DPD could be applied to the entire phased-array. Fig. 4.28(a) and (b) demonstrate the Vth detection mode and normal TX mode, respectively. The Vth mismatch of the Doherty PA is detected by an on-chip threshold voltage detector and 10-bit ADC, and is compensated by tuning the gate bias through the digital interface. The Vth detection is conducted by turning on the SW_{DET}. the PA transistors are configured in diode-connection mode and operated in the subthreshold region. The drain current is controlled by the current mirror. The 10-bit ADC reads out the gate voltage of the diode-connected transistor as Vth [111]. The simulated Vth detection varies with temperature at different process corner conditions can be referred to in Fig. 4.28(c). When it operates in normal TX mode, SW_{DET} is turned off. Thus, the power PMOS array is turned on and the PA transistors are placed in the saturation region. Considering the Vth detection and compensation in a phased-array system, a measurement flow diagram is shown in Fig. 4.29. When detecting the Vth of a specific beamformer element, only the SW_{DET} of this element is turned on, while all other element switches are closed. Then Vth detection is conducted element by element with no input signal required and all the ADC read-outs are sent to a control program with GUI. One reference element is necessary with a

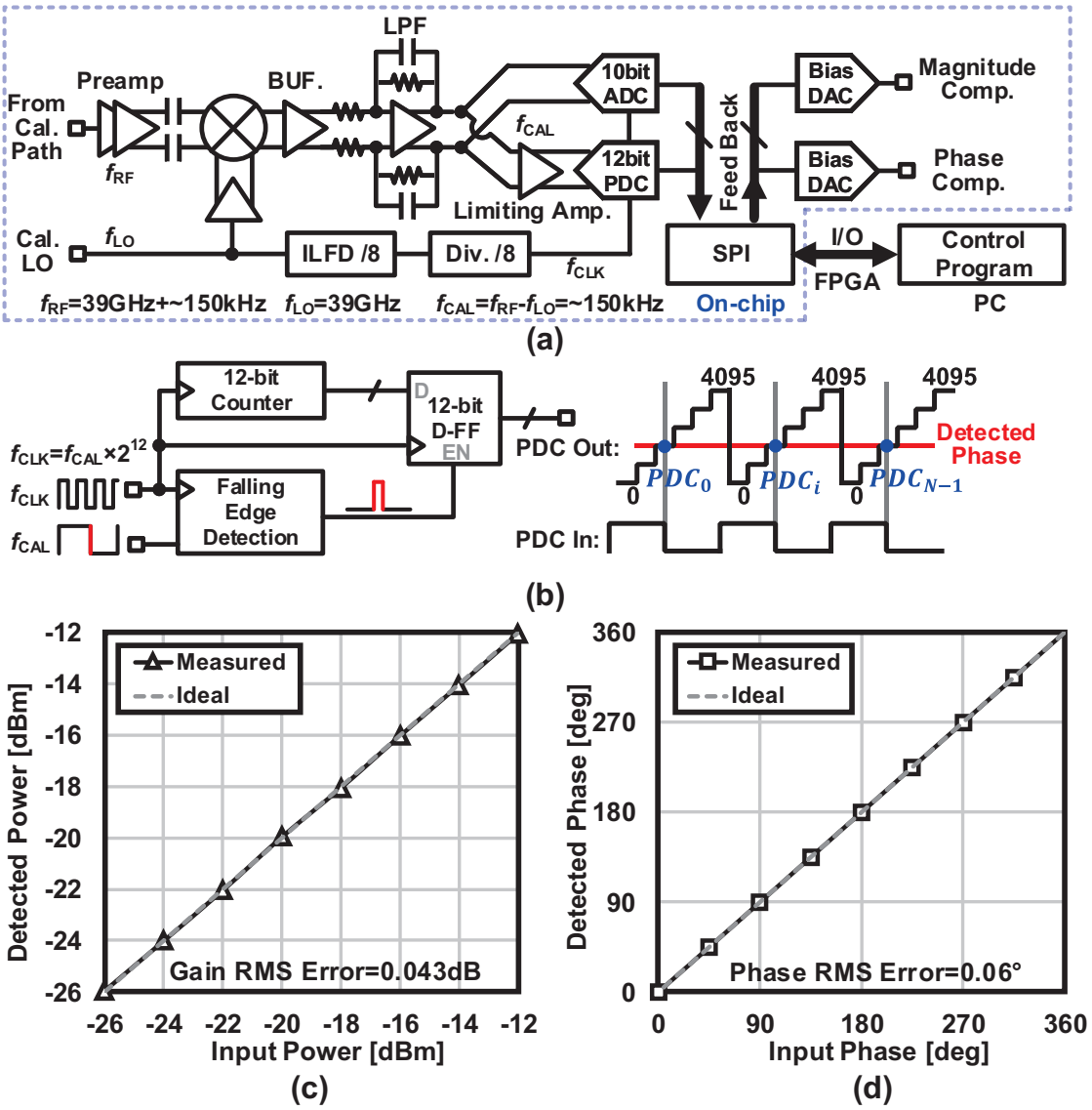


Figure 4.30: (a) Block diagram of the calibration block and (b) the operation of phase detection. The measured detected (c) gain rms error and (d) phase rms error.

reference Vth value, e.g., Vth1 in Fig. 4.29. The optimal reference Vth value can be selected by conducting continours-wave measurements with several ICs. The Vth mismatch ΔVth between the other detected Vth value and the reference Vth1 can be calculated by Vth-Vth1, then a compensated bias of Vgs+ΔVth is written into the DAC to perform the compensation. The Vth compensation is conducted before the following gain and phase compensation to minimize the mismatches inside between the Doherty PA's main path and auxiliary path.

The gain and phase offset mismatches are detected by an on-chip calibration block and compensated by tuning the VGA and phase shifter in each beamformer element. Fig.

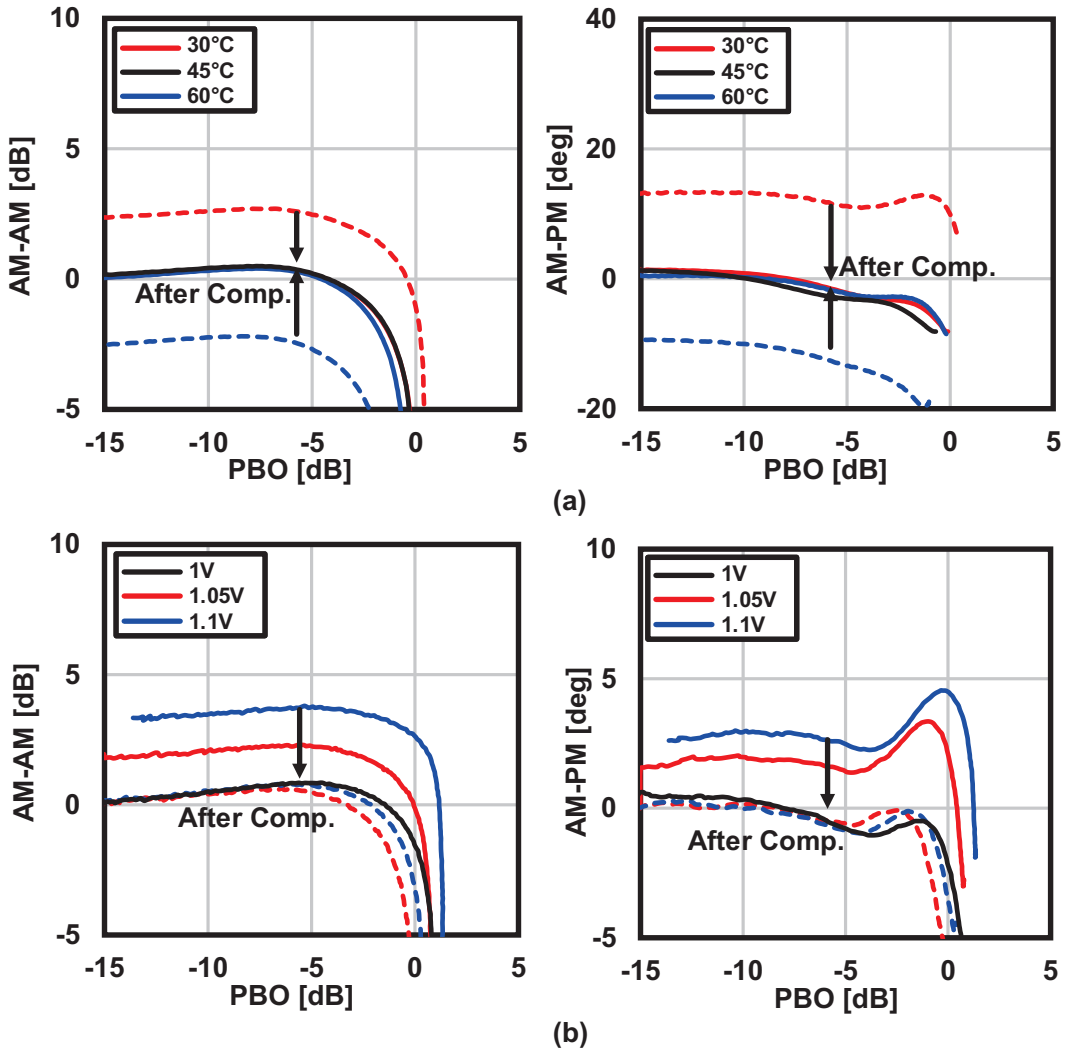


Figure 4.31: Measured AM-AM and AM-PM compensation over (a) temperature variations and (b) supply voltage variations.

4.30(a) shows the block diagram of the calibration block. To perform this calibration, e.g., at 39GHz, the 39-GHz+~150-kHz output signal from each TX output is re-directed and down-converted to a ~150-kHz calibration signal. The 39-GHz calibration LO is reused and divided for digital clock generation. Then, a 10-bit ADC and a 12-bit counter-based phase-to-digital converter (PDC) are utilized for accurate magnitude and phase detection. The readouts of ADC and PDC are sent to the control program. Then, the compensated bias codes are written into the DACs of VGA and PS. Fig. 4.30(b) shows the operation of phase detection. The calibration signal is transformed into a square wave by the limiting amplifier as the input of PDC. The original RF signal's phase information is maintained in the transformed square wave signal. The PDC is mainly composed of a 12-bit counter, a falling edge detecter, and a 12-bit D flip-flop. The phase detection resolution

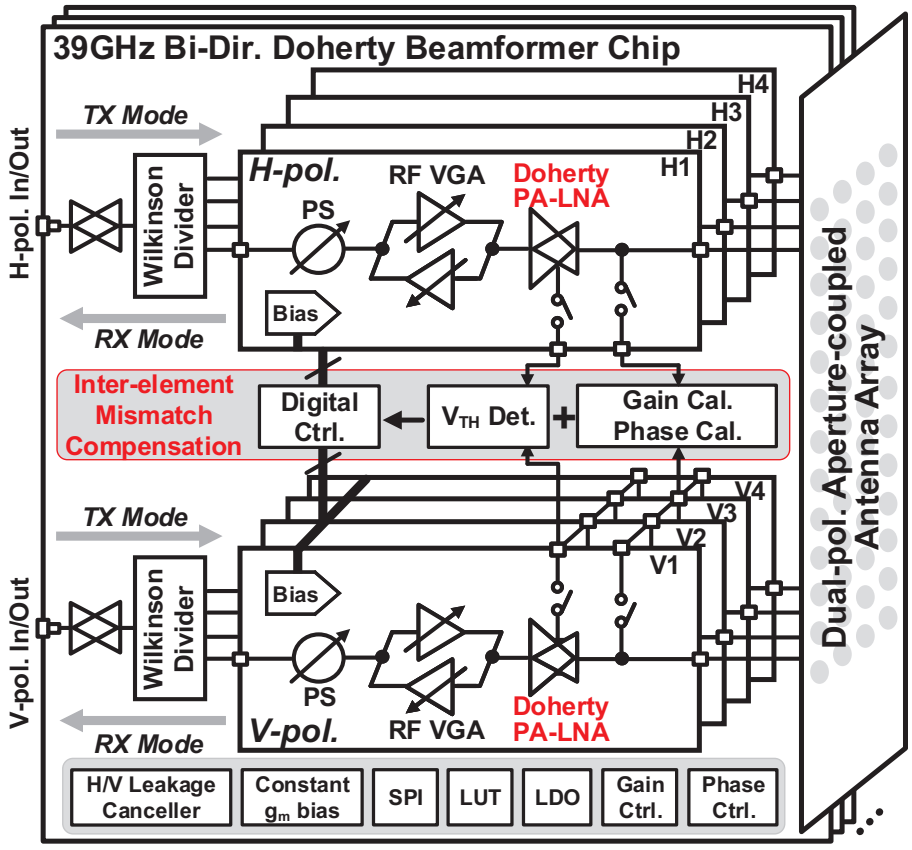


Figure 4.32: Block diagram of the 39-GHz CMOS bi-directional phased-array TRX system.

is determined by the frequency ratio between the clock signal and the calibration signal, i.e., 2^{12}:1. The detected phase is evaluated by the 12-bit countered output value at each falling edge of the input signal. The measured magnitude and phase detection results are also shown in Fig. 4.30(c) and (d). The measured rms error for magnitude detection is 0.043dB, while the measured rms error for phase detection is 0.06°[112].

The inter-element mismatch compensation is conducted at the beginning of the measurement. And repeated compensation at a certain time interval is required considering the environmental variations. The inter-element mismatch compensation time is related to the read-and-write operations through the digital interface. In this work, a 25-MHz SPI clock is utilized. The compensation for one chip costs around 0.2ms. The registers for LUT storage are integrated inside the on-chip digital block. To perform the on-chip calculation for compensation, the additional digital comparator and the supporting logic circuits are necessary.

Fig. 4.31 shows the measured AM-AMs and AM-PMs of the element transmitter before and after the proposed inter-element mismatch compensation over temperature and

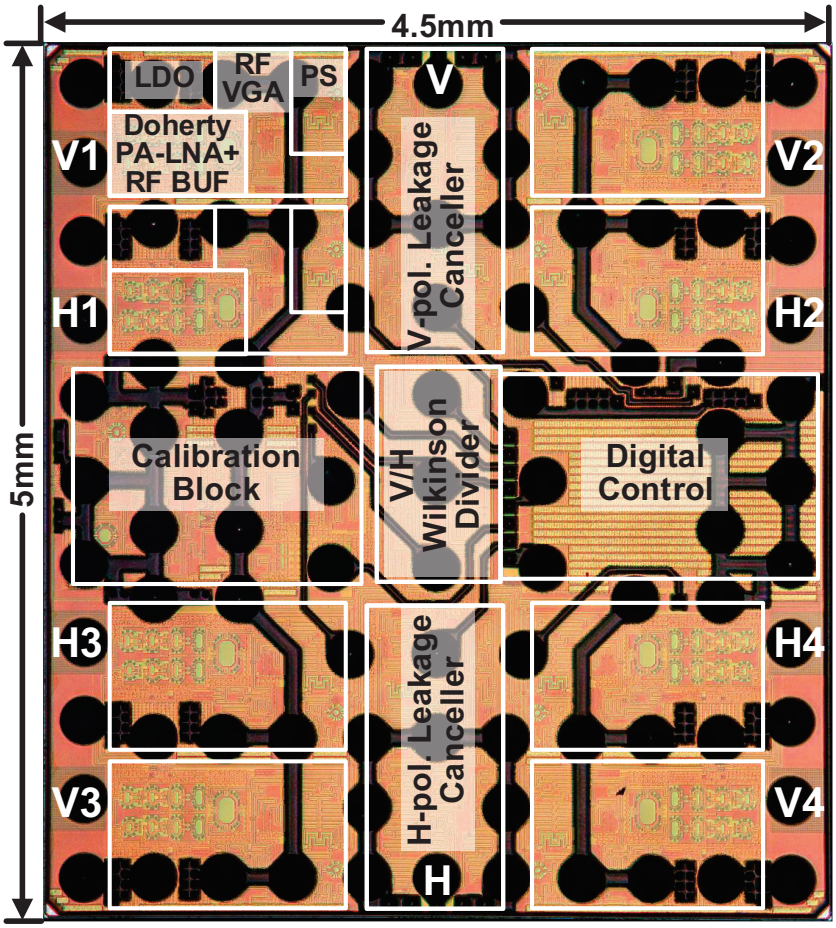


Figure 4.33: Die micrograph of 39GHz CMOS bi-directional phased-array TRX.

supply voltage variations. The mismatches caused by the temperature and supply voltage drifts can also be significantly corrected.

4.3.3 39-GHz Phased-array Beamformer

Fig. 4.32 illustrates the block diagram of the 39-GHz phased-array beamformer. The proposed chip consists of four horizontal-polarized and four vertical-polarized beamformer elements. Each element is composed of a bi-directional Doherty PA-LNA, a three-stage bi-directional RF VGA, and an RF phase shifter. The neutralized bi-directional technique is used to minimize the required chip area [9]. The cross-pol. leakage canceller is also utilized to reduce the cross-pol. leakage to support the DP-MIMO better [10]. To realize an efficient shared-LUT DPD phased-array system, this work introduces a built-in inter-element mismatch compensation technique by cooperating with the Vth detection block and calibration block. The power supplies of beamformer elements will suffer from differ-

Table 4.3: Core Area and Power Consumption Breakdowns

	Sub-Block	Area [mm^2]	TX-Mode PDC [mW]	RX-Mode PDC [mW]
Beamformer Element	Bi-dir. Doherty PA-LNA	0.26	207@Psat Main path:106 Aux. path:101 87@Static Main path:81 Aux. path:6	45
	RF BUF		39.5	11
	RF VGA	0.37	45.5	25
	PS	0.19	0	0
Full Chip Comb.	Canceller	1.14	15	10
	Comb. BUF		20	13
	Wilkinson Divider	0.65	0	0

ent on-board distribution losses without the on-chip LDOs, which introduces additional phase and gain errors for the phased-array system. In this work, the on-chip LDOs are utilized to provide a precise 1-V power supply with high stability. The following part of this section will introduce the detailed circuit implementation of the proposed phased-array beamformer.

4.3.4 Measurements

The proposed 39-GHz phased-array beamformer chip is fabricated in standard 65-nm CMOS technology. Its die micrograph is shown in Fig. 4.33 with a chip size of 4.5mm×5mm. The area breakdown and power consumption breakdown of building blocks are available in Table 4.3. The consumed power for each element is 402mW at saturation point in TX mode and 87mW in RX mode.

Fig. 4.34 summarizes the on-wafer measured single-element beamformer characteristics. Fig. 4.34(a) demonstrates the TX/RX-mode frequency responses. The single-element beamformer achieves around 28.5-dB gain in TX mode and 27.5-dB gain in RX mode, respectively. With 400-MHz channel bandwidth, the calculated SNDR of the RX-mode beamformer is shown in Fig. 4.34(b). A higher than 35-dB RX-mode SNDR is realized.

The 5G standard-compliant OFDMA-mode modulated signals are utilized for evaluating the TX-mode beamformer. As shown in 4.34(c) and (d), the proposed TX-mode beamformer achieves 10.2-dBm output power in 64QAM with −25.1-dB EVM without

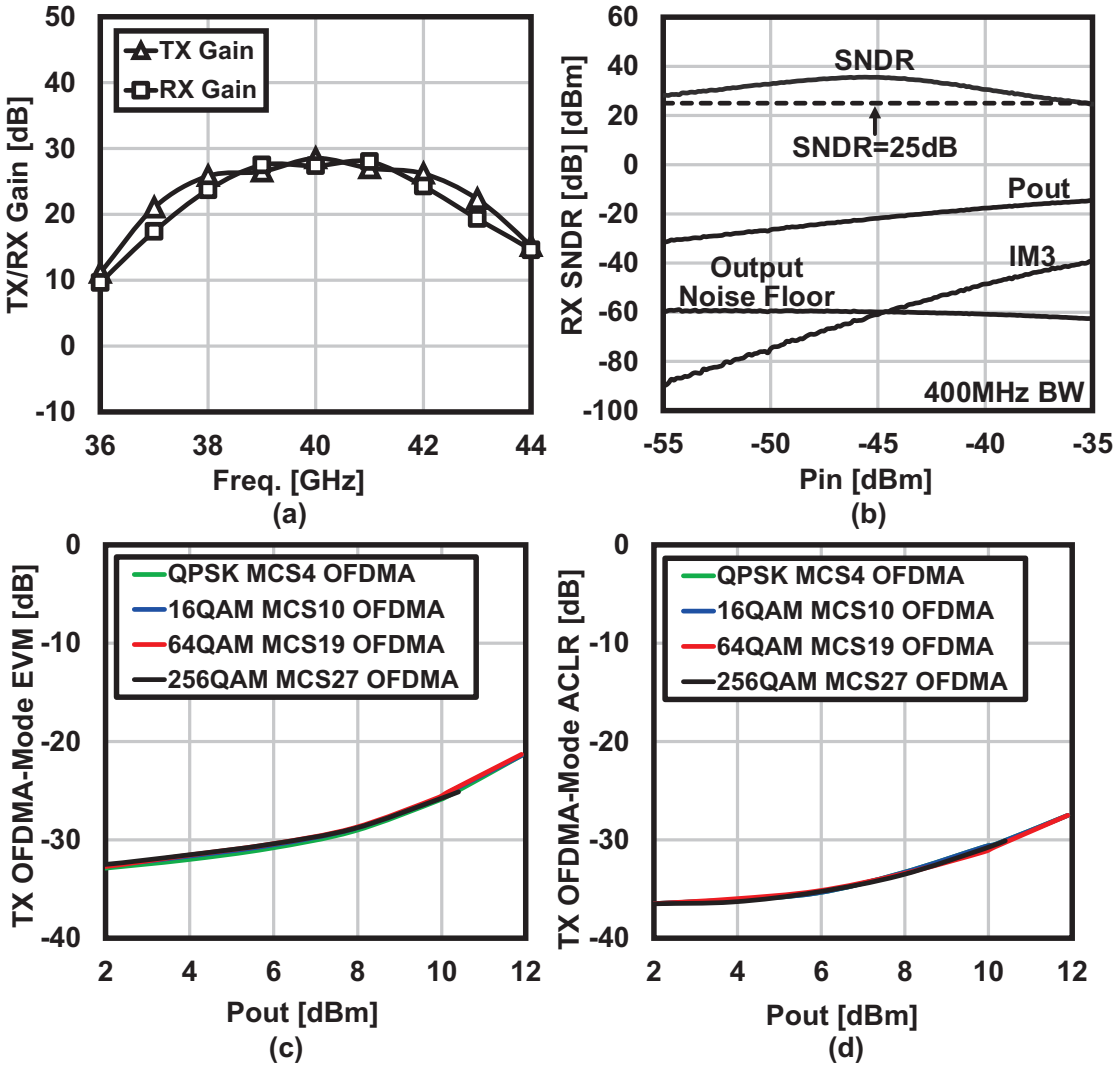


Figure 4.34: Measured single-element beamformer characteristics: (a) TX/RX gain and (b) RX-mode SNDR, TX OFDMA-Mode (c) EVMs and (d) ACLRs with 400MHz bandwidth without DPD.

DPD. The corresponding 64-QAM ACLR is −30.7dBc. A 256-QAM EVM of −31.6dB is also maintained with 3.9-dBm output power and −36.3-dBc ACLR.

To perform the over-the-air (OTA) communication with a large array size, the 16-IC phased-array dual-polarized PCB module is implemented including 64 horizontal-pol. and 64 vertical-pol. beamformer elements. Fig. 4.35(a) shows the front-side photograph of the 16-IC module. The 16-IC module is controlled by Xilinx Zynq UltraScale+ FPGA Kit. Fig. 4.35(b) shows the antenna array photograph at the back side. Each of the IC in the module is connected to a 2×2 dual-pol. antenna sub-array through the wide-band slot feedings. The PCB cross-sectional view is also demonstrated in Fig. 4.35(c).

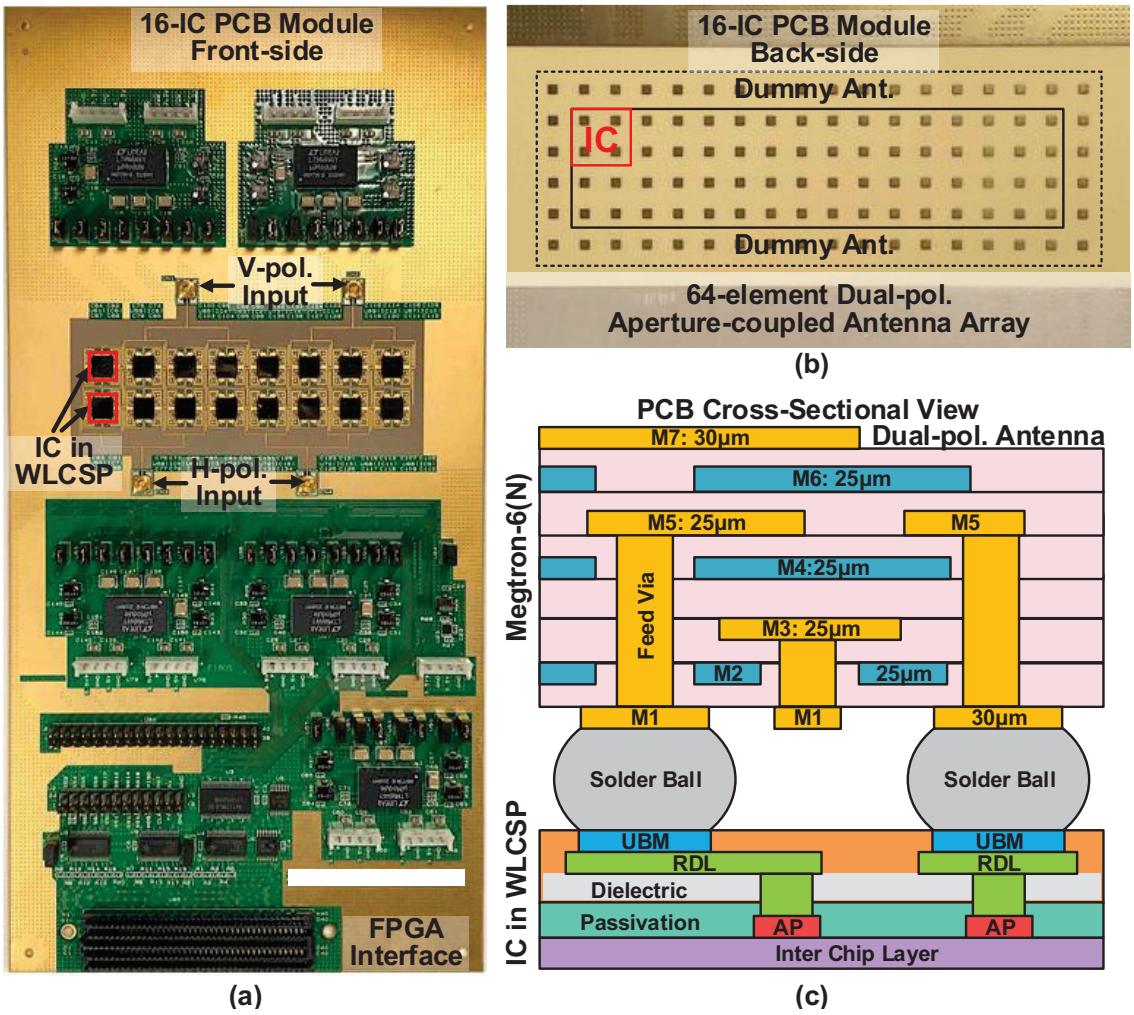


Figure 4.35: (a) Front-side photograph of proposed 16-IC phased-array module. (b) The 64-element dual-polarized aperture-coupled antenna array at the back-side. (c) 7-layer PCB cross-sectional view.

Fig. 4.36(a) shows the measured saturated EIRPs at the broadside against the number of activated beamformers. The proposed mismatch compensation technique is conducted to realize a better EIRP result. The measured single-element saturated EIRP is 20.1dBm, calculated by the saturated TX output power of 18.9dBm and $G_{ANT\_SE} - IL_{WLCSP}$. The single-element antenna gain G_{ANT_SE} with the WLCSP insertion loss IL_{WLCSP} equals 1.2dB. The measured saturated EIRP at room temperature reaches 55.2dBm for the 64-element phased-array module. The 64-element saturated EIRP can be estimated by 18.9dBm+ $20\log_{10}64 + G_{ANT\_ARR} - IL_{WLCSP}$, resulting in a 0.2-dB $G_{ANT\_ARR} - IL_{WLCSP}$. In this case, the antenna pattern gain G_{ANT_ARR} is around 1-dB smaller than the single-element antenna gain G_{ANT_SE} due to the additional coupling among the antenna array. Additional thermal solutions, such as heatsinks with high thermal conductivity and thermal area, are manda-

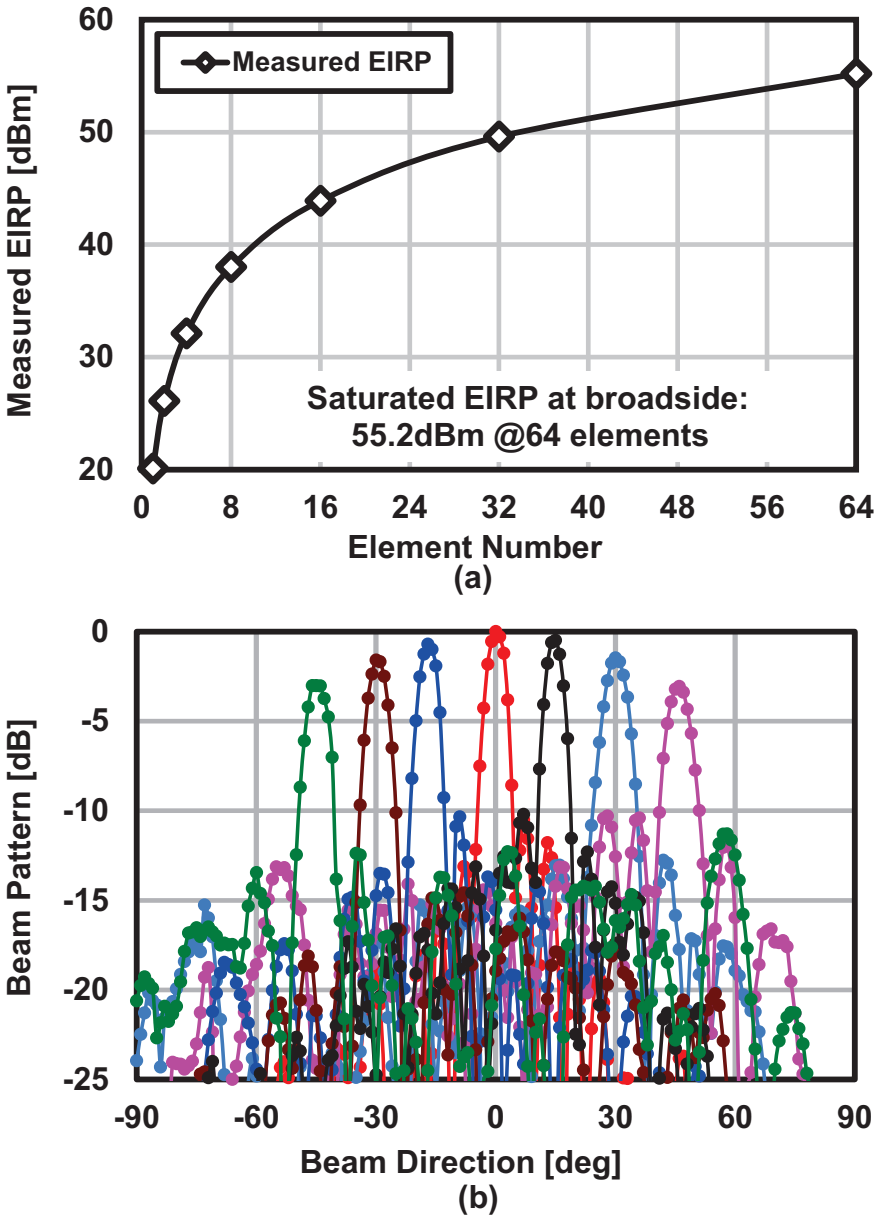
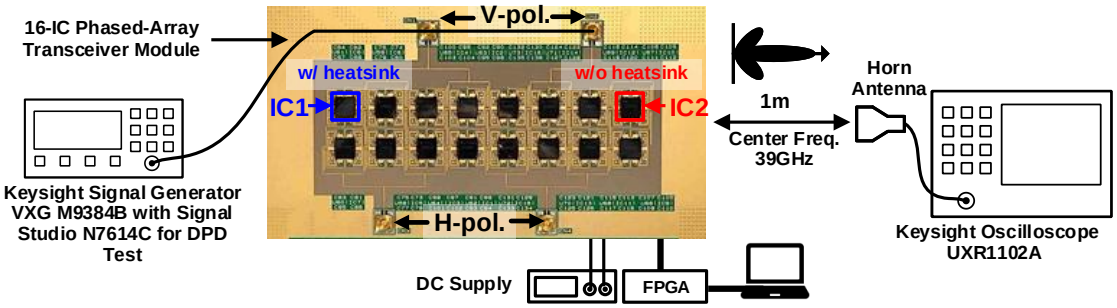


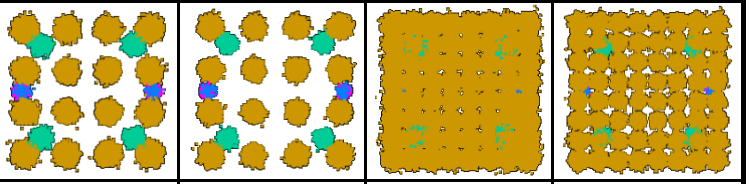
Figure 4.36: Measured TX-mode phased-array module continuous-wave features: (a) the saturated EIRPs at broadside against the number of beamformers and (b) measured 16×2 elements beam pattern in azimuth plane.

tory to maintain the high EIRP performance. Fig. 4.36(b) shows the measured 16×2 elements beam patterns in the azimuth plane. The phased-array module is able to cover ±45° scanning angle with <−10-dB sidelobe level. No tapering window is appended during the measurement.

To validate the proposed shared-LUT DPD with the inter-element mismatch compensation, an OTA measurement with the proposed phased-array module is performed. Fig.

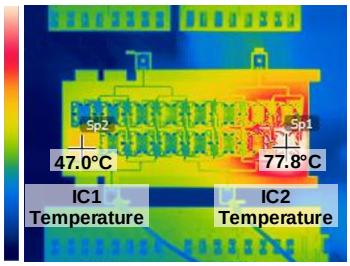


(a)

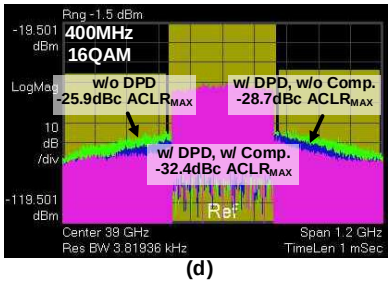
Modulation	16QAM OFDMA		64QAM OFMDA	
MCS* & BW	MCS 10 / 400MHz@39GHz		MCS 19 / 400MHz@39GHz	
Pout	11.4dBm/path		11.3dBm/path	
DPD	Yes	Yes	Yes	Yes
Inter-element Mismatch Compensation	NO	Yes	NO	Yes
Constellation				
TX ACLR	-28.7dBc	-32.4dBc	-28.7dBc	-32.1dBc
TX EVM (RMS)	7.5% (-22.5dB)	5.6% (-25.0dB)	7.6% (-22.4dB)	5.6% (-25.0dB)

*5G NR MCS index table2 for PDSCH is used. (Table 5.1.3.1-2 in 3GPP TS 38.214 V15.2.0)

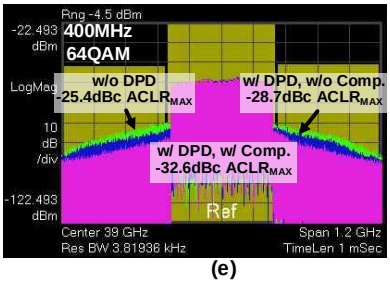
(c)



(d)



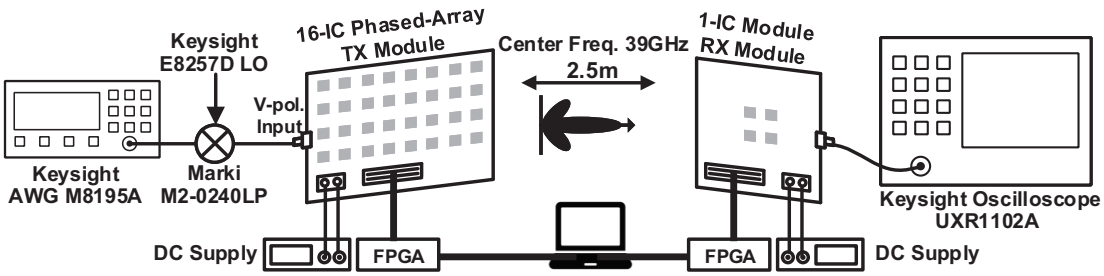
(d)



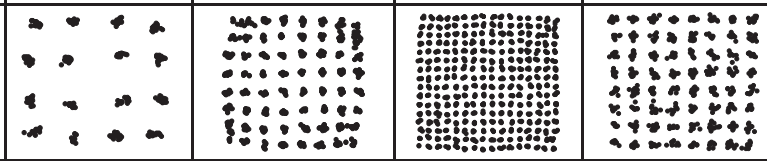
(e)

Figure 4.37: (a) Equipment setup for 2-IC 5G OFDMA-mode OTA measurement with shared-LUT DPD. (b) Thermal imaging photograph of the PCB module with temperature difference between IC1 and IC2. (c) Measured constellations, EVMs and ALCRs in both 16QAM and 64QAM OFDMA-mode with and without proposed inter-element mismatch compensation, (d) measured 400MHz 16QAM OFDMA-mode ACLRs and (e) measured 400MHz 64QAM OFDMA-mode ACLRs.

4.37(a) shows the equipment setup for this measurement. The Keysight signal generator VXG M9384B is used to generate the 5G-standard OFDMA-mode modulated signals. The Keysigh real-time oscilloscope UXR1102A is used to analyze the far-field signal caught by the horn antenna. To better extract the nonlinear behavior with the memory effect, the close-loop memory polynomial model is utilized. The DPD loop is controlled by Keysight signal studio N7614C for DPD Test, and the functions of Crest Factor Re-



(a)

64-to-4 elements TX-to-RX Single Carrier OTA	Modulation Scheme	16QAM	64QAM	256QAM	64QAM
	Baud Rate	400MSymbol/s			3.5GSymbol/s
	TX EIRP (64 elements)	49.6dBm	47.8dBm	45.1dBm	43.2dBm
	TX Constellation				
	TX EVM (RMS)	9.1% (-20.8dB)	5.6% (-25.0dB)	2.6% (-31.6dB)	5.5% (-25.2dB)
	TX-to-RX EVM (RMS)	11.8% (-18.6dB)	7.6% (-22.4dB)	3.4% (-29.4dB)	7.6% (-22.5dB)

(b)

Figure 4.38: (a) Equipment setup for TX-to-RX OTA SC-mode measurement in SISO scenario and (b) measured SC-mode constellations and EVMs.

duction (CFR) and Envelope Tracking (ET) are disabled during the measurement. Several types of PVT variation are considered in phased-array. Because the measured beamformer chips are manufactured in the same lot, the process influence is not obvious during the measurement. The simulated performance with process variations are given in Fig. 4.26. Considering the feasibility of the experiment, the temperature variation is performed to demonstrate the inter-element mismatch compensation. Two of the ICs, eight beamformer elements, located at relative distal positions are activated for EVM and ACLR measurements. The proposed compensation technique can be extended to full phased-array systems. Additional temperature difference is introduced between IC1 and IC2 by adding heat sink only to IC1. As demonstrated in Fig. 4.37(c), the measured temperatures with a thermal camera are 47.0°C and 77.8°C for IC1 and IC2, respectively. The DPD LUT is then extracted from IC1 and applied to both IC1 and IC2. The measurements are conducted in the condition with the proposed compensation technique or by turning off both the Vth compensation and gain/phase calibration. To minimize the input difference introduced by different DPD LUTs, the measurements are based on the same shared-LUT and referred to a fixed Pout per path. The 2-IC subarray achieves 30.3-dBm EIRP and 6% TX efficiency with an 11.3-dBm Pout per path. The measured 5G standard-compliant OFDMA-mode EVMs with shared-LUT DPD are improved from −22.5dB to −25.0dB in 16QAM and −22.4dB to −25.0dB in 64QAM. The corresponding ACLRs are sup-

pressed from −28.7dBc to −32.4dBc in 16QAM and −28.7dBc to −32.1dBc in 64QAM. Fig. 4.37(d) and (e) show the spectra measured in 400-MHz 16-QAM and 400-MHz 64-QAM, respectively. More than 6.5-dB ACLR enhancement is achieved by the proposed inter-element mismatch compensation with shared-LUT DPD. Significant improvement in linearity and power efficiency can be realized by utilizing the inter-element mismatch compensation in 5G NR applications.

The SC-mode OTA measurement is also performed as shown in Fig. 4.38(a). The SC-mode root-raised-cosine filtered signals are generated by Keysight arbitrary waveform generator M8195A. The corresponding roll-off factor is 0.35. The 64-element TX-mode beamformers and 4-element RX-mode beamformers are placed 2.5 meters apart in the measurement. The measurements are conducted after calibration without DPD and the broadside beam direction is selected during the measurement. Due to the different EVM requirements for different modulation schemes, this measurement is aiming for the highest EIRP on the base-station side with the EVM requirement fulfilled. As summarized in Fig. 4.38(b), under 400-MSymbol/s baudrate, the 64-element module can realize −20.8-dB EVM with 49.6-dBm EIRP in 16-QAM, −25.0-dB EVM with 47.8-dBm EIRP in 64-QAM and −31.6-dB EVM with 45.1-dBm EIRP in 256-QAM. The corresponding 64-to-4 elements TX-to-RX EVMs are −18.6dB, −22.4dB and −29.4dB, respectively. The 64-element module can also support 21-Gb/s SC-mode data streaming. The measured 64-element TX EVM is −25.2dB with 43.2-dBm EIRP in 3.5GSymbol/s 64-QAM modulation. The corresponding 64-to-4 elements TX-to-RX EVM is −22.5dB. The 64-element TX module cannot support 256-QAM with 3.5-GSymbol/s baud rate due to the high EVM requirement of 256-QAM modulation.

4.3.5 Summary

Table 4.4 compares this work with the state-of-the-art 39-GHz phased-array beamformers. The proposed bi-directional Doherty beamformer achieves excellent transceiver continuous-wave characteristics. A bi-directional Doherty PA-LNA is proposed and co-designed with WLCSP. The PA mode realizes 18.9-dBm saturated output power and 17.8% PAE at 6-dB PBO due to the Doherty technique. Thanks to the proposed inter-element mismatch compensation technique, the AM-AM and AM-PM characteristics are minimized between different elements over PVT variations, which enhances EVM and ACLR characteristics. The measured EVM and ACLR in 64QAM are improved from −22.4dB to −25.0dB and from −28.7dBc to −32.1dBc, respectively, with a shared-LUT DPD. In 64-to-4-element TX-to-RX communication, the 64-element module achieves a 55.2-dBm saturated EIRP and also supports 21-Gb/s SC-mode data streaming at 43.2dBm.

Table 4.4: Comparison With State-of-the-art 39GHz Beamformers.

		This work			[28] CMU JSSC2020	[11] Tokyo Tech JSSC2019	[24] Samsung ISSCC2020		[25] UCSD TMTT2020
Process		65nm CMOS			65nm CMOS	65nm CMOS	28nm CMOS		0.18μm SiGe BiCMOS
Freq. Band		39GHz			39GHz	39GHz	39GHz		39GHz
Beamformer Integration		Bi-directional Doherty PA-LNA, PS			Dual-band PA,LNA	Class-AB PA, LNA,PS	Stacked PA, LNA,PS		PA,LNA,PS
TX Psat#		18.9dBm			16.7dBm	15.5dBm	>16.5dBm		12.0dBm
TX EIRPsat in CW		55.2dBm 64 elements			N/A	53.0dBm 64 elements	N/A		51.0dBm 64 elements
PA Peak PAE		30.4%			22.2%	25.5%	N/A		N/A
PA PAE @6dB PBO		17.8%			<10%*	9.5%*	N/A		N/A
TX Peak Efficiency		19.3%			N/A	9.5%*	N/A		5%†
PDC/path		TX:402mW@18.9dBm 181mW@Static RX:87mW			TX:116.2mW @Static RX:37.6mW	TX:375mW RX:125mW	TX:105mW @6dBm RX:39mW		TX:250mW @11dBm RX:150mW
Area/path		0.82mm^{2}**			0.48mm^{2}	1.78mm^{2}*	0.77mm^{2}*		N/A
SC Mode	**Modulation Scheme**	64QAM			64QAM	N/A	N/A		64QAM
	Data Rate	21Gb/s			1.5Gb/s	N/A	N/A		30Gb/s
	EIRP in SC	43.2dBm 64 elements			6.5dBm***	N/A	N/A		34.0dBm 64 elements
5G OFDMA-Mode	**Modulation Scheme**	64QAM+			N/A	64QAM	64QAM		N/A
	Inter-Element Mismatch Comp.	No	No w/ DPD	Yes w/ DPD	N/A	No	No		N/A
	TX Pout/path [dBm]	11.3	11.3	11.3	N/A	3.6	6	8.8	N/A
	TX EVM [dB]	N/A	−22.4	−25	N/A	−24.6	−34	−27	N/A
	TX ACLR [dBc]	−25.4	−28.7	−32.1	N/A	N/A	−36.5	N/A	N/A

* Estimated from paper.
\# Probe measurement without packaging.
\+ 2-IC measurement results.
† Refer to OP1dB point.
** On-chip LDO and WLCSP included.
*** Only single-element data is available.

Chapter 5

Conclusion and Future Work

5.1 Conclusion

This thesis introduces the millimeter-wave CMOS phased-array beamformer designs for the low-cost and high-data-rate 5G and next-generation wireless communication networks. The 5G cellular network technical background and existing solutions are discussed at the beginning. Several novel building blocks and system architectures are proposed aiming at the challenges of millimeter-wave phased-array designs. Detailed analysis and design methodology are demonstrated in the following chapters. In this thesis, the proposed beamformers realize high area efficiency and power efficiency, which can be good candidates for the 5G NR applications and are also feasible for the next generation.

The operation frequency extension to millimeter-wave bands not only brings in huge bandwidth resources but also results in new design challenges. The extremely increased FSPL requires sufficient EIRP from base stations. The large-scale phased-array is mandatory to maintain the communication link budget. The array size can be traded off with the single TX-element output power to realize a given EIRP. Moreover, high-order modulation and high PAPR 5G-standard OFDMA-mode signals put up with a stringent requirement for the power back-off and beamformer linearity. The design of low-cost beamformers is becoming an increasingly important research topic.

The high-performance neutralized bi-directional circuits are proposed and optimized to significantly narrow the beamformer die area and lower the manufacturing cost. A novel bi-directional Doherty PA-LNA is proposed to enhance the TX back-off efficiency, which retains the merit of bi-directional operation with minimized die area penalty. The WLCSP co-design is implemented with less packaging insertion loss for better power efficiency. The bi-directional Doherty PA-LNA realizes 18.9-dBm saturated output power and 17.8% PAE at 6-dB PBO in PA mode. The proposed Doherty PA-LNA outperforms

the two-way power-combined class-AB PA by achieving approximately 1.8 times higher PAE at a 6-dB PBO region. Additionally, the Doherty PA-LNA occupies only 66.7% of the equivalent area in PA mode, making it a more efficient and area-saving option. The area-efficient bi-directional phase shifters are also proposed with 360° phase coverage. The measured rms phase and rms gain errors are less than 2° and 1.1dB, respectively.

The DP-MIMO configuration is able to increase the spectrum efficiency, thus improving the data rate. While, the cross-polarization leakage from the chip side, antenna side, and polarization rotation degrade the achievable DP-MIMO EVM and power efficiency. The cross-polarization leakage cancellation is proposed and demonstrated within a 28-GHz phased-array beamformer. Over 40-dB cross-polarization isolation is achieved with rotation between TX and RX. Around 7-dB EVM improvement is obtained in DP-MIMO with the cross-polarization leakage cancellation. Based on the 400-MHz 5G signals, 2×2 DP-MIMO communication in 256QAM can be supported with 3.3%EVM. Besides, the background cancellation is supported by reusing the calibration block, no other measurement equipment is required.

As an effective approach to improving the system linearity and power efficiency, the DPD technique is widely utilized in sub-6GHz communications. As for the hybrid phased-array systems, the shared-LUT is desired to simplify the baseband complexity. The nonlinearity improvement is limited due to the different characteristics of the different beamformer elements. This inter-element mismatch is even enlarged with the Doherty technique. To address this issue, an inter-element mismatch compensation technique is utilized to improve the DPD performance over PVT variations. The measured 64-QAM OFDMA-mode EVM and ACLR with the shared-LUT DPD are improved from −22.4dB to −25.0dB and from −28.7dBc to −32.1dBc, respectively.

The polarization correction and inter-element mismatch compensation improve system EVM, resulting in better power efficiency. In 64-to-4-element TX-to-RX communication, the 64-element module achieves a 55.2-dBm saturated EIRP and also supports 21-Gb/s single-carrier data streaming at 43.2dBm.

Fig. 5.1 compares the phased-array beamformer designs with the state-of-art 5G phased-arrays. The design target is to deliver higher output power with less area cost, meanwhile consuming less DC power. This work demonstrates its area efficiency, as shown in Fig. 5.1(a), by comparing the area per element with the average output power of the transmitter under 5G NR 64-QAM modulation. Furthermore, Fig. 5.1(b) illustrates the TX efficiency of this work compared to other 5G phased-arrays, in terms of both peak and average PAE. Besides, similar to the definition of power efficiency by normalizing pout to DC power consumption, the area efficiency can also be referred to the follows

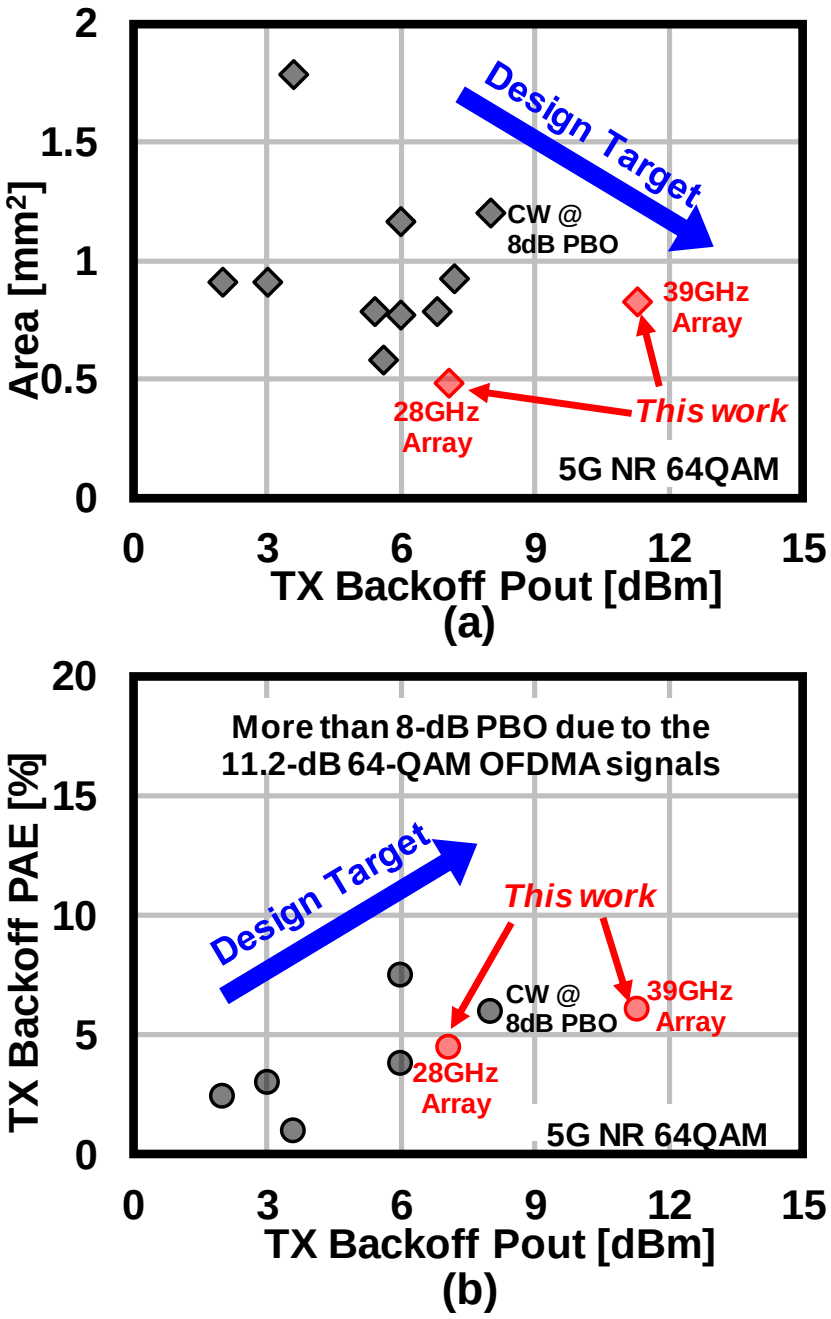


Figure 5.1: Comparison with the state-of-art 5G phased-arrays: (a) Area per element vs. TX backoff output power under 5G NR 64-QAM modulation, and (b) TX backoff efficiency vs. TX backoff output power under 5G NR 64-QAM modulation.

$$Normalized\ Output\ Power = \frac{Backoff\ Pout\ [\mathrm{mW}]}{Element\ Area\ [\mathrm{mm}^2]} \tag{5.1}$$

From Fig. 5.2, this work realizes the best area efficiency with reasonable power efficiency at a higher output power level. To draw a conclusion, this thesis introduces novel

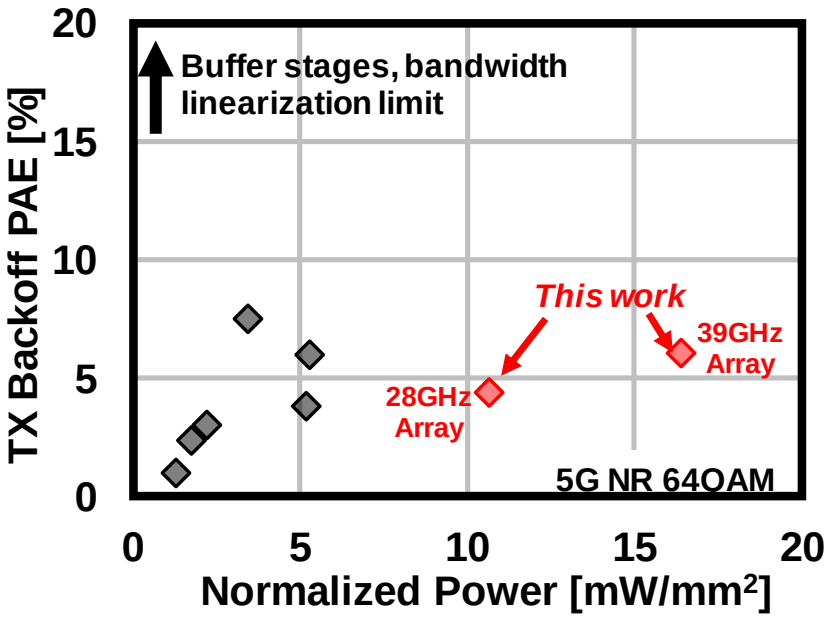


Figure 5.2: Comparison betweent area efficiency and power efficiency: TX backoff efficiency vs. normalized backoff output power under 5G NR 64-QAM modulation

techniques to enhance the area efficiency and power efficiency for 5G and next-generation applications. The high-performance phased-array beamformer design featured in low-cost high-data-rate could be realized.

5.2 Future Work

Today, we are living in the era of 5G and looking forward to the upcoming generation. As advanced manufacturing process becomes cheaper and more sophisticated, high-speed network access is becoming more common across various consumer electronics. However, the attempt to pursue higher communication speed will never stop. What's more, the network development towards the future is not only the Internet of Everything, but also the smarter information interaction environment. This section will discuss a brief outlook for future directions based on the research proposed in this thesis.

5.2.1 Next-Generation Network Exploration

Since the 1980s, mobile communication has revolutionized the world, transforming every aspect of our lives. With the specificated mMTC, uRLLC, and eMBB application scenarios, 5G has brought endless surprises to people. The capability of the next-generation networks will be far beyond the innovation of communication. With the flourishing of

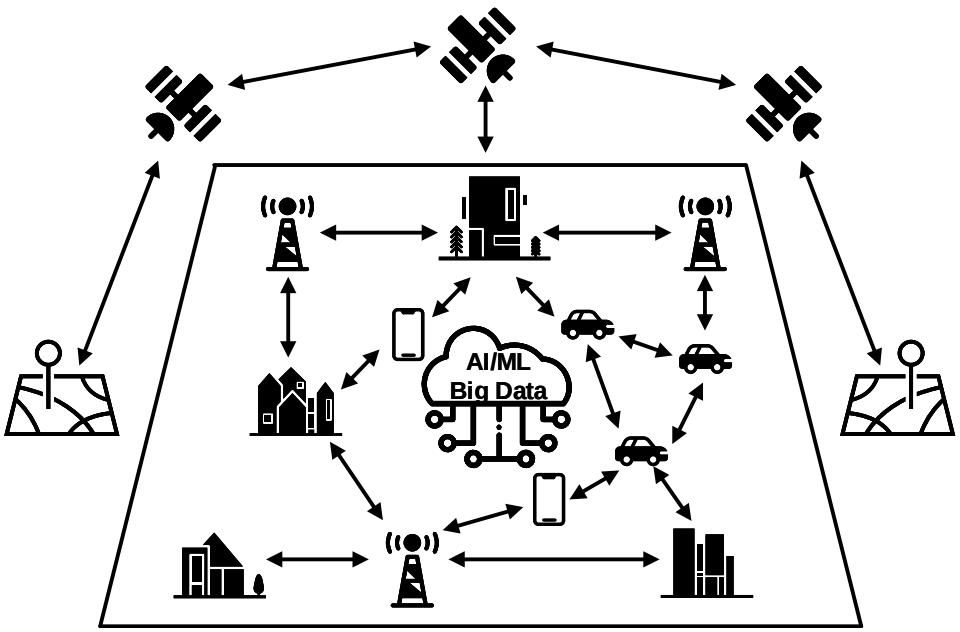


Figure 5.3: Next-generation network enables intelligent intereaction beyond communication

big data, artificial intelligence (AI), and machine learning (MI), we can envision the Intelligence of Everything in the near future. Fig. 5.3 illustrates the simplified scenarios for the next-generation network, supporting the smart society and with everything sensed and connected intelligently.

The future research direction is summarized as the following four points:

1) Tbs-level data rate with extreme-low latency: With the booming computational capability, the data for information exchange is increased exponentially. Some emerging applications will require data rates higher than 100Gb/s with extreme-low latency.

2) Energy-efficient system: Power consumption is always a big consideration in circuit design. The power consumption determines the life length of the wireless circuit. So a low power consumption is desired, which suffers a trade-off with high performance.

3) Coverage extension in non-line-of-sight (NLOS): The non-line-of-sight is used to define the situation when the TX and RX are not in direct line-of-sight. Since the beamforming technique is widely utilized at millimeter-wave bands to maintain the link budget in long-distance communication, the beam width becomes sharper

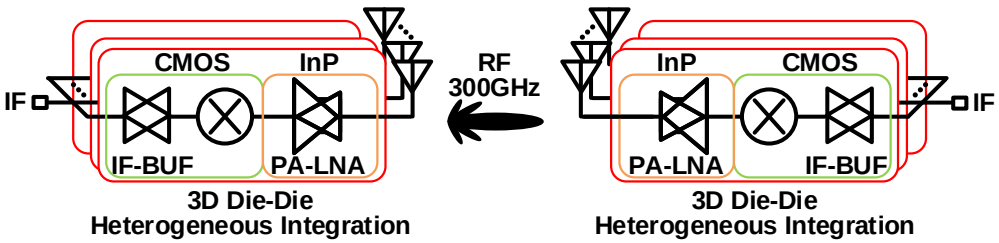


Figure 5.4: High-performance THz phased-array system

along with the increased array size. This makes communication easier obscured by obstacles, especially the dense high-rise buildings in the urban area. Based on strong computing power, each network terminal shares the information with each other like a server. The communication system can serve as a sensor, exploring radio wave transmission, reflection, and scattering to sense and better understand the physical world, ultimately providing a broad range of new services.

4) Integrated terrestrial and non-terrestrial networks: The integration with non-terrestrial networks, as shown in Fig. 5.3, makes it possible to deliver worldwide coverage. As the cost to manufacture and launch satellites decreases, plenty of low- or very low-earth orbit satellites will become a reality in non-terrestrial networks. The integration of terrestrial and non-terrestrial networks promises low-latency long-distance communication. This is good for auto-driving and remote sensing and imaging applications.

5.2.2 High-Performance THz Phased-Array

With the extension of operation frequency towards the THz-band, the next-generation communication envisions up to Tb/s-level peak data rate, 10~100-Gb/s experienced rate and sub-millisecond level latency. However, the propagation models and characteristics of the THz-band need to be studied and tested thoroughly to design suitable network topologies. In addition, baseband circuits such as ADCs, DACs, and digital processing circuits must provide ultra-wideband operation while consuming low power and small area. Besides, the RF beamformer IC alone is not feasible for THz-band applications, additional IF ICs or up-conversion functions are mandatory. Thus, the accurate GHz-to-THz frequency generation for LO source with ultra-low jitter and phase noise is desired [113–115]. Most importantly, the large carrier aggregation at THz bands requires designing a high-performance THz phased-array system. The high-order modulation and ultra-massive MIMO for spatial multiplexing are still effective in further improving the

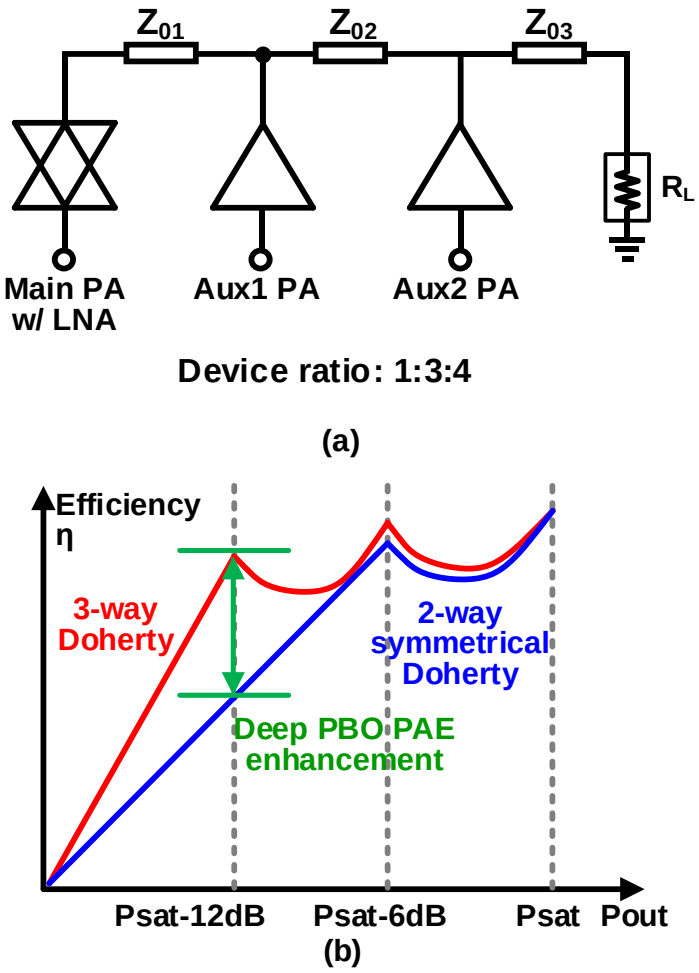


Figure 5.5: (a) Three-way asymmetrical Doherty PA-LNA and (b) the efficiency performance concept.

peak data rate. However, this provides a higher SNR requirement for the THz communication link budget. A possible research direction for the THz phased-array is shown in Fig. 5.4.

At THz bands, the smaller than chip size $\lambda/2$ antenna pitch limits the two-dimensional implementation on the PCB side. However, this makes the antenna integration on-chip become possible. Besides, according to the rule of thumb that the designed operation frequency is less than one-third of the $f_{\max}$, the advanced CMOS process with less than 10-nm gate length is required. Along with the CMOS scaling, the breakdown voltage decreases while the leakage current increases. Besides, the THz phased-array system is rather power-hungry than the 5G NR FR2 system due to the even higher FSPL, a sufficient TX output power is very useful to reduce the total system size. In this case, the high-

performance InP process with THz-level f_{max} can be a good candidate. To minimize the chip-to-chip interconnection loss between the CMOS-based IF chip and InP-based RF front-end, the 3D die-to-die heterogeneous integration can be implemented.

5.2.3 Energy-Efficient System

In future work, energy-efficient design is inevitably a big challenge for next-generation communications. The higher frequency bands, wider bandwidth, and denser distribution of massive antenna arrays in future phased-array systems will enable a single system to integrate wireless signal sensing and communication. The power-efficient base stations are desired. To reduce the total power consumption for phased-array while maintaining EIRP level, further improvement of PA architectures is required, which is also meaningful to lower the phased-array thermal issue. In addition to the base-station side, low-cost and low-power user equipment is urgently demanded to extend the battery life. That is to say, the high-performance PA-LNA becomes increasingly important in future phased-array systems.

As an extension of the area-efficient bi-directional technique in this work, one of the possible solutions of three-way asymmetrical Doherty PA-LNA aiming for the deep PBO power efficiency is shown in Fig. 5.5(a). By constructing the PA transistors ratio of main PA, auxiliary-1 PA and auxiliary-2 PA as 1:3:4, both the 6-dB and 12-dB PBO power efficiency can be improved. As shown in Fig. 5.5(b), compared with the two-way symmetrical Doherty PA, the additional 12-dB PBO efficiency enhancement is attractive due to the large PAPR high-order modulated signals.

The other bottleneck of the energy-efficient system is the output-matching passives, especially the transformer-based inductive components. Along with the increased carrier frequency, the PA transistor at the final stage of the TX chain still requires a relatively large size to provide sufficient TX output power, which means an unignorable device capacitance for output matching. While the required inductance becomes smaller and smaller to perform the LC resonance at the desired frequency and also prevent self-resonance. The smaller inductance shrinks down the passive footprint size, however limits the coupling factor k_m between the transformer windings. The maximum achievable transformer efficiency η can be derived from the follows [116]

$$\eta = \frac{1}{1 + \frac{2}{k_m^2 Q_P Q_S}(1 + \sqrt{1 + k_m^2 Q_P Q_S})} \tag{5.2}$$

where Q_P and Q_S are the quality factor of the transformer's primary and secondary windings. Although the Q_P and Q_S can be improved by selecting the thick metal layers with a

given manufacturing process, the available η still hardly surpasses 80%, which extremely degrades the THz-band PA PAE performance. To figure out this issue, several promising passive structures can be implemented, such as the distributed-balun and slotline-based balun architectures [117–119]. What's more, the high-performance power-combining technique is also one of the most attractive topics for future energy-efficient systems.

Bibliography

[1] J. S. Kilby, "Miniaturized electronic circuits [us patent no. 3,138, 743]," *IEEE Solid-State Circuits Society Newsletter*, vol. 12, no. 2, pp. 44–54, 2007.

[2] ——, "Method of making miniaturized electronic circuits," Jul. 19 1966, uS Patent 3,261,081.

[3] R. Pengelly and J. Turner, "Monolithic broadband ga as fet amplifiers." *Electronics letters*, vol. 12, p. 251, 1976.

[4] TSMC. Cmos process development map. [Online]. Available: https://www.tsmc.com/english/dedicatedFoundry/technology/logic/l_3nm

[5] J. G. Andrews, S. Buzzi, W. Choi, S. V. Hanly, A. Lozano, A. C. Soong, and J. C. Zhang, "What will 5g be?" *IEEE Journal on selected areas in communications*, vol. 32, no. 6, pp. 1065–1082, 2014.

[6] T. S. Rappaport, S. Sun, R. Mayzus, H. Zhao, Y. Azar, K. Wang, G. N. Wong, J. K. Schulz, M. Samimi, and F. Gutierrez, "Millimeter wave mobile communications for 5g cellular: It will work!" *IEEE access*, vol. 1, pp. 335–349, 2013.

[7] R. J. Mailloux, *Phased array antenna handbook*. Artech house, 2017.

[8] 3GPP, "3gpp specification series: 38.101-1, 5g specifications." [Online]. Available: https://portal.3gpp.org/desktopmodules/Specifications/SpecificationDetails.aspx?specificationId=3283

[9] J. Pang, Z. Li, R. Kubozoe, X. Luo, R. Wu, Y. Wang, D. You, A. A. Fadila, R. Saengchan, T. Nakamura, J. Alvin, D. Matsumoto, B. Liu, A. T. Narayanan, J. Qiu, H. Liu, Z. Sun, H. Huang, K. K. Tokgoz, K. Motoi, N. Oshima, S. Hori, K. Kunihiro, T. Kaneko, A. Shirane, and K. Okada, "A 28-ghz cmos phased-array beamformer utilizing neutralized bi-directional technique supporting dual-polarized mimo for 5g nr," *IEEE Journal of Solid-State Circuits*, vol. 55, no. 9, pp. 2371–2386, 2020.

[10] J. Pang, Z. Li, X. Luo, J. Alvin, R. Saengchan, A. A. Fadila, K. Yanagisawa, Y. Zhang, Z. Chen, Z. Huang *et al.*, "A cmos dual-polarized phased-array beamformer utilizing cross-polarization leakage cancellation for 5g mimo systems," *IEEE Journal of Solid-State Circuits*, vol. 56, no. 4, pp. 1310–1326, 2021.

[11] Y. Wang, R. Wu, J. Pang, D. You, A. A. Fadila, R. Saengchan, X. Fu, D. Matsumoto, T. Nakamura, R. Kubozoe *et al.*, "A 39-ghz 64-element phased-array transceiver with built-in phase and amplitude calibrations for large-array 5g nr in 65-nm cmos," *IEEE Journal of Solid-State Circuits*, vol. 55, no. 5, pp. 1249–1269, 2020.

[12] B. Sadhu, Y. Tousi, J. Hallin, S. Sahl, S. K. Reynolds, Ö. Renström, K. Sjögren, O. Haapalahti, N. Mazor, B. Bokinge *et al.*, "A 28-ghz 32-element trx phased-array ic with concurrent dual-polarized operation and orthogonal phase and gain control for 5g communications," *IEEE Journal of Solid-State Circuits*, vol. 52, no. 12, pp. 3373–3391, 2017.

[13] J. D. Dunworth, A. Homayoun, B. Ku, Y. Ou, K. Chakraborty, G. Liu, T. Segoria, J. Lerdworatawee, J. Park, H. Park *et al.*, "A 28ghz bulk-cmos dual-polarization phased-array transceiver with 24 channels for 5g user and basestation equipment," in *2018 IEEE International Solid-State Circuits Conference-(ISSCC)*. IEEE, 2018, pp. 70–72.

[14] K. Kibaroglu, M. Sayginer, A. Nafe, and G. M. Rebeiz, "A dual-polarized dual-beam 28 ghz beamformer chip demonstrating a 24 gbps 64-qam 2×2 mimo link," in *2018 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*. IEEE, 2018, pp. 64–67.

[15] K. Kibaroglu, M. Sayginer, and G. M. Rebeiz, "A low-cost scalable 32-element 28-ghz phased array transceiver for 5g communication links based on a 2×2 beamformer flip-chip unit cell," *IEEE Journal of Solid-State Circuits*, vol. 53, no. 5, pp. 1260–1274, 2018.

[16] S. Mondal, R. Singh, A. I. Hussein, and J. Paramesh, "A 25-30 ghz fully-connected hybrid beamforming receiver for mimo communication," *IEEE Journal of Solid-State Circuits*, vol. 53, no. 5, pp. 1275–1287, 2018.

[17] M.-Y. Huang, T. Chi, F. Wang, T.-W. Li, and H. Wang, "A 23-to-30ghz hybrid beamforming mimo receiver array with closed-loop multistage front-end beamformers for full-fov dynamic and autonomous unknown signal tracking and blocker

rejection," in *2018 IEEE International Solid-State Circuits Conference-(ISSCC)*. IEEE, 2018, pp. 68–70.

[18] H.-T. Kim, B.-S. Park, S.-S. Song, T.-S. Moon, S.-H. Kim, J.-M. Kim, J.-Y. Chang, and Y.-C. Ho, "A 28-ghz cmos direct conversion transceiver with packaged 2×4 antenna array for 5g cellular system," *IEEE Journal of Solid-State Circuits*, vol. 53, no. 5, pp. 1245–1259, 2018.

[19] Y. Yoon, K. H. An, D. Kang, K. Kim, S. Lee, J. S. Jang, D. Minn, B. Suh, J. Lee, J. Kim *et al.*, "A highly linear 28ghz 16-element phased-array receiver with wide gain control for 5g nr application," in *2019 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*. IEEE, 2019, pp. 287–290.

[20] A. Nafe, M. Sayginer, K. Kibaroglu, and G. M. Rebeiz, "2×64-element dual-polarized dual-beam single-aperture 28-ghz phased array with 2×30 gb/s links for 5g polarization mimo," *IEEE Transactions on Microwave Theory and Techniques*, vol. 68, no. 9, pp. 3872–3884, 2020.

[21] R. Garg, G. Sharma, A. Binaie, S. Jain, S. Ahasan, A. Dascurcu, H. Krishnaswamy, and A. S. Natarajan, "A 28-ghz beam-space mimo rx with spatial filtering and frequency-division multiplexing-based single-wire if interface," *IEEE Journal of Solid-State Circuits*, vol. 56, no. 8, pp. 2295–2307, 2020.

[22] B. Sadhu, A. Paidimarri, W. Lee, M. Yeck, C. Ozdag, Y. Tojo, J.-O. Plouchart, X. Gu, Y. Uemichi, S. Chakraborty *et al.*, "A 24-to-30ghz 256-element dual-polarized 5g phased array with fast beam-switching support for> 30,000 beams," in *2022 IEEE International Solid-State Circuits Conference (ISSCC)*, vol. 65. IEEE, 2022, pp. 436–438.

[23] A. G. Roy, O. Inac, A. Singh, T. Mukatel, O. Brandelstein, T. W. Brown, S. Abughazaleh, J. S. Hayden, B. Park, G. Bachmanek *et al.*, "A 37-40 ghz phased array front-end with dual polarization for 5g mimo beamforming applications," in *2019 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*. IEEE, 2019, pp. 251–254.

[24] H.-C. Park, D. Kang, S. Lee, B. Park, K. Kim, J. Lee, Y. Aoki, Y. Yoon, S. Lee, D. Lee *et al.*, "4.1 a 39ghz-band cmos 16-channel phased-array transceiver ic with a companion dual-stream if transceiver ic for 5g nr base-station applications," in *2020 IEEE International Solid-State Circuits Conference-(ISSCC)*. IEEE, 2020, pp. 76–78.

[25] Y. Yin, S. Zihir, T. Kanar, Q. Ma, H. Chung, L. Gao, and G. M. Rebeiz, "A 37–42-ghz 8× 8 phased-array with 48–51-dbm eirp, 64–qam 30-gb/s data rates, and evm analysis versus channel rms errors," *IEEE Transactions on Microwave Theory and Techniques*, vol. 68, no. 11, pp. 4753–4764, 2020.

[26] M.-Y. Huang and H. Wang, "21.2 a 27-to-41ghz mimo receiver with n-input-n-output using scalable cascadable autonomous array-based high-order spatial filters for instinctual full-fov multi-blocker/signal management," in *2019 IEEE International Solid-State Circuits Conference-(ISSCC)*. IEEE, 2019, pp. 346–348.

[27] S. Mondal and J. Paramesh, "A reconfigurable 28-/37-ghz mmse-adaptive hybrid-beamforming receiver for carrier aggregation and multi-standard mimo communication," *IEEE Journal of Solid-State Circuits*, vol. 54, no. 5, pp. 1391–1406, 2019.

[28] ——, "Power-efficient design techniques for mm-wave hybrid/digital fdd/full-duplex mimo transceivers," *IEEE Journal of Solid-State Circuits*, vol. 55, no. 8, pp. 2011–2026, 2020.

[29] S. Mondal, L. R. Carley, and J. Paramesh, "Dual-band, two-layer millimeter-wave transceiver for hybrid mimo systems," *IEEE Journal of Solid-State Circuits*, vol. 57, no. 2, pp. 339–355, 2021.

[30] A. Verma, V. Bhagavatula, A. Singh, W. Wu, H. Nagarajan, P.-K. Lau, X. Yu, O. Elsayed, A. Jain, A. Sarkar *et al.*, "A 16-channel, 28/39ghz dual-polarized 5g fr2 phased-array transceiver ic with a quad-stream if transceiver supporting non-contiguous carrier aggregation up to 1.6 ghz bw," in *2022 IEEE International Solid-State Circuits Conference (ISSCC)*, vol. 65. IEEE, 2022, pp. 1–3.

[31] E. Telatar, "Capacity of multi-antenna gaussian channels," *European transactions on telecommunications*, vol. 10, no. 6, pp. 585–595, 1999.

[32] W. L. Chan and J. R. Long, "A 58–65 ghz neutralized cmos power amplifier with pae above 10% at 1-v supply," *IEEE journal of solid-state circuits*, vol. 45, no. 3, pp. 554–564, 2010.

[33] M. Vigilante and P. Reynaert, "A wideband class-ab power amplifier with 29–57-ghz am–pm compensation in 0.9-v 28-nm bulk cmos," *IEEE Journal of Solid-State Circuits*, vol. 53, no. 5, pp. 1288–1301, 2017.

[34] Y. Wang, R. Wu, and K. Okada, "A compact 39-ghz 17.2-dbm power amplifier for 5g communication in 65-nm cmos," in *2018 IEEE International Symposium on Radio-Frequency Integration Technology (RFIT)*. IEEE, 2018, pp. 1–3.

[35] T.-W. Li, M.-Y. Huang, and H. Wang, "Millimeter-wave continuous-mode power amplifier for 5g mimo applications," *IEEE Transactions on Microwave Theory and Techniques*, vol. 67, no. 7, pp. 3088–3098, 2019.

[36] C. Elgaard, S. Andersson, P. Caputa, E. Westesson, and H. Sjöland, "A 27 ghz adaptive bias variable gain power amplifier and t/r switch in 22nm fd-soi cmos for 5g antenna arrays," in *2019 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*. IEEE, 2019, pp. 303–306.

[37] F. Wang and H. Wang, "A broadband linear ultra-compact mm-wave power amplifier with distributed-balun output network: Analysis and design," *IEEE Journal of Solid-State Circuits*, vol. 56, no. 8, pp. 2308–2323, 2021.

[38] K. Khalaf, V. Vidojkovic, K. Vaesen, M. Libois, G. Mangraviti, V. Szortyka, C. Li, B. Verbruggen, M. Ingels, A. Bourdoux *et al.*, "Digitally modulated cmos polar transmitters for highly-efficient mm-wave wireless communication," *IEEE Journal of Solid-State Circuits*, vol. 51, no. 7, pp. 1579–1592, 2016.

[39] C. R. Chappidi, X. Wu, and K. Sengupta, "Simultaneously broadband and back-off efficient mm-wave pas: A multi-port network synthesis approach," *IEEE Journal of Solid-State Circuits*, vol. 53, no. 9, pp. 2543–2559, 2018.

[40] F. Wang, T.-W. Li, S. Hu, and H. Wang, "A super-resolution mixed-signal doherty power amplifier for simultaneous linearity and efficiency enhancement," *IEEE Journal of Solid-State Circuits*, vol. 54, no. 12, pp. 3421–3436, 2019.

[41] H. Chireix, "High power outphasing modulation," *Proceedings of the Institute of Radio Engineers*, vol. 23, no. 11, pp. 1370–1392, 1935.

[42] T. W. Barton and D. J. Perreault, "Theory and implementation of rf-input outphasing power amplification," *IEEE Transactions on Microwave Theory and Techniques*, vol. 63, no. 12, pp. 4273–4283, 2015.

[43] T. Barton, "Not just a phase: Outphasing power amplifiers," *IEEE Microwave Magazine*, vol. 17, no. 2, pp. 18–31, 2016.

[44] H. Jang, R. Wilson, T. Canning, D. Seebacher, C. Schuberth, B. Arigong, F. Trang, and S. Ward, "Rf-input self-outphasing doherty–chireix combined amplifier," *IEEE Transactions on Microwave Theory and Techniques*, vol. 64, no. 12, pp. 4518–4534, 2016.

[45] S. Li, M.-Y. Huang, D. Jung, T.-Y. Huang, and H. Wang, "A mm-wave current-mode inverse outphasing transmitter front-end: A circuit duality of conventional voltage-mode outphasing," *IEEE Journal of Solid-State Circuits*, vol. 56, no. 6, pp. 1732–1744, 2020.

[46] K.-J. Cho, J.-H. Kim, and S. P. Stapleton, "A highly efficient doherty feedforward linear power amplifier for w-cdma base-station applications," *IEEE Transactions on Microwave Theory and Techniques*, vol. 53, no. 1, pp. 292–300, 2005.

[47] J.-H. Tsai and T.-W. Huang, "A 38–46 ghz mmic doherty power amplifier using post-distortion linearization," *IEEE Microwave and Wireless Components Letters*, vol. 17, no. 5, pp. 388–390, 2007.

[48] A. Agah, H.-T. Dabag, B. Hanafi, P. M. Asbeck, J. F. Buckwalter, and L. E. Larson, "Active millimeter-wave phase-shift doherty power amplifier in 45-nm soi cmos," *IEEE Journal of Solid-State Circuits*, vol. 48, no. 10, pp. 2338–2350, 2013.

[49] D. P. Nguyen, T. Pham, and A.-V. Pham, "A 28-ghz symmetrical doherty power amplifier using stacked-fet cells," *IEEE transactions on microwave theory and techniques*, vol. 66, no. 6, pp. 2628–2637, 2018.

[50] G. Nikandish, R. B. Staszewski, and A. Zhu, "Breaking the bandwidth limit: A review of broadband doherty power amplifier design for 5g," *IEEE Microwave Magazine*, vol. 21, no. 4, pp. 57–75, 2020.

[51] W. Shi, W. Shi, J. Peng, L. Feng, Y. Gao, S. He, and C. P. Yue, "Design and analysis of continuous-mode doherty power amplifier with second harmonic control," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 68, no. 7, pp. 2247–2251, 2021.

[52] D. Wang, W. Chen, X. Chen, X. Liu, F. M. Ghannouchi, and Z. Feng, "A 24-29.5 ghz voltage-combined doherty power amplifier based on compact low-loss combiner," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 68, no. 7, pp. 2342–2346, 2021.

[53] Z. Zong, X. Tang, K. Khalaf, D. Yan, G. Mangraviti, J. Nguyen, Y. Liu, and P. Wambacq, "A 28-ghz soi-cmos doherty power amplifier with a compact transformer-based output combiner," *IEEE Transactions on Microwave Theory and Techniques*, vol. 69, no. 6, pp. 2795–2808, 2021.

[54] S. Hu, F. Wang, and H. Wang, "A 28-/37-/39-ghz linear doherty power amplifier in silicon for 5g applications," *IEEE Journal of Solid-State Circuits*, vol. 54, no. 6, pp. 1586–1599, 2019.

[55] F. Wang, T.-W. Li, and H. Wang, "4.8 a highly linear super-resolution mixed-signal doherty power amplifier for high-efficiency mm-wave 5g multi-gb/s communications," in *2019 IEEE International Solid-State Circuits Conference-(ISSCC)*. IEEE, 2019, pp. 88–90.

[56] E. Kaymaksut, D. Zhao, and P. Reynaert, "Transformer-based doherty power amplifiers for mm-wave applications in 40-nm cmos," *IEEE Transactions on Microwave Theory and Techniques*, vol. 63, no. 4, pp. 1186–1192, 2015.

[57] P. Indirayanti and P. Reynaert, "A 32 ghz 20 dbm-p sat transformer-based doherty power amplifier for multi-gb/s 5g applications in 28 nm bulk cmos," in *2017 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*. IEEE, 2017, pp. 45–48.

[58] Y.-C. Chen, Y.-H. Lin, J.-L. Lin, and H. Wang, "A ka-band transformer-based doherty power amplifier for multi-gb/s application in 90-nm cmos," *IEEE Microwave and Wireless Components Letters*, vol. 28, no. 12, pp. 1134–1136, 2018.

[59] F. Wang and H. Wang, "24.1 a 24-to-30ghz watt-level broadband linear doherty power amplifier with multi-primary distributed-active-transformer power-combining supporting 5g nr fr2 64-qam with > 19dbm average pout and > 19% average pae," in *2020 IEEE International Solid-State Circuits Conference-(ISSCC)*. IEEE, 2020, pp. 362–364.

[60] H. T. Nguyen and H. Wang, "A coupler-based differential mm-wave doherty power amplifier with impedance inverting and scaling baluns," *IEEE Journal of Solid-State Circuits*, vol. 55, no. 5, pp. 1212–1223, 2020.

[61] V. Qunaj and P. Reynaert, "26.2 a doherty-like load-modulated balanced power amplifier achieving 15.5 dbm average p out and 20% average pae at a data rate of 18gb/s in 28nm cmos," in *2021 IEEE International Solid-State Circuits Conference (ISSCC)*. IEEE, 2021, pp. 356–358.

[62] M. Pashaeifar, L. C. De Vreede, and M. S. Alavi, "14.4 a 24-to-30ghz double-quadrature direct-upconversion transmitter with mutual-coupling-resilient series-doherty balanced pa for 5g mimo arrays," in *2021 IEEE International Solid-State Circuits Conference (ISSCC)*. IEEE, 2021, pp. 223–225.

[63] S. Kulkarni and P. Reynaert, "A 60-ghz power amplifier with am–pm distortion cancellation in 40-nm cmos," *IEEE Transactions on Microwave Theory and Techniques*, vol. 64, no. 7, pp. 2284–2291, 2016.

[64] S. N. Ali, P. Agarwal, J. Baylon, S. Gopal, L. Renaud, and D. Heo, "A 28ghz 41%-pae linear cmos power amplifier using a transformer-based am-pm distortion-correction technique for 5g phased arrays," in *2018 IEEE International Solid-State Circuits Conference-(ISSCC)*. IEEE, 2018, pp. 406–408.

[65] S. Golara, S. Moloudi, and A. A. Abidi, "Processes of am-pm distortion in large-signal single-fet amplifiers," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 64, no. 2, pp. 245–260, 2017.

[66] L. C. Nunes, P. M. Cabral, and J. C. Pedro, "Am/am and am/pm distortion generation mechanisms in si ldmos and gan hemt based rf power amplifiers," *IEEE Transactions on Microwave Theory and Techniques*, vol. 62, no. 4, pp. 799–809, 2014.

[67] S. Shakib, H.-C. Park, J. Dunworth, V. Aparin, and K. Entesari, "A highly efficient and linear power amplifier for 28-ghz 5g phased array radios in 28-nm cmos," *IEEE Journal of Solid-State Circuits*, vol. 51, no. 12, pp. 3020–3036, 2016.

[68] M. Vigilante and P. Reynaert, "A wideband class-ab power amplifier with 29–57-ghz am–pm compensation in 0.9-v 28-nm bulk cmos," *IEEE Journal of Solid-State Circuits*, vol. 53, no. 5, pp. 1288–1301, 2017.

[69] S. Shakib, M. Elkholy, J. Dunworth, V. Aparin, and K. Entesari, "2.7 a wideband 28ghz power amplifier supporting 8× 100mhz carrier aggregation for 5g in 40nm cmos," in *2017 IEEE International Solid-State Circuits Conference (ISSCC)*. IEEE, 2017, pp. 44–45.

[70] Y. Yi, D. Zhao, J. Zhang, P. Gu, Y. Chai, H. Liu, and X. You, "A 24–29.5-ghz highly linear phased-array transceiver front-end in 65-nm cmos supporting 800-mhz 64-qam and 400-mhz 256-qam for 5g new radio," *IEEE Journal of Solid-State Circuits*, vol. 57, no. 9, pp. 2702–2718, 2022.

[71] K. Onizuka, K. Ikeuchi, S. Saigusa, and S. Otaka, "A 2.4 ghz cmos doherty power amplifier with dynamic biasing scheme," in *2012 IEEE Asian Solid State Circuits Conference (A-SSCC)*. IEEE, 2012, pp. 93–96.

[72] H. T. Nguyen, T. Chi, S. Li, and H. Wang, "A linear high-efficiency millimeter-wave cmos doherty radiator leveraging multi-feed on-antenna active load modulation," *IEEE Journal of Solid-State Circuits*, vol. 53, no. 12, pp. 3587–3598, 2018.

[73] K. Takahashi, S. Yamanouchi, T. Hirayama, and K. Kunihiro, "An envelope tracking power amplifier using an adaptive biased envelope amplifier for wcdma handsets," in *2008 IEEE Radio Frequency Integrated Circuits Symposium*. IEEE, 2008, pp. 405–408.

[74] D. R. Morgan, Z. Ma, J. Kim, M. G. Zierdt, and J. Pastalan, "A generalized memory polynomial model for digital predistortion of rf power amplifiers," *IEEE Transactions on signal processing*, vol. 54, no. 10, pp. 3852–3860, 2006.

[75] K. Chuang, "Design considerations for behavioral modeling and pre-distortion of wide bandwidth wireless systems," in *2019 IEEE BiCMOS and Compound semiconductor Integrated Circuits and Technology Symposium (BCICTS)*. IEEE, 2019, pp. 1–6.

[76] L. Liu, W. Chen, L. Ma, and H. Sun, "Single-pa-feedback digital predistortion for beamforming mimo transmitter," in *2016 IEEE International Conference on Microwave and Millimeter Wave Technology (ICMMT)*, vol. 2. IEEE, 2016, pp. 573–575.

[77] S. Lee, M. Kim, Y. Sirl, E.-R. Jeong, S. Hong, S. Kim, and Y. H. Lee, "Digital predistortion for power amplifiers in hybrid mimo systems with antenna subarrays," in *2015 IEEE 81st Vehicular Technology Conference (VTC Spring)*. IEEE, 2015, pp. 1–5.

[78] X. Hu, T. Liu, Z. Liu, W. Wang, and F. M. Ghannouchi, "A novel single feedback architecture with time-interleaved sampling for multi-band dpd," *IEEE Communications Letters*, vol. 23, no. 6, pp. 1033–1036, 2019.

[79] S. Hesami, S. R. Aghdam, C. Fager, T. Eriksson, R. Farrell, and J. Dooley, "Single digital predistortion technique for phased array linearization," in *2019 IEEE International Symposium on Circuits and Systems (ISCAS)*. IEEE, 2019, pp. 1–5.

[80] S. Choi and E.-R. Jeong, "Digital predistortion based on combined feedback in mimo transmitters," *IEEE Communications Letters*, vol. 16, no. 10, pp. 1572–1575, 2012.

[81] N. Tervo, J. Aikio, T. Tuovinen, T. Rahkonen, and A. Parssinen, "Digital predistortion of amplitude varying phased array utilising over-the-air combining," in *2017 IEEE MTT-S International Microwave Symposium (IMS)*. IEEE, 2017, pp. 1165–1168.

[82] M. Abdelaziz, L. Anttila, A. Brihuega, F. Tufvesson, and M. Valkama, "Digital predistortion for hybrid mimo transmitters," *IEEE Journal of Selected Topics in Signal Processing*, vol. 12, no. 3, pp. 445–454, 2018.

[83] W. Pan, C. Li, X. Quan, W. Ma, Y. Liu, S. Shao, and Y. Tang, "Digital linearization of multiple power amplifiers in phased arrays for 5g wireless communications," in *2018 IEEE International Symposium on Signal Processing and Information Technology (ISSPIT)*. IEEE, 2018, pp. 247–251.

[84] X. Wang, Y. Li, C. Yu, W. Hong, and A. Zhu, "Digital predistortion of 5g massive mimo wireless transmitters based on indirect identification of power amplifier behavior with ota tests," *IEEE Transactions on Microwave Theory and Techniques*, vol. 68, no. 1, pp. 316–328, 2019.

[85] Q. Luo, X.-W. Zhu, C. Yu, and W. Hong, "Single-receiver over-the-air digital predistortion for massive mimo transmitters with antenna crosstalk," *IEEE Transactions on Microwave Theory and Techniques*, vol. 68, no. 1, pp. 301–315, 2019.

[86] E. Ng, Y. Beltagy, P. Mitran, and S. Boumaiza, "Single-input single-output digital predistortion of power amplifier arrays in millimeter wave rf beamforming transmitters," in *2018 IEEE/MTT-S International Microwave Symposium-IMS*. IEEE, 2018, pp. 481–484.

[87] X. Wang, C. Yu, Y. Li, W. Hong, and A. Zhu, "Real-time single channel over-the-air data acquisition for digital predistortion of 5g massive mimo wireless transmitters," in *2019 IEEE MTT-S International Wireless Symposium (IWS)*. IEEE, 2019, pp. 1–3.

[88] X. Liu, Q. Zhang, W. Chen, H. Feng, L. Chen, F. M. Ghannouchi, and Z. Feng, "Beam-oriented digital predistortion for 5g massive mimo hybrid beamforming transmitters," *IEEE Transactions on Microwave Theory and Techniques*, vol. 66, no. 7, pp. 3419–3432, 2018.

[89] N. Tervo, B. Khan, O. Kursu, J. P. Aikio, M. Jokinen, M. E. Leinonen, M. Juntti, T. Rahkonen, and A. Pärssinen, "Digital predistortion of phased-array transmitter

with shared feedback and far-field calibration," *IEEE Transactions on Microwave Theory and Techniques*, vol. 69, no. 1, pp. 1000–1015, 2021.

[90] Y. Liu, X. Xia, Q. Zhang, W. Pan, S. Shao, and Y. Tang, "Digital predistortion utilizing over-the-air feedback for phased arrays," *IEEE Access*, vol. 9, pp. 37 064–37 074, 2021.

[91] L. Ding, G. T. Zhou, D. R. Morgan, Z. Ma, J. S. Kenney, J. Kim, and C. R. Giardina, "A robust digital baseband predistorter constructed using memory polynomials," *IEEE Transactions on communications*, vol. 52, no. 1, pp. 159–165, 2004.

[92] D. Zhao and P. Reynaert, "A 60-ghz dual-mode class ab power amplifier in 40-nm cmos," *IEEE Journal of Solid-State Circuits*, vol. 48, no. 10, pp. 2323–2337, 2013.

[93] H. Asada, K. Matsushita, K. Bunsen, K. Okada, and A. Matsuzawa, "A 60ghz cmos power amplifier using capacitive cross-coupling neutralization with 16% pae," in *2011 41st European Microwave Conference*. IEEE, 2011, pp. 1115–1118.

[94] W. B. Kuhn and N. K. Yanduru, "Spiral inductor substrate loss modeling in silicon rf ics," in *Proceedings RAWCON 98. 1998 IEEE Radio and Wireless Conference*. IEEE, 1998, pp. 305–308.

[95] S. Gao, L. Li, M. Leong, and T. Yeo, "A broad-band dual-polarized microstrip patch antenna with aperture coupling," *IEEE transactions on antennas and propagation*, vol. 51, no. 4, pp. 898–900, 2003.

[96] S. K. Padhi, N. C. Karmakar, C. Law, and S. Aditya, "A dual polarized aperture coupled circular patch antenna using a c-shaped coupling slot," *IEEE transactions on antennas and propagation*, vol. 51, no. 12, pp. 3295–3298, 2003.

[97] P. K. Mishra, D. R. Jahagirdar, and G. Kumar, "A review of broadband dual linearly polarized microstrip antenna designs with high isolation," *IEEE Antennas and Propagation Magazine*, vol. 56, no. 6, pp. 238–251, 2014.

[98] T.-W. Li and H. Wang, "A millimeter-wave fully integrated passive reflection-type phase shifter with transformer-based multi-resonance loads for 360° phase shifting," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 65, no. 4, pp. 1406–1419, 2017.

[99] R. Garg and A. S. Natarajan, "A 28-ghz low-power phased-array receiver front-end with 360° rtps phase shift range," *IEEE Transactions on Microwave Theory and Techniques*, vol. 65, no. 11, pp. 4703–4714, 2017.

[100] P. Gu and D. Zhao, "Ka-band cmos 360° reflective-type phase shifter with±0.2 db insertion loss variation using triple-resonating load and dual-voltage control techniques," in *2018 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*. IEEE, 2018, pp. 140–143.

[101] H.-S. Lee and B.-W. Min, "W-band cmos 4-bit phase shifter for high power and phase compression points," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 62, no. 1, pp. 1–5, 2014.

[102] Z. Li, Z. Chen, Q. Wang, J. Liu, J. Pang, A. Shirane, and K. Okada, "A 41-ghz 19.4-dbm psat cmos doherty power amplifier for 5g nr applications," *IEICE Electronics Express*, vol. 20, no. 5, pp. 20 220 558–20 220 558, 2023.

[103] Z. Li, J. Pang, Y. Zhang, Y. Yamazaki, Q. Wang, P. Luo, W. Chen, Y. Liao, M. Tang, Y. Wang *et al.*, "A 39-ghz cmos bidirectional doherty phased-array beamformer using shared-lut dpd with inter-element mismatch compensation technique for 5g base station," *IEEE Journal of Solid-State Circuits*, 2023.

[104] J. Pang, R. Kubozoe, Z. Li, M. Kawabuchi, A. Shirane, and K. Okada, "A 28-ghz cmos vector-summing phase shifter featuring i/q imbalance calibration supporting 11.2 gb/s in 256qam for 5g new radio," *IEICE Transactions on Electronics*, vol. 103, no. 2, pp. 39–47, 2020.

[105] J. Pang, X. Luo, Z. Li, A. Shirane, and K. Okada, "A compact 37-40ghz cmos switch-type phase shifter with fine-tuning stage achieving 0.4-db rms gain error," in *2020 IEEE International Conference on Integrated Circuits, Technologies and Applications (ICTA)*. IEEE, 2020, pp. 5–6.

[106] Y. Li, Z. Duan, W. Lv, D. Pan, Z. Xie, Y. Dai, and L. Sun, "A 32-40 ghz 7-bit cmos phase shifter with 0.38 db/1.6 rms magnitude/phase errors for phased array systems," in *2020 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*. IEEE, 2020, pp. 319–322.

[107] E. Björnson, J. Hoydis, L. Sanguinetti *et al.*, "Massive mimo networks: Spectral, energy, and hardware efficiency," *Foundations and Trends® in Signal Processing*, vol. 11, no. 3-4, pp. 154–655, 2017.

[108] F. Meng, K. Ma, K. S. Yeo, and S. Xu, "A 57-to-64-ghz 0.094-mm 2 5-bit passive phase shifter in 65-nm cmos," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 24, no. 5, pp. 1917–1925, 2015.

[109] M. Leffel, "Intermodulation distortion in a multi-signal environment," *RF Design*, vol. 18, no. 6, pp. 78–85, 1995.

[110] N. B. De Carvalho and J. C. Pedro, "Compact formulas to relate acpr and npr to two-tone imr and ip3," *Microwave Journal*, vol. 42, no. 12, pp. 70–70, 1999.

[111] L. Magnelli, F. Crupi, P. Corsonello, C. Pace, and G. Iannaccone, "A 2.6 nw, 0.45 v temperature-compensated subthreshold cmos voltage reference," *IEEE Journal of Solid-State Circuits*, vol. 46, no. 2, pp. 465–474, 2011.

[112] Y. Yamazaki, J. Sakamaki, J. Pang, J. Alvin, Z. Li, A. Shirane, and K. Okada, "A 37-39ghz phase and amplitude detection circuit with 0.060 degree and 0.043db rms errors for the calibration of 5gnr phased-array beamforming," in *2022 IEEE Asian Solid-State Circuits Conference (A-SSCC)*, 2022, pp. 1–3.

[113] W. Wu, C.-W. Yao, C. Guo, P.-Y. Chiang, L. Chen, P.-K. Lau, Z. Bai, S. W. Son, and T. B. Cho, "A 14-nm ultra-low jitter fractional-n pll using a dtc range reduction technique and a reconfigurable dual-core vco," *IEEE Journal of Solid-State Circuits*, vol. 56, no. 12, pp. 3756–3767, 2021.

[114] Y. Shu, Z. Deng, and X. Luo, "8.3 a 28ghz scalable inter-core-shaping multi-core oscillator with dm/cm-configured coupling achieving 193.3 dbc/hz fom and 205.5 dbc/hz fom a at 1mhz offset," in *2023 IEEE International Solid-State Circuits Conference (ISSCC)*. IEEE, 2023, pp. 150–152.

[115] H. Guo, Y. Chen, Y. Huang, P.-I. Mak, and R. P. Martins, "8.4 an 83.3-to-104.7ghz harmonic-extraction vco incorporating multi-resonance, multi-core, and multi-mode (3m) techniques achieving -124dbc/hz absolute pn and 190.7dbc/hz FoM_t," in *2023 IEEE International Solid-State Circuits Conference (ISSCC)*. IEEE, 2023, pp. 152–154.

[116] I. Aoki, S. D. Kee, D. B. Rutledge, and A. Hajimiri, "Distributed active transformer-a new power-combining and impedance-transformation technique," *IEEE Transactions on Microwave Theory and Techniques*, vol. 50, no. 1, pp. 316–331, 2002.

[117] F. Wang and H. Wang, "A broadband linear ultra-compact mm-wave power amplifier with distributed-balun output network: Analysis and design," *IEEE Journal of Solid-State Circuits*, vol. 56, no. 8, pp. 2308–2323, 2021.

[118] X. Li, W. Chen, S. Li, Y. Wang, F. Huang, X. Yi, R. Han, and Z. Feng, "A high-efficiency 142–182-ghz sige bicmos power amplifier with broadband slotline-based power combining technique," *IEEE Journal of Solid-State Circuits*, vol. 57, no. 2, pp. 371–384, 2021.

[119] X. Li, W. Chen, H. Wu, S. Li, X. Yi, R. Han, and Z. Feng, "A 110-to-130 ghz sige bicmos doherty power amplifier with a slotline-based power combiner," *IEEE Journal of Solid-State Circuits*, vol. 57, no. 12, pp. 3567–3581, 2022.

Appendix A

Publication List

A.1 Journal Papers

- **Zheng Li**, Jian Pang, Yi Zhang, Yudai Yamazaki, Qiaoyu Wang, Peng Luo, Weichu Chen, Yijing Liao, Minzhe Tang, Yun Wang, Xi Fu, Dongwon You, Naoki Oshima, Shinichi Hori, Jeehoon Park, Kazuaki Kunihiro, Atsushi Shirane, Kenichi Okada, "A 39-GHz CMOS Bidirectional Doherty Phased-Array Beamformer Using Shared-LUT DPD With Inter-Element Mismatch Compensation Technique for 5G Base Station," *IEEE Journal of Solid-State Circuits (JSSC)*, vol. 58, no. 4, pp. 901-914, Apr. 2023.

- **Zheng Li**, Zixin Chen, Qiaoyu Wang, Junqing Liu, Jian Pang, Atsushi Shirane, Kenichi Okada, "A 41-GHz 19.4-dBm P_{SAT} CMOS Doherty power amplifier for 5G NR applications," IEICE Electronics Express, vol. 20, no. 5, p. 20220558, Feb. 2023.

A.2 International Conferences and Workshops

- **Zheng Li**, Peng Luo, Jian Pang, Qiaoyu Wang, Atsushi Shirane, Kenichi Okada, "A 24–49-GHz CMOS Area-Efficient Phase-Invariant Mixed-Type Attenuator With Capacitive Compensation for 5G New Radio," *IEEE 49th European Solid-State Circuits Conference (ESSCIRC)*, Accepted, 2023.

- **Zheng Li**, Jian Pang, Yi Zhang, Yudai Yamazaki, Qiaoyu Wang, Peng Luo, Weichu Chen, Yijing Liao, Minzhe Tang, Zhengya Guo, Yun Wang, Xi Fu, Dongwon You, Naoki Oshima, Shinichi Hori, Kazuaki Kunihiro, Atsushi Shirane, Kenichi Okada,

"A 39-GHz CMOS Bidirectional Doherty PhasedArray Beamformer Using Shared-LUT DPD With Inter-Element Mismatch Compensation Technique for 5G Base Station," *IEEE Symposium on VLSI Technology and Circuits (VLSI Technology and Circuits)*, Honolulu, HI, pp. 98-99, Jun. 2022.

- **Zheng Li**, Zixin Chen, Qiaoyu Wang, Jian Pang, Atsushi Shirane, Kenichi Okada, "A 41-GHz 19.4-dBm P_{SAT} CMOS Doherty power amplifier for 5G NR applications," *IEEE International Conference on Integrated Circuits, Technologies and Applications (ICTA)*, Xi'an, China, pp. 32-33, Oct. 2022. (Best paper award)

- **Zheng Li**, Jian Pang, Ryo Kubozoe, Xueting Luo, Rui Wu, Yun Wang, Dongwon You, Ashbir Aviat Fadila, Joshua Alvin, Bangan Liu, Zheng Sun, Hongye Huang, Atsushi Shirane, Kenichi Okada, "A 28GHz CMOS Differential Bi-Directional Amplifier for 5G NR," *25th Asia and South Pacific Design Automation Conference (ASP-DAC)*, Beijing, China, pp. 5-6, Jan. 2020.

A.3 Domestic Conferences and Workshops

- **Zheng Li**, Jian Pang, Atsushi Shirane, Kenichi Okada, "An Inter-Element Mismatch Compensation Technique Utilizing Shared-LUT DPD Strategy for 5G Doherty Phased-Array System," *IEICE Society Conference*, Sendai, Sep. 2022.

- **Zheng Li**, Jian Pang, Yi Zhang, Yudai Yamazaki, Qiaoyu Wang, Peng Luo, Weichu Chen, Yijing Liao, Minzhe Tang, Zhengya Guo, Yun Wang, Xi Fu, Dongwon You, Naoki Oshima, Shinichi Hori, Kazuaki Kunihiro, Atsushi Shirane, Kenichi Okada, "A 39-GHz CMOS Bidirectional Doherty PhasedArray Beamformer Using Shared-LUT DPD With Inter-Element Mismatch Compensation Technique for 5G Base Station," *Integrated Circuits and Devices Workshop*, online, Aug. 2022. (invited talk)

- **Zheng Li**, Jian Pang, Atsushi Shirane, Kenichi Okada, "A 28-GHz CMOS Phased-Array Beamformer Supporting Dual-Polarized MIMO with Cross-Polarization Leakage Cancellation," *IEICE Society Conference*, online, Sep. 2021.

- **Zheng Li**, Jian Pang, Xueting Luo, Atsushi Shirane, Kenichi Okada, "A 28-GHz CMOS Phased-Array Beamformer Supporting Dual-Polarized MIMO with Cross-Polarization Leakage Cancellation," *LSI and System Workshop*, Tokyo, May. 2021.

- **Zheng Li**, Jian Pang, Zhongliang Huang, Atsushi Shirane, Kenichi Okada, "A 39-GHz CMOS Bi-Directional Amplifier for 5G Phased-Array Transceiver," *IEICE Society Conference*, online, Mar. 2020.

- **Zheng Li**, Jian Pang, Ryo Kubozoe, Xueting Luo, Rui Wu, Yun Wang, Dongwon You, Ashbir Aviat Fadila, Rattanan Saengchan, Takeshi Nakamura, Joshua Alvin, Daiki Matsumoto, Aravind Tharayil Narayanan, Bangan Liu, Atsushi Shirane, Kenichi Okada, "A 28GHz CMOS Phased-Array Beamformer with Bi-Directional Technique for 5G NR," *LSI and System Workshop*, Tokyo, May. 2019.

- **Zheng Li**, Jian Pang, Xueting Luo, Atsushi Shirane, Kenichi Okada, "Millimeter-wave CMOS Differential Bi-directional Amplifier for 5G Communication," *IEICE Society Conference*, Osaka, Sep. 2019.

A.4 Co-Author

A.4.1 Journals and Letters

- Jian Pang, **Zheng Li**, Yi Zhang, Minzhe Tang, Minghao Fan, Atsushi Shirane, Kenichi Okada, "A Compact 28GHz Bi-Directional Power-Combined Antenna Interface in WLCSP for 5G and B5G Transceivers," *IEEE Solid-State Circuits Letters (SSCL)*, Early Access, 2023.

- Yudai Yamazaki, Jun Sakamaki, Jian Pang, Joshua Alvin, **Zheng Li**, Dongwon You, Jill Mayeda, Atsushi Shirane, Kenichi Okada, "A 37-43.5-GHz Phase and Amplitude Detection Circuit With 0.049° and 0.036-dB Accuracy for 5G Phased-Array Calibration Using Transformer-Based Injection-Enhanced ILFD," *IEEE Journal of Solid-State Circuits (JSSC)*, Early Access, 2023.

- Dongwon You, Xi Fu, Hans Herdian, Xiaolin Wang, Yasuto Narukiyo, Ashbir Aviat Fadila, Hojun Lee, Michihiro Ide, Sena Kato, **Zheng Li**, Yun Wang, Daisuke Awaji, Jian Pang, Hiraku Sakamoto, Kenichi Okada, Atsushi Shirane, "A *Ka*-Band 64-Element Deployable Active Phased-Array TX on a Flexible Hetero Segmented Liquid Crystal Polymer for Small Satellites," *IEEE Microwave and Wireless Technology Letters (MWTL)*, Early Access, 2023.

- Yi Zhang, Jian Pang, **Zheng Li**, Minzhe Tang, Yijing Liao, Ashbir Aviat Fadila, Atsushi Shirane, Kenichi Okada, "A Power-Efficient CMOS Multi-Band Phased-Array Receiver Covering 24–71-GHz Utilizing Harmonic-Selection Technique With

36-dB Inter-Band Blocker Tolerance for 5G NR," *IEEE Journal of Solid-State Circuits (JSSC)*, vol. 57, no. 12, pp. 3617-3630, Dec. 2022.

- Jian Pang, Xueting Luo, **Zheng Li**, Atsushi Shirane, Kenichi Okada, "A Compact and High-Resolution CMOS Switch-Type Phase Shifter Achieving 0.4-dB RMS Gain Error for 5G n260 Band," *IEICE Transactions on Electronics*, vol. 195, no. 3, pp. 102-109, Mar. 2022.

- Xi Fu, Yun Wang, Xiaolin Wang, Xiaofan Gu, Xueting Luo, **Zheng Li**, Jian Pang, Atsushi Shirane, Kenichi Okada, "An 8.5-dB Insertion Loss and 0.8° RMS Phase Error Ka-Band CMOS Hybrid Phase Shifter Featuring Nonuniform Matching for Satellite Communication," *IEICE Transactions on Electronics*, 2021CTP0002, 2022.

- Xi Fu, Yun Wang, **Zheng Li**, Atsushi Shirane, Kenichi Okada, "A CMOS SPDT RF Switch with 68dB Isolation and 1.0 dB Loss Feathering Switched Resonance Network for MIMO Applications," *IEICE Transactions on Electronics*, vol. 104, no. 7, pp. 280-288, Jul. 2021.

- Jian Pang, **Zheng Li**, Xueting Luo, Joshua Alvin, Rattanan Saengchan, Ashbir Aviat Fadila, Kiyoshi Yanagisawa, Yi Zhang, Zixin Chen, Zhongliang Huang, Xiaofan Gu, Rui Wu, Yun Wang, Dongwon You, Bangan Liu, Zheng Sun, Yuncheng Zhang, Hongye Huang, Naoki Oshima, Keiichi Motoi, Shinichi Hori, Kazuaki Kunihiro, Tomoya Kaneko, Atsushi Shirane, Kenichi Okada, "A CMOS dual-polarized phased-array beamformer utilizing cross-polarization leakage cancellation for 5G MIMO systems," *IEEE Journal of Solid-State Circuits (JSSC)*, vol. 56, no. 4, pp. 1310-1326, Jan. 2021.

- Zheng Sun, Hanli Liu, Dingxin Xu, Hongye Huang, Bangan Liu, **Zheng Li**, Jian Pang, Teruki Someya, Atsushi Shirane, Kenichi Okada, "A low-jitter injection-locked clock multiplier using 97-μW transformer-based VCO with 18-kHz flicker noise corner," *IEICE Transactions on Electronics*, 2020CDP0005, Mar. 2021.

- Zheng Sun, Hanli Liu, Hongye Huang, Dexian Tang, Dingxin Xu, Tohru Kaneko, **Zheng Li**, Jian Pang, Rui Wu, Wei Deng, Atsushi Shirane, Kenichi Okada, "A 0.85mm^2 BLE Transceiver Using an On-Chip Harmonic-Suppressed RFIO Circuitry With T/R Switch," *IEEE Transactions on Circuits and Systems I: Regular Papers (TCASI)*, vol. 68, no. 1, pp. 196-209, Nov. 2020.

- Jian Pang, **Zheng Li**, Ryo Kubozoe, Xueting Luo, Rui Wu, Yun Wang, Dongwon You, Ashbir Aviat Fadila, Rattanan Saengchan, Tekeshi Nakamura, Joshua Alvin,

Daiki Matsumoto, Bangan Liu, Aravind Tharayil Narayanan, Junjun Qiu, Hanli Liu, Zheng Sun, Hongye Huang, Korkut Kaan Tokgoz, Keiichi Motoi, Naoki Oshima, Shinichi Hori, Kazuaki Kunihiro, Tomoya Kaneko, Atsushi Shirane, Kenichi Okada, "A 28-GHz CMOS Phased-Array Beamformer Utilizing Neutralized Bi-Directional Technique Supporting Dual-Polarized MIMO for 5G NR," *IEEE Journal of Solid-State Circuits (JSSC)*, vol. 55, no. 9, pp. 2371-2386, Sep. 2020.

- Bangan Liu, Yuncheng Zhang, Junjun Qiu, Hongye Huang, Zheng Sun, Dingxin Xu, Haosheng Zhang, Yun Wang, Jian Pang, **Zheng Li**, Xi Fu, Atsushi Shirane, Hitoshi Kurosu, Yoshinori Nakane, Shunichiro Masaki, Kenichi Okada, "A fully-synthesizable fractional-N injection-locked PLL for digital clocking with triangle/sawtooth spread-spectrum modulation capability in 5-nm CMOS," *IEEE Solid-State Circuits Letters (SSCL)*, vol. 195, pp. 34-37, Jan. 2020.

- Zheng Sun, Dingxin Xu, Hongye Huang, **Zheng Li**, Hanli Liu, Bangan Liu, Jian Pang, Teruki Someya, Atsushi Shirane, Kenichi Okada, "A Compact TF-Based LC-VCO with Ultra-Low-Power Operation and Supply Pushing Reduction for IoT Applications," *IEICE Transactions on Electronics*, 2019CTP0005, 2020.

- Jian Pang, Korkut Kaan Tokgoz, Shotaro Maki, **Zheng Li**, Xueting Luo, Ibrahim Abdo, Seitaro Kawai, Hanli Liu, Zheng Sun, Bangan Liu, Makihiko Katsuragi, Kento Kimura, Atsushi Shirane, Kenichi Okada, "A 28.16-Gbs area-efficient 60-GHz CMOS bidirectional transceiver for IEEE 802.11 ay," *IEEE Transactions on Microwave Theory and Techniques (TMTT)*, vol. 68, no. 1, pp. 252-263, Mar. 2019.

- Jian Pang, Rui Wu, Yun Wang, Masato Dome, Hisashi Kato, Hongye Huang, Aravind Tharayil Narayanan, Hanli Liu, Bangan Liu, Takeshi Nakamura, Takuya Fujimura, Masaru Kawabuchi, Ryo Kubozoe, Tsuyoshi Miura, Daiki Matsumoto, **Zheng Li**, Naoki Oshima, Keiichi Motoi, Shinichi Hori, Kazuaki Kunihiro, Tomoya Kaneko, Atsushi Shirane, Kenichi Okada, "A 28-GHz CMOS phased-array transceiver based on LO phase-shifting architecture with gain invariant phase tuning for 5G new radio," *IEEE Journal of Solid-State Circuits (JSSC)*, vol. 54, no. 5, pp. 1228-1242, Mar. 2019.

A.4.2 Conferences

- Xi Fu, Dongwon You, Xiaolin Wang, Michihiro Ide, Yuncheng Zhang, Jun Sakamaki, Ashibir Aviat Fadila, **Zheng Li**, Yun Wang, Jumpei Sudo, Makoto Higaki,

Soichiro Inoue, Takashi Eishima, Takashi Tomura, Jian Pang, Hiroyuki Sakai, Kenichi Okada, Atsushi Shirane, "A 2.95 mWelement Ka-band CMOS Phased-Array Receiver Utilizing On-Chip Distributed Radiation Sensors in Low-Earth-Orbit Small Satellite Constellation," *IEEE International Solid-State Circuits Conference (ISSCC)*, San Francisco, CA, pp. 18-20, Feb. 2023.

- Dongwon You, Xi Fu, Xiaolin Wang, Yuan Gao, Wenqian Wang, Jun Sakamaki, Hans Herdian, Sena Kato, Michihiro Ide, Yuncheng Zhang, Ashbir Aviat Fadila, Zheng Li, Chun Wang, Yun Wang, Jumpei Sudo, Makoto Higaki, Nahoka Kawaguchi, Masaya Nitta, Soichiro Inoue, Takashi Eishima, Takashi Tomura, Jian Pang, Hiroyuki Sakai, Kenichi Okada, Atsushi Shirane, "A Small-Satellite-Mounted 256-Element Ka-Band CMOS Phased-Array Transmitter Achieving 63.8 dBm EIRP Under 26.6 W Power Consumption Using SingleDual Circular Polarization Active Coupler," *IEEE International Solid-State Circuits Conference (ISSCC)*, San Francisco, CA, pp. 298-300, Feb. 2023.

- Yudai Yamazaki, Jun Sakamaki, Jian Pang, Joshua Alvin, **Zheng Li**, Atsushi Shirane, Kenichi Okada, "A 37-39GHz Phase and Amplitude Detection Circuit with 0.060 degree and 0.043 dB RMS Errors for the Calibration of 5GNR Phased-Array Beamforming," *IEEE Asian Solid-State Circuits Conference (A-SSCC)*, Taipei, Taiwan, pp. 1-3, Nov. 2022.

- Kenichi Okada, Jian Pang, Atsushi Shirane, **Zheng Li**, Yi Zhang, Naoki Oshima, Shinichi Hori, Kazuaki Kunihiro, "Millimeter-Wave CMOS Phased-Array Transceivers for 5G and Beyond," *IEEE 33rd Annual International Symposium on Personal, Indoor and Mobile Radio Communications (PIMRC)*, Kyoto, Japan, pp. 1-6, Sep. 2022.

- Dongwon You, Yun Wang, Xi Fu, Hans Herdian, Xiaolin Wang, Ashbir Fadila, Hojun Lee, Michihiro Ide, Sena Kato, **Zheng Li**, Jian Pang, Atsushi Shirane, Kenichi Okada, "A Ka-Band Dual Circularly Polarized CMOS Transmitter with Adaptive Scan Impedance Tuner and Active XPD Calibration Technique for Satellite Terminal," *IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, Denver, CO, pp. 15-18, Jun. 2022.

- Xiaolin Wang, Dongwon You, Xi Fu, Hojun Lee, **Zheng Li**, Daisuke Awaji, Jian Pang, Atsushi Shirane, Hiraku Sakamoto, Kenichi Okada, "A Flexible Implementation of Ka-Band Active Phased Array for Satellite Communication," *IEEE/MTT-S International Microwave Symposium (IMS)*, Denver, CO, pp. 753-756, Jun. 2022.

- Xi Fu, Yun Wang, Dongwon You, Xiaolin Wang, Ashbir Aviat Fadila, Yi Zhang, Sena Kato, Chun Wang, **Zheng Li**, Jian Pang, Atsushi Shirane, Kenichi Okada, "A 3.4 mWelement Radiation-Hardened Ka-Band CMOS Phased-Array Receiver Utilizing Magnetic-Tuning Phase Shifter for Small Satellite Constellation," *IEEE International Solid-State Circuits Conference (ISSCC)*, San Francisco, CA, pp. 90-92, Feb. 2022.

- Jian Pang, Yi Zhang, **Zheng Li**, Minzhe Tang, Yijing Liao, Ashbir Aviat Fadila, Atsushi, "A Power-Efficient 24-to-71 GHz CMOS Phased-Array Receiver Utilizing Harmonic-Selection Technique Supporting 36dB Inter-Band Blocker Rejection for 5G NR," *IEEE International Solid-State Circuits Conference (ISSCC)*, San Francisco, CA, pp. 434-436, Feb. 2022.

- Yi Zhang, Jian Pang, **Zheng Li**, Atsushi Shirane, Kenichi Okada, "A 28GHz Bi-direction Transceiver with Temperature Compensation," *IEEE International Conference on Integrated Circuits, Technologies and Applications (ICTA)*, Zhuhai, China, pp. 80-81, Nov. 2021.

- Zheng Sun, Dingxin Xu, Junjun Qiu, Zezheng Liu, Yuncheng Zhang, Hongye Huang, Hanli Liu, Bangan Liu, **Zheng Li**, Jian Pang, Atsushi Shirane, Kenichi Okada "A 0.25 mm^2 BLE Transmitter with Direct Antenna Interface and 19% System Efficiency Using Duty-Cycled Edge-Timing Calibration," *IEEE 47th European Solid State Circuits Conference (ESSCIRC)*, Grenoble, Francea, pp. 499-502, Sep. 2021.

- Jian Pang, **Zheng Li**, Xueting Luo, Joshua Alvin, Kiyoshi Yanagisawa, Yi Zhang, Zixin Chen, Zhongliang Huang, Xiaofan Gu, Weichu Chen, Yun Wang, Dongwon You, Zheng Sun, Yuncheng Zhang, Hongye Huang, Naoki Oshima, Keiichi Motoi, Shinichi Hori, Kazuaki Kunihiro, Tomoya Kaneko, Atsushi Shirane, Kenichi Okada, "A Fast-Beam-Switching 28-GHz Phased-Array Transceiver Supporting Cross-Polarization Leakage Self-Cancellation," *IEEE Symposium on VLSI Technology and Circuits (VLSI Technology and Circuits)*, Kyoto, Japan, pp. 1-2, Jun. 2021.

- Dongwon You, Yuta Takahashi, Shinji Takeda, Motoki Moritani, Haruki Hagiwara, Shuhei Koike, Hojun Lee, Yun Wang, **Zheng Li**, Jian Pang, Atsushi Shirane, Hiraku Sakamoto, Kenichi Okada, "A Ka-band 16-element deployable active phased array transmitter for satellite communication," *IEEE MTT-S International Microwave Symposium (IMS)*, Atlanta, GA, pp. 799-802, Jun. 2021.

- Jian Pang, Xueting Luo, **Zheng Li**, Atsushi Shirane, Kenichi Okada, "A compact 37-40GHz CMOS switch-type phase shifter with fine-tuning stage achieving 0.4-dB RMS gain error," *IEEE International Conference on Integrated Circuits, Technologies and Applications (ICTA)*, Nanjing, China, pp. 80-81, Nov. 2020.

- Xi Fu, Yun Wang, **Zheng Li**, Atsushi Shirane, Kenichi Okada, "A 68-dB Isolation 1.0-dB Loss Compact CMOS SPDT RF Switch Utilizing Switched Resonance Network," *IEEE MTT-S International Microwave Symposium (IMS)*, Los Angeles, CA, pp. 1315-1318, Jun. 2020.

- Jian Pang, **Zheng Li**, Xueting Luo, Joshua Alvin, Rattanan Saengchan, Ashbir Aviat Fadila, Kiyoshi Yanagisawa, Yi Zhang, Zixin Chen, Zhongliang Huang, Xiaofan Gu, Rui Wu, Yun Wang, Dongwon You, Bangan Liu, Zheng Sun, Yucheng Zhang, Hongye Huang, Naoki Oshima, Keiichi Motoi, Shinichi Hori, Kazuaki Kunihiro, Tomoya Kaneko, Atsushi Shirane, Kenichi Okada, "A 28-GHz CMOS phased-array beamformer supporting dual-polarized MIMO with cross-polarization leakage cancellation," *IEEE Symposium on VLSI Technology and Circuits (VLSI Technology and Circuits)*, Honolulu, HI, pp. 1-2, Jun. 2020.

- Zheng Sun, Hanli Liu, Dingxin Xu, Hongye Huang, Bangan Liu, **Zheng Li**, Jian Pang, Teruki Someya, Atsushi Shirane, "A 78 fs RMS jitter injection-locked clock multiplier using transformer-based ultra-low-power VCO," *IEEE European Solid State Circuits Conference (ESSCIRC)*, Cracow, Polandna, pp. 101-104, Sep. 2019.

- Jian Pang, **Zheng Li**, Ryo Kubozoe, Xueting Luo, Rui Wu, Yun Wang, Dongwon You, Ashbir Aviat Fadila, Rattanan Saengchan, Takeshi Nakamura, Joshua Alvin, Daiki Matsumoto, Aravind Tharayil Narayanan, Bangan Liu, Junjun Qiu, Hanli Liu, Zheng Sun, Hongye Huang, Korkut Kaan Tokgoz, Keiichi Motoi, Naoki Oshima, Shinichi Hori, Kazuaki Kunihiro, Tomoya Kaneko, Atsushi Shirane, Kenichi Okada, "21.1 a 28GHz CMOS phased-array beamformer utilizing neutralized bidirectional technique supporting dual-polarized MIMO for 5G NR," *IEEE International Solid-State Circuits Conference (ISSCC)*, San Francisco, CA, pp. 344-346, Feb. 2019.

- Jian Pang, Ryo Kubozoe, **Zheng Li**, Masaru Kawabuchi, Kenichi Okada, "A 28GHz CMOS phase shifter supporting 11.2 Gbs in 256QAM with an RMS gain error of 0.13 dB for 5G mobile network," *European Microwave Conference (EuMC*, Madrid, Spain, pp. 807-810, Sep. 2018.