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論 文 要 旨

THESIS SUMMARY

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要旨（英文 800 語程度）
Thesis Summary（approx.800 English Words ）

This thesis introduces the millimeter-wave CMOS phased-array beamformer designs for the low-cost and high-data-rate fifth-generation (5G) and next-generation wireless communication networks. The 5G cellular network technical background and existing solutions are discussed at the beginning. Several novel building blocks and system architectures are proposed aiming at the challenges of millimeter-wave phased-array designs. Detailed analysis and design methodology are demonstrated in the following chapters. In this thesis, the proposed beamformers realize high area efficiency and power efficiency, which can be good candidates for the 5G new radio (NR) applications and are also feasible for the next generation.

The operation frequency extension to millimeter-wave bands not only brings in huge bandwidth resources but also results in new design challenges. The extremely increased free-space path loss (FSPL) requires sufficient effective isotropic radiated power (EIRP) from base stations. The large-scale phased-array is mandatory to maintain the communication link budget. The array size can be traded off with the single transmitter (TX)-element output power to realize a given EIRP. Moreover, high-order modulation and high peak-to-average power ratio (PAPR) 5G-standard orthogonal frequency division multiple access (OFDMA)-mode signals put up with a stringent requirement for the power back-off and beamformer linearity. The design of low-cost beamformers is becoming an increasingly important research topic.

The high-performance neutralized bi-directional circuits are proposed and optimized to significantly narrow the beamformer die area and lower the manufacturing cost. A novel bi-directional Doherty PA-LNA is proposed to enhance the TX power back-off (PBO) efficiency, which retains the merit of bi-directional operation with minimized die area penalty. The wafer level chip scale package (WLCSP) co-design is implemented with less packaging insertion loss for better power efficiency. The bi-directional Doherty PA-LNA realizes 18.9-dBm saturated output power and 17.8% PAE at 6-dB PBO in PA mode. The proposed Doherty PA-LNA outperforms the two-way power-combined class-AB PA by achieving approximately 1.8 times higher PAE at a 6-dB PBO region. Additionally, the Doherty PA-LNA occupies only 66.7% of the equivalent area in PA mode, making it a more efficient and area-saving option. The area-efficient bi-directional phase shifters are also proposed with 360° phase coverage. The measured rms phase and rms gain errors are less than 2° and 1.1dB, respectively.

The dual-polarized multiple-input-multiple-output (DP-MIMO) configuration is able to increase the spectrum efficiency, thus improving the data rate. While, the cross-polarization leakage from the chip side, antenna side, and polarization rotation degrade the achievable DP-MIMO error vector magnitude (EVM) and power efficiency. The cross-polarization leakage cancellation is proposed and demonstrated within a 28-GHz phased-array beamformer. Over 40-dB cross-polarization isolation is achieved with rotation between TX and receiver (RX). Around 7-dB EVM improvement is obtained in DP-MIMO with the cross-polarization leakage cancellation. Based on the 400-MHz 5G signals, 2×2 DP-MIMO communication in 256QAM can be supported with 3.3% EVM. Besides, the background cancellation is supported by reusing the calibration block, no other measurement equipment is required.

As an effective approach to improving the system linearity and power efficiency, the digital pre-distortion (DPD) technique is widely utilized in sub-6GHz communications. As for the hybrid phased-array systems, the shared-LUT is desired to simplify the baseband complexity. The nonlinearity improvement is limited due to the different characteristics of the different beamformer elements. This inter-element mismatch is even enlarged with the Doherty technique. To address this issue, an inter-element mismatch compensation

technique is utilized to improve the phased-array DPD performance. Since the class-C biased Doherty auxiliary PA path is sensitive to the process, voltage and temperature (PVT) variations, additional threshold voltage compensation is required. The proposed inter-element mismatch compensation technique is performed with the cooperation of built-in threshold voltage detection and the accurate on-chip gain/phase calibration block. Thanks to the proposed inter-element mismatch compensation technique, the AM-AM and AM-PM characteristics are minimized between different elements over PVT variations, which enhances EVM and adjacent channel leakage ratio (ACLR) characteristics. The measured 64-QAM OFDMA-mode EVM and ACLR with the shared-LUT DPD are improved from -22.4dB to -25.0dB and from -28.7dBc to -32.1dBc, respectively.

The proposed polarization correction and inter-element mismatch compensation improve system EVM, resulting in better power efficiency. In 64-to-4-element TX-to-RX communication, the 64-element module achieves a 55.2-dBm saturated EIRP and also supports 21-Gb/s single-carrier data streaming at 43.2dBm. Compared with the recently reported state-of-art 5G phased-array beamformers, this work realizes the best area efficiency with reasonable power efficiency at a higher output power level.

To draw a conclusion, this thesis introduces novel techniques to enhance the area efficiency and power efficiency for 5G and next-generation applications. The high-performance phased-array beamformer design featured in low-cost high-data-rate could be realized based on the standard 65-nm CMOS technology. The outlook for future work and possible improvements of beyond-5G communications are also briefly discussed at the end of the thesis.