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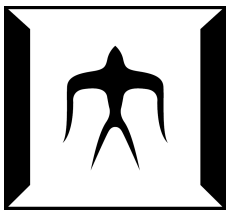
Doctoral Thesis

Study on 1060nm VCSEL arrays for co-packaged optics

By

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July 2023



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Chapter 1 Introduction

In this thesis, a 1060nm VCSEL array for co-packaged optics is proposed and demonstrated. Compared with previous research of VCSELs for optical communication system, the longer operation wavelength and single-mode operation gives the potential for a middle- and long-distance optical transmission with high modulation speed. It provides a new choice of optical resource for the optical transceivers in the next-generation communication system as high speed, high density, low power consumption and low cost. In this chapter, the development of optical module and co-packaged optics will be introduced. Then, the history of VCSEL and the development of VCSELs with different wavelengths will be shown. Finally, the research purpose of this study and the organization of this thesis will be discussed.

1.1 Background

With the explosive growth of global mobile data traffic [1] shown in Fig. 1.1.1, traditional mobile communication technologies are unable to meet the growing bandwidth demands. To address this issue, researchers are developing next-generation wireless communication technologies that go beyond 5G and 6G. These technologies will provide higher data transmission speeds, lower latency, and increased connection density to support more devices and applications.

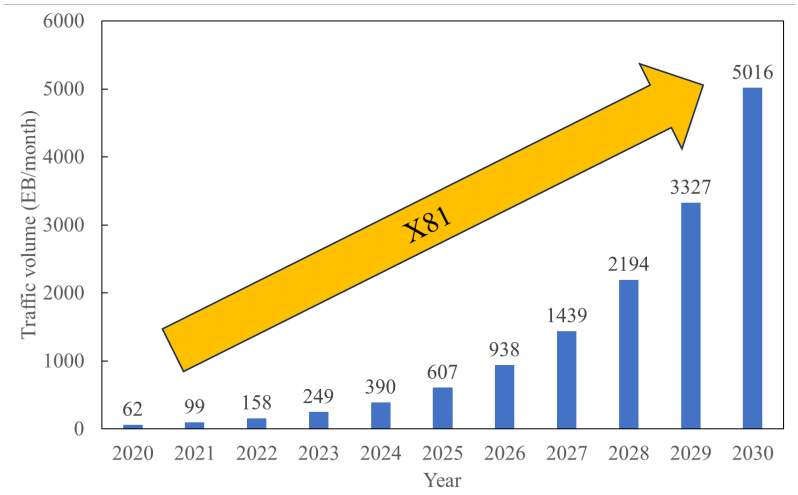


Fig. 1.1.1 The predicted growth of global mobile connectivity during 2020-2030

In order to support these advanced wireless communication technologies, the roles of data centers and edge computing networks are becoming increasingly important. Data centers provide the necessary computational power and storage space to process large amounts of data, while edge computing networks move data processing tasks to the network's edge, reducing data transfer latency and improving application performance.

Although the development of data centers and edge computing networks has supported advancements in wireless communication technologies, traditional pluggable modules still have limitations when facing high-speed, high-capacity data streams. Factors such as power consumption, size, and cost can pose obstacles to further increasing bandwidth density.

To overcome these challenges, researchers have begun exploring new optical interconnect technologies, such as co-packaged optics. Co-packaged optics is a novel optical interconnect technology that integrates optical modules with electronic chips in the same package, enabling higher bandwidth density and lower power consumption.

1.2 Development of optical module

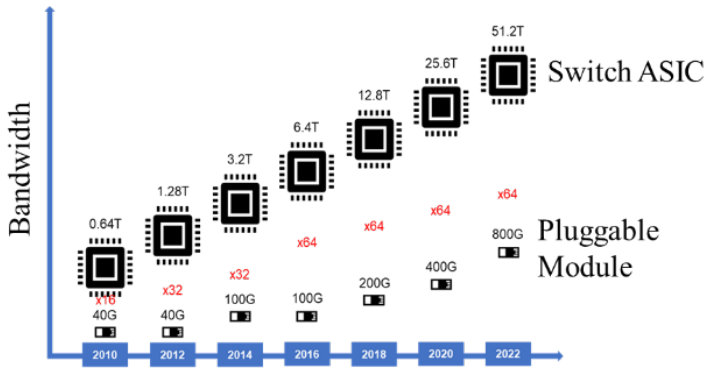


Fig. 1.2.1 Growth gap between the bandwidth of Switch ASIC and pluggable module

For the data center and edge computing networks to accommodate such massive data transmission, the development of existing electronic and optical devices is necessary. The

development of Switch ASICs (Application-specific integrated circuit) has continued to adhere to Moore's Law until 2022. From 0.64T in 2010 to 51.2T in 2022 [2], the speed of Switch ASICs has increased 64-fold over a span of 12 years, equivalent to 2^6. However, the development of optical devices has significantly lagged behind electronic devices, creating a gap known as the "Growth Gap".

From the Fig. 1.2.1, it can be observed that for the currently adopted pluggable optical modules in the market, in 2010, only 16 pluggable modules were required to meet the optoelectronic interconnection requirements. However, by 2022, even with the introduction of the 800G pluggable module by Cisco [3], 64 interface slots still need to be reserved on the rack to fulfill the optoelectronic interconnection needs. Considering the actual size of the rack, this often requires stacking two racks together for deployment, which is highly unfavorable for reducing the overall size of the servers. Furthermore, even at present, when the market is still widely using 400G pluggable modules, the number of interfaces would reach a staggering 128, which is unacceptable under any circumstances.

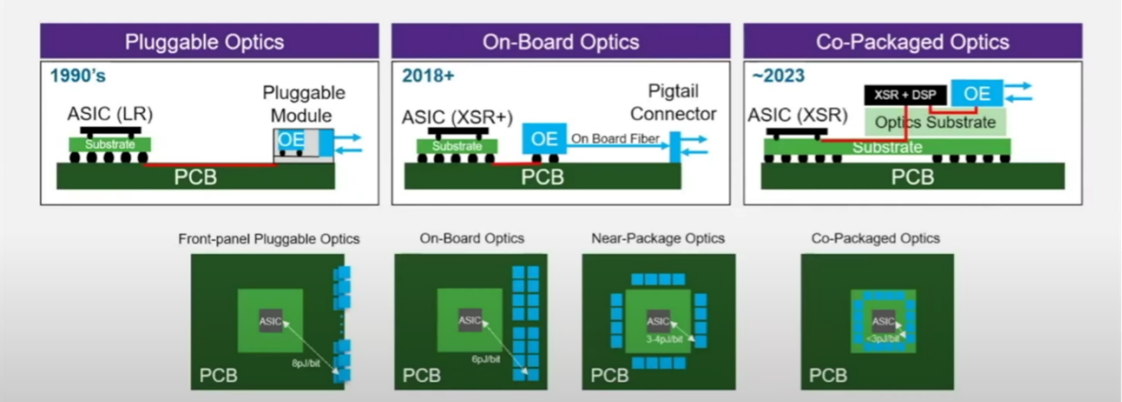


Fig. 1.2.2 Evolving toward co-packaged optics [4]

Therefore, after nearly 30 years of development in pluggable optics, on-board optics and co-packaged optics have been proposed. These two technologies are expected to replace pluggable

optics and have gained wide attention in the industry. The schematic diagrams of these three types of optical transceivers are shown in Fig. 1.2.2.

For traditional pluggable modules, the electrical signals generated by the ASIC are transmitted to the edge through copper wires laid on the PCB board, where they are optically interconnected with the pluggable optical transceivers. There are many advantages to this approach. For example, the number of pluggable modules can be adapted according to the capacity of the switch ASIC. The failure rate of optical components is highest in the entire system, so using pluggable modules makes it convenient to replace damaged components. The fixed positions of the optical fibers and lasers can improve overall coupling efficiency.

However, the drawbacks of pluggable modules are also evident. In addition to the size issue mentioned earlier, which becomes more severe with the "Growth Gap," there are power and thermal issues associated with pluggable modules that have pushed the power consumption and heat dissipation capacity of data centers relying on them to their limits. Moreover, high-frequency electrical signals transmitted through copper wires can cause signal degradation and loss, necessitating the use of retimers to compensate for the signals. This results in additional power consumption, signal delay, and affects signal quality.

On-board optics, in the context of optoelectronic interconnects, refers to the integration and packaging of optical transceivers on the PCB board based on silicon photonics technology. By integrating the transceivers on the PCB, the transmission distance of electrical signals on copper wires is reduced. After being converted into optical signals by the transceivers, they are connected to the external components through optical fibers. Compared to pluggable modules, on-board optics reduces the transmission losses of electrical signals, lowers costs, and improves transmission speeds.

However, because the optical transceivers are integrated and packaged on the PCB, it requires additional space on the PCB for their accommodation, leading to increased PCB size and cost.

For on-board optics, signal compensation and optimization still require the use of DSP (Digital Signal Processing) and CDR (Clock and Data Recovery), which can be detrimental to power consumption reduction. Moreover, once the integrated optical transceivers encounter issues, they are challenging to replace, and the heat generated by the optical components poses thermal management challenges for the PCB. Additionally, when the optical signals within the transceivers need to be coupled with optical fibers for transmission to external interfaces, a second coupling with the fibers is required, which reduces the overall coupling efficiency of the system.

In summary, the research on on-board optics requires a balance between benefits and trade-offs, particularly considering the cost involved in replacing well-established pluggable modules. In light of these considerations, further advancements in co-packaged optics have been proposed.

In 2019, Microsoft and Facebook, two companies with massive data center infrastructures, collaborated and proposed co-packaged optics (CPO) as a potential replacement for pluggable modules in data centers and edge computing networks. Unlike pluggable modules, where the optical transceivers are external to the switch ASIC module, and on-board optics, where the transceivers are integrated on the PCB, co-packaged optics suggests directly integrating the transceivers (referred to as optical engines by some researchers) within the packaging of the switch ASIC. This integration reduces the electrical distance between the CPO device and the ASIC to centimeters or even millimeters, minimizing the losses associated with high-frequency signal transmission. In such proximity, the need for DSP and CDR can be eliminated, resulting in significant power consumption reduction.

Although CPO also faces challenges such as replacement difficulties and thermal management, the reduction in power consumption and size makes CPO highly attractive. With the increasing speed of switch ASICs, CPO is expected to gain an advantage over pluggable modules in terms of competition, thanks to its energy efficiency and compact form factor.

1.3 Research on co-packaged optics

In the research on co-packaged optics (CPO), one of the key debates revolves around whether the optical source should be external or internal. Using an external laser source (ELS) can effectively address thermal issues. The laser source, as the highest heat-generating component in optical devices, is also the most affected by heat. It is connected to the rack's external interface, similar to pluggable modules. The optical signals generated by the laser source are transmitted through optical fibers to the tightly packaged optical engines integrated with the ASIC. The electrical signals are converted into optical signals through external modulation, and then the optical signals are transmitted through optical fibers to the external interfaces.

By using this approach, the laser source can be placed away from the ASIC, which generates a high amount of heat, thus improving thermal management. The laser source only needs to provide high-power light, and the light can simultaneously serve multiple external modulators after fan-in and fan-out. Moreover, in case of issues, the laser source can be easily replaced.

However, this method undoubtedly results in a large number of optical fibers that need to be connected to the optical engines, which increases the challenges of system coupling and integration.

Using an integrated light source involves packaging the light source together with other optical components within the switch ASIC. While thermal issues may arise from the stacking of components, they can be addressed through optimized thermal management systems. The stability of the device can also be improved by incorporating backup components.

The advantage of this approach is that optical component coupling and alignment can be performed during the wafer bonding stage. Additionally, only the optical signal needs to be transmitted through the optical fibers of the optical engine, resulting in improved coupling efficiency, reduced integration challenges, and increased integration density.

1.3.1 Facebook

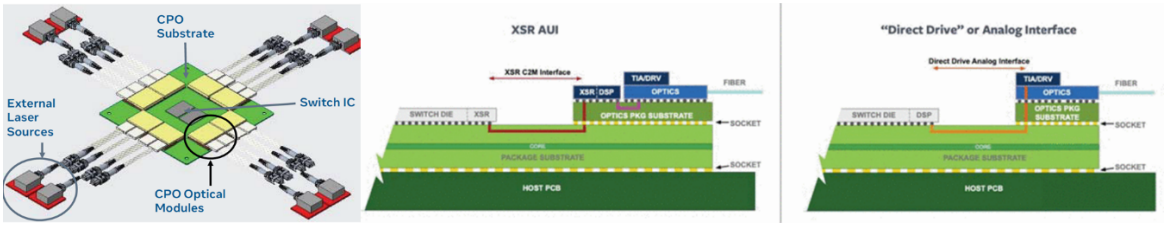


Fig. 1.3.1 Schematic of CPO proposed by Facebook [5]

Fig. 1.3.1 depicts an example of a co-packaged optics (CPO) subassembly provided by Facebook [5]. The CPO transceiver module, which includes a transmitter and receiver array connected by optical fiber pigtails, is shown mounted on sockets around the switch package substrate. The option to use an unmodulated external laser source (ELS) as the optical input for the CPO module is available. The decision to use ELS instead of an on-chip laser source depends on several factors, including the anticipated operating temperature, projected laser reliability, and whether the silicon photonics (SiPh) process technology includes provisions for the integration of III/V materials.

Fig. 1.3.1 displays cross-sectional diagrams of two possible optical interface architecture switching options. The optical links are driven by a DSP-based SerDes integrated within the CPO module. This re-timing architecture follows current industry practices for functional partitioning at 25, 50, and 100 Gb/s, with each channel switching to an Optical Front Panel Pluggable (FPP) interface, providing robustness and the advantages of well-defined and easily understood interface definitions for interoperability between different subcomponents. The right side of the diagram illustrates another further rationalized approach. Here, a combined electrical and optical link is directly "end-to-end" driven by analog channels from the DSP located inside the switch chip. The benefits of this approach include reduced component count and lower power consumption due to the elimination of dedicated optical SerDes interfaces for switching. However, while providing

additional energy-saving benefits compared to re-timing or "AUI" methods, the direct-drive approach also faces challenges in terms of interoperability and robustness.

Facebook's developed CPO devices utilize an external laser source. While optimizations have been made to integrate the DSP onto the ASIC to separate the electrical and optical components, thus further reducing power consumption, the use of DSP still contributes to power consumption.

1.3.2 Intel

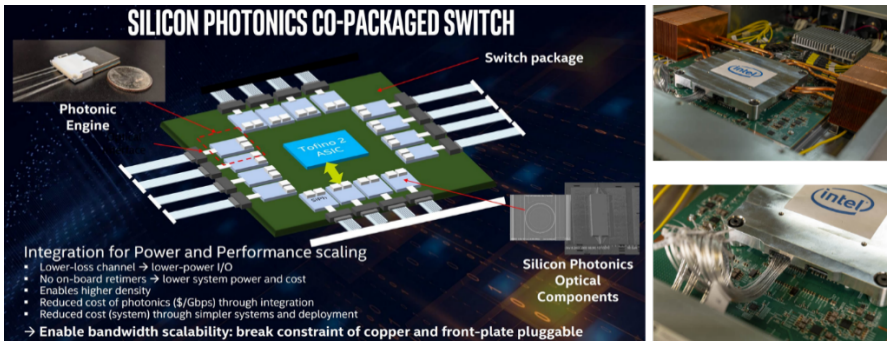


Fig. 1.3.2 CPO module proposed by Intel [6]

In 2020, Intel showcased for the first time in the industry a 12.8Tbps Switch Asic device based on CPO. To support the 12.8Tbps transmission speed, Intel integrated eight optical engines around the ASIC chip, with each engine providing a capacity of 1.6Tbps [7] supported by a built-in laser array consisting of 16 channels, where each channel delivers a transmission speed of 100Gbps. The size of each optical engine is only 25mm by 22mm. The device exhibits a power consumption of merely 19.2pJ/bit, which is one-third lower compared to pluggable modules at 30pJ/bit. It is expected that the power consumption of the next-generation devices can be further reduced to 5pJ/bit. Each optical engine encompasses two sets of optical transceivers, two sets of CDR (Clock and Data Recovery), and two sets of power management. Each set of optical transceivers offers a speed of 2x400G.

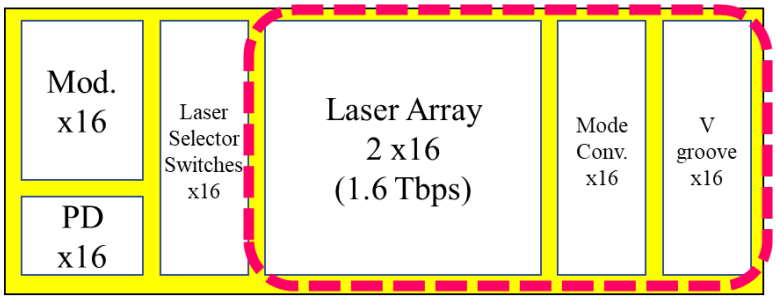


Fig. 1.3.3 Schematic of CPO transceiver of Intel

The Fig. 1.3.3 illustrates the components integrated within each optical engine. The laser array consists of two sets of 16-channel DFB (Distributed Feedback) arrays, employing hybrid integration to reduce system failure rates. The lasers are selected through a 16-channel optical switch with an MZ (Mach-Zehnder) structure and then externally modulated by a 16-channel silicon micro-ring modulator. Due to the limitations of the optical spot shape from the DFB lasers, a 16-channel mode size converter is integrated to achieve mode matching between the lasers and the optical fibers. Finally, a set of V-grooves is integrated to secure the optical fibers and improve coupling efficiency.

Intel chose to adopt integrated on-chip lasers in their CPO devices and improved device stability by growing backup lasers. By reducing the transmission distance of electrical signals, the need for on-board retimers and DSP is eliminated, resulting in significant power consumption reduction. The coupling alignment with optical fibers is greatly enhanced, and the number of optical fibers is reduced, as shown in the diagram. Intel employed copper tubes for heat dissipation of the optical engines to address thermal management concerns.

1.3.3 Broadcom

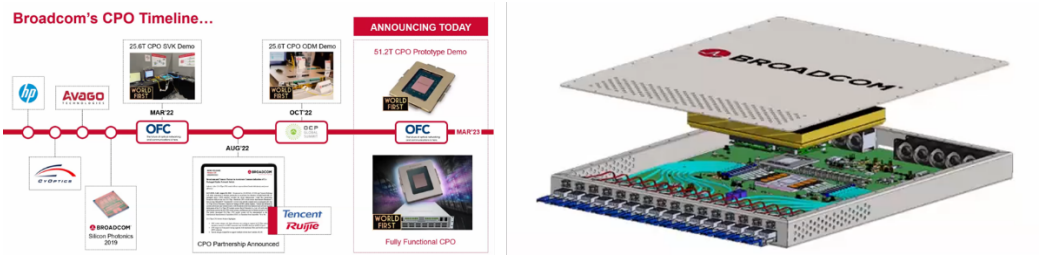


Fig. 1.3.4 Timeline of Broadcom CPO and 51.2T Remote Laser Modules [8]

In 2023, Broadcom showcased the world's first commercially available 25.6Tbps CPO-based switch ASIC and the first 51.2Tbps demo. The Broadcom 25.6Tbps CPO switch is assembled with half of the CPO devices to support a switching speed of 12.8Tbps. It utilizes an external laser source and is supported by four CPO optical engine modules. Each CPO optical engine module has a capacity of 3.2Tbps, with 32 channels per engine, and each channel supports 106G PAM4. Considering only the CPO components, the total power consumption for the 128 channels is 102W, and when considering all power consumption, the power-to-speed ratio is 8pJ/bit.

The 51.2Tbps CPO switch from Broadcom is powered by eight 6.4Tbps CPO optical engines, providing the full switching speed. Each optical engine consists of 64 channels, and the power consumption is reduced to 6.8pJ/bit.

To mitigate the additional coupling losses introduced by the external laser source, a non-contact lens-based beam expansion coupling technique is employed. This approach reduces end-face contact stress, minimizes frictional forces, mitigates air reflections, and enhances coupling efficiency. By utilizing non-contact lens-based beam expansion, the coupling losses associated with the external laser source can be minimized, resulting in improved overall coupling efficiency.

1.3.4 IBM

IBM's research team has been studying VCSELs for several decades and has applied them in CPO

(Chip-to-Package Optical) devices. IBM has focused on the research of multimode VCSELs, and as early as 1993, they demonstrated 3 Gbps transmission using multimode VCSELs in short fiber links[9]. In 2003, IBM began discussing the requirements and demands of optical interconnects in the next-generation servers [10]. Finally, in 2019, IBM collaborated with Finisar to propose the MOTION project, which stands for Multi-Wavelength Optical Transceivers Integrated On Node [11]. The project aimed to develop chip-level optical modules based on VCSELs for CPO, which was still a new concept at that time. The key characteristic of VCSEL-based CPO, specifically the CPO Otx, is its extremely low energy consumption per bit. At the OFC conference in 2023, IBM presented the development and characteristics of MOTION in its two phases shown in Fig. 1.3.5 [12][13].

Parameter	**MOTION Phase 1**	**MOTION Phase 2**
Electrical Interface	16 channels @ 56G NRZ	32 channels @ 112G PAM4
IC Technology	SiGe	CMOS
Optical Interface	16 channels @ 56 G NRZ	32 channels @ 112G PAM4
# of Wavelengths	1: 850nm	2: 850nm, 910nm
# of Fibers	16 Tx + 16 Rx	16 Tx + 16 Rx
Fiber Type	50/125 MMF	50/125 MMF
Supported Distance	30m	30m
Package I/O Pitch	400um	300um
Glass Carrier Size	13x13mm	13x13mm
Energy consumption	4 pJ/bit	2 pJ/bit
Laminate interface	Soldered or LGA	Soldered or LGA

Fig. 1.3.5 Comparison of Specification between MOTION Phase 1 and 2

The MOTION project continues to target short-distance optical links of less than 100 meters. In the first phase, they developed a 900 Gbps transceiver capable of transmitting and receiving 56 Gbps NRZ signals using a 16-channel VCSEL. The energy consumption was reduced to 4 pJ/bit, supporting 30-meter short-distance transmission. In their second phase, the goal is to double the data rate while halving the energy consumption.

1.3.5 CPO in Japan

The National Institute of Information and Communications Technology (NICT) in Japan has funded a research project called B5G (Beyond 5G). The project aims to create a 400G co-packaging technology with 16 channels operating at 25G speed, consuming less than 5W of power, and with a size smaller than 10 mm². Two companies, Furukawa and Fujitsu, are involved in this project.

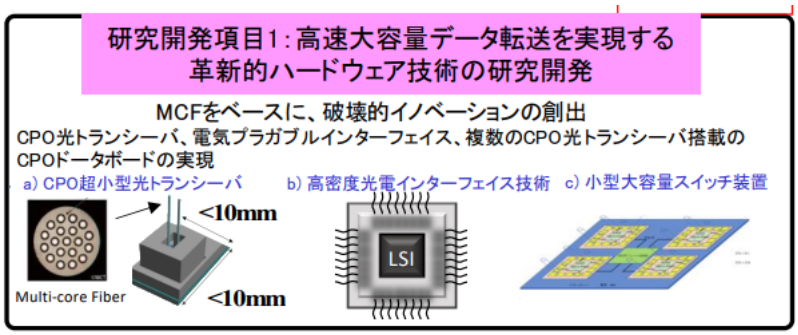


Fig.1.3.6 The research target of B5G [14]

Furukawa has developed an eight-channel transceiver using a 1060nm VCSEL for single-wavelength 56Gbps PAM4 transmission [15]. The VCSEL includes a linear array with top-emitting functionality. The overall package size is 15.9 x 7.7mm², which includes a hexagonal arrangement of 231 solder pads with a 0.3mm pitch. The transceiver operates at a 56Gbps PAM4 data rate with a bit error rate (BER) lower than 10^-12 over multimode fiber spans exceeding 4.4m.

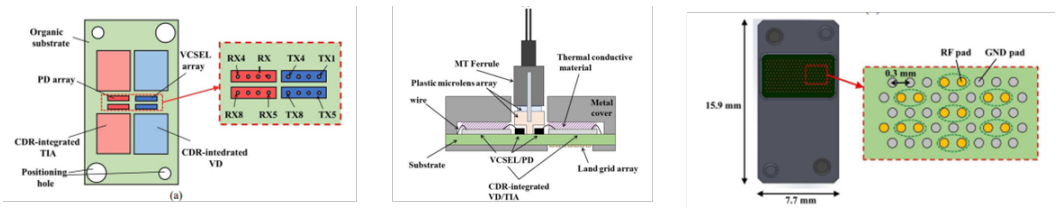


Fig.1.3.7 Schematic illustrations for the 56-Gb/s PAM-4 8-channel transceiver of top view,

cross-sectional view and bottom view and pads layout [15]

Fujitsu has developed a 16-channel 25Gb/s NRZ transceiver using 16 bottom-emitting VCSELs at a wavelength of 1060nm [16], arranged in a hexagonal pattern with a pitch of 40um to match the cores of a 16-core multimode fiber. The optical engine size is 7 x 10mm², mounted within a package of 7.8 x 16mm², featuring 231 solder pads, a 0.3mm pitch, and a hexagonal LGA interface.

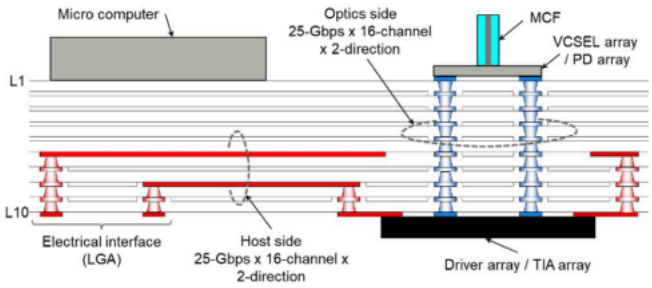


Fig.1.3.8 Cross section view of ultra-compact CPO transceiver module [16]

1.4 VCSEL

VCSELs are a dominant high-quality laser light source for numerous optical systems and applications. VCSELs have a variety of advantages such as low operating current densities, low power dissipation, high efficiency, cost-effective fabrication and testing, on-chip testability, array fabrication and effective fibers coupling [17].

The initial structure of VCSEL was proposed by Professor Kenichi Iga from Tokyo Institute of Technology in 1977, as shown in Fig. 1.4.1 [18] [19]. Two years later, the first VCSEL device appeared, which was fabricated using the liquid-phase epitaxy (LPE) technique and employed GaInAsP/InP materials. The device operated at a wavelength of 1300nm, with a lasing temperature of 77K and a threshold current of approximately 900mA [20].

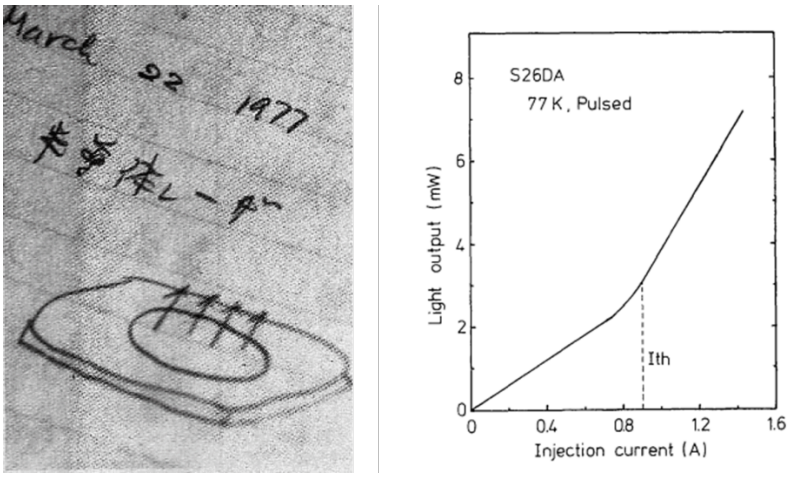


Fig. 1.4.1 Sketch of the VCSEL [19] and IL of pulsed VCSEL [20]

In 1988, Professor Fumio Koyama developed GaAs-based VCSELs with lower threshold currents and successfully achieved continuous-wave lasing under room temperature conditions. The device operated at a wavelength of 850 nm, with a lasing temperature of 22.5°C and a threshold current of 32mA [21][22].

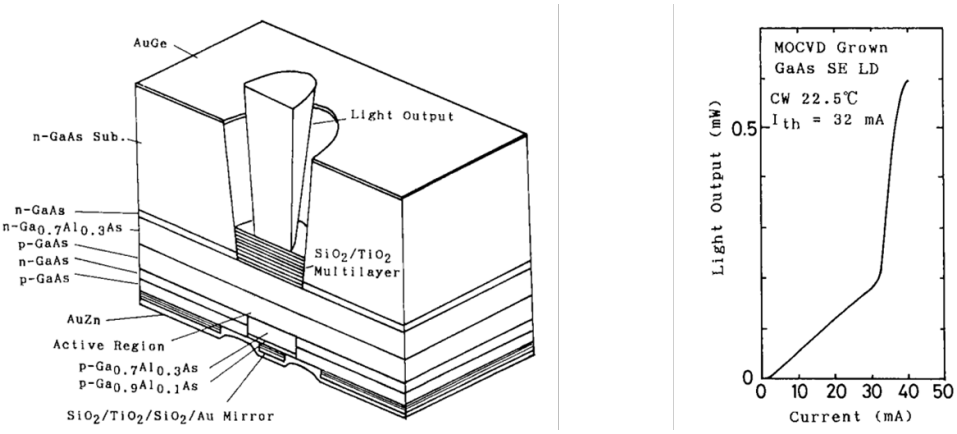


Fig. 1.4.2 Schematic structure of VCSEL worked at CW and IL under room temperature [21]

The VCSEL structure consists primarily of three components: the top p-type distributed Bragg reflector (DBR), the active layer, and the bottom n-type DBR. The resonant cavity of a VCSEL is

typically very thin. To achieve laser output, the top and bottom DBRs must provide a reflectivity over 99% to ensure multiple reflections of light within the resonant cavity, thereby enhancing the gain. To achieve high reflectivity, multiple layers of semiconductor DBRs are constructed during the epitaxial growth process. However, increasing the number of DBR layers also increases the series resistance of the device.

The increase in series resistance leads to the generation of heat when current passes through the device, resulting in an elevated temperature in the active region. The elevated temperature adversely affects the optoelectronic performance of the device, such as reducing efficiency and increasing the threshold current. Therefore, when designing a VCSEL, careful parameter matching of each structure is required to achieve low resistance and low threshold current emission. This includes optimizing the number and thickness of the DBR layers, as well as selecting suitable materials and structures to minimize series resistance and improve device performance.

In Table 1.4.1, the materials of active layer for VCSELs at different wavelengths and the applications are shown.

Table 1.4.1 The materials of active layer for VCSELs at different wavelengths and the applications

Wavelength	Active layer	Application
670 nm	AlGaInP/AlGaAs [23]	biomedical imaging, phototherapy applications, precision measurement, positioning systems, facial recognition, gesture control, eye-tracking, and optical sensing in handheld devices
850nm	AlGaAs/GaAs	short-range data communication

	InGaAs/GaAs	applications, sensing and imaging applications
1060nm	InGaAs/GaAs	long-reach and high-speed optical communication systems, industrial sensing and metrology applications, biomedical imaging applications, material processing applications, LiDAR
1310nm	GaInNAs/GaAs	efficient and long-distance data transmission with low dispersion and low noise, fiber optic sensing applications, fiber optic network testing and troubleshooting, LiDAR,
1550nm	InAlGaAs/InP	long-haul and high-speed optical communication systems, fiber optic sensing applications, coherent optical communication systems

1.4.1 Limit of direct modulation

VCSELs employ direct modulation, which means that, similar to DFB (Distributed Feedback) lasers that use direct modulation, the modulation bandwidth of VCSELs is limited by direct modulation.

Here the limitation of carrier-photon resonance (CPR) on modulation bandwidth was considered.

The rate equation of VCSEL was shown below:

$$\frac{dN}{dt} = \frac{\eta_i}{qV} I - \frac{N}{\tau} - v_g g N_p \quad \textbf{(1.1)}$$

$$\frac{dN_p}{dt} = \Gamma v_g g N_p - \frac{N}{\tau_p} + \Gamma R'_{sp} \quad \textbf{(1.2)}$$

Where N and Np is carrier and photon density. η_i **is the internal efficiency. I is the current, q is the charge of electronic, V is active region volume,** τ and τ_p **is the carrier and photon density,** v_g **is group velocity, g is gain of mode,** Γ is the confinement factor and R'_{sp} **is the spontaneous emission into the defined mode.**

From equation 1.1 and 1.2, relaxation oscillation frequency can be obtained as follow:

$$\omega_R^2 = \frac{g_0 N_{p0}}{\tau_p} \quad \textbf{(1.3)}$$

$$f_R = \frac{\omega_R}{2\pi} = \sqrt{\frac{g_0 \eta_i}{qV}(I - I_{th})} \quad \textbf{(1.4)}$$

Where N_{p0} **is the steady state solution of photon densities.**

At the same time, modulation bandwidth of VCSEL is limited by parasitics and thermal effects. The impact of thermal effects and parasitcis on the VCSEL modulation response is shown in Fig. 1.4.3. With a intrinsic response of 60GHz, a VCSEL effected by thermal effects and parasitics has a low modulation response of 30GHz [24].

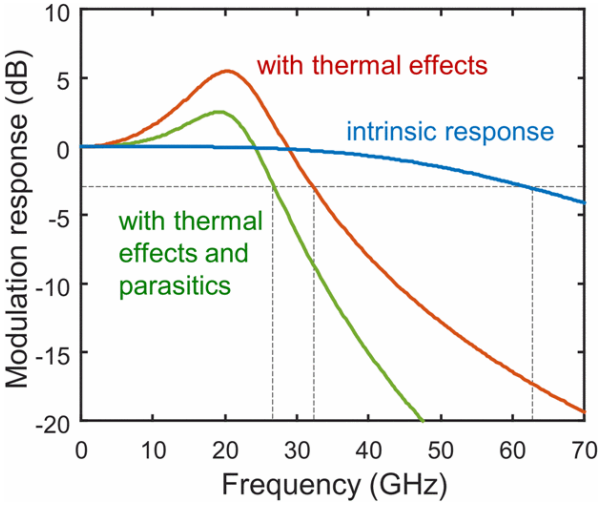


Fig. 1.4.3 Impact of thermal effects and parasitics on the VCSEL modulation response [24]

1.4.2 Photon-photon resonance

From equation 1.3 and 1.4, relaxation oscillation frequency can be increased by increasing the photon density. However, photon density in the cavity can not increase with no limitation.

Thus, photon-photon resonance (PPR) was proposed to enlarge relaxation oscillation frequency. For different resonance cavity, the beating between different modes will lead to PPR at a frequency higher than CPR. VCSELs with transverse coupled cavity (TCC) had been proved that can increase the bandwidth by PPR.

The modeling for the bandwidth enhancement of TCC VCSEL was carried out by the following Lang-Kobayashi rate equation [25][26]:

$$\frac{dN(t)}{dt} = -\Gamma G(t)S(t) - \frac{N(t)}{\tau_s} + \frac{J(t)}{dq} \quad \textbf{(1.5)}$$

$$\frac{dS(t)}{dt} = \left[\Gamma G(t) - \frac{1}{\tau_{ph}}\right] S(t) + 2K_c cos(\theta)\sqrt{S(t)S(t-\tau)} \quad \textbf{(1.6)}$$

Where G(t) is the gain of material, τ_{ph} **is the lifetime of carrier,** Γ is the confinement factor, θ is the relative phase of lateral feedback light, J(t) is the density of current, d is the thickness of active region, Kc is the coupling feedback coefficient and τ is the optical feedback delay time.

Small signal response can be obtained from equation 1.5 and 1.6 as follow:

$$H(\omega) = \frac{\Gamma\frac{dG}{dN}S_0\left(\frac{1}{\tau_{ph}}+2K_C cos(\theta)\right)}{\Gamma\frac{dG}{dN}S_0\left(\frac{1}{\tau_{ph}}+2K_C cos(\theta)\right)+\left(j\omega+\frac{1}{\tau_s}+\Gamma\frac{dG}{dN}S_0\right)*[j\omega+K_C cos(\theta)*\left(1-e^{-i\omega\tau}\right)+\epsilon\Gamma S_0\left(\frac{1}{\tau_{ph}}+2K_C cos(\theta)\right)]}$$

(1.7)

The small signal response is determined by delay time τ, the coupling feedback coefficient Kc and the relative phase of lateral feedback light θ.

1.4.3 TCC VCSEL

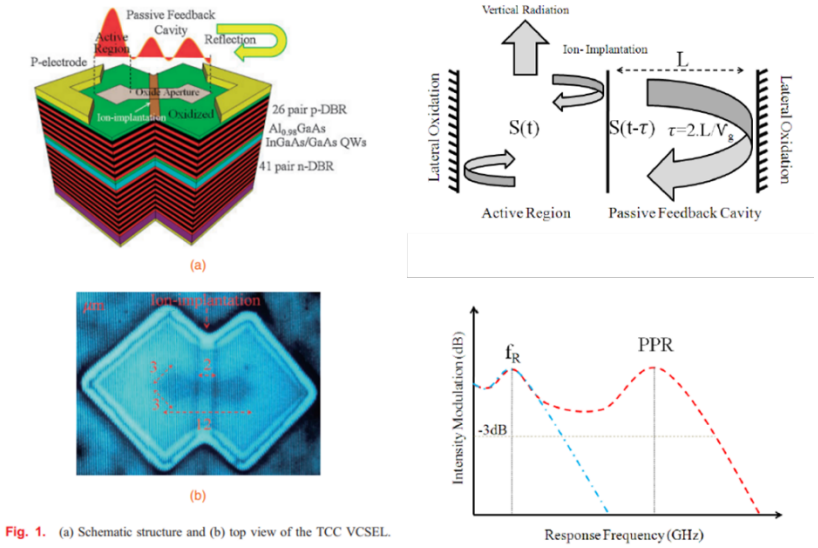


Fig. 1. (a) Schematic structure and (b) top view of the TCC VCSEL.

Fig. 1.4.4 Schematic of TCC-VCSEL and mechanism of exploiting PPR based on TCC VCSEL and extended modulation bandwidth obtained by applying PPR effects [28]

In 2013, VCSEL with a transverse coupled cavity (TCC) was proposed for bandwidth enhancement [27]. TCC VCSEL worked at 980 nm with InGaAs/GaAs quantum wells. In order to form transverse coupled cavity structures, bow-tie shaped mesas were formed by dry-etching process and followed by wet-oxidation process. Proton implantation was carried out for the electrical isolation between the top two p-electrodes of the VCSEL and the feedback cavity. The transverse fields were reflected at the end interface and increase the lateral optical coupling into VCSEL. The typically 3-dB by applying PPR was shown in Fig. 1.4.4.

1.4.4 DTCC VCSEL

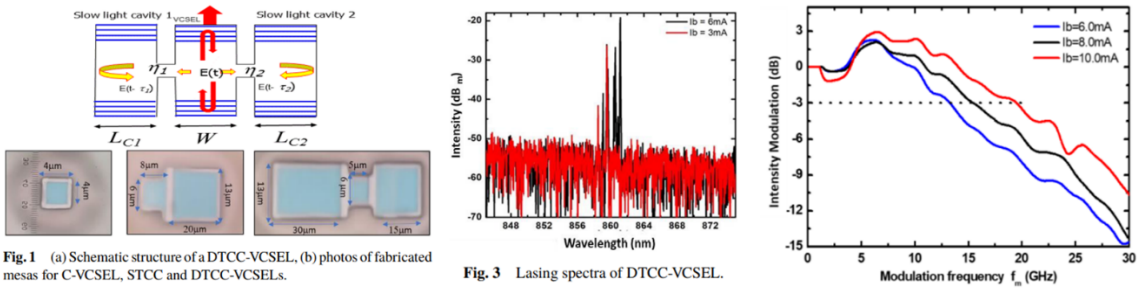


Fig. 1 (a) Schematic structure of a DTCC-VCSEL, (b) photos of fabricated mesas for C-VCSEL, STCC and DTCC-VCSELs.

Fig. 3 Lasing spectra of DTCC-VCSEL.

Fig. 1.4.5 Schematic of DTCC-VCSEL, lasing spectra and small signal response with different injection currents [29]

The schematic of DTCC-VCSEL was shown in Fig. 1.4.5. The VCSEL was coupled with two transverse coupled cavities through oxidation aperture. The mesa size was 50 μm*13 μm. The DTCC-VCSEL was fabricated at 850 nm-band. The small signal response was increased over 20GHz [29]. In 2019, single-mode DTCC-VCSEL with large oxide apertures was demonstrated due to Vernier effect [30].

1.4.5 Metal-aperture VCSEL

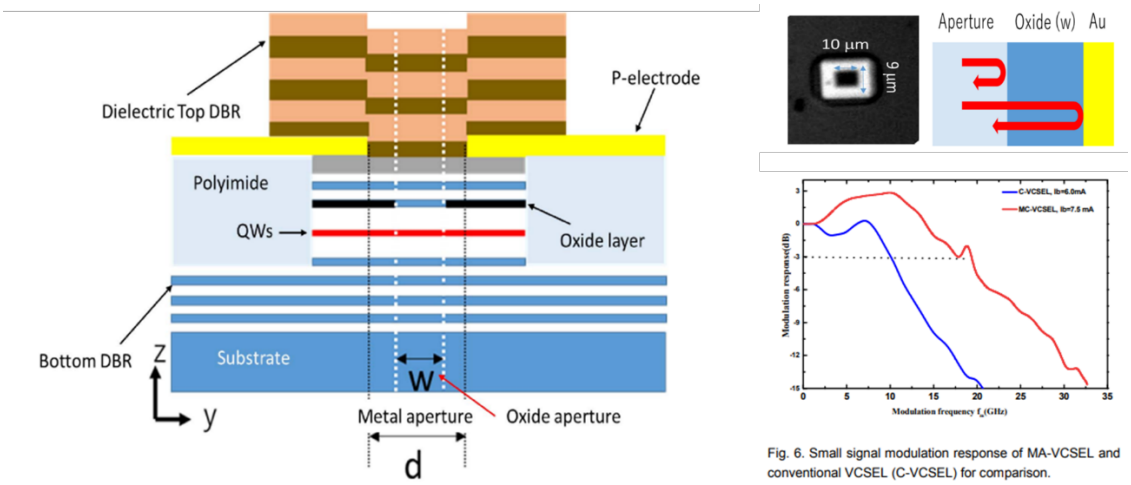


Fig. 6. Small signal modulation response of MA-VCSEL and conventional VCSEL (C-VCSEL) for comparison.

Fig. 1.4.6 Schematic of metal-aperture VCSEL, top view of oxidation aperture, schematic of transverse resonance and small signal response of MA-VCSEL

In 2020, a single-mode VCSEL with a large oxidation aperture was proposed[31]. The transverse coupled cavity was provided by the boundaries between oxidation aperture and contact metal. Compared with TCC and DTCC VCSELs with extra coupled cavity, the fabrication process of MA-VCSEL was as same as conventional VCSELs without any extra process. The bandwidth can be double thanks to the transverse couple cavity effect.

1.4.6 Double-ring Surface-relief VCSEL

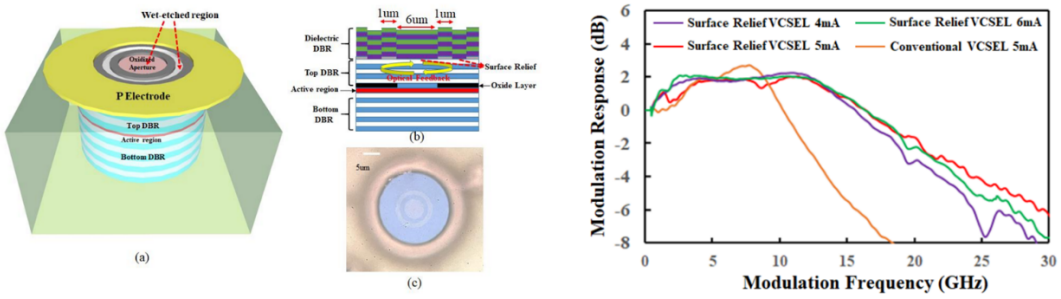


Fig. 1.4.7 Schematic and cross-sectional view of double-ring surface-relief VCSEL, top view of a surface relief and small signal response [32]

Double-ring surface-relief VCSEL was fabricated by a half VCSEL formed by 30 pairs bottom DBR, InGaAs quantum wells and 4 pairs top DBR. A wet etching to the surface left ring regions with a diameter of 6 μm and a 1 μm ring outside. The depth of surface relief was 20 nm. The oxidation aperture was 6 μm which was as same as center surface relief. The transverse resonance came from that shorter resonant wavelength at etched region can travel laterally into the oxidized region and reflects at the boundary of outside ring. The small signal response was double compared with conventional VCSEL on the same wafer.

1.5 Research purpose

Considering the problems in current optical transmission system, a 16-ch 1060nm bottom-emitting single-mode VCSEL array with transverse coupled cavity is an attractive laser source for CPO modules for high speed, high density, low power consumption, long distance. The purpose of this thesis is to develop the VCSEL array by:

- Designing and fabricating densely integrated 16-ch VCSEL array for a 400 Gbps transmission. Density is 2.5 Tbps/mm^2.
- Constructing measurement and evaluation system for bottom emitting VCSEL array.
- Fabricating transverse coupled cavity without increasing fabrication complexity. Realizing high bandwidth and single-mode operation for large oxidation aperture.
- Introducing surface relief for a better uniformity of single-mode operation for 16-ch VCSEL array.
- Reducing parasitic capacitance of mesa and electrode pads for a higher speed.
- Realizing high product of bit rate and fiber length.
- Completing coupling of multi-core fiber and flip-chip bonded VCSEL array.

1.6 Organization of the thesis

Chapter 1: The development of CPO and previous works on high speed VCSELs with transverse coupled cavity were introduced.

Chapter 2: The design of VCSEL arrays for applications in CPO was introduced. The arrangement, emitting type, wavelength choice, structure choice and the methods to improve the speed and single-mode uniformity of 16-ch VCSEL array were proposed. The package process and coupling with multi-core fiber were explained.

Chapter 3: The internal and optimized wafer-scale fabrication process of 16-ch VCSEL array were

introduced. The system for static characteristics measurement and the static characteristics of top emitting and bottom emitting 16-ch VCSEL array was demonstrated. The methods and experiment results for improvement on SMSR and its uniformity was proposed and demonstrated.

Chapter 4: The methods and experiment results on improving the high speed modulation characteristics were preposed and demonstrated. The improvement on small signal response and quality of 25Gbps NRZ eye pattern of 16-ch VCSEL array was shown. With pulse-compression in single-mode fiber transmission, a long-distance and high product of speed and transmission distance was demonstrated.

Chapter 5: The dicing and flip-chip bonding process for VCSEL arrays were explained. The calculation and experiment results for the direct coupling of VCSEL array and MCF was demonstrated.

Chapter 6: The prospective and potential of VCSEL array and its coupling with MCF will be discussed and the thesis will be concluded.

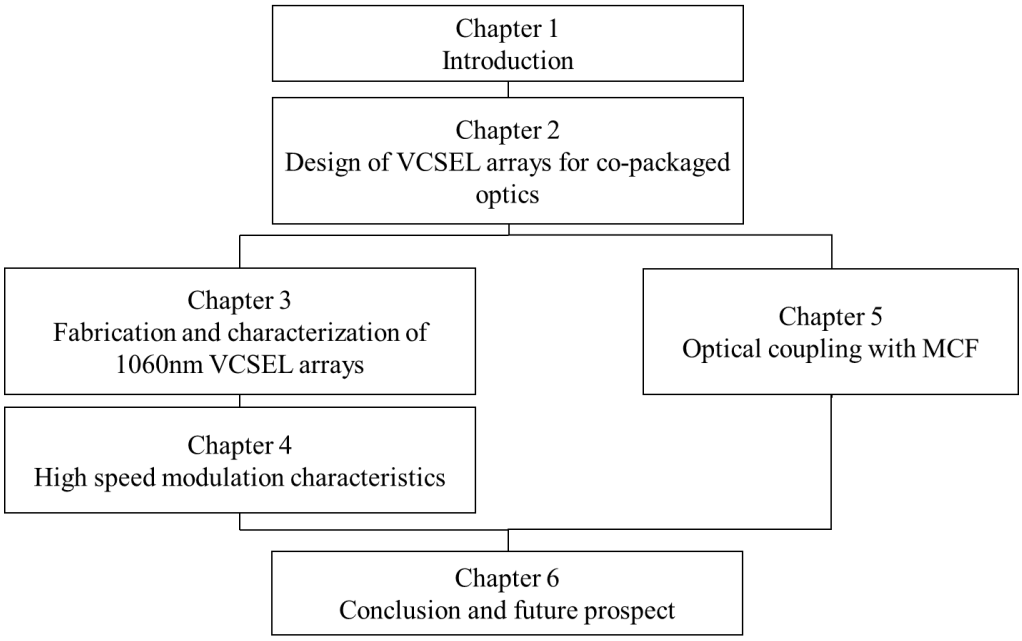


Fig. 1.6 Organization structure of the thesis

Chapter 2　Design of VCSEL arrays for co-packaged optics

2.1 Introduction

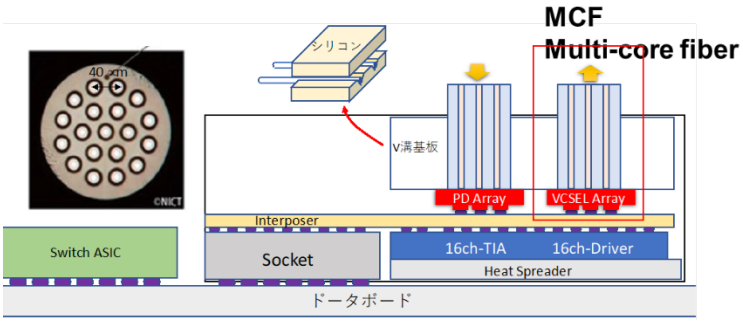


Fig. 2.1 Schematic of CPO module based on VCSEL array

The schematic of our proposed CPO module based on 16-ch VCSEL array is shown in Fig. 2.1. The optical transceiver is integrated near the Switch ASIC. The optical transceiver can be divided into two parts: PIC and EIC. PIC consists of 16-ch VCSEL array and 16-ch PD array. VCSEL array and PD array are integrated on interposer by flip-chip bonding process. Compared with wire bonding process, the parasitic caused by electric wire can be avoided and the speed characteristics of VCSEL array can be improved. EIC consists of 16-ch TIA (Transimpedance Amplifier) and 16-ch Driver. EIC and PIC are connected by interposer. As mentioned in Chapter 1, for CPO module with integrated laser source, heat caused by Switch ASIC and inside CPO will increase the risk of VCSEL. In this case, the optical transceiver is integrated with a heat spreader to lead the heat into PCB for a better thermal management. The VCSEL array is coupled with a 16-ch single-mode multi-core fiber. Compared with using 16 single-mode fibers, the transmission density per fiber is increased to 16 times. By reducing the amount of fiber, the integration of CPO module can be improved, and the coupling loss can be reduced. The multi-core fiber is fixed by a silicon V-groove for a better alignment and better coupling efficiency.

In this research, the target speed per channel for VCSEL array is 25 Gbps NRZ to realize a high-speed transmission of 400 Gbps per CPO module. By improving the performance of speed

characteristics, VCSELs with a speed of 50Gbps NRZ and 100 Gbps PAM-4 are expected. The speed of CPO module will reach to 800 Gbps and 1.6 Tbps.

2.2 Arrangement of VCSEL array

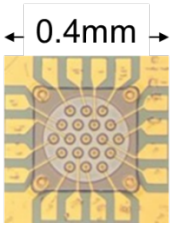


Fig. 2.2 Photo of 16-ch VCSEL array with electrodes

In Fig. 2.2, the photo of 16-ch VCSEL array with electrodes is shown. The minimum size for 16-ch VCSEL array with electrodes is 0.4 mm * 0.4 mm. As shown in the Fig. 2.2, the VCSEL array consists of 19 VCSELs. 3 VCSELs at the center are fabricated as back-up devices (In this design, these 3 VCSELs are not fabricated with electrodes). The other 16 VCSELs are fabricated with electrodes. The distance between adjacent channels is 40 μm. The distance is determined by the thermal crosstalk and stability. In two-dimensional space, a hexagonal lattice is the most common arrangement for circular closest packing, often referred to as a "honeycomb packing". In this case, the arrangement of VCSELs' position is based on hexagonal lattice. The p electrodes are individua and n electrodes are used in common. In this research, a high rate-density can be realized. For 25 Gbps per channel, rate-density of this VCSEL array is 2.5 Tbps/mm^2. In the case of 100 Gbps per channel, rate-density of this VCSEL array can be 10 Tbps/mm^2.

2.3 Top emitting and bottom emitting

VCSELs can achieve vertical emission, which allows for two types of light output. In one mode, the light passes through the active region and undergoes multiple reflections in the distributed Bragg reflector (DBR), eventually exiting through the top p-type DBR to achieve top-emitting. In the other mode, the light passes through the active region and undergoes multiple reflections in the DBR, then exits through the bottom n-type DBR and substrate to achieve bottom-emitting. Top emitting and bottom emitting VCSELs are both common choices in the application of high-speed transmission.

For top-emitting VCSELs, there are two common structures. The first structure involves fabricating only the p-electrode on the top surface of the device, while the n-electrode is directly deposited on the bottom surface of the substrate. The advantage of this approach is that it allows for ample space on the top for the design of the p-electrode. There is no need for wet etching on the top to form the n-contact, and directly depositing the electrode on the bottom surface simplifies the fabrication process. The n-electrode can also serve as a reflector to enhance the reflectivity of the bottom DBR, enabling top emission.

The second structure involves growing both the p-electrode and n-electrode on the top surface of the device. This arrangement places the p-electrode and n-electrode at the same height to reduce parasitic capacitance and improve the modulation speed of the VCSEL. However, the trade-off is that the top surface becomes more crowded, and a more complex production process is required.

The advantage of using top-emitting VCSELs is that the absorption of light by the substrate material does not need to be considered, allowing for the freedom to choose the substrate material according to specific requirements. However, the drawback is that both structures of top-emitting VCSELs require integration using the wire bonding process. It will bring worse

thermal management, complex packaging and integration process and high-speed signal degradation.

The structure of a bottom emitting VCSEL was shown in Fig. 2.3. The p-electrode and n-electrode are grown on the top surface of the mesa structure, maintaining the same height to reduce parasitic capacitance. Light is emitted through the substrate from the bottom. The disadvantage of bottom emitting VCSELs is evident as the absorption of light by the substrate reduces the output power. This effect can be mitigated by reducing the thickness of the substrate, but it increases the complexity and difficulty of the fabrication process. The substrate's light absorption is wavelength-dependent, so the compatibility between the substrate material and the wavelength needs to be considered.

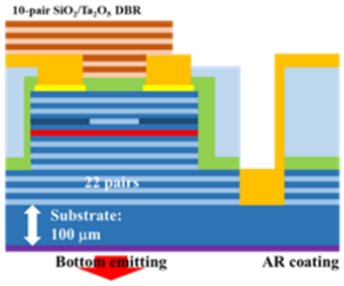


Fig. 2.3 Schematic of bottom emitting VCSEL

One significant advantage of bottom-emitting VCSELs over top-emitting VCSELs is their compatibility with the flip-chip bonding process. This allows for compact and high-density packaging, improved thermal management, and higher-speed applications.

2.4 Wavelength and mode choice of VCSEL

Table 2.4 Comparison of VCSELs at different wavelengths

	AlGaAs/GaAs based VCSEL (850nm)	InGaAs/GaAs based VCSEL (1060nm)	InP based VCSEL (1310nm/1550nm)
Threshold voltage	1.46V	1.17V	0.9V
Transparent current density	100A/cm^2	20A/cm^2	
Differential gain: dg/dJ	8x10^{16}cm^2/A	40x10^{16}cm^2/A	
Attenuation	2dB/km	1dB/km	0.5dB/km 0.27dB/km
Fiber chromatic dispersion	-90ps/(nm*km)	-30ps/(nm*km)	0ps/(nm*km) 17ps/(nm*km)
Substrate transparency back-side emission	No	Yes	Yes
Comment	Unable to be bottom emitting	Good	Low refractive index difference and low thermal conductivity of InP based materials

850nm, 1060nm, 1310nm, 1550nm is the typical wavelengths of VCSEL made by different materials. The characteristics of these VCSELs are shown in Table 2.4.

For GaAs substrate, the window wavelength can be easily calculated by band gap:

$$E_g(T) = 1.519 - \frac{5.408*10^{-4}T^2}{T+204} \quad \textbf{(2.4.1)}$$

When T=300K, E_g=1.422eV

$$E_g = \frac{hc}{\lambda_g} \quad \textbf{(2.4.2)}$$

Then λ_g=872 nm

This means that GaAs substrates are opaque to light at the 850nm wavelength, making it unsuitable for bottom emitting VCSELs.

For longer-wavelength VCSELs based on InP materials, the current production technology is still not fully mature, and the devices' stability and performance do not meet the requirements. Therefore, using InGaAs/GaAs VCSELs is the best choice for bottom-emitting applications. With InGaAs-based VCSELs, as the In composition increases, the wavelength becomes longer [33]. However, increasing the In composition also increases the stress between InGaAs and GaAs materials, raising the risk of device failure due to rupture. As a result, the wavelength limit for InGaAs-based VCSELs is around 1100nm. Considering material stability, we have chosen a wavelength of 1060nm in our design. Compared to the 850nm wavelength, the 1060nm wavelength has lower attenuation and fiber chromatic dispersion in optical fibers, making it advantageous for achieving longer-distance transmission.

2.5 Transverse coupled cavity VCSEL

The transmission scale of 850nm multimode VCSEL with multimode fiber in data centers faces a bottleneck after exceeding the transmission distance over 100m. The implementation of single mode VCSELs can be achieved by reducing the oxide aperture size to below 3.5 μm. However, reducing the oxidation aperture size results in higher resistance and thermal resistance, which leads to decreased modulation speed and device stability. Therefore, achieving single-mode operation under larger oxide aperture conditions is desirable, and there is a need for higher-speed

VCSELs with longer wavelengths.

VCSELs with transverse coupled cavity can realize single-mode operation with large oxidation aperture dur to Vernier effects. High modulation bandwidth thanks to coupled cavity. In this case, it was a good choice for meet the requirement for higher-speed and longer-distance optical transmission.

Table 2.5.1 Comparison of different VCSELs with transverse coupled cavity

	TCC VCSEL	**DTCC VCSEL**	**Surface-relief VCSEL**	**MA-VCSEL**
Transverse coupled cavity	Slow light cavity	Slow light cavity	Surface relief boundaries	Boundaries of oxidation aperture and contact metal
Mesa shape	Taper shaped mesas	Taper shaped mesas	Circle mesas	Circle mesas/Square mesas
Mesa size	8*6+20*13 μm	5*6+30*13+15*13 μm	26 μm	20*19 μm
OA size	3 μm	3 μm	6 μm	10*9 μm
External fabrication process	Ion-Implantation	Ion-Implantation	Wet etching	No necessary
Operation mode	Multi-mode/Single mode	Multi-mode/Single mode	Single mode	Single mode

Metal-aperture VCSEL was able to work at single mode operation for large oxidation aperture without external fabrication process. It was good for array fabrication process and the coupling with MCF.

2.6 Surface relief

Each transverse mode of VCSELs corresponds to a longitudinal mode. The transverse mode refers to the spatial distribution of the optical field, while the longitudinal mode is associated with the wavelength. VCSELs have short resonant cavities, which facilitates achieving single longitudinal mode output. Compared to the longitudinal modes, the transverse dimensions of VCSELs are much larger, which leads to insufficient confinement of the transverse optical field, resulting in multiple transverse modes. These multiple transverse modes often exhibit asymmetric distributions, which can affect the spectral linewidth and divergence angle of the laser. In this study, the objective is to achieve single longitudinal mode and single transverse mode lasing, requiring control over the transverse modes.

As shown in the Fig. 2.4, an oxidized aperture structure is formed on the oxide-confinement VCSEL after wet oxidation. The structure consists of a high refractive index center region surrounded by a lower refractive index region. The surface structure can be viewed as a cylindrical waveguide. By analyzing the modes within the waveguide, the fundamental mode is located in the central region of the higher refractive index waveguide, while the higher-order modes have intensity distributions at the edges of the lower refractive index waveguide. For single-mode VCSELs, it is necessary to suppress the higher-order modes.

By introducing a surface relief structure through etching circular grooves on the device surface, the surface relief structure is created. The reflectivity of the top distributed Bragg reflector (DBR) decreases with increasing etching depth. The reduction in reflectivity increases the mirror losses, requiring a higher threshold gain to achieve lasing. As a result, the higher-order modes in this

region are suppressed, leading to the realization of single transverse mode output. The low refractive index at center leaded more power to transverse coupling.

Meanwhile, because the etched region has a shorter resonant wavelength than the un-etched region, lasing light in the oxidized aperture can travel laterally into the oxidized region and is reflected at the boundary of the surface relief structure, which causes transverse resonance.

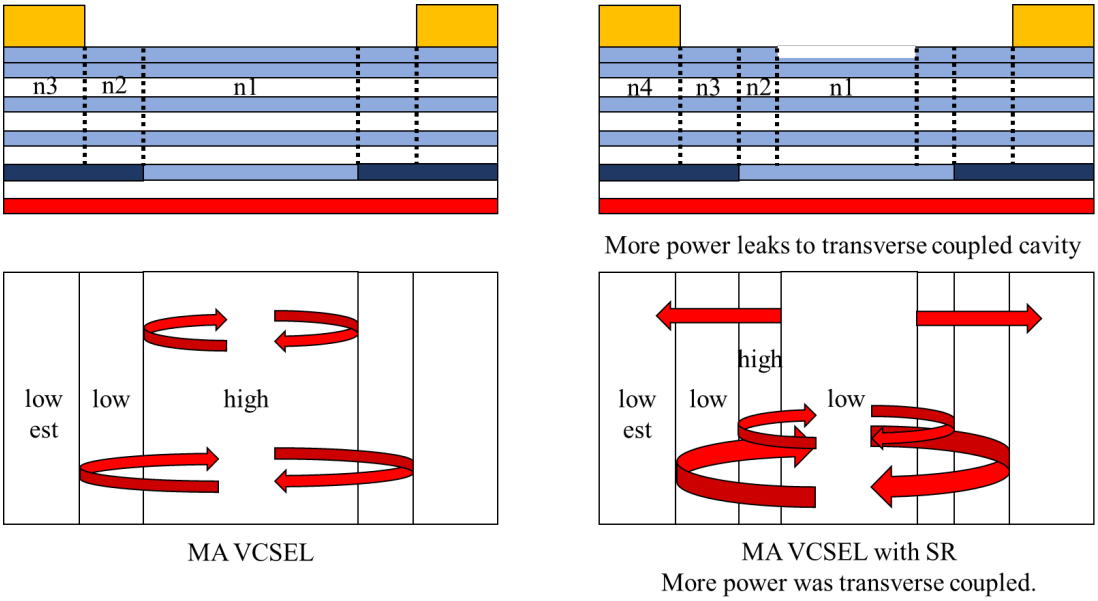


Fig. 2.4 Schematic of MA-VCSEL and MA-VCSEL with surface relief

In Fig. 2.5, the simulation results of the relationship between surface relief depth and transverse coupling power were shown. With the increase in depth, the transverse coupling power rose, and after reaching a peak, it began to decline with further increase in depth. At the same time, the lasing wavelength of the device shortened with the increase in depth. Therefore, the depth of the surface relief has a significant impact on transverse coupling. In the fabrication process, it is necessary to control the depth and aim for better etching quality. Regarding the diameter of the surface relief, in this study, it was designed to be less than or equal to the diameter of the oxidation aperture to meet the requirements of refractive index variation.

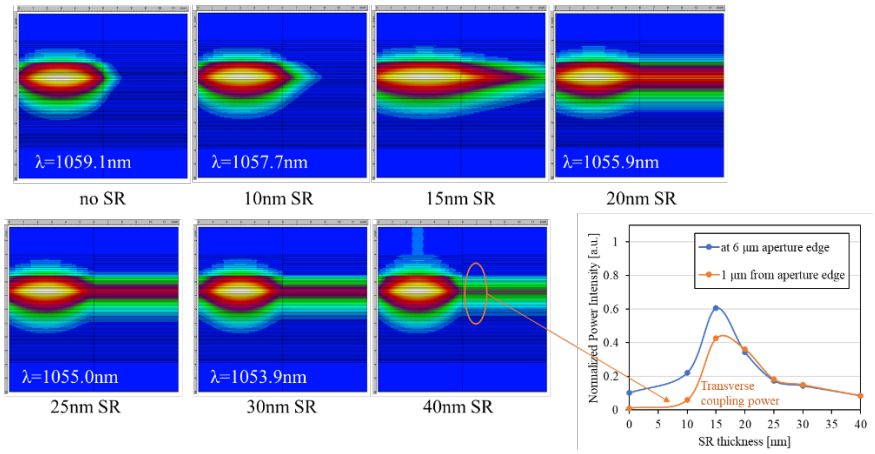


Fig. 2.5 The simulation results of the relationship between surface relief depth and transverse coupling power

2.7 Extrinsic parasitic response

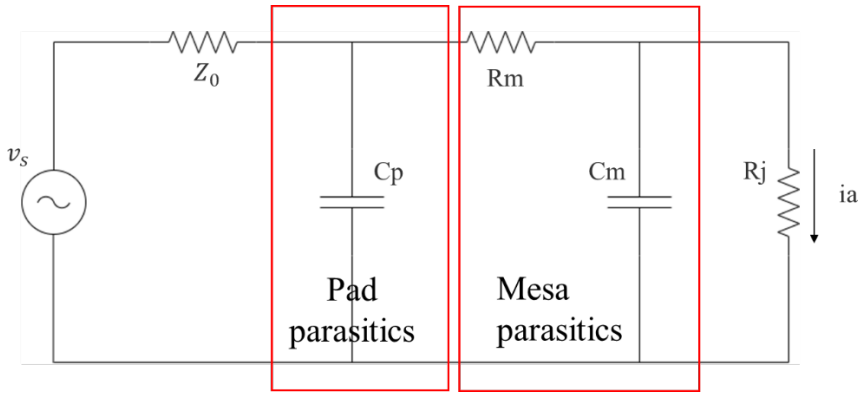


Fig. 2.6 Small-signal model with the driving source

Transfer function related to extrinsic parasitic response can be analyzed by Fig. 2.6 as follow:

$$\boldsymbol{Hext(\omega)} = \frac{\boldsymbol{i_a(\omega)}}{\boldsymbol{v_s}} = \frac{\mathbf{1}}{\boldsymbol{Z_0}\left[\mathbf{1}+\boldsymbol{R_j j\omega C_m}+\left(\boldsymbol{R_j j\omega C_m R_m}+\boldsymbol{R_m}+\boldsymbol{R_j}\right)\boldsymbol{j\omega C_p}\right]+\left(\boldsymbol{R_j j\omega C_m}+\mathbf{1}\right)\boldsymbol{R_m}+\boldsymbol{R_j}} \quad \textbf{(2.7.1)}$$

The frequency at which $|\boldsymbol{Hext(\omega)}|^2/|\boldsymbol{Hext(0)}|^2$ =1/2 is defined as the f3dB frequency which represents the maximum modulation bandwidth set by the parasitics.

From equation 2.7.1, it can be obtained that the extrinsic parasitic response was influenced by four parameters, pad parasitic Cp, mesa parasitic Cm, resistance Rm (total resistance of both DBRs, sheet resistance in the n-contact layer and contact resistance of both contacts) and junction resistance Rj. In this study, extrinsic parasitic response related to parasitics was considered. The modulation bandwidth at different pad parasitics was shown in Fig. 2.7. By reducing pad parasitics, extrinsic parasitic response can be pver 40GHz.

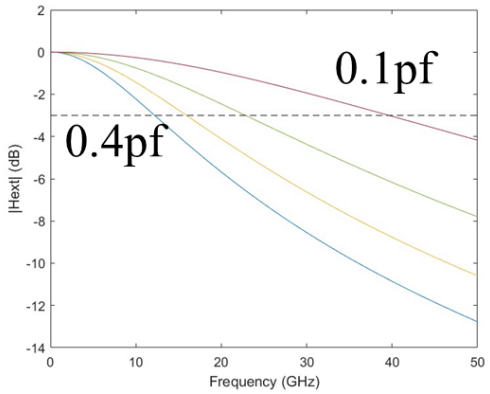


Fig. 2.7 extrinsic transfer function at different pad parasitics

2.8 Mesa parasitics

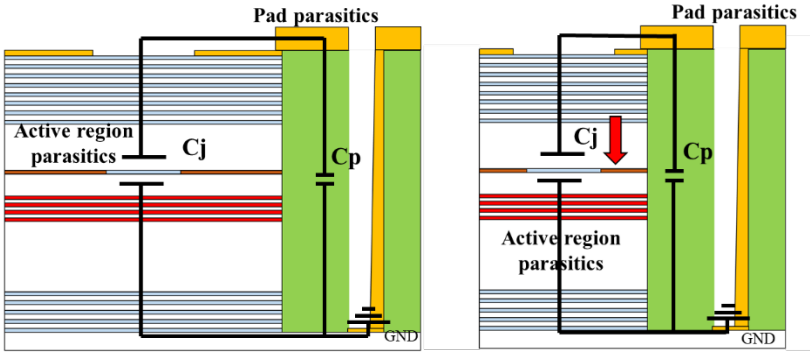


Fig. 2.8 Electrical parasitic capacitances and resistance in VCSEL

In this study, VCSEL arrays with both large-sized mesa structures and small-sized mesa structures were fabricated. For VCSELs with large-sized mesa structures, the mesa diameter was the target oxidation aperture plus 20 μm. For VCSELs with small-sized mesa structures, the mesa diameter was the target oxidation aperture plus 10 μm.

After the ICP (inductively coupled plasma) process, the wafer formed mesa structures for the oxide-confinement VCSELs. Increasing the diameter of the mesa structures can reduce the aspect ratio (height-to-diameter ratio) of the mesa structures, thereby enhancing their stability. However, as shown in Fig. 2.8, the mesa structures of the oxide-confinement VCSELs exhibit a mesa capacitance (Cm). Increasing the size of the mesa structures would increase the mesa capacitance, which can affect the device's speed response. Therefore, a trade-off needs to be made between these two mesa sizes.

2.9 Parasitic capacitance of electrode pads

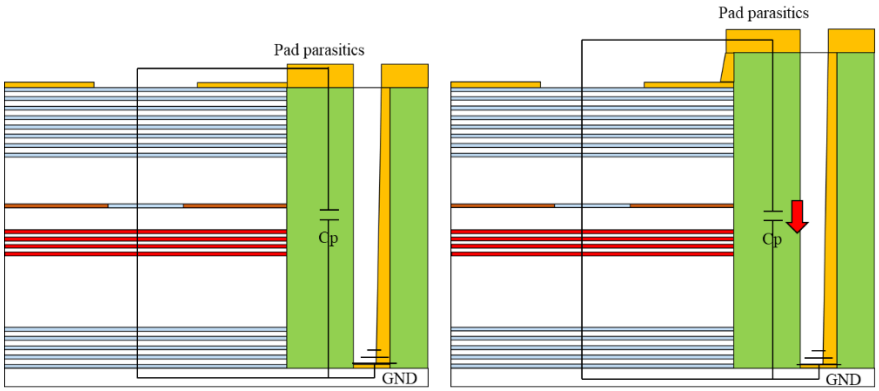


Fig. 2.9 Schematic of pad parasitics in VCSEL

In Fig. 2.9, the schematic of a typical oxide-confined VCSEL and the pad parasitics in VCSEL are shown. The pad capacitance Cp represents the capacitance between the signal and ground from the probe tips to the metal contacts. The value of Cp depends on the pad layout, the materials between the pads, and the height between the pads.

The reduction of pad parasitics was achieved by increasing the height between the pads, as

shown in the Fig. 2.9. Additionally, in this study, the p-electrode pad and n-electrode pad are grown at the same height on a planarized surface to reduce parasitic capacitance. To further minimize the parasitic capacitance of the electrodes, the connecting electrode between the p contact metal and p electrode pads was fabricated as narrow as possible.

2.10 Flip-chip bonding process

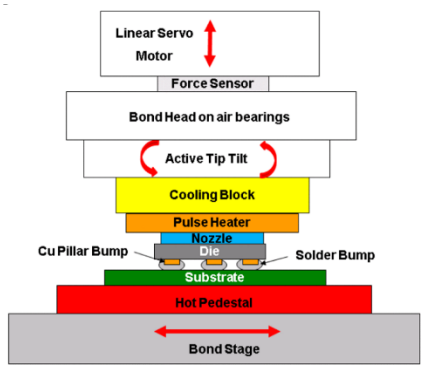


Fig. 2.10 Schematics of bonding apparatus (showing bond head to bond stage stacking) [34]

The bottom-emitting 1060nm 16-ch VCSEL can be packaged with CMOS IC and silicon carrier by flip-chip bonding process. The flip-chip bonding process has been widely applied in electronic and optoelectronic integration. It enables integration through small metal bumps. The advantages include improved signal transmission speed, higher I/O density, and enhanced thermal performance. Common method includes solder bonding by Thermo-Compression Bonding (TCB) [34]. The schematics of bonding apparatus for TCB is shown in Fig. 2.10. To avoid damage caused by high temperature, methods by new solder materials[35], surface-activated bonding (SAB) [36], ultrasonic flip-chip bonding (UFB) [37] are provided.

2.11 Multi-core fiber

In this study, the Vertical-Cavity Surface-Emitting Laser (VCSEL) array is coupled with multi-core fiber (MCF). Through spatial division multiplexing, the transmission capacity of a single fiber has been greatly increased. We have designed an MCF with 19 cores. The distribution of cores in MCF corresponds to the distribution of VCSELs in the VCSEL array. The cores are arranged in a hexagonal close-packed layout. The distance between two adjacent cores is 40um. The total diameter of the MCF is 220um. The MCF is designed for single-mode transmission. The mode field diameter (MFD) of the common single-mode fiber is 9um at 1060nm wavelength. This would lead to significant coupling losses. To achieve the best coupling efficiency, it is necessary to match the MFD of the MCF with the MFD of the VCSELs. The MFD of the fiber can be given by equation 2.11.1:

$$\boldsymbol{MFD = 2a(0.65 + \frac{1.619}{V^{\frac{3}{2}}} + \frac{2.879}{V^6})} \quad \textbf{(2.11.1)}$$

Where a is core radius and V is given by equation 2.11.2:

$$\boldsymbol{V = \frac{2\pi}{\lambda} aNA = \frac{2\pi}{\lambda} a\sqrt{n_{core}^2 - n_{cladding}^2}} \quad \textbf{(2.11.2)}$$

From equation 2.11.2, it can be seen that in order to reduce the MFD of the fiber, the refractive index difference between the core and the cladding needs to be increased. In this study, at 1060nm, the MFD of the MCF is 6.5um.

Chapter 3 Fabrication and characteristics of 1060nm VCSEL arrays

3.1 Introduction

In this study, the introduction of fabrication process of 1060nm VCSEL arrays is divided into two parts. One is the internal chip fabrication process done in our laboratory, Tokyo Tech. The sample size of the chip piece is 1.5 cm* 1.5 cm. The other one is wafer-scale fabrication process made in the foundry and our laboratory for 3-inch and 6-inch. These two fabrication processes are shown in section 3.2 and 3.3.

3.2 Internal chip fabrication process in Tokyo Tech

The internal chip fabrication process consists of wafer cut for a suitable sample size, sample wash, surface relief of GaAs, SiO_2 protect layer, p-contact metal, ICP (Inductively Coupled Plasma) to form mesa structure, oxidation to form oxidation confinement structure, n-contact wet etching, polyimide process, n-contact metal, p-electrode pad, dielectric DBR.

3.2.1 Wafer structure

The internal chip fabrication process done in our laboratory is based on 3-inch wafer grown by MOCVD. MOCVD stands for Metal-Organic Chemical Vapor Deposition. It is a technique used in the semiconductor industry for the deposition of thin films of various materials, particularly compound semiconductors. MOCVD is a popular method for growing high-quality epitaxial layers with precise control over thickness, composition, and doping.

The wafer structure of VCSEL is shown in Fig. 3.2.1. The initial wafer structure of VCSEL primarily consists of top p-type semiconductor DBR (Distributed Bragg Reflector) layers, an oxidation layer for oxide confinement, MQWs (Multiple Quantum Well), bottom n-type semiconductor DBR layers, and a substrate.

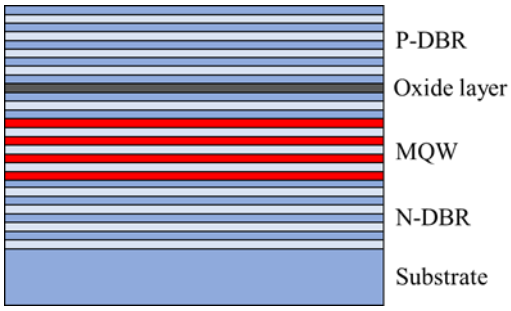


Fig. 3.2.1 Schematic of half-VCSEL wafer

The top p-type DBR is composed of two materials, GaAs and $Al_{0.92}Ga_{0.08}As$. Carbon doping is introduced into the materials to form a p-type configuration. In order to avoid structural instability and degradation of electrical performance caused by lattice mismatch, the composition of the layers gradually changes between the GaAs and $Al_{0.92}Ga_{0.88}As$ layers.

The bottom n-type DBR is composed of two materials, GaAs and $Al_{0.95}Ga_{0.05}As$. Silicon doping is introduced into the materials to form a n-type configuration. In order to avoid structural instability and degradation of electrical performance caused by lattice mismatch, the composition of the layers gradually changes between the GaAs and $Al_{0.95}Ga_{0.08}As$ layers.

For material GaAs, in the energy range below or near the fundamental absorption edge the dispersion of the refractive index n(λ) of GaAs can be calculated by the first-order Sellmeier equation [38]:

$$\boldsymbol{n(\lambda) = \sqrt{A + \frac{B}{1 - \frac{C^2}{\lambda^2}}}} \qquad \textbf{(3.1)}$$

Where the symbols and constants have the following meaning in the case of GaAs at room temperature:

Table 3.2.1 The symbols and constants in equation 3.1

λ	1.06 μm	vacuum wavelength
A	8.950	empirical coefficient

B	2.054	empirical coefficient
C^2	0.390	empirical coefficient

When wavelength is 1.06 μm, refractive index of GaAs can be calculated as 3.365.

For material $Al_xGa_{1-x}As$, the refractive index decreases with an increasing concentration of Al. According to [38], the real part of the refractive index n of a zinkblende material below the direct band gap edge can be expressed due to a simplified interband-transition model as:

$$\boldsymbol{n(\lambda) = \sqrt{A_0\left[f(X) + \frac{f(X_{s0})}{2}\left(\frac{E_0}{E_0+\Delta_0}\right)^{\frac{3}{2}}\right] + B_0}} \quad \textbf{(3.2)}$$

$$\boldsymbol{f(X) = \frac{2-\sqrt{1+X}-\sqrt{1-X}}{X^2}} \quad \textbf{(3.3)}$$

$$\boldsymbol{X = \frac{hc}{\lambda E_0}} \quad \textbf{(3.4)}$$

$$\boldsymbol{X_{s0} = \frac{hc}{\lambda(E_0+\Delta_0)}} \quad \textbf{(3.5)}$$

Where the symbols and constants have the following meaning in the case of $Al_xGa_{1-x}As$ at the room temperature :

Table 3.2.2 The symbols and constants in equation 3.2-3.5

n	(real part) of the refractive index	
λ	1.06 μm	vacuum wavelength
h	$6.626*10^{-34}$ Js	Planck´s constant
c	$2.998*10^8$ m/s	speed of light in vacuum
hc/λ	0.117 eV	Photon energy
x		Al fraction in the AlxGa1-xAs alloy
A_0	6.3 + 19.0 x	fitted constant
B_0	9.4 - 10.2 x	fitted constant
E_0	1.425 + 1.155 x + 0.37 x^2 eV	fundamental band gap at Γ-point

$E_0 + \Delta_0$	1.765 + 1.115 x + 0.37 x^2 eV	spin-orbit splitting energy

The relationship between refractive index and Al fraction in the AlxGa1-xAs is shown in Fig. 3.2.2.

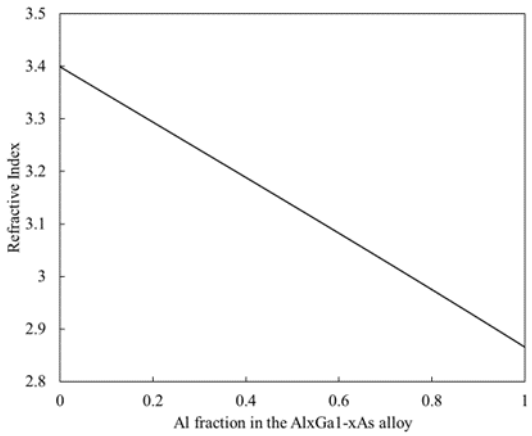


Fig. 3.2.2 Refractive index related to Al fraction

For p-type DBR, refractive index of $Al_{0.92}Ga_{0.88}As$ is 2.910. For n-type DBR, refractive index of $Al_{0.95}Ga_{0.08}As$ is 2.894. Compared with GaAs whose refractive index is 3.478, such large refractive index difference provides high reflectance. Reflectance can be calculated by the following equation:

$$\boldsymbol{R = 1 - \frac{4n}{n_1^2} * (\frac{n_2}{n_1})^{2k}} \quad \textbf{(3.6)}$$

Where R is reflectivity, n is the refractive index of substrate, n_1 is the high refractive index, n_2 is low refractive index and k is the pair number of DBR.

The relationship between reflectance and pairs of DBR for bottom n-type DBR is shown in Fig. 3.2.3.

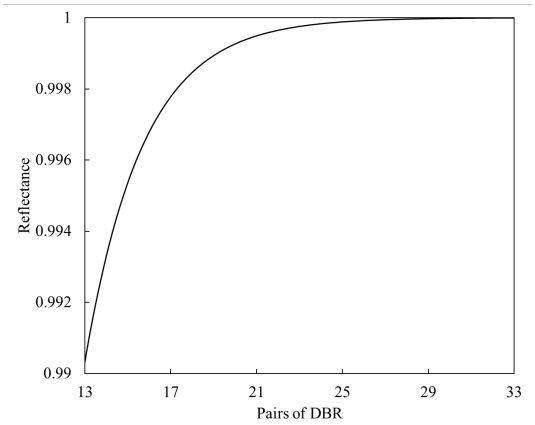


Fig. 3.2.3 Reflectance related to pairs of DBR

The pairs of bottom n-type DBR of the initial wafer is determined. For top emitting VCSEL wafer, pairs number of bottom n-type DBR is 33, the reflectance is 99.99%. For bottom emitting VCSEL wafer, pairs number of bottom n-type DBR is reduced to 22. The reflectance is 99.96%.

The reflectance of top DBRs is determined by the pairs of dielectric mirrors which are grown after finishing all fabrication process. In this case, this part is introduced in the following content.

The MQWs used for this study consists of $In_{0.25}Ga_{0.75}As/GaAs$. The PL (Photoluminescence) wavelength of MQWs is 1040 ± 2 nm. The thickness of adjacent n-type DBR and p-type DBR is adjusted to make sure the F-P dip at 1063 ± 5 nm which is shown in Fig. 3.2.4.

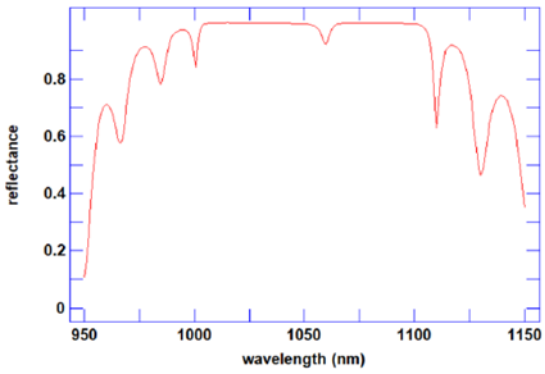


Fig. 3.2.4 F-P lasing wavelength

The introduction of oxide layer is explained in the section of oxidation process.

3.2.2 Mask

The internal fabrication process uses a direct writing lithography system to create mask patterns. The exposure power is set at 15mW, and the duty cycle is set at 80%. Depending on the pattern requirements, an XOR operation is selected. For example, when creating a surface relief pattern, a hollow pattern is generated for exposure, so there is no need to select XOR. However, when creating a pattern for the p contact metal, a solid pattern is needed to block the beam aperture at the center, so XOR needs to be selected. After the direct writing process, development is performed, and once the pattern boundaries are confirmed to be clear, the chromium (Cr) is etched. Finally, the photoresist on the mask surface is removed, completing the manufacturing of the mask pattern.

In the previous internal fabrication process, the photoresist was removed by immersing it in an AZ stripper solution at 80 °C. AZ stripper is a hazardous chemical. In this improved fabrication process, the removal of the photoresist was optimized. The mask aligner's laser check mode was used to perform a global exposure on the mask. Then, the mask was developed using the previous step's developer solution, effectively removing the photoresist from the mask. The condition for mask development is show in Table 3.2.3.

Table 3.2.3 Condition for mask

Step	Process	Time
1	AZ developer	1min
2	H_2O	1min
3	Air Dry	
4	Observation	
5	Cr etching	1min
6	H_2O	1min
7	Air Dry	

8	Observation	
9	Expose	50s
1	AZ developer	1min
2	H_2O	1min
3	Air Dry	
4	Observation	

3.2.3 Surface relief

Before photoresists, samples are washed by acetone and methanol. Acetone is a strong solvent that can effectively remove organic residues, oils, and greases from the sample surface. Methanol, on the other hand, is a milder solvent that is commonly used for general cleaning purposes.

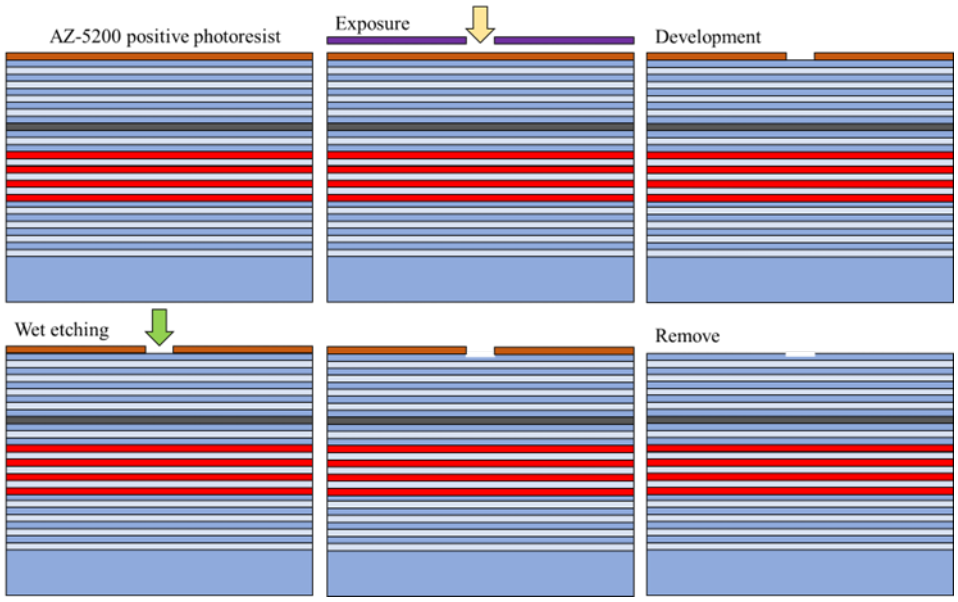


Fig. 3.2.5 Surface relief process

Surface relief of GaAs is for a better transverse coupling. The schematic of fabrication process of surface relief is shown in Fig. 3.2.5.

Positive photoresist is used for making pattern for wet etching. The spin-coating condition is shown in Table. 3.2.4.

Table 3.2.4 Spin-coating condition for SR pattern

500 rpm	5 s
1000 rpm	10s
3500 rpm	35 s

After a soft bake at 100 °C and 90 seconds, the positive photoresist is ready.

The photoresist-coated sample is exposed to UV light through a photomask, which contains the desired pattern. The exposure time should be controlled as short as possible to make sure the pattern size is not extended. The exposed areas of the photoresist undergo a photochemical reaction, causing them to become more soluble. The sample is immersed in a developer solution that selectively removes the more soluble areas, revealing the patterned resist.

The surface relief depth in this study is 30 nm. In this fabrication process, a hydrogen peroxide sulfuric acid solution is used for wet etching of the GaAs surface. By adding a drop of sulfuric acid and hydrogen peroxide to 100ml of water, an acidic solution is formed to slow down the etching rate of gallium arsenide, enabling better control over the etching depth. Although wet etching is an isotropic etching process that cannot guarantee precise etching quality and has limited control over the pattern, it offers advantages over dry etching. Wet etching does not require additional equipment, has lower cost, high selectivity, and good repeatability. It is well-suited for exploratory manufacturing in laboratory environments. In this fabrication process, wet etching is used as the first step. By performing multiple dummy samples for measurements of etching depth, the etch rate can be verified and the etching quality can be observed, ensuring that the surface relief is achieved as per the design specifications.

3.2.4 SiO_2 protective layer

To prevent damage or contamination of the sample surface from various chemical reagents or operations used in subsequent fabrication process, it is necessary to protect the sample surface after completing the surface relief. In this fabrication process, a few nanometers of SiO_2 protective layer are deposited on the sample surface using sputtering method shown in Fig. 3.2.6.

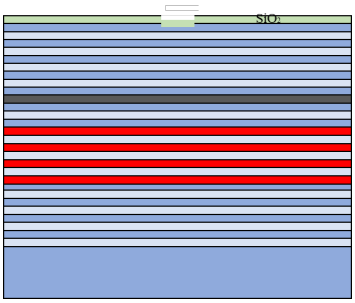


Fig. 3.2.6 Sputtering SiO_2

3.2.5 P contact metal

In the fabrication process of metal aperture VCSELs, the photoresist pattern for the p-contact metal is important. Here are some reasons:

1. The alignment between the p-contact metal position and the surface relief is critical but difficult.
2. The p-contact metal is in the form of a circular ring, with a small inner diameter of only a few μm. The photoresist used to mask the aperture positions is prone to misplacement or even loss due to its small area. It is necessary to reduce the exposure time to avoid overexposure and potential lateral exposure. The development time should be minimized to prevent excessive undercut. Gentle airflow should be used during the drying process.
3. Due to the small undercut, conventional heating for electrode lift-off becomes extremely difficult. In this fabrication process, ultrasonic-assisted heating is employed for electrode lift-off.

The schematic of fabrication process of p contact metal is shown in Fig. 3.2.7.

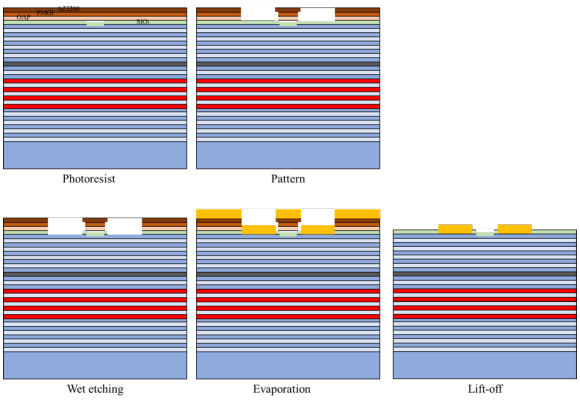


Fig. 3.2.7 The schematic of fabrication process of p contact metal

Due to the presence of the SiO_2 protective layer, first, OAP was spin coated at 3500 rpm for 45 seconds, then baked on hot plate at 100°C for 90 seconds to enhance the adhesion between the photoresist and SiO_2. Under the same conditions, PMGI and AZ5200 are spin-coated, with pre-baking at 150°C and 100 °C, respectively. Spin-coating PMGI is done to create an undercut after development, facilitating the lift-off process of the electrodes. Before evaporation, a quick wet etching of SiO_2 by HF should be done by using this pattern.

The evaporation composition is shown in Table 3.2.5.

Table 3.2.5 The evaporation composition of p contact metal

Metal	Thickness
Au	20nm
Zn	60nm
Au	150nm

Zn or Ti could be used to form alloy with contact layer of wafer to decrease the resistance of the device after annealing. The resistance is very important for high-power operation. The p contact metal is annealed at 420°C for 2 minutes. Then, annealing is performed in stages, gradually reducing the temperature by 10°C at a time until reaching 300°C. Afterward, the sample

is allowed to cool down to room temperature.

After annealing, the sample is placed in Remove PG and subjected to heating using an ultrasonic instrument to complete the lift-off process of the electrodes. If the photoresist pattern meets the requirements, the electrodes will be successfully removed through the lift-off process, revealing the aperture positions. However, if there are issues with the photoresist pattern, the electrodes at the aperture positions may not be removed, resulting in the failure of device fabrication. The photo of p contact metal is shown in Fig. 3.2.8.

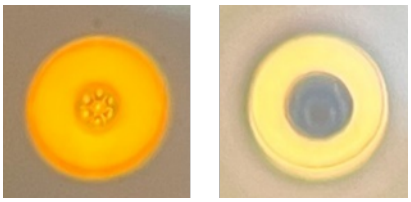


Fig. 3.2.8 P contact metal

3.2.6 ICP

To form the oxide-confinement structure, the sample needs to undergo ICP (Inductively Coupled Plasma) etching to create mesa structures and expose the sidewalls of the mesa. Due to equipment limitations, the ICP process is fabricated by an external company. Here, we will only provide an explanation of the ICP pattern. The presence of the SiO_2 protective layer requires the use of OAP and AZ5200 to form the ICP photoresist pattern. The spin-coating and baking methods mentioned earlier are employed. After the pattern is formed, HF (Hydrofluoric acid) is used to etch the exposed SiO_2 for the ICP etching of GaAs. The schematic of the ICP process is shown in

By using ICP technology, the mesa structures for the VCSEL array are formed simultaneously with the formation of the mesa structures shown in Fig. 3.2.9. Through the etching of the top P-DBR layer, the mesa structures of the VCSELs in each channel of the array are isolated from the laser cavities. The unetched bottom N-DBR layer will be used in the following process to form

the n-electrode contact. In other words, all channels in the array share the same n-electrode, ensuring a higher success rate for the array fabrication.

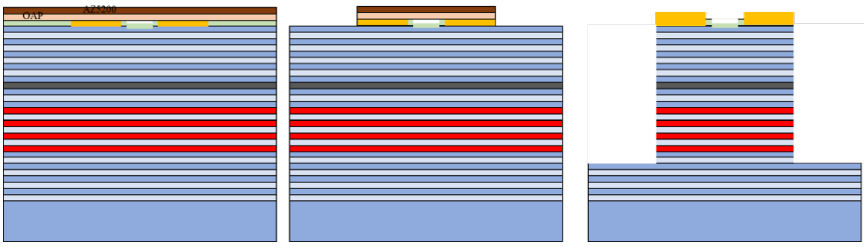


Fig. 3.2.9 ICP process

After the completion of ICP, the photoresist becomes difficult to remove. In this manufacturing process, the photoresist is first immersed in a 502A solution while being heated to facilitate its removal. Subsequently, any remaining photoresist is removed using plasma treatment.

3.2.7 Oxidation process

After the mesa structure was formed through ICP etching, the sidewalls of the entire mesa structure were exposed to the air. The semiconductor layer with a high concentration of Al slowly oxidized, increasing the device's resistance, and hindering the normal progress of wet oxidation. Therefore, the samples needed to be stored properly in a vacuum environment, and the wet oxidation fabrication process had to be arranged promptly. In the internal fabrication process, considering the strict vacuum requirements, the samples were stored in the equipment used for electrode evaporation after ICP, and the vacuum pump was activated to maintain a pressure below 10^{-5} Pa. If the samples were exposed to the air for too long, before proceeding with the wet oxidation process, the oxidized portion had to be etched using a diluted ammonia solution.

At high temperatures, water vapor can react with the oxide layer containing a high concentration of Al. The oxidation process occured laterally within the layer. By controlling the

oxidation process, the resulting Al_2O_3 can act as an electrical insulator, while the unoxidized central region served as the current injection area. Additionally, Al_2O_3 has a lower refractive index, making it suitable for waveguide confinement of optical waves. The introduction of oxide-confinement structures can significantly enhance the optoelectronic performance of VCSELs as shown in Fig. 3.2.10.

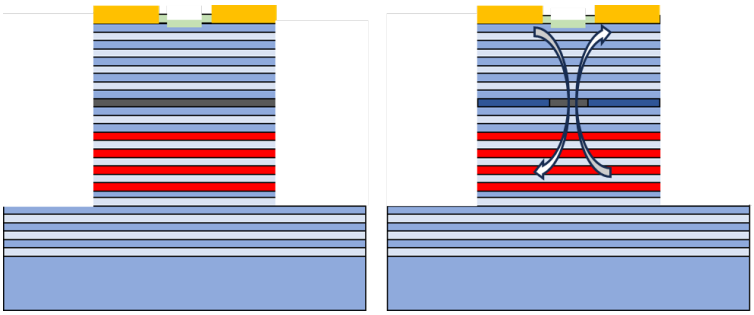


Fig. 3.2.10 Oxidation process

In the previous fabrication process, oxide layer was formed by AlGaAs which needs a high oxidation temperature at 390°C. The oxidation rate is also slow of 0.1 μm/min. To avoid the high temperature and long oxidation time, oxide layer is changed into AlAs. The oxidation temperature is reduced to 340°C. The oxidation rate is 0.2 μm/min.

The reaction equation is as follows:

$$\boldsymbol{2AlAs + 3H_2O \rightarrow Al_2O_3 + 2AsH_3} \quad \textbf{(3.7)}$$

Due to the low refractive index of the oxide formed after the oxidation of AlAs, which is only 1.6, a refractive index contrast is created between the oxidized and unoxidized regions. By observing the sample surface under a microscope at a specific wavelength, the oxidation process can be monitored in real-time, and the size of the oxide apertures can be measured. The oxidation rate depends not only on factors such as furnace temperature, nitrogen flow rate, and water temperature but also on the thickness of the AlAs layer and the diameter of the mesa structures. In this fabrication process, the thickness of the AlAs oxide-confinement layer used is set at 30nm. MFC (Mass Flow Controller) is at 10 SLM (Standard Liters per Minute). LMFC (Liquid Mass

Flow Controller) is at 1.00 g/min. The photo of oxidation apertures and mesa of VCSEL array taken by the microscope is shown in Fig. 3.2.11. The small black circle at the center means a high refractive index region.

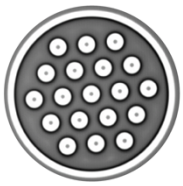


Fig. 3.2.11 Oxidation aperture of VCSEL array

Under the same oxidation conditions and for the same oxide width, it is expected that the oxidation time would be the same. However, in practical oxidation processes, variations in oxidation time are observed. The analysis reveals that the actual oxidation widths are different. Taking a mesa structure with a diameter of 16 μm as an example shown in, the sizes of mesa structures formed after several rounds of ICP are shown in Fig. 3.2.13. It can be observed that the top of the mesa structure is consistently etched according to the design size, thanks to the protection provided by the photolithography resist pattern on the surface. However, the bottom of the mesa structure tends to expand outward, and the observed maximum bottom diameter is 1.5 times the design diameter. This results in the overall mesa structure taking on a trapezoidal shape, which affects the required oxidation width during the process. While the final oxide aperture is determined through real-time observation, this phenomenon makes it challenging to predict the exact oxidation time.

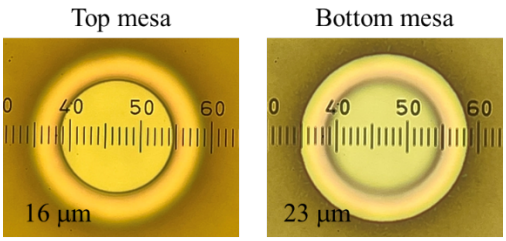


Fig. 3.2.12 Mesa size after ICP

During the oxidation process, the presence of surface relief on the mesa surface can impact the observation of the oxidation process. Here, microscope images are shown of mesa structures with and without surface relief after the oxidation process in Fig. 3.2.13. It can be clearly seen that mesa structures with surface relief can cause indistinct edges of the oxide apertures, thereby affecting the measurement of oxide aperture diameters. Therefore, when reserving test devices for the oxidation process, it is important to avoid any surface treatment of the devices.

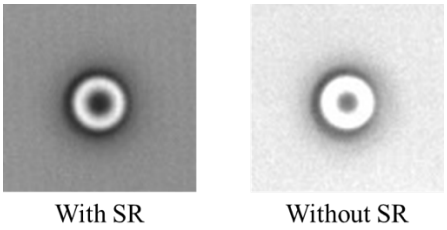


Fig. 3.2.13 OA images with and without SR

3.2.8 Wet etching for n contact

The bottom n-type DBR is etched to facilitate the subsequent deposition of n-contact metal. The etching process can be performed using either dry etching or wet etching. Dry etching allows for precise control of etching depth without side-etching effects. However, it can cause significant surface damage to the sample, and the photoresist used as a mask may become difficult to remove, potentially leading to further surface damage during the removal process. Wet etching, on the other hand, utilizes an acidic solution where etching occurs not only beneath the mask but also

affects the substrate. However, its advantages lie in minimal damage to the chip surface, low cost, and simplicity of operation. Therefore, wet etching is employed for etching the bottom n-type DBR.

In III-V compound materials such as GaAs, GaAlAs, and InGaAsP, the most commonly used selective etchant is the H_2SO_4-H_2O_2-H_2O series. This etchant is prepared by mixing concentrated H_2SO_4 (98%), H_2O_2 (30%), and water in a ratio of 1:8:80 for wet etching purposes.

The variation in solution temperature has a significant impact on the etching rate. By controlling the temperature of the etchant using a water bath, it is possible to maintain consistent etching rates across multiple experiments, thereby avoiding excessive etching depth that could lead to an increase in VCSEL resistance. At 22°C, etching speed of 2 μm/min can be obtained. Side-etching effects can be observed as shown in Fig. 3.2.14. In this fabrication process, the wet etching requirement for the lateral etching shown in the image is not stringent, and the observed side-etching will not significantly affect the performance of the VCSEL.



Fig. 3.2.14 n-contact etching and side-etching effects

3.2.9 N contact metal

The n contact metal was fabricated by evaporation, starting with the evaporation of AuGe followed by the evaporation of Au. The n contact metal undergoes alloying with the semiconductor by annealing at 360 °C for 2 minutes. The annealing process is carried out in the same manner as the operation for the p contact metal.

3.2.10 Polyimide

Polyimide is a polymer that is widely known for its thermo-oxidative stability, unique electrical properties, high radiation and solvent resistance, and high mechanical strength[39]. By spin-coating of polyimide, all mesa sidewalls in the VCSEL array were electrically insulated from electrodes and prevented from air. Meanwhile, planarization of samples was finished. The photosensitive positive polyimide was removed with lithograph pattern after exposure. The utilization of polyimide lowers interconnect and pad capacitance beyond that achieved with conventional silicon oxide (SiO_2, $\varepsilon r = 3.9$) or nitride (Si_3N_4, $\varepsilon r = 7.5$) passivation since it exhibits a lower dielectric constant ($\varepsilon r = 3.4$) and readily permits much thicker layers [40][41].

The thickness of polyimide used in the internal fabrication process, with same spin-coating and curing condition, was changed due to the variation composition of polyimide. As a result, dummy was needed for each fabrication process to determine the set of spin-coating and curing.

Here are the commonly used conditions for polyimide in the internal fabrication process. The lithography pattern should be smaller than p contact metal and n contact metal to avoid the disconnection of electrode caused by the large height difference.

According to the internal fabrication process experience, the height should be between 2.5 μm and 3 μm after curing. Because the lithography pattern was smaller than p contact metal, the height of the polyimide on p contact metal needed to be checked carefully after curing. If the height was more than 2 μm, plasma etching was needed to reduce the height to avoid the disconnection of electrodes.

Table 3.2.6 Condition of polyimide

Spin-coating	polyimide	1000 rpm	10 s
		4500 rpm	40 s
	Pre-bake	100 °C	90 s
Exposure		350W	22 s

Development	Cyclopentanone	Room temperature	60 s
	2-Acetoxy-1-methoxypropane	Room temperature	60 s
	Air-dry		
Cure		340 °C	45 min

3.2.11 Thick electrode pads

After the planarization and passivation of the samples by polyimide, thick electrode pads were fabricated by evaporation. The thickness of Au electrodes pads was between 500 nm to 2000 nm. Thick electrode pads didn't require alloying with the semiconductor, therefore annealing process was not necessary.

3.2.12 Dielectric DBR deposition

The dielectric DBR deposition of Ta_2O_5/SiO_2 was completed to provided high reflectivity of top DBRs. Compared with semiconductor DBR of AlGaAs/GaAs, dielectric DBR of Ta_2O_5/SiO_2 can offer much higher index contrast and less absorption[42]. A few pairs of dielectric DBRs are enough for VCSEL to achieve lasing. According to the calculation results, a 10-pair dielectric DBR provides a reflectivity equivalent to that of a 33-pair top semiconductor DBR. This avoided the formation of high series resistance and heat generation that may result from growing an thick top p-type DBR.

Dielectric DBRs were deposited at the end of fabrication process, which increases the flexibility in the fabrication process design.

Since the deposition of contact metal and electrode pads were completed, the dielectric DBRs didn't cause any device discontinuity.

3.3 Wafer-scale fabrication process

In order to validate that the designed VCSEL array is suitable for wafer-level manufacturing, a wafer-scale fabrication process was developed based on the required steps of the internal fabrication process. The entire wafer-scale fabrication process was entrusted to foundrys. The VCSEL arrays made by 3-inch and 6-inch wafer-scale fabrication process was shown in Fig. 3.3.1. For 3-inch wafer, it consisted of 4560 arrays. For 6-inch wafer, it consisted of 18240 arrays.



Fig. 3.3.1 Photo of VCSEL arrays made by 3-inch and 6-inch wafer-scale fabrication process

The schematic of wafer-scale fabrication process was shown in Fig. 3.3.2.

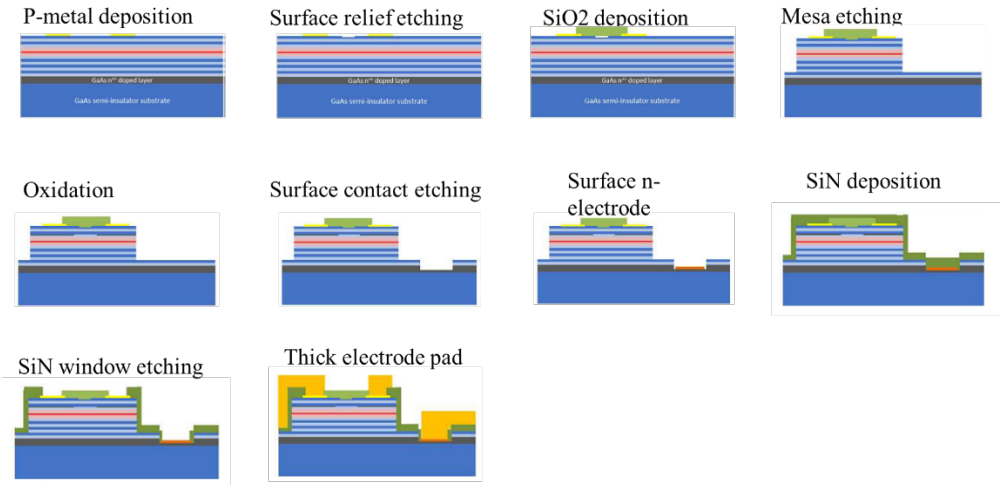


Fig. 3.3.2 Schematic of wafer-scale fabrication process

The wafer-scale fabrication process is based on the design and process of the internal fabrication process. With the validation of the wafer-scale fabrication process, the design of the

VCSEL array can be used for large-scale manufacturing. However, some issues inevitably arise. In this study, we noticed two main issues. The first one is the anisotropic oxidation rate during the external oxidation process, which leads to irregular shapes of the oxidation apertures that can't reach the design value. For MA VCSEL, the distance between the oxidation aperture and the contact metal must be well controlled to provide lateral coupling. Therefore, in this study, the 3-inch wafer-scale oxidation process was carried out internally. The oxidation aperture was well controlled. The second issue is that controlling the depth of the surface relief is not easy. Therefore, when the surface relief does not meet expectations, the device is improved through the internal wet etching process. At the same time, optimization of parasitic capacitance was performed on the VCSEL array that had already grown electrodes in the wafer-scale fabrication process. In this study, the electrodes were removed by wet etching, and after increasing the height between the electrode and the ground with polyimide, the electrodes were regrown. This verified the performance enhancement by reducing the parasitic capacitance. Finally, the wafer-scale fabrication process was improved.

3.3.1 Internal oxidation process in wafer-scale fabrication process

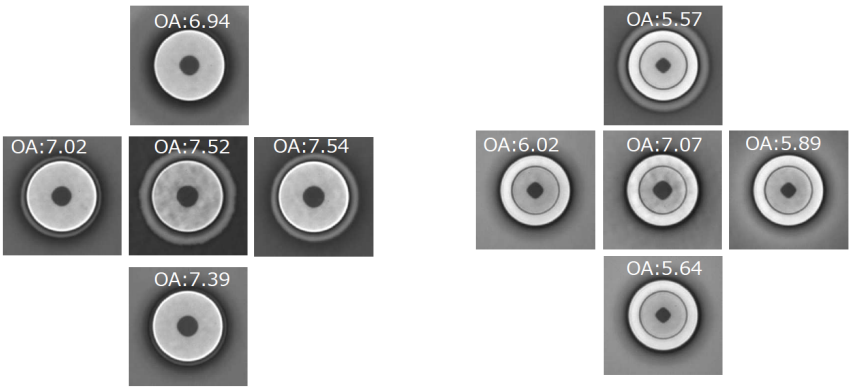


Fig. 3.3.3 Photos of oxidation aperture after oxidation process in Tokyo Tech and foundry

In the wafer-scale fabrication process, different issues were observed for 3-inch, 6-inch, and 12-inch wafers. Firstly, there was a significant variation in the oxidation aperture across different

positions on the same wafer. Secondly, the oxidation rate exhibited anisotropy in different directions of the mesa structure, resulting in a circular mesa structure with a diamond-shaped oxidation aperture. Therefore, the oxidation process for the 3-inch wafer-scale fabrication was conducted in our laboratory instead of using the same process as the foundry.

In our laboratory, the oxidation rate was only half of that in the foundry, using the same oxidation temperature. This difference was clearly observed through observations. In the internal fabrication process, the oxidation aperture remained consistent across different positions on the wafer, and the oxidation rate was consistent in all directions. Microscope images of the oxidation apertures and corresponding measurement results are shown in Fig. 3.3.3, with a target value of 7 μm for the oxidation aperture. The results on the left side correspond to the internal fabrication process.

3.3.2 Internal surface relief process in wafer-scale fabrication process

In the wafer-scale fabrication process, the final growth of the dielectric DBR (distributed Bragg reflector) does not take place. Therefore, before the growth of the dielectric DBR, further optimization of the samples can be performed using the internal fabrication process.

In the wafer-scale fabrication process, a protective layer of SiN is deposited by sputtering. By etching the SiN layer above the beam aperture, a surface relief structure can be formed to enhance the lateral coupling of the device. At this stage, due to the small spacing between the p-contact metal and the surface relief pattern, it is difficult to measure the etching depth accurately using probe contact after wet etching. After multiple attempts, the final approach chosen was to estimate the etching depth based on the color change of the SiN layer. The relationship between the color of SiN and its thickness is shown in Fig. 3.3.4.

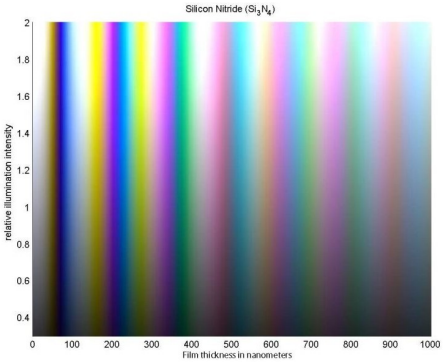


Fig. 3.3.4 The relationship between the color of SiN and its thickness

In this fabrication process, the reason for not choosing to etch SiN first followed by GaAs to form the surface relief structure is that without a protective layer, during the development of the dielectric DBR pattern, the development solution would damage the GaAs surface at the beam aperture, resulting in the device being unable lasing.

3.3.3 Internal electrode pads remake process in wafer-scale fabrication process

In the wafer-scale fabrication process, electrode pads were composed of Ti/Au or Au. In the internal fabrication process, wet etching could be performed on the electrode pads shown in Fig. 3.3.5.

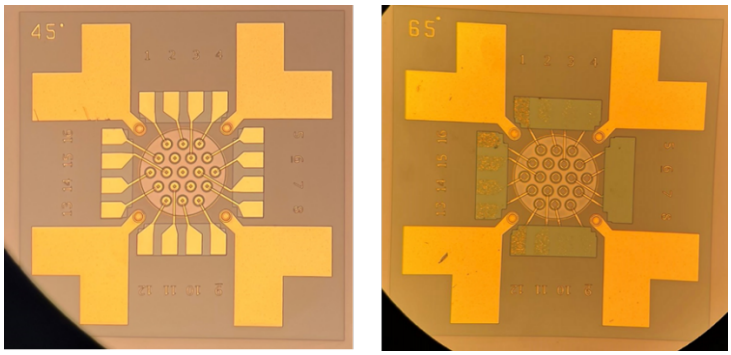


Fig. 3.3.5 P electrode pads remove

After etching, the height between the electrodes and GND was increased by curing polyimide

in the etched areas, and finally, the electrode pads were re-deposited shown in Fig. 3.3.6.

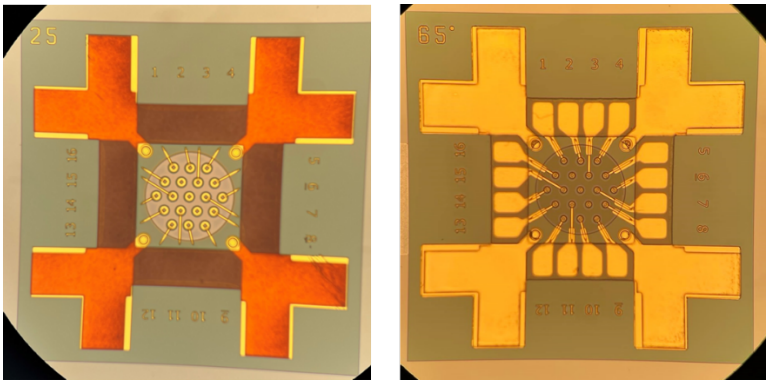


Fig. 3.3.6 Photo of polyimide and remake p electrode pads

By increasing the height between the electrodes and GND, the parasitic capacitance of the electrode pads could be reduced.

3.4 Characteristics of 1060nm VCSEL arrays

In this study, the research on VCSEL arrays transitioned from top emitting to bottom emitting. In this section, the static characteristics of the VCSEL array, including the ILV curve, spectrum, NFP and FFP, as well as thermal resistance and crosstalk, were investigated. The ILV curve provides information on the threshold current, turn-on voltage, maximum output power, thermal rollover current, slope efficiency, and conversion efficiency of the VCSEL. The spectrum analysis focuses on determining whether the VCSEL operates in single-mode operation and monitoring the changes in laser center wavelength with temperature variations. The linewidth of the main spectral peak and the side mode suppression ratio (SMSR) are used to analyze the transverse mode characteristics of the VCSEL. In this study, an indicator for single-mode operation was set as an SMSR greater than 30 dB. The near-field pattern (NFP) allows us to observe different transverse modes, including the fundamental mode and higher-order modes. The far-field pattern (FFP) can be used to assess the beam quality based on the laser's divergence angle.

3.4.1 Measurement system for static characteristics

a) Top emitting measurement system for static characteristics

The top emitting measurement system was designed to test top emitting VCSELs. After verification, it was found that the bottom emitting VCSELs can also be tested using this system by capturing the weak light emitted from the top. The threshold current, spectrum, and other parameters can be quickly tested. For the same device, the IL curve obtained from the top emitting measurement system and the bottom emitting measurement system is shown in the Fig. 3.4.1.

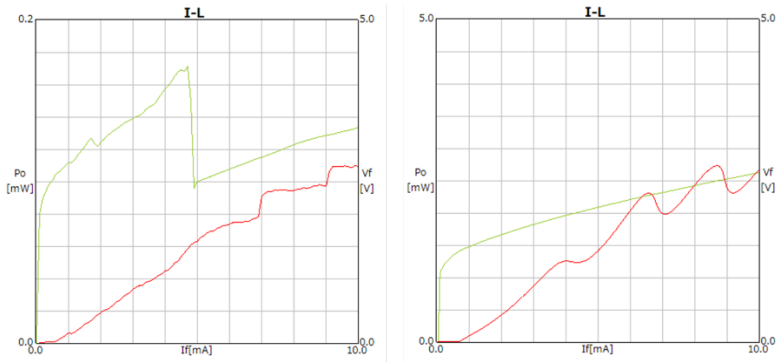


Fig. 3.4.1 ILV curve measured from top emitting measurement system and bottom emitting measurement system

Top emitting measurement system is divided into two parts. One part allows for manual and automatic testing of the ILV curve and spectrum, while the other part enables testing of the near-field pattern (NFP) and far-field pattern (FFP).

The ILV and spectrum testing system is based on the Laser Diode Test System provided by FSC company. The sample is securely fixed on a metal platform with temperature control using a vacuum pump. The metal platform is grounded and its position can be controlled by a motor. The sample is driven by the FSC company's laser diode tester, model FSC-LDTS-HNP-20A30V200N, which has a maximum drive current of 20A and a maximum drive voltage of 30V. It enables both continuous wave (CW) and pulse testing of VCSELs. The light emitted by the VCSEL is converted into electrical signals by a photodetector (PD) to measure the ILV curve. The

light is then coupled through optical fibers and connected to a spectrum analyzer to measure the spectral response.

The NFP (Near-Field Pattern) and FFP (Far-Field Pattern) measurements are integrated within the same imaging system. The measurement of NFP involves using a combination of lenses to magnify the NFP and focus it onto the receiving screen of a CCD (Charge-Coupled Device). This allows for the visualization and analysis of the near-field characteristics of the VCSEL.

On the other hand, the FFP measurement is performed directly in the Fraunhofer diffraction region. The FFP is captured using a receiving screen, and the resulting beam pattern is imaged onto the CCD receiving screen. This enables the observation and analysis of the far-field properties, including the divergence angle and beam quality of the VCSEL.

b) Bottom emitting measurement system

For the bottom emitting VCSEL array, where the electrode contact is in the opposite direction of the light emission, a specialized testing system needs to be set up. The sample is placed on a glass platform that can move along a sliding rail. The laser beam passes through the glass to perform the testing as shown in Fig. 3.4.2.

The bottom emitting measurement system integrates ILV testing, spectrum testing, NFP testing, and FFP testing into a single setup. These testing components are arranged in sequence on one side of the sliding rail.

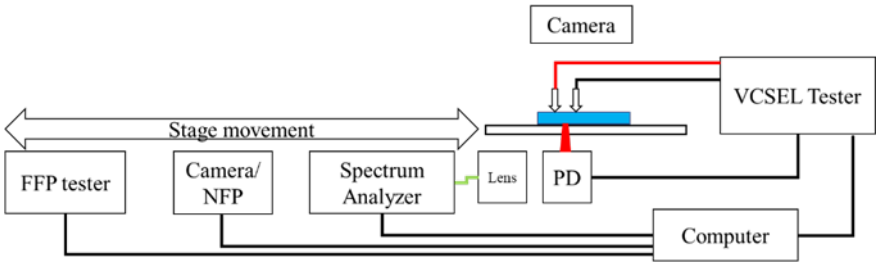
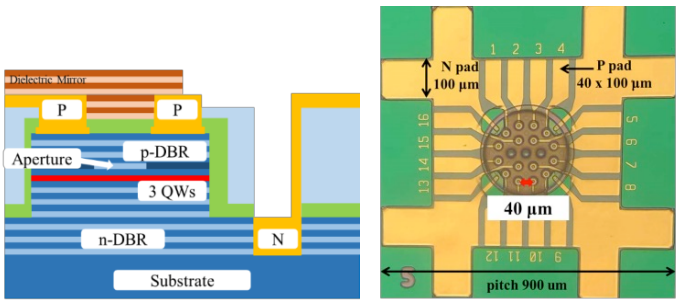


Fig. 3.4.2 Schematic of bottom emitting measurement system

3.4.2 Top emitting 16-ch VCSEL array

Fig.s 1 (a) and (b) show the schematic structure and photo of 1060 nm 16-ch top emitting intra-

cavity metal aperture VCSEL array, respectively, which was fabricated by 6-inch wafer foundry process. The active region consists of three $In_{0.25}Ga_{0.75}As$/GaAs quantum wells and the emitting wavelength is adjusted at 1060 nm. Mesa structures of VCSEL were fabricated through inductively coupled plasma (ICP) etching. The mesa diameter was designed as 20 mm for the target oxidation aperture of 6 mm. An oxidation confinement layer is formed by $Al_{0.98}Ga_{0.02}As$ at the node position of standing waves. We found that the intracavity metal aperture works as transverse coupled cavities which cause single mode operation and the bandwidth enhancement in modulation response at the same time. The distance between the metal electrode and oxide aperture could work as ultrashort external cavity. The experiment exhibited that the modulation bandwidth increases to more than two times larger than a conventional VCSEL thanks to the coupled cavity effect. Tiny coupled cavities (< 2 mm) enable stable bandwidth enhancement and single transverse mode operations, where a phase tuning mechanism could be unnecessary. In order to make such an intra-cavity contact, we used a hybrid top mirror composed of 6-pair AlGaAs semiconductor distributed Bragg reflector (DBR) and 6-pair SiO_2/Ti_2O_5 dielectric DBR. The reflectivity of the top DBRs is 99.3% and the reflectivity of the 33 pairs bottom DBR is over 99.9%.



(a) (b)

Fig. 3.4.3 (a) Schematic structure and (b) photo of 16-ch top emitting intra-cavity metal aperture VCSEL array.

We formed densely-integrated 16-ch VCSEL array as shown in Fig. 1 (b). While 19 mesas were

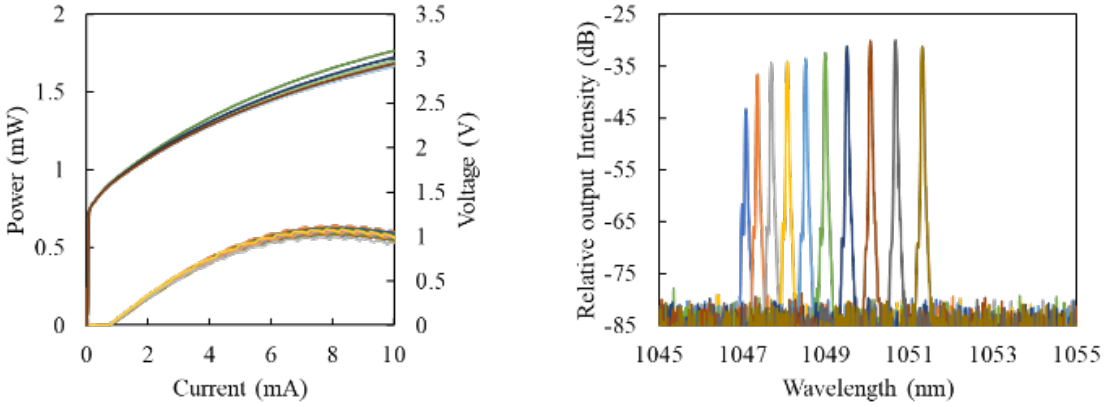
formed. Our 16-ch VCSEL array is designed and fabricated for co-packaged optics transceiver, supporting 1.6 Tbps with 100 Gbps per channel in the future. Meanwhile, three center VCSELs are not used in the 16-channel hexagonal array. These three center VCSELs could be used as a backup to improve the reliability.

The spacing between adjacent VCSELs is as small as 40 mm, which could be matched with a 19-core fiber. The total chip size of the array is as small as 900 mm by 900 mm. Each VCSEL can be operated individually.

The current-output (IL) characteristic and lasing spectra of the 16-ch VCSEL array are shown in Fig. 3.4.4. The series resistance of the top emitting VCSELs is approximately 138 Ω. The device shows single mode operations for the entire current range from 2 mA to 10 mA. The side mode suppression ratio (SMSR) is over 30 dB. The temperature change caused by self-heating can be estimated from the lasing wavelength shift as shown in Fig. 3.4.4(b) and is shown in Fig. 3.4.5, where the temperature dependence of lasing wavelength is assumed as 0.07 nm /K. The thermal resistance R of VCSEL in the array is defined by the following equation [43].

$$\boldsymbol{R = \frac{\Delta T}{I \cdot V - P_{light}}} \qquad \textbf{(3.4.1)}$$

where ΔT is the temperature change, $I \cdot V$ is the electrical power and P_{light} is the optical output power. From Fig. 3.4.5, the thermal resistance is estimated as 1900 K/W.



(a) (b)

Fig. 3.4.4 (a) Current-output (IL) characteristics and (b) lasing spectra at different bias currents from 2mA to 10mA.

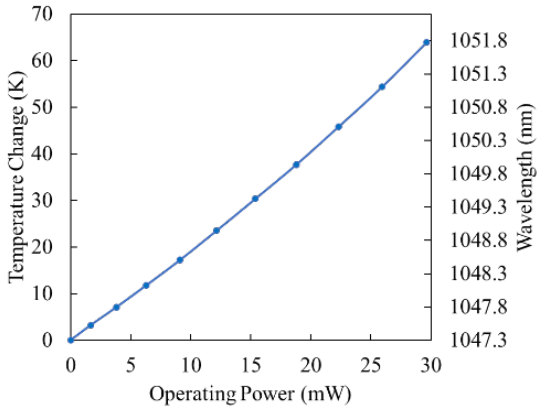


Fig. 3.4.5 Wavelength shift and temperature change versus electrical input power.

Then, the thermal crosstalk inside the 16-ch VCSEL array was measured. The total thermal crosstalk can be forecasted as the sum of the thermal crosstalk caused by each channel VCSEL. Thus, after the thermal crosstalk caused by each VCSEL in the array is measured, we can evaluate the total thermal crosstalk when all VCSELs are operated simultaneously.

The operating current to drive VCSELs in the array is set as 5.0 mA. The distance between two VCSELs in the array is the most important factor for thermal crosstalk. We measured the

wavelength shift and hence temperature change at different distances as shown in Fig. 3.4.6.

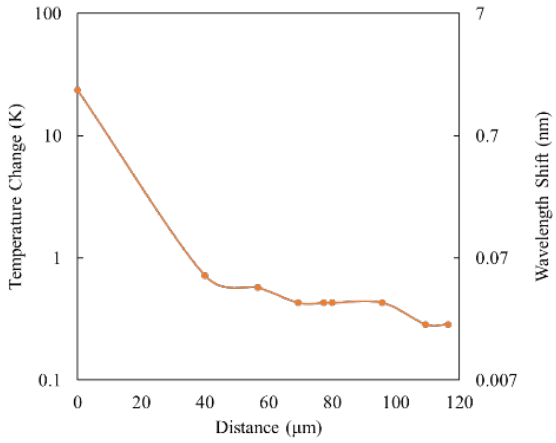
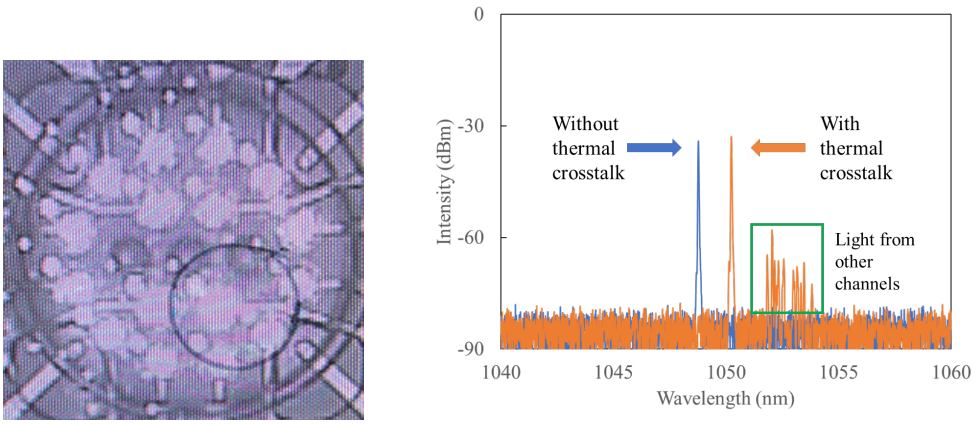


Fig. 3.4.6 Wavelength shift and temperature change at difference distances when current is fixed as 5.0 mA.

The temperature change caused by self-heating is approximately 23 K. The temperature change caused by an adjacent VCSEL at the distance of 40 μm is less than 1 K. Next, we carried out the evaluation of total thermal crosstalk when all the channels are operated simultaneously. The injection current of a VCSEL was fixed at 5 mA and other 15 VCSELs were operated at the same time as shown in Fig. 3.4.7(a). The injection current of other 15 channel VCSELs were changed from 0 to 10 mA. Fig. 3.4.7(b) shows the wavelength shift of the target device when other devices were operated at 10 mA. Based on the measured spectrum, the wavelength shift is 1.5 nm, and the total thermal crosstalk is estimated as 21 K. The forecast of the total thermal crosstalk of 16 VCSEL array at different injection currents is shown in Fig. 6. When all VCSELs are operated at 5 mA, the total thermal crosstalk is 7 K. A bias current of 5 mA is typical in current 25G 850nm VCSELs. At this bias current, the overall thermal crosstalk of 7K is much smaller even for all 16 channels are pumped simultaneously than the self-heating of 23K as shown in Fig. 3.4.6. Thus, the thermal crosstalk is not a big issue in our densely-integrated VCSEL array. In this case, a distance between each adjacent VCSELs of 40 mm could be large enough for keeping the thermal

crosstalk acceptable.



(a) (b)

Fig. 3.4.7 (a) Near field pattern of 16-ch VCSEL array and (b) lasing spectrum for all the 16-ch devices operated simultaneously.

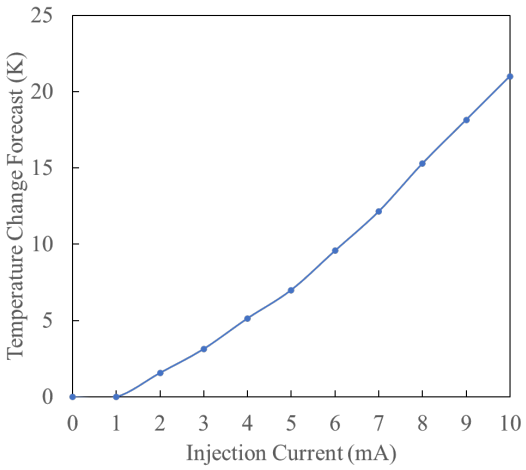
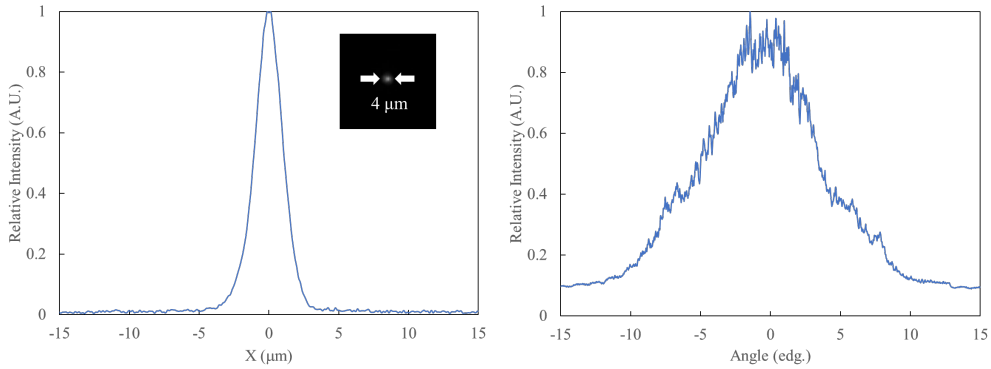


Fig. 3.4.8 Temperature change forecast at different injection currents

The near field pattern (NFP) and far field pattern (FFP) of the top emitting VCSEL array at a bias current of 5 mA are shown in Fig. 3.4.9(a) and (b), respectively.



(a) (b)

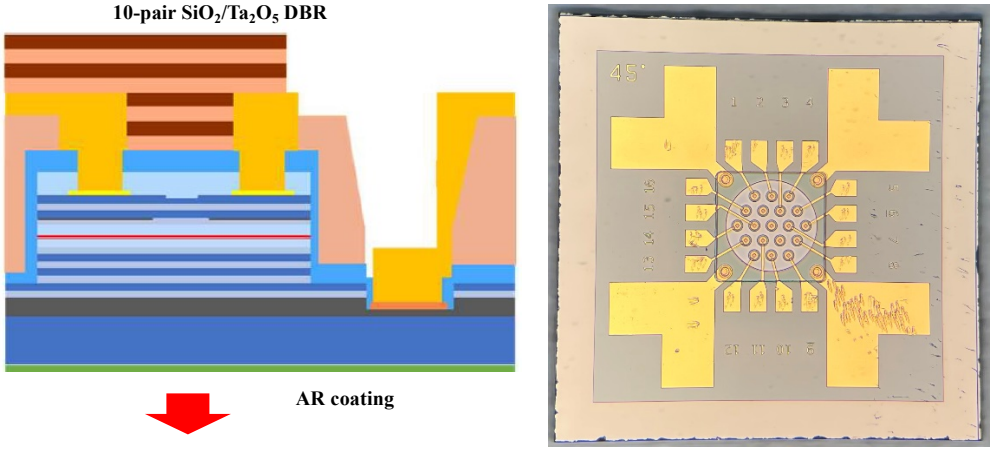
Fig. 3.4.9 (a) NFP and (b) FFP at 5 mA

The mode field diameter (MFD) is 4 μm and the full-width-at-half-maximum (FWHM) divergence angle is 10°. The MFD is controlled by the diameter of oxidation aperture. In order to further reduce the thermal crosstalk, we should realize single mode operation with a larger oxidation aperture.

3.4.3 Bottom emitting VCSEL array

Fig. 3.4.10 (a) and (b) show the schematic structure and photo of 1060 nm 16-ch bottom emitting intra-cavity metal aperture VCSEL array, respectively, which was fabricated by 3-inch wafer foundry process. There are structure differences in the bottom emitting VCSEL arrays. The hexagonal layout is used in the bottom emitting VCSEL array since the distance of neighboring channels could be equally 40 μm, which is a requirement from a multi-core fiber (MCF) because of constant optical crosstalk design in each core. In the fabrication of top emitting VCSEL arrays, outer VCSELs were not placed strictly according to the hexagonal placement. However, the impact on the thermal crosstalk could be negligible. Also, the size of oxidation apertures is slightly different. The target oxide aperture diameters of top emitting and bottom emitting VCSEL arrays are 5 μm and 7 μm, respectively. VCSELs with larger oxide apertures provide lower series

resistance and lower thermal crosstalk. We are currently working for expanding the oxide aperture diameter for better thermal management and better optical coupling with MCF as discussed later. For the bottom emitting array, the reflectivity of the 10 pairs top dielectric DBR is as high as 99.96%. The reflectivity of the 22-pairs bottom DBR is 99.25% with anti-reflection coating of a substrate back surface.



(a) (b)

Fig. 3.4.10 (a) Schematic structure and (b) photo of 16-ch bottom emitting intra-cavity metal aperture VCSEL array.

Two types of devices with oxidation apertures of 5 μm and 7 μm based on the mesa size, both located on the same wafer. The oxidation aperture can be estimated using the near-field pattern (NFP). According to previous research, the variation of oxidation aperture and NFP for VCSELs is 1 μm. The NFPs are displayed in Fig. 3.4.11. For devices with a 5 μm oxidation aperture, the NFP measures 4.2 μm, increasing to 5.6 μm when the oxidation aperture expands to 7 μm. This variation arises from different oxidation rates at various wafer positions. The NFP results align with our target oxidation apertures.

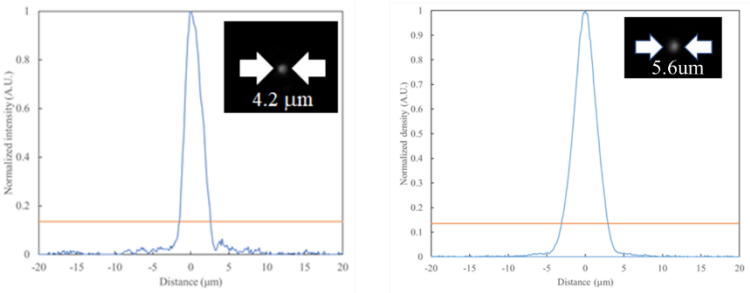


Fig. 3.4.11 NFP for devices with 5 μm OA (Left) and 7 μm OA (Right)

The current-voltage-light (IVL) curve and spectrum of the bottom-emitting VCSEL are measured under continuous wave (CW) conditions at room temperature (20°C). Without the flip-bonding process, the VCSEL array is placed on a glass slide to measure the output power and spectrum from the bottom side. The substrate's backside is coated with an anti-reflection (AR) coating, and both sides of the glass plate are coated with AR coatings to minimize the impact of reflection.

For devices with a 5 μm oxidation aperture, the IVL curve of all 16 channels and the typical spectrum are depicted in Fig. 3.4.12 (a) and (b), with a 1.5 μm boundary gap between the oxidation aperture (OA) and the contact metal (CM). At 6 mA, the voltage is below 2.2 V, and the threshold voltage is only 1.1 V. The output power at 6 mA is approximately 3 mW, with a threshold current of 0.6 mA. For the entire operating current range from 1 mA to 6 mA, the devices maintain single-mode operation with a side-mode suppression ratio (SMSR) above 40 dB, demonstrating effective transverse coupling.

For devices with a 7 μm oxidation aperture, the spectrum is displayed in Fig. 3.4.12 (c), with a 1.5 μm boundary gap between OA and CM. Thanks to the transverse coupled cavity, devices with a 7 μm oxidation aperture can operate in single-mode for the current range of 1 mA to 6 mA.

Devices with a boundary gap between the contact metal and oxidation aperture exceeding 2 μm lack a transverse coupled cavity. The spectrum for devices on the same piece is presented in

Fig. 3(d). Even for devices with a 5 μm oxidation aperture, multi-mode operation is observed.

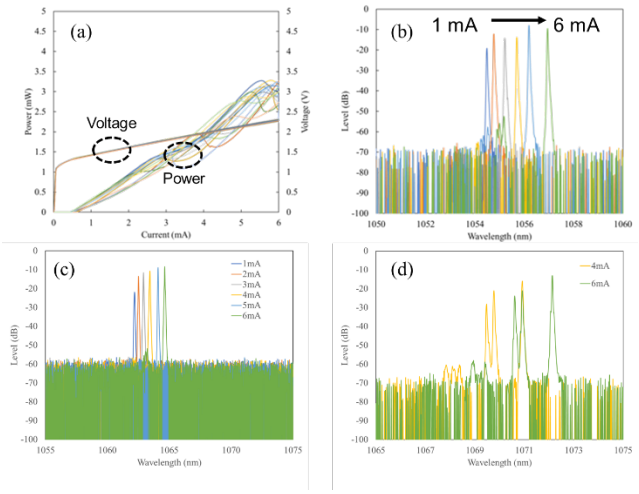


Fig. 3.4.12 (a) 16-channel IVL curve with 5μm OA; (b) Spectrum of single-mode VCSEL with 5μm OA; (c) Spectrum of single-mode VCSEL with 7μm OA; (d) Spectrum of conventional VCSEL with 5μm OA.

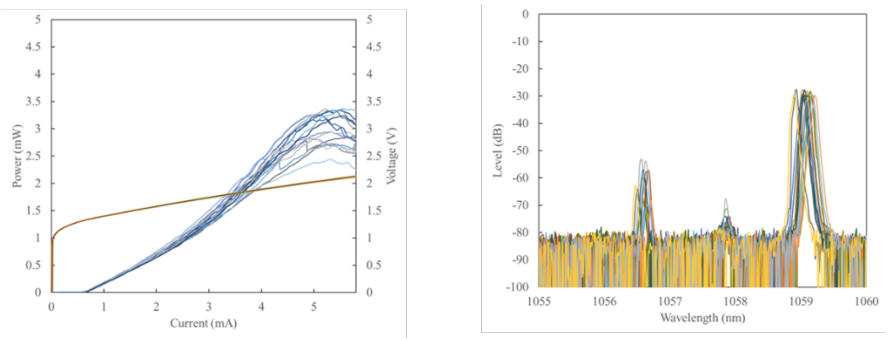


Fig. 3.4.13 Superimposed ILV curves and spectra of 16-ch VCSEL array without SR

In Fig. 3.4.13, the superimposed ILV curves and spectra of all 16 channels in a VCSEL array without SR was shown. The boundaries gap between OA and CM was 0.5 μm. The threshold voltage was 1.1V and threshold current was 0.6mA. Resistance was 100 Ω. Output power was 3.5 mW.

The SMSR at 6mA for all 16 channels were 30dB. 30dB was enough for single-mode operation.

The single-mode operation came from the transverse coupled cavity by the metal aperture structure. However, the transverse coupled cavity was weak leaded to high order mode which caused noise and poor beam quality.

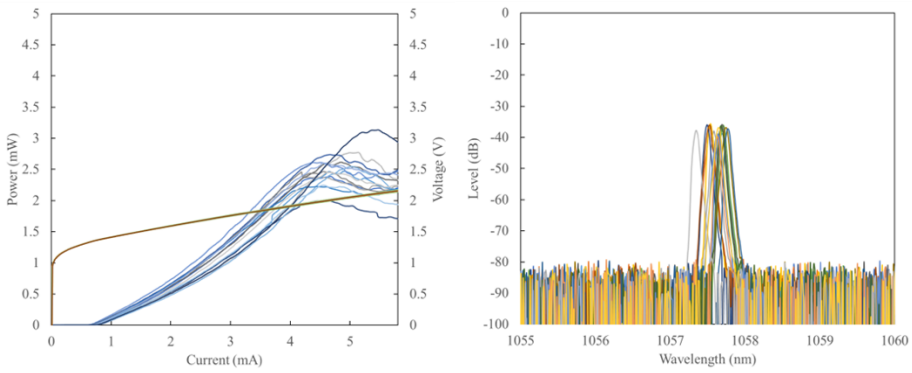


Fig. 3.4.14 Superimposed ILV curves and spectra of 16-ch VCSEL array with SR

In Fig. 3.4.14, the superimposed ILV curves and spectra of all 16 channels in a VCSEL array with SR was shown. The devices in Fig. 3.4.13 and 3.4.14 were selected from the same wafer. The boundaries gap between OA and CM was 0.5 μm which was as same as device shown in Fig. 3.4.13. In this case, the variation came from surface relief. The threshold voltage was 1.1V and threshold current was 0.8mA. Resistance was 150 Ω. Output power was 2.5 mW. The reduce of output power and increase of threshold current were caused by the mirror loss due to surface relief.

The SMSR at 6mA for all 16 channels were over 40dB. With surface relief, the reflectivity of top DBR was decreased. The resonant wavelength was shift to a shorter wavelength leaded to a stronger transverse coupling. All high order transverse modes were disappeared.

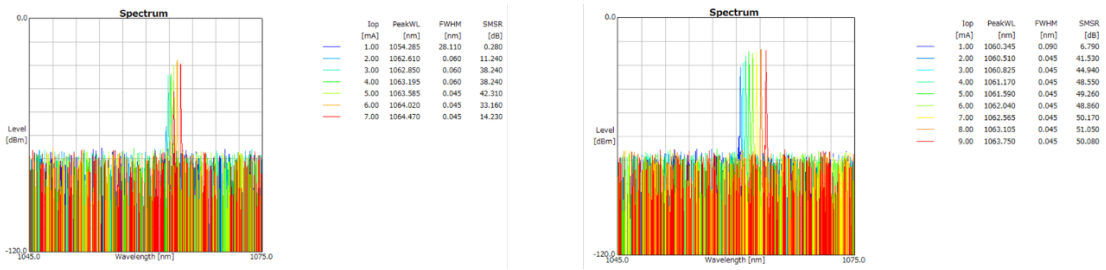


Fig. 3.4.15 SMSR and wavelength shift related to SR depth (Left) 15 nm and (Right) 30 nm

The spectra of devices with large oxidation aperture with different SR depths were shown in Fig. 3.4.15. The oxidation aperture was 7 μm and diameter of inner contact metal was 8 μm. The boundaries gap between OA and CM was 0.5 μm. With SR, devices with large oxidation aperture showed good single mode operation at 2mA to 6mA. But SMSR was different at higher operation current. With a narrow surface relief, SMSR was reduced to 14 dB at 7mA. With a deep surface relief, SMSR was over 50dB at 9mA.

The wavelength shift in the region with surface relief was related to surface relief depth. At 6mA, with a narrow surface relief, wavelength was 1064.02nm. With a deep surface relief, wavelength was 1062.04nm. The wavelength shift was 2nm.

Detuning of the resonant wavelength between the region with surface relief and without surface relief give a better SMSR.

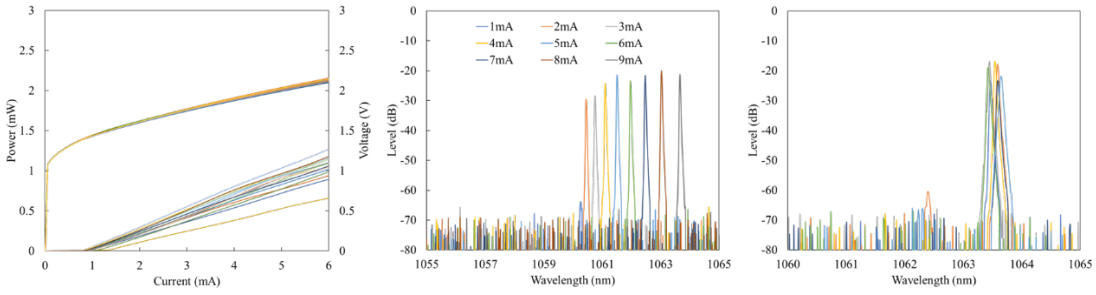


Fig. 3.4.15 Superimposed ILV curves, spectrum from 1mA to 9mA and superimposed spectra of 16-ch VCSEL array with large oxidation aperture

The Superimposed ILV curves and superimposed spectra of 16-ch VCSEL array with large oxidation aperture were shown in Fig. 3.4.15. With SR depth of 30nm, spectrum from 2mA to 9mA showed SMSR over 40dB. The superimposed spectra at 9 mA showed a good uniformity of

all 16 channels.

The evaluation of thermal resistance and thermal crosstalk of bottom emitting VCSEL array was also considered. For comparison, devices with 5 μm oxidation aperture and 7 μm oxidation aperture was measured of output power, operation power and spectrum to see the effect of oxidation aperture size on thermal resistance. The dissipated power was defined as the difference value of operation power and output power. The relationship between dissipated power and temperature change of devices with 5 μm OA and 7 μm OA was shown in Fig. 3.4.16. The slope of the graph represents the thermal resistance. From the figure, the thermal resistance of devices with 5 μm oxidation aperture was 2.4K/mW and it was 1.9K/mW when the oxidation aperture was increased to 7 μm.

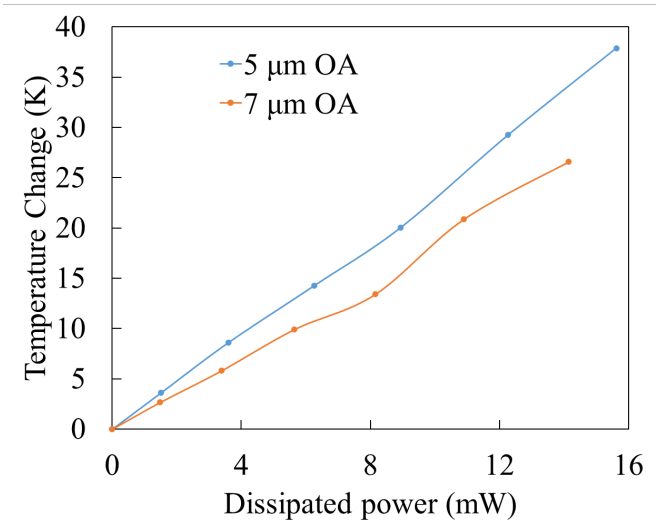


Fig. 3.4.16 The relationship between dissipated power and temperature change of devices with 5 μm OA and 7 μm OA

In this study, 10 pairs of dielectrics DBR of Ta_2O_5/SiO_2 was used for enough reflectivity of top DBRs. The thermal conductivity of Ta_2O_5 was 0.3W/mK and SiO_2 was 1.4 W/mK. Both were much lower than thermal conductivity of GaAs and $Al_{0.92}Ga_{0.08}As$ which was 55 W/mK and 70 W/mK. In this case, the thermal resistance in this study was compared with the results from other

research as shown in Fig. 3.4.17.

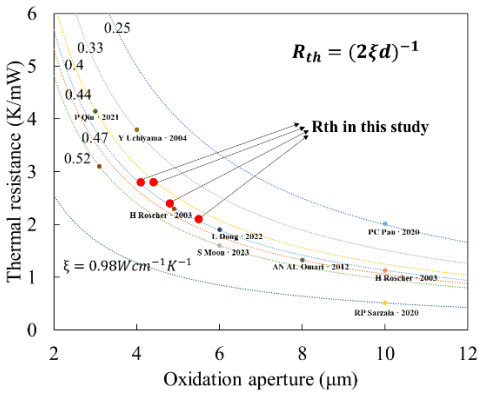


Fig. 3.4.17 The comparison of thermal resistance with other research

Thermal resistance Rth follows the relation $R_{th} = (2\xi d)^{-1}$, which d is the oxidation aperture and ξ is the thermal conductivity. In this figure, the estimated ξ value was listed by using the best fits of Rth and oxidation aperture. From the figure, the thermal resistance in this study by growing dielectric DBRs was still in an acceptable range.

The thermal crosstalk related to distance of bottom emitting VCSEL was measured by using devices with different thermal crosstalk. The relationship between thermal crosstalk and distance with self-heating was shown in Fig. 3.4.18. From the figure, VCSEL array with low thermal resistance has low thermal crosstalk. If the distance was increased to be over 40 μm which was the space between adjacent channels, the thermal crosstalk was reduced to a low level and it's difficult to be further lower. In this case, 40 μm was suitable for our 16 channels VCSEL array.

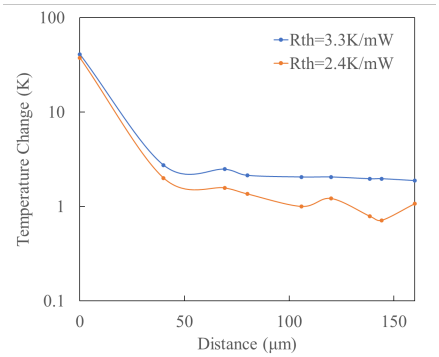


Fig. 3.4.18 Thermal crosstalk related to the distance

From the relationship between thermal crosstalk, the total thermal crosstalk at different positions can be estimated. The results when thermal resistance was 2.4 K/mW were shown in Fig. 3.4.19.

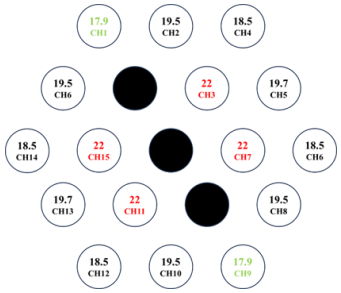


Fig. 3.4.19 Total thermal crosstalk related to channel position

The highest total thermal crosstalk happened at the center channels. The lowest total thermal crosstalk happened at the edge channels. The variation was 4 K. The total thermal crosstalk can be reduced by reducing the operation current and selecting large oxidation aperture devices.

Chapter 4 High speed modulation characteristics

4.1 Introduction

In this chapter, we demonstrate a 16-channel single-mode bottom-emitting VCSEL array operating at 1060 nm for longer optical transmission and bottom emission. This VCSEL array is designed for integration via a flip-chip bonding process and will optically couple with a single-mode 16-channel MCF. With a small signal response of 23 GHz, and benefiting from pulse compression after transmission in single-mode fiber (SMF), we achieved 70 Gbps NRZ and 90 Gbps PAM-4 signal transmission with pre-equalization.

4.2 Structure

In our co-packaged optics research, we have concentrated on a 1060 nm bottom-emitting VCSEL array featuring a metal aperture structure, as depicted in Fig. 4.2.1(a). By controlling the gap between the contact metal and oxidation aperture boundaries, we achieve better transverse coupling, thereby enhancing the device's performance. The metal aperture VCSEL design offers a high modulation bandwidth due to the coupled cavities, and the Vernier effect facilitates single-transverse mode operation. Moreover, the fabrication process is relatively simple, and the large mode field diameter is suitable for coupling. The bottom-emitting characteristic allows for flip-chip bonding, reducing the need for complex electrical wiring.

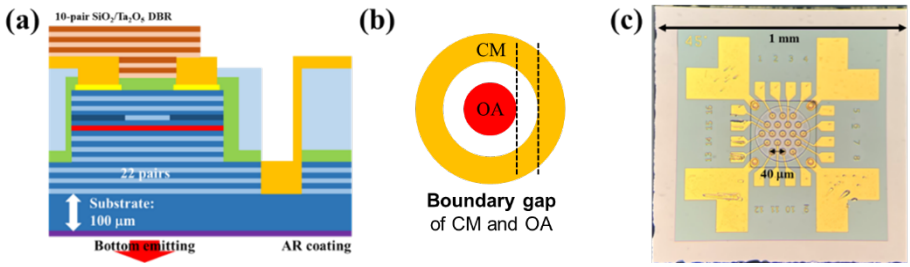


Fig. 4.2.1 (a) Schematic of MA VCSELs; (b) Boundary gap of CM and OA; (c) Photo of VCSEL array

The fabrication process is based on the conventional CMOS process for 3-inch wafers. We employ inductively coupled plasma (ICP) to form the mesa structure of the VCSEL. The mesa size is set at 15 μm and 17 μm to create oxidation apertures of 5 μm and 7 μm, reducing the mesa size to decrease the junction capacitance compared to the previous process involving 25 μm and 27 μm. To realize bottom emission, the number of n-DBR (Distributed Bragg Reflector) pairs is reduced to 22, providing a reflectance of 99.96%. The top p-DBRs offer a reflectance of 99.25%. For better oxidation aperture control, we use an AlAs oxidation layer and form an oxide-confined VCSEL through wet oxidation at 340°C. The oxidation apertures are 5 μm and 7 μm, and a GaAs surface relief is created to enhance the transverse coupled cavity effect. The space between the oxidation aperture and contact metal boundaries is less than 2 μm, resulting in a transverse coupled cavity, as shown in Fig. 4.2.1 (b). We increase the thickness of the polyimide to reduce parasitic capacitance and improve speed performance.

We have fabricated a 16-channel 1060 nm bottom-emitting VCSEL array with a channel spacing of 40 μm and a small chip size, as illustrated in Fig. 4.2.1(c). The total chip size, including electrode pads and the protection region, measures 1 mm by 1 mm.

4.3 Small signal response

The small signal response is measured from the bottom side. To avoid reflection caused by the glass plate and increase the coupled power, we replaced the glass plate with a metal plate featuring a hole, allowing the light beam to be coupled into a single-mode fiber using a lens focuser.

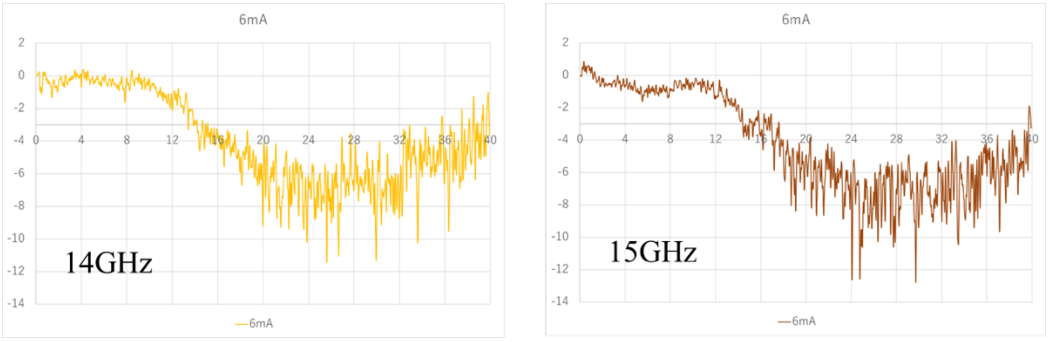


Fig. 4.3.1 Small signal response of devices with and without SR

The small signal response of devices with and without SR was shown in Fig. 4.3.1. The devices were from the same wafer. The ILV curve and spectrum was shown in Chapter 3.4.3. The oxidation aperture was 5 μm and diameter of contact metal was 6 μm. The mesa size was 25 μm. With surface relief, more power was transverse coupled leaded to stronger transverse coupling. Benefited from PPR, small signal response was increased from 14GHz to 15GHz.

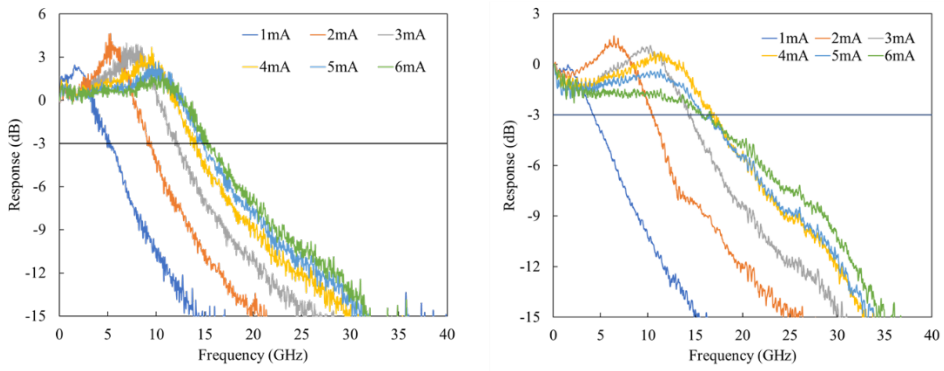


Fig. 4.3.2 Small signal response of devices with large mesa and small mesa

The mesa size was reduced from larger than OA for 20 μm to 10 μm. The mesa parasitic capacitance was smaller due to the decrease of mesa area. The small signal response was improved from 16 GHz to 18GHz at the same operation current.

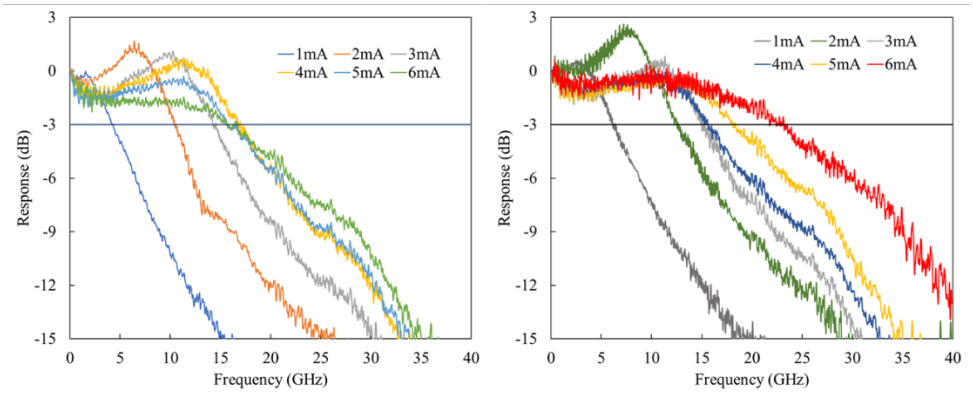


Fig. 4.3.3 Small signal response without and with reducing pad parasitic

The small signal response for devices without and with reducing pad parasitic by increasing the height between p electrode pads and GND were shown in Fig. 4.3.3. Both devices were fabricated on the same wafers with same parameters. Oxidation aperture was 5 μm and diameter of contact metal was 8 μm. Diameter of surface relief was 5 μm and SR depth was 30 nm. By reducing pads parasitics, small signal response was improved from 18GHz to 23GHz.

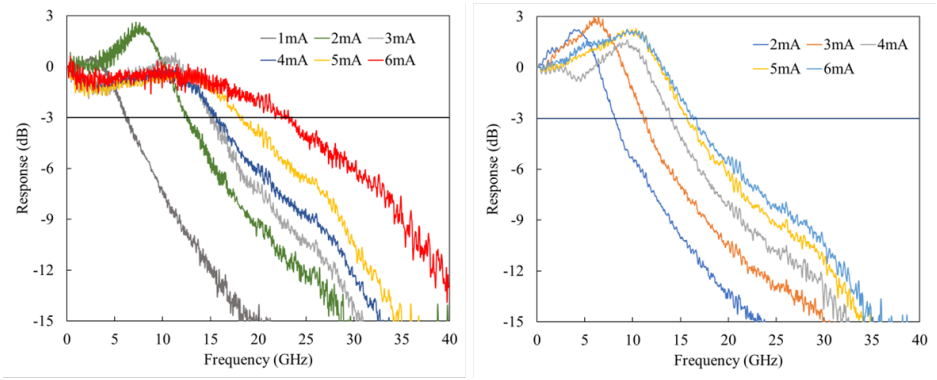


Fig. 4.3.4 Small signal response with and without transverse coupled cavity

The small signal responses for devices with and without transverse coupled cavities are shown in Fig. 4.3.4. Both devices are fabricated on the same wafers using the same layers with thick polyimide, so the improvement solely results from the transverse coupled cavity of the metal-aperture (MA) structure. Owing to the transverse coupled cavity provided by the MA structure,

the 3 dB cutoff frequency (f3dB) increases from 16 GHz to 23 GHz.

The bandwidth enhancement from the transverse coupled cavity and the reduction of parasitic capacitance are evident in Fig. 4.3.5. If the parasitic characteristics caused by the electrode pads can be mitigated through the flip-chip bonding process, we anticipate a further improvement in the small signal response.

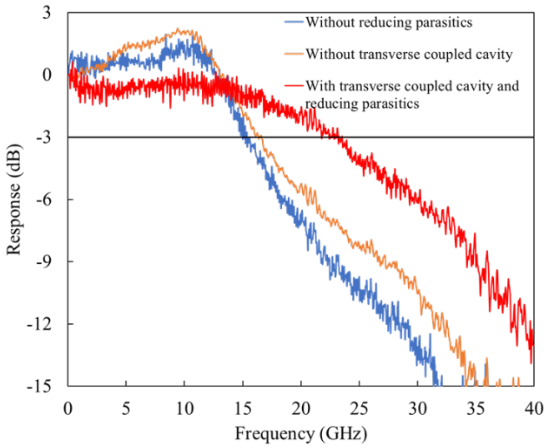


Fig. 4.3.5 Bandwidth enhancement with transverse coupled cavity and reducing parasitics

4.4 Large signal measurement

A total transmission capacity of 400 Gbps by utilizing 25 Gbps per channel across 16 channels was the target in this study. For large signal measurements, a signal with a pseudorandom bit sequence of 2^9-1 word length is generated by the Keysight M8194A 120 GSa/s Arbitrary Waveform Generator (AWG). In this measurement, at the operation current of 6mA, a typical peak-to-peak voltage (Vpp) of the AWG signal required to achieve an extinction ratio of over 4.5 dB without pre-equalization is 190 mV, and after an 11 dB amplifier (SHF M827B), the Vpp increases to 674 mV. The eye pattern is observed using the Keysight DCA-M N1092A.

At 6 mA, 25 Gbps back-to-back eye patterns with an extinction ratio of 5 dB for all 16 channels from VCSEL array without SR were displayed in Fig. 4.4.1. The ILV curves and spectra were shown in chapter 3.4.3. The small signal response was 14GHz. Some channels showed large noise.

The noise came from high order modes, weak transverse coupled cavity, thermal effects and reflection of the test system. The channels with good eye pattern quality were shown in red. The uniformity based on the quality of eye pattern was 9/16.

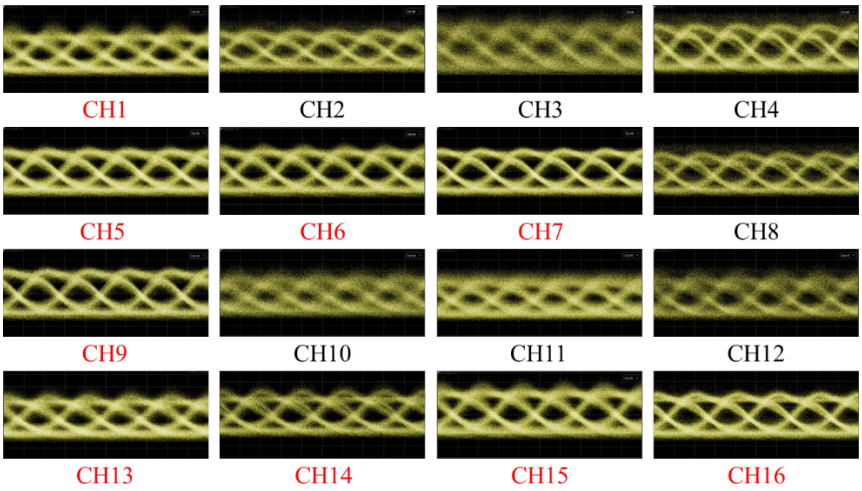


Fig. 4.4.1 16-ch 25Gbps eye pattern of VCSEL array without SR

At 6 mA, 25 Gbps back-to-back eye patterns with an extinction ratio of 5 dB for all 16 channels from VCSEL array with SR were shown in Fig. 4.4.2. With SR, the VCSEL array demonstrated better SMSR. The small signal response increased to 15GHz. Better transverse coupling provided improved eye pattern quality and uniformity. The channels with good eye pattern quality were shown in red. The uniformity based on the quality of eye pattern was 13/16.

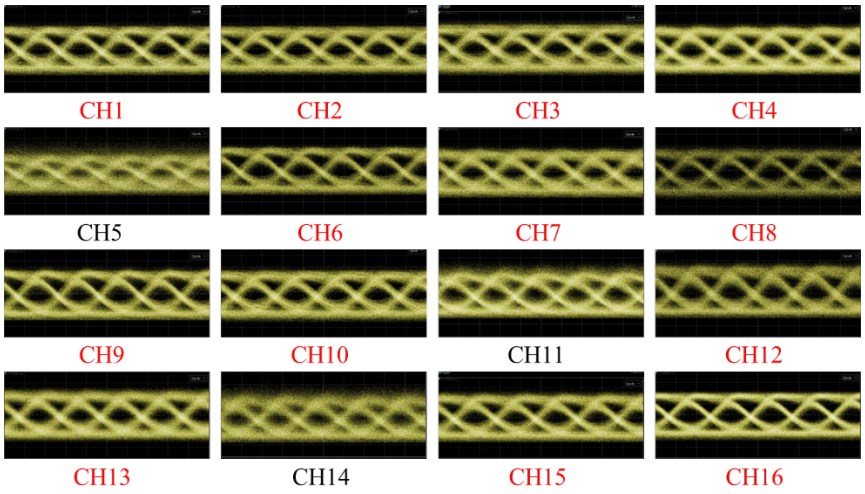


Fig. 4.4.2 16-ch 25Gbps eye pattern of VCSEL array with SR

In this study, the boundaries gap between oxidation aperture and contact metal should be well controlled to provide transverse coupled cavity. By the internal wafer-scale oxidation process, a good OA uniformity was realized which shown a better uniformity of eye pattern quality. At 6 mA, 25 Gbps back-to-back eye patterns with an extinction ratio of 5 dB for all 16 channels from VCSEL array with better OA control were shown in Fig. 4.4.3. The channels with good eye pattern quality were shown in red. The uniformity based on the quality of eye pattern was 14/16.

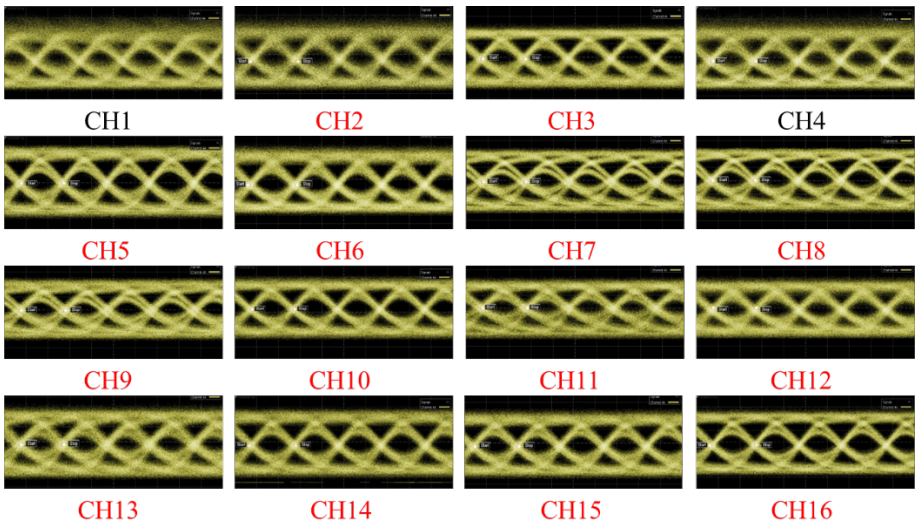


Fig. 4.4.3 16-ch 25Gbps eye pattern of VCSEL array with better OA control

By reducing the parasitics of the mesa, the small signal response was increased to 18GHz. 18GHz was sufficient for the transmission of 25Gpbs signals. At 6mA, when the extinction ratio was 5dB, the eye patterns of 16 channels were shown in Fig. 4.4.4. All channels' eye patterns were open, demonstrating good uniformity. Slight noise appeared in two channels, speculated to be thermal noise from within the device.

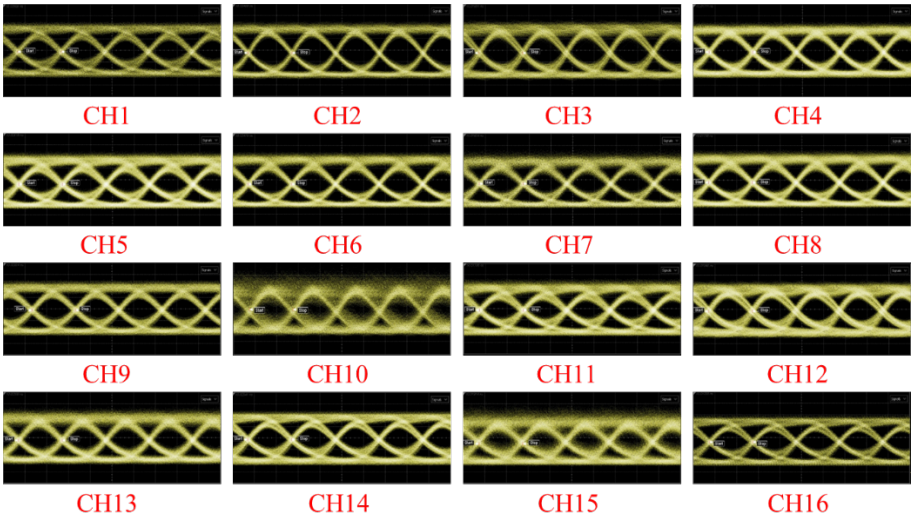


Fig. 4.4.4 16-ch 25Gbps eye pattern of VCSEL array after reducing mesa parasitics

By reducing pad parasitics, the small signal response was increased to 23GHz. At 6mA, when the extinction ratio was 5dB, noiseless 25Gbps eye patterns of 16 channels were shown in Fig. 4.4.5. This was the first time in the world that a total transmission capacity of 400Gbps was achieved based on a high densely integrated 16-channel VCSEL array, which is of great significance.

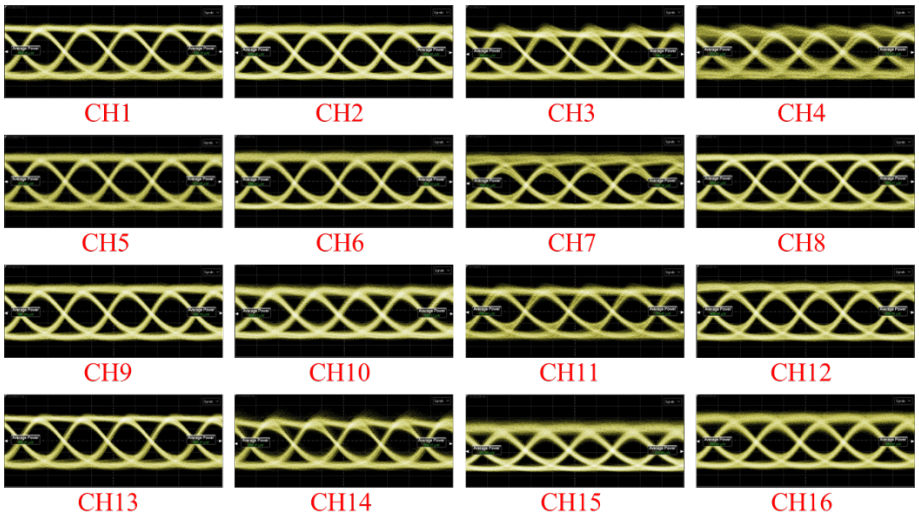


Fig. 4.4.5 16-ch 25Gbps eye pattern of VCSEL array after reducing pad parasitics

One channel in VCSEL array after reducing parasitics was selected to do the large signal measurement for high speed. The eye pattern measured at back-to-back is shown in Fig. 4.4.6. Signal Error Rate (SER) is employed to evaluate signal quality. Without pre-equalization, a high SER of 1e-18 can be achieved at 45 Gbps NRZ, as illustrated in Fig. 4.4.6(a). However, due to the small signal response of 23 GHz, at 50 Gbps NRZ, the SER is reduced to 2e-4, as displayed in Fig. 4.4.6(b). Using a calibration function provided by the AWG, the signal can be pre-equalized with tap numbers of 3 and 5 to achieve a better modulation response. With a tap number of 3, the SER at 50 Gbps NRZ is 5e-8. With a tap number of 5, the SER at 60 Gbps NRZ is 3e-6.

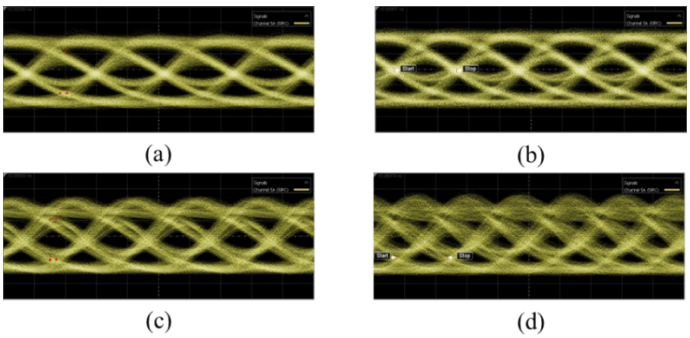


Fig. 4.4.6 NRZ eye pattern at back-to-back (a) 45Gbps without pre-equalization (b) 50Gbps

without pre-equalization (c) 50Gbps with a taps number of 3 (d) 60Gbps with a taps number of 5

For the PAM-4 signal, the eye pattern with and without pre-equalization is shown in Fig. 4.4.7. We observed the eye opening at 60 Gbps without pre-equalization. With pre-equalization, the Transmitter and Dispersion Eye Closure Quaternary (TDECQ) can be measured to evaluate the quality of the PAM-4 eye pattern. With a tap number of 3, the TDECQ is 3.3 dB, as shown in Fig. 4.4.7(b). With a tap number of 5, the TDECQ is 2.2 dB, as displayed in Fig. 4.4.7(c). Pre-equalization with a tap number of 5 can achieve better signal quality. With a tap number of 5, we observed that the 100 Gbps PAM-4 eye pattern is open. By increasing the bandwidth and reducing noise, we expect a clear 100 Gbps PAM-4 eye pattern in the future.

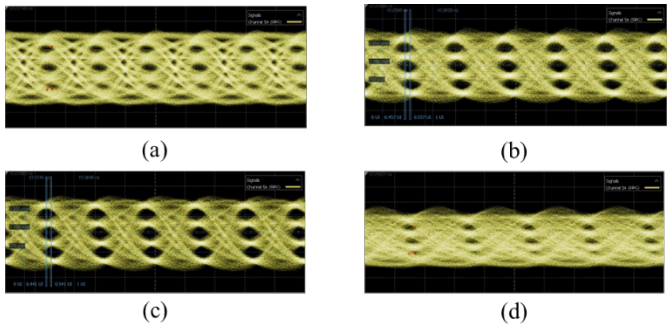


Fig. 4.4.7 PAM-4 eye pattern at back-to-back (a) 60Gbps without pre-equalization; (b) 60Gbps with a taps number of 3; (c) 60Gbps with a taps number of 5; (d) 100Gbps with a taps number of 5.

4.5 Pulse compression

The product of maximum bit rate (B) and the square root of fiber length (L) can be described as a function of the linewidth enhancement factor (α) as follows:

$$BL^{\frac{1}{2}} = \frac{1}{2[2(\alpha^2+1)^{\frac{1}{2}}+2\alpha]|\beta''|^{\frac{1}{2}}} \quad \textbf{(4.5.1)}$$

where B is the maximum bit rate, L is the fiber length, β" is the second derivative of the propagation constant, and α is the linewidth enhancement factor.

When the α-parameter is negative, the product of maximum bit rate (B) and the square root of the fiber length (L) will be higher than without phase modulation. In this case, the negative linewidth enhancement factor leads to an increase in the maximum bit rate and the square root of the fiber length [44][45].

For the single-mode fiber (SMF) transmission, when the wavelength is shorter than 1310 nm, negative dispersion will result in pulse width compression. As a result, bandwidth enhancement after SMF transmission is expected based on the calculation provided in equation (4.5.1). This means that a system with a negative linewidth enhancement factor (α) can potentially achieve higher transmission rates and longer distances when operating at wavelengths shorter than 1310 nm.

The small signal response after a single-mode fiber (SMF) transmission for 2 km and 5 km is measured and shown in Fig 4.5.1(a). The SMF used in this measurement complies with the ITU-T G.652 standard. The experimental and calculated transfer functions for 2 km and 5 km SMF transmissions at 1060 nm are shown in Fig. 4.5.1(b). The α-parameter is assumed to be 2, and the dispersion at 1060 nm is -30 ps/km/nm.

For the 2 km SMF transmission, the 3 dB bandwidth is extended to over 35 GHz, which indicates the potential for 70 Gbps (NRZ) and 140 Gbps (PAM-4) transmission rates. This can meet the requirements of intra-datacenter transmission. For the 5 km SMF transmission, bandwidth enhancement is also observed to be over 30 GHz. The degradation of the 5 km transfer function at higher modulation speeds is caused by frequency chirp.

The frequency chirp can be reduced by optimizing the transverse coupled cavity. After optimization, longer-distance and higher-speed transmissions can be realized. This research highlights the potential of using 1060 nm VCSELs and SMF for high-speed, long-distance

communication, which could significantly benefit intra-datacenter networking applications.

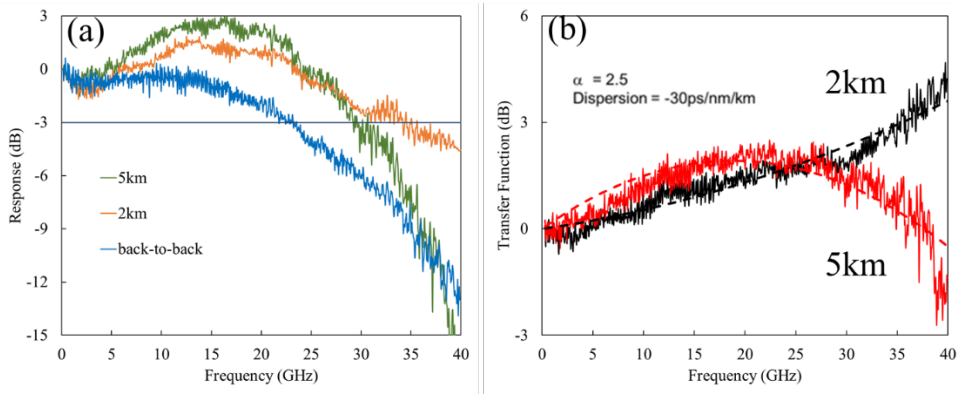


Fig. 4.5.1 (a) Small signal response of back-to-back, after 2km and 5km SMF transmission; (b) Transfer Function for 2km and 5km SMF transmission

The eye patterns after 2 km SMF transmission are shown in Fig. 4.5.2. With pre-equalization applied, for NRZ signal, the eye pattern is open at 70 Gbps with a SER of 1e-6. The product of the bit rate and transmission distance is 140 Gbpskm. For PAM-4 signal, the eye pattern is open at 60 Gbps without pre-equalization, as shown in Fig. 4.5.2(c). With a taps number of 5, an eye open at 90 Gbps PAM-4 is observed, as shown in Fig. 4.5.2 (d). The product of the bit rate and transmission distance is 180 Gbpskm.

These results demonstrate the potential of using 1060 nm VCSELs and SMF for high-speed, long-distance communication. The successful transmission of 70 Gbps NRZ and 90 Gbps PAM-4 signals over 2 km SMF highlights the promise of this technology for future intra-datacenter networking applications. The capability to achieve higher bit rates and longer transmission distances can significantly benefit datacenter performance, supporting the growing demand for high-speed communication systems.

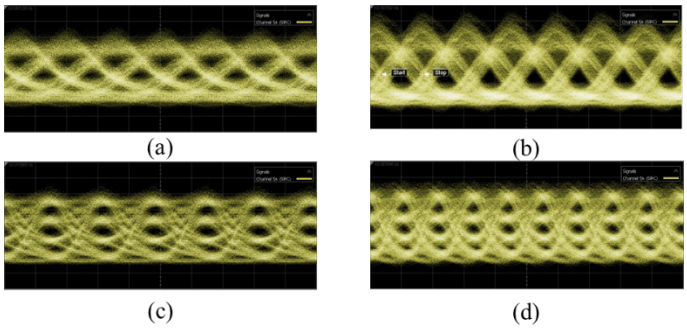


Fig. 4.5.2 Eye pattern after 2km SMF transmission (a) 65Gbps NRZ without pre-equalization; (b) 70Gbps NRZ with pre-equalization; (c) 60Gbps PAM-4 without pre-equalization; (d) 90Gbps PAM-4 with pre-equalization.

The eye patterns after 5 km SMF transmission are shown in Fig. 4.5.3. With pre-equalization applied, for NRZ signal, the eye pattern is open at 60 Gbps with a SER of 5e-5. The product of the bit rate and transmission distance is 300 Gbpskm. For PAM-4 signal, with a taps number of 5, an eye open at 70 Gbps PAM-4 is observed, as shown in Fig. 10(d). The product of the bit rate and transmission distance is 350 Gbpskm.

These results further demonstrate the potential of using 1060 nm VCSELs and SMF for high-speed, long-distance communication. The successful transmission of 60 Gbps NRZ and 70 Gbps PAM-4 signals over 5 km SMF showcases the capability of this technology to address the increasing need for high-speed communication systems in various applications, including datacenter networks and telecommunications. The improvements in bit rates and transmission distances can significantly contribute to enhancing the performance of communication networks, supporting the growing demand for data transmission and connectivity.

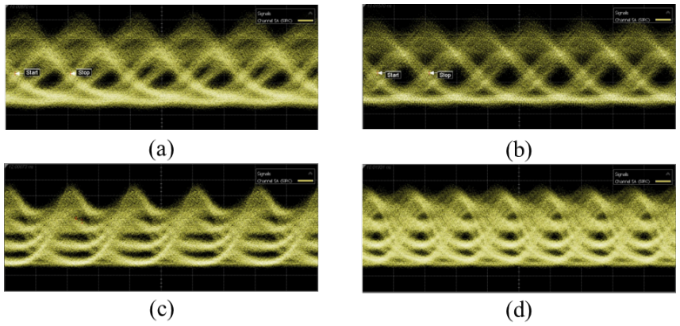


Fig. 4.5.3 Eye pattern after 5km SMF transmission (a) 55Gbps NRZ without pre-equalization; (b) 60Gbps NRZ with pre-equalization; (c) 50Gbps PAM-4 without pre-equalization; (d) 70Gbps PAM-4 with pre-equalization.

In Fig. 4.5.4, the relationship between SER (Symbol Error Ratio) and bit rate under different transmission conditions was shown when transmitting with NRZ signals. It can be seen that, thanks to the enhancement of small signal bandwidth to 23GHz, error-free transmission of 45Gbps can be achieved in back-to-back transmission. By introducing pre-equalization, the SER at higher transmission speeds can be reduced. In this study, it is possible to achieve 55Gbps transmission with low SER over 2km and 50Gbps transmission with low SER over 5km. By relaxing the SER requirements, 70Gbps transmission over 2km and 60Gbps transmission over 5km can be achieved.

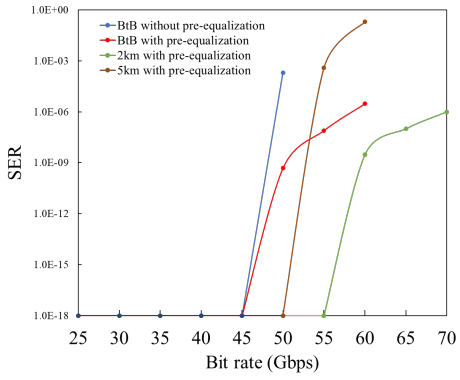


Fig. 4.5.4 SER related to bit rate (NRZ) at BtB, 2km and 5km transmission

Chapter 5 Optical coupling with Multi-core Fiber

5.1 Introduction

In the design for CPO module based on VCSEL array, a MCF instead of multiple single-mode fibers was applied for optical signal transmission.

It was not possible to test all 16 channels of the VCSEL array simultaneously under laboratory conditions. Therefore, the performance testing of the VCSEL array was based on individual testing of each channel. In this study, multi-mode fiber and various singgle-mode fibers were used to couple the light signals generated by the bottom-emitting VCSEL from the bottom side, in order to test the spectrum and signal response. The coupling efficiency of the VCSEL array, after flip-chip bonding, was measured using MCF. The advantages and disadvantages of each fiber type are explained below.

a) Multi-mode fiber

The advantages of multi-mode fibers are that they have a larger core diameter, which facilitates easier coupling and alignment. In this study, core and cladding size for MMF was 62.5/125 μm. MMF was employed in the bottom-emitting spectrum test system to reduce the impact of misalignment on the coupled power caused by the movement of the testing platform. With an aspheric fiberport coupler, at focus, couple efficiency is -3dB.

b) Single-mode fiber (SMF28)

In the initial signal response measurement, a single-mode fiber (SMF28) with an aspheric fiberport coupler was used. The SMF28 fiber complies with the industry standard ITU-T G.652.D. The parameters of SMF28 were shown in Table 5.1.

Table 5.1 Optical characteristics of SMF28

Parameter	Value
Operation Wavelength	1260 - 1625 nm
Mode Field Diameter	9.2 ± 0.4 μm @ 1310 nm 10.4 ± 0.5 μm @ 1550 nm
Cladding	125 ± 0.7 μm
Cut-Off Wavelength	< 1260 nm
Attenuation (Max)	≤0.32 dB/km @ 1310 nm ≤0.18 dB/km @ 1550 nm
NA	0.14

The combination of reflections from the fiber coupler surface, the glass platform surface, and the return loss of the fiber can cause measurement issues in signal response. For example, in small signal testing, fluctuations in the signal response may occur, while in large signal testing, noise may appear in the eye diagram. The schematic of coupling system with fiber coupler is shown in Fig. 5.1.1.

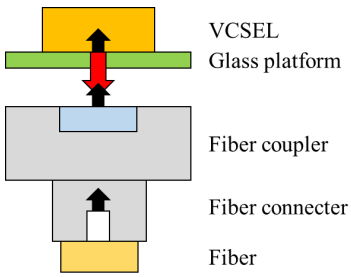


Fig. 5.1.1 Schematic of coupling system with fiber coupler

c) Single-mode fiber with FC/APC connector (SMF28)

To minimize the impact of reflections and return loss from the testing system on the measurement results, optimizations were made to the coupling system.

An anti-reflection (AR) coating film was applied to the surface of the fiber coupler. Additionally, a customized single-mode fiber with an FC/APC connector was used. The single-mode fiber was connected to the fiber coupler using an FC/APC connector on one end. The narrow key connector utilizes a ferrule that has an 8° angle polished tip, ensuring typical return loss of 60 dB. The coupling efficiency was -5dB.

d) Single-mode fiber with aspheric fiber collimators

Using a glass platform and coupling system C provides a convenient way to perform fast testing on the bottom-emitting VCSEL array. However, this fast testing comes at the cost of reduced coupling efficiency and increased reflections and return loss. When conducting detailed testing of signal response, particularly for signal response after transmission through kilometers of single-mode fiber, it is necessary to improve the coupling efficiency of the entire testing system to ensure an adequate optical power for signal quality.

The glass platform was replaced with a metal platform with a center aperture, and single-mode fiber with aspheric fiber collimators was used for directly coupling the optical signals. The coupling efficiency is -4 dB.

e) Multi-core fiber with Fan-in

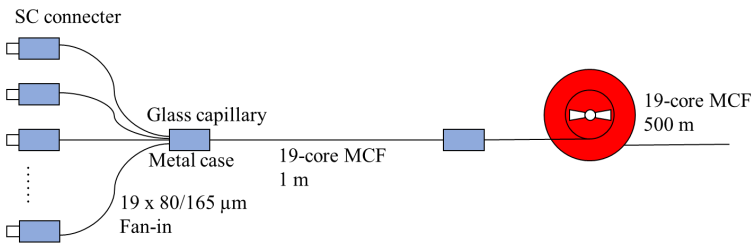


Fig. 5.1.2 Schematic of 19-core MCF with Fan-in

Based on the design of the VCSEL array, a customized 19-core multi-fiber cable (MFC) with a length of 500m was created. This MFC was fused with a 19-core fan-in to separate the 19-core

MFC into 19 individual single-mode fibers for testing the coupling of each channel. The schematic was shown in Fig. 5.1.2. The distance between the cores in the MFC is 40 μm. The MFC was manufactured by Furukawa Electric. The design and manufacturing methods of the MFC can be obtained from Furukawa Electric's publicly available publications [47][48][49].

The parameters of MCF with fan-in in this study is shown in Table 5.1.2.

Table 5.1.2 The parameters of 19-core MCF with fan-in

Parameter	Target value	Real value
Core diameter	5.8 μm	
Cladding diameter	240 ± 1.0 μm	239.5~240.5 μm
MFD (1060nm)	6.5 ± 1.0 μm	6.4~6.7 μm
Cutoff wavelength	<1040 nm	<950 nm
Attenuation (1060nm)	<2 dB/km	0.79~0.81 dB/km
Dispersion (1060nm)	-37 ps/(km*nm)	
Crosstalk in adjacent cores	< -50 dB/km	< -73 dB/km
Insert loss (FI)		< 0.8 dB
Insert loss (MFC+FI)		< 2.3 dB

f) Multi-core fiber with AR coating

To reduce reflection between the substrate and the surface of the 19-core multi-fiber cable (MCF), an anti-reflection (AR) coating was applied to both ends of the MCF. The MCF has a total length of 2 meters. Fig. 5.1.3 shows the two ends of the MCF with AR coating.

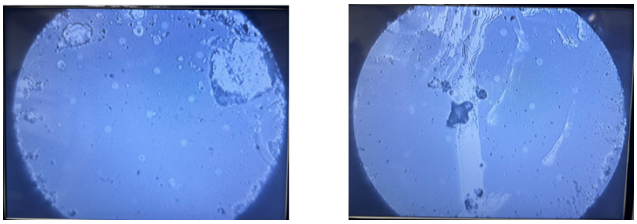


Fig. 5.1.3 Photo of MCF ends with AR coating

In the Fig., it can be observed that the 19 cores in the MCF are arranged in a tightly packed hexagonal pattern. The cladding diameter of the 19-core MCF is only 240 μm, making it challenging to deposit an AR coating film on such a small surface area and maintain quality. The AR coating film can also be susceptible to damage during the testing process. This can have an impact on the coupling efficiency.

5.2 Dicing and flip-chip bonding process

5.2.1 Dicing process

a) Manual dicing: For a single VCSEL array with a side length of 0.9mm, the devices can be diced manually using a surgical blade under a microscope. This method is the simplest, but it has obvious drawbacks as it can easily cause physical damage to the devices.

b) Machine-assisted dicing: For a single VCSEL with a side length smaller than 250um, machine assistance is used for dicing. The machine setup is shown in the Fig.5.2.1. The position of the blade in the horizontal direction is fixed, and the alignment between the sample and the blade is achieved by observing through a microscope. Pressing down the blade completes the dicing process. The drawback of this method is that stress during dicing can cause the devices to be ejected, but this can be mitigated by fixing them with adhesive tape.

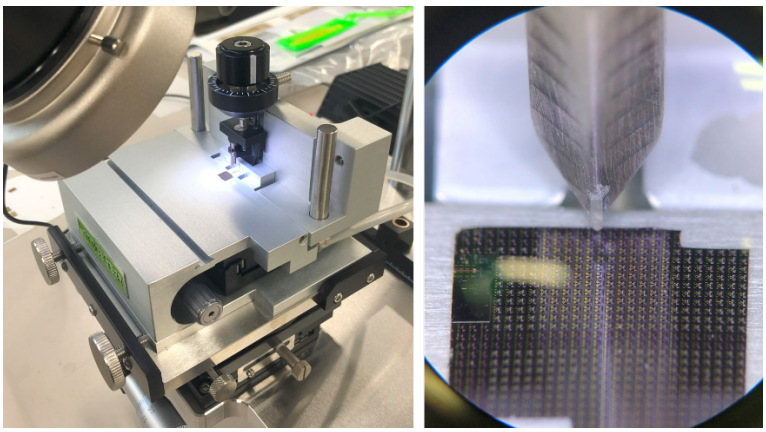


Fig. 5.2.1 Photos of machine-assisted dicing

c) External dicing: The sample typically has a side length of 2cm and contains 400 VCSEL arrays. It is difficult to manually separate them into 400 individual devices. Therefore, the sample is sent to an external factory for dicing. The diced VCSEL arrays will be sequentially fixed on adhesive tape. The desired devices can then be selected for subsequent flip-chip bonding.

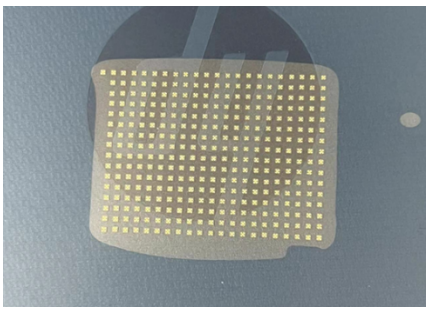


Fig. 5.2.2 VCSEL arrays after external dicing

5.2.2 Flip-chip bonding process

a) Internal flip-chip bonding process

The internal flip-chip bonding process is carried out using a manual die bonder produced by Finetech.

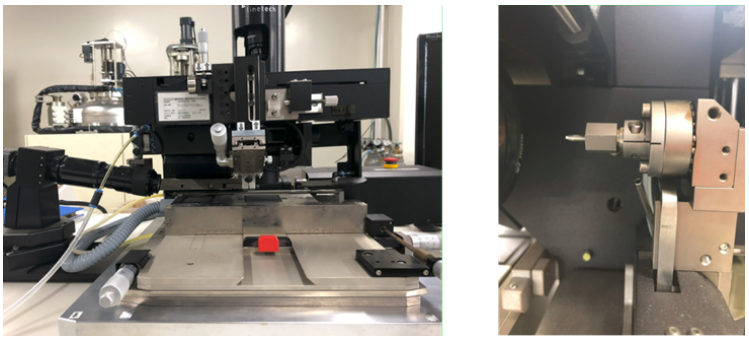


Fig. 5.2.3 Flip-chip bonder

The process can be divided into the following steps:

i) Place the VCSEL array upside down on the heater and adjust its position. Then, using the suction tool shown in the Fig., change the orientation of the VCSEL array from a horizontal position to a vertical position. Verify the orientation of the VCSEL array by observing it through the imaging system.

ii) Place the carrier in the correct orientation on the heater. Using the half-mirror beam splitter in the observation system, align the image of the VCSEL array with the image of the carrier, allowing for easy alignment.

iii) Lower the suction tool to bring the VCSEL array into contact with the carrier. Apply a force of 1N and heat the heater to 180 degrees Celsius. Maintain this temperature and pressure for 3 minutes to complete the internal flip-chip bonding process.

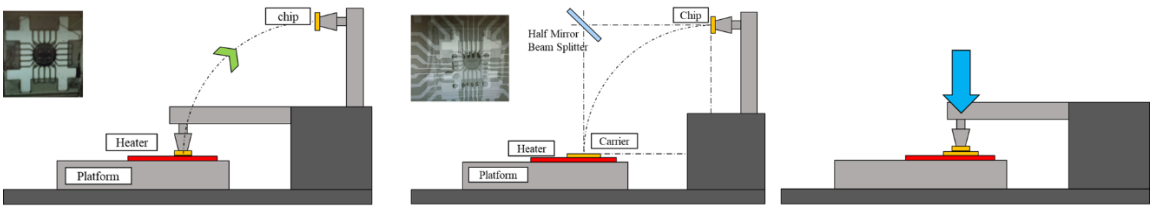


Fig. 5.2.4 Schematic of flip-chip bonding process

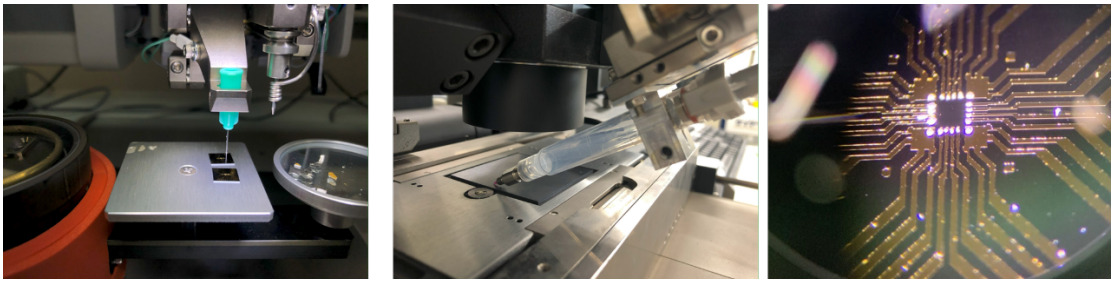


Fig. 5.2.5 Bumps for flip-chip bonding

In the internal flip-chip bonding process, a conductive die-bonding paste was used as the material for bumps. The paste is provided by Panasonic CONNECT and its model number is DBC138SG. It can cure at low temperatures (100-180 degrees Celsius) to minimize the impact on the devices caused by high temperatures. Two methods were attempted to apply the paste on the carrier. The first method involved using a needle to pick up an appropriate amount of paste under a microscope and transfer it onto the carrier. This method requires a lot of practice, but it allows for precise control of the bump size. The second method involved applying the paste from the syringe onto the carrier using air pressure. By adjusting the air pressure, the size of the bumps can be accurately controlled. The carrier with applied bumps is shown in the Fig.5.2.5.

5.3 Calculation theory of coupling efficiency for Gaussian beams

The low-loss coupling between VCSEL array and MCF is very important for their application in CPO transceiver especially for realize high product of transmission speed and fiber length.

The coupling between VCSEL and MCF can be considered as the coupling of Gaussian beams [50]. The schematic of coupling between VCSEL and MCF is shown in Fig. 5.3.1.

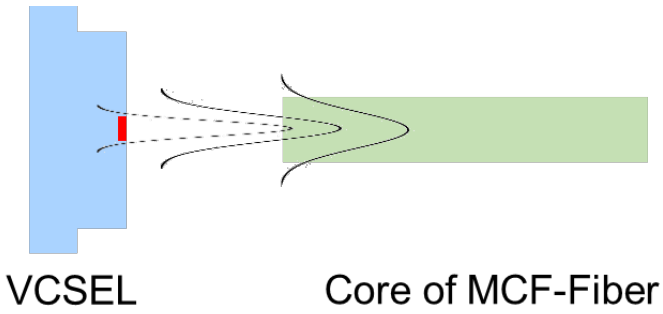


Fig. 5.3.1 Schematic of coupling between VCSEL and MCF

In the free space, an m order Gaussian beam in the x-direction and an n order in the y-direction are represented by the equation below:

$$\boldsymbol{TEM_{mn} = f_m(x)g_n(y)} \tag{5.3.1}$$

Here,

$$\boldsymbol{f_m(x) = \left(\sqrt{\frac{2}{\pi}}\frac{1}{w(z)2^m m!}\right)^{\frac{1}{2}} H_m\left(\frac{x}{w(z)}\sqrt{2}\right) exp\left(-\frac{x^2}{w^2(z)} - jk\frac{x^2}{2R(z)}\right)} \tag{5.3.2}$$

$$\boldsymbol{g_n(y) = \left(\sqrt{\frac{2}{\pi}}\frac{1}{w(z)2^n n!}\right)^{\frac{1}{2}} H_n\left(\frac{y}{w(z)}\sqrt{2}\right) exp\left(-\frac{y^2}{w^2(z)} - jk\frac{y^2}{2R(z)}\right)} \tag{5.3.3}$$

Where k is wave number, w(z) is the spot size related to z and R(z) is the radius of curvature related to z. To avoid affecting the subsequent discussion, the phase term in the z-axis direction has been omitted.

Assuming that the incident mode is of m1 order in the x-direction and n1 order in the y-direction, then

$$\boldsymbol{incident\ field = \emptyset_{m1}(x)\emptyset_{n1}(y)} \tag{5.3.4}$$

When this incident field is incident on a receiving system, such as an optical fiber, it can be expanded into the eigenmodes of the receiving system as shown in the following equation:

$$\boldsymbol{\emptyset_{m1}(x)\emptyset_{n1}(y) = \sum_{m2=0}\sum_{n2=0} C_{m1n1m2n2}\,\psi_{m2}(x)\ \psi_{n2}(y)} \tag{5.3.5}$$

Here, the subscripts 1 and 2 are used to represent the incident system and the receiving system, respectively. Cm1n1m2n2 represents the expansion coefficient associated with the (m2,n2) mode

in the receiving system when expanding the Gaussian beam with mode numbers (m1,n1) in the x and y directions using the eigenfunctions of the receiving system. The coupling efficiency from the (m1,n1) mode to the (m2,n2) mode is expressed as the square of the absolute value of this coefficient:

$$|C_{m1n1m2n2}|^2 = C_{m1n1m2n2}C^*_{m1n1m2n2} = |c_{m1m2}|^2|c_{n1n2}|^2 \quad \textbf{(5.3.6)}$$

Here

$$c_{m1m2} =< \psi_{m2}(x)|\emptyset_{m1}(x) > \quad \textbf{(5.3.7)}$$

$$c_{n1n2} =< \psi_{n2}(x)|\emptyset_{n1}(x) > \quad \textbf{(5.3.8)}$$

It means that when the system has the separation of variables in the x and y coordinates as shown in equation (5.3.1), the coupling efficiency $|C_{m1n1m2n2}|^2$ between the (m1,n1) mode of the incident system and the (m2,n2) mode of the receiving system can be obtained by separately calculating the x-direction component $|c_{m1m2}|^2$ and the y-direction component $|c_{n1n2}|^2$ and then taking their product.

For the coupling of single-mode VCSEL and single-mode MCF, the coupling efficacy was considered as the 0 order Gaussian beam. Consider the coupling of zero-order Gaussian beams with only different spot sizes, assuming no axial displacement or angular displacement. For the wave functions ψ1(x) of the incident system and ψ2(x) of the receiving system, on the surface where they are coupled, the curvature radius of the wavefront is infinite, and can be expressed by the following equation:

$$\psi_i(x) = \left(\sqrt{\frac{2}{\pi}}\frac{1}{w_i}\right)^{\frac{1}{2}} exp\left(-\frac{x^2}{w_i^2}\right) \ (i = 1, 2) \quad \textbf{(5.3.9)}$$

In this case, coupling efficiency can be calculated by equation (5.3.6) as

$$\eta = |c_{00}|^2 = \frac{4}{(\frac{w_1}{w_2}+\frac{w_2}{w_1})^2} \quad \textbf{(5.3.10)}$$

Considering the coupling case where an incident Gaussian beam with a spot size of w_1 is coupled to a receiving system with a spot size of w_2, with a displacement in the direction of the

optical axis z, a displacement in the direction perpendicular to the optical axis x, and an angular displacement θ, the coupling efficiency can be calculated as:

$$\boldsymbol{\eta = \kappa \exp[-\kappa \left\{ \frac{x^2}{2} \left(\frac{1}{w_1^2} + \frac{1}{w_2^2} \right) + \frac{\pi^2 \theta^2}{2\lambda^2} \left(w_1^2(z) + w_2^2 \right) - x\theta \frac{z}{w_1^2} \right\}]} \quad \textbf{(5.3.11)}$$

here

$$\boldsymbol{\kappa = \kappa_x \kappa_y = \frac{4}{(\frac{w_1}{w_2} + \frac{w_2}{w_1})^2 + (\frac{\lambda z}{\pi w_1 w_2})^2}} \quad \textbf{(5.3.12)}$$

$$\boldsymbol{w_1(z) = w_1 \sqrt{1 + (\frac{\lambda z}{\pi w_1^2})^2}} \quad \textbf{(5.3.13)}$$

Introducing the refractive index of the space between VCSEL and MCF into the equation, the coupling efficiency is shown in:

$$\boldsymbol{\eta_n = \kappa \exp[-\kappa \left\{ \frac{x^2}{2} \left(\frac{1}{w_1^2} + \frac{1}{w_2^2} \right) + \frac{\pi^2 \theta^2 n^2}{2\lambda^2} \left(w_1^2(z) + w_2^2 \right) - x\theta \frac{z}{w_1^2} \right\}]} \quad \textbf{(5.3.14)}$$

here

$$\boldsymbol{\kappa = \frac{4}{(\frac{w_1}{w_2} + \frac{w_2}{w_1})^2 + (\frac{\lambda z}{\pi n w_1 w_2})^2}} \quad \textbf{(5.3.15)}$$

$$\boldsymbol{w_1(z) = w_1 \sqrt{1 + (\frac{\lambda z}{\pi n w_1^2})^2}} \quad \textbf{(5.3.16)}$$

where η_n is the coupling loss, x is the position misalignment and θ is the angle misalignment. z is the space between VCSEL and fiber. λ is the operating wavelength and n is the refractive index of space between VCSEL and fiber. w_1 and w_2 are the spot size. The spot size is the radius of the laser beam at $\frac{1}{e^2}$ (13.5%) of the peak intensity.

$$\boldsymbol{w_1 = \frac{MFD(VCSEL)}{2}} \quad \textbf{(5.3.17)}$$

$$\boldsymbol{w_2 = \frac{MFD(MCF)}{2}} \quad \textbf{(5.3.18)}$$

5.4 Coupling of bottom emitting VCSEL with MCF

Considering about the coupling between bottom emitting VCSEL and MCF, the parameters

used for the calculation is shown in Table. 5.4.1.

Table 5.4.1 Parameters in the coupling of VCSEL and MCF

Parameter	Values
MFD of MCF	6.5 μm
Refractive index of GaAs	3.5
Wavelength	1060 nm

In Fig. 5.4.1, the calculated coupling loss related to different VCSEL MFD and different thickness of substrate without position and angle misalignments. The surface of MCF end was contacted with substrate bottom surface. In this case, the equation (5.3.14) is simplified as

$$\eta_n = \frac{4}{(\frac{w_1}{w_2}+\frac{w_2}{w_1})^2+(\frac{\lambda z}{\pi n w_1 w_2})^2} \tag{5.3.19}$$

where z was the thickness of substrate.

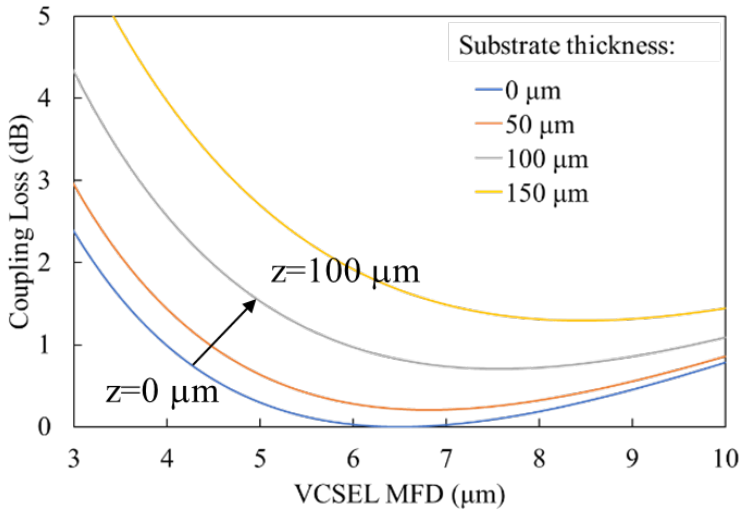


Fig. 5.4.1 Coupling loss related to VCSEL MFD and substrate thickness

Before the flip-chip bonding process, the bottom emitting VCSEL array underwent substrate

polishing, followed by the deposition of an AR-coating film. Thinning the substrate was done to reduce light absorption by the substrate, while the AR-coating was applied to minimize reflections from the bottom surface. Based on the calculation result, if the substrate was totally removed, the coupling efficiency was nearly 0 dB when the MFD of VCSEL was over 6 μm.

In this study, the thickness of substrate is 100 μm. In this case, a high coupling efficiency below 1 dB can be obtained when the MFD of VCSEL was over 7 μm. Benefit from the transverse coupled cavity, single-mode operation can be realized for large oxidation aperture. Based on the experience of the relationship between MFD and oxidation aperture of VCSEL, the oxidation aperture is 1 μm larger than MFD. It means a single-mode bottom emitting VCSEL array with oxidation aperture at 8 μm can realize high coupling efficiency for the direct coupling with MCF.

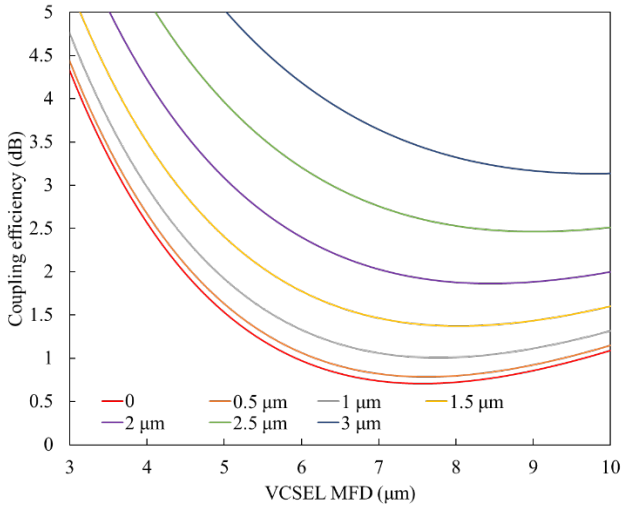


Fig. 5.4.2 Coupling efficiency related to VCSEL MFD and position misalignment

In Fig. 5.4.2, the calculated coupling loss related to different VCSEL MFD and position misalignment without angle misalignments. The surface of MCF end was contacted with substrate bottom surface. The thickness of substrate is 100 μm. In this case, the equation (5.3.14) is simplified as

$$\eta_n = \kappa \exp\left[-\kappa\left\{\frac{x^2}{2}\left(\frac{1}{w_1^2}+\frac{1}{w_2^2}\right)\right\}\right] \tag{5.3.20}$$

Based on the design of the VCSEL array oxidation aperture, the VCSEL MFD was set to 4 μm and 6 μm. Through calculations, it was possible to obtain the coupling loss when position misalignment was introduced during the coupling process. Taking an increase of -3dB in coupling loss compared to the case with no position misalignment as a reference, the misalignment tolerance could be determined. The VCSEL with a larger oxidation aperture exhibited better misalignment tolerance. When the VCSEL's MFD was 6 μm, the misalignment tolerance was 2.9 μm. When the VCSEL's MFD was 4 μm, the misalignment tolerance was 2.7 μm.

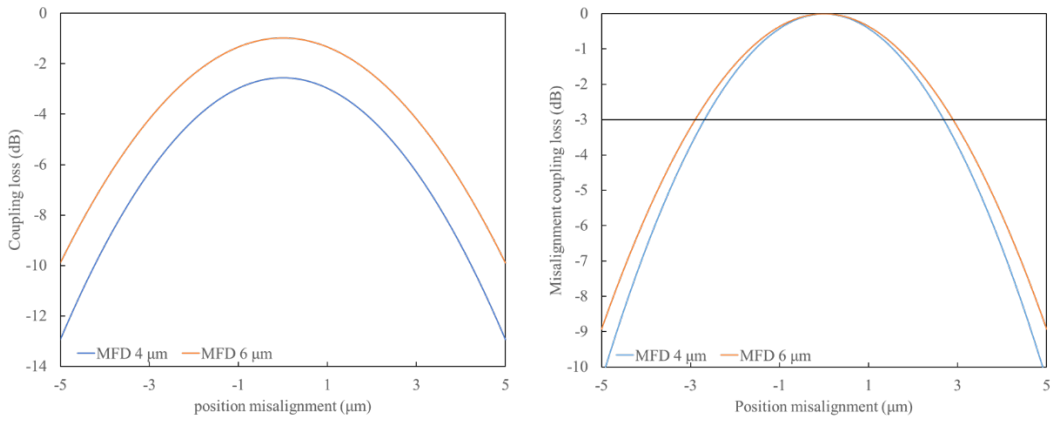


Fig. 5.4.3 position misalignment and tolerance

When angle misalignment was introduced during the coupling process without position misalignment, the equation (5.3.14) was simplified as

$$\eta_n = \kappa \exp[-\kappa \left\{ \frac{\pi^2 \theta^2 n^2}{2\lambda^2} \left(w_1^2(z) + w_2^2 \right) \right\}] \tag{5.3.21}$$

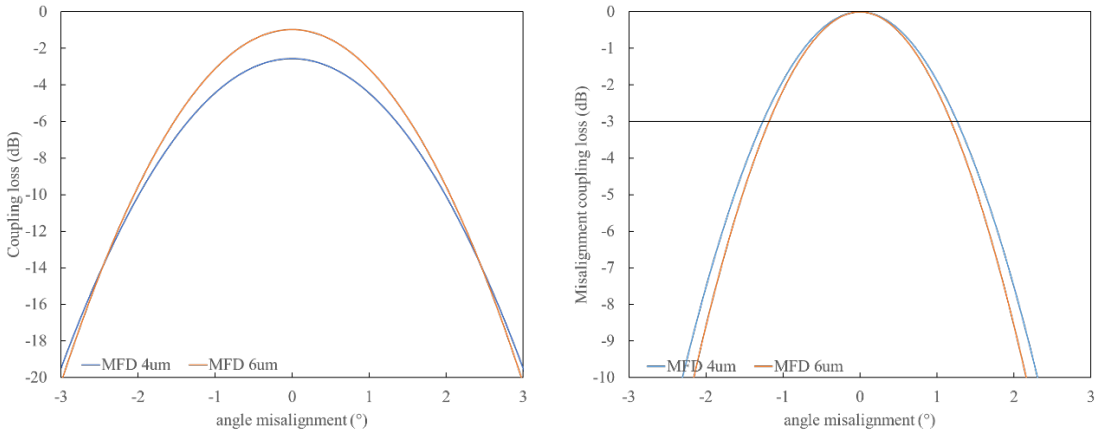


Fig. 5.4.4 Angle misalignment and tolerance

Through calculations, it was possible to obtain the coupling loss when angle misalignment was introduced during the coupling process. Using an increase of -3dB in coupling loss compared to the case with no angle misalignment as a benchmark, the misalignment tolerance could be determined. The VCSEL with a smaller oxidation aperture exhibited better angle misalignment tolerance. When the VCSEL's MFD was 6 μm, the misalignment tolerance was 1.2 degrees. When the VCSEL's MFD was 4 μm, the misalignment tolerance was 1.3 degrees.

5.5 Coupling of MCF with Fan-in

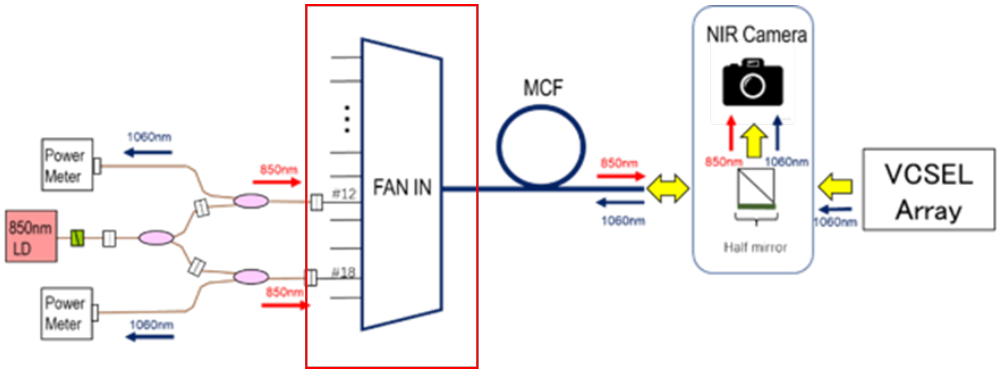


Fig. 5.5.1 Schematic of coupling system for MCF with Fan-in

The schematic of coupling system for MCF with fan-in was shown in Fig. 5.5.1. In this study,

coupling tests were conducted between two channels in the VCSEL array and their corresponding channels in the MCF. In order to reduce the difficulty in locating the coupling position, the single fiber after fan-in was spectrally decomposed again, and a new laser source was introduced. When performing the coupling test, the two channels of the VCSEL array were driven first. The position of the two light spots was observed by the NIR camera after the beam passed through the 45° half-mirror. Subsequently, the laser source was turned on, and light entered the 45° half-mirror from two cores of the MCF. At this time, the positions of the two channels of the VCSEL array and the corresponding two cores of the MCF could be observed from the NIR camera shown in Fig. 5.5.2. After adjusting the light spots to overlap, the half-mirror was removed. Then, the coupling test could be conducted by adjusting the position of the MCF. Using this method significantly reduced the difficulty of locating the corresponding positions and improved the efficiency of the test.

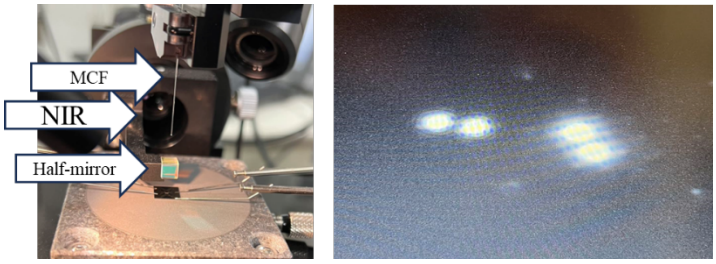


Fig. 5.5.2 Set-up of coupling and NIR image

The CH11 and CH15 with the space of 40 μm in VCSEL array were used for coupling test. The IL curve of CH11 and CH15 was shown in Fig. 5.5.3. The slope efficiency for CH15 was 0.18W/A. The slope efficiency for CH11 was 0.14 W/A. The AR coating was fine after dicing and flip-chip bonding process.

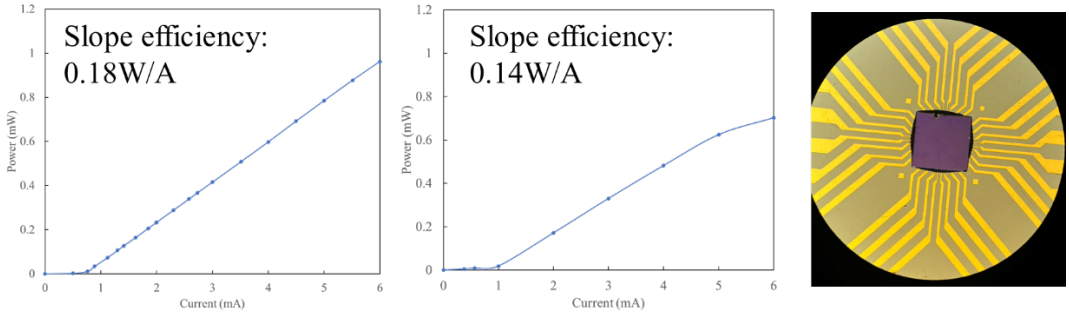


Fig. 5.5.3 IL curve of CH15 (Left) and CH11 (Center); Photo of back-side with AR-coating

The power of CH11 and CH15 at 2mA, 4mA and 6mA were shown in Table 5.5.1 and 5.5.2.

Table 5.5.1 Power of CH15

Current	**Power(mW)**	**Power(dBm)**
2mA	0.234	-6.30
4mA	0.598	-2.23
6mA	0.963	-0.17

Table 5.5.2 Power of CH11

Current	**Power(mW)**	**Power(dBm)**
2mA	0.171	-7.6
4mA	0.482	-3.15
6mA	0.702	-1.52

The NFP and FFP of CH15 at 2mA, 4mA and 6mA was shown in Fig. 5.5.4. The decrease of FFP benefited from the suppression of high order mode by transverse coupled cavity. CH11 and CH15 were from same VCSEL array. The NFP and FFP was similar.

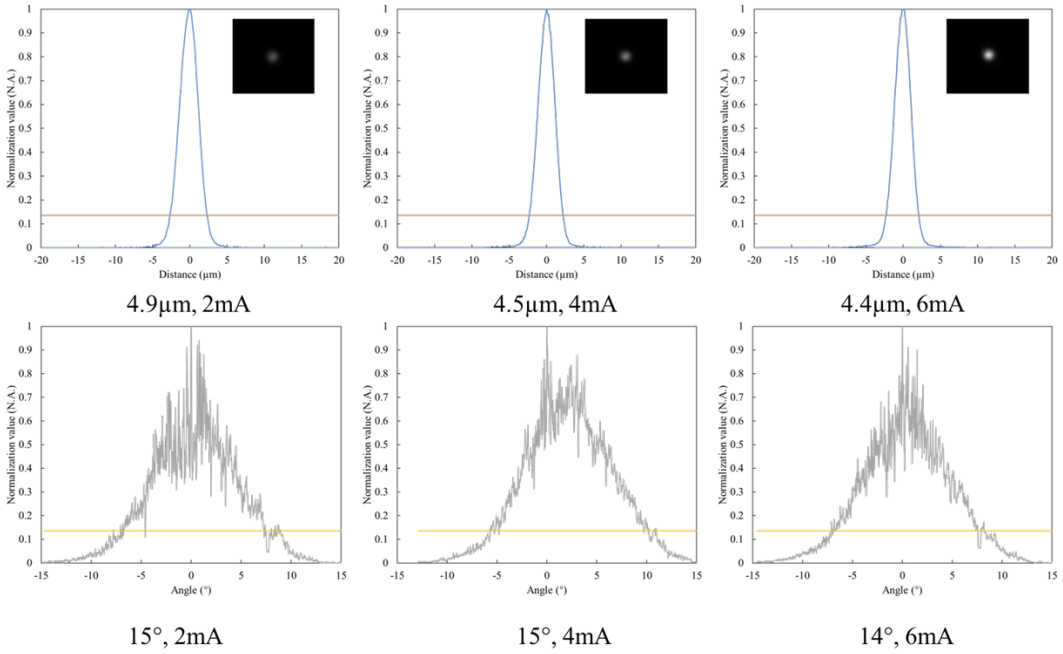


Fig. 5.5.4 NFP and FFP of CH15

The calculation and experiment results for CH15 and CH11 were show in Table 5.5.3 and 5.5.4.

Table 5.5.3 Calculation and experiment results for CH15

Current(mA)	**NFP(μm)**	**Calculated CE(dB)**	**Power(dBm)**	**Coupled power(dBm)**	**Experimental CE(dB)**	**Extra Coupling Loss(dB)**
2	4.9	**1.61**	-6.30	-14.26	**7.96**	4.05
4	4.5	**1.97**	-2.23	-11.31	**9.08**	4.81
6	4.4	**2.08**	-0.17	-8.47	**8.3**	3.92

Table 5.5.4 Calculation and experiment results for CH11

Current(mA)	**NFP(μm)**	**Calculated CE(dB)**	**Power(dBm)**	**Coupled power(dBm)**	**Experimental CE(dB)**	**Extra Coupling Loss(dB)**

2	4.9	**1.61**	-7.6	-15.47	**7.87**	3.96
4	4.7	**1.78**	-3.15	-11.86	**8.71**	4.63
6	4.6	**1.88**	-1.52	-9.69	**8.17**	3.99

By comparing the experimental results of CH11 and CH15, it can be concluded that the coupling between the VCSEL array and the MCF has good consistency in coupling efficiency. Crosstalk was tested. When the driving current of CH11 was changed, the coupling efficiency of CH15 remained unchanged, which was consistent with the parameters of the MCF. There was a significant difference between the experimental results and the calculated results. After excluding the common insertion losses of MCF and Fan-in, compared with the calculated results, the experimental results showed an additional coupling loss of 4dB. The sources of the additional coupling loss included the fiber connector, surface damage to the MCF, reflections from the coupling system, and so on.

5.6 Coupling of MCF with AR-coating

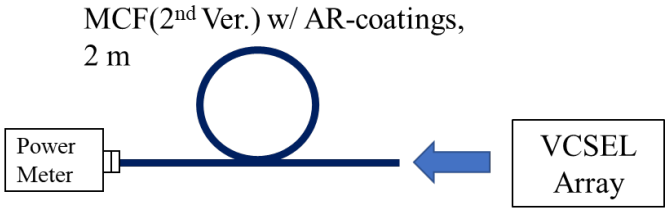


Fig. 5.6.1 Schematic of coupling system for MCF with AR-coating

In order to determine the source of the additional coupling loss, the complexity of the coupling system was reduced. The new coupling system, as shown in the Fig. 5.6.1, was used for testing the coupling of a single channel. A 2m-long MCF was custom made, and

the surfaces at both ends of the MCF were coated with AR coating. The calculation and experiment results of CH15 were shown in Table. 5.6.1.

Table 5.6.1 Calculation and experiment results of CH15

Current(mA)	NFP(μm)	Calculated CE(dB)	Power(dBm)	Coupled power(dBm)	Experimental CE(dB)	Extra Coupling Loss(dB)
2	4.9	1.61	-6.30	-9.75	3.45	1.84
4	4.5	1.97	-2.23	-5.75	3.52	1.97
6	4.4	2.08	-0.17	-3.65	3.48	1.40

By reducing the complexity and reflection of the coupling system, the additional coupling loss was reduced to below 2dB, reaching a minimum of 1.4dB. Comparing with the result of 5.5, it can be concluded that the additional coupling loss caused by reflections and connectors, etc., was 2.5dB.

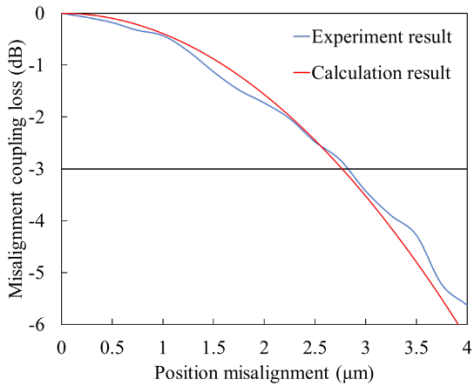


Fig. 5.6.2 Calculation and experiment results with position misalignment

Position misalignment was introduced and its effect on the coupling result was analyzed. Fig. 5.6.2 shows the calculated coupling loss caused by position misalignment when the MFD of the VCSEL is 4.9 μm, and the experimental value of the coupling loss at 2mA. The misalignment tolerance was 2.7 μm. The experimental results are consistent

with the calculated results, proving the correctness of the calculation. There are still some factors in the coupling system that affect the coupling efficiency. It should be noted that, under laboratory conditions, it is difficult to achieve precise alignment of the VCSEL array and the MCF. Dust floating in the air and dirt adhering to the surfaces of the VCSEL array and MCF can cause a rapid decline in coupling efficiency. Under ideal conditions, experimental results should be consistent with calculated results. It is entirely possible for the VCSEL array and MCF to achieve high coupling efficiency through direct coupling.

Chapter 6 Conclusion and future prospect

6.1 Future prospect

a) Commercial CPO module based on VCSEL array

In this study, a high densely integrated 16-channel bottom emitting 1060nm VCSEL array with a transverse coupled cavity was proposed and demonstrated for the first time. A total transmission capacity of 400Gbps NRZ was achieved, reaching a rate density ratio of 2.5Tbps/mm^2. By utilizing SDM technology, ultra-high density optical signal transmission can be achieved through coupling with MCF. The VCSEL array proposed in this paper can achieve single-mode output under a large oxidation aperture. The MCF was also designed for single-mode transmission. By matching the mode field diameter of the VCSEL array with MCF, high coupling efficiency direct coupling can be achieved, greatly reducing packaging difficulty and cost. This is impossible in traditional VCSEL with MMF and SMF links. With single-mode transmission and low transmission loss at 1060nm, high-speed signal transmission over 2km can be achieved. The bottom emitting VCSEL array is integrated through a flip-chip bonding process, which can reduce the transmission distance of the electrical signal, suppress parasitics, and further enhance the modulation bandwidth.

This VCSEL array is expected to be used for the commercial application of CPO modules. Based on Beyond 5G NICT project, the optical transceiver based on this VCSEL array has the world's smallest footprint, only 7.7mm. The total power consumption will be less than 4pj/bit. As can be seen from Fig. 6.1, the CPO module based on VCSEL has a significant advantage in low power consumption.

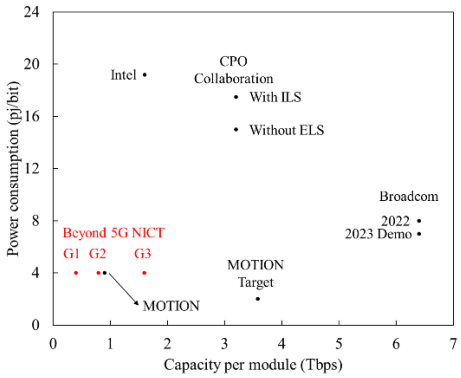


Fig. 6.1 The position of this study and other commercial works

b) Towards over 1Tbps Co-packaged optics

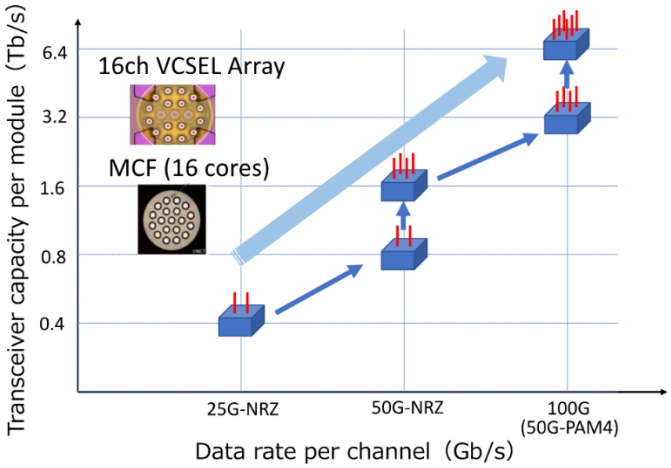


Fig. 6.2 Transmission capacity of VCSEL array with MCF

In the first step of this study, a 16-ch VCSEL array and a 16-ch PD were integrated into a single CPO module. The total capacity was 0.4Tbps by realizing 25Gbps NRZ transmission per channel.

In the second step, a total capacity of 0.8Tbps was expected by realizing 50Gbps NRZ transmission per channel and a total capacity of 1.6Tbps was expected by realizing 100Gbps PAM-4 transmission per channel.

In the third step, by integrating more VCSEL arrays into one CPO module, the total

capacity can be double and more.

Based on the precious results [51], the IM response of DTCC-VCSEL can be over 115GHz. However, in the real situation, it still meets the problems for 100Gbps transmission. The following work is to find the transverse coupled cavity structure with stronger coupling and optimize the coupled cavity length for better improvement. Meanwhile, the stability of bandwidth enhancement and control of mode field diameter for better coupling with multi-core fiber should be considered.

c) Towards high-speed long-distance transmission

As the scale of data centers expands, a single short-distance high-speed modulation is already difficult to meet the demand. Achieving a high speed-distance product becomes more meaningful. The speed-distance product of the traditional 850nm VCSEL and MMF link is only 10Gbps*km. Fig. 6.3 lists the comparison of this study with other research based on VCSEL. It can be seen that the single mode 1060nm VCSEL array has a clear advantage in transmission distance. The speed-distance product also far exceeds other studies.

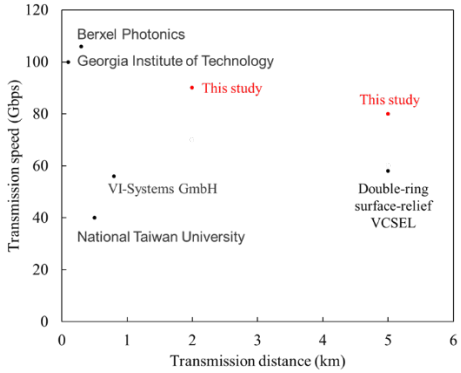


Fig. 6.3 The position of this study and other works on VCSEL

6.2 Conclusions

◆ **VCSEL for Co-packaged optics**

- CPO is an attractive solution for optical transceiver in next-generation communication system due to high-density and low power consumption.
- VCSEL is a better optical resource for CPO due to high-speed, low power consumption, small footprint, low cost, wafer-scale test, easy fabrication into array and circle beam.

◆ **Design of VCSEL arrays for co-packaged optics**

- A densely integrated 16-channel bottom emitting VCSEL array was demonstrated at 1060 nm-band for single-mode multi-core fiber transmission.
- The space between each adjacent channel is 40 μm. The core-size of VCSEL array and electrode pads is 400 μm. The total pitch size of array chip is 900 μm.

◆ **Structure and characterization of 1060nm VCSEL arrays**

- Transverse coupled cavity can be formed when the boundary gap of oxidation aperture and contact metal is 0.5-1.5 μm.
- Transverse coupled cavity can realize single-mode operation for large oxidation aperture devices due to Vernier effects.
- Detuning of the resonant wavelength between the region with surface relief and without surface relief gives a better SMSR.
- For bottom emitting VCSEL array, with 5 μm oxidation aperture, the typical output power is 2.5-3.5 mW. The threshold current is 0.6-0.8 mA. Single-mode operation can be obtained at whole current range. All channels show good single-mode operation uniformity.

- The total thermal crosstalk of top emitting VCSEL at 5mA is 7K. For bottom emitting VCSEL, at 6mA, total thermal crosstalk is 18K.

◆ **High speed modulation characteristics**

- With transverse coupled cavity, surface-relief and reducing parasitic, small signal response at 6mA is 23 GHz.
- At 6mA, when the extinction ratio was 5dB, noiseless 25Gbps eye patterns of 16 channels were demonstrated. This was the first time in the world that a total transmission capacity of 400Gbps was achieved based on a high densely integrated 16-channel VCSEL array, which is of great significance.
- Without pre-equalization, at back-to-back, SER for 50Gbps NRZ is 2e-4. With pre-equalization, SER for 60Gbps NRZ is 3e-6. TDECQ for 60Gbps PAM4 is 2.2dB.
- Pulse Compression with negative fiber dispersion and frequency chirp realizes bandwidth enhancement. After 2km fiber transmission, with pre-equalization, SER for 70Gbps NRZ is 1e-7 and eye pattern were open at 90Gbps PAM-4.
- After 5km fiber transmission, with pre-equalization, eye pattern for 60Gbps NRZ and 80Gbps PAM-4 were open. The transmission distance of 5km was realized.

◆ **Optical coupling with MCF**

- 19-core SM-MCF was fabricated. The space between adjacent cores was 40 μm. The diameter of MCF was 220 μm. The MFD at 1060nm was 6.5 μm.
- The VCSEL array was packaged by flip-chip bonding after dicing. The calculation coupling loss with MCF is 1dB when VCSEL MFD was 6 μm.
- The direct coupling of VCSEL array and MCF was limited in lab. When

MFD of VCSEL array was 4.4 μm, a varication of 1.4 dB between calculation CE and experiment CE.

- The experimental position misalignment tolerance fitted calculation results. When the VCSEL MFD was 4.9 μm, position misalignment tolerance was 2.7 μm.

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Publication List

a) Journal Papers (as first author)

1. L. DONG, et. al, “Densely packed 1.1 □m band vertical cavity surface emitting laser array for co-packaged optics,” Japanese Journal of Applied Physics, Jun. 2022, vol. 61, pp. SK1011.
2. L. DONG, et. al, “1060-nm Single-mode Bottom-emitting VCSEL Array for High-speed Multi-core Fiber Transmission”, Chinese Optics Letters.

b) International Conferences (as presenter)

1. L. Dong, et. al, "Thermal Crosstalk Evaluation of 1.1 μm-band Vertical Cavity Surface Emitting Laser Array for Multi-core Fiber Transmission," 2021 26th Microoptics Conference (MOC), 2021, pp. 1-2.
2. L. Dong, et. al, "Densely Integrated 1060nm 2D VCSEL Array for Space-division Multiplexing Toward Co-packaging Optics Transceivers," 2021 IEEE CPMT Symposium Japan (ICSJ), 2021, pp. 13-16.
3. L. Dong, et. al, “1060nm Single-mode Bottom Emitting VCSEL Array with Intra-cavity Metal-aperture for Multi-core Fiber Co-packaged Optics Transceivers,” 2022 International Conference on Solid State Devices and Materials (SSDM). 2022.
4. L. Dong, et. al, "16-ch 1060-nm Single-Mode Bottom-Emitting Metal-Aperture VCSEL Array for Co-Packaged Optics," 2023 Optical Fiber Communication Conference and Exhibition (OFC), 2023, W4B.3.

c) Domestic Conferences

1. L. Dong, et. al, “Thermal Crosstalk Evaluation of Densely Packed 1.1 μm-band VCSEL Array for Multi-core Fiber Transmission,” The 82nd JSAP Autumn Meeting 2021.
2. L. Dong, et. al, “1060nm VCSEL array for co-packaged optics,” International Symposium on Optical Communications 2021.

3. L. Dong, et. al, “16-ch 1060nm 2D VCSEL Array for Multi-core Fiber Transmission Toward Co-Packaging Optics Transceivers,” The 69th JSAP Spring Meeting 2022.
4. L. Dong, et. al, “1060nm Single-mode Bottom Emitting VCSEL Array for Multi-core Fiber Co-packaged Optics Transceivers,” The 83rd JSAP Autumn Meeting 2022.
5. L. Dong, et. al, “1060 nm Transverse Coupled Cavity VCSEL Array for CPO Transceivers,” International Symposium on Optical Communications 2022.
6. L. Dong, et. al, “16-ch 50Gbps 1060-nm Single-mode Bottom-emitting Metal-aperture VCSEL Array through 5km-long SMF,” The 70th JSAP Spring Meeting 2023.

List of Awards

Best Oral Presentation (1st place)



賞状

Best Oral Presentation Award (1st place)

Liang Dong　殿

あなたは第44回光通信研究会において優れた
発表を行い頭書の成績を収められましたので
これを賞します

令和４年８月２４日
光通信研究会
代表　　末松安晴

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