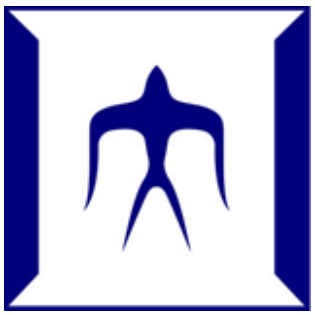
論文 / 著書情報
Article / Book Information

題目(和文)	
Title(English)	Dual-Layer Proton Irradiation on CMOS On-Chip Passive Devices for Sub-THz Circuit Performance Enhancement
著者(和文)	HERDIAN HANS
Author(English)	Hans Herdian
出典(和文)	学位:博士(学術), 学位授与機関:東京工業大学, 報告番号:甲第12920号, 授与年月日:2024年9月20日, 学位の種別:課程博士, 審査員:岡田 健一,廣川 二郎,德田 崇,伊藤 浩之,白根 篤史,高野 恭弥
Citation(English)	Degree:Doctor (Academic), Conferring organization: Tokyo Institute of Technology, Report number:甲第12920号, Conferred date:2024/9/20, Degree Type:Course doctor, Examiner:,,,,,
学位種別(和文)	博士論文
Type(English)	Doctoral Thesis



Dual-Layer Proton Irradiation on CMOS On-Chip Passive Devices for Sub-THz Circuit Performance Enhancement

by

Hans Herdian

A Ph. D. dissertation submitted in partial satisfaction of the requirements for the degree of

Electrical and Electronic Engineering

in the

School of Engineering

of

Tokyo Institute of Technology

Supervised by

Prof. Kenichi Okada

Fall 2024

To my family,

Acknowledgment

I am deeply grateful to my academic advisor, Professor Kenichi Okada, for his unwavering support and guidance throughout my doctoral study. Despite his demanding schedule, he always made time for me, providing invaluable advice and encouragement. His support was instrumental in helping me navigate the challenges of my research, and I am truly proud to be his student.

I am also thankful to Professor Atsushi Shirane for his continuous support and helpful discussions throughout my research. He also spent precious time reviewing my thesis and gave valuable comments and suggestions.

I want to thank the thesis examination committee members, Professor Takashi Tokuda, Professor Jiro Hirokawa, Professor Hiroyuki Ito and Professor Takano Kyouya for spending their time to improve the quality of my dissertation through helpful review, comments, and suggestions.

I would like to express my gratitude to Dr. Takeshi Inoue for his expertise in ion irradiation and for providing the equipment required for the experiment.

I am also grateful to Professor Hiroyuki Sakai and Professor Kazuaki Kunihiro for their continuous support in measurement methodology and data acquisition.

Furthermore, I extend my thanks to Ms. Yoshino Kasuga, Ms. Makiko Tsunashima, and Ms. Tomoko Iwahiro for their support in managing lab activities and resolving campus-related issues, allowed me to focus entirely on my research, and I deeply appreciate their efforts.

I also would like to express special gratitude to the research group members Dr. Ibrahim Abdo, Chun Wang, and Dr. Ning Li for their guidance and technical advice throughout my research. I also thank all the students of Okada Laboratory for their support, especially Liu Chenxin, Ashbir Aviat Fadila, and Dr. Dongwon You.

I am also grateful to Mr. Teruo Jyo and Mr. Hiroyuki Takahashi for their support throughout the NTT joint research period.

I want to express my sincere gratitude to the Japanese government for its precious support and for giving me such a great experience.

Finally, I would like to thank my parents and my two sisters. Their love and support are what make me who I am today.

Abstract

The demand for larger bandwidth and data rate for the future 6G wireless communication system, coupled with the frequencies below 10 GHz becoming crowded, has prompted extensive research on the utilization of sub-terahertz frequencies. At this frequency, the wavelength shrinks to a sub-millimeter scale, causing a reduction in the size of passive components to the point where they cannot be precisely manufactured by a typical PCB process, which points to on-chip implementation as an obvious solution. However, the substrate's low substrate resistivity and high permittivity reduce the performance of the passive components, especially in the standard CMOS process where substrate resistivity can be as low as 3 Ω·cm. This dissertation presents the development of a dual-layer proton irradiation method to improve the performance of the CMOS on-chip passive components at sub-terahertz frequencies by increasing the resistivity of the silicon substrate. By targeting the Si-SiO_2 layer with additional irradiation, the total dose required to achieve thermal stability is reduced from 10^{15} cm^{-2} to $4x10^{14}$ cm^{-2}. The margin distance requirement for the active component is reduced from 50 μm to 22 μm while keeping the same final substrate resistivity as with the conventional method. This method was then applied on a 300 GHz band on-chip Vivaldi antenna and a 300 GHz band on-chip waveguide transition to test its efficacy on sub-terahertz frequency. After irradiation, measurement results show a 4 dB gain improvement and efficiency increase from 32% to 87% on the antenna, with a 2.1 dB reduction of transmission loss on the waveguide transition. The proposed dual-layer irradiation enables CMOS on-chip passive components to achieve competitive performance at sub-terahertz frequency and solves the substrate loss issue.

Contents

List of Figures

List of Tables

Chapter 1

Introduction

1.1 The Future Wireless Communication System

The exponential growth of data consumption has pushed the evolution of the wireless communication technology in the last 20 years, as technologies such as social media, video streaming, e-learning, remote work, e-commerce, and more applications becomes more commonly used worldwide. The deployment of 5G wireless communication network further opens up new potential applications that utilize massive machine-type communications and ultra-reliable low-latency communications, such as internet-of-things (IoT) and self-driving car [8]. The mainly used sub-6GHz frequency band is too crowded and does not have enough bandwidth to accommodate these potential new applications. Therefore, the 3rd Generation Partnership Project (3GPP) develops a 5G New Radio (5G NR) standards to utilizes the millimeter-wave band at 28 GHz and 39 GHz for higher data rate and lower latency in exchange for shorter link distance [9]. The 5G NR systems are expected to reach data rates more than 10 Gb/s with low latency and beam-forming support for the millimeter-wave frequency to compensate the increasing path loss. The 5G NR is currently in the implementation phase for over the next 5 years with the technology constantly being refined to achieve its maximum potential.

With 5G already in implementation phase, significant efforts are underway to characterize the use case and requirements of the next generation wireless communication systems, which is commonly referred as 6G. Several analyses and discussions has been published by journals, organizations, and standardization bodies such as International Telecommunication Union (ITU-T) [1, 10–13]. From these discussions, the expected requirement of the future 6G wireless communication network can be summarized as [1]:

1. **Data rate**: More than 1 Tb/s peak data rate is required mainly for use cases such as holographic communication and hologram assisted technology [12, 14], including

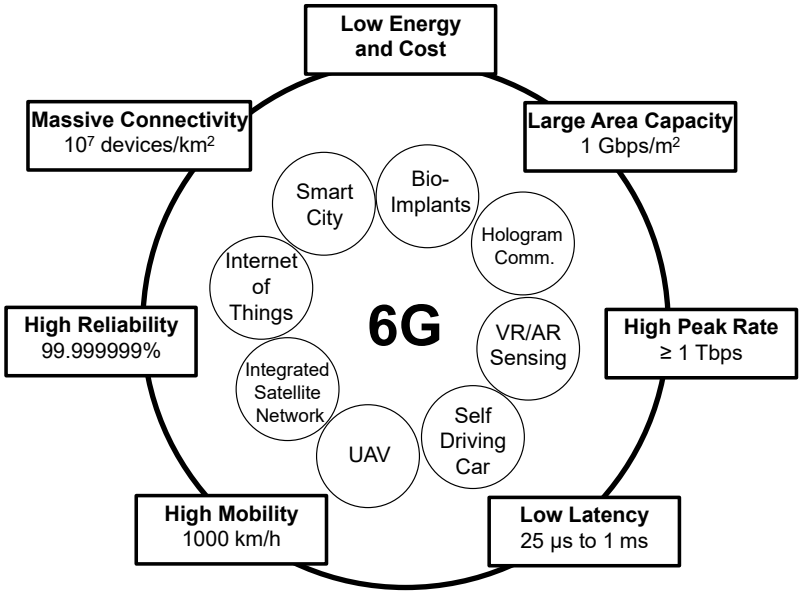


Figure 1.1: Vision of the 6G systems and its underlying use case [1].

remote health care, remote repair and remote industrial monitoring. This also covers the needs for information shower kiosks, the millimeter-wave small cell backhaul [15], and chip-to-chip communication. The user data rate is expected to reach at least 1 Gb/s.

2. **User latency**: At least 1 ms is required mainly for use cases such as holographic communication and hologram assisted technology [16, 17], and sub-ms latency maybe required for application requiring instantaneous haptic feedback.

3. **Mobility**: 6G systems should be able to communicate with target traveling up to 1000 km/h, which take into account communication with airplane and satellite-to-satellite communication [18]. Communications with multiple moving target should be supported.

4. **Connection density per km^2**: Assuming the exponential growth of the number of devices connected to the network, connection density requirement is expected to be 10× of 5G, which is around 10^7 devices/km^2.

5. **Reliability**: Applications such as cooperative autonomous driving and industrial automation requires 99.999% network reliability [19]. Industrial IoT systems could require reliability as high as 99.99999% [20].

All of these requirements and example use cases are summarized in Fig. 1.1.

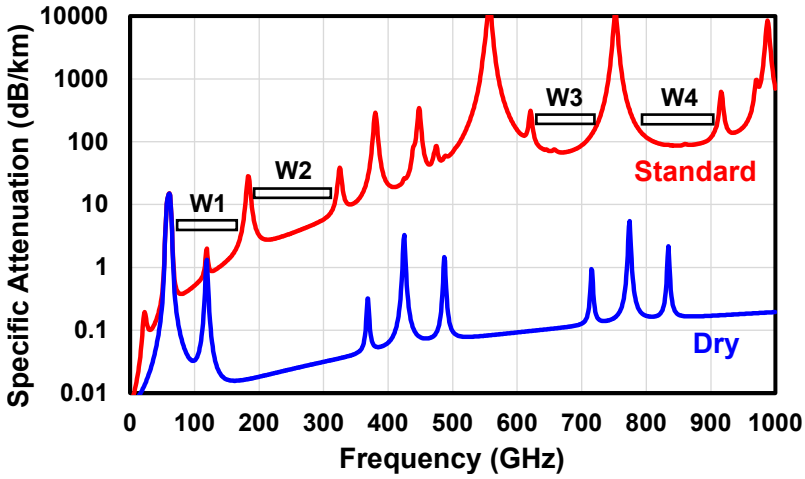


Figure 1.2: Atmospheric absorption loss across different frequency and possible candidate for 6G sub-terahertz band.

From all the requirements listed above, this thesis will focus the discussion on the fulfillment of the 1 Tb/s data rate requirement. This data rate is not achievable with the frequency band used in the current 5G implementation. Therefore, there are a lot of discussions [1, 1, 10–13, 21] about extending the 6G frequency band to cover the sub-terahertz frequency range (100 GHz to 1 THz).

1.1.1 Sub-terahertz Frequency Extension

Fig. 1.2 shows atmospheric absorption loss of all the sub-terahertz frequency range, which is the first consideration in choosing a suitable frequency band for 6G sub-terahertz. Within the sub-terahertz frequency range, there are some frequency bands with very high atmospheric absorption rate, causing high attenuation and not suitable for long range communication. Therefore, frequency windows W1 to W4 are initially considered as they have a wide available bandwidth where the atmospheric absorption is relatively low. W3 and W4 are outside the capabilities of the widely available and low cost chip manufacturing process, such as CMOS process. Consequently, W1 and W2 becomes the main frequency of interest for the future 6G sub-terahertz band. W1 corresponds to F-band (90 GHz to 140 GHz) and D-band (110 GHz to 170 GHz), while W2 corresponds to the 300 GHz band (220 GHz to 320 GHz). These bands has 3 desirable characteristics as a candidate for 6G sub-terahertz band:

1. They provide a large available bandwidth with less crowdedness compared to the lower frequency bands.

2. Can be implemented with widely available low cost chip manufacturing process

with reasonable performance.

3. The short wavelength enables passive components miniaturization, such as antenna. Allowing high-density large-element array system with low area occupation.

The characteristic number 3 is of a particular interest of this thesis, as this push the migration of typically off-chip components (antenna, chip-to-waveguide transition, etc.) towards on-chip implementation.

1.1.2 Large-Scale Small Cells Deployment

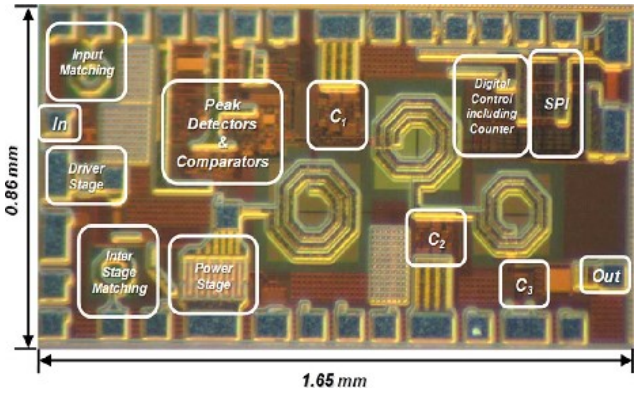
Similar to the deployment of the 5G millimeter-wave, the 6G sub-terahertz is expected to be deployed either as a high capacity backhaul or as large-scale small cells inside home and large density residential area [15]. Compared to 5G millimeter-wave, the 6G sub-terahertz will suffer more path loss and only capable to perform line-of-sight communication [22]. Therefore, larger number of small cells are required to cover the same area. Furthermore, array topology with large number of elements will be used to compensate path loss and line-of-sight through array gain, beam-forming, and beam-steering technology [23]. This large element array implementation requires large number of chips, and the large number of small cells further increase the number of chip requirement while the cost should be kept low. Due to the all factors above, low cost technology with large production capacity, such as the standard CMOS process, is preferable for this implementation.

1.2 Passive Component Implementation on Sub-terahertz Frequency

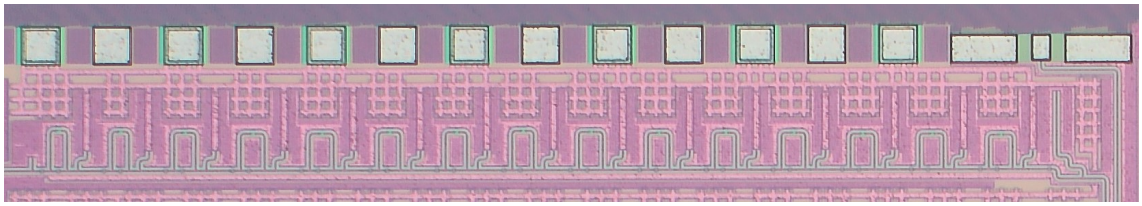
As the operating frequency approach sub-terahertz range, the design wavelength of passive components shrink to the sub-millimeter size. This shrinkage has different impact on implementation method and design considerations based on the type of the passive components, leading to different ways on how active circuits are implemented in the sub-terahertz range. The size reduction also allows the typically off-chip components to be implemented on-chip.

1.2.1 Lumped Inductor and Capacitor

Lumped inductor and capacitor are components that can be implemented on-chip from frequency as low as 1 GHz. These two components are the main building blocks of many



(a)



(b)

Figure 1.3: Comparison between (a) a 2.4 GHz CMOS power amplifier from [2], and (b) a 250 GHz CMOS power amplifier from [3].

analog circuits such as voltage-controlled oscillator (VCO), amplifier, mixer, matching network, and so on. However, as the operating frequency increase above 60 GHz, the shunt parasitic capacitance to the substrate starts to become more significant, reducing the quality factor and limiting the maximum operating frequency of both components. Consequently, the usage of lumped inductors and capacitors become impractical at sub-terahertz range. This also holds true for passive components derived from these two, such as inductor-based transformer, coupler, or balun. On CMOS substrate, the degradation of quality factor becomes more severe as the low substrate resistivity has more impact on the lumped components at high frequency.

1.2.2 Transmission Line

In contrast to the lumped inductor and capacitor, the usage of on-chip transmission line (TL) in a matching network or as a derivative component is impractical at low frequency because the length of the TL cannot fit inside the chip. However, as the operating frequency reach the sub-terahertz range, the required TL length shrinks to around micrometer range, which fits inside the standard area of a chip. Consequently, the design approach of matching network for on-chip amplifier design change from lumped component based

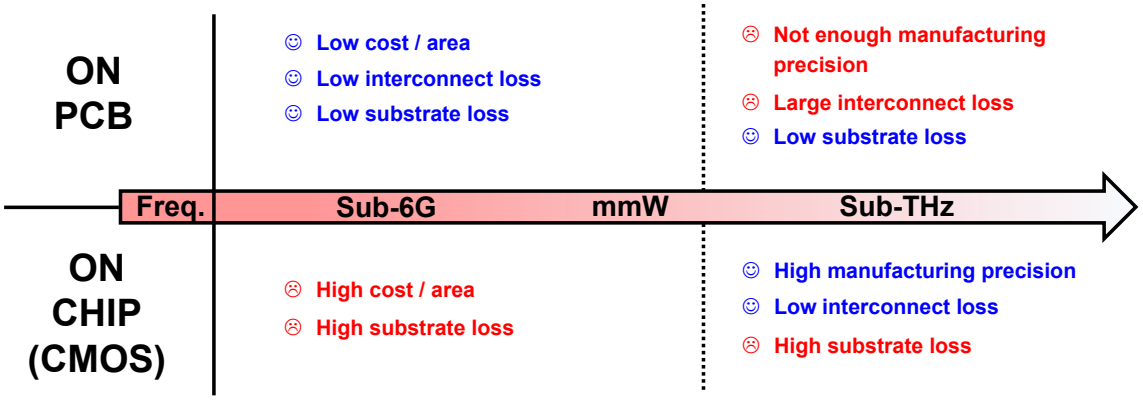


Figure 1.4: General trend of antenna and on-chip-transition implementation across frequency.

to TL-based at sub-terahertz frequency, as shown in Fig. 1.3. The design of many derivative components such as coupler and balun also becomes TL-based. Another benefits on using TL matching network is the substrate isolation through bottom metal shielding, eliminating the effect of the low resistivity substrate on CMOS process.

1.2.3 Antenna and Chip-to-Waveguide Transition

Antenna and chip-to-waveguide transition are passive components typically implemented on-PCB because their large size. Compared to on-chip implementation, the on-PCB implementation at lower frequency has low cost per area and low substrate loss, with negligible interconnect loss due to the short interconnect length compared to the design wavelength. As the design frequency increases to sub-terahertz range, the radiating structure shrinks to the level where it becomes difficult to precisely manufacture with low-cost PCB process, requiring migration to a better PCB process with higher cost. Additionally, the interconnect length relative to the wavelength increases to the point where bump and pad mismatch on flip-chip or wirebonding connection becomes non-negligible [24, 25]. Furthermore, most sub-terahertz TRXs with on-chip antenna are implemented as array to mitigate the large path loss in sub-terahertz frequency [3, 26], which requires inter-element distance less than 600 μm for a 300 GHz band TRX. All of these factors push the sub-terahertz antenna and chip-to-waveguide transition development towards on-chip implementation, where there is no interconnect loss, high manufacturing precision, and comparable cost to advanced PCB manufacturing process (Fig. 1.4).

The biggest drawback for on-chip antenna and transition implementation, especially on CMOS process, is the low substrate resistivity (around 3 Ω-cm to 15 Ω-cm), which causes high substrate loss. The low substrate resistivity absorbs most of the energy radi-

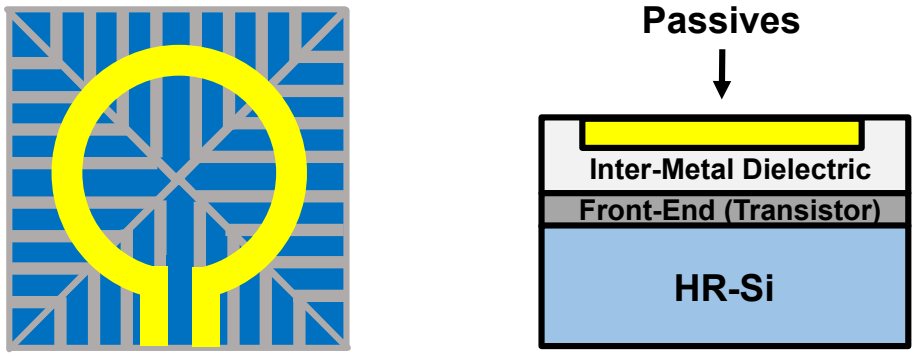


Figure 1.5: (a) Ground metal shielding, and (b) high resistivity substrate integration.

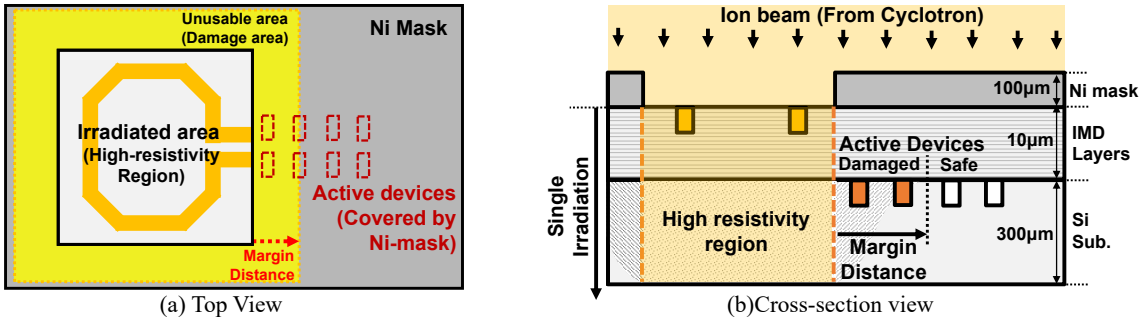
ated by the antenna and dissipates it as heat, which significantly reduces CMOS on-chip antenna efficiency to less than 50% [27, 28]. This also applies for CMOS on-chip transition implementation, which results in 3dB higher insertion loss [7] than other on-chip transition implemented on semi-insulating substrate [29]. Therefore, this substrate loss problem must be mitigated for the CMOS on-chip antenna or chip-to-waveguide transition to achieve competitive performance.

1.3 Substrate Loss Mitigation Techniques

1.3.1 Ground Metal Shielding

The simplest and most common solution to solve the substrate loss issue is by preventing the interaction between the lossy substrate and the passive component through metal shielding [28, 30, 31], as shown in Fig. 1.5(a). This method is readily available in all standard CMOS processes and can be implemented immediately in-process, with accurate modeling can be quickly performed through an EM simulator. There is no need to develop a separate post-process or modify the existing CMOS manufacturing process.

However, this technique has several drawbacks. First, this technique cannot be used on all types of passive component. While this technique can be implemented on a transmission line without any issue, implementation on capacitor and inductor result in a large parasitic capacitance to the ground, which limits their maximum operating frequency. For antenna and chip-to-waveguide transition implementation, this technique limits the usable architecture to the broadside structure such as patch, making it impossible to implement end-fire structure. Furthermore, the proximity between the top metal used for the passive component and the bottom shield metal (less than 10 μm) induce a large image current in



(a) Top View (b)Cross-section view

Figure 1.6: The general principle of ion irradiation (a) top view, and (b) cross-section view.

the bottom shield metal, leading to additional loss as heat [32]. Therefore, the final performance of these shielded antennas and transitions are still worse than the typical PCB implementation, although still better compared to the implementation that suffers from substrate loss.

1.3.2 High-Resistivity Substrate Integration

For a solution that can be applied on all types of passive component, a method to directly increase the substrate resistivity is required. The most common method is to replace the low resistivity silicon substrate in standard CMOS processes with high-resistivity Silicon (HR-Si) such as amorphous Si or porous Si [33–37], which can achieve resistivity as high as 10 kΩ-cm [33]. Because high performance active device cannot be implemented directly on the HR-Si, a thin layer of low-resistivity silicon was added on top of the HR-Si where the circuit is implemented, creating a silicon-on-insulator (SOI) process [36, 37] as shown in Fig. 1.5(b).

The main drawback of this approach is the need to develop a new manufacturing process. A new manufacturing facilities, infrastructures, and development environment must be build and optimized. Furthermore, the characteristics of active devices implemented on the new process needs to be remodeled as a library for easier design process. All of this require large amount of investment and time. In addition, the more specific target application of the process limits the consumer demand, resulting in reduced production scale. Coupled with higher manufacturing complexity than a standard CMOS process on the same process node, all the above-mentioned factors resulting in higher process cost compared to the existing CMOS process.

1.3.3 Ion Irradiation

Ion irradiation (Fig. 1.6) is a method to increase the substrate resistivity by bombarding high energy ions to the substrate, which generates defects and charge traps in the silicon crystal structure that reduces carrier mobility [4, 5, 38, 39]. This method can be performed on a manufactured chip as a post-process, which eliminates the need to modify the existing standard CMOS processes. Therefore, the total implementation cost can be kept low by utilizing the large-scale infrastructure and development environment available on the CMOS processes. Another benefit of ion irradiation is the ability to control the shape and location of the high-resistivity region through a mask, enabling separation between high-resistivity substrate required for passive components and the default substrate resistivity where the active devices were designed and modeled. Therefore, there is no need to remodel and re-characterize the available active device models. Furthermore, ion irradiation can be applied to all types of passive component because it increases the substrate resistivity directly, surpassing the ground metal shielding method in terms of component universality. All of these benefits makes ion irradiation the most promising solution to improve on-chip passive component performance in terms of cost and component types coverage.

Even with all above-mentioned benefits, ion irradiation method has three main drawbacks:

1. The defects and charge traps generated in the silicon crystal can be recovered by performing high-temperature heat treatment (annealing) to the irradiated substrate, which can reduce the induced high resistivity. This makes the formed high-resistivity region vulnerable to common high-temperature post-processing such as flip-chip process [40] and reflow soldering [41]. This thermal stability problem also prevents the chip usage on extreme environment, such as low-earth orbit satellite application.

2. While the thermal stability problem can be solved by generating more defects, more irradiation time is needed to generate those defects. This leads to longer machine operation time and lower wafer throughput, which ultimately increases the process cost.

3. Some of the irradiated ions can spread laterally beyond the mask edge, which damages all active devices within the specified margin. This creates an extended unusable area around the target irradiation area. This margin requirement can be as high as 50 μm on proton irradiation [4, 5], which is especially wasteful on higher CMOS process nodes.

These drawbacks has to be reduced or mitigated to make the ion irradiation process more viable for large-scale implementation.

1.4 Research Objective

The main objective of this thesis is to improve the performance of on-chip passive components for sub-terahertz circuit implementation on CMOS. Based on the previous discussions, the main challenge to improve passives performance is substrate loss due to the low-resistivity substrate. While conventional ion irradiation is a promising solution, it has several drawbacks that can be suppressed or mitigated. Therefore, this thesis aims to develop a new ion irradiation profile with direction as follows:

1. Perform a deep analysis on the conventional ion irradiation process to identify if there are any possibility to further improve the process.

2. If the potential mechanisms or theories to improve the conventional are found, propose a new improved process by utilizing the previously found mechanisms or theories. The new ion irradiation process should improve the previously discussed three drawbacks of the ion irradiation, which are thermal stability, high cost due to the long irradiation time, and wasted area due to the large unusable area around the irradiated region.

3. The proposed ion irradiation process should be tested on several on-chip sub-THz passive components to verify its efficacy on the sub-THz frequency and to make sure this process can be applied on the future 6G transceiver system.

To limit the scope of the sub-THz frequency range for evaluation on the Objective 3, the 300 GHz band (220 GHz to 320 GHz) is used as the target frequency for the passive component implementation. This is because 300 GHz band is the highest f_{max} limit of the transistor implemented on standard CMOS processes.

1.5 Thesis Organization

This thesis is organized as follows: Chapter 2 introduces the mechanism of the conventional ion irradiation and the parameters that affect the irradiation performance. This chapter also analyzes how these design parameters related to the issues of the ion irradiation. This chapter also explore the impact of the parasitic surface conduction layer formation, which is not discussed previous study, on the previously discussed issues, and use it as the basis theory to propose the new ion irradiation process.

Chapter 3 presents the proposed dual-layer proton irradiation, which includes the detailed steps and implementation requirement of this process; the optimization of process parameters through experimental method; and lastly, the evaluation of the optimized process and comparison with the conventional irradiation.

Chapter 4 and Chapter 5 presents the application of the proposed dual-layer proton irradiation on the sub-THz on-chip passive components. In Chapter 4, a 300 GHz band CMOS on-chip Vivaldi antenna was designed and applied with the proposed dual-layer proton irradiation. The antenna performance before and after irradiation was measured and compared. In Chapter 5, a 300 GHz band CMOS on-chip chip-to-waveguide transition was designed and applied with the proposed dual-layer proton irradiation. The transition performance before and after irradiation was measured and compared. Furthermore, the transition was integrated with a 250 GHz transmitter as a transmitter module, which was measured.

Finally, the conclusions and future directions of this research are presented in Chapter 6.

Chapter 2

Analysis of Conventional Ion Irradiation [1]

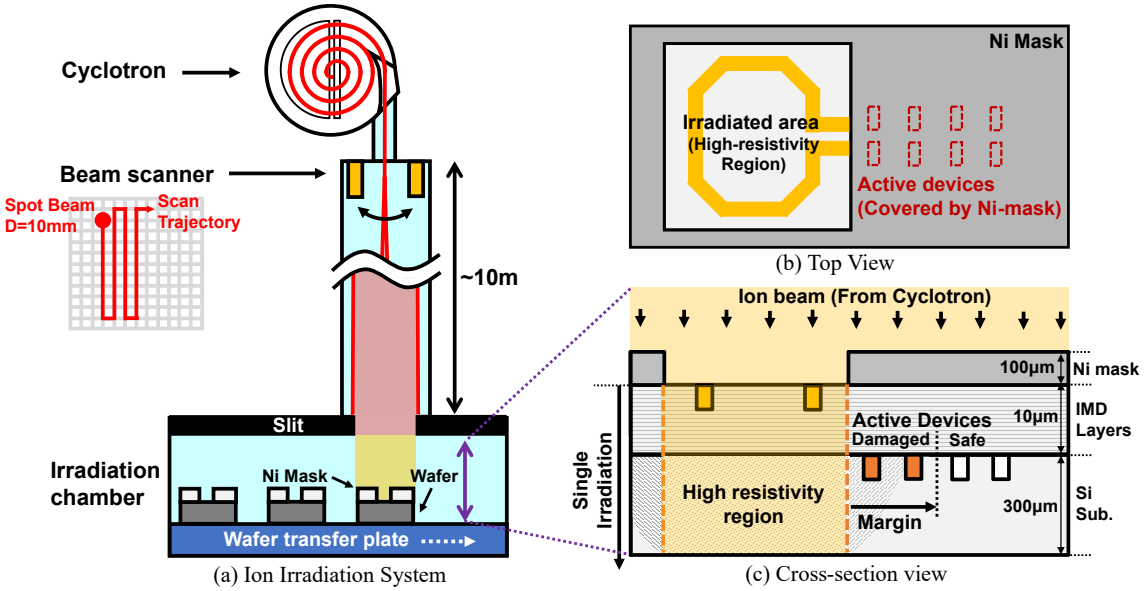
As discussed in previous chapter, ion irradiation is the most promising method to create a high-resistivity substrate on a CMOS processes without modifying the process itself. However, there are several issues preventing efficient implementation of this method. This chapter explains the detailed mechanism of conventional ion irradiation and its related process parameters, which is crucial to understand the underlying cause of problems found in ion irradiation and to propose ways to mitigate them.

2.1 Process Overview

Fig. 2.1(a) shows the general setup to perform an ion irradiation on a wafer. First, an ion accelerator is needed to accelerate the ion from the source to the desired energy level. Depending on ion species, this ion accelerator can be a cyclotron, extractor-type ion gun, or other kinds of accelerator. The output of the ion accelerator is a spot ion beam with 5 mm to 50 mm diameter, which is not enough to cover the whole silicon wafer. Therefore, a beam scanner is used to rasterize the ion beam to cover the whole wafer surface. This irradiation is performed for certain amount of time until the desired ion concentration (fluence) is reached. Finally, the wafer transfer plate moves out the irradiated wafer and put in the new wafer to the irradiation area for another irradiation cycle.

Fig. 2.1(b) and (c) shows the setup of the chip during irradiation process. The chip was covered with nickel mask to choose the irradiation target area and protect the active de-

[1] This chapter is based on "Dual-Layer Proton Irradiation for Passive Component Enhancement and Noise Coupling Suppression on CMOS Process" [42] by the same author, which appeared in the IEEE Transactions on Electron Devices,



(a) Ion Irradiation System

(b) Top View

(c) Cross-section view

Figure 2.1: Ion irradiation mechanism: (a) overall system, (b) top-view of the irradiated chip with mask, and (c) the cross-section view of the irradiated chip.

vices (transistors, diodes, etc.) from radiation damages, eliminating the need to re-model these devices. At the irradiation target area, the high energy ions generate defects and charge traps [4, 5, 43] in the silicon substrate, increasing the substrate resistivity by reducing carrier mobility. Higher ion fluence generates more defects, which further increases substrate resistivity and making it more resistant to high-temperature post-processing. However, higher ion fluence also increase irradiation time, leading to higher process cost. The active devices must be placed with a certain margin from the edge of the irradiation area due to the possibility of ion lateral scattering, rendering the area within a certain margin outside the irradiation area unusable for active devices placement.

2.2 Process Modeling

Throughout this work, SRIM (Stopping and Range of Ions in Matter) software package is used to simulate the ion range and defects distribution through Monte-Carlo simulation [44]. Ion range was determined with Brag's rule corrected with Core and Bond approach [45] and experimental data [46]. The accuracy of this software package varies depending on the implant ion and the target substrate. The stopping range mean error for proton implantation on silicon, which is the focus of this work, is around 3.9% [44]. The mean error of the vacancy defects concentration is around 14% [47].

2.3 Process Parameters

2.3.1 Ion Energy

Ion beam energy level, denoted in eV, determines the penetration depth (R_p) and the straggle (ΔR_p) of the implanted ions within the target material. R_p is the average depth the ions travel from the surface of the target material, and ΔR_p is the deviation of ion distribution from the R_p. Both are illustrated in Fig. 2.2(a). Factors that impact R_p and ΔR_p can be seen in the simplified LSS model equations [48, 49]:

$$R_p \approxeq \frac{R}{1 + (M_t/3M_i)} \tag{2.1}$$

$$\Delta R_p \approxeq \frac{2R_p\sqrt{M_i M_t}}{3(M_i + M_t)} \tag{2.2}$$

indicating that R_p and ΔR_p are mainly affected by the mass of the implant atoms (M_i), mass of the target atoms (M_t), and the implant ion range (R), which in itself is determined by the following equation [48, 49]:

$$R \approxeq K\frac{E}{\rho_t}\left(\frac{M_t(M_i + M_t)}{M_i}\right)\left(\frac{\sqrt{Z_i^{2/3} + Z_t^{2/3}}}{Z_i Z_t}\right) \tag{2.3}$$

which indicates that the atomic number of the implant atoms (Z_i), atomic number of the target atoms (Z_t), implant energy (E), and target substrate density (ρ_t) also affect R_p and ΔR_p (K is a constant). The derivation of a more accurate model [50, 51] are beyond the scope of this dissertation. A simulator called the Stopping Range of Ion in Matter (SRIM) [44] was used for all ion irradiation related analysis in this dissertation to ensure accurate simulation results.

2.3.2 Ion Species

From previous section, it can be inferred that the energy and mass of the ion species chosen will affect the penetration depth R_p. Fig. 2.2(b) shows the penetration depth of various ion species into the silicon substrate across different energy levels. While heavier ions have less lateral scattering and generate more defects compared to lighter ions [38, 52], the energy required to penetrate the silicon substrate (typically 300 μm in a standard 65 nm CMOS process) increases exponentially, requiring the use of larger, specialized, and costly ion accelerator. Due to this limitation, most works involving ions heavier than hydrogen and helium only involves the creation of a thin passivation layer, either at the

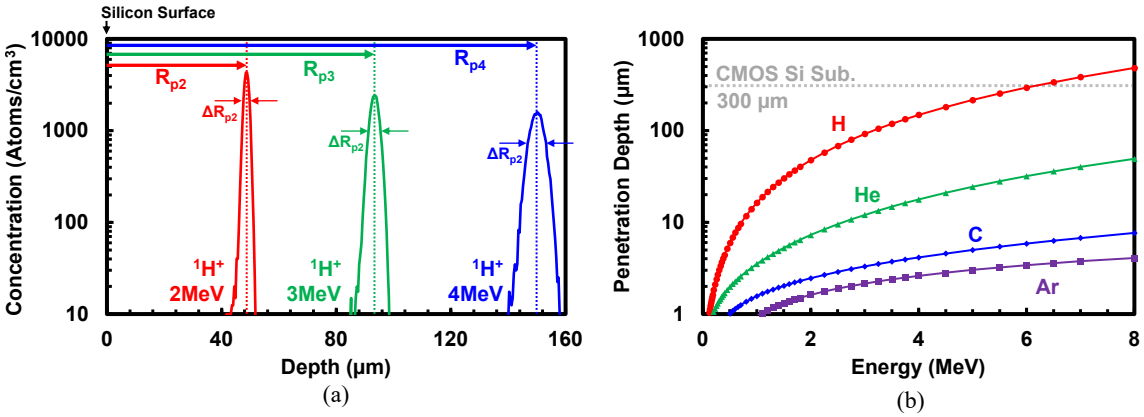


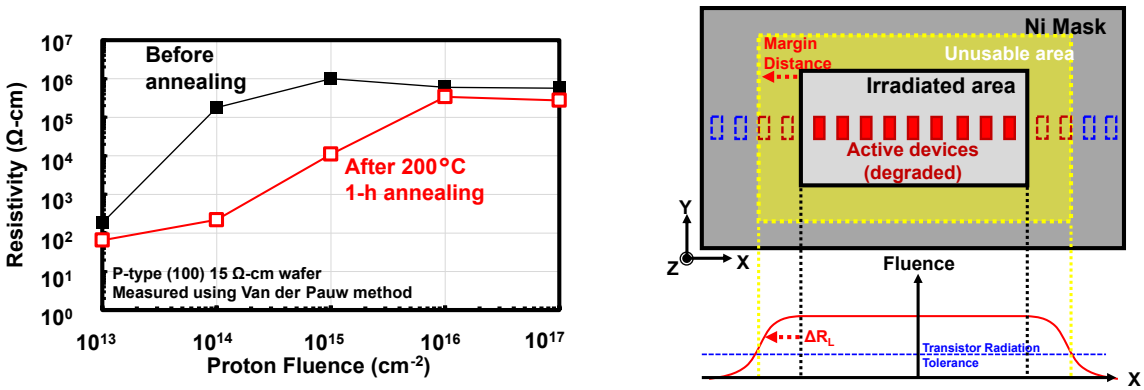
Figure 2.2: Simulation results of (a) The effect of ion energy of proton on penetration depth R_p and straggle ΔR_p with silicon target. (b) The effect of ion energy on penetration depth across different ion species into a silicon substrate.

Si-SiO_2 interface [52, 53] or at the interface of the externally-added high-resistivity silicon (HR-Si) in silicon-in-insulator (SOI) process [54, 55]. Therefore, hydrogen ion (proton) is typically chosen to create a localized high-resistivity region in a standard CMOS processes [4, 5, 39] as it can penetrate through a typical 300 μm thick substrate with low energy requirement, allowing the usage of low-cost ion accelerators and eliminating the need of existing process modification or integrating external HR-Si.

Ion species also determine the type of defects inflicted to the target substrate, as several ion-related defects can behave as electron donor or acceptor, which can increase or decrease substrate resistivity. Proton generates two kinds of defects, pure crystal damage defects (vacancy related), and hydrogen-related defects [43, 56–60]. The pure crystal damage defects are vacancy-related, such as oxygen-vacancy pair, divacancy center, and phosporus-vacancy pair, leads to amorphization at high enough concentration, and always increases resistivity [43]. On the other hand, hydrogen-related defects can behave as electron donor if these defects are activated through annealing above 350°C [58–60], which increases resistivity in P-type silicon and decreases resistivity in N-type silicon. Therefore, for high-resistivity region formation, the target substrate must be P-type silicon and post processing with temperature above 300°C must be avoided if possible.

2.3.3 Ion Fluence

Ion fluence (N_F) is the concentration of irradiated ions in a given surface area of the target substrate, typically given in units of atoms/cm^2 (shortened to cm^{-2}). Alternatively, the term ion dose is used for irradiation to organic material. Higher irradiation fluence generates higher concentration of defects and charge traps, which leads to higher resistivity.



(a) (b)

Figure 2.3: (a) The measured substrate resistivity across different proton fluence from [4]. (b) The impact of lateral scattering and its measurement method in [5].

Factors that affect defects generation can be observed from the Kinchin-Pease damage function for $E \geq \xi/2E_d$ [49]:

$$\langle N_d(E) \rangle = \frac{\xi v(E)}{2E_d} \tag{2.4}$$

where the average number of defects generated by a single implant ion ($\langle N_d(E) \rangle$) is determined by the implant energy E, the target material minimum displacement energy (E_d), atomic interaction factor ξ ($\xi < 1$), and nuclear damage energy $v(E)$. Keep in mind that the energy loss of implant ion through a solid material (dE/dx) happens through a combination of nuclear and electronic energy loss, as expressed in [49]:

$$\frac{dE}{dx} = \frac{dE}{dx}\bigg|_{nuclear} + \frac{dE}{dx}\bigg|_{electronic} \tag{2.5}$$

where nuclear energy loss is the only one caused by collisions and generate defects. The relation between total nuclear energy loss and $v(E)$ can be expressed as:

$$v(E) \equiv \int^{R} \frac{1}{N_t} \frac{dE}{dx}\bigg|_{nuclear} dx \tag{2.6}$$

where N_t is the atomic density of the target substrate and R is the implant ion range. $v(E)$ is typically 20% to 30% smaller than total nuclear energy loss.

Because equation (2.4) is for a single ion, increasing the fluence will increase defects in proportion with the number of ions. Fig. 2.3(a) shows the measured substrate resistivity across different the proton fluence in conventional proton irradiation performed in [4], which depicts how the resistivity increase with proton fluence until it reach saturation due to amorphization [61].

2.3.4 Ion Channeling

Because the target substrate is monocrystalline Si used for chip manufacturing, the substrate orientation can have pronounced effect on the ion penetration range and defects generation due to the channeling effect [49]. The channeling effect significantly increases ion penetration depth and decreases defects generation of the transiting ions, which can lead to significant increase of fluence requirement to generate the same defects concentration. Furthermore, the SRIM simulator used in this work does not take channeling into account [44]. Therefore, the irradiated samples must be aligned to avoid channeling as much as possible.

2.3.5 Ion Lateral Scattering

Ion lateral scattering (ΔR_L) is the deviation of ion from its targeted location in the direction lateral to its implantation direction. Fig. 2.3(b) illustrates how lateral scattering on XY-directions happens to ion implanted in Z-direction. This value is closely related to range straggle (ΔR_p). Therefore, while numerical expressions exist for lateral scattering [62, 63], it is typically expressed in its relations with ΔR_p[49]:

$$\Delta R_L = C\Delta R_p \tag{2.7}$$

with the constant C inversely proportional with M_i, where $C > 1$ in lighter implants and $C < 1$ for heavier implants. In practical implementation, the lateral scattering determine the margin distance required from the irradiation area to prevent radiation damage, which is determined by ΔR_L and the active devices radiation tolerance (process dependent). In this case, ion fluence also affects margin distance as more fluence leads to the expansion of the distance where ion concentration exceeds the transistor radiation tolerance. This is proven by measurement in previous works, where proton irradiation requires 50 μm margin distance [5], while irradiation using lower fluence and heavier helium only requires 10 μm margin distance [38].

2.4 Issues

2.4.1 Thermal Stability

The thermal stability of the formed high-resistivity region is one of the main issue in ion irradiation [4, 5, 38, 43]. If the irradiation fluence is too low, the Si substrate largely maintain its crystalline structure, with isolated damage zones scattered across the sub-

strate [64]. This isolated damage zones can be recovered with lower annealing temperature, making the resistivity unstable. As the fluence increase, these damage zones become larger and harder to anneal, until they cover the whole substrate, resulting in complete amorphization. For conventional proton irradiation, a fluence above 10^{16} cm^{-2} is needed for complete amorphization, raising the stable temperature to around 500°C [43], which is far above the peak temperature of typical reflow soldering post-process of 260°C [40]. However, study in [4] shows that thermal stability is proportional to proton fluence in lower fluence cases (below 10^{16} cm^{-2}), which can be seen in Fig. 2.3(a). Furthermore, resistivity above 1 kΩ-cm cannot be maintained with fluence below 4×10^{14} cm^{-2} after a 1 hour 200°C annealing, making the formed high-resistivity region vulnerable to degradation after a reflow soldering post-process. Therefore, studies in [4] and [5] concluded that at least a proton fluence of 10^{15} cm^{-2} is required to form a thermally stable high-resistivity region that can withstand 200°C to 300 °C temperature process.

2.4.2 Irradiation time

Proton fluence requirement is directly related to irradiation time, which determines a significant part of the process cost due to the proton accelerator's power consumption and irradiated wafer throughput. The output of a proton accelerator is typically specified by the beam current I_B, with typical value around 50 μA to 300 μA on commercially available PET cyclotrons [65]. Irradiation time t_i for proton can be expressed as:

$$t_i = \frac{eN_F}{I_B}A \tag{2.8}$$

where N_F is the proton fluence, e is the elementary charge of one proton (1.602×10^{-19} C), and A is the area of the irradiation target (720 cm^2 for a 12 in silicon wafer). It can be seen how the reduction of proton fluence directly reduces irradiation time, leading to reduction of machine power consumption per wafer and increased throughput.

2.4.3 Margin Distance Requirement

As briefly mentioned in subsection 2.3.5, a margin distance from the irradiation area is required to prevent radiation damage on active devices, especially transistors, due to the lateral scattering. Fig. 2.3(b) shows how this margin distance creates an unusable area around the irradiation area, which is especially undesirable on higher process nodes due to the higher cost per area and higher possible transistor density per area. In addition to lateral scattering, margin distance is also affected by proton fluence and the transistor damage tolerance. The transistor damages are mainly caused by the accumulation

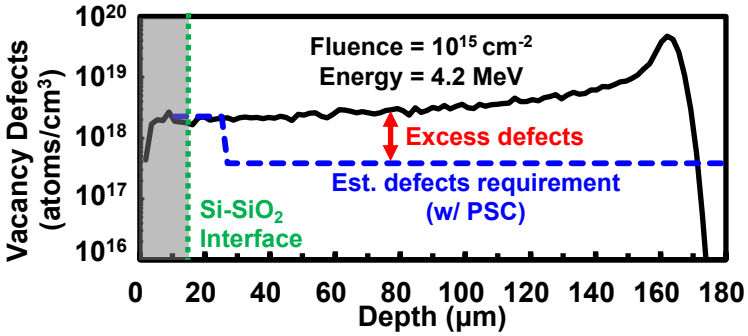


Figure 2.4: (a) Simulation of vacancy defects of a single 4.2 MeV proton irradiation with 10^{15} cm^{-2} fluence compared to estimated defect requirement after considering PSC effects.

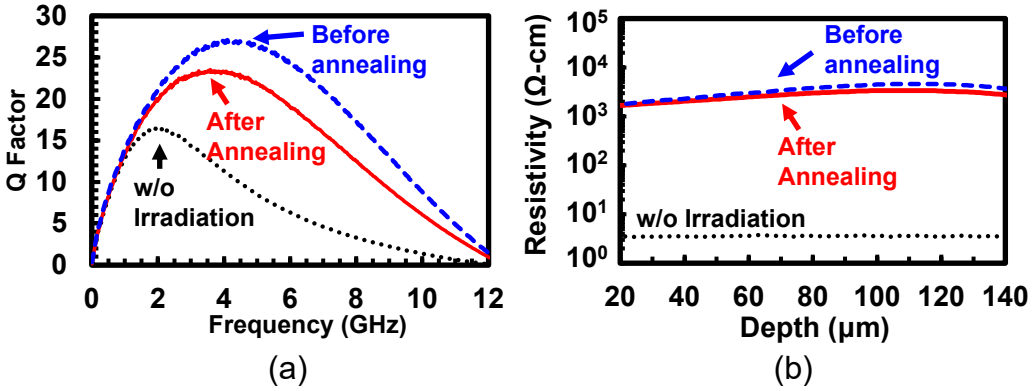


Figure 2.5: Measurement results of (a) the Q-factor of a 1.8 nH on-chip inductor manufactured in a standard 65 nm CMOS process, and (b) the resistivity of a CZ-P (100) 4 Ω-cm Si wafer. Both structures were irradiated with 4×10^{14} cm^{-2} proton fluence and measured before and after 1 minute 260°C annealing

of defects and charge traps at the oxides surrounding the transistor, such as gate oxide and shallow trench isolation (STI) oxide, which cause performance degradation due to increased leakage current and flicker noise [66, 67]. The difference in oxide thickness, channel length, and implants cause different radiation tolerance across different CMOS processes, with higher tolerance on higher process nodes [66, 68]. If ion species and process node are fixed, the only way to improve margin distance requirement is to reduce proton fluence.

2.5 Parasitic Surface Conduction Layer

Parasitic surface conduction (PSC) effect refers to the formation of a low resistivity layer at the Si-SiO_2 interface due to the presence of fixed positive charges in the oxide, which attract free carriers to the interface and generate low resistivity inversion layer. As a re-

sult, the effective substrate resistivity seen by passive components decreases by a factor of 10 to 10^4 from its original value [34, 69, 70]. The PSC effect was overlooked in previous proton irradiation studies because the PSC layer formation was naturally prevented by increasing the proton fluence until the transiting protons generated enough traps and defects to passivate the Si-SiO_2 interface. While thermal stability can be achieved, this leads to increased fluence requirement to fulfills the interface defect requirement, as the transiting proton has low defect generation efficiency. Furthermore, the total-ionizing dose (TID) effect at SiO_2 induced by the proton irradiation increases the concentration of fixed positive charges at the Si-SiO_2 interface [66, 71], which intensifies the PSC effect and further increases the fluence requirement. Additionally, excess defects generated in the deeper part of the silicon substrate, where the PSC effect does not happen, and the defect requirement for thermal stability is not as high as the interface, as illustrated by the simulation results in Fig. 2.4. The additional resistivity generated by this excess defect has minimal effect on passive component performance improvement, as substrate loss becomes negligible above 1 kΩ-cm resistivity. The single irradiation used by previous studies [4, 5] could not solve this issue due to the inability to independently adjust the defect generation at the interface and in the deeper region.

To demonstrate this phenomenon, a comparison was performed between the Q-factor measurement of a 1.8 nH on-chip inductor manufactured in a standard CMOS 65 nm process and the spread resistance profiling (SRP) measurement of a bare Czochralski p-type (100) Si wafer with 4 Ω-cm initial resistivity. Both structures were irradiated with 4×10^{14} cm^{-2} proton fluence and measured before and after 1 minute 260°C annealing. The Q-factor degradation after annealing observed in Fig. 2.5(a) indicates that the effective substrate resistivity seen by the inductor was not thermally stable. However, the direct resistivity measurement at the deeper region in Fig. 2.5(b) did not change after annealing. These results show that the proton fluence of 4×10^{14} cm^{-2} generated enough defects to maintain thermally stable resistivity at the deeper regions but did not generate enough defects to prevent PSC layer formation at the Si-SiO_2 interface, resulting in degraded inductor performance. Hence, the fluence must be increased to prevent PSC layer formation, resulting in the 10^{15} cm^{-2} proton fluence requirement obtained in previous studies [4, 5] to achieve thermal stability.

2.6 Research Direction Summary

The analysis results of the conventional proton irradiation can be summarized as follows:

1. High proton fluence (> 10^{15} cm^{-2}) is required in conventional proton irradiation to

maintain thermal stability against typical high-temperature post-processing.

2. Due to the high proton fluence, irradiation time also increases, leading to longer machine time, lower throughput, and ultimately higher process costs.

3. Higher proton fluence also increases the concentration of the laterally scattered ion, increasing the distance where ion concentration is higher than transistor damage tolerance, and consequently increasing margin distance.

4. The minimum thermally stable proton fluence value from previous studies [4, 5] did not consider PSC effect, leaving a room to further reduce the thermally stable proton fluence.

From the analysis results above, the direction of research was determined as follows:

1. Propose a new process to reduce the overall proton fluence requirement by taking advantage of the knowledge about the PSC layer.

2. Devise a method to optimize the new process for obtaining the minimum thermally stable proton fluence value where the substrate resistivity level is high enough to prevent passive component degradation, which leads to reduction in irradiation time.

3. Devise a method to evaluate and verify the active device margin distance requirement on the optimized new process.

4. Apply the new process on several sub-THz on-chip passive components to investigate its effectiveness.

Chapter 3

Dual-Layer Proton Irradiation [1]

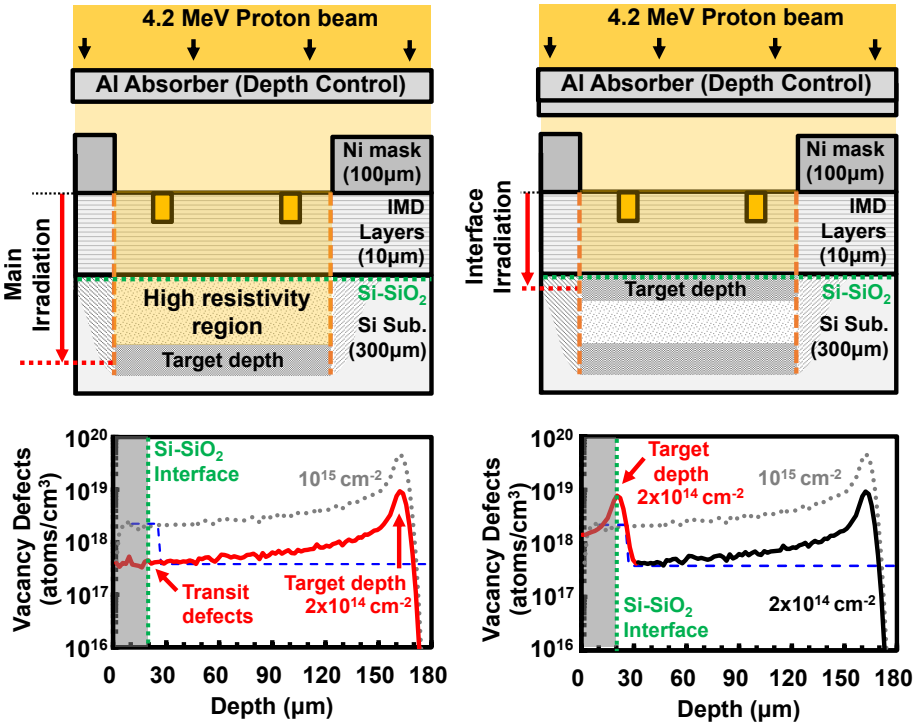
3.1 Process Overview

To efficiently achieve the different defect requirements at the interface and deeper region, a dual-layer proton irradiation profile was proposed with process details shown in Fig. 3.1. The additional irradiation targeted at the interface utilizes the increased defect generation at the target depth compared to the transit depth, which decreases the fluence requirement by up to a factor of 10 to generate the same amount of defects. The interface irradiation also removes the requirement on the main irradiation to generate interface defects, allowing the main irradiation fluence to only generate defects required for the deeper region, leading to the reduction of overall fluence requirement and the elimination of excess defects generation. The depth adjustment to perform interface irradiation was achieved by adjusting the thickness of the aluminum (Al) absorber.

3.1.1 Target Depth and Transit Depth Defects

It can be seen from the defects concentration graph in Fig. 3.1(a) that the target depth defects is around 10 times larger than transit defects within the narrow straggle range ΔR_p of 8 μm. This phenomenon happens due to the difference in energy loss between the high energy transit proton, and the low energy proton close to the target depth, which is shown in Fig. 3.2(a). It was explained in the subsection 2.3.3 that only nuclear energy loss generate defects, and energy loss in high energy proton is dominated by electronic loss. Therefore, the high energy transit proton is very inefficient in generating defects. As

[1] This chapter is based on "Dual-Layer Proton Irradiation for Passive Component Enhancement and Noise Coupling Suppression on CMOS Process" [42] by the same author, which appeared in the IEEE Transactions on Electron Devices, © 2024 IEEE. Some of the figures of this paper are reused from [42] under the permission of the IEEE.



(a) Step 1: Main Irradiation (b) Step 2: Interface Irradiation

Figure 3.1: The proposed dual-layer proton irradiation consists of (a) main irradiation and (b) interface irradiation. Expected defects generated by both steps were simulated with TRIM.

the proton becomes closer to the target depth, it gradually loses its energy and becomes a low energy proton, where the nuclear energy loss becomes higher and the likelihood of generating defects increases. Therefore, the defects increases until it peaked at the target depth. This behavior persists over different fluences, as shown in Fig. 3.2(b). Because the PSC-induced increase in defects requirement at the Si-SiO_2 interface is thinner (< 1 μm) than the straggle range at 4.2 MeV (around 8 μm), the target depth defects can be used to fulfill the requirement with 10 times lower fluence than in conventional case. And because the main irradiation does not have to generate defects at the interface, the fluence of the main irradiation can be reduced, resulting in reduction in the total fluence.

3.1.2 Depth Control

A target depth control mechanism is needed to perform two irradiations with different depths. As explained in subsection 2.3.1, one method to control proton penetration depth is by adjusting the proton energy. Fig. 3.3(a) shows the relationship of proton energy with penetration depth and straggle range. It can be seen that the penetration depth is

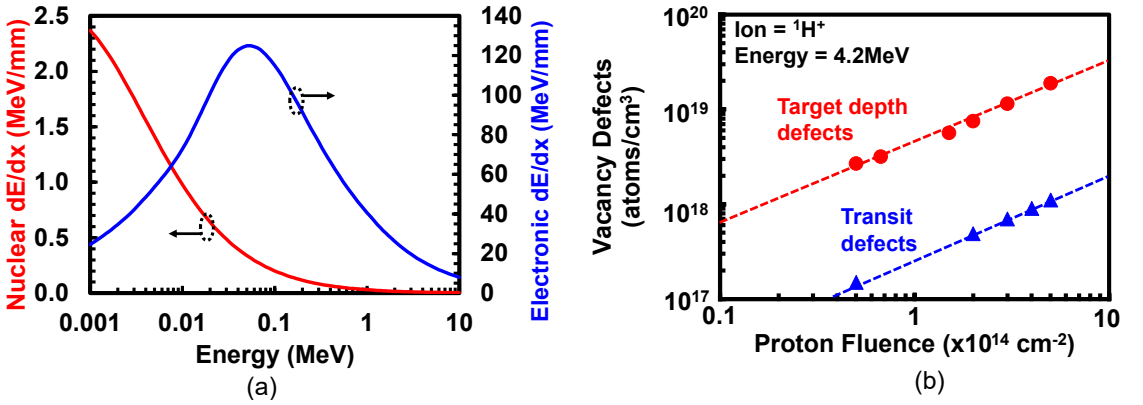


Figure 3.2: TRIM simulation of (a) nuclear and electronic energy loss across different proton energy, and (b) defects generated at target depth and transit depth across different fluences.

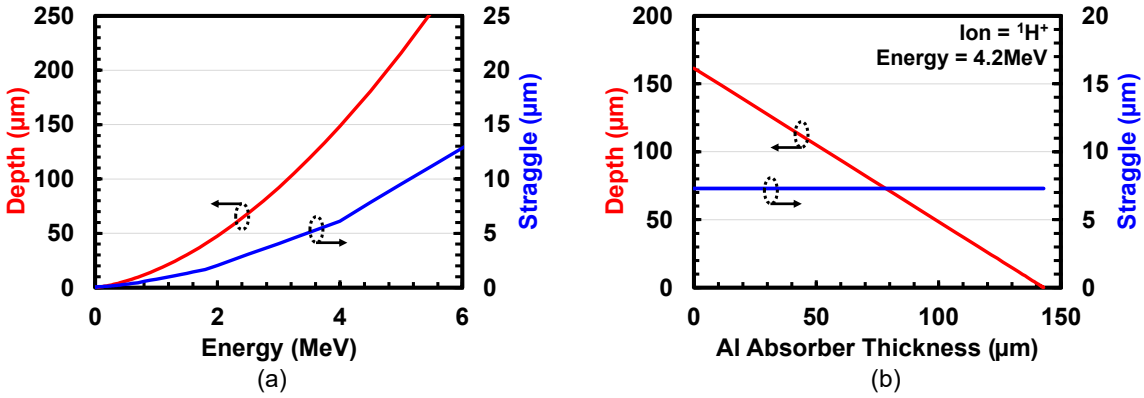


Figure 3.3: TRIM simulation of (a) penetration depth and straggle across different proton energy, and (b) penetration depth and straggle across different Al absorber thickness.

not linearly related with the proton energy. Furthermore, the straggle range change in proportion to the energy, becoming smaller for shallower depth. For the Si-SiO_2 interface at 10 μm deep, the straggle range is only around 0.5 μm, making it very sensitive to the inter-metal dielectric (IMD) thickness variation. Additionally, the proton accelerator need to support the required energy range and able to change quickly between the two energy state.

An alternative target depth control mechanism was achieved by putting an Al absorber above the target chip and adjusting its thickness according to the target depth, as shown in Fig. 3.3(b). This method was chosen over directly changing the proton energy due to a more linear relationship with target depth and no reduction in the ion straggle range at shallow target depth. Furthermore, the usage of Al absorber keeps the proton accelerator at a constant energy output, relaxing the accelerator requirement. A wider ion straggle

range allows a larger tolerance of absorber thickness error due to manufacturing variation. The chosen 4.2 MeV proton beam energy has a maximum penetration depth of 160 μm and an ion straggle range of around 8 μm, which allows a depth variation of ±4 μm before the defect concentration degrades by 50% from its peak value. This variation can be caused by thickness variation in the Al absorber, or additional interconnect metals covering the irradiated area. For each 1 μm thick Al interconnect, penetration depth will decrease by around 1 μm. While each micron thickness of Cu interconnect will decrease penetration depth by 1.9 μm. With thick enough interconnect, it is possible for interface irradiation to miss the Si-SiO_2 interface. Therefore, the dummy metal placement on the irradiated area should be avoided if possible, or kept less than 4 μm for Al and less than 2 μm for Cu. If the irradiated area is fully covered with metal (especially thick top metal), the interface irradiation target depth should be adjusted to take into account those interconnect metal thickness.

3.2 Process Optimization

3.2.1 Optimization Methodology

The proposed dual-layer proton irradiation process needs to be optimized to achieve the minimum fluence possible, while still maintaining thermal stability and achieve the resistivity required to prevent quality factor degradation of the passive components. To achieve this, a method to measure substrate resistivity needs to be devised. Direct resistivity measurement method such as spread-resistance profiling (SRP) [72] or spread-resistance microscopy (SRM) [73] require the chip samples to be cut diagonally, which prevent accurate measurement of resistivity under the PSC effect. This happens because the cutting process changes the fixed charge concentration in the oxide at the Si-SiO_2 interface. Furthermore, the diagonal cut reduces the oxide thickness above the interface, which can reduce or even eliminate the PSC effect on the measured sample. Another drawback is two different samples are required to measure the resistivity before and after annealing process due to the destructive nature of the measurement, which increases measurement cost and time.

Due to the factors mentioned above, indirect measurement method through a substrate-dependent on-chip passive component is preferred because of its non-destructive nature and quick measurement time. In this work, several on-chip 2-turn 1.8 nH inductors fabricated in a 65 nm CMOS process (Fig. 3.4(a)) was used to measure the substrate resistivity indirectly through the quality factor (Q-factor) measurement. The relation between Q-factor and substrate resistivity can be inferred from the simplified on-chip inductor model

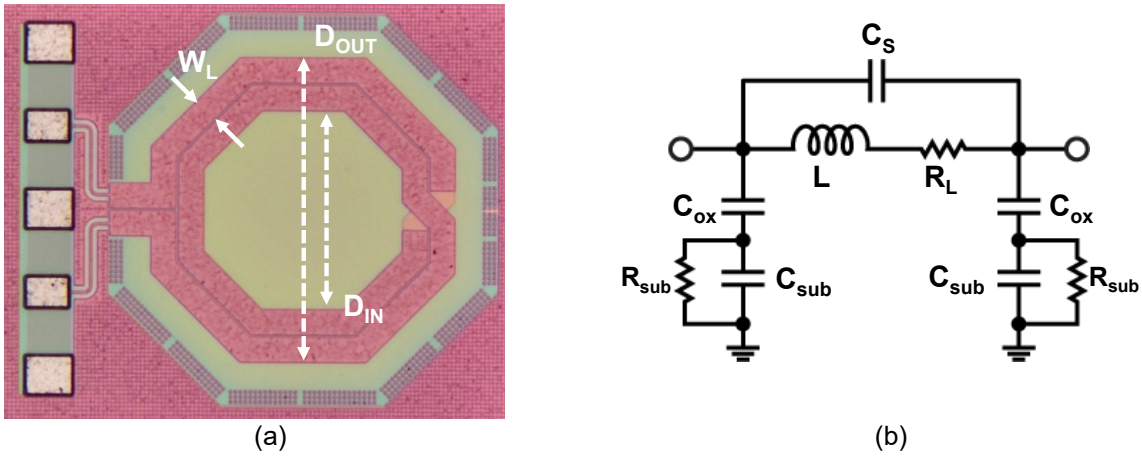


Figure 3.4: (a) Die micrograph of the on-chip 2-turn 1.8nH inductor manufactured in a standard 65 nm CMOS process used for process optimization. (b) The equivalent inductor model based on [6]. (Inductor parameters: D_{IN} = 240 µm, D_{OUT} = 366 µm, and W_L = 30 µm).

shown in Fig. 3.4(b) [6] as:

$$Q = \frac{\omega L(1-\omega^2 LC_s)}{R_L + \frac{(\omega^2 L^2 + R_L^2)}{R_{sub}}\left(\frac{C_{ox}}{C_{sub}+C_{ox}}\right)} \tag{3.1}$$

where R_{sub} is a parameter related to substrate resistivity (ρ_{sub}) as expressed in:

$$R_{sub} = F\rho_{sub} \tag{3.2}$$

where F is a variable that depends on inductor geometry and operating frequency, typically obtained from measurement [74, 75]. Therefore, the optimization process will be performed by comparing Q-factors across different annealing and irradiation conditions.

There are three process parameters that will be optimized: the depth of the main irradiation, the fluence of the main irradiation, and the fluence of the interface irradiation. The optimization of the main irradiation depth determines the minimum depth required to achieve the optimum Q-factor. The optimization of the main and interface irradiation fluence determines the minimum fluence required to for the measured Q-factor to be thermally stable. The heat treatment chosen for the fluence optimization processes are 260°C for 1 minute on a hot plate, emulating the thermal stress in a reflow soldering process [40].

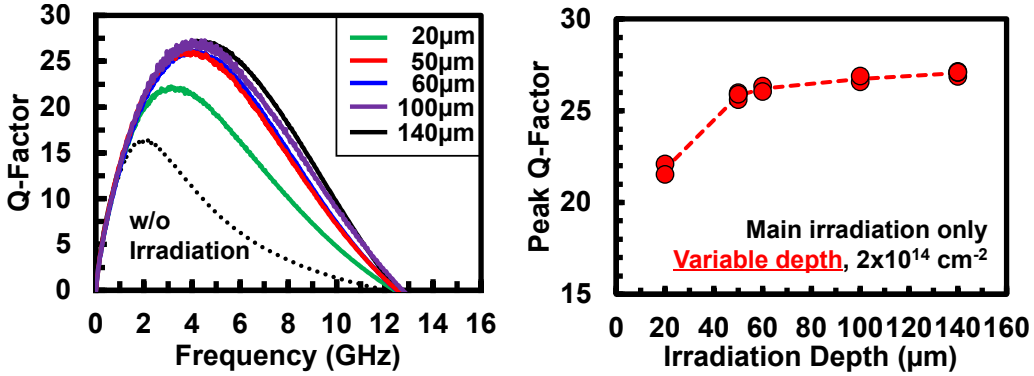


Figure 3.5: Measurement results of inductor Q-factor across different main irradiation depths.

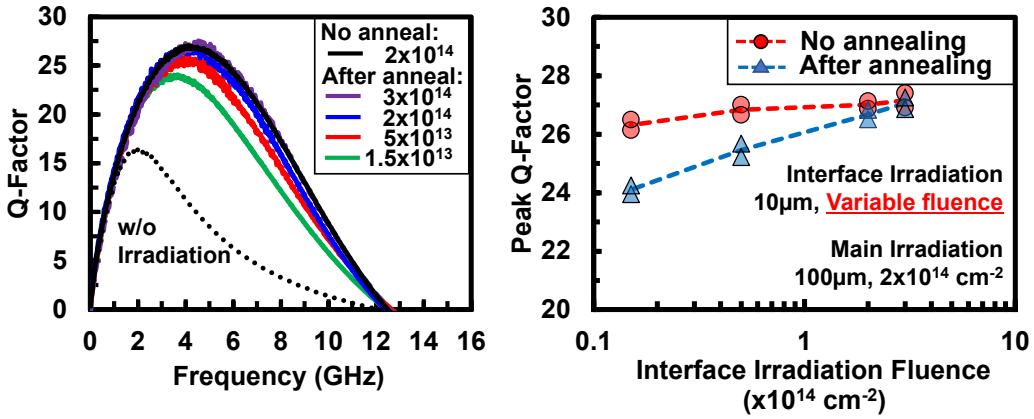


Figure 3.6: Measurement results of inductor Q-factor across different interface irradiation fluences before and after 1 minute 260°C annealing.

3.2.2 Optimization Results

The optimum main irradiation depth was investigated by irradiating several inductors with a constant proton fluence of 2×10^{14} cm^{-2} across various depths and comparing the measured Q-factor. The measurement results in Fig. 3.5 show how the Q-factor increase as the depth increase until around 60 µm depth, where the Q-factor starts to saturate and further increase in depth leads to minimum increase in Q-factor. It can be concluded that if possible, the main irradiation depth should be as deep as possible, covering the whole substrate thickness. However, if there are any constraints on the proton accelerator energy output, at least it should be able to achieve 60 µm, which corresponds to 2.5 MeV energy output. Therefore, the 4.2 MeV energy output used in this work is adequate to achieve optimum irradiation depth.

The minimum thermally stable fluence for interface irradiation was investigated by irradiating several inductors with various fluences at the interface while keeping the main

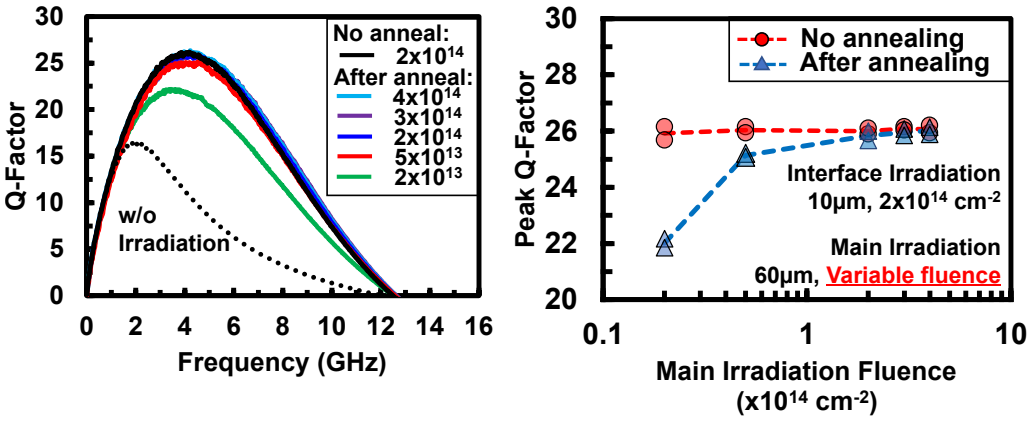


Figure 3.7: Measurement results of inductor Q-factor across different main irradiation fluences before and after 1 minute 260°C annealing.

Table 3.1: Optimized Irradiation Profile Summary

Condition	**Energy (MeV)**	**Fluence (cm^{-2})**	**Target Depth (μm)**	**Absorber (μm)**
Dual-Layer	4.2	2.0×10^{14} 2.0×10^{14}	10 (interface) 100 (main)	150 60
Conventional (for comparison)	4.2	4.0×10^{14}	160	N/A

irradiation constant at 100 μm depth with 2×10^{14} cm^{-2} proton fluence. The Q-factor was measured before and after 1-minute 260°C annealing. The measurement results in Fig. 3.6 shows how the peak Q-factor degrades after annealing if the interface irradiation fluence is too low. At least 2×10^{14} cm^{-2} proton fluence was required to suppress the post-anneal Q-factor degradation to around 1%, which indicates a successful PSC formation prevention at the Si-SiO_2 interface for the 4.2 MeV proton energy case.

The minimum thermally stable fluence for main irradiation was investigated with the same method previously used on interface irradiation, with the main irradiation as the variable while the interface irradiation is kept constant at 60 μm depth and 2×10^{14} cm^{-2} proton fluence instead. The measurement results in Fig. 3.7 show that at least 2×10^{14} cm^{-2} proton fluence is required to prevent thermal resistivity degradation at the deeper region inside the substrate.

The optimized dual-layer irradiation process is summarized in Table 3.1, with a conventional profile with the same total fluence added for comparison purpose. The interface irradiation target depth of 10 μm is optimized for no metal interconnect case, and should be increased accordingly if the irradiated area is covered by thick metal layer.

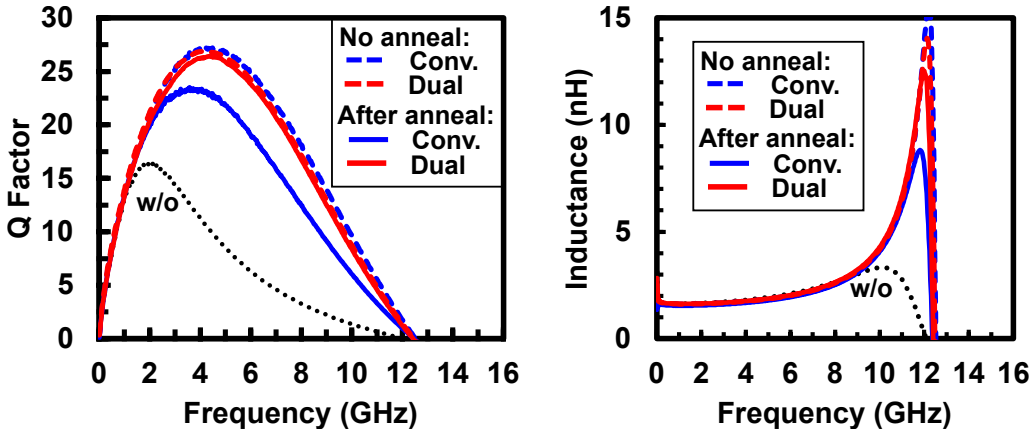


Figure 3.8: Measurement results of inductor Q-factor across different main irradiation fluences before and after 1 minute 260°C annealing.

3.3 Evaluation of the Optimized Process

3.3.1 Inductor Evaluation

This final dual-layer profile was tested and compared with the conventional profile with the same total fluence on the on-chip inductor in Fig. 3.4(a), with measurement results shown in Fig. 3.8. From the measurement results, the proposed dual-layer proton irradiation profile was able to reduce post-annealing peak Q-factor degradation from around 14% (27.1 to 23.3) in conventional irradiation to around 1% (26.8 to 26.5) at the same total fluence. This result also shows that the dual-layer proton irradiated substrate could achieve thermal stability with a total fluence of 4.0×10^{14} cm^{-2}, a 60% reduction compared to conventional irradiation, where a fluence of 10^{15} cm^{-2} is typically required for thermal stability [4, 5]. No change in inductance value and self-resonant frequency was observed, indicating that proton irradiation has a negligible effect on metal conductivity and dielectric permittivity of the oxide layer and the substrate.

3.3.2 Metal Conductivity Evaluation

To further evaluate the effect of irradiation on metal conductivity, a meandering metal structure shown in Fig. 3.9 was fabricated in a standard 180 nm CMOS process. The structure consists of a meandering metal 1 line and a meandering metal 6 line with length of 151 mm and 15.3 mm, respectively. Both lines are designed with minimum width allowable by the design rule. DC pads are used to connect the line with the voltage source, consisting of force and sense pads connected in parallel to eliminate the effect of probe and cable when resistivity measurement is performed. The resistivity measurement for

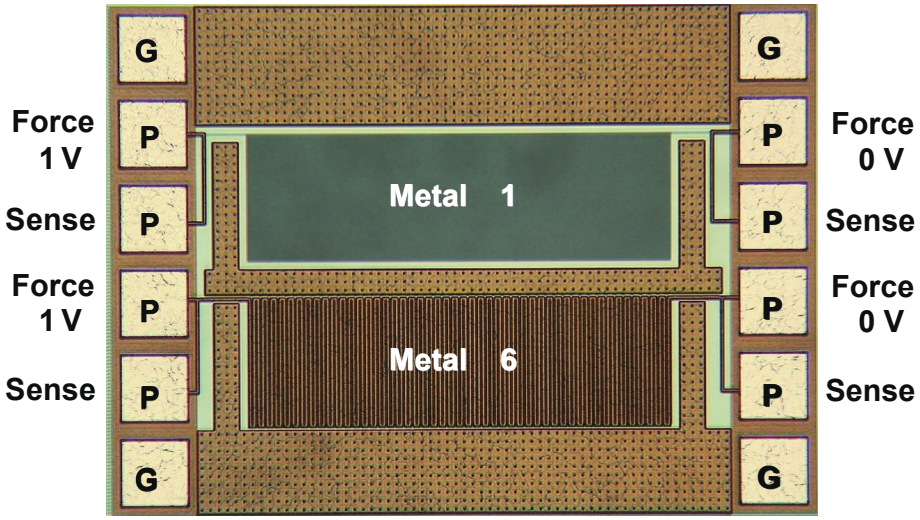


Figure 3.9: The structure fabricated in a standard 180 nm CMOS to evaluate change in metal conductivity after irradiation.

Table 3.2: Irradiation Effect on Metal Resistivity

	Resistivity (kΩ)	
	Before Irradiation	**After Irradiation**
M1	50.7	51.2
M6	35.8	35.5

both lines were performed before and after dual-layer proton irradiation with the profile listed in Table 3.1, with results summarized in Table 3.2. The resistivity variation after irradiation for both metal lines are less than 1%, which is lower than instrument error and process variation. Therefore, it can be concluded that the optimized dual-layer proton irradiation process has no effect on metal conductivity on DC measurement. While proton irradiation creates defects on copper surface with average diameter around 2 nm [76], this irradiation induced defects is much smaller than the 9.5 nm RMS roughness of the copper metal in CMOS processes [77]. Therefore, additional losses due to irradiation at 300 GHz is less than 0.05 dB when calculated using improved Hurray surface roughness model [78].

3.3.3 Margin Distance Evaluation

The structure shown in Fig. 3.10 was manufactured in a 180 nm CMOS process to measure the minimum margin distance required between the active device and the edge of irradiation area (mask edge) to prevent radiation-induced damage. The structure consists

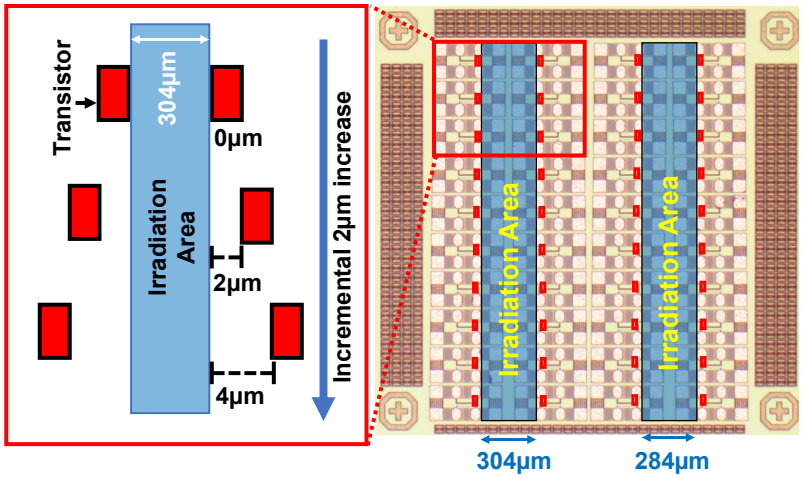
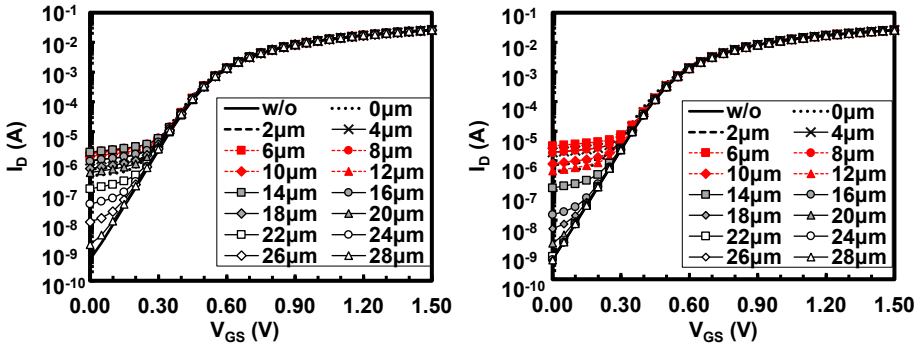


Figure 3.10: The structure fabricated in a standard 180 nm CMOS to evaluate margin distance requirement from the mask edge (Transistor parameters W = 2 µm, L = 200 nm, and finger = 30).



(a) Conventional (b) Dual-layer

Figure 3.11: Measured I_D-V_{GS} characteristics of transistors within 0 µm to 28 µm distance from the mask edge after irradiation with (a) conventional and (b) dual-layer profile listed in Table 3.1.

of 20 pairs of transistors placed at the mask edge, with a 2 µm incremental transistor-to-mask-edge distance increase between each successive pair, covering a range from 0 to 28 µm. This transistor pair structure was used to enable the detection and correction of mask misalignment. The increment of the transistor-to-mask-edge distance determines the resolution of the structure, which is 2 µm in this case. The transistor was connected with two GSSG probe for connection to the gate, source, drain, and body; which then connected to the E5270B DC measurement mainframe to measure the transistor DC characteristics.

To investigate the difference between conventional and dual-layer proton irradiation, two structures was fabricated, with each irradiated with conventional and dual-layer profiles from Table 3.1. The I_D-V_{GS} measurement result for both cases are shown in Fig. 3.11. The transistor damage caused by the irradiation mainly affects the leakage current,

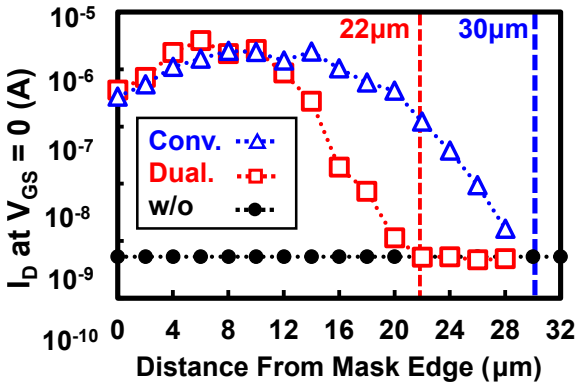


Figure 3.12: Comparison of transistor leakage current at V_{GS} = 0 across all measured distances from Fig. 3.11 to determine the margin distance requirement of conventional and dual-layer proton irradiation.

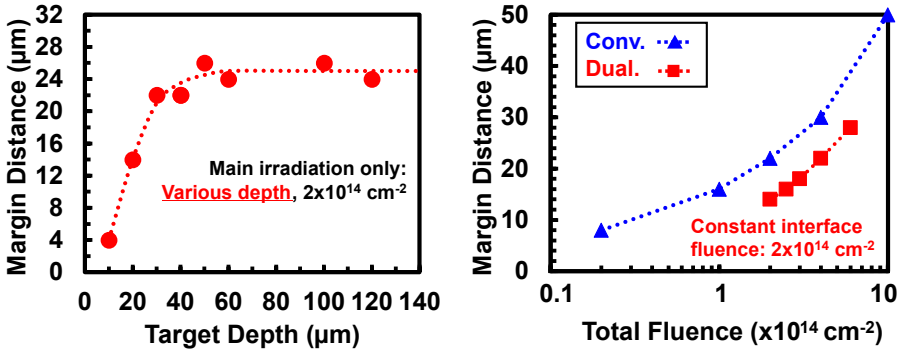


Figure 3.13: (a) Measured margin distance across different target depths, and (b) measured margin distance across different total fluence on conventional and dual-layer proton irradiation.

which can be seen from the increase in leakage current at V_{GS} = 0. Then, the leakage current at V_{GS} = 0 was plotted over distances from the mask edge to identify the minimum distance required for the transistor to remain undamaged by the irradiation, resulting in the plot shown in Fig. 3.12. The measured margin distance for the optimized dual-layer proton irradiation profile was 22 µm, which is a 56% reduction compared to the 50 µm required in thermally stable conventional proton irradiation with 10^{15} cm^{-2} fluence [5], and a 26% reduction compared to the 30 µm required in conventional proton irradiation with the same fluence.

To investigate the cause of improvement, the previous measurements were repeated with constant fluence across various depths and various total fluences for both conventional and dual-layer irradiation. Measurement results in Fig. 3.13(a) show that below 60 µm, the margin distance decreased in proportion to the target depth. In the dual-layer case, the margin distance caused by the interface irradiation at 10 µm was covered by the

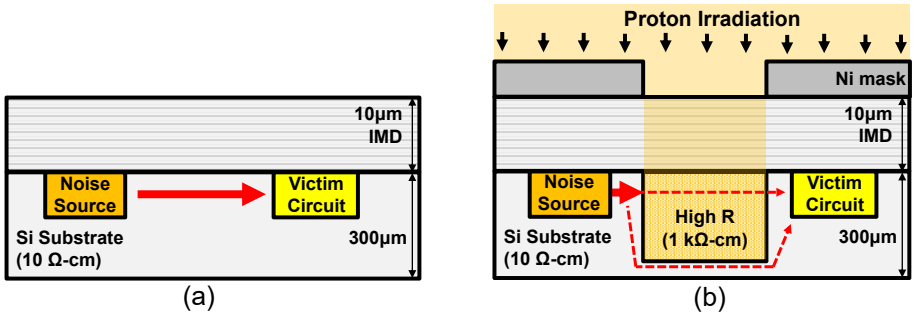


Figure 3.14: Substrate noise coupling mechanism: (a) normal condition, (b) with high resistivity guard-band formed through irradiation.

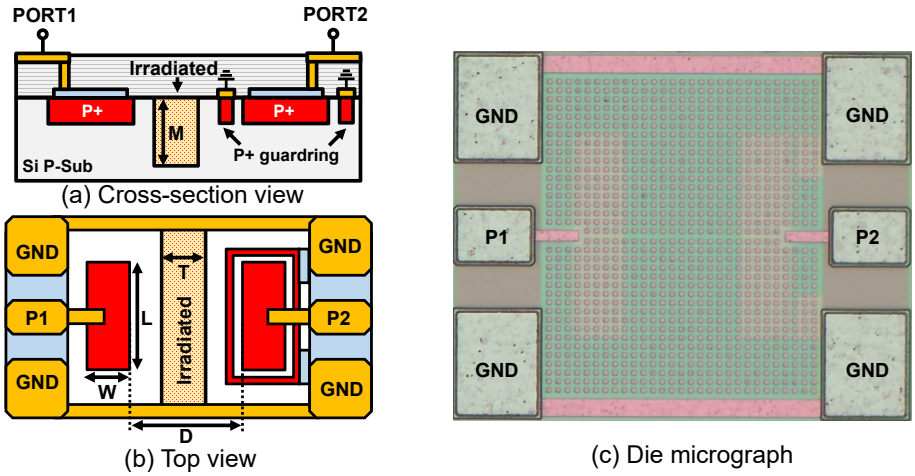


Figure 3.15: The structure fabricated in a standard 65 nm CMOS process to evaluate noise coupling suppression (W = 35 μm, L = 140 μm, and D = 100 μm). The effect of guard-band thickness T and depth M on noise suppression were investigated.

larger margin distance caused by the main irradiation at 100 μm. Therefore, the margin distance in dual-layer case was determined solely by the main irradiation fluence, which was only half of the conventional fluence for the profiles in Table 3.1, resulting in margin distance reduction. Comparison between conventional and dual-layer cases measured in Fig. 3.13(b) also shows that the margin distance in the dual-layer case was similar to the conventional case when only the main irradiation fluence (total fluence minus interface fluence) was considered.

3.3.4 Noise Isolation Evaluation

The ability to control the location and shape of the irradiated area enables the creation of a high-resistivity guard-band. As shown in Fig. 3.14, this guard-band separates the noise-generating area from other parts of the chip, which helps to reduce substrate noise

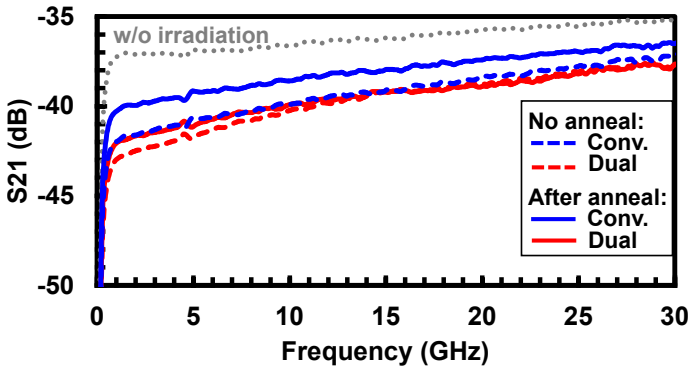


Figure 3.16: Measured transmission coefficient of conventional and dual-layer guard-band before and after 1 minute 260°C annealing.

coupling.

To investigate the noise suppression capability of the guard-band, a two-tap structure was fabricated in a standard 65 nm process, with detailed dimensions shown in Fig. 3.15. A guard-band with a specific thickness (T) and depth (M) was formed between the two taps through proton irradiation. The noise coupling between the two taps was measured through the transmission coefficient (S21) obtained from a network analyzer, and the noise suppression value was determined by comparing the S21 before and after the guard-band formation. The comparison of noise suppression and thermal stability performance between the guard-bands (T = 20 μm) formed by conventional and dual-layer irradiation is shown in Fig. 3.16. Both cases achieved a similar 5 dB noise suppression at 1 GHz before annealing. However, the guard-band in the dual-layer case maintained the 5 dB noise suppression after annealing, while in conventional case, the noise suppression degraded to 3 dB. This thermal behavior remains consistent for both cases until 30 GHz. However, as the frequency increases to 30 GHz, the post-anneal noise suppression gradually decreased to 1.5 dB for the conventional case and 3 dB for the dual-layer case.

The impact of guard-band thickness (T) and guard-band depth (M) on noise suppression was examined on the guard-bands created through dual-layer proton irradiation. Fig. 3.17 shows the measured noise suppression across T values from 20 μm to 80 μm. The results indicate an additional increase of 2.5 dB noise suppression for each doubling of T at 1 GHz, which gradually decrease to 2 dB at 15 GHz and 1 dB at 30 GHz. The effect of M on noise suppression was investigated by changing the main irradiation depth from 40 μm to 140 μm, while keeping the interface irradiation condition constant at 2×10^{14} cm^{-2} fluence and 10 μm target depth. Measurement results in Fig. 3.18 show negligible change in noise suppression when the main irradiation depth was varied between 40 μm to 140 μm.

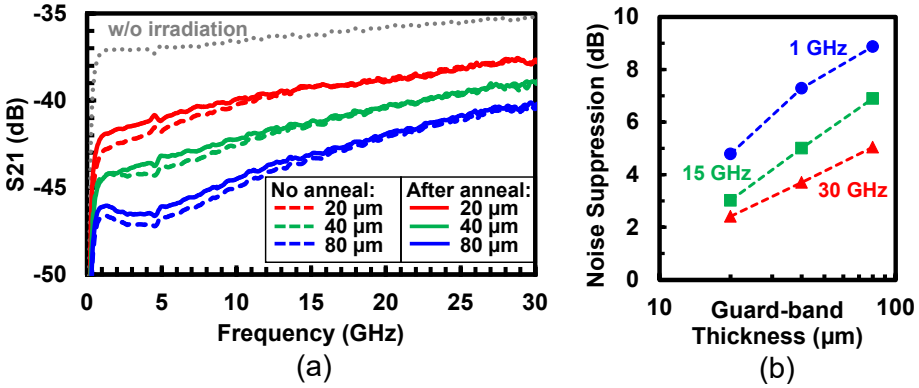


Figure 3.17: (a) Measured transmission coefficient of dual-layer guard-bands with different thicknesses (T) before and after 1 minute 260°C annealing, and (b) summarized post-anneal noise suppression measurement for different guard-band thicknesses at 1 GHz, 15 GHz, and 30 GHz.

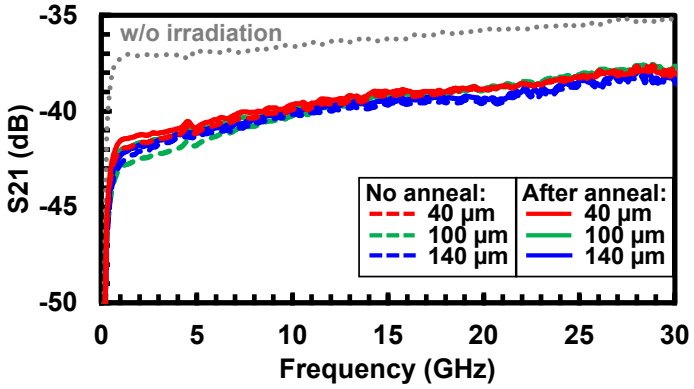


Figure 3.18: Measured transmission coefficient of dual-layer guard-bands with different main irradiation depths (M) before and after 1 minute 260°C annealing with interface irradiation parameters kept constant.

3.4 Conclusion

In this work, the dual-layer proton irradiation profile was formulated from parasitic surface conduction analysis and successfully optimized to reduce the total fluence requirement to achieve thermal stability. The optimized dual-layer profile reduced the total fluence requirement by 60%, from 10^{15} cm^{-2} in conventional irradiation to 4×10^{14} cm^{-2}, leading to a proportional reduction in machine operational time and energy costs. The reduction in the total fluence requirement also reduces the mask-edge margin distance requirement from the active devices by 56%, from 50 µm to 22 µm, increasing the available area for design. The guard-band formation using dual-layer proton irradiation to suppress substrate noise coupling from the noise-generating area has been demonstrated, resulting

in 5 dB noise coupling suppression at 1 GHz for 20 μm thick guard-band, with a further 2.5 dB increase every time the thickness was doubled.

Chapter 4

300GHz-Band CMOS On-Chip Vivaldi Antenna [1]

4.1 Introduction

In recent years, research on 300 GHz band (220 GHz to 320 GHz) transceivers (TRX) has uncovered a lot of potential for applications such as imaging [80–82], radar [27, 83–86], and ultra-high speed communication [3, 87–91]. The large available bandwidth can be utilized to improve radar spatial resolution or achieve the Tb/s data rates required for future 6G wireless communication systems [1]. The sub-millimeter wavelength reduces antenna size to the point where on-chip antenna (OCA) implementation is possible, eliminating additional losses, parasitics, and variations introduced by chip-to-PCB interconnects [24, 25]. However, the 300 GHz band has a significant path loss [22] and cannot penetrate through obstacles. Adding a lens on top of an OCA [82–85, 92] compensates for the path loss with the high lens gain. However, the narrow beamwidth and the static radiation pattern necessitate external mechanical parts for beam steering to detect or avoid obstacles. Such mechanical parts are undesirable as they increase system size and complexity. A phased array antenna implementation satisfies the high gain and electronically controlled beam steering requirement [23]. The sub-millimeter-sized antenna enables the implementation of many elements within the same area footprint typically occupied by a single sub-10 GHz antenna. Furthermore, the feasibility of TRX implementation using a standard CMOS process has been demonstrated [3, 27, 87–90], promising low cost, high yield, and large production capacity needed to manufacture the required high number of

[1] This chapter is based on "A Proton Irradiated CMOS On-Chip Vivaldi Antenna for 300 GHz Band Slat Array Implementation" [79] by the same author, which appeared in the IEEE Open Journal of Antennas and Propagation,

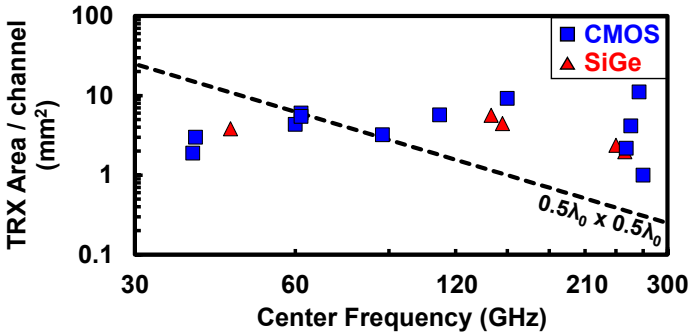


Figure 4.1: Survey of TRX chip area in relation to center frequency on CMOS and SiGe BiCMOS process.

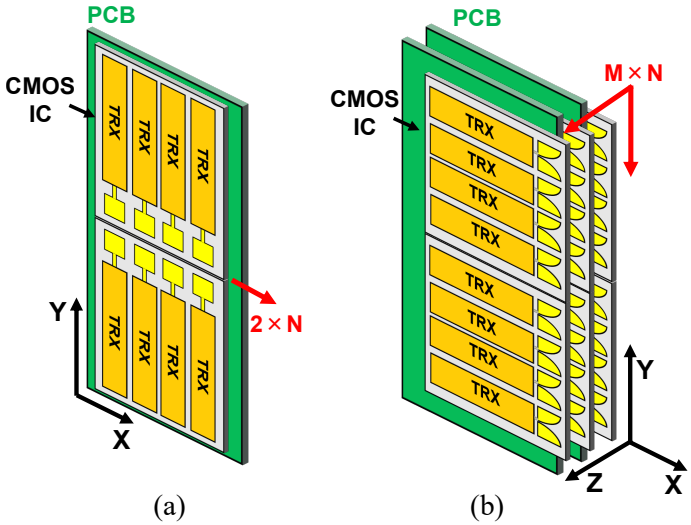
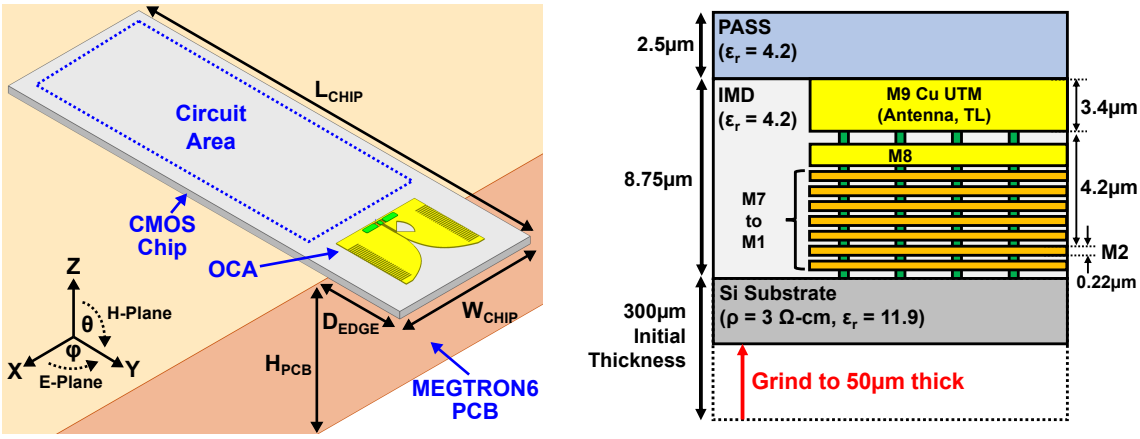


Figure 4.2: 300 GHz band phased array implemented as (a) tile array, and (b) slat array.

elements.

The implementation of a phased array below 60 GHz is typically done in tile configuration [93–95] due to the ease of assembly, simplicity, and lower cost [96]. However, the TRX chip area survey in Fig. 4.1 shows that as the frequency increases above 60 GHz, the TRX chip area stays roughly the same [26, 97–103], while the $0.5\lambda_0 \times 0.5\lambda_0$ tile area limit keeps shrinking until it becomes smaller than the TRX area (λ_0 is the wavelength in free space). The TRX shape can be modified to only maintain less than $0.5\lambda_0$ length at one side [26, 27], forming a tile array depicted in Fig. 4.2(a). However, the array scalability is decreased from M×N into 2×N, which reduces array density and area efficiency. The slat array implementation using end-fire OCAs, shown in Fig. 4.2(b), eliminates the TRX area limitation by introducing a third dimension to expand the array, restoring the array scalability to M×N. However, end-fire OCA performance on sub-terahertz frequency suffers from the surface wave effect and resistive loss induced by the high per-



(a) (b)

Figure 4.3: (a) Overall single-element Vivaldi OCA implementation structure, and (b) process cross-section of the standard 65-nm CMOS process used. (L_{CHIP} = *3 mm*, W_{CHIP} = *0.75 mm*, D_{EDGE} = *0.4 mm*, H_{PCB} = *3 mm*)

mittivity (ϵ_r = 11.9) and low resistivity (around 3 to 15 Ω·cm) of the silicon substrate used in the standard CMOS process [32, 104]. Furthermore, simple substrate isolation methods commonly implemented in broadside OCAs, such as bottom metal shielding [28, 30, 31, 105–107] and artificial magnetic conductors (AMC) [108], cannot be applied to the end-fire antenna. Therefore, most end-fire OCAs were either implemented on a separate low-loss substrate like quartz [109] and glass [110] or utilized a special etching technique to remove the silicon substrate below the antenna [111, 112], resulting in more complex design fabrication and integration. A fully in-process end-fire OCA implementation has been demonstrated in the SiGe BiCMOS process [113]. However, the silicon substrate in the SiGe BiCMOS process has a higher substrate resistivity (around 50 Ω·cm) compared to the standard CMOS process, which significantly reduces degradations due to the substrate resistive loss.

In this chapter, an end-fire 300 GHz band Vivaldi OCA fabricated on the standard 65-nm CMOS process is proposed. The Vivaldi architecture was chosen for being a wideband end-fire antenna that can cover 220 GHz to 320 GHz frequency. Because single-element gain becomes less important for large-scale arrays, the Vivaldi OCA was optimized for wide 3-dB beamwidth and high efficiency, resulting in a shorter antenna length and smaller area than the typical gain-optimized Vivaldi antenna. Comb-shaped slots were added to prevent back radiation from happening due to the short length. To improve efficiency, the substrate was thinned to 50 μm to prevent the excitation of higher mode surface waves, and the dual-layer proton irradiation was applied to raise the substrate resistivity without modifying the existing CMOS process.

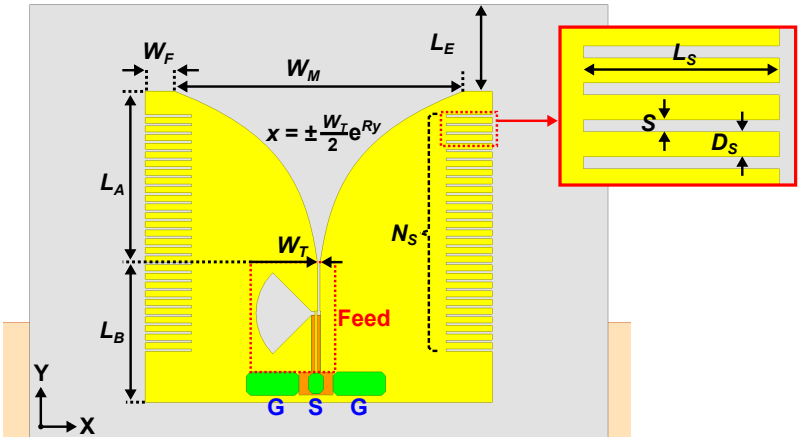


Figure 4.4: Structure and parameters of the proposed Vivaldi OCA. (R = 3, W_M = 450 μm, W_F = 25 μm, W_T = 5 μm, L_A = 300 μm, L_B = 200 μm, L_E = 150 μm, L_S = 80 μm, S = 5 μm, D_S = 10 μm, N_S = 28)

4.2 Antenna Design

4.2.1 Antenna Structure and Operating Principle

Fig. 4.3(a) shows the overall implementation of the proposed Vivaldi OCA. The chip size, the antenna placement on the chip, and the chip placement on the PCB were made to closely replicate a single 300 GHz band TRX implementation. Fig. 4.3(b) shows the cross-section of the standard 65-nm CMOS process used to implement the Vivaldi OCA, consisting of nine copper metal layers enclosed with 8.75 µm silicon dioxide inter-metal dielectric (IMD) and 2.5 µm passivation layer formed above the silicon substrate with permittivity and resistivity of 11.9 and 3 Ω·cm, respectively.

The Vivaldi OCA was implemented at the top metal (M9), with the detailed structure shown in Fig. 4.4. The antenna radiates through the traveling-wave mechanism [114] formed by the exponential-tapered slot defined by:

$$x(y) = \pm\frac{W_T}{2}e^{Ry} \tag{4.1}$$

with x as the distance from the central y-axis, growing from the initial slot opening W_T with the exponential rate of R, and ends at aperture width W_M, resulting in total taper length of L_A. Theoretically, the feeding structure limits the upper-frequency cutoff, while W_M determines the lower frequency cutoff f_L as defined by [115, 116]:

$$W_M = \frac{c}{2f_L\sqrt{\epsilon_r}} \tag{4.2}$$

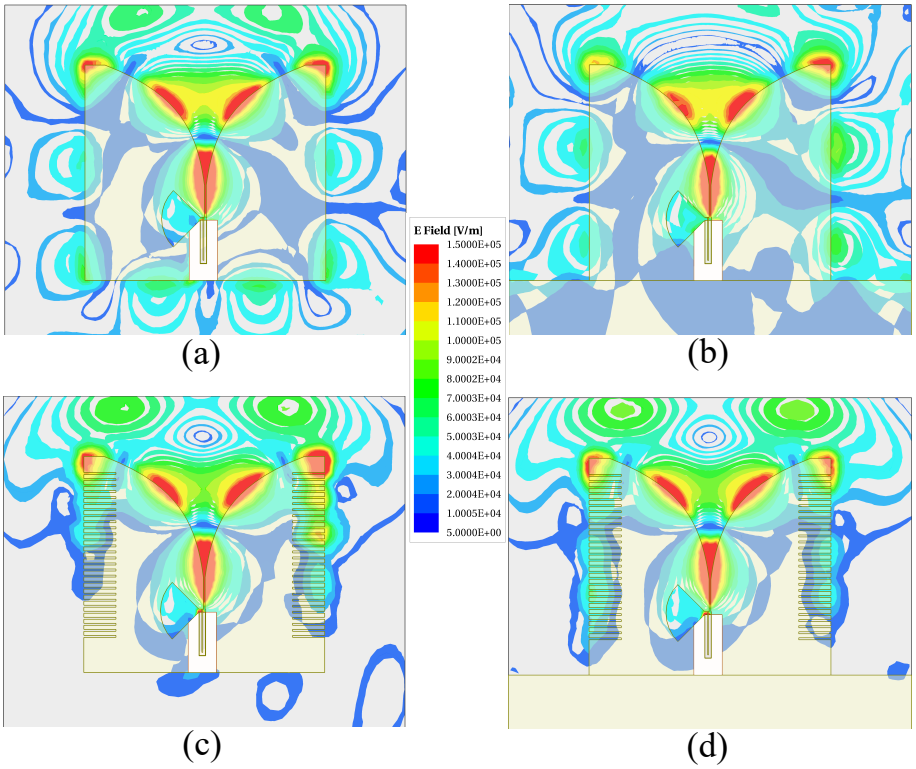


Figure 4.5: Comparison of simulated Vivaldi OCA E-field at 320 GHz between smooth flare edge (a) without reflector, (b) with reflector, and comb-shaped slots flare edge (c) without reflector, (d) with reflector.

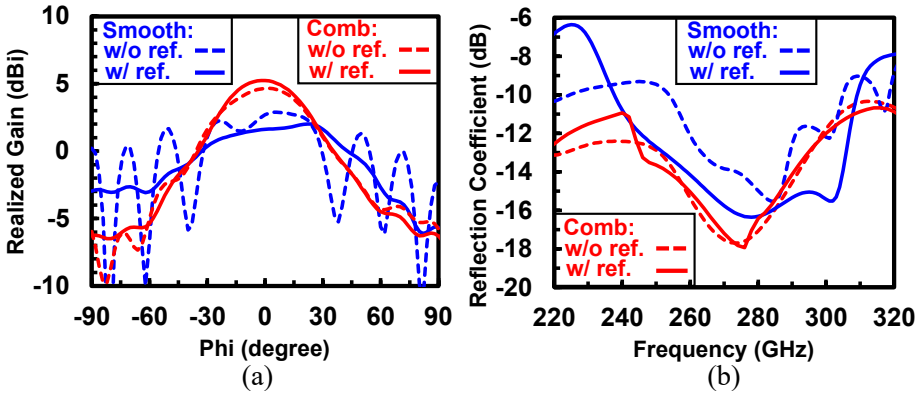
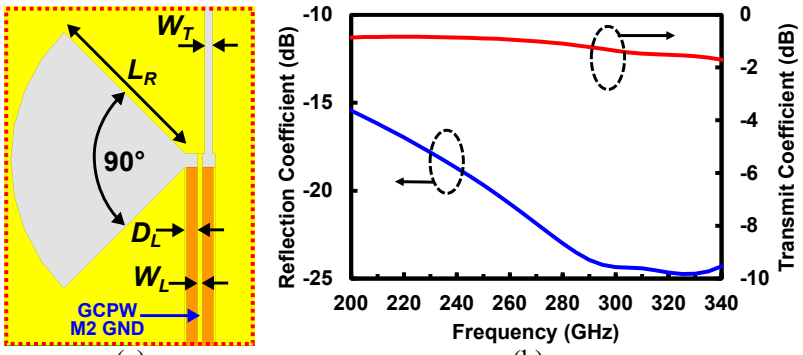


Figure 4.6: Comparison of simulated (a) E-plane realized gain pattern at 320 GHz and (b) reflection coefficient between smooth and comb-shaped flare edge, both with and without reflector.

The aperture width W_M also directly proportional to the directivity and inversely proportional to the beamwidth of the antenna. However, due to the optimum R value usually kept constant, the tapper length L_A indirectly affects aperture width, making it also proportional to the directivity and inversely proportional to the beamwidth [116, 117]. Therefore, optimizing for maximum beamwidth leads to shorter L_A, with added benefits of area



(a) (b)

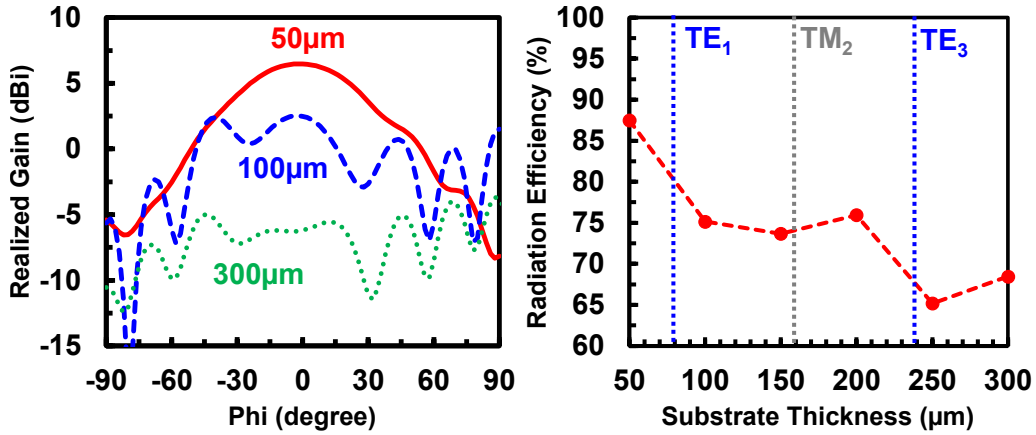
Figure 4.7: (a) Slotline radial stub feeding structure, and (b) the simulation results of the feeding structure in back-to-back configuration. (L_R = *100 µm*, W_T = *5 µm*, W_L = *2.5 µm*, D_L = *7.25 µm*)

reduction. However, there is a limit on how short the L_A is before the antenna deviates from the typical traveling-wave antenna behavior [116]. This anomalous behavior can be attributed to the increasing non-radiated energy flowing backward through the outer side of the flare as the L_A becomes shorter and a high permittivity substrate is used. This excess energy can interact with structures outside the antenna and cause problems such as unwanted side lobes, resonance, and circuit interference. The antenna characteristics also become more sensitive to structural change outside the antenna, as illustrated by the significant changes of the radiation pattern in Fig. 4.6(a) and reflection coefficient in Fig. 4.6(b) due to additional reflector placed at the back of the antenna (Fig. 4.5(a) and 4.5(b)). Therefore, comb-shaped slots were added to the outer side of both antenna flares to increase the path impedance at those locations, forcing more energy to radiate forward and preventing further flow to the back of the antenna, as shown in Fig. 4.5(c) and 4.5(d). Consequently, the antenna characteristics become more resistant to structure variations outside the antenna, as shown in Fig. 4.6. The slot length L_S was set approximately by the following [118]:

$$L_S = \frac{0.25\lambda_0}{\sqrt{\epsilon_r}} \tag{4.3}$$

with λ_0 denoting the wavelength at the center frequency. The slots should cover the whole flare outer sides to maximize the suppression of the energy back flow.

Fig. 4.7(a) shows the slot line radial stub feeding structure used to convert the grounded co-planar waveguide (GCPW) transmission line to the slot line mode of the Vivaldi OCA. This architecture was chosen because it provides the largest bandwidth compared to other planar CPW-to-slot line transitions [119]. The back-to-back structure simulation in Fig. 4.7(b) shows that the coverage of this feeding structure exceeded the target design frequency (220 GHz to 320 GHz), ensuring that the antenna bandwidth is not limited by the



(a) (b)

Figure 4.8: The simulated effect of substrate thickness at 270 GHz on (a) E-plane realized gain pattern and (b) efficiency of the Vivaldi OCA.

feeding structure.

4.2.2 Effect of Higher-Mode Surface Wave

At the 300 GHz band, the 300 μm thick silicon substrate used in the 65-nm CMOS process enables the excitation of higher transverse electric (TE) and transverse magnetic (TM) modes within the substrate, reducing radiation efficiency and distorting the radiation pattern. The relationship between substrate thickness (d) and the cutoff frequency (f_c) of the TE and TM modes n for both grounded (g) and ungrounded (ug) substrates are given as follows[104]:

$$d_g = \frac{nc}{4f_c\sqrt{\epsilon_r\mu_r - \epsilon_0\mu_0}}, \begin{cases} n = 1,3,5,...\text{for TE} \\ n = 0,2,4,...\text{for TM} \end{cases} \tag{4.4}$$

$$d_{ug} = \frac{nc}{2f_c\sqrt{\epsilon_r\mu_r - \epsilon_0\mu_0}}, \begin{cases} n = 0,1,2,...\text{for TE} \\ n = 0,1,2,...\text{for TM} \end{cases} \tag{4.5}$$

where c, ϵ_r, and μ_r are the speed of light, substrate dielectric permittivity, and substrate dielectric permeability, respectively. Therefore, the substrate thickness must be reduced until the cutoff frequency of TE_1 and TM_1 mode is higher than the maximum operating frequency of the antenna. Because the Vivaldi OCA metal structure behaves like a large ground cover, (4.4) was used to determine the suitable substrate thickness. The substrate thickness value of 50 μm was chosen to ensure that the higher order modes above 320 GHz are suppressed while the chip maintains enough structural integrity for further post-

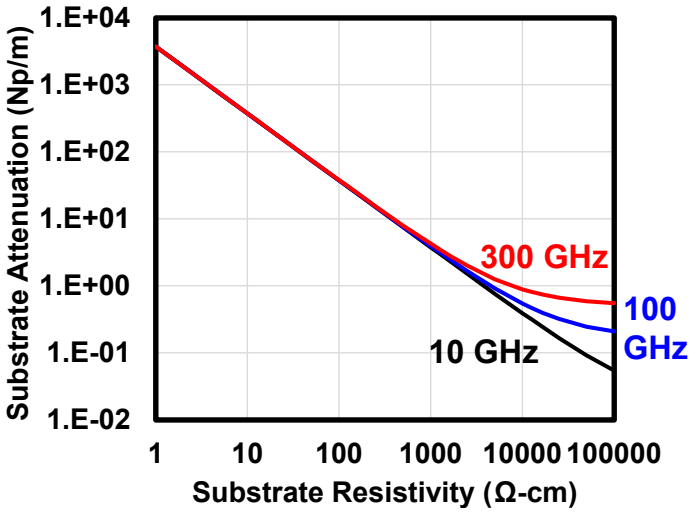


Figure 4.9: The substrate attenuation per meter.

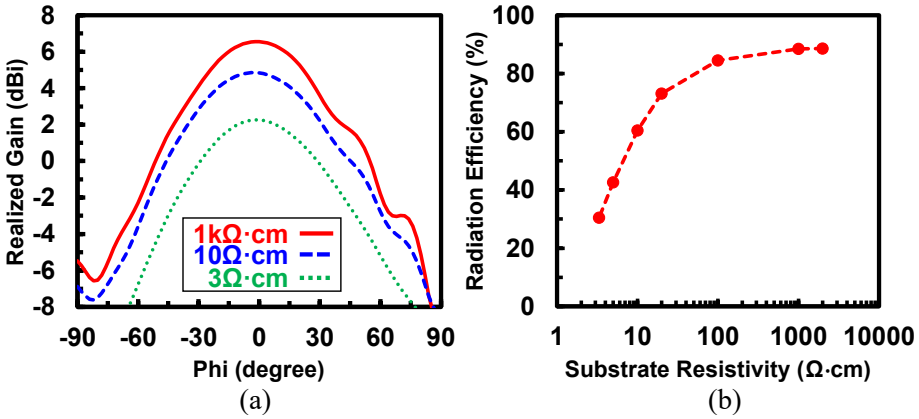


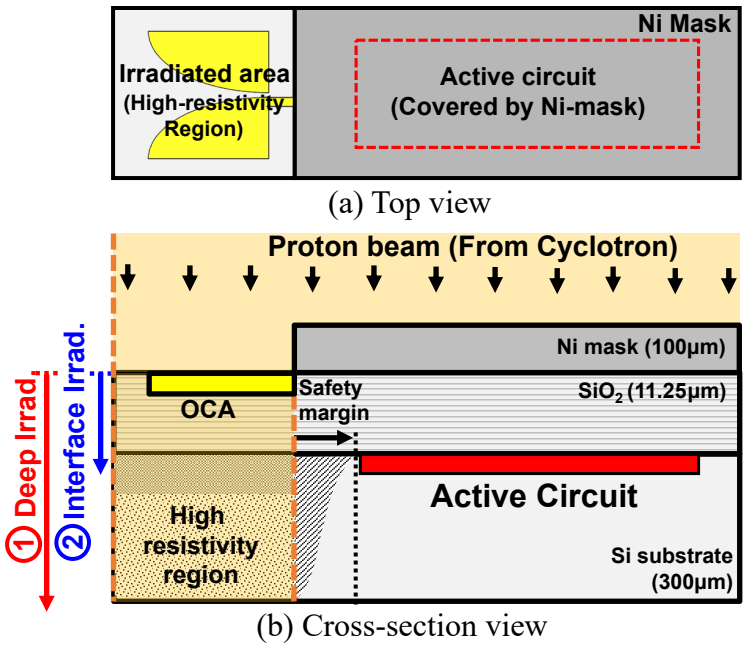
Figure 4.10: The simulated effect of substrate resistivity at 270 GHz on (a) E-plane realized gain pattern and (b) efficiency of the Vivaldi OCA.

processing. Fig. 4.8(a) shows how reducing the substrate thickness to 50 µm eliminates distortion on the radiation pattern. Fig. 4.8(b) also shows how the efficiency decreases as more TE modes get excited with increasing thickness.

4.2.3 Effect of Dual-Layer Proton Irradiation

The 3 Ω·cm resistivity of the substrate used in the 65-nm CMOS process increases the attenuation of the exponential slot-line of the Vivaldi antenna, reducing its gain and efficiency. Which can be explained by approximating the exponential taper as a variable width slot-line with propagation constant of [120, 121]:

$$\gamma = \alpha + j\beta \tag{4.6}$$



(a) Top view

(b) Cross-section view

Figure 4.11: The (a) top view and (b) cross-section view of the dual-layer proton irradiation process.

where β is the phase constant, and α is the attenuation constant, which further divided into conductor attenuation α_c and substrate attenuation α_d [121]. α_c is structure dependent and can be ignored in this analysis, while the α_d can be described as:

$$\alpha_d = \frac{\pi}{\lambda_0} \frac{\epsilon_r}{\epsilon_r - 1} \frac{\epsilon_{eff} - 1}{\sqrt{\epsilon_{eff}}} tan\delta \tag{4.7}$$

where ϵ_r is the relative dielectric constant (11.8 in silicon), λ_0 is the free-space wavelength, and ϵ_{eff} is the effective permittivity of the slot-line, which can be approximated as $(\epsilon_r - 1)/2$ [120]. The loss tangent:

$$tan\delta = \frac{\epsilon''}{\epsilon'} + \frac{1}{\rho\omega\epsilon_0\epsilon'} \tag{4.8}$$

is dependent on the complex permittivity, $\epsilon = \epsilon' - j\epsilon''$, where ϵ''/ϵ' is around 1.2×10^{-5} to 5×10^{-5} [122–127]. The plot of Eq. (4.7) can be seen in Fig. 4.9. Assuming the exponential taper length is 300 μm, loss due to the substrate attenuation at 3 Ω-cm resistivity is around 3.64 dB, and increasing substrate resistivity to 1 kΩ-cm reduces substrate loss to 0.01 dB, which is 3.63 dB improvement. This results agrees well the HFSS simulation in Fig. 4.10(a), which shows around 4 dB improvement after resistivity increase. Due to the diminishing returns on reducing substrate loss, Fig. 4.10(b) shows the maximum efficiency improvement achieved at 1 kΩ-cm. Therefore, dual-layer proton irradiation was used to increase the substrate resistivity above 1 kΩ·cm [128], achieving the maximum

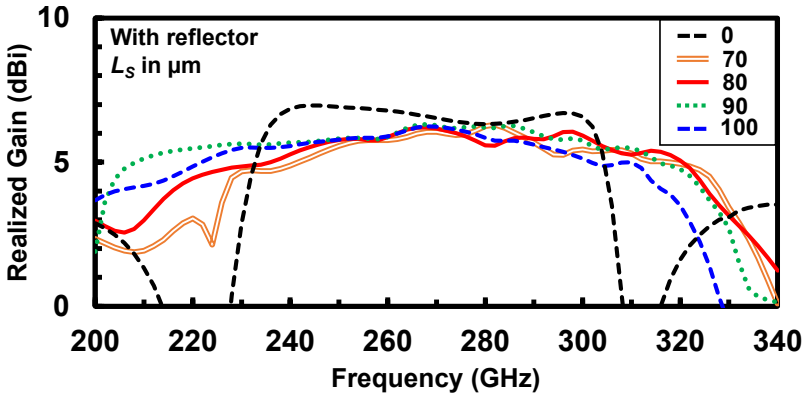


Figure 4.12: The realized gain simulation for different L_S.

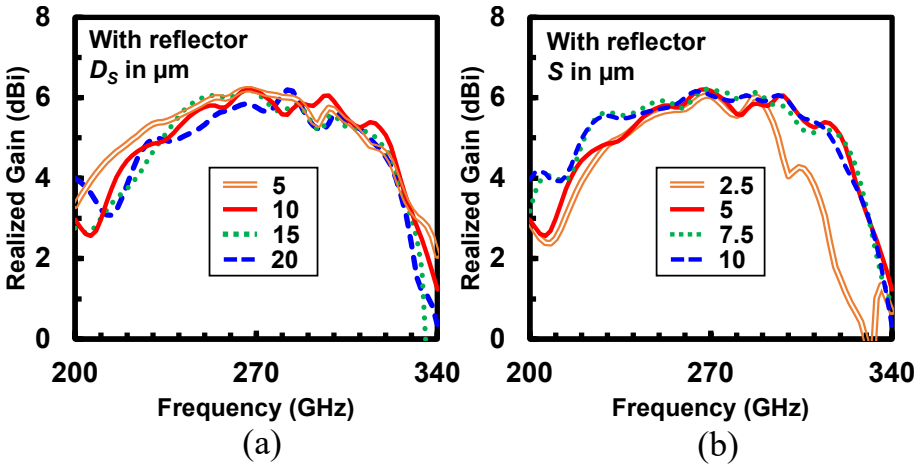


Figure 4.13: The realized gain simulation for various (a) D_S and (b) S.

achievable efficiency of 87%. This is a significant improvment compared to alternative method such as intrinsic layer (NTN Layer) [129], which only increase resistivity to 10Ω-cm and limiting efficiency improvement to around 50%.

with process details shown in Fig. 4.11. A 100 μm thick nickel mask was used to localize the high-resistivity region formation around the OCA and protect the active circuit from radiation damage, eliminating the need for remodeling or redesign. A dual-layer profile was used instead of the typical single profile [4, 5] to reduce the total proton fluence requirement, shortening the irradiation time [128]. For this implementation, the dual-layer profile consists of a deep irradiation at 60 μm depth with 2×10^{14} cm^{-2} fluence, and an interface irradiation at 10 μm depth with 2×10^{14} cm^{-2} fluence.

4.2.4 Design Process and Parametric Optimization

The Vivaldi OCA design process began with the initialization of all design parameters. First, the substrate thickness and resistivity were set to 50 μm and 1kΩ·cm, in accordance

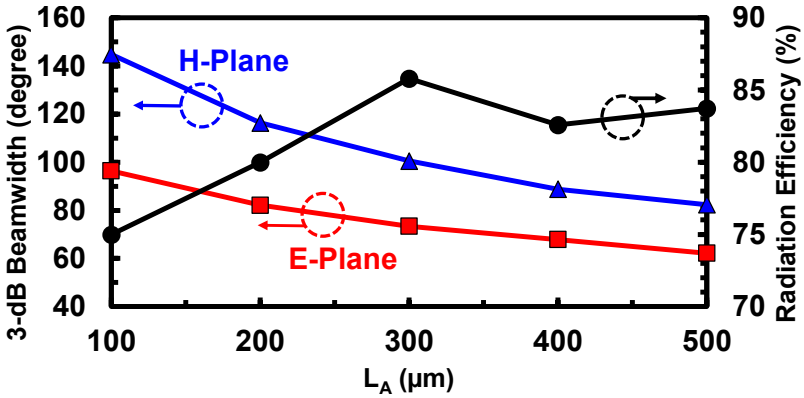


Figure 4.14: The simulation of efficiency, E-plane 3-dB beamwidth, and H-plane 3-dB beamwidth at 270 GHz for different L_A.

with the discussion in the previous subsection. Then, the feeding structure was designed and optimized on the initialized substrate, resulting in optimized design parameters in Fig. 4.7, where the value of $W_T = 5$ μm was determined. Finally, the rest of the OCA was built and initialized as follows (all units in μm, except R): $W_M = 450$, $W_F = 25$, $L_A = 300$, $L_B = 200$, $L_E = 150$, $L_S = 80$, $S = 5$, $D_S = 10$, and $R = 3$. W_F and L_B were kept constant. The optimization and parametric analysis were performed within the 200 GHz to 340 GHz frequency range, with a target operating frequency of 220 GHz to 320 GHz.

The first parametric analysis was performed on the comb-shaped slots parameters L_S, S, and D_S. A back reflector similar to Fig. 4.5(d) was added to better see the impact of the comb-shaped slots. Fig. 4.12 shows how the slots suppress gain dips at 220 GHz and 312 GHz induced by the energy reflected from the reflector. Shorter L_S provides better dip suppression at a higher frequency, while longer L_S has better low-frequency dip suppression. Therefore, L_S was adjusted to around 80 μm to achieve balanced dip suppression performance centered around 270 GHz, which also shows good agreement with (4.3). Fig. 4.13 shows the optimum value for both D_S and S is between 5 μm to 10 μm, or around $L_S/10$. The deviation of D_S value from $L_S/10$ has a minor effect, while the S value must be kept larger than 5 μm to prevent degradation at upper-frequency cut-off. After the optimization of comb-shaped slots, the reflector will not affect the antenna characteristics and can be removed during subsequent optimizations.

The rest of the design parameter, L_A, W_M, R, and L_E, was investigated and optimized through parametric analysis. The results in Fig. 4.14 confirm that shorter L_A leads to the wider E-plane and H-plane 3-dB beamwidth. However, there is a point where efficiency starts to degrade because the taper is too short to perform the traveling-wave radiation mechanism properly. Therefore, L_A should be set at the minimum value where it still operates above 80% efficiency, which was 300 μm in this case. The impact of W_M shown in

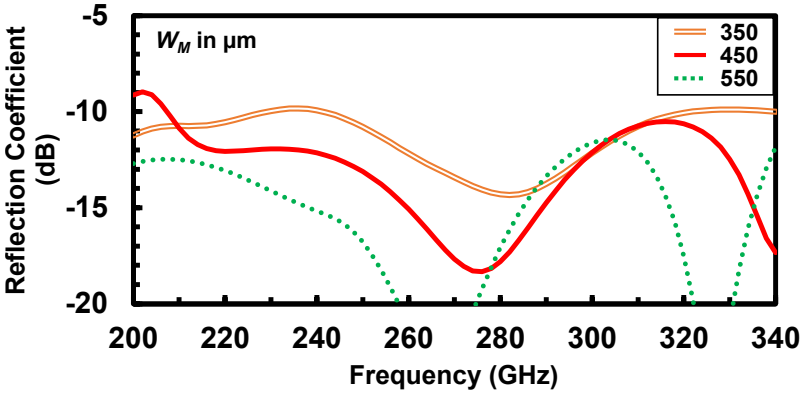


Figure 4.15: The simulation of reflection coefficient for different W_M.

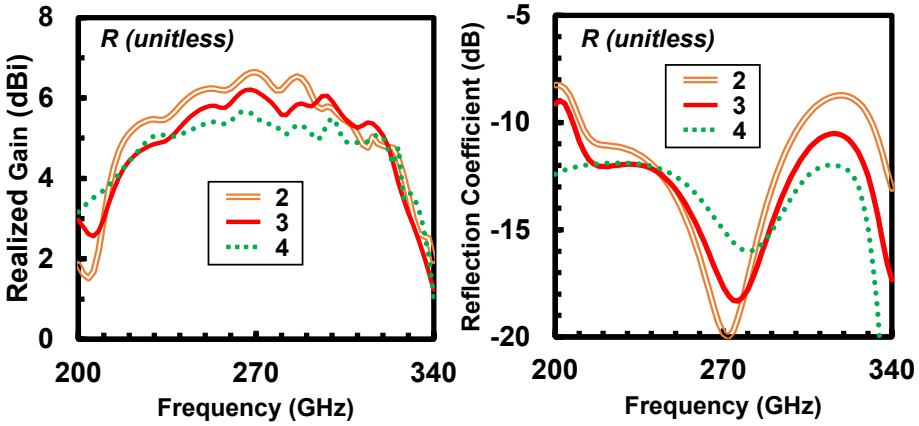


Figure 4.16: The simulation of (a) realized gain and (b) reflection coefficient for different R.

Fig. 4.15 indicates that the overall reflection coefficient increases as W_M decreases. This can be attributed to Equation (4.2), where smaller W_M moves the lower cutoff frequency closer to the operating frequency, causing the reflection coefficient to increase. To keep the antenna area small, W_M was reduced to the minimum size where the overall reflection coefficient is still below -10 dB, which is around 450 µm. The parametric analysis results of R shown in Fig. 4.16 are mainly a trade-off between gain and reflection coefficient, where the gain and the reflection coefficient are inversely proportional to R. Therefore, R was also reduced to the point where the overall reflection coefficient is still below -10 dB, which is around 3. Finally, the analysis of the L_E variation summarized in Fig. 4.17 shows how it behaves as a dielectric load [113] that can be tuned to boost the gain or to adjust the reflection coefficient of the antenna. In this design, L_E is tuned to achieve balance between both gain and reflection coefficient, resulting L_E value set to 150 µm.

The post-optimization design parameters for the OCA main structure can be found in Fig. 4.4. For the chip implementation, the area around the OCA was filled with

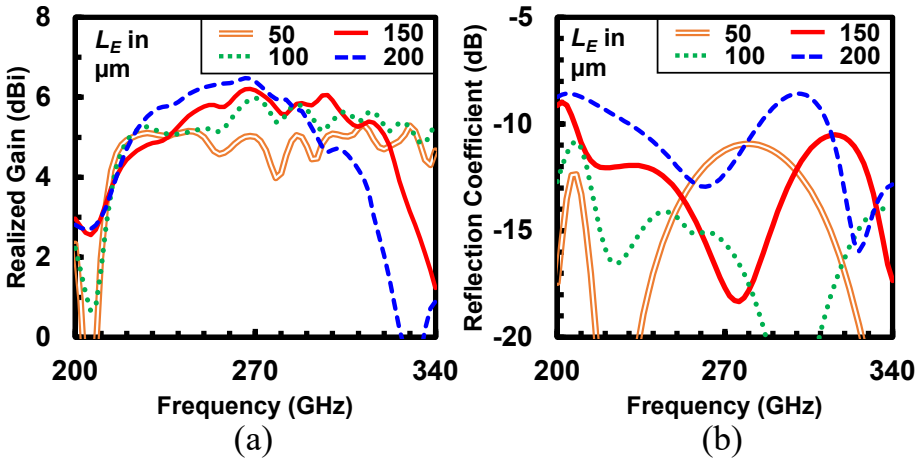


Figure 4.17: The simulation of (a) realized gain and (b) reflection coefficient for different L_E.

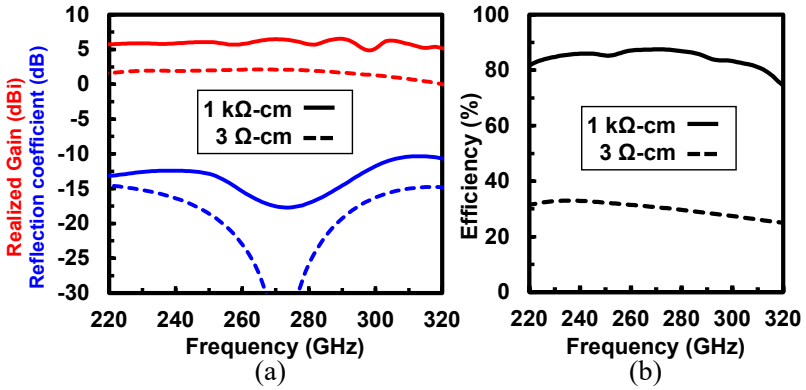


Figure 4.18: The post-optimization Vivaldi OCA simulation results of (a) realized gain, reflection coefficient and (b) efficiency before and after irradiation.

metal dummies to fulfill the metal density requirement. Fig. 4.18 shows the final simulation results of the non-irradiated and irradiated OCA gain, reflection coefficient, and efficiency after dummy placement. After irradiation, the designed on-chip Vivaldi antenna can achieve 6 dBi realized gain and around 80% efficiency across 220 GHz to 320 GHz. The reflection coefficient stays below -10 dB and the gain never decrease below 3-dB of the peak gain across the operating frequency, indicating more than 37% impedance and 3-dB gain bandwidth. Fig. 4.19 shows the Vivaldi OCA simulated radiation pattern from 220 GHz to 320 GHz, with detailed E and H plane 3-dB beamwidth values shown in Fig. 4.20. From 220 GHz to 280 GHz, the 3-dB beamwidth for the E-plane and H-plane is constant at around 76° and 100°, respectively. As the frequency increase to 320 GHz, the beamwidth of both E-plane and H-plane gradually decreased to 58° and 92°, respectively.

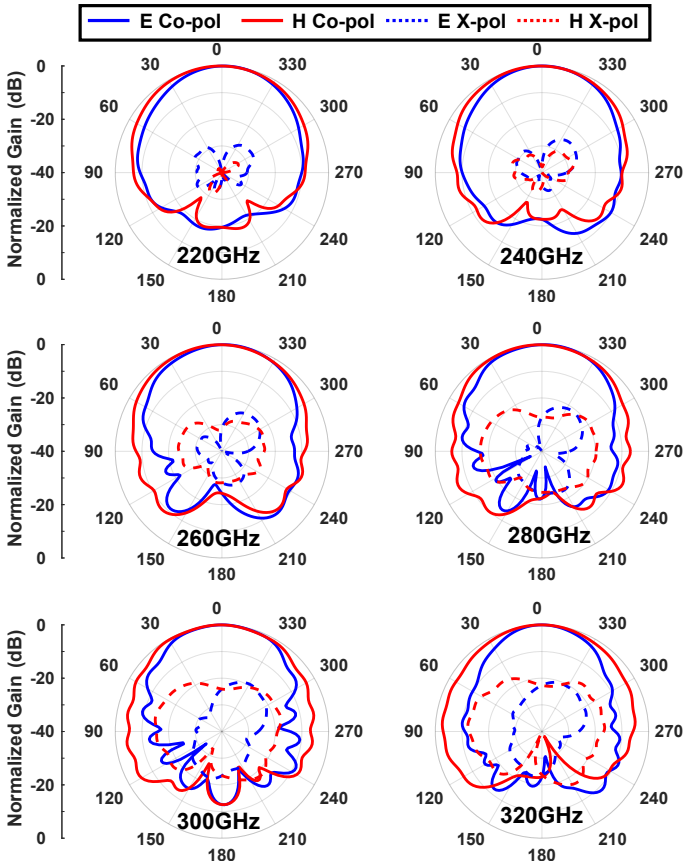


Figure 4.19: The simulated radiation pattern of the irradiated post-optimization Vivaldi OCA from 220 GHz to 320 GHz.

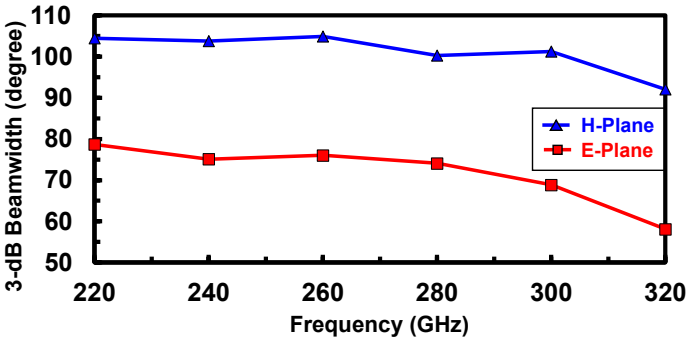


Figure 4.20: The simulated E-plane and H-plane 3-dB beamwidth of the irradiated post-optimization Vivaldi OCA .

4.3 Antenna Measurement

4.3.1 Fabrication and Measurement Methodology

Fig. 4.21 shows the die micrograph of the Vivaldi OCA manufactured using the TSMC 65-nm CMOS process. The antenna occupies 0.5 mm × 0.5 mm area on the chip. The

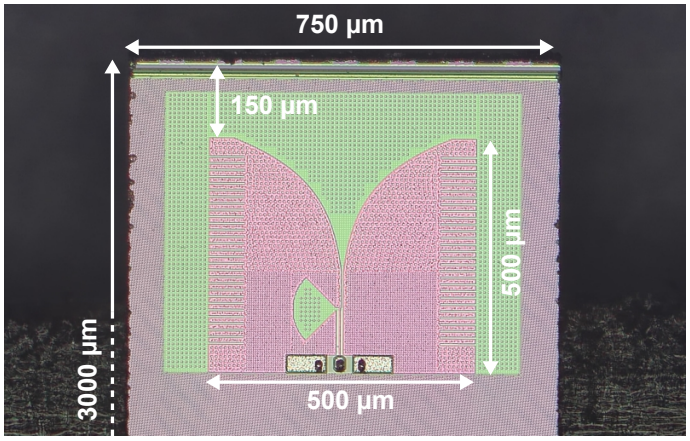


Figure 4.21: Die micrograph of the single element Vivaldi OCA.

fabricated chips were diced to 0.75 mm × 3 mm, and the substrates were thinned to 50 µm thick. The antenna gain and reflection coefficient were measured before and after irradiation. Another measurement was performed after 260°C annealing for 1 minute to investigate the ability of the irradiated substrate to withstand high-temperature post-processing (e.g., flip-chip, reflow soldering).

Fig. 4.22 shows the measurement setup to measure the reflection coefficient, gain, and radiation pattern of the single-element Vivaldi OCA as device-under-test (DUT). The setup consisted of two VDI WR-3.4 extenders connected to the Keysight PNA-X to perform S-parameter measurements from 220 GHz to 320 GHz frequency. The extender port-1 was connected to the DUT via a 325-GHz RF probe (Cascade Microtech i325-S-GSG), and the extender port-2 was connected to the VDI WR-3.4 diagonal horn antenna. The DUT was placed on the edge of the 3 mm thick MEGTRON6 board with a 300 µm distance between the antenna tip and the board edge to replicate the antenna implementation on the PCB. The minimum distance R between the horn and the DUT was determined using the far-field equation [115]:

$$R = \frac{2D^2}{\lambda} \tag{4.9}$$

with D as the aperture size. Since the horn has a significantly larger aperture than the DUT, the horn aperture diameter of 5.6 mm was used to calculate the minimum distance. The distance of 7 cm was chosen because it meets the far-field requirement at 320 GHz with some margins. The extender with the horn antenna can be swept within ±60° around the E-plane for radiation pattern measurements. The metal parts of the measurement setup, including the extender and the GSG probe near DUT, were covered with absorbers during the measurement session to reduce interference.

To calibrate the measurement setup, two calibrations were required to remove errors from both the GSG probe and the two extenders. The first calibration was the 1-port

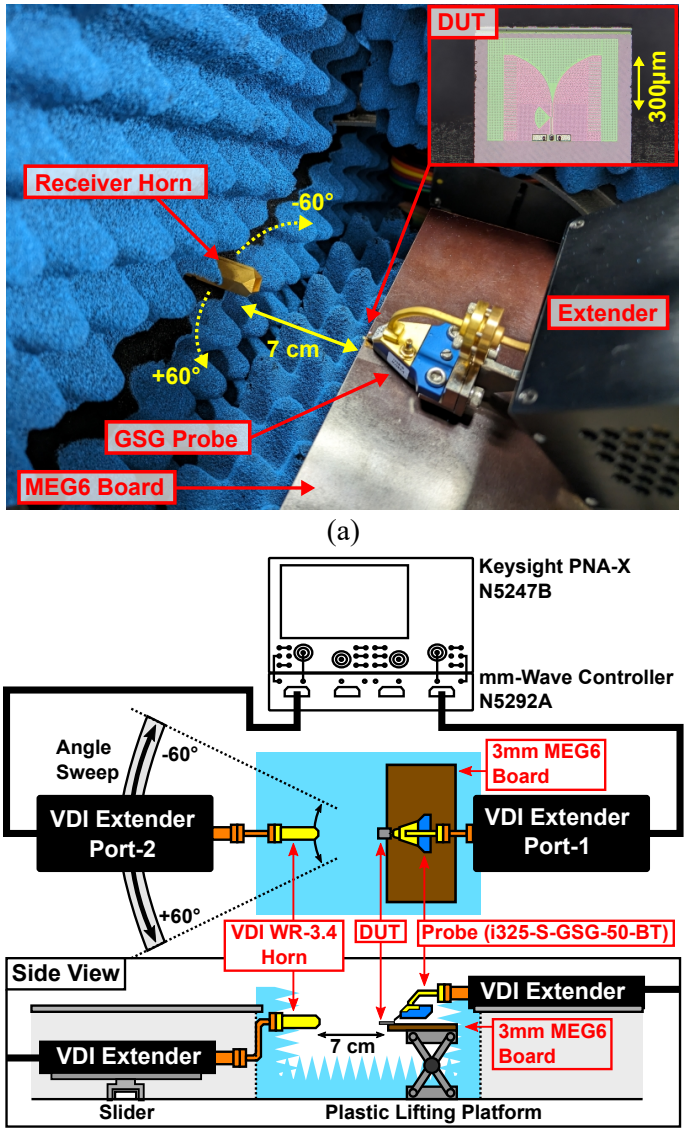


Figure 4.22: Measurement setup for reflection coefficient, gain, and radiation pattern.

short-open-load (SOL) calibration of the GSG probe using the impedance standard substrate (ISS) provided by the manufacturer. The second calibration was the 2-port thru-reflect-line (TRL) calibration between the WR-3.4 port of each extender. From these two calibrations, the GSG probe S-parameter characteristics can be extracted from the difference between the first measurement plane (probe tip) and the second measurement plane (extender output/probe input port). For the final setup, the 2-port TRL extender calibration was used as the base with the extracted GSG probe characteristics attached to the port-1 as an adapter using the internal de-embedding function available in the PNA.

With this setup, the reflection coefficient and the gain across the operating frequency can be measured directly at the same time. The measured reflection coefficient includes

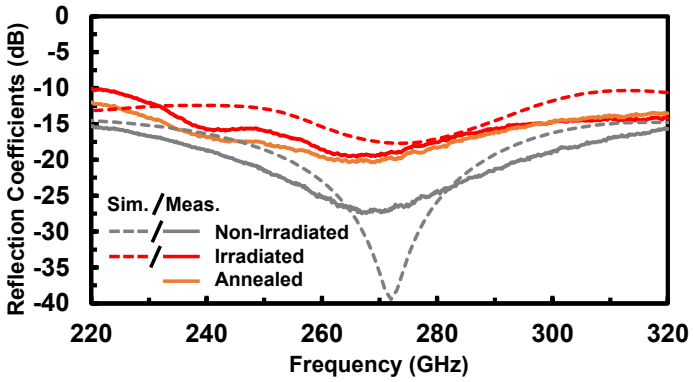


Figure 4.23: Simulated and measured reflection coefficient of the fabricated Vivaldi OCA.

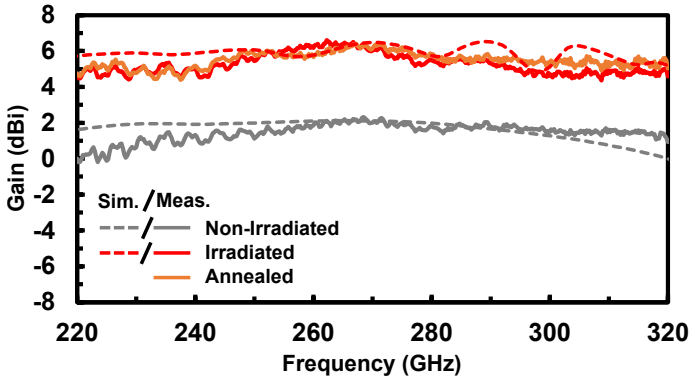


Figure 4.24: Simulated and measured gain of the fabricated Vivaldi OCA.

both the DUT and the pad. The pad was characterized separately and de-embedded from the measurement results, leaving only the reflection coefficient of the DUT. The antenna gain can be extracted from the S_{21} measurement using the following equation:

$$G_{DUT} = S_{21} - G_{horn} + L_{pad} + L_{wg} + 20\log_{10}(\frac{\lambda}{4\pi R}) \tag{4.10}$$

where G_{horn} is the gain of the horn antenna, L_{pad} is the loss of the pad, L_{wg} is the interconnect loss from the horn to the extender, and R is the distance between the horn and the DUT. All terms are in dB. The values of G_{horn}, L_{pad}, and L_{wg} are known from the datasheet or from separate measurements. The normalized radiation pattern can be obtained by comparing S_{21} at 0°with measurements from different angles.

4.3.2 Measurement Results and Analysis

The simulated and measured reflection coefficients for all irradiation conditions are compared in Fig. 4.23. The measured reflection coefficient was below -10 dB within the measurement frequency range of 220 GHz to 320 GHz, or more than 37% impedance

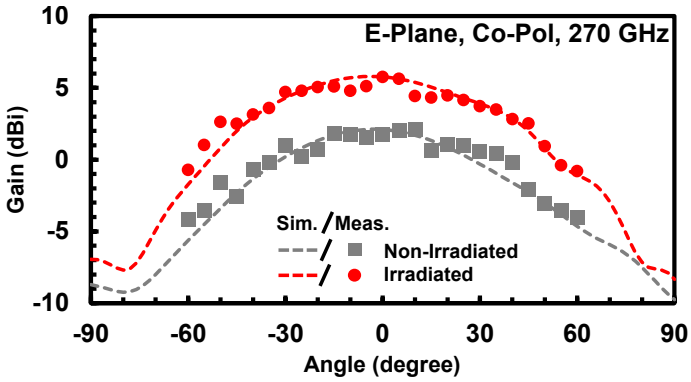


Figure 4.25: Simulated and measured E-plane radiation pattern of the fabricated Vivaldi OCA at 270 GHz.

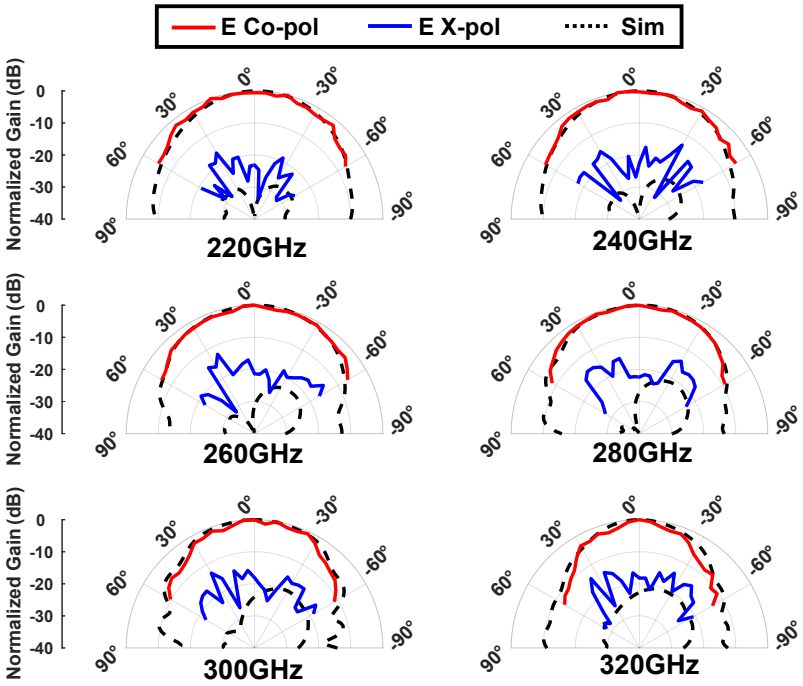


Figure 4.26: Simulated and measured E-plane radiation pattern of the irradiated Vivaldi OCA across the measurement frequency.

bandwidth for all sample groups. The reflection coefficients of the irradiated DUT were around 5 dB to 10 dB higher than the non-irradiated DUT because the increase in substrate resistivity reduced the substrate loss, resulting in more energy available to be transmitted or reflected.

The gain measurement and simulation results for all sample groups are compared in Fig. 4.24. The peak measured gain for the non-irradiated DUT was 2 dBi at 270 GHz with 2 dB variation across the measurement frequency range, which improved by 4 dB to 6 dBi peak gain at 270 GHz with 1dB variation after irradiation. The 3-dB gain bandwidth

was measured to be at least 100 GHz (>37%) for all irradiation cases. No significant gain variation was observed between the irradiated and the annealed DUTs, indicating that the gain enhancement provided by the irradiation process can withstand the high-temperature post-processing.

Fig. 4.25 shows the measured and simulated effect of irradiation on the E-plane co-polarized radiation pattern at 270 GHz. The irradiation caused similar gain improvement at pattern within ±48° angle and slowly diminished above that limit. The measured E-plane 3-dB beamwidth was around 76° at 270 GHz both before and after irradiation because the beamwidth was within the ±46° limit. The E-plane radiation pattern of the irradiated Vivaldi OCA across the measurement frequency is shown in Fig. 4.26. The measured E-plane 3-dB beamwidths were around 76° from 220 GHz to 280 GHz, which slowly decreases to 72° at 300 GHz and 54° at 320 GHz.

Overall, the measurement results generally match the simulation results, with a discrepancy of more than 5 dB in some parts of the reflection coefficient and cross-polarization values. The possible causes of these discrepancies include the difference between real and simulated substrate resistivity value, the rough chip edge after the dicing process, the probe affecting the antenna characteristics, and the adhesive used to fix the DUT. Due to the limitation of the measurement setup, the antenna efficiency and H-plane 3-dB beamwidth were determined from the simulation after the model was verified with measurement results. The simulated efficiency at 270 GHz is 32% for the non-irradiated DUT and 87% after irradiation. The simulated 3-dB H-plane beamwidth is 96° before and after irradiation.

Table 4.1 shows the comparison with other published silicon on-chip antennas operating at the 300 GHz band. The proposed antenna offers the widest bandwidth, the highest radiation efficiency, and a relatively large 3-dB beamwidth compared to previous works. This work is the only end-fire on-chip antenna implemented using a standard CMOS process with less than $0.5\lambda_0 \times 0.5\lambda_0$ dimension, making it suitable for slat array implementation.

4.4 Conclusion

This chapter presented the design process, optimization, and parametric analysis of a 300 GHz band on-chip Vivaldi antenna for implementation on a standard 65nm CMOS process with a proton-irradiated substrate. The designed OCA was fabricated, irradiated, and measured to verify the proposed design. The measurement results shows 3-4 dB gain improvement across the operating frequency after irradiation, achieving 6 dBi peak gain and 87% efficiency at 270 GHz. The Vivaldi OCA achieved 76° E-plane beamwidth at

Table 4.1: Comparison with state-of-the-art 300GHz band on-chip antennas

Ref.	Process	Type	Rad. Dir.	Freq. (GHz)	BW (%)	Gain (dBi)	Eff. (%)	BeamW (°)		Area (λ_0)
								E	H	
[27]	65-nm CMOS	SIW Slot	Broad-side	270	15	0	22*	60#	60#	0.40 ×0.40
[28]	65-nm CMOS	Patch	Broad-side	300	14	3.1	40.3*	38#	68#	0.23 ×0.42
[130]	65-nm CMOS	DRA	Broad-side	325	34.5*	8.6	44	60*#	43#	0.87 ×0.87
[131]	65-nm CMOS	DRA	Broad-side	298	22*#	6.5*	58*	–	–	0.50 ×0.33
[105]	130-nm SiGe	μ bump	Broad-side	283	7	9.87	54.4*	37	55	0.85 ×0.85
[31]	130-nm SiGe	Patch	Broad-side	295	9	1.7	–	–	45*#	0.25 ×0.36
[106]	130-nm SiGe	Ring	Broad-side	324	9	1.4*	41*	75*#	80*#	0.54 ×0.54
[107]	130-nm SiGe	SIW Slot	Broad-side	340	7	3.3	45*	88	76	0.58 ×0.58
[113]	130-nm SiGe	Dipole	End-fire	320	12.5	3.9	80*	63*#	105*#	0.50 ×0.64
This Work	**65-nm CMOS**	**Vivaldi**	**End-fire**	**270**	**37**	**6**	**87***	**76**	**96***	**0.45 ×0.45**

Estimated from paper * Simulated value λ_0 = Wavelength at center frequency
Bandwidth (BW) is the worst case between 3-dB gain BW or 3-dB impedance BW.
Beamwidth (BeamW) is not plus-minus.

270 GHz and fully covers the 300 GHz band (220 GHz to 320 GHz), which corresponds to 37% impedance and 3-dB gain bandwidth. The wide bandwidth, large beamwidth, and high efficiency demonstrated by the Vivaldi OCA make it suitable for future on-chip slat array implementation to achieve full 2-dimensional array scaling.

Chapter 5

300GHz-Band CMOS On-Chip Chip-to-Waveguide Transition for Flip-Chip Implementation [1]

5.1 Introduction

Recently, the 300 GHz band (220 GHz to 320 GHz) has garnered a lot of research interest due to the potential utilization of the available large bandwidth for the future high-speed and low-latency 6G wireless communication system [21]. However, the relatively large path loss [22] requires a high gain antenna or high transmitter (TX) output power to achieve practical link distance. While the CMOS process promises low cost, digital integration, and high volume, its on-chip antenna suffers from low gain due to substrate effects [32], and it has relatively low output power. A phased array structure [87, 97] improves gain and adds active beam steering capabilities. However, large number of elements are needed, leading to larger power consumption and possible thermal issues due to low element efficiency. Therefore, most transceiver (TRX) implementations use integrated lenses [83, 84, 133] or standardized waveguide interfaces [7, 89, 134–137]. The waveguide interface offers the most modularity and flexibility, allowing integration with various antenna modules [138] or amplifier modules fabricated using different technologies [27].

A low-loss chip-to-waveguide transition is necessary to connect the TX chip with the waveguide interface. The on-PCB transition [89, 136, 137] has the lowest fabrica-

[1] This chapter is based on "A 300-GHz Band Chip-to-Waveguide Transition on Proton-Irradiated Standard 65nm CMOS Si Substrate for Flip-Chip Packaging Implementation" [132] by the same author, which appeared in the IEEE International Microwave Symposium (IMS),

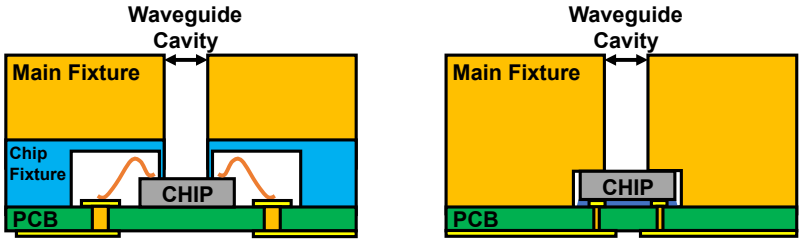


Figure 5.1: Waveguide fixture assembly for (a) wirebond mounted [7], and (b) flip-chip mounted chip.

tion cost. However, it has a significant interconnect loss at the 300 GHz band, and the sub-millimeter structure size is difficult to manufacture precisely with a low-cost PCB process, causing an 8 dB packaging loss. On-chip end-fire topology [27, 29, 106, 134] requires inserting the chip directly into the waveguide block and is typically used for small components such as the amplifier module. However, the block machining and fabrication complexity increases for a TX system that requires a lot of external I/O and supporting circuits, while broadside topology [7, 139] allows external I/O and components placement on external low-cost PCB. All published TXs with on-chip broadside transition [7, 135] are mounted to the PCB with wirebonds, which need to be covered with additional structure (Fig. 5.1). Furthermore, the low substrate resistivity (10 Ω·cm) and high relative permittivity (ϵ_r = 11.9) of the substrate used in standard CMOS process degrade transition efficiency.

This chapter proposes an integrated on-chip chip-to-waveguide transition for the waveguide interface. The transition was designed to radiate through the chip's backside, enabling flip-chip mounting to the PCB, providing more reliable, high-speed interconnect implementation, and simplifying the TX module's overall structure and assembly process. The transition was fabricated using the standard 65-nm CMOS process, and proton irradiation was applied to increase substrate resistivity around the transition, reducing transition loss to 2.9 dB. Integration with a 300 GHz TX was demonstrated through the creation of a TX module, which demonstrated a maximum data rate of 80 Gb/s for direct measurement and 64 Gb/s with a 40 cm link distance.

5.2 Transition Design

5.2.1 Transition Structure and Operating Principle

Fig. 5.2(a) shows the proposed chip-to-waveguide transition overall design. The transition probe is implemented using the top metal on the 65nm standard CMOS process. The chip

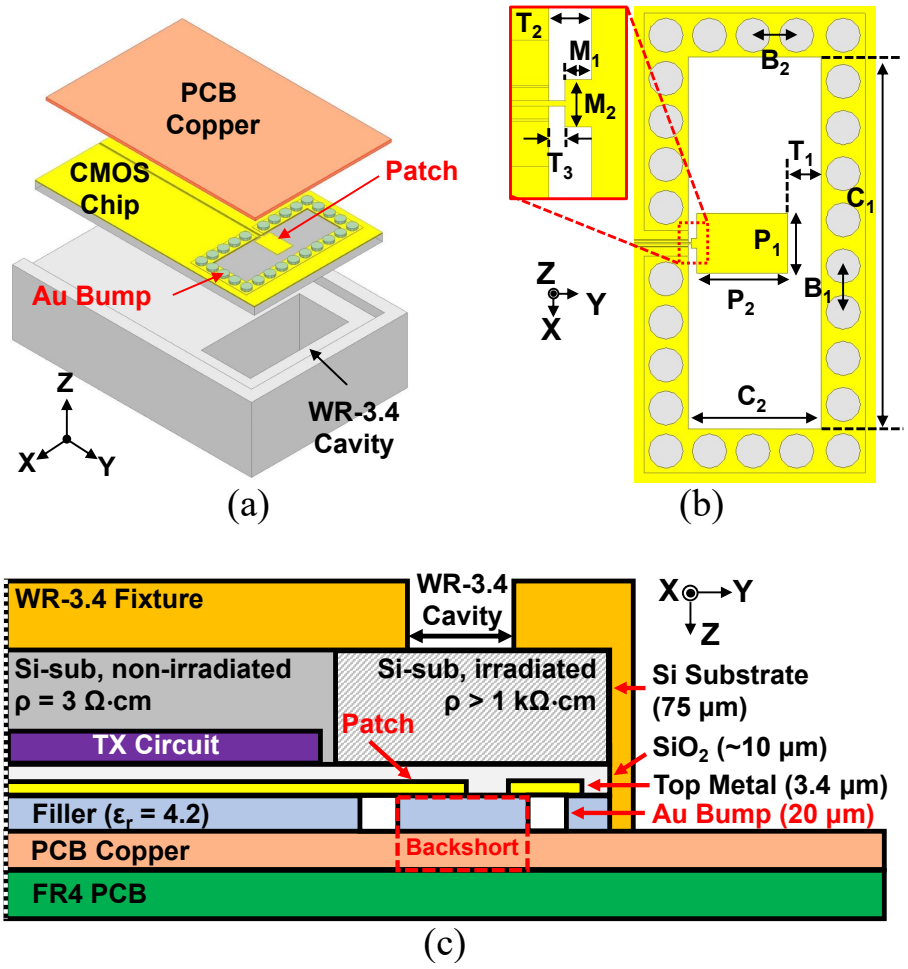


Figure 5.2: Proposed on-chip chip-to-waveguide transition design: (a) 3D isometric view, (b) transition design parameter, and (c) cross-section view. (All parameters in μm: P_1 = 140, P_2 = 210, C_1 = 864, C_2 = 308, T_1 = 78, B_1 = 107, B_2 = 101, T_2 = 20, T_3 = 7.5, M_1 = 12.5, and M_2 = 22.5)

is attached using Au bump to the top metal of the PCB with the air gap in-between filled with dielectric material (ϵ_r = 4.2). The solid PCB top metal isolates the effect of the PCB dielectric, allowing flexible use of various PCB materials. The back-short structure is formed using the top metal of the PCB and the bump around the probe cavity to create a quasi-metallic wall. The waveguide cavity is attached directly below the transition probe. Therefore, the probe radiates through the silicon substrate to the waveguide cavity.

Fig. 5.2(b) shows the detailed structure and dimensions of the proposed transition. Due to the fixed height of the Au bump of 20 μm provided by the flip-chip process, the back-short length is limited to 20 μm, which is 15% longer than the $\lambda_g/4$ = 17 μm at 240 GHz. Therefore, a patch structure was chosen for the transition probe to provide additional matching point by adjusting the dimension of the probe patch (P_1 and P_2) and

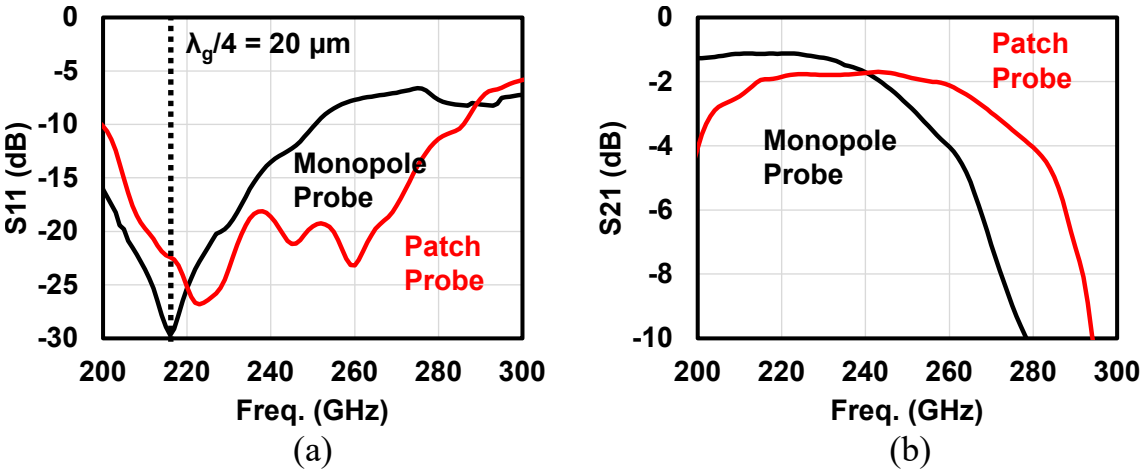


Figure 5.3: Comparison between monopole probe and patch probe.

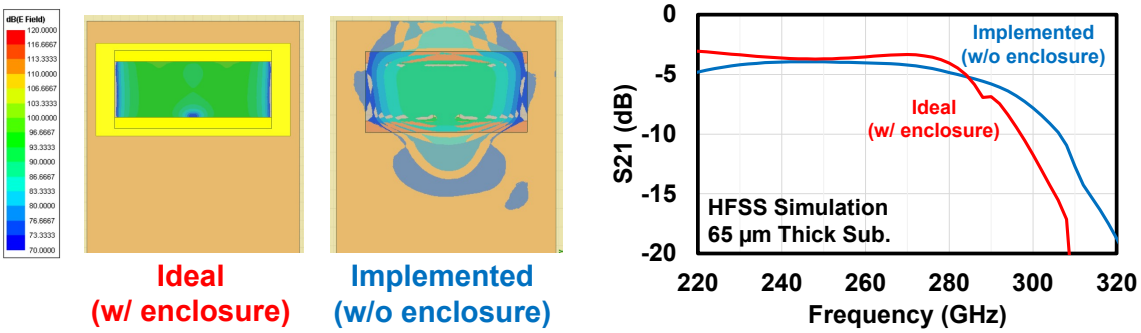


Figure 5.4: The effect of through-silicon wall on the transition insertion loss simulated with HFSS.

the distance between the probe patch and the cavity wall (T_1). This additional matching points extends the transition bandwidth in expense of higher insertion loss, as shown in Fig. 5.3. The substrate thickness is adjusted by grinding the chip backside to around a quarter of the relative wavelength inside the substrate. The matching between the transmission line and the patch can be controlled by adjusting the distance between the feeding side of the patch and the cavity wall (M_1, M_2, T_2, and T_3).

Fig. 5.2(c) shows the detailed cross-section of the transition implementation. Thru-silicon vias (TSV) are not used to create a metalic wall through the Si substrate due to the high permittivity of the Si substrate (ϵ_r = 11.9), which makes the field more compact and less prone to spread through the gap between the probe and the open cavity. The simulation result in Fig. 5.4 shows how the removal of enclosure has less than 1 dB impact on the transition insertion loss. Furthermore, the wall removal increase the transition bandwidth. Therefore, the removal of the wall reduces the chip manufacturing cost with minimum impact on performance.

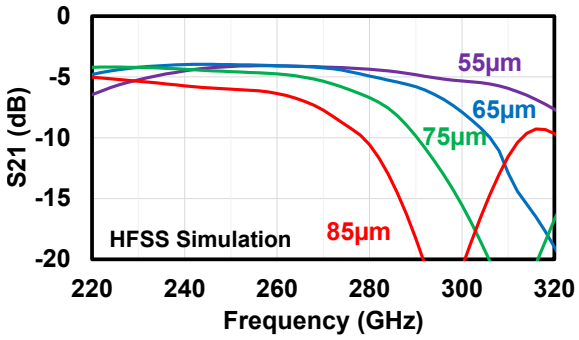


Figure 5.5: The effect substrate thickness on the transition insertion loss simulated with HFSS.

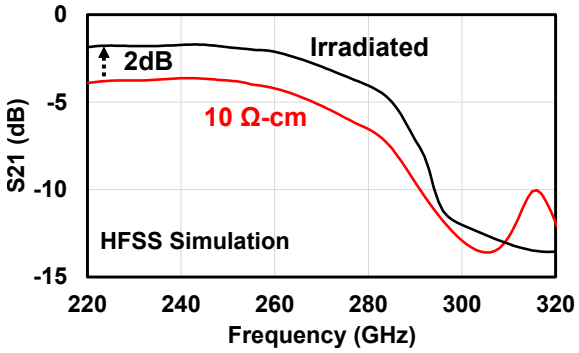


Figure 5.6: The effect of irradiation on the transition insertion loss simulated with HFSS.

The transition substrate thickness needs to be optimized to obtain the best insertion loss characteristic. Fig. 5.5 shows the effect of substrate thickness on the transition insertion loss characteristic across frequency. If the substrate thickness is larger than 80 µm, a parasitic TE_1 mode surface wave is able to propagate through the substrate in accordance to the Equation (4.4), which causes energy to propagate through the substrate rather than the waveguide cavity. This phenomenon causes the insertion loss degradation depicted in the 85 µm substrate shown in Fig. 5.5. For thickness below 80 µm, the silicon substrate can be treated as a silicon-filled waveguide cavity connected to the air-filled WR-3 waveguide cavity, which caused mismatch due to the different characteristic impedance between the two. Therefore, the substrate thickness must be adjusted to around $\lambda_{si}/4$ to prevent mismatch, with λ_{si} as the wavelength inside the silicon. In this implementation, 65 µm substrate thickness was chosen, which corresponds to $\lambda_{si}/4$ around 250 GHz, resulting in the blue curve in Fig. 5.5.

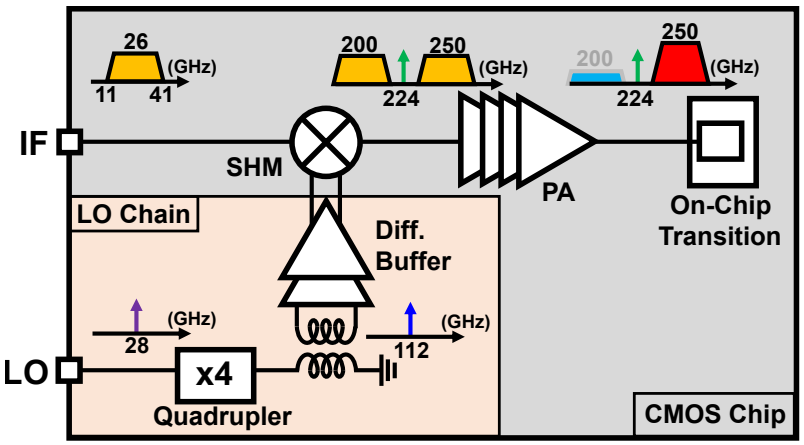


Figure 5.7: Block diagram of the entire CMOS TX chip.

5.2.2 Effect of Dual-Layer Proton Irradiation

To prevent substrate loss caused by low resistivity substrate, a dual-layer proton irradiation was performed to increase the resistivity of the substrate around the transition probe using the optimized irradiation profile obtained in Chapter 3. Fig. 5.6 shows the effect of irradiation on the transition insertion loss. After irradiation, the transition insertion loss decreases from 4 dB to 2 dB, which is 2 dB improvement. It can be seen that the irradiation only affect insertion loss, and there is no change in the transition bandwidth.

5.3 TX Module Integration

To demonstrate the chip-to-waveguide transition in the TX module, the TX architecture presented in [97] was modified by removing the phase-shifter from the LO chain and adding the transition structure, as shown in Fig. 5.7. The TX chip consists of a local oscillator (LO) multiplication chain, a sub-harmonic mixer (SHM), a power amplifier, and an on-chip chip-to-waveguide transition. The 250 GHz RF signal was generated by sub-harmonic mixing to halve the required LO chain output frequency to 112 GHz, reducing its power consumption. The LO chain consists of a quadrupler to multiply the 28 GHz input to 112 GHz, a balun for conversion to differential signal required by the SHM, and differential buffers to ensure enough LO power to drive the SHM. The power amplifier (PA) was designed using a custom transistor layout and gain boosting architecture to boost its f_{max} and achieve around 20 dB gain from 235 GHz to 265 GHz. Due to its bandpass characteristic, the PA also suppresses the image at 200 GHz.

Fig. 5.8(a) shows the micrograph of the TX chip fabricated using a standard 65-nm CMOS process, with 1.2 mm $\times$ 3.6 mm of area. The fabricated chip was irradiated and

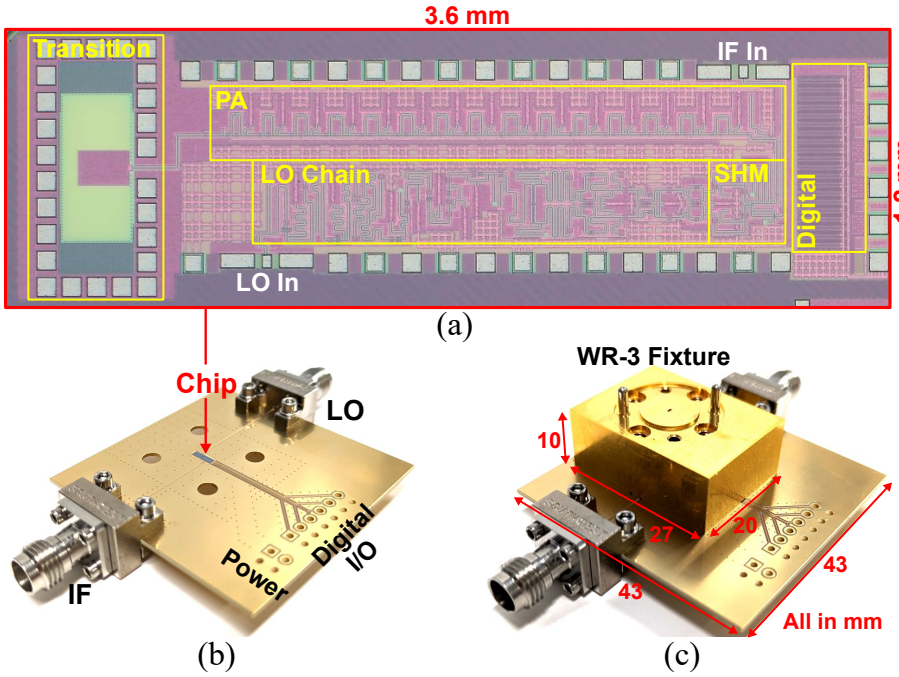


Figure 5.8: Fabricated TX module: (a) chip micrograph, (b) PCB implementation photo, and (c) fixture implementation photo and module dimensions.

ground to the target substrate thickness. Then, the chip was mounted to a 43 mm × 43 mm PCB using the flip-chip process, resulting in the implementation shown in Fig. 5.8(b). A chip-to-WR3 fixture was fabricated with split-block method and directly mounted to the PCB using four 3.2 mm screws, resulting in the final module assembly shown in Fig. 5.8(c).

5.4 Measurement Results

5.4.1 Transition Measurement

To verify the performance of the transition, the transition was manufactured and measured in a back-to-back configuration. The prototype transition was fabricated using the standard 65nm CMOS process (Fig. 5.9). Several chips were irradiated for comparison with the non-irradiated chip. A 1.6 mm thick FR-4 PCB with 18 µm top copper thickness was used as back-short and attached to the chip using Au bump (Fig. 5.10). A metal fixture (Fig. 5.11) was used to connect the output of the chip to the WR-3.4 interface, which was then connected to the OML VNA extender module and Agilent N5260A Network Analyzer (Fig. 5.12).

Fig. 5.13(a) shows the insertion loss measurement results of the back-to-back transi-

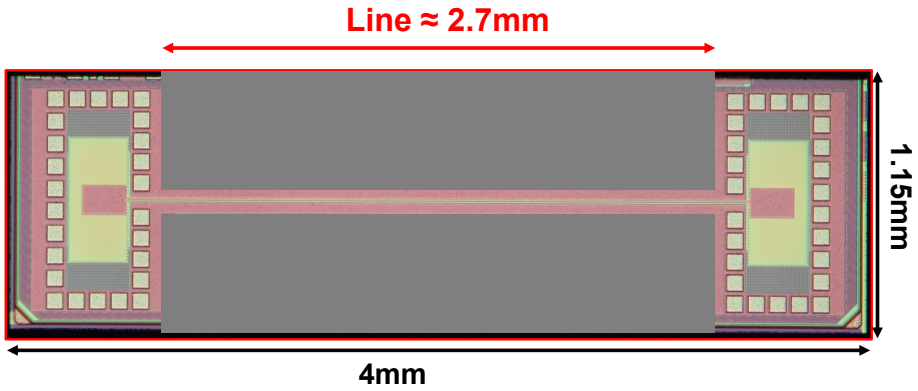


Figure 5.9: Chip photo of the prototype back-to-back transition manufactured in standard 65nm CMOS process.

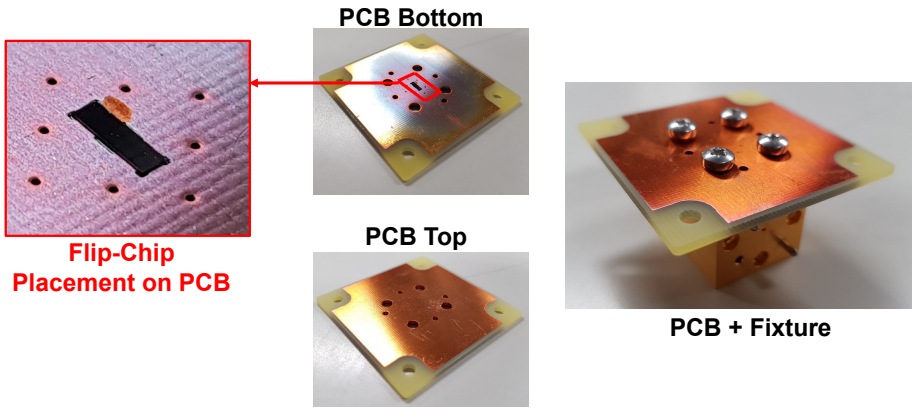


Figure 5.10: Details of the chip implementation on the FR4 PCB and integration with the WR-3 fixture.

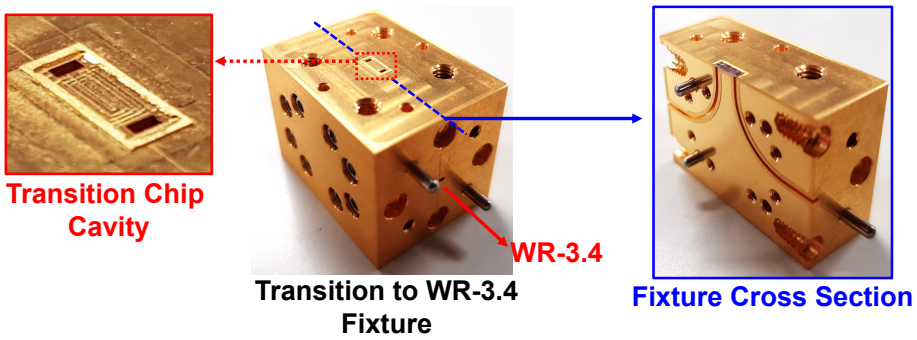


Figure 5.11: Details of the fabricated WR-3 fixture for the transition measurement.

tion and the calculated single transition measurement for both irradiated and non-irradiated chips. The calculation is done by dividing the back-to-back measurement results by 2 and subtracting the transmission line loss, which is measured to be around 2.2 dB/mm. The measurement result shows the 3-dB bandwidth from 220 GHz to 283 GHz for both irra-

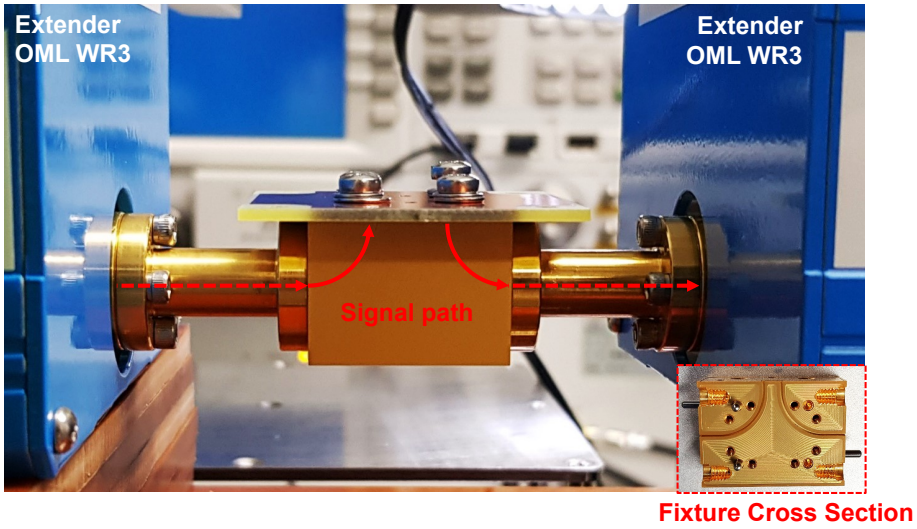


Figure 5.12: Measurement setup for measuring back-to-back transition.

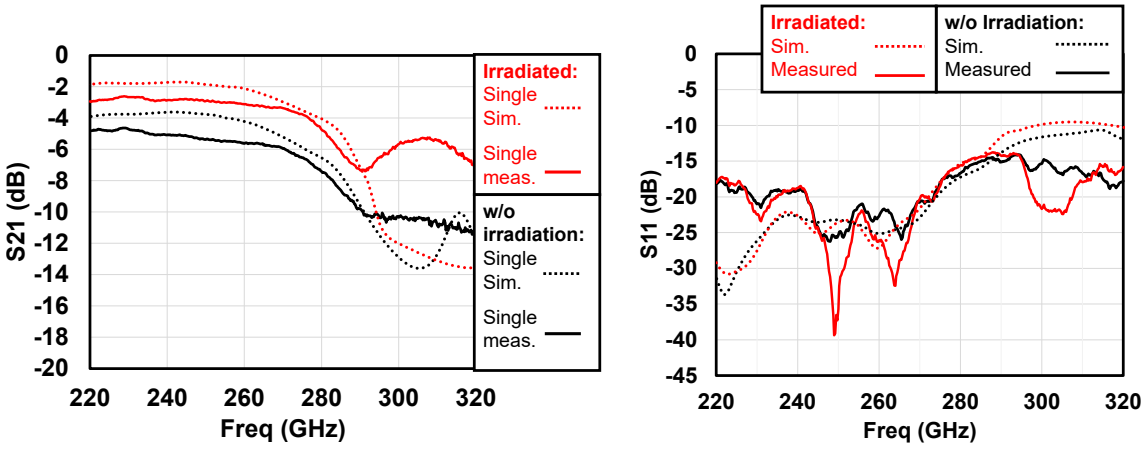


Figure 5.13: Measurement results of (a) transition insertion loss, and (b) transition return loss.

diated and non-irradiated chips. The insertion loss of 4.9 dB at 240 GHz was obtained before irradiation, and irradiation improves the return loss to 2.8 dB at 240 GHz, which corresponds to around 2.1 dB improvement across operating frequency. The measured return loss of back-to-back transition can be seen in Fig. 5.13(b), which shows no significant difference before and after irradiation. The difference in magnitude of S11 and S21 between simulation and measurement can be attributed to chip misalignment and fixture manufacturing tolerance.

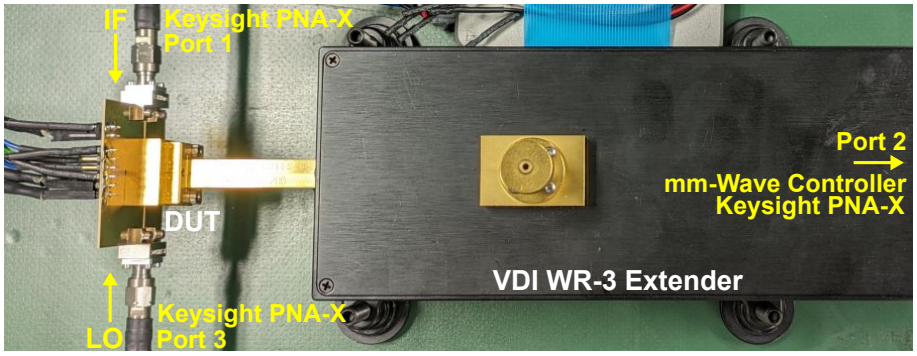


Figure 5.14: Measurement setup for TX linearity, output power and conversion gain.

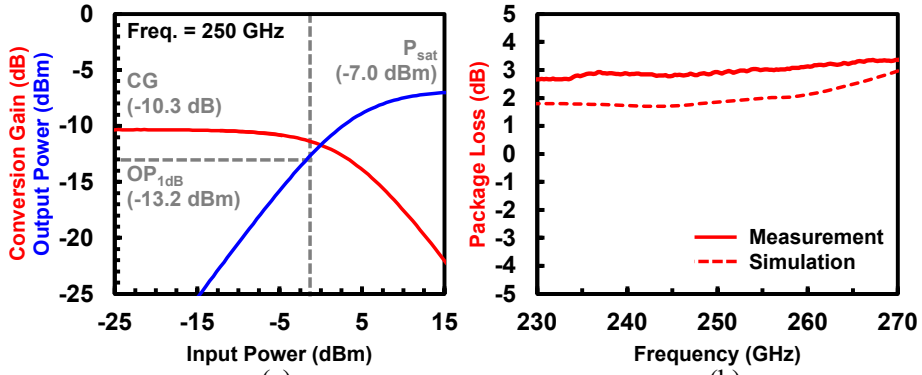


Figure 5.15: Measurement results of the TX module's (a) linearity at 250 GHz; (b) package loss (transition + WR-3 fixture) across measurement frequency.

5.4.2 TX Module Measurement

Fig. 5.14 shows the linearity, output power, and conversion gain measurement setup with the TX module as device-under-test (DUT). A Keysight PNA-X N5247B was set to scalar mixer/converter measurement (SCM) mode with port-1 as IF source, port-3 as LO source, and port-2 connected to the VDI WR-3 extender through a mm-wave head controller for the RF power measurement. Fig. 5.15(a) shows the measured conversion gain (CG) of -10.3 dB, output P_{1dB} of -13.2 dBm, and saturated power (P_{sat}) of -7 dBm at the center frequency of 250 GHz. The SHM and PA gain have been measured in [97] as -23 dB and 22 dB, respectively. The rest of the -9.3 dB CG degradation is caused by interconnect loss from the IF connector to the SHM input and the package loss. The package (transition + WR-3 fixture) loss was measured by comparing the PA probe P_{sat} measurement result of -3.4 dBm in [97] and the TX module P_{sat} measurement after de-embedding the PA-to-transition interconnect loss of 0.8 dB, resulting in 2.9 dB package loss at 250 GHz, which is close to the 2.8 dB obtained from the back-to-back measurement results in [132]. This

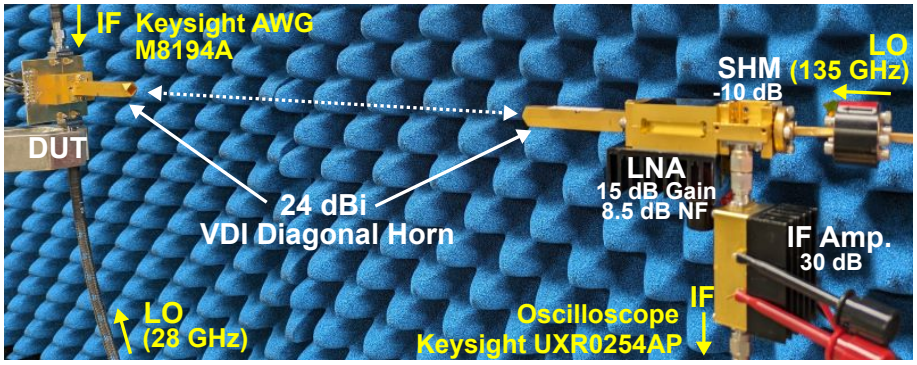


Figure 5.16: Measurement setup for OTA EVM_{rms} measurement.

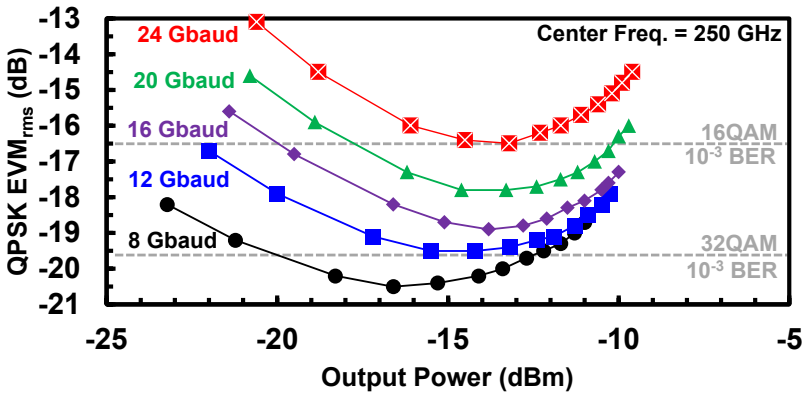


Figure 5.17: TX module direct QPSK EVM_{rms} measurement across different output power and baudrate.

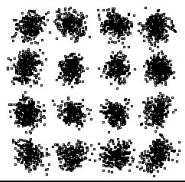
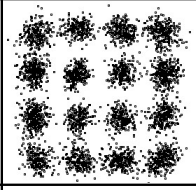
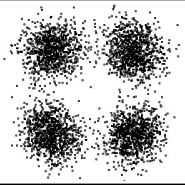
Link distance (m)	Direct	0.4	0.7
Modulation	16QAM	16QAM	QPSK
Symbol rate (Gbaud)	20	16	24
Data rate (Gb/s)	80	64	48
Constellation			
EVM_{rms} (dB)	-17.2	-16.7	-9.9

Figure 5.18: Measured TX module's constellations.

process was repeated across the measurement frequency, resulting in Fig. **??**(b), which shows around 3 dB package loss across the operating frequency and confirms the previous B2B transition measurement results.

Table 5.1: Comparison of state-of-the-art 300 GHz band TXs with Waveguide Interface

Ref.	[135]	[137]	[7]	**This Work**
Process	130-nm SiGe BiCMOS	40-nm CMOS	28-nm CMOS	65-nm CMOS
Freq. (GHz)	220	300	390	250
Chip Mounting	Wirebond	Flip-chip	Wirebond	**Flip-chip**
Transition Type	On-Chip Broadside	PCB Broadside	On-Chip Broadside	**On-Chip Broadside**
Transition Loss (dB)	3.7	8.0	5.0*	**2.9**
Module P_{sat} (dBm)	4.4	-13.5	-16	**-7**
Modulation	16QAM	16QAM	QPSK	16QAM
Data Rate (Gb/s)	12	48	6	80 / 64
Link Dist. (m)	0.5	0.05	Direct	Direct / 0.4
P_{dc} (mW)	640	1400	850	**215**

* Simulated value

Fig. 5.16 shows the setup for data link evaluation through the TX module's error vector magnitude (EVM) measurement. An arbitrary waveform generator (AWG) was used to generate modulated IF at a particular frequency and symbol rate for the TX, which was demodulated and measured with oscilloscope after down-conversion with discrete receiver (RX). Initial measurement was performed by directly connecting the TX module output to the discrete RX SHM input to evaluate the optimum output power and symbol rate of the TX module. The results in Fig. 5.17 indicate optimum output power of around -16 dBm to -13 dBm, and the maximum speed of 80 Gb/s (16QAM, 20 Gbaud) is confirmed through measurement results shown in the Fig. 5.18. The fastest over-the-air (OTA) data rate measurement was 64 Gb/s (16QAM, 16 Gbaud) over 0.4 m link distance. The longest link distance supported by the QPSK modulation with 24 Gbaud symbol rate is 0.6 m, resulting in a 48 Gb/s.

Table 5.1 compares the proposed TX module with other CMOS 300 GHz band TXs with waveguide interface. The proposed back-radiating on-chip chip-to-waveguide transition, combined with proton irradiation, can achieve the lowest transition loss compared to the other works. This work also achieves the highest data rate and lowest power consumption because of the PA, which eliminates the need for power combining and allows

higher output power compared to other standard CMOS implementations.

5.5 Conclusion

A 300GHz band chip-to-waveguide transition on proton-irradiated standard 65nm CMOS Si substrate was designed and measured. The manufactured prototype exhibits 220GHz-283GHz operating frequency, with 4.9dB insertion loss before irradiation and 2.8dB insertion loss after irradiation at 240GHz. A TX module was also fabricated to demonstrate the transition integration with a 300 GHZ band system. The proposed transition enables flip-chip mounting, reducing the TX module fabrication and integration complexity. The TX module achieves a maximum data rate of 80 GB/s for direct measurement and 64 Gb/s over a 0.4 m link distance.

Chapter 6

Conclusion and Future Work

6.1 Conclusion

This thesis presented the proposed dual-layer proton irradiation to improve the performance of the on-chip passive components implemented on standard CMOS processes through creating a localized high-resistivity region on the target component, which eliminates the need of active device remodeling and the modification of the existing CMOS process.

The dual-layer proton irradiation process splits the irradiation into two steps, the interface irradiation and the main irradiation, to efficiently mitigate the formation of the parasitic surface conduction layer, which was not taken into account in the previous proton irradiation process.

The optimized dual-layer proton irradiation reduce the fluence requirement to create a thermally stable high resistivity substrate from 10^{15} cm^{-2} to 4×10^{14} cm^{-2}, which is 60% reduction compared to the conventional irradiation. This also reduce the irradiation time by 60%, which reduce the process cost. Due to the reduction in the main irradiation fluence, the optimized dual-layer proton irradiation reduce the margin distance requirement for active devices from 50 μm to 22 μm, which is 56% reduction compared to the conventional irradiation, leading to less wasted area for active device placement.

The proposed dual-layer proton irradiation has been tested on a 300 GHz band CMOS on-chip Vivaldi antenna and a 300 GHz band CMOS on-chip chip-to-waveguide transition to evaluate its efficacy on the sub-THz passive components. After irradiation, the antenna shows a 4 dB gain improvement from 2 dBi to 6 dBi, which corresponds to efficiency improvement from 27% to 87%. In addition, the irradiated antenna was able to withstand the heat treatment test without any change in gain. The irradiation on the chip-to-waveguide transition resulting in a 2.1 dB insertion loss reduction from 4.9 dB to 2.8 dB.

Based on the results above, the proposed dual-layer proton irradiation is able to improve the performance of CMOS on-chip passive components for the future low-cost 6G transceiver system implementation.

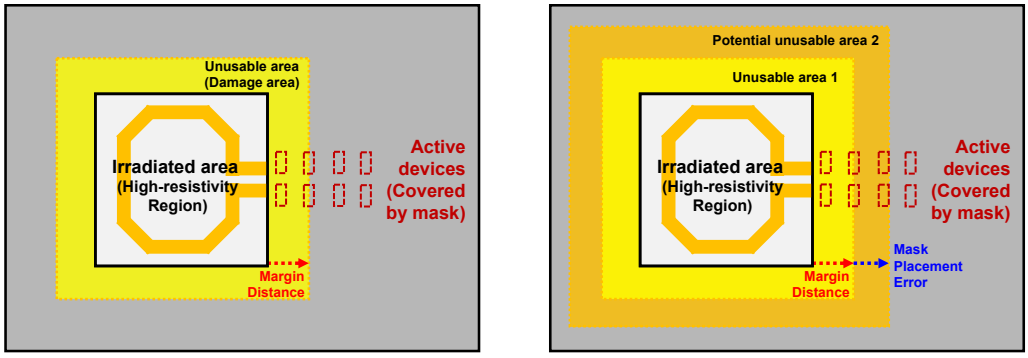


Figure 6.1: Margin distance requirement caused by (a) only lateral scattering and (b) both lateral scattering and mask placement error.

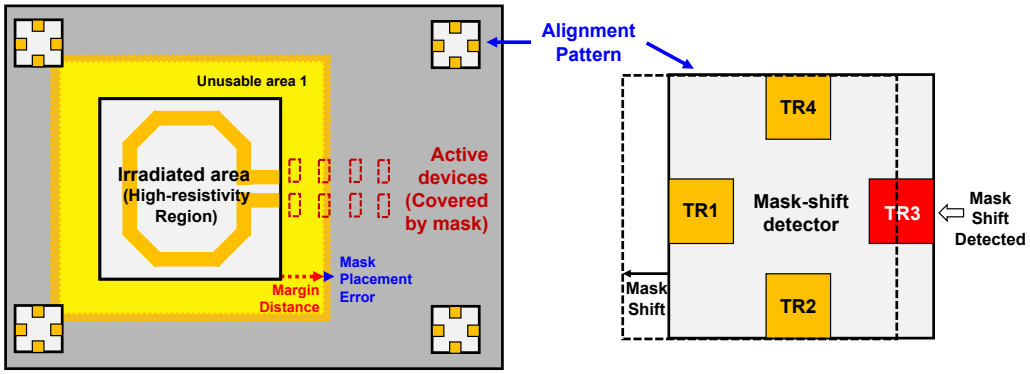


Figure 6.2: Mask placement accuracy improvement and verification method for better yield.

6.2 Future Directions

6.2.1 Mask Placement Reliability Improvement

Currently, this thesis mainly focuses on the formulation and optimization of dual-layer proton irradiation process in terms of proton fluence and irradiation depth, with margin distance from the mask edge determined purely from the proton lateral scattering (Fig. 6.1(a)). However, errors in the mask placement can increase the required margin distance (Fig. 6.1(b)) and invalidate any improvement achieved from scattering-dependent margin distance. Therefore, more research should be performed on mask placement accuracy improvement and mask placement verification method. Mask placement accuracy can be improved by creating automatic machine-based/machine-assisted mask alignment algorithm with the help of on-chip alignment mark (Fig. 6.2). Furthermore, the alignment mark should be able to detect the mask shift for binning and process improvement

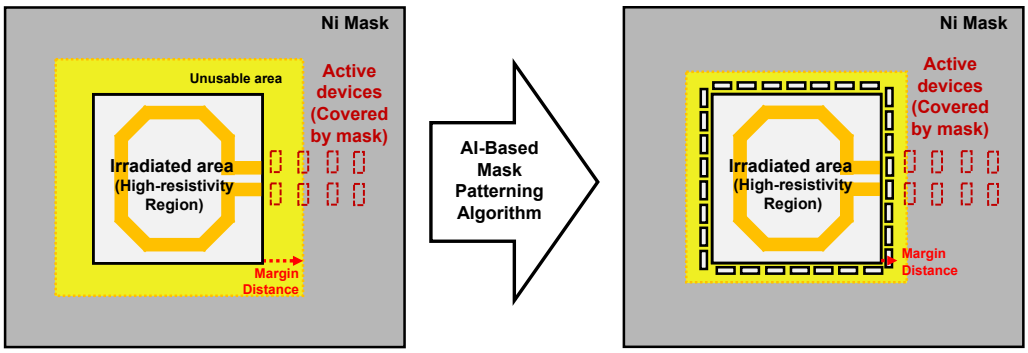


Figure 6.3: AI-assisted mask patterning for scattering reduction.

purpose, with this mark designed to be as small and simple as possible to minimize verification cost.

6.2.2 AI-Assisted Mask Patterning for Further Scattering Reduction

In addition to fluence control, mask patterning is also one of the method to reduce ion scattering. This method has been widely implemented on semiconductor lithography process to improve pattern accuracy and reduce scattering [140]. However, the calculation of such pattern requires complex model and large computational power, with the resulting optimum pattern is typically irregularly shaped. To speed up the calculation process and improve pattern performance, AI based mask patterning algorithm has been proposed [141]. This method can also be implemented to the mask creation for dual-layer proton irradiation purpose to further reduce lateral scattering and reduce margin distance (Fig. 6.3).

6.2.3 Process-Independent Irradiation Parameters Prediction Model

The dual-layer proton irradiation parameters obtained in this thesis are optimized for a standard CMOS process on 180 nm and 65 nm process nodes with planar transistor. While this technique can be applied on a significantly different process, such as SiGe BiCMOS or CMOS nodes with FinFET transistor ($<$ 16 nm), the irradiation parameters needs to be re-optimized. This re-optimization process takes a lot of time and investment to be performed. Therefore, a mathematical prediction model should be developed to predict the parameters requirement with reasonable accuracy. This model will narrows down the number of cases need to be tested, and reduce the re-optimization time. This also simplifies the integration of a new process and enable quick evaluation when considering the integration of a certain process.

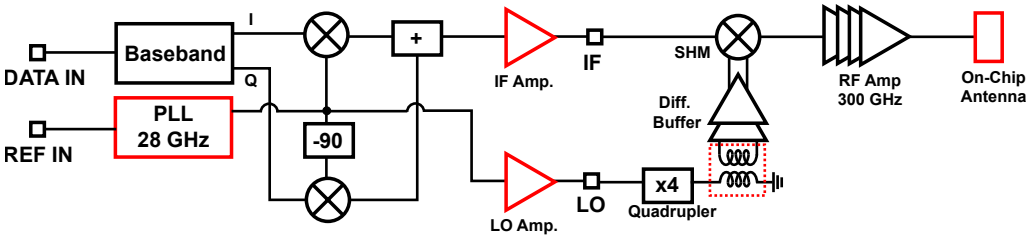


Figure 6.4: Possible target for multi-component system level irradiation, marken in red.

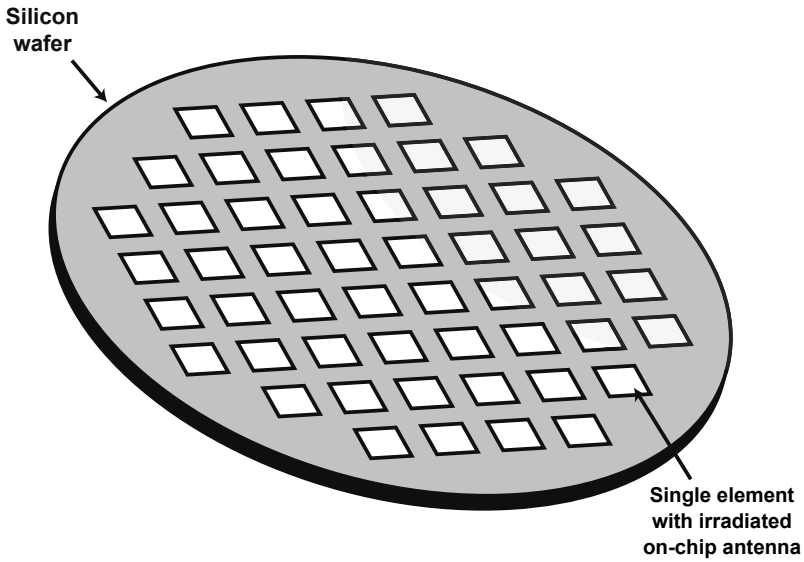


Figure 6.5: Fully on-chip wafer-scale phased array.

6.2.4 System-Level Multi-Component Irradiation

This thesis has demonstrated improvement on individual passive component (inductor, antenna, chip-to-waveguide transition) after dual-layer proton irradiation, and how this improvement happens from sub-6GHz frequency to the 300 GHz band frequency range. Therefore, it is possible to use irradiation to improve the performance of all the TRX building blocks through passive component improvement, resulting in system-wide performance improvement. The largest improvement happens especially to blocks that use inductors or transformers, such as LO PLL and various amplifiers (IF, RF, LO, etc.). Furthermore, the noise isolation guard-band can be created through irradiation to isolate noise sensitive circuits with other circuits.

6.2.5 Wafer Scale Array

Wafer-scale phased-arrays are being used recently to implement high performance millimeter-wave phased-arrays as in [142]. The trade-off between the chip cost and the PCB cost is

one of the main considerations before choosing the suitable packaging option. Smaller chips may cost less due to the high yield, but an expensive PCB is required to implement the high frequency connections. On the other hand, a wafer-scale phased-array has all the high-frequency connections on-chip, but the chip area is very large. The wafer-scale phased-array concept is shown in Fig. 6.5. This concept has been applied successfully for frequencies as high as 440GHz [142]. The small antenna size at sub-terahertz frequency enables the on-chip antenna and the on-chip array implementation options. Previously, the low resistivity of the silicon substrate causes the antenna efficiency to drop heavily. However, the dual-layer proton irradiation introduced in this thesis should be able to solve this issue.

Bibliography

[1] H. Tataria, M. Shafi, A. F. Molisch, M. Dohler, H. Sjoland, and F. Tufvesson, "6g wireless systems: Vision, requirements, challenges, insights, and opportunities," *Proc. IEEE*, vol. 109, no. 7, pp. 1166–1199, Jul. 2021.

[2] Y. Yoon, H. Kim, H. Kim, K.-S. Lee, C.-H. Lee, and J. S. Kenney, "A 2.4-ghz cmos power amplifier with an integrated antenna impedance mismatch correction system," *IEEE Journal of Solid-State Circuits*, vol. 49, no. 3, pp. 608–621, Mar. 2014.

[3] C. Wang, H. Herdian, W. Zheng, C. Liu, J. Mayeda, Y. Liu, O. A. Yong, W. Wang, Y. Zhang, C. D. Gomez, A. Shehata, S. Kato, I. Abdo, T. Jyo, H. Hamada, H. Takahashi, H. Sakai, A. Shirane, and K. Okada, "A 236-to-266GHz 4-element amplifier-last phased-array transmitter in 65nm CMOS," in *Proc. Int. Solid-State Circuits Conf. (ISSCC)*, Feb. 2024, pp. 415–417, doi: 10.1109/ISSCC49657.2024.10454273.

[4] L. S. Lee, C. Liao, C. L. Lee, T. H. Huang, D. D. L. Tang, T. S. Duh, and T. T. Yang, "Isolation on Si wafers by MeV proton bombardment for RF integrated circuits," *IEEE Trans. Electron Devices*, vol. 48, no. 5, pp. 928–934, May 2001, doi: 10.1109/16.918241.

[5] D. Tang, W. Lin, L. Lai, C. Wang, L. Lee, H. Hsu, C. Wu, C. Chang, W. Lien, C. Chao, C. Lee, G. Chern, J. Guo, C. Chang, Y. Sun, D. Du, K. Lan, and L. Lin, "The integration of proton bombardment process into the manufacturing of mixed-signal/RF chips," in *IEDM Tech. Dig.*, Dec. 2003, pp. 28.6.1–28.6.4, doi: 10.1109/IEDM.2003.1269370.

[6] C. Yue and S. Wong, "Physical modeling of spiral inductors on silicon," *IEEE Transactions on Electron Devices*, vol. 47, no. 3, pp. 560–568, Mar. 2000, doi: 10.1109/16.824729.

[7] A. Standaert and P. Reynaert, "A 390-GHz Outphasing Transmitter in 28-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 55, no. 10, pp. 2703–2713, Oct. 2020.

[8] M. Shafi, A. F. Molisch, P. J. Smith, T. Haustein, P. Zhu, P. De Silva, F. Tufvesson, A. Benjebbour, and G. Wunder, "5g: A tutorial overview of standards, trials, challenges, deployment, and practice," *IEEE Journal on Selected Areas in Communications*, vol. 35, no. 6, pp. 1201–1221, Jun. 2017.

[9] S. Parkvall, E. Dahlman, A. Furuskar, and M. Frenne, "Nr: The new 5g radio access technology," *IEEE Communications Standards Magazine*, vol. 1, no. 4, pp. 24–30, Dec. 2017.

[10] K. B. Letaief, W. Chen, Y. Shi, J. Zhang, and Y.-J. A. Zhang, "The roadmap to 6g: Ai empowered wireless networks," *IEEE Communications Magazine*, vol. 57, no. 8, pp. 84–90, Aug. 2019.

[11] Z. Zhang, Y. Xiao, Z. Ma, M. Xiao, Z. Ding, X. Lei, G. K. Karagiannidis, and P. Fan, "6g wireless networks: Vision, requirements, architecture, and key technologies," *IEEE Vehicular Technology Magazine*, vol. 14, no. 3, pp. 28–41, Sep. 2019.

[12] R. Li, "Network 2030: Market drivers and prospects," in *Proc. 1st Int. Telecommun. Union (ITU-T) Workshop Netw.*, Oct. 2018, pp. 1–21.

[13] "Network 2030: A blueprint of technology, applications, and market drivers toward the year 2030," International Telecommunication Union (ITU-T), Tech. Rep., Nov. 2019. [Online]. Available: http://handle.itu.int/11.1002/pub/81363ffa-en

[14] A. Clemm, M. T. Vega, H. K. Ravuri, T. Wauters, and F. D. Turck, "Toward truly immersive holographic-type communication: Challenges and solutions," *IEEE Communications Magazine*, vol. 58, no. 1, pp. 93–99, Jan. 2020.

[15] V. Petrov, J. Kokkoniemi, D. Moltchanov, J. Lehtomaki, Y. Koucheryavy, and M. Juntti, "Last meter indoor terahertz wireless access: Performance insights and implementation roadmap," *IEEE Communications Magazine*, vol. 56, no. 6, pp. 158–165, Jun. 2018.

[16] A. Matsubayashi, Y. Makino, and H. Shinoda, "Direct finger manipulation of 3d object image with ultrasound haptic feedback," in *Proceedings of the 2019 CHI Conference on Human Factors in Computing Systems*, ser. CHI '19. ACM, May 2019.

[17] G. P. Fettweis, "The tactile internet: Applications and challenges," *IEEE Vehicular Technology Magazine*, vol. 9, no. 1, pp. 64–70, Mar. 2014.

[18] I. del Portillo, B. G. Cameron, and E. F. Crawley, "A technical comparison of three low earth orbit satellite constellation systems to provide global broadband," *Acta Astronautica*, vol. 159, pp. 123–135, Jun. 2019.

[19] H. D. Schotten, R. Sattiraju, D. G. Serrano, Z. Ren, and P. Fertl, "Availability indication as key enabler for ultra-reliable communication in 5g," in *2014 European Conference on Networks and Communications (EuCNC)*. IEEE, Jun. 2014.

[20] M. T. Vega, T. Mehmli, J. v. d. Hooft, T. Wauters, and F. D. Turck, "Enabling virtual reality for the tactile internet: Hurdles and opportunities," in *2018 14th International Conference on Network and Service Management (CNSM)*, 2018, pp. 378–383.

[21] H.-J. Song and N. Lee, "Terahertz communications: Challenges in the next decade," *IEEE Trans. THz Sci. Technol.*, vol. 12, no. 2, pp. 105–117, Mar. 2022.

[22] A. Saeed, H. E. Yaldiz, and F. Alagoz, "Ghz-to-thz broadband communications for 6g non-terrestrial networks," *ITU Journal on Future and Evolving Technologies*, vol. 4, no. 1, pp. 241–250, Mar. 2023.

[23] K. Sarabandi, A. Jam, M. Vahidpour, and J. East, "A Novel Frequency Beam-Steering Antenna Array for Submillimeter-Wave Applications," *IEEE Trans. THz Sci. Technol.*, vol. 8, no. 6, pp. 654–665, Nov. 2018.

[24] P. V. Testa, C. Carta, and F. Ellinger, "Novel high-performance bondwire chip-to-chip interconnections for applications up to 220 GHz," *IEEE Microwave Wireless Compon. Lett.*, vol. 28, no. 2, pp. 102–104, Feb. 2018, doi: 10.1109/LMWC.2018.2792695.

[25] C. H. Li and T. Y. Chiu, "Low-loss single-band, dual-band, and broadband mm-wave and (sub-)THz interconnects for THz SoP heterogeneous system integration," *IEEE Trans. THz Sci. Technol.*, vol. 12, no. 2, pp. 130–143, Mar. 2022, doi: 10.1109/TTHZ.2021.3128596.

[26] A. Karakuzulu, W. A. Ahmad, D. Kissinger, and A. Malignaggi, "A four-channel bidirectional d-band phased-array transceiver for 200 gb/s 6g wireless communications in a 130-nm bicmos technology," *IEEE J. Solid-State Circuits*, vol. 58, no. 5, pp. 1310–1322, May 2023.

[27] X. Yi, C. Wang, X. Chen, J. Wang, J. Grajal, and R. Han, "A 220-to-320-GHz FMCW radar in 65-nm CMOS using a frequency-comb architecture," *IEEE J. Solid-State Circuits*, vol. 56, no. 2, pp. 327–339, feb 2021.

[28] C. Lee and J. Jeong, "THz CMOS On-Chip Antenna Array Using Defected Ground Structure," *Electronics*, vol. 9, no. 7, p. 1137, Jul. 2020.

[29] C.-G. Choi, H.-H. Jeong, and H.-J. Song, "THz-Wave Waveguide Packaging with Multiple THz On-Chip Transitions Integrated in Single Chip," in *2021 IEEE MTT-S International Microwave Symposium (IMS)*. IEEE, Jun. 2021.

[30] L. J. Xu, F. C. Tong, X. Bai, and Q. Li, "Design of miniaturised on-chip slot antenna for THz detector in CMOS," *IET Microwaves, Antennas and Propagation*, vol. 12, no. 8, pp. 1324–1331, mar 2018.

[31] T. Pfahler, M. Vossiek, and J. Schür, "Compact and broadband 300 GHz three-element on-chip patch antenna," in *Proc. Radio and Wireless Symp. (RWS)*, Jan. 2023, pp. 139–142, doi: 10.1109/RWS55624.2023.10046297.

[32] H. M. Cheema and A. Shamim, "The Last Barrier: On-chip Antennas," *IEEE Microwave Mag.*, vol. 14, no. 1, pp. 79–91, Jan. 2013.

[33] J. Buechler, E. Kasper, P. Russer, and K. Strohm, "Silicon high-resistivity-substrate millimeter-wave technology," *IEEE Transactions on Electron Devices*, vol. 33, no. 12, pp. 2047–2052, Dec. 1986.

[34] M. Spirito, F. De Paola, L. Nanver, E. Valletta, B. Rong, B. Rejaei, L. de Vreede, and J. Burghartz, "Surface-passivated high-resistivity silicon as a true microwave substrate," *IEEE Trans. Microwave Theory Tech.*, vol. 53, no. 7, pp. 2340–2347, Jul. 2005, 10.1109/TMTT.2005.850435.

[35] M. Capelle, J. Billoue, P. Poveda, and G. Gautier, "N-type porous silicon substrates for integrated rf inductors," *IEEE Trans. Electron Devices*, vol. 58, no. 11, pp. 4111–4114, Nov. 2011.

[36] K. B. Ali, C. R. Neve, A. Gharsallah, and J.-P. Raskin, "RF performance of SOI CMOS technology on commercial 200-mm enhanced signal integrity high resistivity SOI substrate," *IEEE Trans. Electron Devices*, vol. 61, no. 3, pp. 722–728, Mar. 2014, doi: 10.1109/TED.2014.2302685.

[37] N. Andre, D. Flandre, M. Rack, L. Nyssens, C. Gimeno, D. Oueslati, K. Ben Ali, S. Gilet, C. Craeye, and J.-P. Raskin, "Ultra low-loss Si substrate for on-chip UWB

GHz antennas," *IEEE J. Electron Devices Soc.*, vol. 7, pp. 393–397, 2019, doi: 10.1109/JEDS.2019.2902636.

[38] N. Li, K. Okada, T. Inoue, T. Hirano, Q. Bu, A. T. Narayanan, T. Siriburanon, H. Sakane, and A. Matsuzawa, "High-Q inductors on locally semi-insulated Si substrate by Helium-3 bombardment for RF CMOS integrated circuits," *IEEE Trans. Electron Devices*, vol. 62, no. 4, pp. 1269–1275, Apr. 2015, doi: 10.1109/TED.2015.2403873.

[39] K. Chan, A. Chin, Y. Lin, C. Chang, C. Zhu, M. Li, D. Kwong, S. McAlister, D. Duh, and W. Lin, "Integrated antennas on Si with over 100 GHz performance, fabricated using an optimized proton implantation process," *IEEE Microwave Wireless Compon. Lett.*, vol. 13, no. 11, pp. 487–489, Nov. 2003, doi: 10.1109/LMWC.2003.817146.

[40] Z. Li, S. Lee, J. L. Evans, and D. F. Baldwin, "Comprehensive study of lead-free reflow process for a 3-D flip chip on silicon package," *IEEE Trans. Compon. Packag. Manuf. Technol.*, vol. 1, no. 11, pp. 1856–1863, Nov. 2011, doi: 10.1109/TCPMT.2011.2163314.

[41] M. Harrison, J. Vincent, and H. Steen, "Lead free reflow soldering for electronics assembly," *Soldering and Surface Mount Technology*, vol. 13, no. 3, pp. 21–38, Dec. 2001.

[42] H. Herdian, T. Inoue, A. Shirane, and K. Okada, "Dual-layer proton irradiation for passive component enhancement and noise coupling suppression on CMOS process," *IEEE Trans. Electron Devices*, vol. 71, no. 8, pp. 4498–4503, Aug. 2024.

[43] G. H. Schwuttke, K. Brack, E. F. Gorey, A. Kahan, and L. F. Lowe, "Resistivity and annealing properties of implanted Si:H+," *Radiat. Eff.*, vol. 6, no. 1, pp. 103–106, Jan. 1970, doi: 10.1080/00337577008235051.

[44] J. F. Ziegler, M. Ziegler, and J. Biersack, "Srim – the stopping and range of ions in matter (2010)," *Nuclear Instruments and Methods in Physics Research Section B: Beam Interactions with Materials and Atoms*, vol. 268, no. 11–12, pp. 1818–1823, Jun. 2010.

[45] J. R. Sabin and J. Oddershede, "Calculated stopping cross sections for diamond and solid silicon and germanium," *Nuclear Instruments and Methods in Physics Research Section B: Beam Interactions with Materials and Atoms*, vol. 24–25, pp. 339–342, Apr. 1987.

[46] J. F. Ziegler. (2024, Jul.). [Online]. Available: http://srim.org/PlotCit.htm

[47] S. Agarwal, Y. Lin, C. Li, R. Stoller, and S. Zinkle, "On the use of srim for calculating vacancy production: Quick calculation and full-cascade options," *Nuclear Instruments and Methods in Physics Research Section B: Beam Interactions with Materials and Atoms*, vol. 503, pp. 11–29, Sep. 2021.

[48] J. Linhard, M. Scharff, and H. E. Schiott, "Range concepts and heavy ion ranges," *Matt. Fys. Medd. Dan. Vid. Selsk*, vol. 33, no. 14, pp. 1–42, 1963.

[49] M. Nastasi and J. W. Mayer, *Ion Implantation and Synthesis of Materials*, 1st ed., ser. Springer Series in Materials Science. Heidelberg: Springer Berlin, 2006.

[50] J. Biersack, "Calculation of projected ranges — analytical solutions and a simple general algorithm," *Nuclear Instruments and Methods*, vol. 182–183, pp. 199–206, Apr. 1981.

[51] D. G. Ashworth, M. D. J. Bowyer, and R. Oven, "A revised version of pral-the projected range algorithm," *Journal of Physics D: Applied Physics*, vol. 24, no. 8, pp. 1376–1380, Aug. 1991.

[52] Y. Wu, A. Chin, K. Shih, C. Wu, C. Liao, S. Pai, and C. Chi, "Fabrication of very high resistivity si with low loss and cross talk," *IEEE Electron Device Letters*, vol. 21, no. 9, pp. 442–444, Sep. 2000, doi: 10.1109/55.863105.

[53] I. Tyschenko, F. Tikhonenko, A. Gutakovskii, V. Vdovin, K. Rudenko, and V. Popov, "High-resistance thermally stable silicon layers produced by the co+ ion implantation," *Materials Letters*, vol. 318, pp. 132–162, Jul. 2022, doi: 10.1016/j.matlet.2022.132162.

[54] B. Rong, J. Burghartz, L. Nanver, B. Rejaei, and M. vanderZwan, "Surface-passivated high-resistivity silicon substrates for rfics," *IEEE Electron Device Letters*, vol. 25, no. 4, pp. 176–178, Apr. 2004, doi: 10.1109/LED.2004.826295.

[55] M. Norling, D. Kuylenstierna, A. Vorobiev, K. Reimann, D. Lederer, J.-P. Raskin, and S. Gevorgian, "Comparison of high-resistivity silicon surface passivation methods," in *2007 European Microwave Integrated Circuit Conference*, Oct. 2007, pp. 215–218, doi: 10.1109/EMICC.2007.4412687.

[56] L. Palmetshofer and J. Reisinger, "Defect levels in h+-, d+-, and he+-bombarded silicon," *Journal of Applied Physics*, vol. 72, no. 6, pp. 2167–2173, Sep. 1992.

[57] J. Barbot, C. Blanchard, E. Ntsoenzok, and J. Vernois, "Defect levels in n-silicon after high energy and high dose implantation of proton," *Materials Science and Engineering: B*, vol. 36, no. 1–3, pp. 81–84, Jan. 1996.

[58] W. Wondrak and D. Silber, "Buried recombination layers with enhanced n-type conductivity for silicon power devices," *Physica B+C*, vol. 129, no. 1–3, pp. 322–326, Mar. 1985.

[59] J. G. Laven, R. Job, H.-J. Schulze, F.-J. Niedernostheide, W. Schustereder, and L. Frey, "Activation and dissociation of proton-induced donor profiles in silicon," *ECS Journal of Solid State Science and Technology*, vol. 2, no. 9, pp. P389–P394, 2013.

[60] J. G. Laven, M. Jelinek, R. Job, W. Schustereder, H. Schulze, M. Rommel, and L. Frey, "Dlts characterization of proton-implanted silicon under varying annealing conditions," *physica status solidi (b)*, vol. 251, no. 11, pp. 2189–2192, Sep. 2014.

[61] A. V. Dvurechenskii and L. S. Smirnov, "Localized states and conductivity in silicon amorphized by ion implantation," *Physica Status Solidi (a)*, vol. 56, no. 2, pp. 647–654, Dec. 1979, doi: 10.1002/pssa.2210560231.

[62] P. Sigmund and K. Winterbon, "Small-angle multiple scattering of ions in the screened coulomb region," *Nuclear Instruments and Methods*, vol. 119, pp. 541–557, Jul. 1974, doi: 10.1016/0029-554x(74)90805-2.

[63] A. Marwick and P. Sigmund, "Small-angle multiple scattering of ions in the screened coulomb region," *Nuclear Instruments and Methods*, vol. 126, no. 3, pp. 317–323, Jun. 1975, doi: 10.1016/0029-554x(75)90693-x.

[64] D. J. Mazey, R. S. Nelson, and R. S. Barnes, "Observation of ion bombardment damage in silicon," *Philosophical Magazine*, vol. 17, no. 150, pp. 1145–1161, Jun. 1968.

[65] *Cyclotron Produced Radionuclides: Principles and Practice*, ser. Technical Reports Series. Vienna: International Atomic Energy Agency, 2008, no. 465. [Online]. Available: https://www.iaea.org/publications/7849/cyclotron-produced-radionuclides-principles-and-practice

[66] H. J. Barnaby, "Total-ionizing-dose effects in modern CMOS technologies," *IEEE Trans. Nucl. Sci.*, vol. 53, no. 6, pp. 3103–3121, Dec. 2006, doi: 10.1109/TNS.2006.885952.

[67] Q. Zeng, Z. Yang, X. Wang, S. Li, and F. Gao, "Research progress on radiation damage mechanism of SiC MOSFETs under various irradiation conditions," *IEEE Trans. Electron Devices*, vol. 71, no. 3, pp. 1718–1727, Mar. 2024, doi: 10.1109/TED.2024.3359172.

[68] C.-M. Zhang, F. Jazaeri, G. Borghello, F. Faccio, S. Mattiazzo, A. Baschirotto, and C. Enz, "Characterization and modeling of gigarad-tid-induced drain leakage current of 28-nm bulk mosfets," *IEEE Transactions on Nuclear Science*, vol. 66, no. 1, pp. 38–47, Jan. 2019, doi: 10.1109/TNS.2018.2878105.

[69] M. Rack, L. Nyssens, and J. P. Raskin, "Low-loss Si-substrates enhanced using buried PN junctions for RF applications," *IEEE Electron Device Lett.*, vol. 40, no. 5, pp. 690–693, May 2019, doi: 10.1109/LED.2019.2908259.

[70] H. Gamble, B. Armstrong, S. Mitchell, Y. Wu, V. Fusco, and J. Stewart, "Low-loss CPW lines on surface stabilized high-resistivity silicon," *IEEE Microw. Guided Wave Lett.*, vol. 9, no. 10, pp. 395–397, 1999, doi: 10.1109/75.798027.

[71] Y. Song, G. Zhang, X. Cai, B. Dou, Z. Wang, Y. Liu, H. Zhou, L. Zhong, G. Dai, X. Zuo, and S. Wei, "General model for defect dynamics in ionizing-irradiated sio2-si structures," *Small*, vol. 18, no. 14, Feb. 2022.

[72] H. Berkowitz, D. Burnell, R. Hillard, R. Mazur, and P. Rai-Choudhury, "Optimization of the spreading resistance profiling technique for submicron structures," *Solid-State Electronics*, vol. 33, no. 6, pp. 773–781, Jun. 1990, doi: 10.1016/0038-1101(90)90191-g.

[73] C.-M. Yang, C.-K. Wei, H.-P. Chen, J.-S. Luo, Y. J. Chang, T.-C. Wu, and C.-S. Lai, "Scanning spreading resistance microscopy for doping profile in saddle-fin devices," *IEEE Transactions on Nanotechnology*, vol. 16, no. 6, pp. 999–1003, Nov. 2017, doi: 10.1109/tnano.2017.2738667.

[74] H. Hasegawa, M. Furukawa, and H. Yanai, "Properties of microstrip line on si-sio/sub 2/ system," *IEEE Transactions on Microwave Theory and Techniques*, vol. 19, no. 11, pp. 869–881, Nov. 1971, doi: 10.1109/tmtt.1971.1127658.

[75] Y. Eo and W. Eisenstadt, "High-speed vlsi interconnect modeling based on s-parameter measurements," *IEEE Transactions on Components, Hybrids, and Manufacturing Technology*, vol. 16, no. 5, pp. 555–562, 1993, doi: 10.1109/33.239889.

[76] K. L. Merkle, "Radiation-induced point defect clusters in copper and gold," *physica status solidi (b)*, vol. 18, no. 1, pp. 173–188, Jan. 1966.

[77] S. Kumar and R. Sharma, "Analytical modeling and performance benchmarking of on-chip interconnects with rough surfaces," *IEEE Transactions on Multi-Scale Computing Systems*, vol. 4, no. 3, pp. 272–284, Jul. 2018.

[78] L. Simonovich, "Practical method for modeling conductor roughness using cubic close-packing of equal spheres," in *2016 IEEE International Symposium on Electromagnetic Compatibility (EMC)*. IEEE, Jul. 2016.

[79] H. Herdian, C. Wang, T. Inoue, A. Shirane, and K. Okada, "A proton irradiated CMOS on-chip vivaldi antenna for 300 GHz band slat array implementation," *IEEE Open Journal of Antennas and Propagation*, 2024, (Early Access).

[80] S. X. Huang, Y. S. Zeng, G. B. Wu, K. F. Chan, B. J. Chen, M. Y. Xia, S. W. Qu, and C. H. Chan, "Terahertz Mueller Matrix Polarimetry and Polar Decomposition," *IEEE Trans. THz Sci. Technol.*, vol. 10, no. 1, pp. 74–84, Jan. 2020.

[81] J. Grajal, G. Rubio-Cidre, A. Badolato, L. Ubeda-Medina, F. Garcia-Rial, A. Garcia-Pino, and O. Rubinos, "Compact Radar Front-End for an Imaging Radar at 300 GHz," *IEEE Trans. THz Sci. Technol.*, vol. 7, no. 3, pp. 268–273, May 2017.

[82] A. Mostajeran, S. M. Naghavi, M. Emadi, S. Samala, B. P. Ginsburg, M. Aseeri, and E. Afshari, "A high-resolution 220-ghz ultra-wideband fully integrated isar imaging system," *IEEE Trans. Microwave Theory Tech.*, vol. 67, no. 1, pp. 429–442, Jan. 2019.

[83] S. Thomas, C. Bredendiek, and N. Pohl, "A SiGe-Based 240-GHz FMCW Radar System for High-Resolution Measurements," *IEEE Trans. Microwave Theory Tech.*, vol. 67, no. 11, pp. 4599–4609, Nov. 2019.

[84] E. Turkmen, I. K. Aksoyak, P. Djondovic, S. B. Yilmaz, W. Debski, W. Winkler, and A. C. Ulusoy, "A 223-276-GHz Cascadable FMCW Transceiver in 130-nm SiGe BiCMOS for Scalable MIMO Radar Arrays," *IEEE Trans. Microwave Theory Tech.*, vol. 71, no. 12, pp. 5393–5412, Dec. 2023.

[85] J. Grzyb, K. Statnikov, N. Sarmah, B. Heinemann, and U. R. Pfeiffer, "A 210–270-ghz circularly polarized fmcw radar with a single-lens-coupled sige hbt chip," *IEEE Trans. THz Sci. Technol.*, vol. 6, no. 6, pp. 771–783, Nov. 2016.

[86] R. Hasan, M. H. Eissa, W. A. Ahmad, H. J. Ng, and D. Kissinger, "Wideband and efficient 256-ghz subharmonic- based fmcw radar transceiver in 130-nm sige bicmos technology," *IEEE Trans. Microwave Theory Tech.*, vol. 71, no. 1, pp. 59–70, Jan. 2023.

[87] I. Abdo, C. da Gomez, C. Wang, K. Hatano, Q. Li, C. Liu, K. Yanagisawa, A. A. Fadila, T. Fujimura, T. Miura, K. K. Tokgoz, J. Pang, H. Hamada, H. Nosaka, A. Shirane, and K. Okada, "A Bi-Directional 300-GHz-Band Phased-Array Transceiver in 65-nm CMOS With Outphasing Transmitting Mode and LO Emission Cancellation," *IEEE J. Solid-State Circuits*, vol. 57, no. 8, pp. 2292–2308, Aug. 2022.

[88] S. Lee, S. Hara, T. Yoshida, S. Amakawa, R. Dong, A. Kasamatsu, J. Sato, and M. Fujishima, "An 80-Gb/s 300-GHz-Band Single-Chip CMOS Transceiver," *IEEE J. Solid-State Circuits*, vol. 54, no. 12, pp. 3577–3588, Dec. 2019.

[89] S. Hara, R. Dong, S. Lee, K. Takano, N. Toshida, A. Kasamatsu, K. Sakakibara, T. Yoshida, S. Amakawa, and M. Fujishima, "A 76-gbit/s 265-ghz cmos receiver with wr-3.4 waveguide interface," *IEEE J. Solid-State Circuits*, vol. 57, no. 10, pp. 2988–2998, Oct. 2022.

[90] K. Katayama, K. Takano, S. Amakawa, S. Hara, A. Kasamatsu, K. Mizuno, K. Takahashi, T. Yoshida, and M. Fujishima, "A 300 GHz CMOS Transmitter With 32-QAM 17.5 Gb/s/ch Capability Over Six Channels," *IEEE J. Solid-State Circuits*, vol. 51, no. 12, pp. 3037–3048, Dec. 2016.

[91] H. Hamada, T. Tsutsumi, H. Matsuzaki, T. Fujimura, I. Abdo, A. Shirane, K. Okada, G. Itami, H.-J. Song, H. Sugiyama, and H. Nosaka, "300-GHz-Band 120-Gb/s Wireless Front-End Based on InP-HEMT PAs and Mixers," *IEEE J. Solid-State Circuits*, vol. 55, no. 9, pp. 2316–2335, Sep. 2020.

[92] S. van Berkel, E. S. Malotaux, C. De Martino, M. Spirito, D. Cavallo, A. Neto, and N. Llombart, "Wideband Double Leaky Slot Lens Antennas in CMOS Technology at Submillimeter Wavelengths," *IEEE Trans. THz Sci. Technol.*, vol. 10, no. 5, pp. 540–553, Sep. 2020.

[93] T. Sowlati, S. Sarkar, B. Perumana, W. L. Chan, B. Afshar, M. Boers, D. Shin, T. Mercer, W.-H. Chen, A. P. Toda, A. G. Besoli, S. Yoon, S. Kyriazidou, P. Yang, V. Aggarwal, N. Vakilian, D. Rozenblit, M. Kahrizi, J. Zhang, A. Wang, P. Sen, D. Murphy, M. Mikhemar, A. Sajjadi, A. Mehrabani, B. Ibrahim, B. Pan, K. Juan, S. Xu, C. Guan, G. Geshvindman, K. Low, N. Kocaman, H. Eberhart, K. Kimura, I. Elgorriaga, V. Roussel, H. Xie, L. Shi, and V. Kodavati, "A 60ghz 144-element phased-array transceiver with 51dbm maximum eirp and ±60° beam steering for backhaul application," in *2018 IEEE International Solid - State Circuits Conference - (ISSCC)*. IEEE, Feb. 2018.

[94] H.-C. Park, D. Kang, S. M. Lee, B. Park, K. Kim, J. Lee, Y. Aoki, Y. Yoon, S. Lee, D. Lee, D. Kwon, S. Kim, J. Kim, W. Lee, C. Kim, S. Park, J. Park, B. Suh, J. Jang, M. Kim, D. Minn, I. Park, S. Kim, K. Min, J. Park, S. Jeon, A.-S. Ryu, Y. Cho, S. T. Choi, K. H. An, Y. Kim, J. H. Lee, J. Son, and S.-G. Yang, "4.1 a 39ghz-band cmos 16-channel phased-array transceiver ic with a companion dual-stream if transceiver ic for 5g nr base-station applications," in *2020 IEEE International Solid- State Circuits Conference - (ISSCC)*. IEEE, Feb. 2020.

[95] Y. Wang, R. Wu, J. Pang, D. You, A. A. Fadila, R. Saengchan, X. Fu, D. Matsumoto, T. Nakamura, R. Kubozoe, M. Kawabuchi, B. Liu, H. Zhang, J. Qiu, H. Liu, N. Oshima, K. Motoi, S. Hori, K. Kunihiro, T. Kaneko, A. Shirane, and K. Okada, "A 39-ghz 64-element phased-array transceiver with built-in phase and amplitude calibrations for large-array 5g nr in 65-nm cmos," *IEEE J. Solid-State Circuits*, vol. 55, no. 5, pp. 1249–1269, May 2020.

[96] J. S. Herd and M. D. Conway, "The Evolution to Modern Phased Array Architectures," *Proc. IEEE*, vol. 104, no. 3, pp. 519–529, Mar. 2016.

[97] C. Wang, I. Abdo, C. Liu, C. d. Gomez, J. Mayeda, H. Herdian, W. Wang, X. Fu, D. You, A. Shehata, S. Park, Y. Wang, J. Pang, H. Sakai, A. Shirane, and K. Okada, "A sub-THz full-duplex phased-array transceiver with self-interference cancellation and LO feedthrough suppression," *IEEE J. Solid-State Circuits*, vol. 59, no. 4, pp. 978–992, Apr. 2024, doi: 10.1109/JSSC.2024.3353067.

[98] K. K. Tokgoz, T. Iwai, K. Okada, A. Matsuzawa, S. Maki, J. Pang, N. Nagashima, I. Abdo, S. Kawai, T. Fujimura, Y. Kawano, and T. Suzuki, "A 120gb/s 16qam cmos millimeter-wave wireless transceiver," in *2018 IEEE International Solid - State Circuits Conference - (ISSCC)*. IEEE, Feb. 2018.

[99] W. Deng, Z. Chen, H. Jia, P. Guan, T. Ma, A. Yan, S. Sun, X. Huang, G. Chen, R. Ma, S. Dong, L. Duan, Z. Wang, and B. Chi, "A d-band joint radar-communication cmos transceiver," *IEEE J. Solid-State Circuits*, vol. 58, no. 2, pp. 411–427, Feb. 2023.

[100] M. Elkhouly, J. Ha, M. J. Holyoak, D. Hendry, M. Sayginer, R. Enright, I. Kimionis, Y. Baeyens, and S. Shahramian, "Fully integrated 2d scalable tx/rx chipset for d-band phased-array-on-glass modules," in *2022 IEEE International Solid- State Circuits Conference (ISSCC)*. IEEE, Feb. 2022.

[101] J. Pang, S. Maki, S. Kawai, N. Nagashima, Y. Seo, M. Dome, H. Kato, M. Katsuragi, K. Kimura, S. Kondo, Y. Terashima, H. Liu, T. Siriburanon,

A. Tharayil Narayanan, N. Fajri, T. Kaneko, T. Yoshioka, B. Liu, Y. Wang, R. Wu, N. Li, K. K. Tokgoz, M. Miyahara, A. Shirane, and K. Okada, "A 50.1-Gb/s 60-GHz CMOS transceiver for IEEE 802.11ay with calibration of LO feedthrough and I/Q imbalance," *IEEE J. Solid-State Circuits*, vol. 54, no. 5, pp. 1375–1390, May 2019, doi: 10.1109/JSSC.2018.2886338.

[102] K. Dasgupta, S. Daneshgar, C. Thakkar, S. Kang, A. Chakrabarti, S. Yamada, N. Narevsky, D. Choudhury, J. E. Jaussi, and B. Casper, "A 60-ghz transceiver and baseband with polarization mimo in 28-nm cmos," *IEEE J. Solid-State Circuits*, vol. 53, no. 12, pp. 3613–3627, Dec. 2018.

[103] P. Zhou, J. Chen, P. Yan, J. Yu, J. Hu, H. Dong, L. Wang, D. Hou, H. Gao, and W. Hong, "A -28.5-db evm 64-qam 45-ghz transceiver for ieee 802.11aj," *IEEE J. Solid-State Circuits*, vol. 56, no. 10, pp. 3077–3093, Oct. 2021.

[104] B. B. Adela, P. T. M. van Zeijl, U. Johannsen, and A. B. Smolders, "On-Chip Antenna Integration for Millimeter-Wave Single-Chip FMCW Radar, Providing High Efficiency and Isolation," *IEEE Trans. Antennas Propag.*, vol. 64, no. 8, pp. 3281–3291, Aug. 2016.

[105] T. Deng, Y. Zhang, Z. Zheng, Q. Yan, and J.-F. Mao, "High-gain and high-efficiency sub-terahertz antenna-on-chip with microbumps for highly-integrated systems," *IEEE Trans. Antennas Propag.*, vol. 72, no. 5, pp. 4107–4115, May 2024.

[106] H. Zhu, X. Li, Z. Qi, and J. Xiao, "A 320 GHz Octagonal Shorted Annular Ring On-Chip Antenna Array," *IEEE Access*, vol. 8, pp. 84 282–84 289, 2020.

[107] X. D. Deng, Y. Li, W. Wu, and Y. Z. Xiong, "340-GHz SIW cavity-backed magnetic rectangular slot loop antennas and arrays in silicon technology," *IEEE Transactions on Antennas and Propagation*, vol. 63, no. 12, pp. 5272–5279, dec 2015.

[108] H. Zhu, X. Li, W. Feng, J. Xiao, and J. Zhang, "235 GHz on-chip antenna with miniaturised AMC loading in 65 nm CMOS," *IET Microwaves, Antennas and Propagation*, vol. 12, no. 5, pp. 727–733, mar 2018.

[109] Q. Le Zhang, X. G. Shi, B. J. Chen, K. F. Chan, K. M. Shum, and C. H. Chan, "325 ghz to 500 ghz single-layer planar goubau-line antenna with endfire radiation based on substrate mode," *IEEE Trans. Antennas Propag.*, vol. 70, no. 9, pp. 7755–7765, Sep. 2022.

[110] S. Erdogan and M. Swaminathan, "D-band quasi-yagi antenna in glass-based package," in *2021 IEEE MTT-S International Microwave and RF Conference (IMARC)*. IEEE, Dec. 2021.

[111] W. T. Khan, A. Cagri Ulusoy, G. Dufour, M. Kaynak, B. Tillack, J. D. Cressler, and J. Papapolymerou, "A d-band micromachined end-fire antenna in 130-nm sige bicmos technology," *IEEE Trans. Antennas Propag.*, vol. 63, no. 6, pp. 2449–2459, Jun. 2015.

[112] S. Gearhart, H. Ekstrom, P. Acharya, E. Kollberg, S. Jacobsson, and G. Rebeiz, "Submillimeter-wave endfire slotline antennas," in *IEEE Antennas and Propagation Society International Symposium 1992 Digest*. IEEE, 1992.

[113] X.-D. Deng, Y. Li, H. Tang, W. Wu, and Y.-Z. Xiong, "Dielectric loaded endfire antennas using standard silicon technology," *IEEE Trans. Antennas Propag.*, vol. 65, no. 6, pp. 2797–2807, Jun. 2017.

[114] P. Gibson, "The vivaldi aerial," in *1979 9th European Microwave Conference*. IEEE, Sep. 1979.

[115] C. A. Balanis, *Antenna Theory: Analysis and Design*, 4th ed. Wiley, Feb. 2016.

[116] D. Schaubert, E. Kollberg, T. Korzeniowski, T. Thungren, J. Johansson, and K. Yngvesson, "Endfire tapered slot antennas on dielectric substrates," *IEEE Trans. Antennas Propag.*, vol. 33, no. 12, pp. 1392–1400, Dec. 1985.

[117] F. J. Zucker, *Antenna engineering handbook*, 4th ed. New York: McGraw-Hill, 2007, ch. Surface-Wave Antennas, p. 10.

[118] M. Moosazadeh, S. Kharkovsky, J. T. Case, and B. Samali, "Antipodal Vivaldi antenna with improved radiation characteristics for civil engineering applications," *IET Microwaves Antennas Propag.*, vol. 11, no. 6, pp. 796–803, Mar. 2017.

[119] C. H. Ho, L. Fan, and K. Chang, "New uniplanar coplanar waveguide hybrid-ring couplers and magic-t's," *IEEE Trans. Microwave Theory Tech.*, vol. 42, no. 12, pp. 2440–2448, 1994.

[120] S. Cohn, "Slot line on a dielectric substrate," *IEEE Transactions on Microwave Theory and Techniques*, vol. 17, no. 10, pp. 768–778, Oct. 1969.

[121] G. E. Ponchak, "Rf transmission lines on silicon substrates," in *1999 29th European Microwave Conference*. IEEE, Oct. 1999.

[122] J. Krupka, B. Salski, T. Karpisz, P. Kopyt, L. Jensen, and M. Wojciechowski, "Irradiated silicon for microwave and millimeter wave applications," *IEEE Microwave and Wireless Components Letters*, vol. 32, no. 6, pp. 700–703, Jun. 2022.

[123] J. Krupka, P. Kamiński, R. Kozłowski, B. Surma, A. Dierlamm, and M. Kwestarz, "Dielectric properties of semi-insulating silicon at microwave frequencies," *Applied Physics Letters*, vol. 107, no. 8, Aug. 2015.

[124] T. Ohba and S.-i. Ikawa, "Far-infrared absorption of silicon crystals," *Journal of Applied Physics*, vol. 64, no. 8, pp. 4141–4143, Oct. 1988.

[125] M. van Exter and D. Grischkowsky, "Carrier dynamics of electrons and holes in moderately doped silicon," *Physical Review B*, vol. 41, no. 17, pp. 12 140–12 149, Jun. 1990.

[126] V. V. Parshin, R. Heidinger, B. A. Andreev, A. V. Gusev, and V. B. Shmagin, "Silicon as an advanced window material for high power gyrotrons," *International Journal of Infrared and Millimeter Waves*, vol. 16, no. 5, pp. 863–877, May 1995.

[127] J. Dai, J. Zhang, W. Zhang, and D. Grischkowsky, "Terahertz time-domain spectroscopy characterization of the far-infrared absorption and index of refraction of high-resistivity, float-zone silicon," *Journal of the Optical Society of America B*, vol. 21, no. 7, p. 1379, Jul. 2004.

[128] H. Herdian, T. Inoue, T. Hirano, M. Sogabe, A. Shirane, and K. Okada, "Dual-layer proton irradiation for creating thermally-stable high-resistivity region in si cmos substrate," in *ESSDERC 2021 - IEEE 51st European Solid-State Device Research Conference (ESSDERC)*. IEEE, Sep. 2021.

[129] R. Karim, A. Iftikhar, and R. Ramzan, "Performance-issues-mitigation-techniques for on-chip-antennas – recent developments in rf, mm-wave, and thz bands with future directions," *IEEE Access*, vol. 8, pp. 219 577–219 610, 2020.

[130] S. Kong, K. M. Shum, C. Yang, L. Gao, and C. H. Chan, "Wide impedance-bandwidth and gain-bandwidth terahertz on-chip antenna with chip-integrated dielectric resonator," *IEEE Trans. Antennas Propag.*, vol. 69, no. 8, pp. 4269–4278, Aug. 2021, doi: 10.1109/TAP.2021.3060060.

[131] E. Shaulov, S. Jameson, and E. Socher, "A Zero Bias J-Band Antenna-Coupled Detector in 65-nm CMOS," *IEEE Trans. THz Sci. Technol.*, vol. 11, no. 1, pp. 62–69, jan 2021.

[132] H. Herdian, T. Inoue, M. Sogabe, A. Shirane, and K. Okada, "A 300-GHz Band Chip-to-Waveguide Transition on Proton-Irradiated Standard 65nm CMOS Si Substrate for Flip-Chip Packaging Implementation," in *Proc. IEEE International Microwave Symposium (IMS)*. IEEE, Jun. 2022.

[133] C. Yi, K. M. Lee, H. J. Kim, and M. Kim, "WR-3.4 InP HBT Amplifier Module With Integrated Wideband Waveguide Transitions," *IEEE Microwave Wireless Compon. Lett.*, vol. 31, no. 12, pp. 1315–1318, Dec. 2021.

[134] Z. Simon He, M. Bao, Y. Li, A. Hassona, J. Campion, J. Oberhammer, and H. Zirath, "A 140 GHz Transmitter with an Integrated Chip-to-Waveguide Transition Using 130nm SiGe BiCMOS Process," in *2018 Asia-Pacific Microwave Conference (APMC)*. IEEE, Nov. 2018.

[135] F. Xie, Z. Li, C. Ding, Z. Chen, and Z.-C. Hao, "A Fully Integrated 220-GHz Transmitter and Receiver System for High-Speed Wireless Communication," in *2023 International Conference on Microwave and Millimeter Wave Technology (ICMMT)*. IEEE, May 2023.

[136] T. Yoshida, S. Hara, T. Hagino, M. H. Mubarak, A. Kasamatsu, K. Takano, Y. Sugimoto, K. Sakakibara, S. Amakawa, and M. Fujishima, "A 2D Beam-Steerable 252-285-GHz 25.8-Gbit/s CMOS Receiver Module," in *2023 IEEE Asian Solid-State Circuits Conference (A-SSCC)*. IEEE, Nov. 2023.

[137] K. Takano, K. Katayama, S. Hara, R. Dong, K. Mizuno, K. Takahashi, A. Kasamatsu, T. Yoshida, S. Amakawa, and M. Fujishima, "300-GHz CMOS transmitter module with built-in waveguide transition on a multilayered glass epoxy PCB," in *2018 IEEE Radio and Wireless Symposium (RWS)*. IEEE, Jan. 2018.

[138] R. Xu, S. Gao, B. S. Izquierdo, C. Gu, P. Reynaert, A. Standaert, G. J. Gibbons, W. Bosch, M. E. Gadringer, and D. Li, "A Review of Broadband Low-Cost and High-Gain Low-Terahertz Antennas for Wireless Communications Applications," *IEEE Access*, vol. 8, pp. 57 615–57 629, 2020.

[139] F. Xie, Z.-C. Hao, Z. Li, and Z. Chen, "A 220-GHz Perpendicular Chip-to-Waveguide Transition Using an LBE-SiGe-Based Cavity," *IEEE Microwave and Wireless Technology Letters*, vol. 33, no. 9, pp. 1266–1269, Sep. 2023.

[140] R. Pease and S. Chou, "Lithography and other patterning techniques for future electronics," *Proceedings of the IEEE*, vol. 96, no. 2, pp. 248–270, Feb. 2008.

[141] S.-K. S. Fan, M.-S. Chen, C.-Y. Hsu, and Y.-J. Park, "An artificial intelligence transformation model – pod redesign of photomasks in semiconductor manufacturing," *Journal of Industrial and Production Engineering*, vol. 41, no. 3, pp. 201–216, Nov. 2023.

[142] G. M. Rebeiz, W. Shin, F. Golcuk, O. Inac, S. Zihir, O. Gurbuz, J. Edwards, and T. Kanar, "Wafer-scale millimeter-wave phased-array rfics," in *2014 IEEE Compound Semiconductor Integrated Circuit Symposium (CSICS)*. IEEE, Oct. 2014.

Appendix A

Publication List

A.1 Journal Papers

- **Hans Herdian**, Takeshi Inoue, Atsushi Shirane, and Kenichi Okada, "Dual-Layer Proton Irradiation for Passive Component Enhancement and Noise Coupling Suppression on CMOS Process," in IEEE Transaction on Electron Device (TED), Vol. 71, No. 8, Aug. 2024.
- **Hans Herdian**, Chun Wang, Takeshi Inoue, Atsushi Shirane, and Kenichi Okada, "A Proton Irradiated CMOS On-Chip Vivaldi Antenna for 300 GHz Band Slat Array Implementation," in IEEE Open Journal of Antennas and Propagation (OJAP), Jul. 2024 (Early Access).

A.2 International Conferences

- **Hans Herdian**, Takeshi Inoue, Masatsugu Sogabe, Atsushi Shirane, and Kenichi Okada, "300-GHz Band Chip-to-Waveguide Transition on Proton-Irradiated Standard 65nm CMOS Si Substrate for Flip-Chip Packaging Implementation," IEEE/MTT-S International Microwave Symposium (IMS), Denver, CO, USA, 2022, pp. 673-675.
- **Hans Herdian**, Takeshi Inoue, Masatsugu Sogabe, Atsushi Shirane, Kenichi Okada, “Dual-Layer Proton Irradiation for Creating Thermally-Stable High-Resistivity Region in Si CMOS Substrate,” IEEE European Solid-State Device Research Conference (ESSDERC), Grenoble, France, 2021, pp. 191-194.
- **Hans Herdian**, Takeshi Inoue, Masatsugu Sogabe, Atsushi Shirane, and Kenichi Okada, "300GHz Band On-Chip Vivaldi Antenna on Dual-Layer Proton Irradiated

CMOS Si Substrate," IEEE Asia-Pacific Microwave Conference (APMC), Brisbane, Australia, 2021, pp. 440-442.

- **Hans Herdian**, Haosheng Zhang, Aravind Tharayil Narayanan, Atsushi Shirane, and Kenichi Okada, "10GHz Varactor-less VCO with Helium-3 Ion Irradiated Inductor," IEEE Asia-Pacific Microwave Conference (APMC), Singapore, 2019, pp. 63-65.

A.3 Domestic Conferences

- **Hans Herdian**, Haosheng Zhang, Atsushi Shirane, and Kenichi Okada, "Wide Tuning-Range VCO Implementation with Helium-3 Irradiated Inductor," IEICE General Conference, Kanazawa University, Kanazawa, C-12-26, Sep. 2018.

A.4 Co-Author

A.4.1 Journals and Letters

- Chun Wang, Chenxin Liu, **Hans Herdian**, Abanob Shehata, Jill Mayeda, Kazuaki Kunihiro, Hiroyuki Sakai, Atsushi Shirane, and Kenichi Okada, "A D-Band Wideband Single-Ended Neutralized Upconversion Mixer With Controlled LO Feedthrough in 65-nm CMOS," in IEEE Solid-State Circuits Letters, vol. 7, pp. 167-170, 2024.

- Chun Wang, Ibrahim Abdo, Chenxin Liu, Carrel da Gomez, Jill Mayeda, **Hans Herdian**, Wenqian Wang, Xi Fu, Dongwon You, Abanob Shehata, Sunghwan Park, Yun Wang, Jian Pang, Hiroyuki Sakai, Atsushi Shirane, and Kenichi Okada, "A Sub-THz Full-Duplex Phased-Array Transceiver With Self-Interference Cancellation and LO Feedthrough Suppression," in IEEE Journal of Solid-State Circuits, vol. 59, no. 4, pp. 978-992, April 2024.

- Dongwon You, Xiaolin Wang, **Hans Herdian**, Xi Fu, Hojun Lee, Michihiro Ide, Carrel Da Gomez, Zheng Li, Jill Mayeda, Daisuke Awaji, Jian Pang, Hiraku Sakamoto, Kenichi Okada, and Atsushi Shirane, "A Ka-Band Deployable Active Phased Array Transmitter Fabricated on 4-Layer Liquid Crystal Polymer Substrate for Small-Satellite Mount," in IEEE Access, vol. 11, pp. 69522-69535, 2023.

- Dongwon You, Xi Fu, **Hans Herdian**, Xiaolin Wang, Yasuto Narukiyo, Ashbir Aviat Fadila, Hojun Lee, Michihiro Ide, Sena Kato, Zheng Li, Yun Wang, Daisuke

Awaji, Jian Pang, Hiraku Sakamoto, Kenichi Okada, and Atsushi Shirane, "A Ka-Band 64-Element Deployable Active Phased-Array TX on a Flexible Hetero Segmented Liquid Crystal Polymer for Small Satellites," in IEEE Microwave and Wireless Technology Letters, vol. 33, no. 6, pp. 903-906, June 2023.

- Junjun Qiu, Zheng Sun, Bangan Liu, Wenqian Wang, Dingxin Xu, **Hans Herdian**, Hongye Huang, Yuncheng Zhang, Yun Wang, Jian Pang, Hanli Liu, Masaya Miyahara, Atsushi Shirane, and Kenichi Okada, "A 32-kHz-Reference 2.4-GHz Fractional-N Oversampling PLL With 200-kHz Loop Bandwidth," in IEEE Journal of Solid-State Circuits, vol. 56, no. 12, pp. 3741-3755, Dec. 2021.

- Haosheng Zhang, **Hans Herdian**, Aravind Tharayil Narayanan, Atsushi Shirane, Mitsuru Suzuki, Kazuhiro Harasaka, Kazuhiko Adachi, Shigeyoshi Goka, Shinya Yanagimachi, and Kenichi Okada, "ULPAC: A Miniaturized Ultralow-Power Atomic Clock," in IEEE Journal of Solid-State Circuits, vol. 54, no. 11, pp. 3135-3148, Nov. 2019.

- Haosheng Zhang, Aravind Tharayil Narayanan, **Hans Herdian**, Bangan Liu, Rui Wu, Atsushi Shirane, and Kenichi Okada, "A power-efficient pulse-VCO for chip-scale atomic clock," IEICE Transaction on Electronics, vol. E102-C, no. 4, pp.276-286, Apr. 2019.

A.4.2 Conferences

- Chun Wang, **Hans Herdian**, Wenbin Zheng, Chenxin Liu, Jill Mayeda, Yuxuan Liu, Olivia Angel Yong, Wenqian Wang, Yuncheng Zhang, Carrel Da Gomez, Abanob Shehata, Sena Kato, Ibrahim Abdo, Teruo Jyo, Hiroshi Hamada, Hiroyuki Takahashi, Hiroyuki Sakai, Atsushi Shirane, and Kenichi Okada, "A 236-to-266GHz 4-Element Amplifier-Last Phased-Array Transmitter in 65nm CMOS," IEEE International Solid-State Circuits Conference (ISSCC), San Francisco, CA, USA, 2024, pp. 415-417.

- Chun Wang, Ibrahim Abdo, Chenxin Liu, Carrel Da Gomez, **Hans Herdian**, Wenqian Wang, Xi Fu, Dongwon You, Abanob Shehata, Sunghwan Park, Yun Wang, Jian Pang, Hiroyuki Sakai, Atsushi Shirane, and Kenichi Okada, "A Sub-THz Full-Duplex Phased-Array Transceiver with Self-Interference Cancellation and LO Feedthrough Suppression," IEEE Symposium on VLSI Technology and Circuits (VLSI Technology and Circuits), Kyoto, Japan, 2023, pp. 1-2.

- Dongwon You, Xi Fu, Xiaolin Wang, Yuan Gao, Wenqian Wang, Jun Sakamaki, **Hans Herdian**, Sena Kato, Michihiro Ide, Yuncheng Zhang, Ashbir Aviat Fadila, Zheng Li, Chun Wang, Yun Wang, Jumpei Sudo, Makoto Higaki, Nahoka Kawaguchi, Masaya Nitta, Soichiro Inoue, Takashi Eishima, Takashi Tomura, Jian Pang, Hiroyuki Sakai, Kenichi Okada, and Atsushi Shirane, "A Small-Satellite-Mounted 256-Element Ka-Band CMOS Phased-Array Transmitter Achieving 63.8dBm EIRP Under 26.6W Power Consumption Using Single/Dual Circular Polarization Active Coupler," IEEE International Solid-State Circuits Conference (ISSCC), San Francisco, CA, USA, 2023, pp. 298-300.

- Dongwon You, Yun Wang, Xi Fu, **Hans Herdian**, Xiaolin Wang, Ashbir Fadila, Hojun Lee, Michihiro Ide, Sena Kato, Zheng Li, Jian Pang, Atsushi Shirane, and Kenichi Okada, "A Ka- Band Dual Circularly Polarized CMOS Transmitter with Adaptive Scan Impedance Tuner and Active XPD Calibration Technique for Satellite Terminal," IEEE Radio Frequency Integrated Circuits Symposium (RFIC), Denver, CO, USA, 2022, pp. 15-18.

- Junjun Qiu, Zheng Sun, Bangan Liu, Wenqian Wang, Dingxin Xu, **Hans Herdian**, Hongye Huang, Yuncheng Zhang, Yun Wang, Atsushi Shirane, and Kenichi Okada, "A 32kHz-Reference 2.4GHz Fractional-N Oversampling PLL with 200kHz Loop Bandwidth," IEEE International Solid-State Circuits Conference (ISSCC), San Francisco, CA, USA, 2021, pp. 454-456.

- Haosheng Zhang, Aravind Tharayil Narayanan, **Hans Herdian**, Bangan Liu, Yun Wang, Atsushi Shirane, and Kenichi Okada, "0.2mW 70Fsrms-Jitter Injection-Locked PLL Using De-Sensitized SSPD-Based Injecting-Time Self-Alignment Achieving -270dB FoM and -66dBc Reference Spur," IEEE Symposium on VLSI Circuits, Kyoto, Japan, 2019, pp. C38-C39.

- Haosheng Zhang, **Hans Herdian**, Aravind Tharayil Narayanan, Atsushi Shirane, Mitsuru Suzuki, Kazuhiro Harasaka, Kazuhiko Adachi, Shinya Yanagimachi, and Kenichi Okada, "Ultra-Low-Power Atomic Clock for Satellite Constellation with 2.2×10^{-12} Long-Term Allan Deviation Using Cesium Coherent Population Trapping," IEEE International Solid-State Circuits Conference (ISSCC), San Francisco, CA, USA, 2019, pp. 462-464.

- Haosheng Zhang, **Hans Herdian**, Aravind Tharayil Narayanan, Bangan Liu, Rui Wu, Atsushi Shirane, and Kenichi Okada, "A -194 dBc/Hz FoM VCO with Low-Supply Sensitivity for Ultra-Low-Power Atomic Clock," Asia-Pacific Microwave Conference (APMC), Kyoto, Japan, 2018, pp. 788-790.