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著者(和文)	XUDingxin
Author(English)	Dingxin Xu
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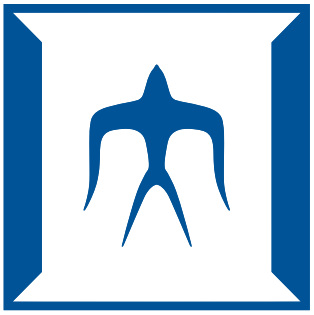

A Study of Fractional Spur Suppression Techniques in Digital Phase-Locked Loops

by

Dingxin Xu

A Ph. D. dissertation submitted in partial fullfillment of the requirements for the degree of

Doctor of Philosophy

in

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in the

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of

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Supervised by

Prof. Kenichi Okada

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To my family,

Acknowledgment

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Abstract

Due to the ease of integration with digital baseband (BB), digital PLL (DPLL) is a strong candidate for the local oscillator (LO) in modern wireless communication and FMCW radar systems. Conventional DPLLs employ digital-to-time converters (DTCs) to cancel the quantization noise (QN) from the delta-sigma modulator, which is used to achieve the fractional frequency resolution. However, the nonlinearities from the DTCs will cause fractional spurs at the DPLL output, leading to either polluted error-vector magnitude (EVM) or degraded range/velocity accuracies. To mitigate the fractional spur problem in DPLLs, several techniques are presented in this thesis, including: a) a dual-fractional-N cascaded PLL technique and that can push the fractional spurs to out-of-band; b) a digital pre-distortion (DPD) and dither-free DPLL with a cascaded fractional divider and pseudo-differential DTCs that can achieve low fractional spur without the degradation of in-band phase noise or PLL locking time; c) a differential voltage-domain QN cancellation technique that is resilient to the nonlinearity degradation caused by supply ripples; d) a voltage-controlled oscillator topology (VCO) that can achieve robust flicker noise suppression against the low-quality-factor decoupling network, enabling a narrow-bandwidth PLL operation for further fractional spur suppressions.

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Chapter 1

Introduction

Radio wave is the most important building block in modern human society for its wide usage in communication applications. The first generation (1G) of wireless cellular technology, pioneered by Bell Labs in the 1980s, offered a maximum data rate of 2.4 Kbps. With such limited bandwidth, only phone calls and text messages were possible with 1G technology. Driven by the demand for applications with larger data volume and shorter data transfer latency, wireless communication standards nowadays (*e.g.,* 5G-Advanced, IEEE 802.11be) can support data rate more than 1 Gbps, an over millionfold increase in the past few decades.

Fig. 1.1 shows the block diagram of a typical wireless communication system, where the digital data generated by the BB from the transmitter (TX) side is converted to analog signal by a digital-to-analog converter (DAC). The frequency of the DAC output is at intermediate frequency (IF), which will be mixed with a high frequency signal generated by the LO to generate the RF signal. The RF signal will then be amplified by the power amplifier (PA) before being transmitted into the air. On the receiver (RX) side, the electromagnetic (EM) wave captured by the antenna will be amplified by a low-noise amplifier (LNA) so that the attenuated RF signal power can be recovered. The LNA output is down-converted to IF frequency in order to be sampled by the analog-to-digital converter (ADC). In the end, the data will be processed by the RX BB to complete the communication.

Another significant application of radio waves is radar system, which is extensively employed for weather monitoring, traffic control, remote sensing, *etc.* Recently, the FMCW radar technique has been attracting considerable research interest due to its potential in automotive applications.

Fig. 1.2 shows the block diagram of a typical FMCW radar system. An LO is required to generate a frequency chirp, which will then be amplified by the PA and transmitted

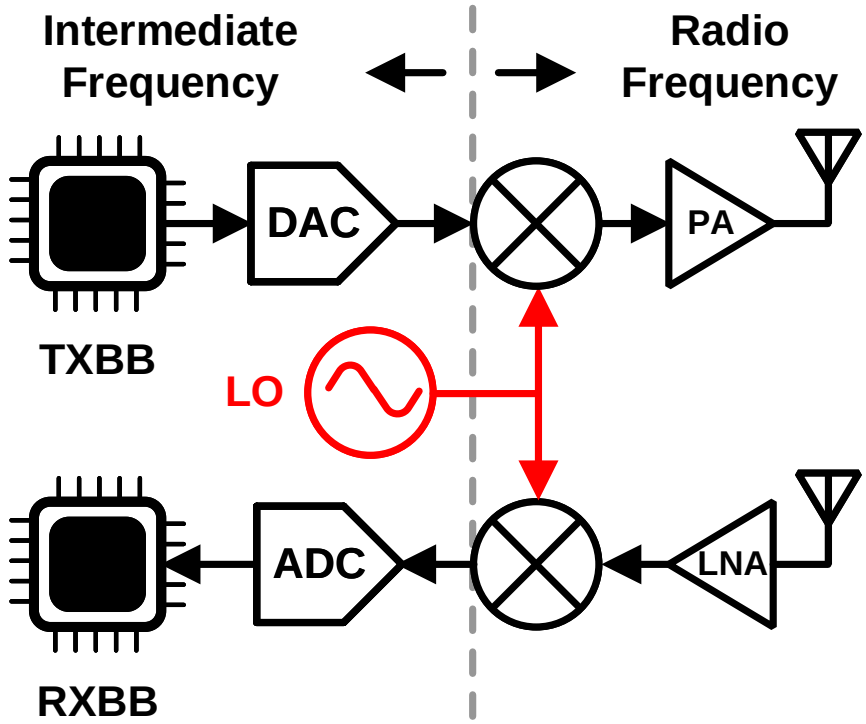


Figure 1.1: Typical wireless communication system.

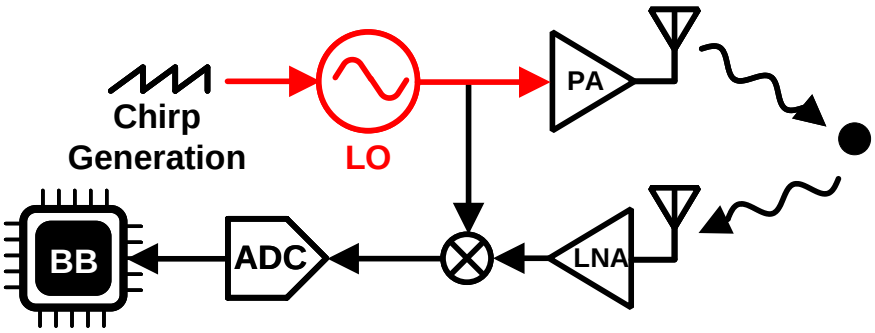


Figure 1.2: Typical FMCW system.

into the air by the TX antenna. When the EM wave encounters the target object, it will be reflected and captured by the RX antenna. Depending on the distance between the TRX and the target object, the instantaneous frequency of the TX and RX chirp will be different. When being mixed by the RX mixer the frequency difference can be sampled by the ADC. A range fast Fourier transform (FFT) will be finished at the BB to derive the distance from the ADC output.

1.1 PLLs in Wireless Communication and FMCW Radar Systems

The two systems mentioned above have many similarities. Notably, both require an LO to perform frequency conversion or frequency modulation. In practical designs, the LO is usually implemented as a PLL.

1.1.1 Integer-*N* PLLs

A PLL is a negative feedback system where a clean and low-frequency reference siganl (usually from a crystal oscillator, XO) is used to calibrate the phase (and thus frequency) of a high-frequency VCO. Fig. 1.3 shows the block diagram of a simple integer-*N* analog PLL (APLL). The VCO frequency is fed into a multi-modulus divider (MMD) to generate a feedback signal (CK_{fb}). The division ratio (r_{div}) is controlled by the frequency control word (FCW), such that the frequency of CK_{fb} is close to the frequency of the reference signal denoted by CK_{ref}. The phase difference (ε_{pd}) between CK_{ref} and CK_{fb} is compared by the phase detector (PD), which will then generate positive or negative voltage pulses according to the ε_{pd}. Those voltage pulses will be passed through a R-C loop filter (LF) to generate the control voltage (V_{ctrl}) for the VCO. As implied by its name, the FCW in an integer-*N* PLL can only be integer numbers, *i.e.,* the VCO frequency can only be integer multiples of the reference frequency.

The linearized model of the integer-*N* PLL is shown in Fig. 1.4, where the reference noise is denoted as n_{ref}, the VCO noise is denoted as n_{vco}, the PD gain is represented by K_{pd}, the LF transfer function is denoted by *H(s)*. The noise transfer functions (NTFs) for the reference noise and the VCO noise can be derived as Eq. (1.1, 1.2), where the open-loop transfer function $H_{ol}(s)$ is defined in Eq. (1.3). It can be observed that the reference noise is low-pass filtered by the PLL, and the VCO noise is high-pass filtered by the PLL. To achieve the optimum output PN performance, the bandwidth of the LF is usually controlled to balance the noise contributions from the reference and the VCO.

$$NTF_{ref}(s) = \frac{K_{\mathrm{pd}} H(s) K_{vco}/s}{1 + H_{ol}(s)} \tag{1.1}$$

$$NTF_{vco}(s) = \frac{1}{1 + H_{ol}(s)} \tag{1.2}$$

$$H_{ol}(s) = \frac{K_{pd} K_{vco} H(s)}{sN} \tag{1.3}$$

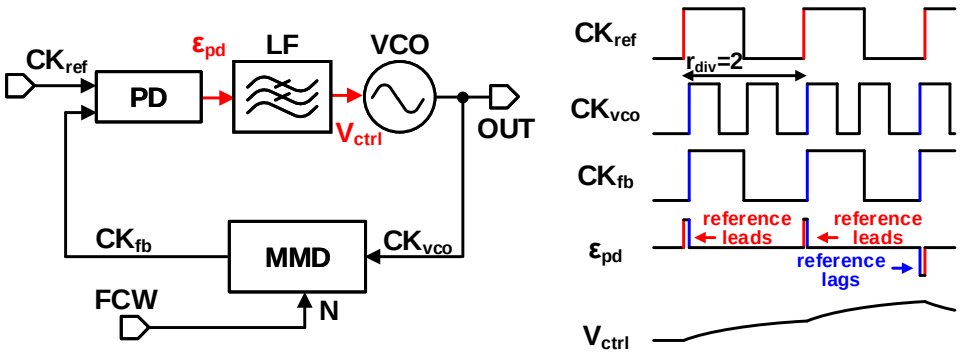


Figure 1.3: Typical integer-*N* analog PLL.

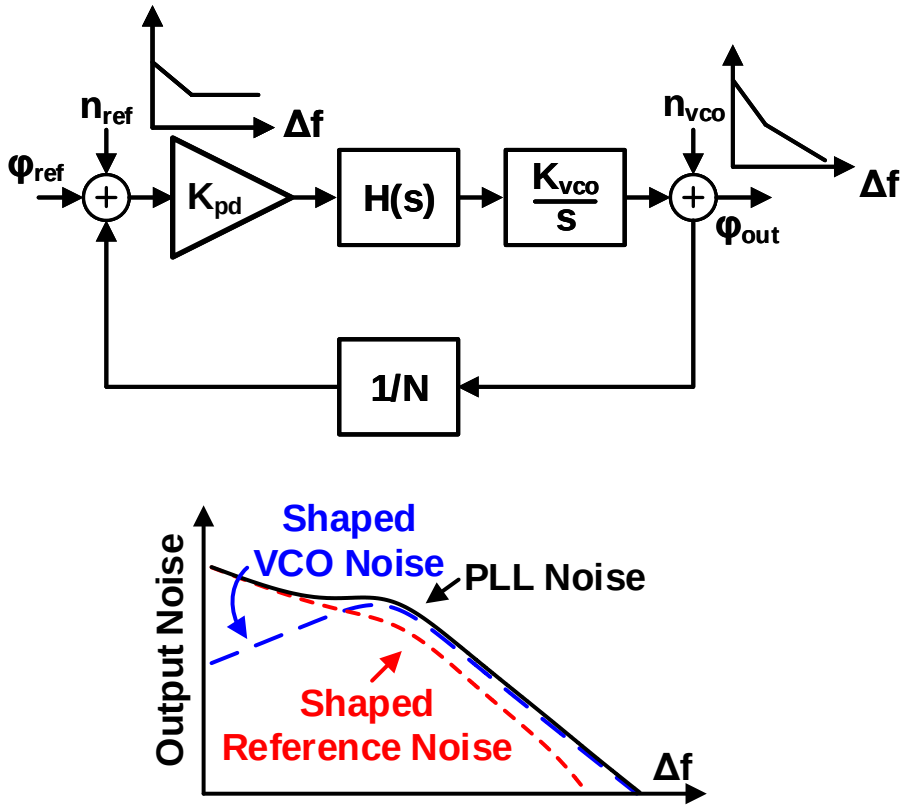


Figure 1.4: Noise model and output PN spectrum of an integer-*N* PLL.

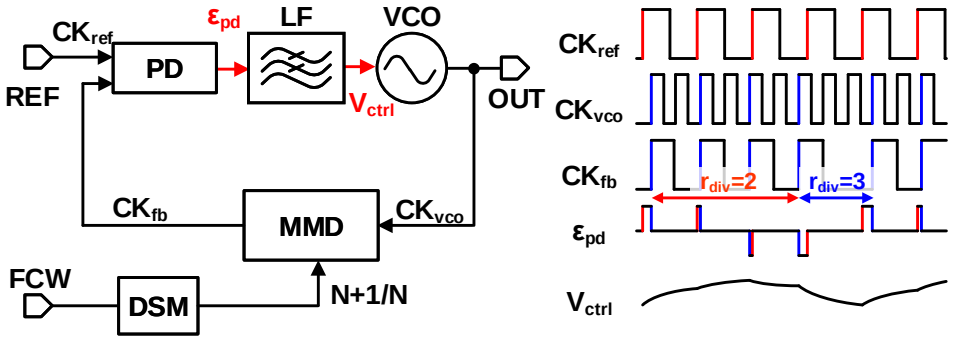


Figure 1.5: Typical fractional-N analog PLL.

1.1.2 Fractional-N PLLs

The frequencies of the typical commercial XOs usually range from several kHz to several hundred of MHz. However in modern wireless communication systems, a frequency resolution of even lower than 1 kHz is sometimes required, limiting the application of a simple integer-N PLL in those scenarios. As a result, a fractional-N PLL is needed to achieve a lower frequency resolution.

Fig. 1.5 shows the schematic of a fractional-N PLL, in which r_{div} is dynamically controlled by a delta-sigma modulator (DSM). Denote the integer part of the FCW by N, and the fractional part of the FCW by α, r_{div} will toggle between N and $N+1$. In this way, an on-average frequency multiplication ratio of $N+\alpha$ can be achieved. Because the r_{div} is never equal to $N+\alpha$ in a fractional-N PLL, the quantization noise (QN) will be injected into the loop. As depicted in Fig. 1.6, because the DSM QN is low-pass filtered by the PLL, the bandwidth of LF should be adjusted lower to balance the in-band and out-of-band PN, leading to a degraded jitter performance. Moreover, the ε_{pd} faced by the PD varies in a wider range, which will induce stronger nonlinearities from the PD and thus fractional spurs. With a reference frequency of f_{ref}, the fractional spurs will appear at the harmonics of αf_{ref}. When a near-integer channel (*i.e.,* when α is close to 0 or 1) is synthesized, the fractional-N spurs will be located in-band and thus cannot be filtered by the loop, causing extra degradation in the PLL PN.

1.2 The Demand for Low-Noise and Low-Spur PLLs

According to the famous Shannon-Hartley theorem, which is shown in Eq. (1.4), the channel capacity (C) is directly related to the channel bandwidth (BW) and the signal-to-

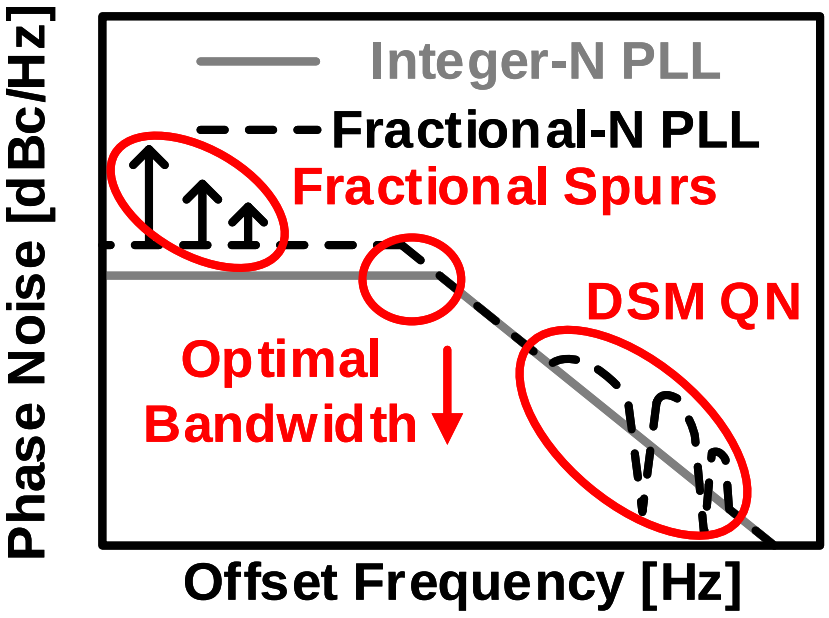


Figure 1.6: Phase noise comparison of integer-*N* and fractional-*N* PLLs.

noise ratio (SNR) of the TRX chain. In order to maximize C, the noise generated inside the TRX chain should be minimized. As shown in Fig. 1.7, when a fractional-*N* PLL is employed in a TX, the PN of the PLL will directly pollute the EVM, the fractional spurs will be mixed with neighboring channels, leading to inter-channel interference. On the other hand, when a fractional-*N* PLL is employed in an FMCW radar system, the fractional spurs will appear in the result of range FFT. As depicted in Fig. 1.8, the difference between the fractional spurs and the target object becomes indistinguishable, leading to a degraded distance and velocity resolution.

$$C = BW log_2(1 + S/N) \tag{1.4}$$

Moreover, PLL is not the only block contributing to the SNR degradation. The high-power PAs that are needed for ensuring long communication distance are always not linear, which will deteriorate the EVM in a TX. The noise from LNA will also directly degrade the SNR at the RX side. The integrated PN (IPN) of the PLL is thus often required to be even lower in order to leave enough margin for system design considerations.

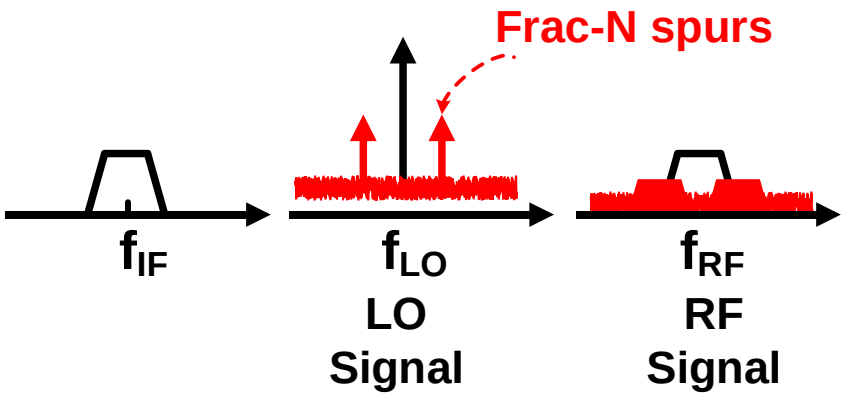


Figure 1.7: The spectrum of transmitted signal polluted by PLL PN and fractional spurs.

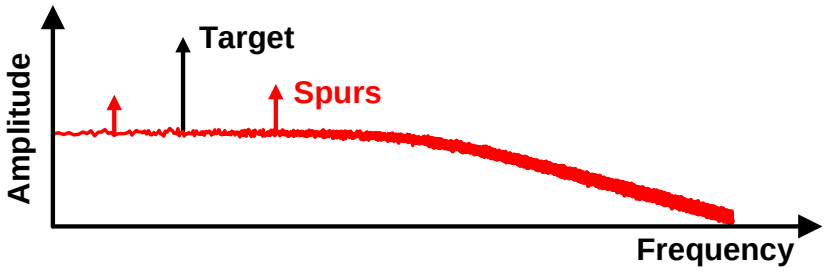


Figure 1.8: The range FFT result polluted by fractional spurs.

For example, an IPN of less than -36 dBc is usually required for 256 quadrature amplitude modulation (QAM). For this reason, the PN and spur performance needs to be improved in modern PLLs.

1.3 The Need of Digital PLLs

In addition to the above-disucssed PN and spur power requirement, the PLLs are often required to be integrated with other block circuits such as BB, PA, and LNA in a system-on-a-chip (SoC). In order to improve the performance of BB, which is necessary for processing larger amount of data, advanced process nodes are preferred. During the past one decade, commercial SoCs have transitioned from planar CMOS process nodes to FinFET process nodes. As the transistors become faster, the cost of the chips also in-

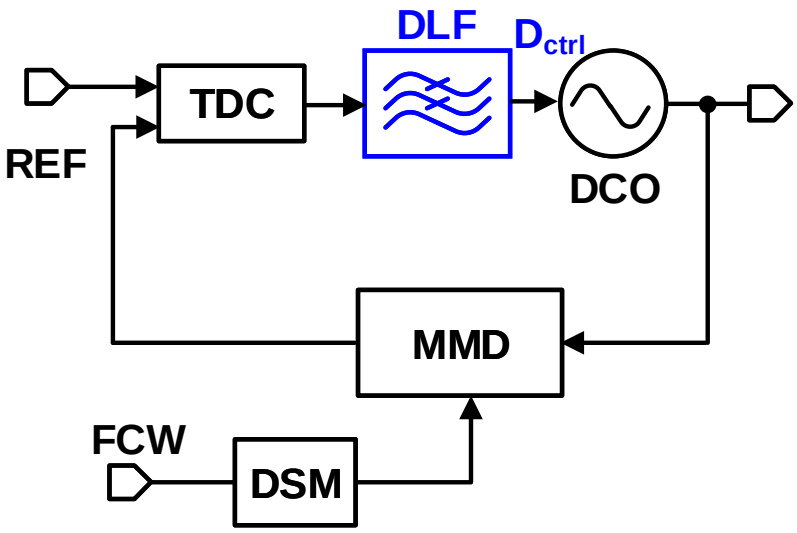


Figure 1.9: Typical TDC-based DPLL.

creases rapidly. However, the RC filter size of the APLL doesnot scale down with the process as quickly as the digital BB, which causes even higher chip cost.

Driven by the need for smaller area overhead, DPLL is now a strong candidate for SoCs on recent advanced process nodes. The block diagram of a typical DPLL is shown in Fig. 1.9, in which the analog PD is replaced with a time-to-digital converter (TDC) [1]. The TDC will convert the phase error information into digital codes, which can be easily processed by a digital LF (DLF). The output of the DLF, D_{ctrl} will adjust the frequency of a digitally controlled oscillator (DCO) so that the phase difference between the reference and feedback can be minimized. Due to the elimination of the bulky RC filter, the area of a DPLL can be much smaller. Recent DPLL in 5 nm FinFET can be implemented within only 0.0036 mm^2 [2]. Meanwhile, because of the adoption of DLFs, frequency modulations can be easily implemented in DPLLs. This is another reason that makes DPLLs popular in wireless communication and FMCW radar systems [3–8].

To fully take advantage of digitizing the PLL, several challenges should be addressed. First of all, the resolution of a TDC is limited by the minimum gate delay that can be achieved on a specific process. As shown in Fig. 1.10, when a TDC is used to sample the input time difference, quantization error (QE) will be generated according to the input. Those quantization error will degrade the in-band PN, and thus the final performance of the TRX. In the scenario where the DPLL is required to work in fractional-N mode, the input range of the TDC becomes dependent on the order of the DSM. Higher DSM order

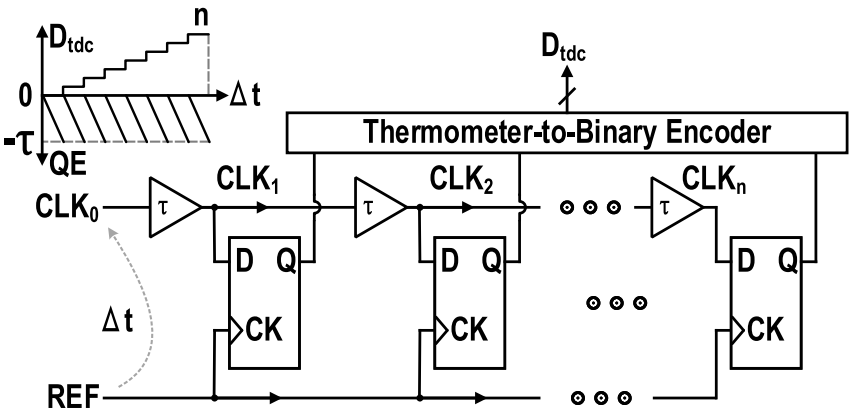


Figure 1.10: Schematic of a flash-TDC.

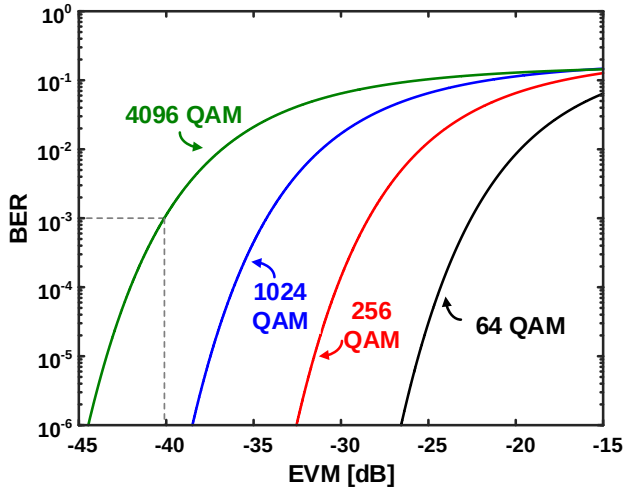


Figure 1.11: EVM v.s. BER for different QAM modulations.

is usually preferred to suppress the DSM QN, which causes a larger TDC input range. In this case, the nonlinearities from the TDC, which is usually dominated by the mismatch between the delay line elements, will elevate the the power of fractional spurs. Moreover, the QE of the TDC also becomes periodical, which modulates the frequency of the DCO and lead to further fractional spur degradation.

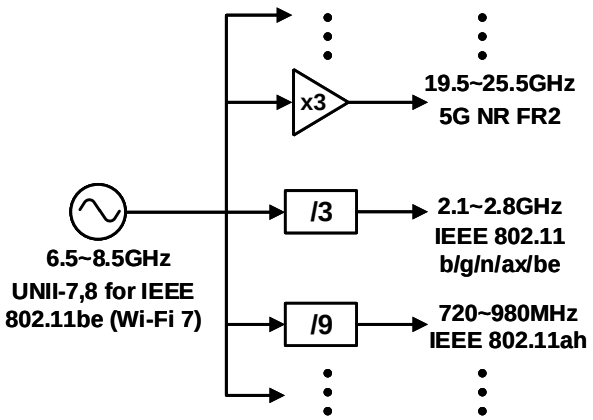


Figure 1.12: Frequency plan for supporting multiple wireless communication standards.

1.4 Thesis Objective and Organization

In order to improve the data rate in wireless communications, high-order QAMs are applied in recent wireless communication standards. For example, 256-QAM is required for 5G-Advanced, 4096 QAM is adopted in IEEE 802.11be (WiFi-7). The need of higher-order QAMs, in turn, becomes the need of extremely low EVM for the TRX. As shown in Fig. 1.11, less than -40 dB EVM is required for 4096-QAM with less than 0.1% bit-error-rate (BER) [9]. Some recent commercial TRXs for WiFI-7 can even achieve less than -42 dB EVM [10, 11]. The target DPLL frequency is 6.5-to-8 GHz, for the best available Q factor of on-chip inductors and the flexibility to cover multiple frequency bands for different communication standards. Figure 1.12 shows the conceptual frequency plan based on the proposed PLL, where frequency dividers or multipliers are used to cover frequencies from sub-GHz bands to milimeter-wave bands.

In a practical TRX design, the nonlinearities from PA can contribute to a significant amount of EVM of the whole TRX chain. In order to leave enough margin for the PA design, the IPN from PLLs should be far less than -40 dBc for a 4096-QAM. To this aim, the target DPLL IPN of this thesis is defined as -46 dBc. On the other hand, the IPN of DPLL is typically limited by the reference noise and DCO phase noise. Low-phase-noise and high-frequency XOs are highly desired for achieving low IPN. However, it will also significantly increase the overall fabrication cost and thus cannot always be utilized. On the other hand, DCO phase noise is usually limited by the maximum allowed voltage swings at a specific process, which is also hard to be further improved [12]. In order to leave enough margin for the IPN degradation from less-clean XOs and DCOs, the target

worst-case fractional spur power is defined as -60 dBc, which is equivalent to 4% of the overall -46 dBc IPN. Both new PLL topologies and new building block circuit designs are required to achieve these stringent specifications on IPN and fractional spur level, which will be introduced in detail throughout the rest of thesis. The thesis organization is shown in Fig. 1.13, in which 5 more chapters are included:

Chapter 2 provides an overview of recent low-phase-noise and low-spur DPLL design techniques. The operation of DTC-based DPLLs is introduced in detail in this chapter, which is the key to mitigate the DSM QN and thus is important for the phase noise improvement in modern DPLLs. Techniques that are usually exploitted to mitigate the nonlinearities of DTCs are also introduced, including dithering techniques and DPD techniques.

Chapter 3 introduces a 6.5-to-8 GHz cascaded dual-fractional-N DPLL designed to mitigate fractional spur degradation in near-integer channels. This is accomplished by employing two PLLs with carefully selected fractional FCWs to optimize fractional spur performance at the output. Additionally, the design includes a 14-bit segmented DTC with background nonlinearity calibration, achieving a 0.05% integral nonlinearity (INL) to further suppress fractional spurs. This PLL achieves an integrated jitter of 154.4 fs in integer-N mode and 190.8 fs in fractional-N mode, consuming 14.2 mW of power with a 50 MHz reference, resulting in a figure of merit (FoM) of -242.9 dB. The fractional spur at the near-integer channel is as low as -63.7 dBc, and the reference spur is -72.4 dBc. This PLL is fabricated using a 65-nm CMOS process, occupying a core area of 0.48 mm^2. Related works has been presented in [13].

Chapter 4 introduces a 7 GHz fractional-N DPLL that functions without any DPD for the DTC INL or the use of dither. By employing a cascaded fractional divider, the fractional spur offset frequency is shifted beyond the PLL loop bandwidth, which results in less fractional spur degradation in near-integer channels. Additionally, a pseudo-differential DTC (PD-DTC) technique is used to cancel even-symmetric nonlinearity components, thereby achieving better fractional spur suppression. Thanks to these two techniques, the PLL achieves a worst-case fractional spur of -62.1 dBc without degrading the in-band PLL PN or PLL locking time. Implemented in a 65-nm CMOS process and occupying an area of 0.23 mm^2, this PLL achieves an integrated jitter of 143.7 fs with a 100 MHz reference frequency and 8.89 mW power consumption, resulting in a figure of merit (FoM) of -247.4 dB. Related works has been presented in [14].

Chapter 5 introduces a low-flicker-noise VCO (DCO) topology that can be readily integrated to the PLLs presented in chapter 3 and chapter 4. Thanks to the low-flicker-noise characteristic, the PLL loop bandwidth is allowed to become lower, which can benefit in further fractional spur suppression in the above-mentioned PLL techniques. The VCO has

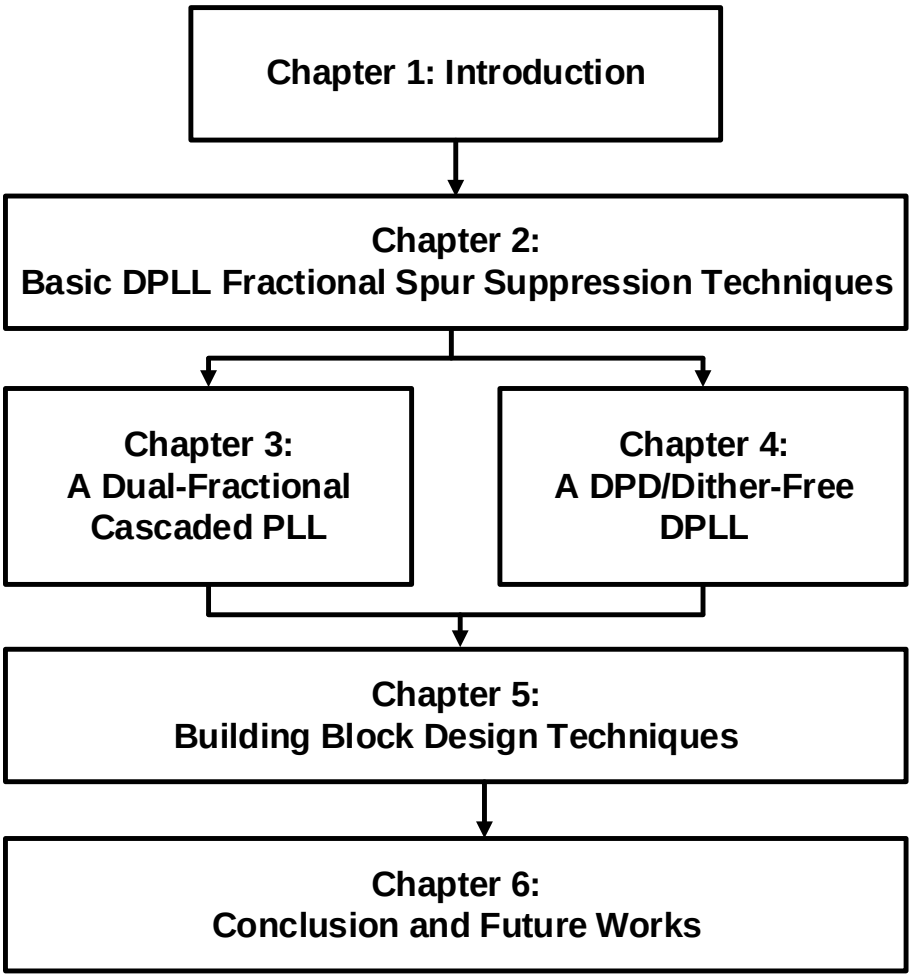


Figure 1.13: The organization of this thesis.

been presented in [15]. A novel DSM QN cancellation technique is also presented in this chapter. Different from conventional DTC-based DSM QN cancellation technique, the proposed DSM QN cancellation technique is in voltage domain. Similar to the PD-DTC technique in chapter 4, the proposed voltage domain QN cancellation technique suffers less from the even-symmetric nonlinearity components. Moreover, the disturbances from a nonideal power supply can also be partially mitigated by the presented technique, which can ensure an improved fractional spur performance compared to DTC-based PLLs.

Conclusions to the techniques introduced in chapter 3, 4, and 5 are drawn in the final chapter. The remaining works that need to be finished in the future are also presented in this chapter.

Chapter 2

DTC-Based DPLLs and Fraction Spur Suppression Techniques

As discussed in chapter 1, the TDC in conventional DPLLs contributes to in-band PN degradation and fractional spurs. One key observation can be made from Fig. 1.10: the TDC QE is closely related to the input range, *i.e.,* if the TDC input range can be reduced, the noise penalty from the TDC QE can also be suppressed. To this aim, a DTC can be implemented in the DPLL to cancel out the DSM QN from MMD, so that the input range of the TDC in a fractional-N DPLL can be almost the same with that in an integer-N DPLL [4].

2.1 Operation of DTC-based DPLLs

The schematic of a basic DTC-based DPLL is depicted in Fig. 2.1. In this PLL, the MMD is assumed to be driven by a first order DSM, which can be implemented as a simple digital accumulator. The DSM QN increases by the fractional part of the FCW in each reference cycle until it reaches 1, after which the integer part of the QN will be wrapped to 0, and r_{div} becomes $N + 1$ in the corresponding cycle. The DSM QN creates a periodical pattern (ε_{qn}) at the TDC input, with an amplitude of one DCO period (T_{dco}). In order to cancel the DSM QN, the reference can be dynamically delayed, which is achieved by a DTC. The simplest DTC can be implemented as a inverter with digitally controlled load capacitors, as shown in Fig. 2.2. In this DTC, longer DTC delay τ_{dtc} can be obtained by turning on more elements in the capacitor bank. Because the charging slope of the DTC in Fig. 2.2 is different according to the wanted τ_{dtc}, it is also named as *variable-slope DTC* (VS-DTC).

The DTC delay range is expected to be able to cover exactly one T_{dco}, so that ε_{qn} can

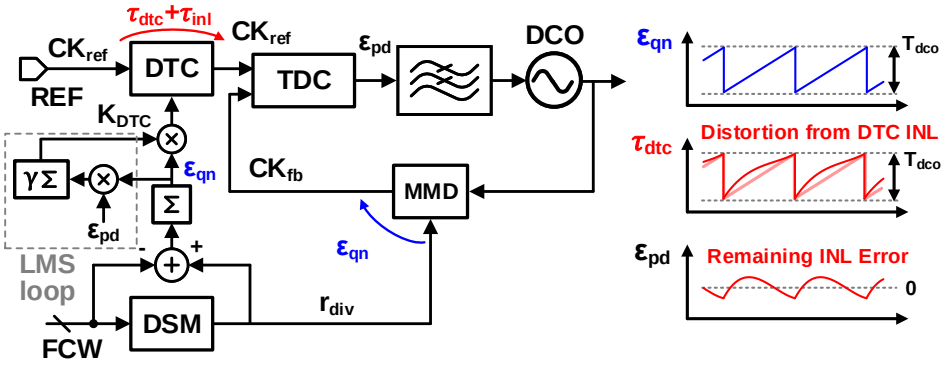


Figure 2.1: Schematic of a DTC-based PLL.

be completely canceled. Fig. 2.3 shows the simulated DPLL PN at a fractional channel before and after turning on the DTC to cancel the DSM QN. A 1-bit TDC, *i.e.*, a bang-bang PD (BBPD) is utilized in the simulation, of which the QE is heavily degraded due to the existance of DSM QN. Note that the gain of BBPD is inversely related to the input phase error range, the DPLL bandwidth thus becomes narrower [16]. Meanwhile, strong fractional spurs appear at the PN spectrum, leading to severe IPN degradation. It is shown in the blue curve that the DSM QN is perfectly removed thanks to the utilization of an ideal DTC. The BBPD input range in this case is dominated by the reference and DCO noise, leading to less degradation on its QE. Moreover, no fractional spurs appear at the PLL output, indicating a better overall IPN.

Nevertheless, due to the process-voltage-temperature (PVT) variation, the DTC delay range always deviates from the ideal value. In that case, the DSM QN can only be partially canceled, generating a QN residue that will still be detected by the TDC. As a result, the PLL PN will be degraded again, and so will the fractional spurs. To mitigate this problem, the DTC delay range needs to be calibrated. As shown in Fig. 2.4, when the DTC gain (K_{dtc}) is lower than the target value, the TDC output becomes positive when ε_{qn} is larger than 0, and negative when ε_{qn} is smaller than 0. Similarly, the sign of TDC output becomes opposite to the sign of ε_{qn} when K_{dtc} is larger than the target value. The correlation thus can be found between the K_{dtc} error and the TDC output, *i.e.,* if the product of $\varepsilon_{qn}\cdot\varepsilon_{pd}$ is positive, the K_{dtc} should be tuned larger, and vice versa. When K_{dtc} gets closer to the target value, the noise from the PLL may also start to affect the polarity of $\varepsilon_{qn}\cdot\varepsilon_{pd}$. Because the noise is generally uncorrelated with K_{dtc}, its effect on the calibration accuracy can be easily eliminated by a moving average operation of $\varepsilon_{qn}\cdot\varepsilon_{pd}$, which can be implemented as a digital accumulator. The calibration technique described in this

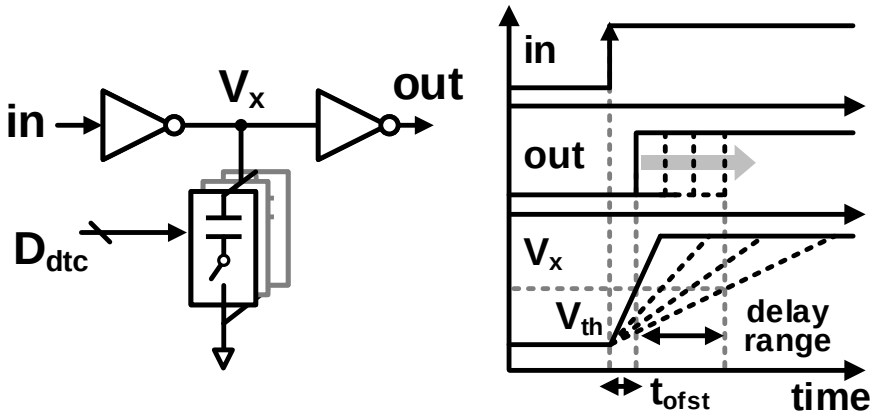


Figure 2.2: Schematic and operation of a variable-slope DTC.

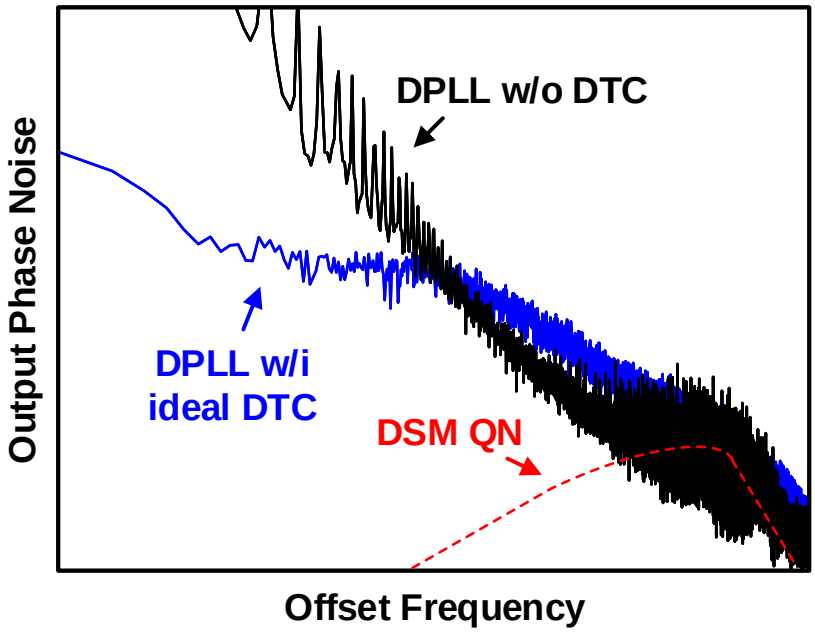


Figure 2.3: Fractional-*N* Bang-Bang DPLL spectrum with and without a DTC.

paragraph is called *least-mean-square* (LMS) algorithm, which can be easily extended for calibrating other nonideal characteristics.

Since the LMS algorithm also relies on negative feedback, it may compete with the

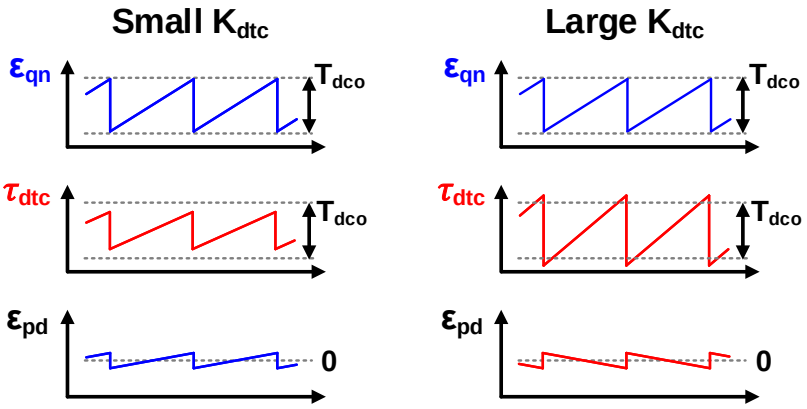


Figure 2.4: The effect of nonideal DTC gain.

PLL. When implementing DTC gain calibration, the loop gain is usually set small such that the DTC gain calibration loop bandwidth can be much narrower than the PLL loop bandwidth. Despite the competition from the PLL, the convergence speed of DTC gain calibration also depends on the FCW. When the FCW is close to an integer number, the period of the DSM QN pattern becomes long, which in turn causes slower DTC gain convergence speed and sometimes even convergence failure. To avoid this problem, higher order DSM such as multi-stage noise shaping (MASH) can be employed to generate a more random QN pattern. Fig. 2.5 shows the simulated DTC gain calibration convergence with different DSM orders at a near-integer channel. In the simulations, the only difference is the DSM order, and a near-integer cahnnel is selected. With the reference frequency of 100 MHz, it takes roughly 8 ms for the DTC gain calibration to converge when a first order DSM is employed, corresponding to 800k reference cycles. On the other hand, the convergence can finish within 1 ms when a second order DSM is employed, corresponding to an eight-fold improvement. convergence can be accelerated with the aid of a second order DSM.

Although K_{dtc} can be calibrated with sufficient accuracy to completely cancel the DSM QN. The code-to-delay conversion in the DTC is always not linear. For the VS-DTC shown in Fig. 2.2, the delay of the second inverter is sensitive to the charging slope at its input. This slope-to-delay relationship was extensively studied in the end of the last century, which is driven by the need for high-accuracy standard cell delay models [17]. According to those models, the inverter delay shows a polynomial dependence on the input slope. Since the charging slope is determined by the capacitance from the capacitor bank, which varies according to the digital control codes, this slope-dependent delay man-

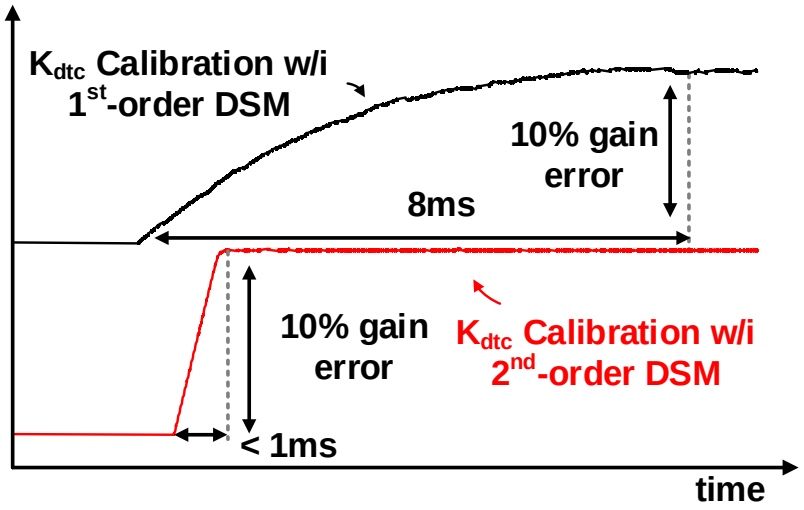


Figure 2.5: The convergence of DTC gain calibration with different DSMs.

ifests as nonlinearities in VS-DTCs. Those DTC delay nonlinearities (τ_{inl}) will appear at the TDC output, modulate the DCO frequency, and eventually limit the fractional spur performance of a DTC-based DPLL. Fig. 2.6 shows the PN spectrum of a DPLL with the nonlinearities form the DTC. Compared to the spectrum shown in Fig. 2.3, one fractional spur appears in-band, and the DSM QN residue appears out-of-band. It worth mentioning that the shape of DTC INL is usually complicated, and DTC is not the only block circuit that exhibits nonlinearity. In a real DPLL, the harmonics of fractional spur might also appear at the ouput spectrum.

2.2 Linear DTC Topologies

2.2.1 Constant-Slope DTC

To achieve lower fractional spur and phase noise, the issues caused by DTC nonlinearities must be addressed. One possible solution is to implement DTC topologies with higher linearities. Recall from the previous section that the nonlinearities in a VS-DTC arises from the slope-dependent second inverter delay, potentially higher linearity can be achieved by trying to decouple τ_{dtc} from the charging slope.

Following this idea, *constant-slope DTC* (CS-DTC) is developed [18]. Fig. 2.7 shows the schematic and operation of a CS-DTC. In this CS-DTC, a current source (I_{ch}) is uti-

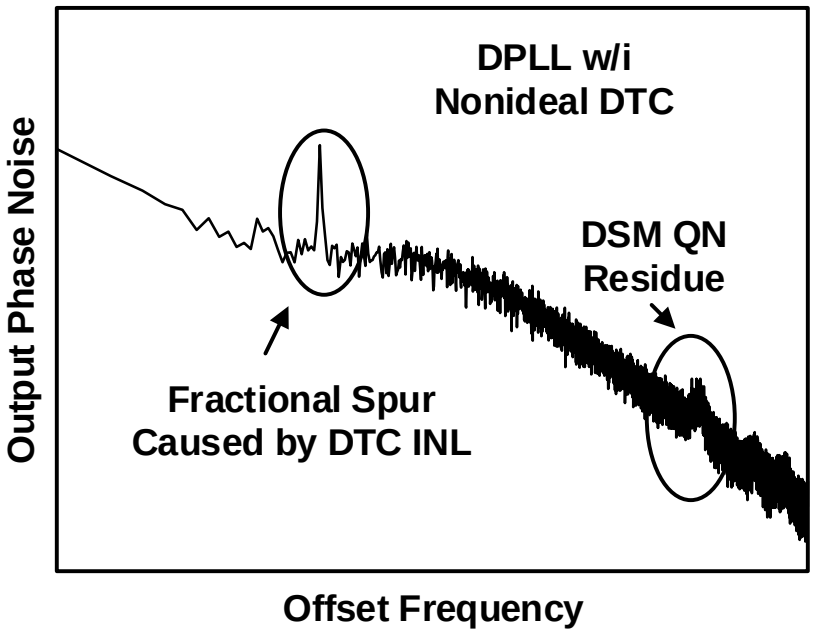


Figure 2.6: PN spectrum of a DPLL with non-linear DTCs.

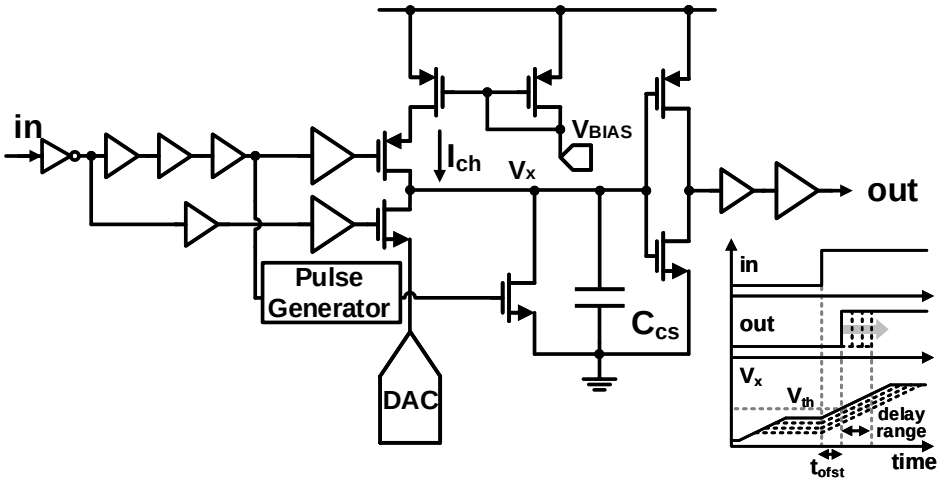


Figure 2.7: Schematic and operation of a CS-DTC.

lized to charge a fixed capacitance C_{cs}. Different τ_{dtc} is controlled by the DAC which pre-charges C_{cs} with different voltages. In the CS-DTC, the charging slope is always I_{ch}/C_{cs} and doesnot depend on the pre-charging voltage generated by the DAC. In this

way, the slope-induced nonlinearity at the output inverter buffer can be eliminated.

Despite the elimination of slope-induced nonlinearities, other nonlinearity sources are presented in the CS-DTC, which need to be considered during design process. First of all, the DAC is not perfectly linear. For the simplicity of implementation, an R-DAC is usually used [19], in which the nonlinearity is usually limited by the matching between resistor elements. Second, the current source suffers from short channel effect, and thus presents nonlinearity. Lastly, the pre-charging operation takes time to settle. Because the pre-charging speed is limited by the R-C constant, which is related to the output impedance of the DAC and C_{cs}, sufficient pre-charging time needs to be guaranteed. Otherwise if the pre-charging voltage is not propoerly settled, nonlinearities will be generated, which is also the reason why the application of CS-DTC cannot be easily extended to PLLs with high reference frequencies. In practical design, the maximum pre-charging voltage of a CS-DTC is usually controllled to be well below the threshold voltage (V_{th}) of the output buffer, so that the nonlinearities contributed by the current source can be suppressed. Regarding the nonlinearities from the R-DAC, a C-DAC might be used for a naturally better matching and better nonlinearity [20, 21].

2.2.2 Inverse-Constant-Slope DTC

The linearity of a CS-DTC can be further improved if the effect from I_{ch} nonlinearity can be eliminated. Recently, a novel and useful DTC topology, known as *inverse-constant-slope DTC* (ICS-DTC) is proposed, which is shown in Fig. 2.8 [22]. In the ICS-DTC, the MMD output is retimed multiple times using the DCO output. The precharging time can thus be controlled by selecting different MMD retimed outputs, which can be precise integer multiples of one DCO cycle. The precharging speed is controlled by the current source I_{ch}. After $n_{pch}{\cdot}T_{dco}$, the precharging is finished, and the other $(m\text{-}1)I_{ch}$ current sources are turned on. The voltage on C_{ics} will be charged from V_{pch} to V_{th} by a current of mI_{ch}, after which a rising edge will be triggered at the output.

The magic of ICS-DTC is that the nonlinearity from I_{ch} does not generate any influence on τ_{dtc}. This characteristic can be revealed by looking into the time-varying behavior of V_x. During the precharging and charging phase of the ICS-DTC, the precharging (or charging) time and V_x construct a bijection, *i.e.,* for any precharging (or charging) time, there is only one corresponding V_x, and vice versa. This allows the definition of a mapping from V_x to time t. The precharging time τ_{pch} can thus be expressed by Eq. (2.1).

$$\tau_{pch} = t|_{V_x=V_{pch}} = t(V_{pch}) \int_0^{V_{pch}} \frac{dt}{dV_x} dV_x. \tag{2.1}$$

In the precharging phase, V_x can be described by the charging function, *i.e.,* dV_x/dt =

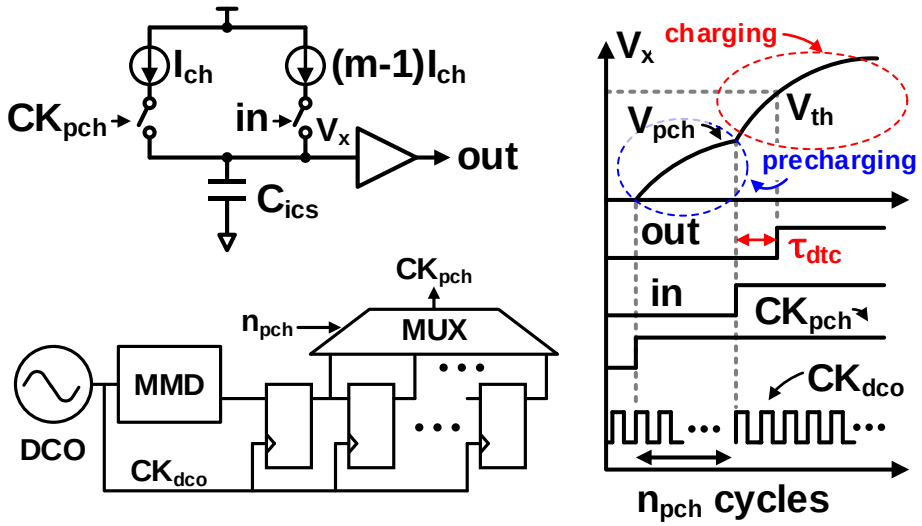


Figure 2.8: Schematic and operation of an ICS-DTC.

I_{ch}/C_{ics}. By inversing this function, $dt = (C_{ics}(V_x)/I_{ch}(V_x))dV_x$ can be obtained. Note that $C_{ics}(V_x)$ and $I_{ch}(V_x)$ imply that the charging current and charging capacitance both depend on V_x, which is the source of nonlinearities. Substituting this relationship to Eq. (2.1), an explicit expression of τ_{pch} can be obtained:

$$\tau_{pch} = \int_0^{V_{pch}} \frac{C_{ics}(V_x)}{I_{ch}(V_x)} dV_x. \tag{2.2}$$

Similarly, in the charging phase, the DTC delay τ_{dtc} can be derived as:

$$\tau_{dtc} = \int_{V_{pch}}^{V_{th}} \frac{C_{ics}(V_x)}{mI_{ch}(V_x)} dV_x. \tag{2.3}$$

A closed-form expression on the DTC delay can be obtained by substituting Eq. (2.3) into Eq. (2.2), which yields:

$$\tau_{dtc} = \frac{1}{m}\left(\int_0^{V_{th}} \frac{C_{ics}(V_x)}{I_{ch}(V_x)} dV_x - \tau_{pch}\right) = \frac{1}{m}\left(\int_0^{V_{th}} \frac{C_{ics}(V_x)}{I_{ch}(V_x)} dV_x - n_{pch}T_{dco}\right). \tag{2.4}$$

It can be seen from Eq. (2.4) that the nonlinear $C_{ics}(V_x)$ and $I_{ch}(V_x)$ create only a fixed term in τ_{dtc}. This means that the linearity of ICS-DTC can be well decoupled from the nonlinear current sources or charging capacitors. Meanwhile, the matching between I_{ch} and $(m\text{-}1)I_{ch}$ only affects the DTC gain instead of the DTC linearity, which can be easily

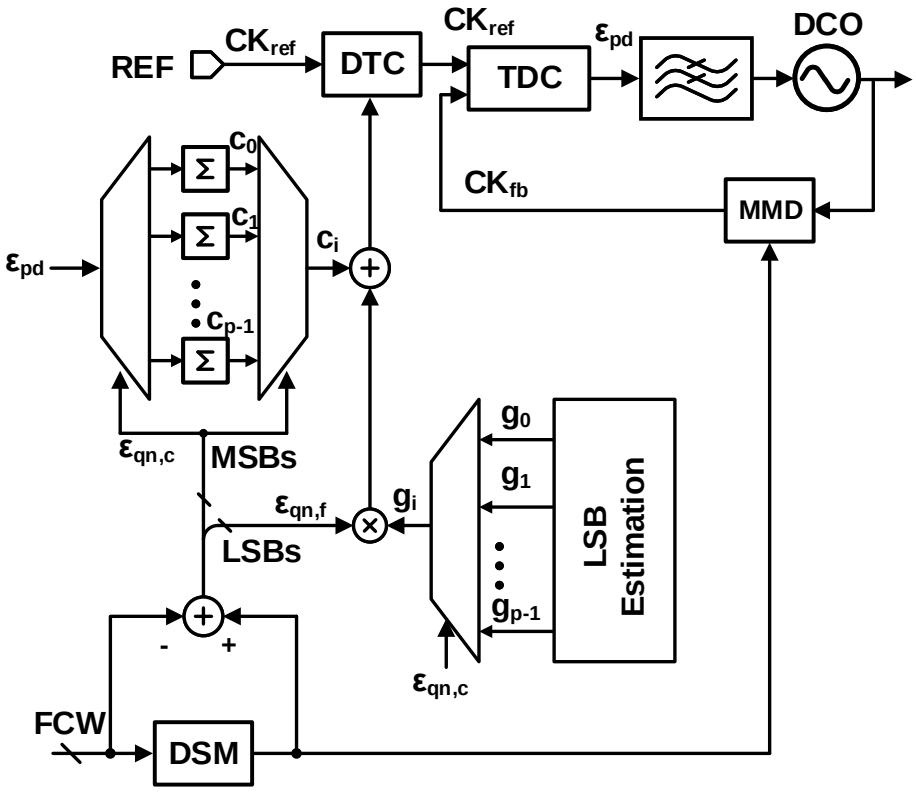


Figure 2.9: Schematic of a PLL with 1st order DPD.

calibrated by the LMS algorithm introduced in the previous section.

2.3 Digital Pre-Distortion on the DTC INL

The fractional spur performance can also be improved by applying some system design techniques. One straightforward method is *digital pre-distortion* (DPD), by which a lookup table (LUT) is utilized to learn the shape of τ_{inl}. Based on the information stored in the LUT, the delay control code can be adjusted accordingly to compensate τ_{inl}.

2.3.1 First Order Piecewise-Linear DPD

The first DPLL with DTC DPD was implemented in [23], with its schematic shown in Fig. 2.9.

In this PLL, the DSM QN was divided into p regions, so that the DTC gain can be estimated separately for each region. It can be seen from Fig. 2.10 that at the boundary

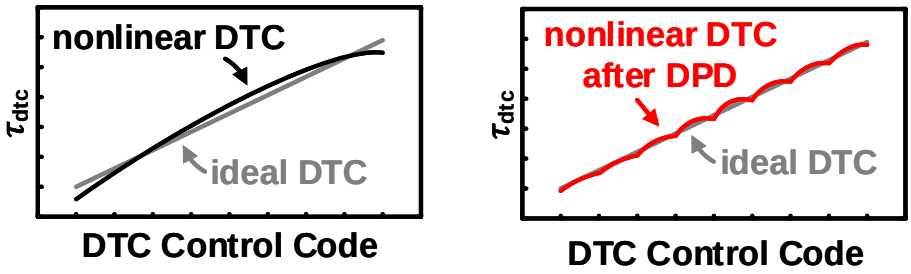


Figure 2.10: The effect of DPD.

of each region, the DTC nonlinearity can be fully eliminated, resulting in an overall improvement in the DTC INL. If the QN can be divided into more pieces, *i.e.,* if p can be further increased, the DTC INL can be eliminated on more and more points. However in real implementation, this corresponds to an increased number of integrators, which might take considerably large chip area and thus may sometimes not allowed by the chip budget. A more practical method is to limit the value of p, so that the most significant bits (MSBs) of the DTC can be sufficiently linear. For the least significant bits (LSBs), they are linearly scaled with different coefficients according to different DSM QN regions. For example, if the DSM is designed to be M-bit, the DSM QN will range from 0 to 2^M. The LSBs of ε_{qn} in the i-th region can be scalled by a factor of g_i, where g_i is estimated by:

$$g_i = \frac{p}{2^M}(c_{i+1} - c_i). \tag{2.5}$$

2.3.2 Zero Order Piecewise-Linear DPD

The DPD technique introduced previously is often referred to as first order piecewise-linear (PWL) DPD, for it calibrates the first order relationship (slope) between delay control code and τ_{dtc}. Although excellent fractional spur performance can be achieved with this technique, some limitations exist in this kind of DPD technique.

One of the limitation is that the calibration effect will be decreased when the DTC linearity is not continuous. This situation can happen when a segmented DTC structure is employed, *i.e.,* when the MSBs and LSBs of the DSM QN are canceled by two coarse and fine DTCs. Fig. 2.11 shows an example, where the coarse DTC is implemented as a path-selection DTC (PS-DTC), and the fine DTC is implemented as a VS-DTC. This kind of coarse-fine segmented DTC is often used in synthesizable PLLs [24]. Because

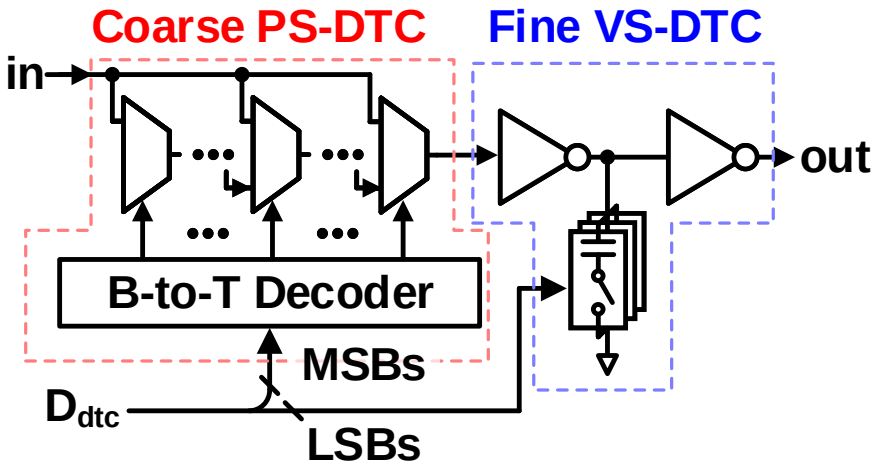


Figure 2.11: A coarse-fine segmented DTC.

the delay cell is usually ready to use in most of the standard cell libraries, the PS-DTC is preferred as the coarse stage. In each referecne cycle, the multiplexers (MUXs) in the PS-DTC are selected to be on or off so that the amount of activated delay cell can be selected according to the delay control code. Due to the automatic placing and routing (P&R) of the digital design tool, the load capacitances and device threshold voltages of different delay cells can suffer from big mismatch, resulting in a discontinuous INL curve. The fine DTC stage is usually implemented as VS-DTCs, where the parasitic varactors on the logic gates (*e.g.*, NAND gate) are used for load capacitance control.

The INL characteristic of the segmented DTC in Fig. 2.11 is shown in the left of Fig. 2.12. The overall INL is dominated by the coarse PS-DTC, which exhibits strong discontinuities. The upper right of Fig. 2.12 shows the resulting INL if the first order PWL DPD in [23] is implemented. Because of the mismatch-dominated INL, the slope information between neighboring coarse DTC control codes becomes meaningless. This information will erroneously scale the fine DTC control codes according to Eq. (2.5), leading to a INL amplitude degradation from 15 ps to 25 ps.

In this scenario, the DPD scheme should be adjusted such that the calibrator can successfully eliminate the coarse DTC INL. This can be achieved by the zero order interpolation (ZOI) DPD, which was reported in [24]. The ZOI PWL calibration scheme is depicted in Fig. 2.13, in which the coarse DTC INL is estimated and subtracted in the fine DTC control code. In this way, only the delay offset caused by coarse DTC INL is calibrated, the slope *i.e.,* the coarse DTC gain is not calibrated by the pre-distorter. For

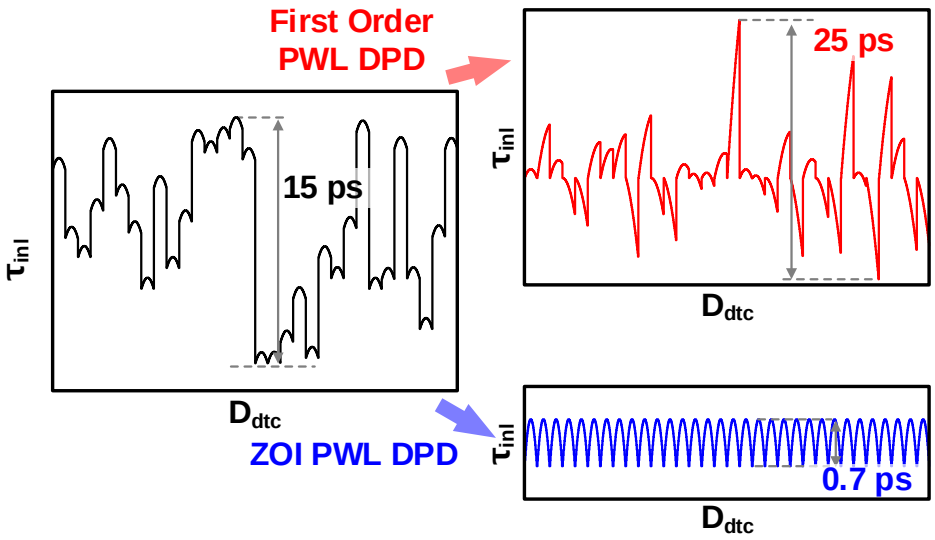


Figure 2.12: The INL of segmented DTC and the effect of different DPD schemes.

this reason, the LMS-based DTC gain calibration in [4] is still needed so that the effective DTC delay range can perfectly cover the range of DSM QN. With ZOI PWL DPD, the delay mismatch between different coarse DTC elements can be precisely removed. As shown in the bottom right of Fig. 2.12, the DTC INL is limited by the fine DTC nonlinearity, exhibiting segmented parabolic shapes across different DTC control codes.

2.3.3 Polynomial Fitting DPD

The above mentioned first order and ZOI PWL DPDs share the same drawback: the required LUT size will be larger if the targeted DTC INL residue is very small. For a numerical example, if the top 6 MSBs of the DTC delay needs to be calibrated, correspondingly 2^6 LUT elements will be needed, which can take a considerable large on-chip area to implement the digital accumulators and registers. Moreover, considerable time might be consumed for all the 2^6 LUT elements to update, which limits its implementation in the applications where the allowed PLL locking time is limited. Luckily, this problem can be alleviated if the DTC INL can be approximated by polynomials, which is exactly the case of VS-DTCs.

A typical VS-DTC INL curve is shown in Fig. 2.14 (balck curve). The shape can be very well approximated by the polynomial equation in Eq. (2.6). Based on this observation, the DTC INL can be compensated by estimating the corresponding polynomial coefficients, *i.e.*, p_2, p_3, *etc.* This DPD scheme is called *polynomial-fitting DPD*, which is

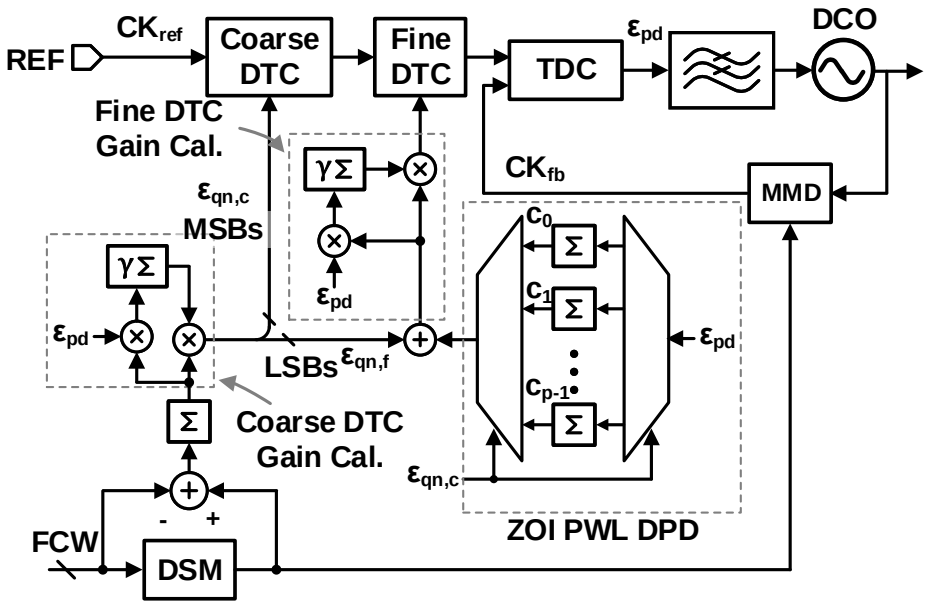


Figure 2.13: The DPLL with coarse-fine segmented DTC and ZOI PWL DPD.

firstly implemented for DTC INL calibration in [25].

$$\tau_{inl}[D_{dtc}] = p_0 + p_1 D_{dtc} + p_2 D_{dtc}^2 + ... \tag{2.6}$$

The polynomial coefficients can be estimated by correlating the TDC output with the corresponding powers of dtc control code. Fig. 2.15 shows the implementation of polynomial-fitting DPD in a DPLL. Similar to the LMS DTC gain calibration in Fig. 2.1, the second and third power of the DSM QN are correlated with the TDC output. The three LMS loops converge to the points where the first three polynomial terms matches the DTC INL curve. The effect of polynomial-fitting DPD is shown in Fig. 2.14. Because the DTC INL is dominated by the p_2 term in Eq. (2.6), a more than 8-fold INL suppression can be achieved by cancelling the p_2 term. Stronger INL suppression can be achieved if the p_3 term can also be canceled, leading to an overall 59-fold INL reduction. The advantage of this kind of DPD scheme is that much less LUT elements are required. In the example shown in Fig. 2.15, only 3 accumulators are required, which brings a huge reduction in hardware cost and calibration time.

In a practical implementation, the effect of polynomial-fitting DPD is often limited by the mismatch dependent INL components, which can result from layout mismatches, device mismatches, *etc.* Moreover, the effect in INL suppression can be limited in the

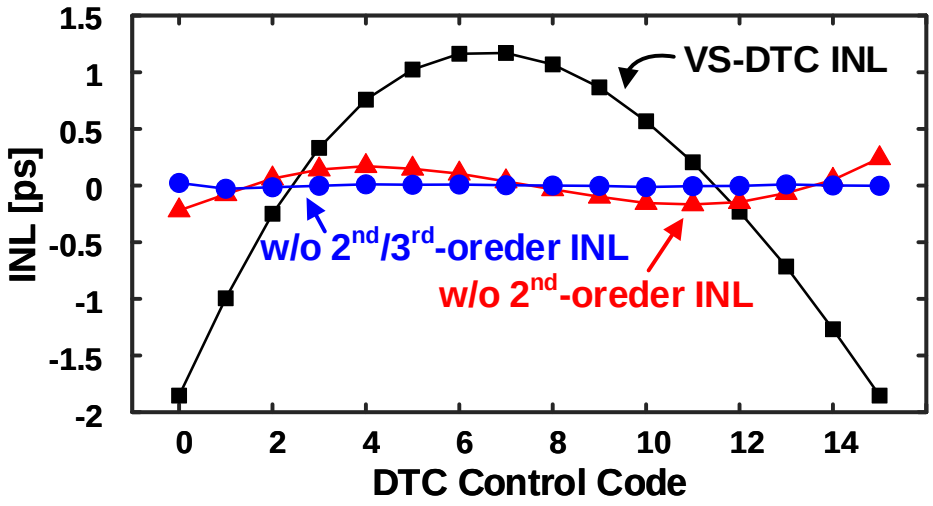


Figure 2.14: VS-DTC INL suppression via polynomial fitting DPD.

case where the DTC INL cannot be approximated by a limited number of polynomial terms, *e.g.,* the PS-DTC. The key idea here is that DPD schemes should be carefully selected according to the DTC topology, the required chip area, and the calibration time specifications.

2.4 Fractional Spur Suppression by Dithering

DPD is not the only way to improve fractional spur performance. One another effective method is to randomize the DSM QN pattern by a *dithering* signal, which can date back to early APLLs based on charge pump (CP) [26]. The concept of dithering is shown in Fig. 2.16, where a the DSM QN sequence is randomized by a dither signal. Due to the randomized DSM QN, the pattern of DTC control code, and thus the corresponding INL error pattern can also be randomized. Ideally, due to the randomized INL error pattern, the spur power generated by the DTC nonlinearity can be scrambled to wider frequency ranges. As shown in the bottom of Fig. 2.16, no spurious tones can be observed in the reference path noise spectrum. Instead, the noise floor is elevated, with the power contributed by the original INL errors.

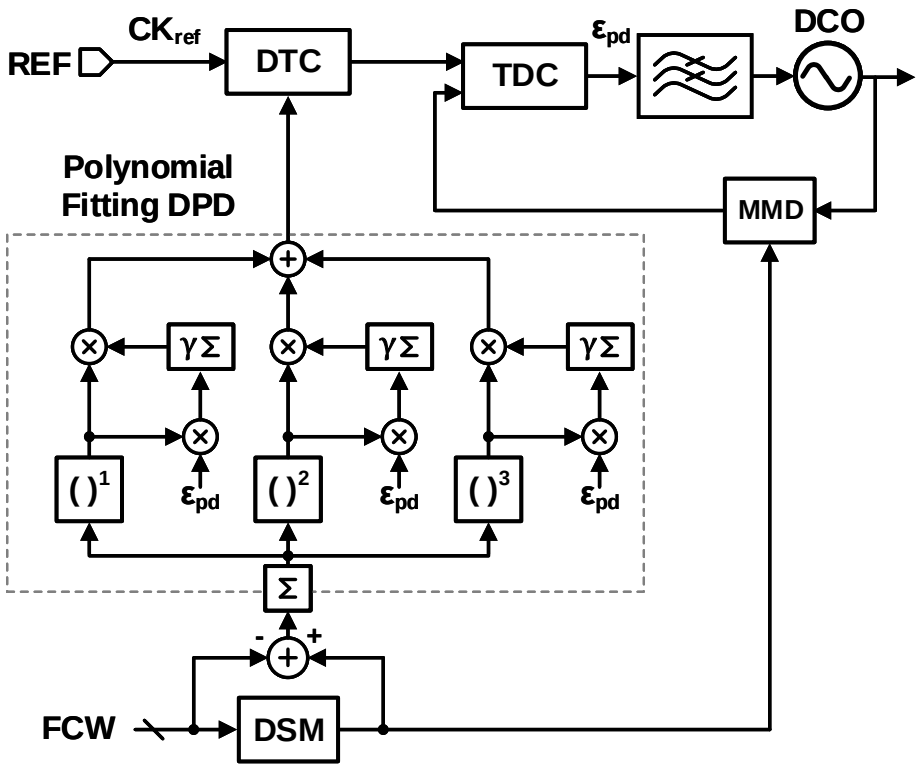


Figure 2.15: DPLL with polynomial fitting DPD for DTC INL calibration.

2.4.1 Randomizing the Pattern of INL Error

There are multiple ways to apply the dithering signal, of which the simplest one is to add the dithering signal directly at the input of a MASH-1-1 DSM. Fig. 2.17 shows this type of implementation and the corresponding operation details. The FCW is added with the output of a pseudo random number generator (PRNG), the result of which is then fed into the DSM. In this example, the FCW is assumed to be with a 6-bit fractional resolution. The fractional part of FCW is assumed to be $9/2^6$. Without being applied with the dither signal, the DSM output, r_{div} behaves a strong periodicity, generating a moving average of exatcly $9/2^6$. When being applied with a dithering signal which takes randomly from 0 and $9/2^6$, the DSM output becomes more randomized. One drawback of this kind of dithering is that the moving average of the DSM output will be elevated (by $9/2^7$), leading to a frequency deviation of the PLL. Another drawback of this dithering method is that the DSM QN cannot be sufficiently randomized, which can be evidenced from the dithered DSM output in Fig. 2.17, which still exhibits some periodicity. The spectrum of an ideal DTC delay driven by a MASH-1-1 DSM is shown in Fig. 2.18, of which the shape is

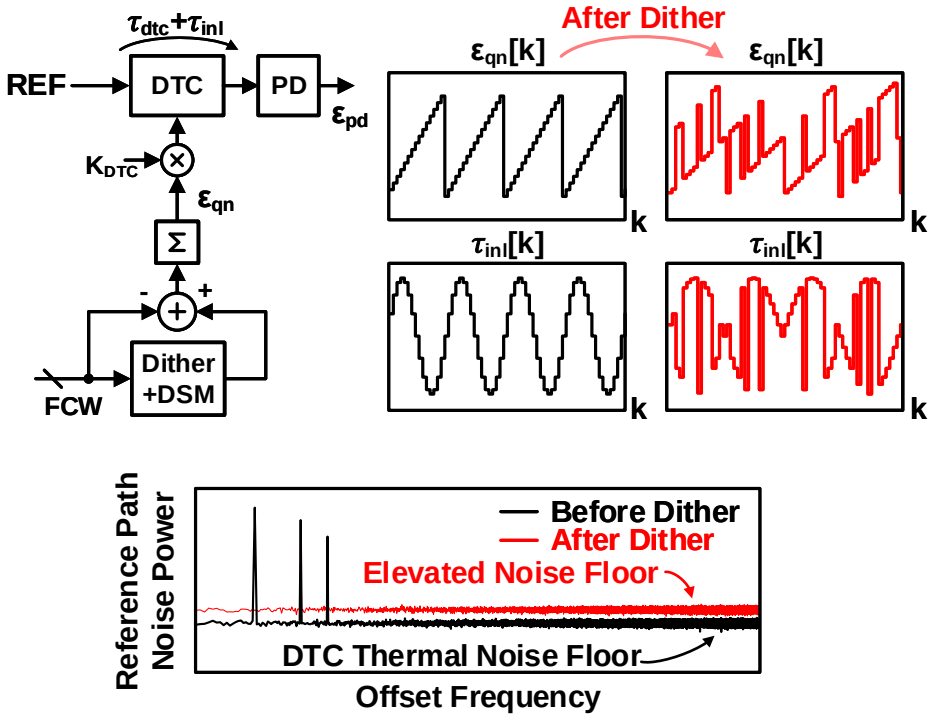


Figure 2.16: The concept of suppressing the fractional spurs by dithering.

equal to that of the DSM QN. When the input dither is applied to the DSM, the fractional spurs still appear if the DTC is not linear, as shown in the bottom of the same figure.

Since the ultimate objective of dithering is to randomize the INL error pattern, the dither signal can also be added directly to the DTC control codes. This can be achieved by the time-invariant probability modulator (TIPM) proposed in [27], with its topology shown in Fig. 2.19. Note that if the dither signal is directly added to the DTC control codes, the dither power will be paased to the DTC output. In order to avoid the PLL PN degradation, the dither power needs to be canceled. To this aim, another DTC is implemented at the output of MMD, with its delay controlled directly by the dither signal *di[k]*. In this way, the relative delay generated by the reference-path DTC (DTC_r) and divider-path DTC (DTC_d) is still equal to the DSM QN. Meanwhile, the delay control codes of each single DTC can be randomized, as depicted in Fig. 2.20.

Note that care must be taken in generating the dithering signal (*di[k]*) such that the DTC control codes for DTC_r and DTC_d can be uniformly distributed between 0 and 1. This can be done by the combination of the DSM QN and an uniformly-distributed random number (*urn[k]*) generated by digital logics. Eq. (2.7) shows how this is operated mathematically:

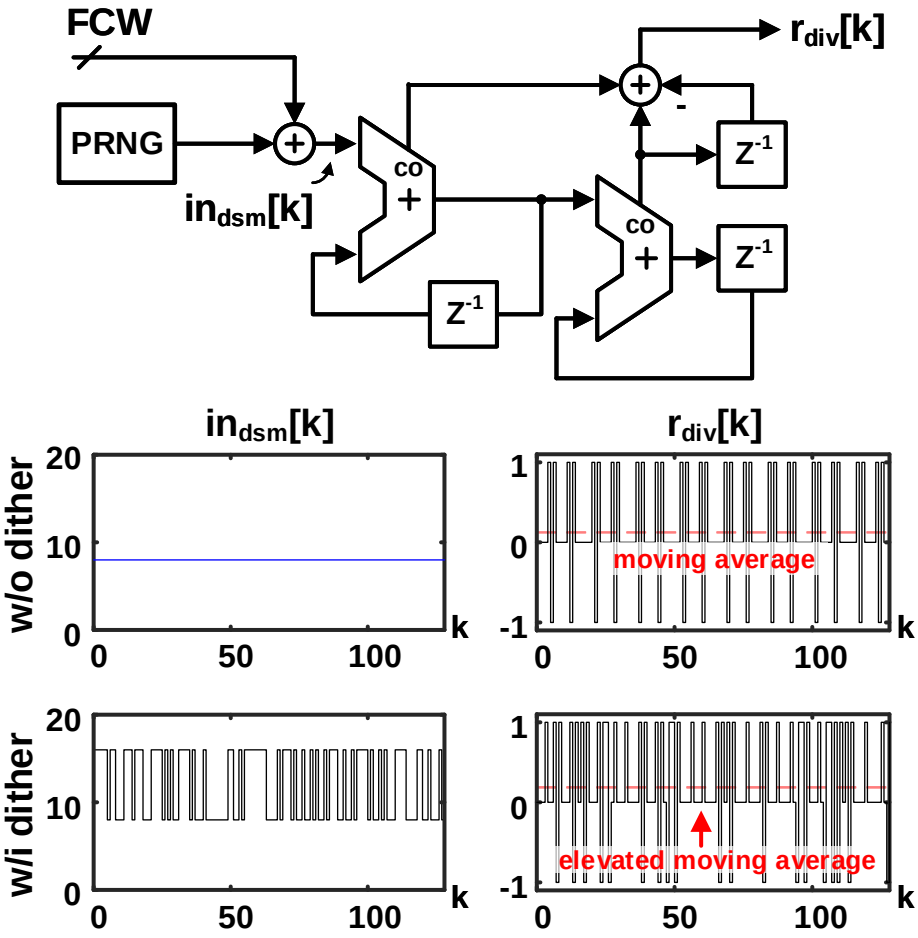


Figure 2.17: Input-dithered DSM.

$$di[k] = \begin{cases} 1 - urn[k](1 - \varepsilon_{qn}[k]) & ,\varepsilon_{\text{qn}}[\text{k}] > 0 \\ urn[k](1 + \varepsilon_{qn}[k]) & ,\text{else.} \end{cases} \tag{2.7}$$

With TIPM, the DTC control code can be sufficiently randomized, as shown in the top of Fig. 2.21, where no spurious tones can be observed. The spectrum of the equivalent delay generated by the DTC pair is also shown in the bottom side of the same figure. It is worth mentioning that the in-band noise power density of the equivalent delay is around -150 dBc/Hz, which is higher than the spectrum of an ideal DTC (around -175 dBc/Hz, as shown in the top of Fig. 2.18). This is because the original spur power does not disappear, rather, they are spreaded out into a wider frequency range.

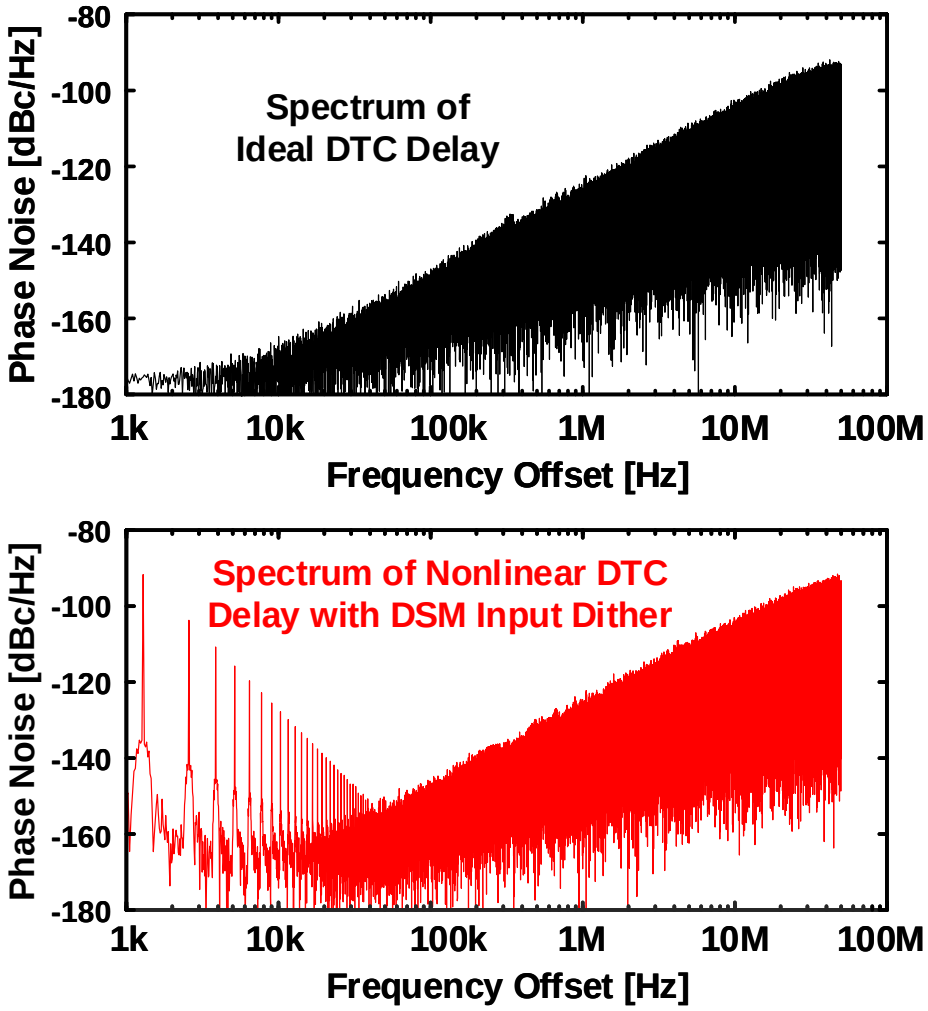


Figure 2.18: The DTC delay spectrum.

2.4.2 Whitening the DSM QN Spectrum

In low-phase-noise DTC-based DPLLs, the input range of the TDC can be far lower than the TDC resolution. In this case, even a multi-bit TDC can be treated as equivalent to a BBPD. The TDC nonlinearity caused by the mismatch between different TDC delay elements will not degrade the PLL output spectrum because they are no longer experienced by the TDC in this case. On the other hand, in the DPLLs where the ouput PN is less good, *e.g.,* in DPLLS that are based on ring oscillators (ROs), the TDC input range can easily go beyond the TDC resolution. In this situation, the mismatch-dependent TDC nonlinearity still disturbs the loop. Even in the case where the TDC resembles a BBPD,

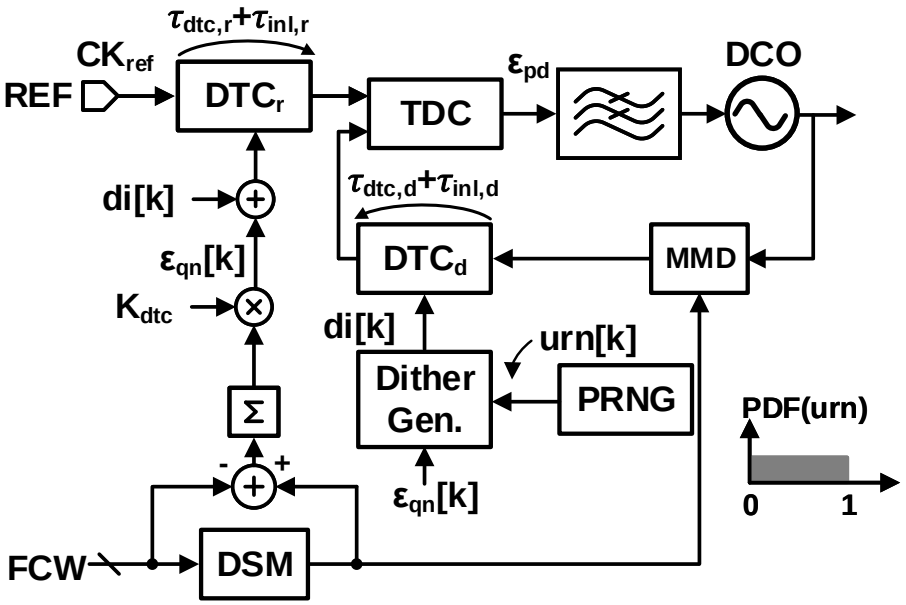


Figure 2.19: The DTC delay spectrum with TIPM.

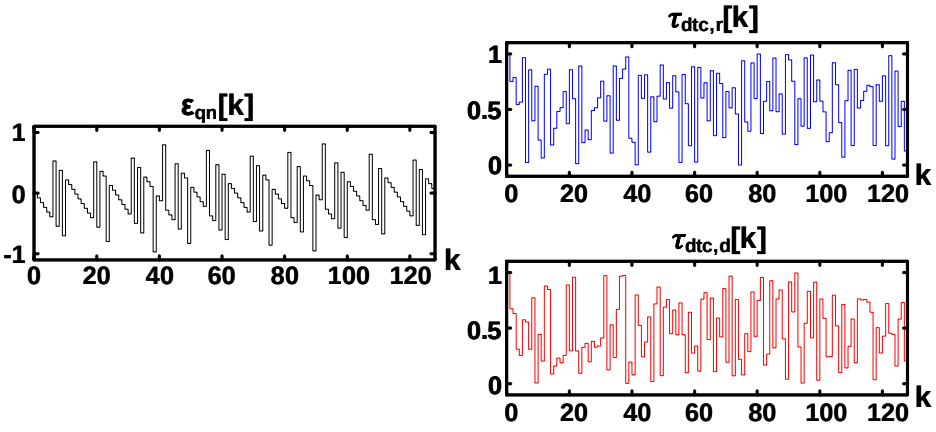


Figure 2.20: The DTC delay spectrum with TIPM.

the PD nonlinearity still exist. Moreover, the DCO also contributes to nonlinearity when its control codes toggle between several different numbers.

Taking those factors into consideration, the limitation of the previously introduced TIPM can be revealed: the TIPM only randomizes the DTC control codes, while the DSM QN pattern is still preserved and thus will exhibit periodicity. Because of this, the

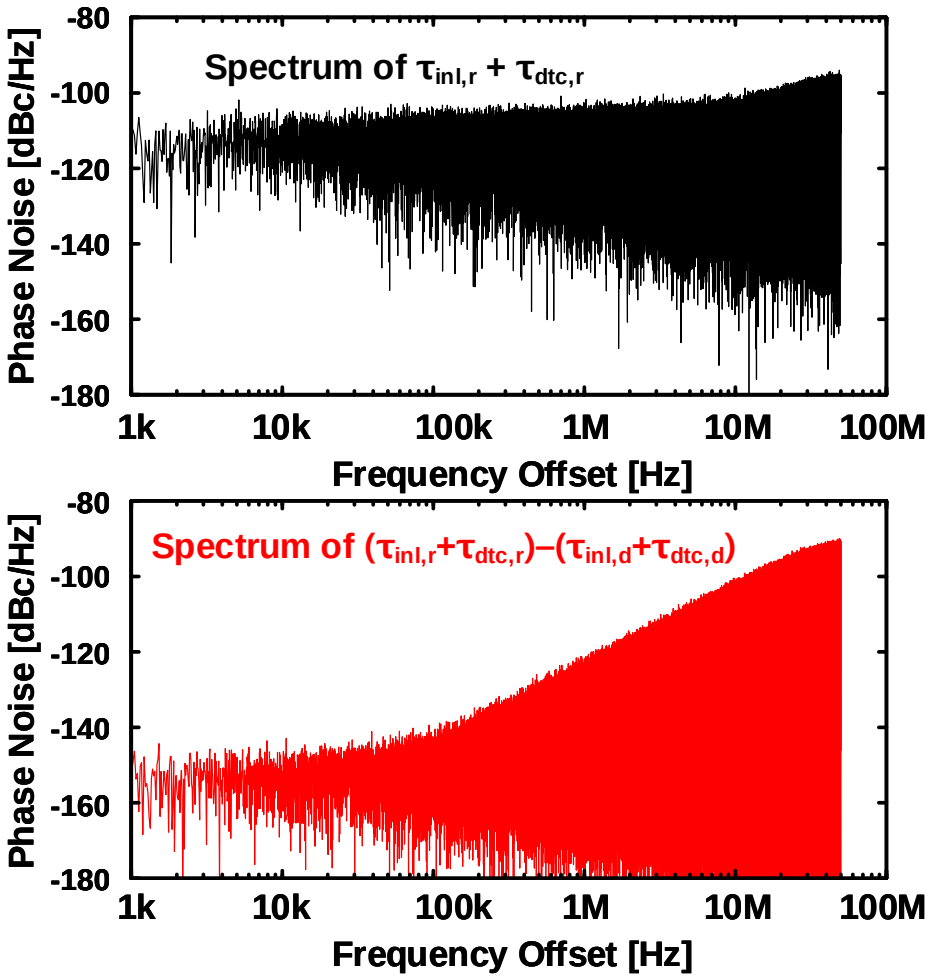


Figure 2.21: The DTC delay spectrum with TIPM.

nonlinearities generated by the TDC and DCO, which are dependent on the DSM QN, will still be periodical. In other words, the TIPM is only effective for randomizing DTC INL.

In order to mitigate the nonlinearities from other block circuits in the DPLL, the DSM QN itself could be randomized. This can be achieved by the *probability-density-shaping DSM* (PDS-DSM), which was proposed in [25]. The implementation of a PDS-DSM is shown in Fig. 2.22. The dither signal *di[k]*, which is generated by combining two identical and independently distributed (i.i.d.) random numbers (urn_1 and urn_2), is fed to the input of the second stage accumulator of a conventional MASH-1-1 DSM. Remarkably, because urn_1 and urn_2 are both uniformly distributed, the combination of them leads to a very interesting characteristic: the dithered DSM QN can become immune to polyno-

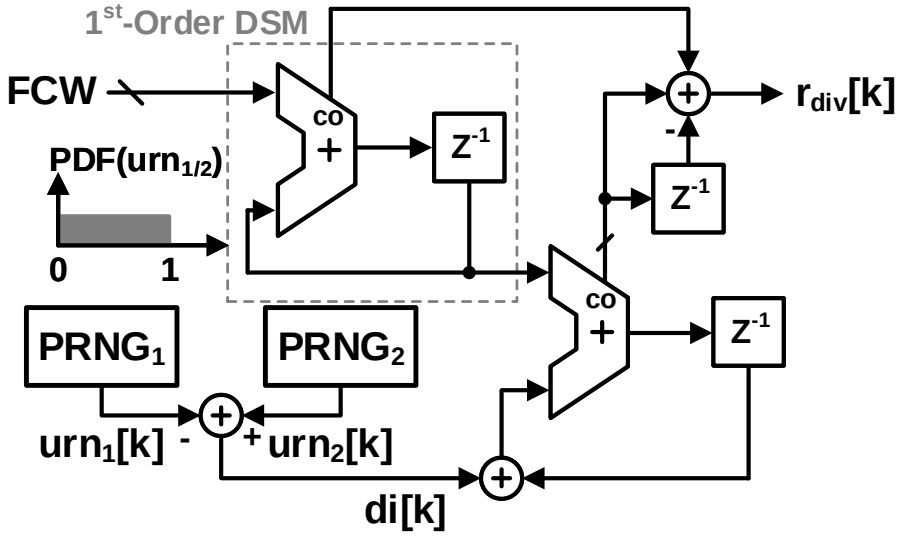


Figure 2.22: The implementation of PDS-DSM.

mial nonlinearities up to some specific orders, *i.e.,* the DSM QN spectrum is free from some fractional spurs. The detailed derivation of this characteristic is beyond the scope of this thesis, but it can be found in [28]. For the example in Fig. 2.22, the DSM QN is immune to up to third order polynomial nonlinearities, regardless of where are the nonlinearities generated from. In this way, the nonlinearities form the TDC and DCO can also be scrambled. Moreover, the TIPM can be implemented together with this PDS-DSM utilizing *di[k]*. The benefit of doing this is that the DTC control codes can be sufficiently randomized such that the memoryless DTC nonlinearities up to any order will not contribute to fractional spurs in the DPLL output.

Notably, this immunity to polynomial nonlinearities is at the cost of extended DTC delay range. This can be understood by comparing the distribution of DSM QN of a MASH-1-1 DSM and the PDS-DSM in [25], which is shown in Fig. 2.23. During the DSM operation, the DSM QN can be considered as *periodically* taking values *randomly* from different *tracks* [29]. For a conventional MASH-1-1 DSM, there are two possible tracks for the DSM QN to reside on, leading to a required DTC delay range of $2T_{dco}$. On the othewr hand, 4 tracks exist in the QN of a PDS-DSM, requiring a DTC delay range of $4T_{dco}$. Longer DTC delay range will result in higher thermal noise contributed by the DTCs, which implies an inherent trade-off between the fractional spur suppression effect and the PLL IPN.

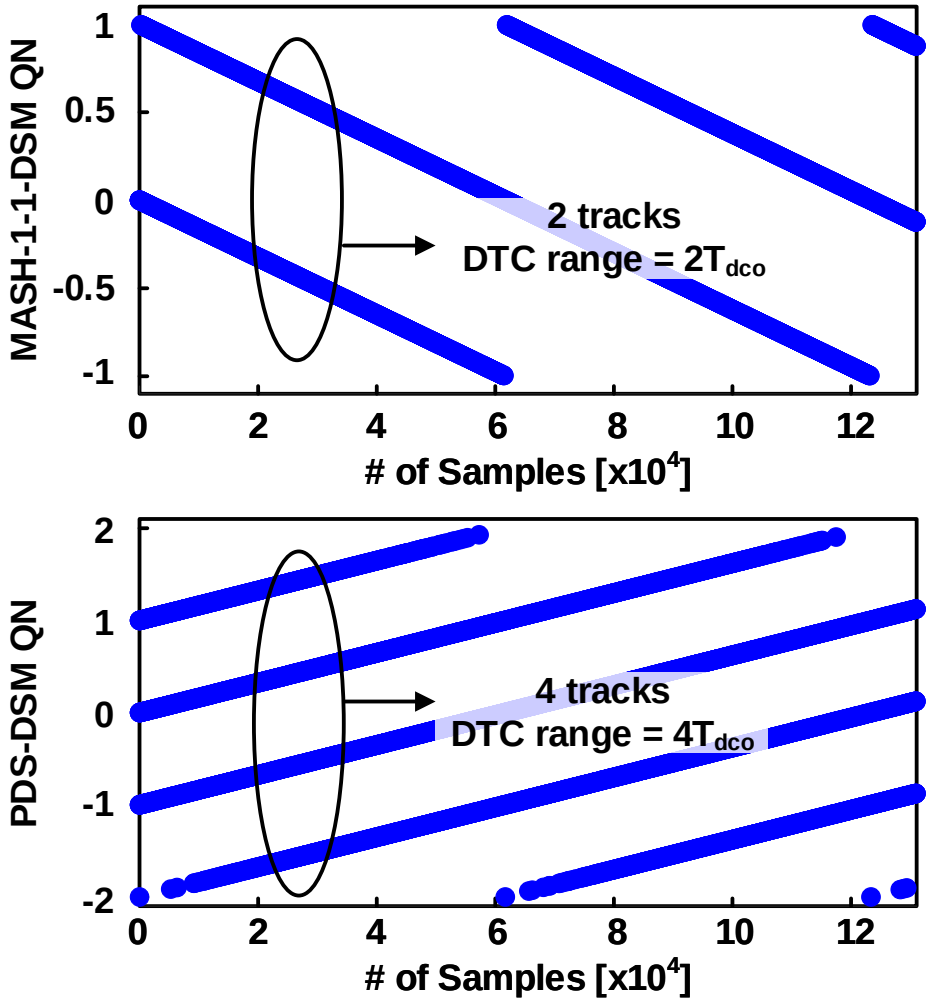


Figure 2.23: The implementation of PDS-DSM.

2.5 Summary

In this chapter, the basic structure of DTC-based DPLLs is introduced. When a near-integer channel is simulated, the nonlinearities from the DTC will be modulated by the DSM QN, and lead to fractional spurs. In order to improve the fractional spur performance in DTC-based DPLLs, three conventional methods are presented:

1. High-linearity DTC topologies such as CS-DTCs and ICS-DTCs can be implemented, which lead to a directly lower DTC INL, and thus the improvement in fractional spur and phase noise performance of the DPLL.

2. DPDs can be utilized to learn and compensate the DTC INL. Nevertheless, different

DPD schemes should be carefully selected according to the specific DTC topology, PLL locking time specification, and area specification, *etc.*

3. Dither can be applied to the DSM such that the DTC INL, or even TDC and DCO INL patterns can be randomized. In this way, the spur power can be scrambled into wider frequency ranges, leading to an effective suppression in its power. It worths mentioning that the spur power still exists in the form of random noise, which is the reason why an elevated noise floor can always be observed when dithering is implemented.

Note that it is possible to combine those techniques together to achieve a even better PLL phase noise and fractional spur performance. On the other hand, limitations might exist for each of the single techniques. For example, although an excellent spur performance can be achieved by the PDS-DSM, the IPN degradation might still be severe when the PLL loop bandwidth needs to be wide for filtering the PN from a noisy DCO. The linearity of CS-DTC is high, but the pre-charging phase can be time-consuming, which limits its application to PLLs with high reference frequencies.

In order to overcome these limitations, other fractional spur suppression techniques need to be developed.

Chapter 3

A Cascaded Dual-Fractional-*N* DPLL for Fractional Spur Suppression

In some cases, the output of a PLL can be utilized as the reference signal of another PLL, *i.e.,* a *cascaded PLL* is constructed. Conventional cascaded PLLs are widely used for extending the frequency range [30, 31], synthesizing higher frequency *e.g.,* millimeter-wave [32], and suppressing DSM QN [33], *etc.*

The combination of two PLLs can take a lot of different forms. For example, each PLL can be selected from LC or RO-based topologies, leading to 4 different combination possibliities. When a fractional frequency resolution is needed, at least one PLL needs to be a fractional-*N* PLL, which can be placed in either the first stage or the second stage. Utilizing the extraordinary degree of freedom in cascaded PLL design, a novel cascaded PLL topology, in which both of the two stages are fractional-*N* PLLs, will be presented in this chapter. By combining the two fractional *FCWs*, the fractional spur degradation at near-integer channels can be avoided.

3.1 Cascaded PLL for Fractional Spur Suppression

3.1.1 Operation Principles

The proposed PLL is inspired by some of the modern PLLs with cascaded structures. For example, as shown in Fig. 3.1 (a), the cascaded PLL employs a fractional-*N* first stage and an integer-*N* second stage. This topology is widely used for millimeter-wave synthesis [32]. Usually, the first stage will generate a frequency of sub-10 GHz because the on-chip inductor can achieve optimal quality factor (Q factor) in this frequency and thus best phase noise performance can be achieved. The first stage loop bandwidth $f_{bw,1}$

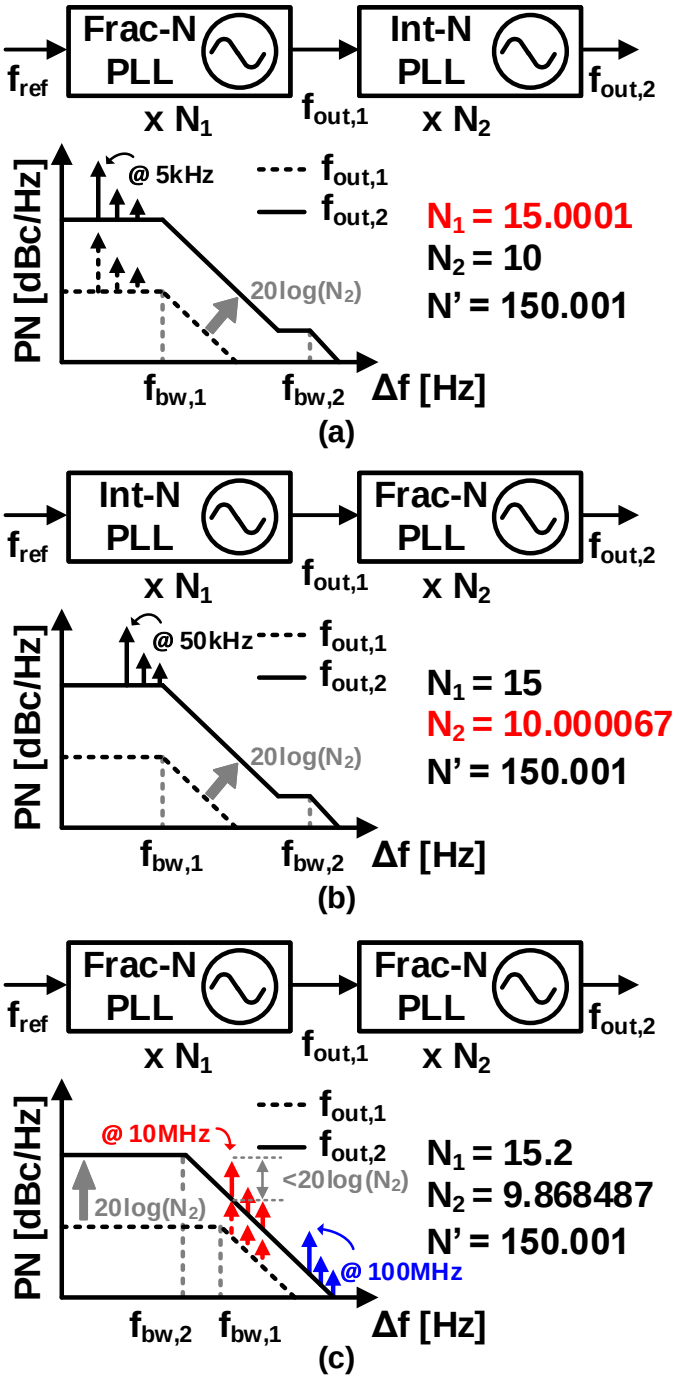


Figure 3.1: Conceptual illustration of the topologies and PN spectra of (a) fractional-*N*-integer-*N* cascaded PLL, (b) integer-*N*-fractional-*N* cascaded PLL, and (c) cascaded dual fractional-*N* PLL.

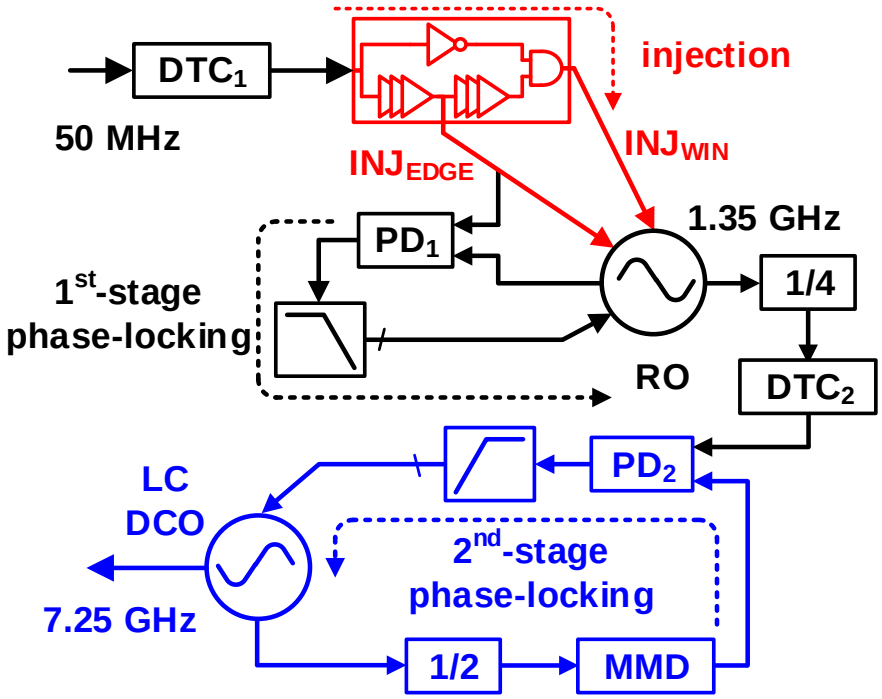


Figure 3.2: Simplified schematic of the proposed cascaded fractional-N PLL.

is usually selected to balance the phase noise from reference and the first DCO (or VCO). The second stage loop bandwidth $f_{bw,2}$ is usually high to suppress the bad second DCO (or VCO) phase noise. When a near-integer channel is being synthesized, the first stage will generate fractional spurs with low offset frequencies that cannot be filtered by $f_{bw,1}$. Those spurs will be further amplified by the feedback gain in the second stage, leading to severe spurious emission problems in the final output. As shown in Fig. 3.1 (b), the fractional-N PLL can be moved to the second stage as in [33] and [34]. In this way, the DSM quantization noise can be suppressed because of the high sampling frequency. However, when a near-integer channel is being synthesized, the fractional spurs still get degraded due to the low offset frequency.

Different to the topologies in Fig. 3.1(a) and Fig, 3.1(b), we propose a cascaded PLL of which both stages are in fractional-N mode. As shown in Fig. 3.1(c), when a near-integer channel is being synthesized, the two FCWs N_1 and N_2 are selected to be far from 0 or 1 such that the fractional spurs will be located at high offset frequencies. In this way, those spurs can be filtered by the second stage loop bandwidth $f_{bw,2}$, leading to low spur power at near-integer channels.

Numerical examples are also shown in Fig. 3.1 to illustrate the fractional spur suppression in the proposed PLL. Assume $N_1 = N_{int,1} + N_{frac,1}$, and $N_2 = N_{int,2} + N_{frac,2}$, where

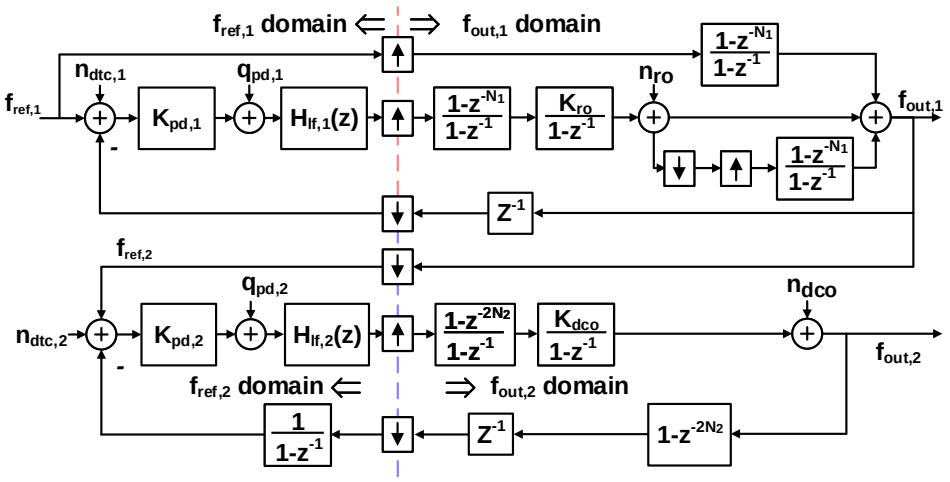


Figure 3.3: Discrete time noise model of proposed cascaded fractional-N PLL.

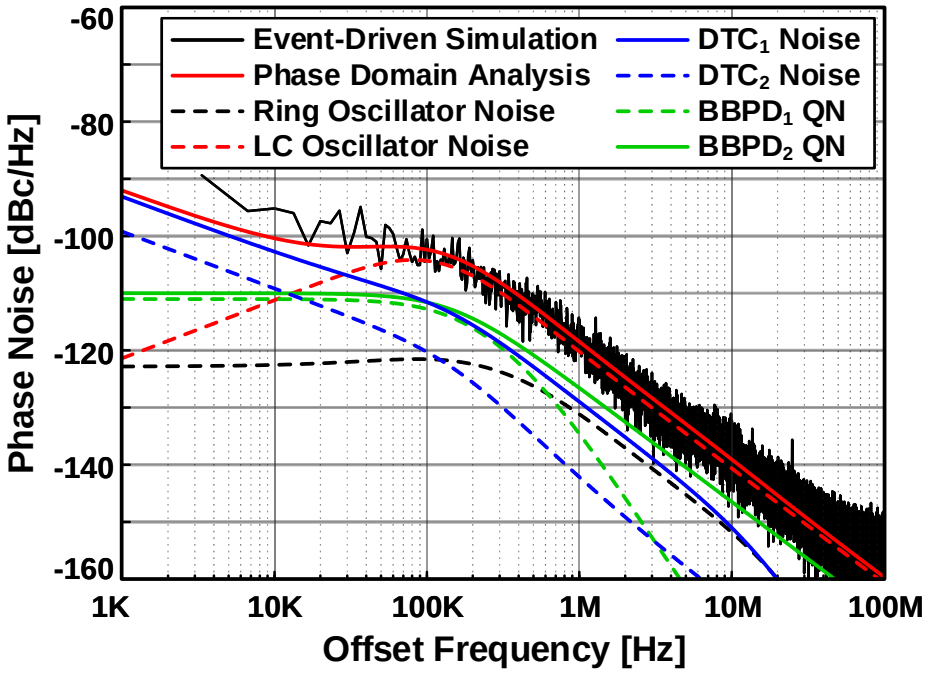


Figure 3.4: Phase noise contribution from different noise sources in the proposed cascaded fractional-N PLL.

$N_{int,1}$, $N_{int,2}$ are integer numbers, and $N_{frac,1}$, $N_{frac,2}$ are fractional numbers between 0 and 1. The output frequencies of the two stages are $f_{out,1} = N_1 f_{ref}$, and $f_{out,2} = N_2 f_{out,1}$ respectively. The cascaded PLL will thus multiply the reference frequency f_{ref} by a factor of $N' = N_1 N_2$. Suppose the cascaded PLL is going to generate an $f_{out,2}$ of 7500.05 MHz from a 50 MHz f_{ref}, and $N_{int,1}$ is fixed at 15 for convenience. When the first stage is a fractional-N PLL and the second stage is an integer-N PLL, fractional spurs will appear at $f_{out,1}$ with offset frequencies of $N_{frac,1} f_{ref} = 5$ kHz [29, 35] and the corresponding harmonic frequencies, e.g., 10 kHz, 15 kHz, etc. Those spurs will appear at the final output, with amplitudes

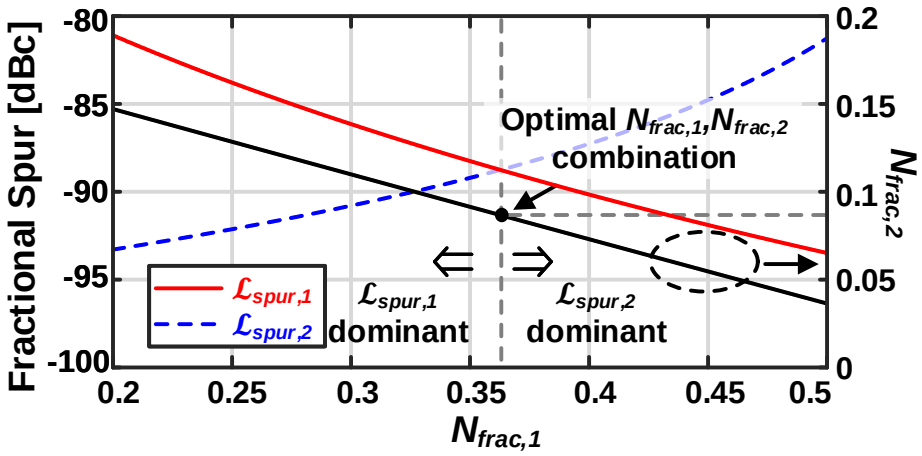


Figure 3.5: The optimization of FCWs in the proposed cascaded fractional-N PLL.

elevated by $20\log N_2$. Similarly when the first stage is an integer-N PLL and the second stage is a fractional-N PLL, because $f_{out,1}$ = 750 MHz, fractional spurs in the final output will appear at $N_{frac,2}f_{out,1} \approx 50$ kHz and the corresponding harmonic frequencies. In the above two situations, the fractional spurs cannot be filtered by the second stage because of the low offset frequencies. However, as shown in Fig. 3.1(c), in the proposed structure, N_1 is set to 15.2 and N_2 is set to 9.868487. The first stage will generate fractional spurs with a fundamental frequency of $N_{frac,1}f_{ref}$ = 10 MHz. Because $N_{frac,2} > 0.5$, the second stage will generate fractional spurs with a fundamental frequency of $(1 - N_{frac,2})f_{out,1} \approx$ 100 MHz [29, 35]. The fractional spurs in the proposed PLL can thus be easily filtered by the loop characteristics.

Fig. 3.2 shows a simplified schematic of the proposed cascaded PLL. Because both of the two stages are in fractional-N mode, DTCs are utilized in both stages to cancel the DSM quantization noise. A ring oscillator (RO) is implemented in the first stage because an LCDCO at low frequency will be bulky. A multiplying delay-locked loop (MDLL) topology is used in the first stage to provide high $f_{bw,1}$ for better suppression of the RO phase noise. In the second stage, a type-II DPLL with $f_{bw,2}$ of around 200 kHz is adopted. An LCDCO is used in the second stage to achieve better phase noise performance. It needs to be clarified that the proposed cascaded PLL can also be implemented as two cascaded LCDCO-based DPLLs in the scenarios where lower PN performance is required. However, it is necessary to set the bandwidth of at least one of the two stages to be "narrow" such that fractional spurs can be easily filtered. Moreover, when high-linearity DTCs are employed or DPD is applied, the loop bandwidth can be wider for the trade-off between reference noise and DCO noise. The frequency plan of the proposed cascaded PLL is as follows: the first stage generates an $f_{out,1}$ of 1.2 $\sim$ 1.5 GHz from an $f_{ref,1}$ of 50 MHz, in order to avoid the long DTC delay range for fractional-N operation at low frequencies. A

1/4 divider is inserted after $f_{out,1}$ to generate the reference for the second stage, $f_{ref,2}$. The final output $f_{out,2}$ ranges from 6.5 to 8 GHz.

3.1.2 Loop Characteristics

Detailed analyses of MDLL and Bang-Bang DPLL have been performed in [36–38]. The discrete-time noise model of the proposed PLL based on these analyses is shown in Fig. 3.3. The phase noises contributed by different noise sources are calculated from the discrete-time noise model, which is shown in Fig. 3.4. It can be seen that the phase noise from RO is greatly filtered by the two stages and is almost negligible compared to other noise sources. The overall phase noise of the PLL is dominated by the noise from DTC_1 and the noise from LCDCO. An event-driven simulation in verilog environment is performed to validate the noise model, with the result shown in the same figure.

Just like the noises from the two DTCs, the INL errors of DTC_1 and DTC_2 are introduced before the inputs of the two PDs. As a result, the INL of DTC_1 will be low-pass filtered by both of the two stages, with the noise transfer function of

$$NTF_{inl,1}(f) = \frac{N_1 N_2/2}{(1+i\frac{f}{f_{bw,1}})(1+i\frac{f}{f_{bw,2}})}, \tag{3.1}$$

Note that different from the frequency multiplication ratio *N'* in section-II A, the frequency multiplication ratio N in the real implementation is $N_1N_2/2$ because of the /4 divider and the /2 pre-scaler. The INL of DTC_2 will be filtered by the noise fransfer function of:

$$NTF_{inl,2}(f) = \frac{2N_2}{(1+i\frac{f}{f_{bw,2}})}. \tag{3.2}$$

Assume the INL of DTC_1 is in sine-shape with an amplitude of $INL_{pp,1}$, the phase disturbance induced by it will cause a tone with double-sided power of $(\pi^2/4)(INL_{pp,1}/T_{ref,1})^2$ [23], where $T_{ref,1}$ is the period of reference signal. The fractional spur level induced by DTC_1's INL can be expressed as:

$$\begin{aligned}\mathscr{L}_{spur,1}(f) &= (\frac{\pi INL_{pp,1}}{2T_{ref,1}})^2 |NTF_{inl,1}(f)|^2 \\ &= |\frac{\pi INL_{pp,1}}{2T_{dco}(1+i\frac{f}{f_{bw,1}})(1+i\frac{f}{f_{bw,2}})}|^2,\end{aligned} \tag{3.3}$$

where T_{dco} is the period of the LCDCO in the second stage.

Similarly, the fractional spur level induced by the INL of DTC_2 can be estimated as the

following equation, given the assumption that it is also in sine-shape with an amplitude of $INL_{pp,2}$:

$$\begin{aligned}\mathscr{L}_{spur,2}(f) &= (\frac{\pi INL_{pp,2}}{2T_{ref,2}})^2 |NTF_{inl,2}(f)|^2 \\ &= |\frac{\pi INL_{pp,2}}{2T_{dco}(1+i\frac{f}{f_{bw,2}})}|^2.\end{aligned} \tag{3.4}$$

According to [35], the frequency of fractional spur in the m-th stage (m= 1, 2) can be expressed as:

$$f_{spur,m} = \begin{cases} N_{frac,m} f_{ref,m}, & \text{if } N_{frac,m} < 0.5, \\ (1-N_{frac,m}) f_{ref,m}, & \text{if } N_{frac,m} > 0.5. \end{cases} \tag{3.5}$$

For the fixed $N_{int,1}$, $N_{int,2}$, and N, $N_{frac,2}$ becomes a function of $N_{frac,1}$, which can be derived as:

$$N_{frac,2} = \frac{N/2}{N_{int,1}+N_{frac,1}} - N_{int,2}. \tag{3.6}$$

It can be seen from Eq. (3.6) that as $N_{frac,1}$ becomes larger, a smaller $N_{frac,2}$ is required to achieve the same output frequency. On the other hand, Eq. (3.5) implies that the $N_{frac,m}$ to $f_{spur,m}$ relationship is not monotonic, which further leads to non-monotonic $N_{frac,1}$ to $L_{spur,m}$ relationships. As a result, the optimization of FCWs needs to be discussed in four different cases where: 1) $N_{frac,1} < 0.5$ and $N_{frac,2} > 0.5$; 2) $N_{frac,1} > 0.5$ and $N_{frac,2} < 0.5$; 3) $N_{frac,1} < 0.5$ and $N_{frac,2} < 0.5$; 4) $N_{frac,1} > 0.5$ and $N_{frac,2} > 0.5$.

In the first case, increasing $N_{frac,1}$ causes a smaller $N_{frac,2}$. Because $N_{frac,1} < 0.5$ and $N_{frac,2} > 0.5$, lower fractional spur levels can be expected from the two stages. Further increasing $N_{frac,1}$ until $N_{frac,1}$ or $N_{frac,2}$ becomes 0.5 leads to the optimal fractional spur performance in this case. In the second case, $N_{frac,1}$ and $N_{frac,2}$ can be optimized in a similar way until one of $N_{frac,1}$ and $N_{frac,2}$ reaches 0.5. The last two cases correspond to the worst scenarios, where increasing $N_{frac,1}$ causes $L_{spur,1}$ and $L_{spur,2}$ to vary in different directions. In those cases, the optimal $N_{frac,1}$ and $N_{frac,2}$ can be obtained by equating Eq. (3.3) and Eq. (3.4). Fig. 3.5 shows an example with 1 ps $INL_{pp,1}$ and $INL_{pp,2}$, $N_{int,1}$ of 27, $N_{int,2}$ of 10, and N of 138.001. The optimal $N_{frac,1}$ is around 0.361, and $N_{frac,2}$ can be calculated from (3.6), which is 0.0874237.

It worths mentioning that the above analysis tends to over-optimize the fractional spurs from the two loops. As can be seen from the example in Fig. 3.5, when $N_{frac,1}$ changes from 0.2 to 0.5, the amplitude of the strongest fractional spur changes from -81.1 dBc (at $N_{frac,1}$ of 0.2) to -88.7 dBc (at $N_{frac,1}$ of 0.361), corresponding to only 7.6 dB difference. Moreover, as will be discussed in section V, inter-stage coupling can cause spurs that

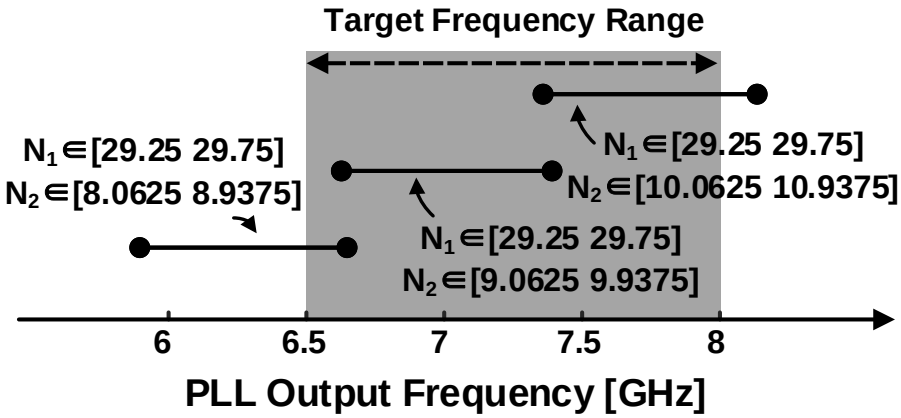


Figure 3.6: The FCW arrangement for fractional spur optimization in the target frequency band.

could be stronger than the fundamental fractional spurs contributed by the two loops. As a result, it is unnecessary to strictly follow the analysis above to select $N_{frac,1}$ and $N_{frac,2}$. Rather, a more practical and simpler method for optimizing FCWs is to set the boundary values of $N_{frac,1}$ and $N_{frac,2}$ such that the fundamental fractional spur power can be limited well below the coupling spur amplitude (-52.7 dBc from the measurement).

The detailed N_1, N_2 arrangement for the target frequency band is shown in Fig. 3.6. In the real implementation, N_1 is always limited between [29.25, 29.75], $N_{frac,2}$ is limited between [0.0625, 0.9375], and $N_{int,2}$ is selected between $\{8, 9, 10\}$ for covering the target output frequency range without any frequency gaps. With the example of 1 ps $INL_{pp,1}$ and $INL_{pp,2}$, this FCW arrangement leads to the worst case $L_{spur,1}$ of around -84 dBc and the worst case $L_{spur,2}$ of around -86 dBc, respectively, which will not limit the fractional spur performance of the implemented cascaded PLL.

3.1.3 Frequency Resolution

One potential issue of cascaded PLL is the degradation of frequency resolution caused by the integer-N stage. For example in the case shown in Fig. 3.1(b), the frequency resolution will be degraded by N_1. Around 4 extra bits in the fractional part of N_2 are needed to compensate for this degradation. When the second stage is working with a high input frequency, considerable power will be consumed because of the extended DSM input length [33, 34].

In the proposed cascaded PLL, both N_1 and N_2 are implemented with 10-bit fractional resolution. The equivalent frequency resolution can thus be easily extended to more than 10-bit with fractional N_1 and N_2. Fig. 3.7 shows the achievable frequency steps across the

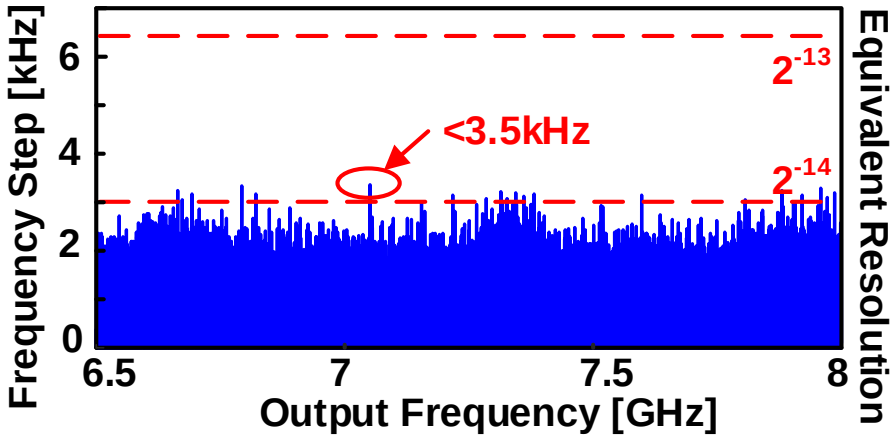


Figure 3.7: The frequency resolution of the proposed cascaded fractional-N PLL.

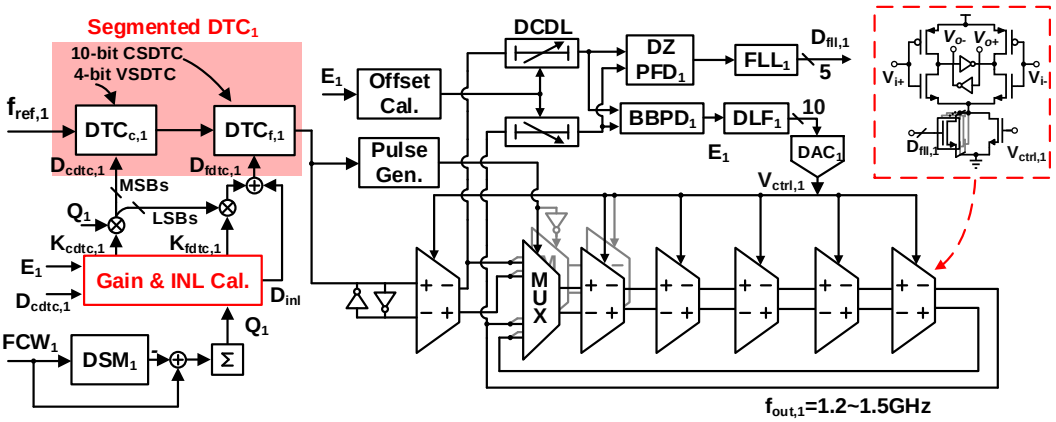


Figure 3.8: Detailed schematic of the first stage MDLL.

output frequency range. Fractional parts of N_1 and N_2 are limited to [0.2, 0.8] and [0.1, 0.9] to avoid low-frequency fractional spurs. The maximum frequency step is less than 3.5 kHz, corresponding to an equivalent resolution of 2^{-13}. Finer frequency resolution can be achieved by further extending the number of bits of the fractional part of N_1, which is easy because of the low operating frequency of the first stage DSM.

3.2 First Stage MDLL Implementation

3.2.1 MDLL Structure

The detailed schematic of the first stage MDLL is shown in Fig. 3.8. The delay cells of RO are designed in a pseudo-differential topology for the robustness against common

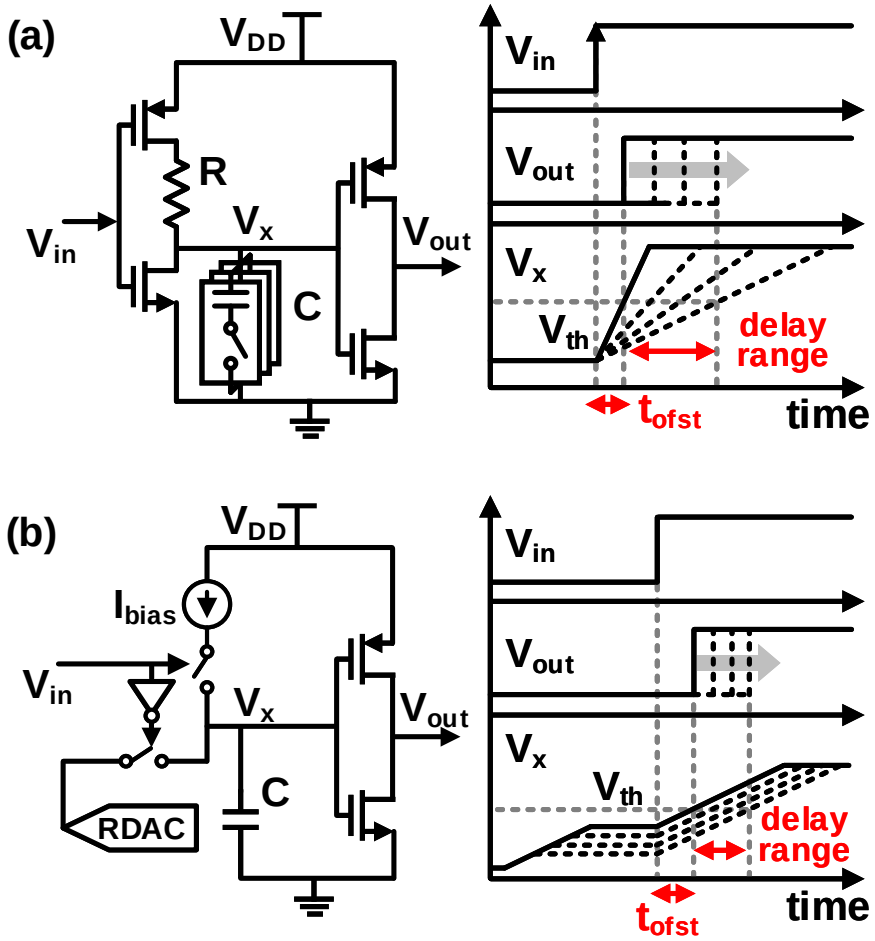


Figure 3.9: The structures and operations of: (a) constant-slope DTC, and (b) variable-slope DTC.

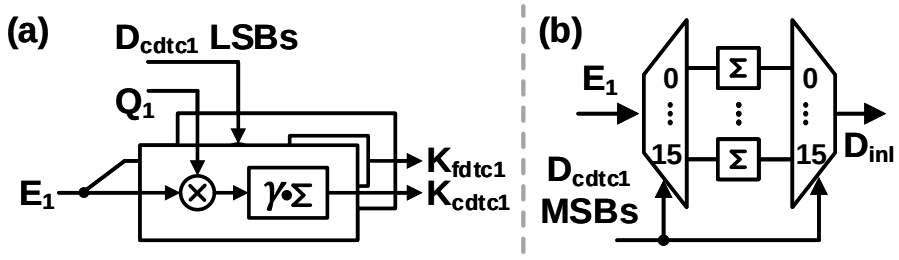


Figure 3.10: The block diagram of gain and INL calibration for segmented DTC.

mode disturbances from the supply. A dummy delay stage is inserted before the multiplexer (MUX) to balance the driving strength of the two pairs of MUX inputs [39], [40]. An FLL is implemented to track the RO frequency, with the output controlling a 5-bit

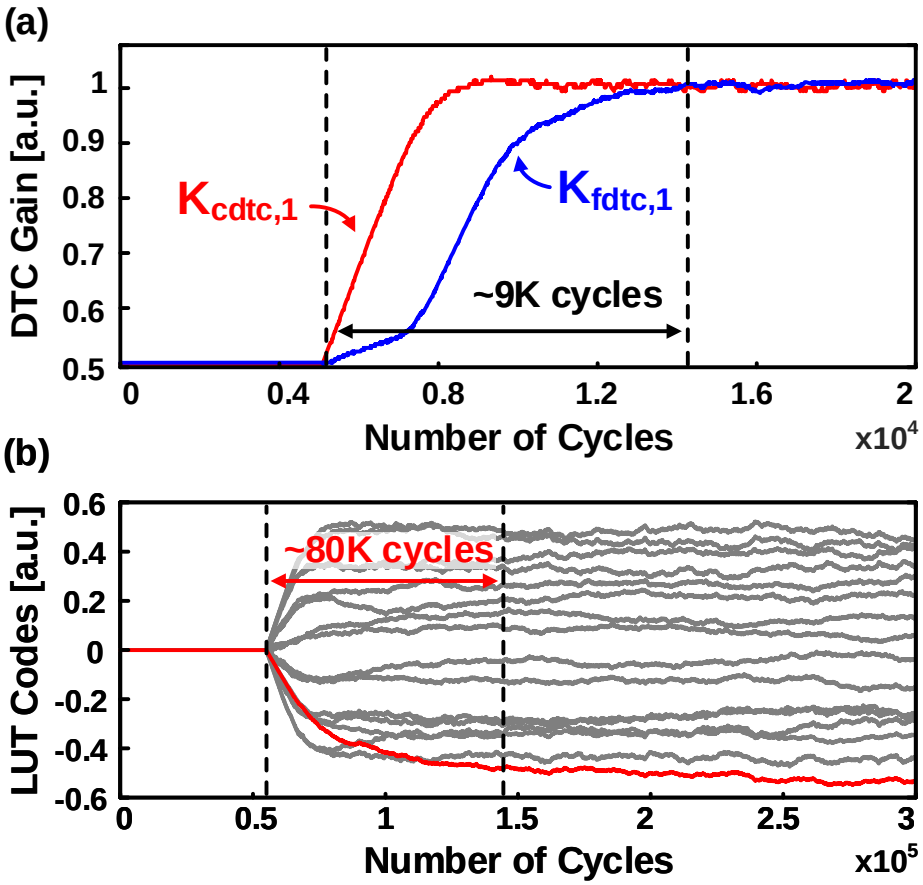


Figure 3.11: Convergence of DTC gain and INL calibrations.

current-starver bank directly [41]. The phase of the RO is tracked by a PLL, which is used to generate a bias voltage through a 10-bit digital-to-analog converter (DAC). A subsampling Bang-Bang phase detector (BBPD) is implemented to reduce the delay mismatch between the phase-tracking path and the edge-multiplexing path to reduce the reference spur and phase noise degradation at low offset frequencies. The residual delay mismatch is calibrated with a method similar to the one in [24].

A 1st order DSM is implemented for division ratio and DTC control to suppress the phase noise induced by long DTC range, which is required by higher-order DSMs [42]. The gains of the coarse and fine DTCs are calibrated in the background by an LMS-based calibrator [4], which is shown in Fig. 3.10(a). One may worry about the convergence time of DTC gain calibration, which is usually long for near-integer FCWs. In fact, near-integer FCWs are avoided in the proposed PLL, and thus will not cause any convergence issue in the DTC gain calibration. The simulated convergence procedure of DTC gain calibration at a fractional channel with $N_{frac,1}$ of 0.126 (2^{-3}+2^{-10}) is shown in Fig. 3.11(a). It can be seen that the DTC_1 gain calibration can converge within 9 thousand of reference

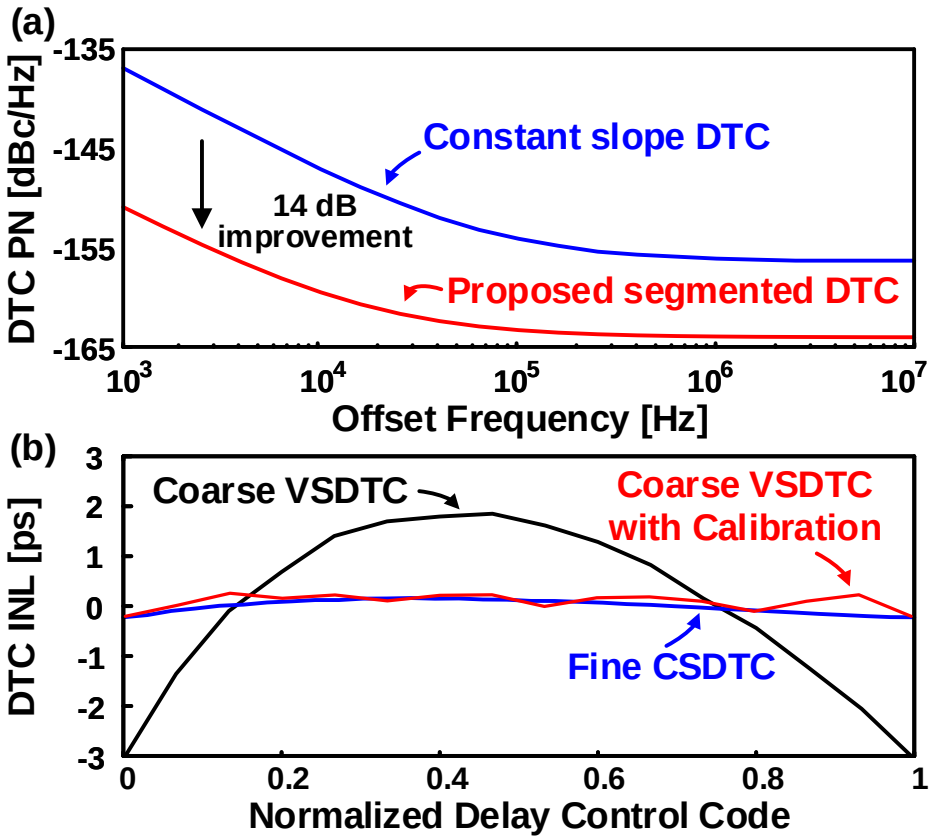


Figure 3.12: Simulated INL and phase noise of proposed segmented DTC.

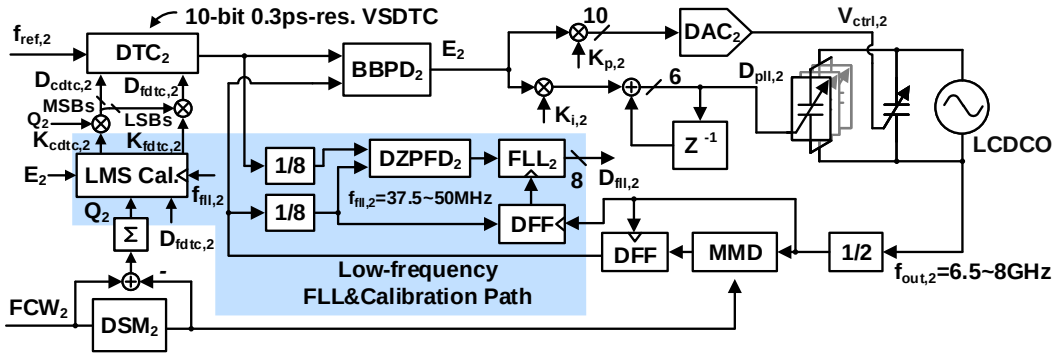


Figure 3.13: Schematic of the second stage type-II DPLL.

cycles, corresponding to 0.18 ms under 50 MHz $f_{ref,1}$. The initial gain erros are 20% for both coarse and fine DTCs in the simulation.

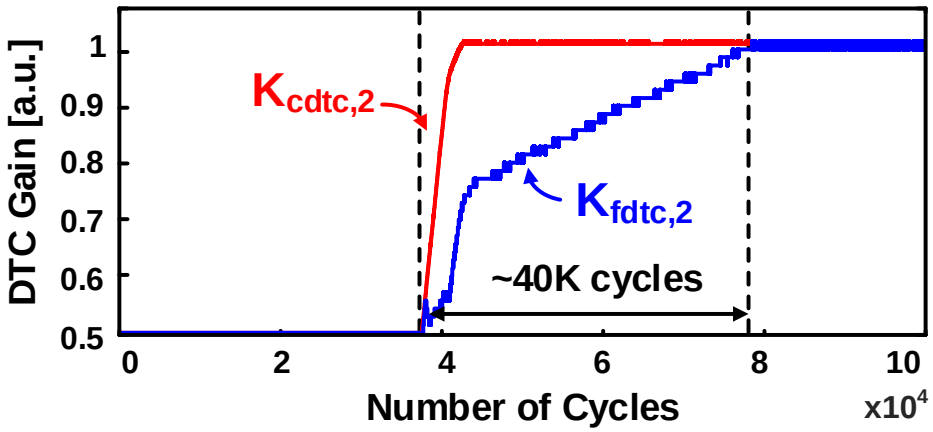


Figure 3.14: Convergence of DTC_2 gain calibration.

3.2.2 Segmented DTC with INL Calibration

One important observation can be made from equations (3.3) and (3.4). For fractional spurs generated in each stage, the spur power is proportional to the amplitude of INL, indicating that the linearities of DTC_1 and DTC_2 are "equally" important. However, the delay range of DTC_1 is longer than that of DTC_2, leading to a potentially worse linearity. For a stronger suppression in fractional spur power, DTC_1 needs to be designed with cautiousness.

Among conventional DTC structures, constant-slope DTC (CSDTC) can achieve the best INL performance by eliminating the charging-slope dependent nonlinearity generated at the comparator [18, 21]. However, to avoid the linearity degradation in the bias current source, the maximum pre-charging voltage must be kept low, resulting in a long delay offset, and thus worse phase noise. On the other hand, the delay offset in a variable-slope DTC (VSDTC) is only limited by the parasitic capacitance at the input node of the comparator, which is favorable in suppressing DTC phase noise [4, 43]. Nevertheless, the INL is heavily limited by the slope-dependent nonlinearity in this kind of DTCs.

To relax the stringent noise-linearity trade-off in DTC_1, a segmented DTC structure is implemented, which is shown in Fig. 3.10. The coarse stage employs a 4-bit VSDTC with the resolution of 80 ps and range of around 1.2 ns for safely covering the RO period (no more than 833 ps) across PVT variations. The fine stage employs a 10-bit CSDTC with the resolution of 0.2 ps and range of 200 ps to cover more than 2 LSBs of the coarse DTC delay, which can guarantee enough margin for further INL calibration on the coarse stage. In this way, the delay offset in CSDTC can be reduced to less than 100 ps, and thus will not limit the phase noise performance of the whole DTC_1. To mitigate the bad nonlinearity in the coarse VSDTC, a piecewise-linear (PWL) INL calibration

similar to [24] is implemented. The detail of the INL calibration block is shown in Fig. 3.10(b), where 15 accumulators in the look-up table (LUT) are utilized to learn the shape of coarse DTC INL. The simulated INL of both of the two stages is shown in Fig. 3.12. It can be seen that after the PWL INL calibration, the peak INL of the proposed segmented DTC can be suppressed to around 600 fs (0.05% full scale). The post-layout simulation of the phase noise of the proposed segmented DTC and a CSDTC with the same delay range is also shown in Fig. 3.12, a larger than 14 dB improvement in phase noise can be achieved. The convergence of PWL INL calibration is simulated and shown in Fig. 3.11(b). Around 80 thousand reference cycles (1.6 ms) are needed for the LUT to coverge so that the maximum redisue INL from the coarse stage can be less than the peak INL from the fine stage. The convergence is simulated at a $N_{frac,1}$ of 0.126 (2^{-3}+2^{-10}).

3.3 Second Stage DPLL Implementation

3.3.1 Type-II DPLL Structure

A type-II DPLL is implemented as the second stage, which is shown in Fig. 3.13. The major design concern in the second stage is to reduce the potentially high power consumption induced by the high input frequency. To this aim, the proportional path and integral path of the loop filter are separated in the analog domain. The proportional path controls a 10-bit DAC directly, which is used to tune the bias voltage of the varactor in the LCDCO. The integral path controls a 6-bit capacitor bank. In this way, the multi-bit multiplication and summation operations can be avoided in the DLF, leading to less power consumption at high clocking frequencies. Moreover, the reference and feedback signals are divided by 8 before being fed into the FLL_2, so that FLL_2 is working with a less than 50 MHz frequency. The divided-by-8 feedback signal is further retimed to generate $f_{fll,2}$ to clock-gate the DTC gain calibration block for more power reduction.

A current mode logic (CML) divide-by-2 circuit is inserted between the MMD and DCO to prevent the potential malfunctions of MMD under high input frequency. Similar to the first stage, a first-order DSM is used for MMD and DTC control. Because of the CML, the delay range of DTC_2 needs to be two LCDCO periods, which is around 300 ps. One may want to implement a CSDTC in the second stage for better linearity. However, a long time is required for the pre-charging voltage to be well settled, which hinders the implementation of CSDTC at high input frequencies. As a result, a VSDTC with a 5-bit coarse capacitor bank and a 5-bit fine capacitor bank is implemented as DTC_2. The coarse and fine gain calibrations of DTC_2 is shown in Fig. 3.14, where $N_{frac,2}$ is set to 0.03125, and the initial gain errors are set to be 20% for both the coarse and fine DTC banks. It

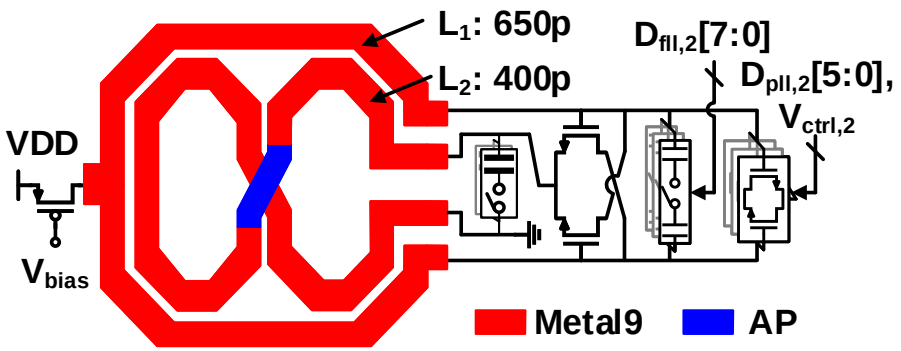


Figure 3.15: Schematic of the implemented DCO with 8-shaped tail inductor.

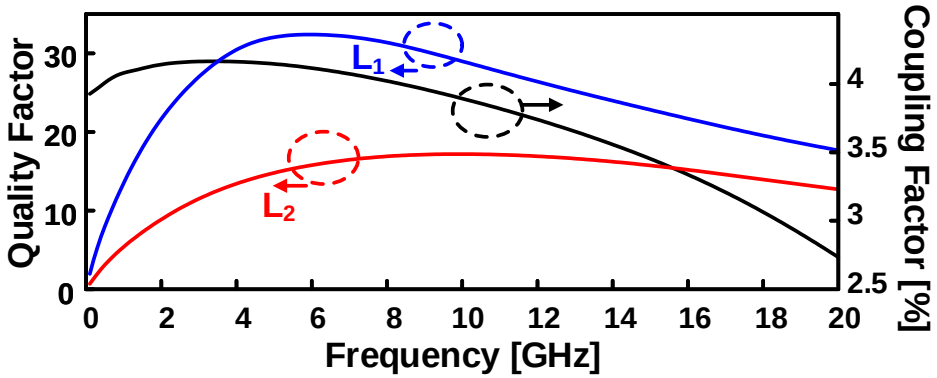


Figure 3.16: Simulated Q factors and coupling factor of the two inductors in the LCDCO.

takes around 40 thousand cycles for the coarse DTC gain calibrations to converge, which corresponds to 1.07 ms when the calibration clock frequency is 37.5 MHz.

3.3.2 Low-Phase-Noise Class-B DCO

To avoid the jitter degradation from DCO under a narrow $f_{bw,2}$, a class-B DCO with a second-order harmonic tail resonator is implemented to suppress the flicker noise up-conversion [44]. The detailed schematic of the DCO is shown in Fig. 3.15. Similar to [42], the tail inductor is designed to be 8-shaped and placed inside the main inductor to avoid extra area overhead and to improve the isolation. According to the EM simulation result, the primary inductor shows an inductance of L_1 = 650 pH, and the secondary inductor shows an inductance of L_2 = 400 pH. The simulated Q factors of L_1, L_2 and the coupling factor between them are shown in Fig. 3.16. It can be seen that the coupling factor is less than 3.5%, indicating a good isolation between L_1 and L_2. Because there is no metal overlap in L_1, the Q factor of L_1 can be larger than 30 across the DCO frequency range, which can further benefit the phase noise of the DCO.

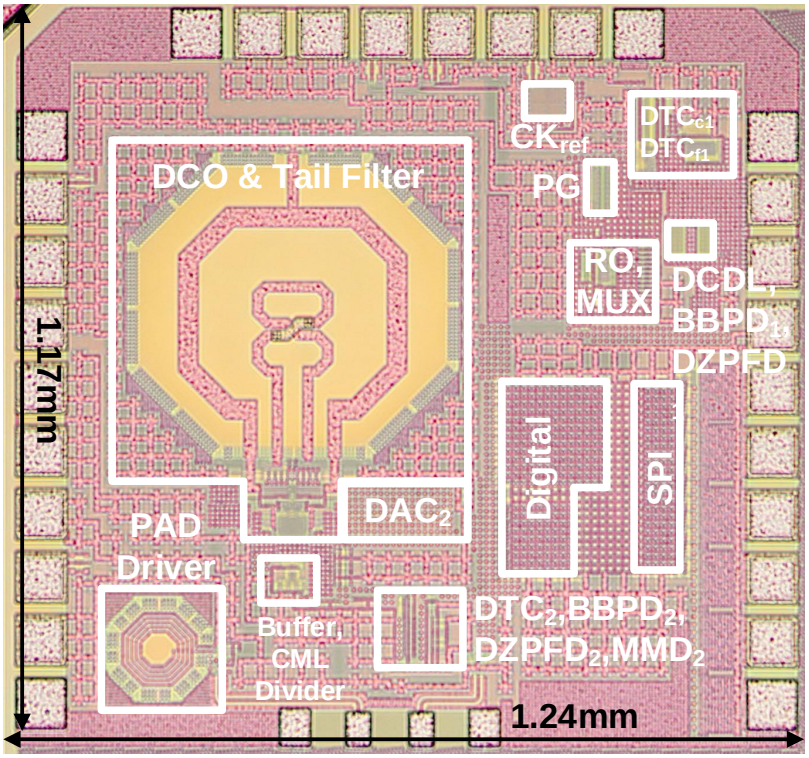


Figure 3.17: Die micrograph of the proposed cascaded dual-fractional-N PLL.

3.4 Measurement Result

Fig. 3.17 shows the die micrograph of the proposed cascaded PLL, which is implemented in 65nm CMOS process. The core area occupies 0.48 mm^2. The 50 MHz reference for the implemented cascaded PLL is generated by Rhode&Schwartz SMA100B. The phase noise spectrum is measured by a signal source analyzer (Keysight E5052B). The spectrum is measured by a spectrum analyzer (Anritsu MS2830A).

The first stage MDLL consumes totally 5.79 mW. The power breakdown is as follows: the segmented DTC consumes 0.4 mW, the DCDL for phase offset calibration consumes 0.05 mW, the divider for frequency tracking and for generating the input for the second stage PLL consumes 0.91 mW, the RO and the MUX for edge injection consumes 4.24 mW, the digital logics consume 0.16 mW, and the $BBPD_1$ consumes 0.03 mW. The phase noise spectrum of the MDLL at a near-integer channel of N_I = 29.001 is shown in Fig. 3.18. The integrated jitter from 10 kHz to 10 MHz is 611.4 fs when the MDLL frequency is 1.45005 GHz. The fractional spur level is also measured. As shown in the same figure, the fractional spur level can be suppressed from -45.12 dBc to -62.94 dBc with the PWL INL calibration. The peak-to-peak INL of the segmented DTC after PWL INL calibration can be estimated as 314 fs, corresponding to around 0.045% of the whole DTC tuning

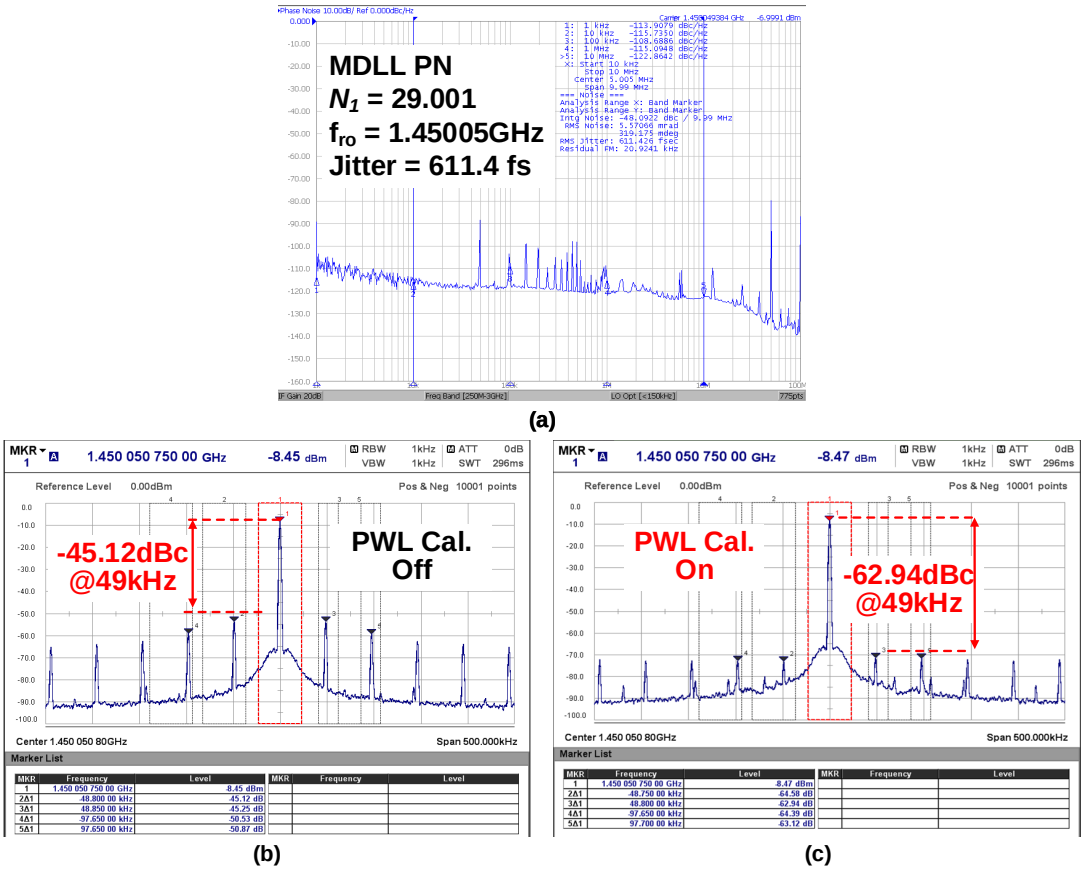


Figure 3.18: Measured: (a) MDLL phase noise at a near-integer channel, (b) MDLL fractional spur without PWL calibration, and (c) MDLL fractional spur with PWL calibration

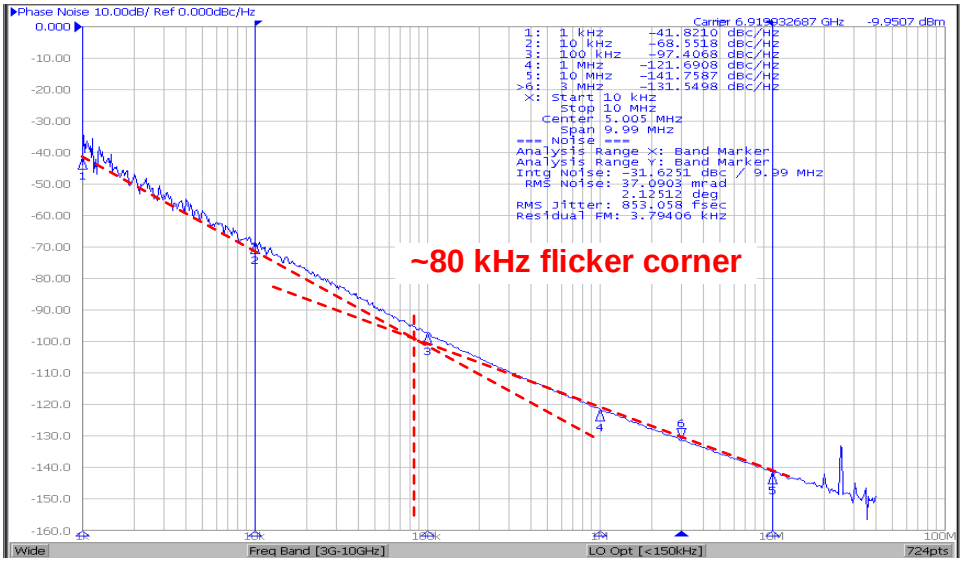


Figure 3.19: The phase noise spectrum of LCDCO in freerun.

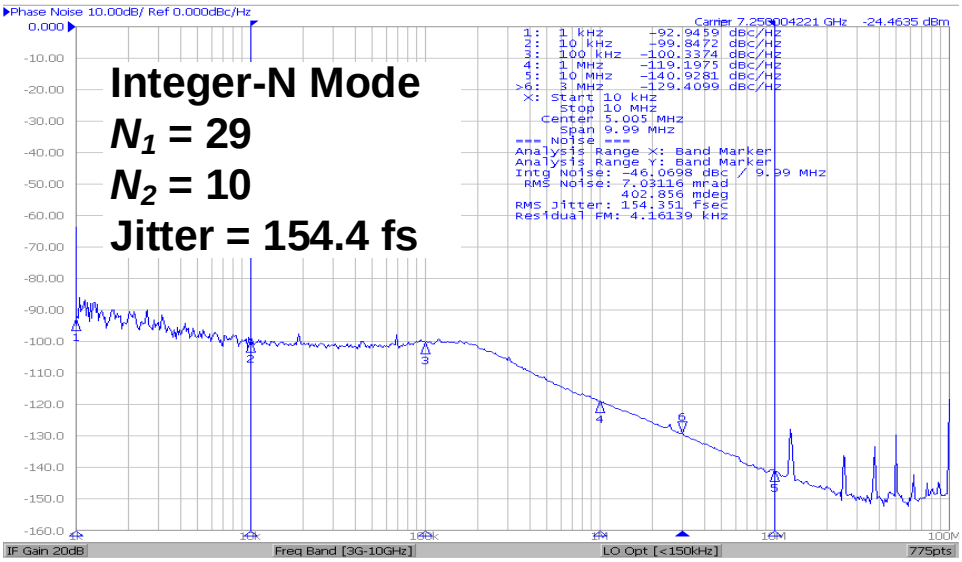


Figure 3.20: Measured phase noise spectrum of the cascaded PLL in integer-N mode at 7.25 GHz.

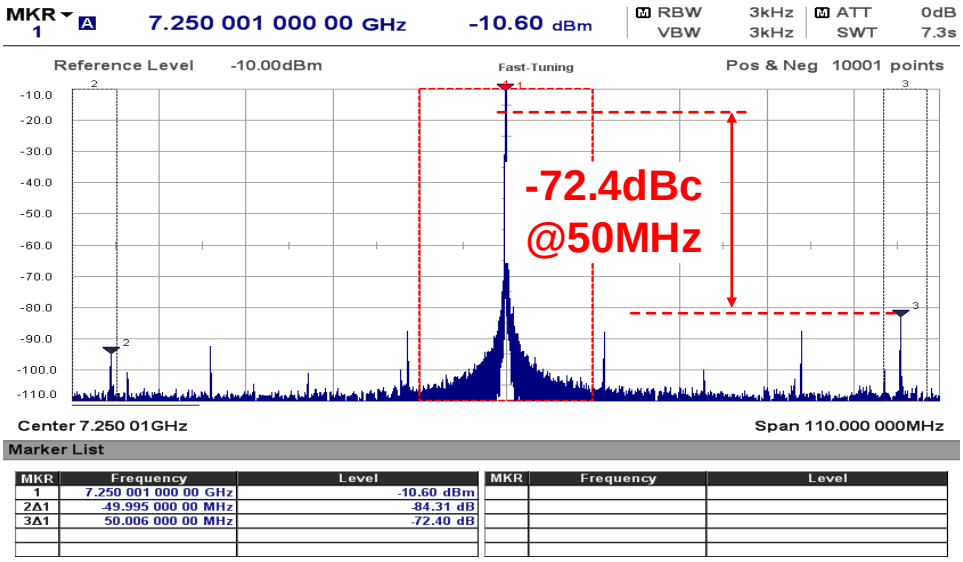


Figure 3.21: Measured reference spur level of the cascaded PLL.

range.

The second stage type-II DPLL consumes 8.4 mW. The second stage DTC consumes 0.55 mW, the CML divider and the MMD in the second stage consume 3.19 mW together, the LCDCO consumes 3.76 mW, the $BBPD_2$ consumes 0.07 mW, the digital circuits in the second stage consume 0.83 mW. The measured phase noise of the LCDCO is shown in Fig. 3.19. Thanks to the high-Q single-turn inductor and the tail filter, the flicker corner is as low as around 80 kHz. The phase noise at 1 MHz offset is -121.69 dBc/Hz, leading to an FoM of -192.7 dBc/Hz at 6.92 GHz oscillating frequency. The phase noise of the

cascaded PLL in integer-N mode is shown in Fig. 3.20, where N_1 is set to 29, N_2 is set to 10. It can be observed that the bandwidth of the second stage PLL is around 200 kHz. Thanks to the low-noise LCDCO, the integrated jitter from 10 kHz to 10 MHz can be 154.4 fs at a 7.25 GHz output frequency. The reference spur is also measured, which is -72.4 dBc as shown in Fig. 3.21.

The phase noise of the cascaded PLL at a near-integer channel is shown in Fig. 3.22(a), where N_1, N_2 are set to 29.3671875 and 9.875, leading to a cascaded PLL output frequency of around 7.250024 GHz. The integrated jitter is 190.8 fs, which is mainly degraded by the coupling spurs that fall within the loop bandwidth. The worst spur strength is measured in Fig. 3.22(b), which is -52.79 dBc at 24 kHz offset frequency. For spurs that are located out-of-band, the amplitudes are all below -63.7 dBc, as shown in Fig. 3.22(c).

The coupling spurs are mainly caused by the DTC_1 supply ripples that are induced by the LCDCO and the CML pre-scaler [19]. Because the working frequency of DTC_1 is 50 MHz, the supply ripple component at the LCDCO frequency of 7.250024 GHz is aliased to 24 kHz at the DTC_1 output, which leads to the worst fractional spur reported above. In order to illustrate the generation of coupling spurs, the MDLL output spectrum at N_1 of 29.3671875 is measured before and after turning on the second stage DPLL. It can be seen from Fig. 3.23 (a) that there are no spur at 24 kHz when the second stage DPLL is off. After turning on the second stage DPLL, fractional spurs appear at $\pm$24 kHz offset frequencies due to the EM coupling from the LCDCO and CML pre-scaler, as shown in Fig. 3.23(b). The coupling spur amplitude at the MDLL output is -67.05 dBc. After being referred to the LCDCO frequency, it becomes -67.05 + $20\log_{10}(7.25/1.47) \approx$ -53.2 dBc, which matches with the measured 24 kHz spur of -52.79 dBc amplitude at the second stage DPLL output.

Moreover, due to the other nonlinearities from the circuits such as LCDCO, BBPD, *etc.* the fractional spurs may appear at any frequencies that are multiples of 24 kHz. On the other hand, the spurs in the test environment might also be mixed with the coupling spurs, leading to various possible spur positions. However, those spurs are only significant when the offset frequencies are within the second stage DPLL loop bandwidth. It also needs to be clarified that those coupling spurs can be potentially improved by increasing the physical distance between different block circuits, or utilizing on-chip low-dropouts (LDOs) for improving the DTC supply resilience. Most importantly, the coupling spurs generally exist in multi-PLL systems, and is not related to the utilization of two fractional FCWs. Rather, in conventional fractional-N-integer-N cascaded PLL, the coupling spur could be worse when a near-integer channel is being synthesized.

The cascaded PLL with different N_1 and N_2 configurations are measured for a com-

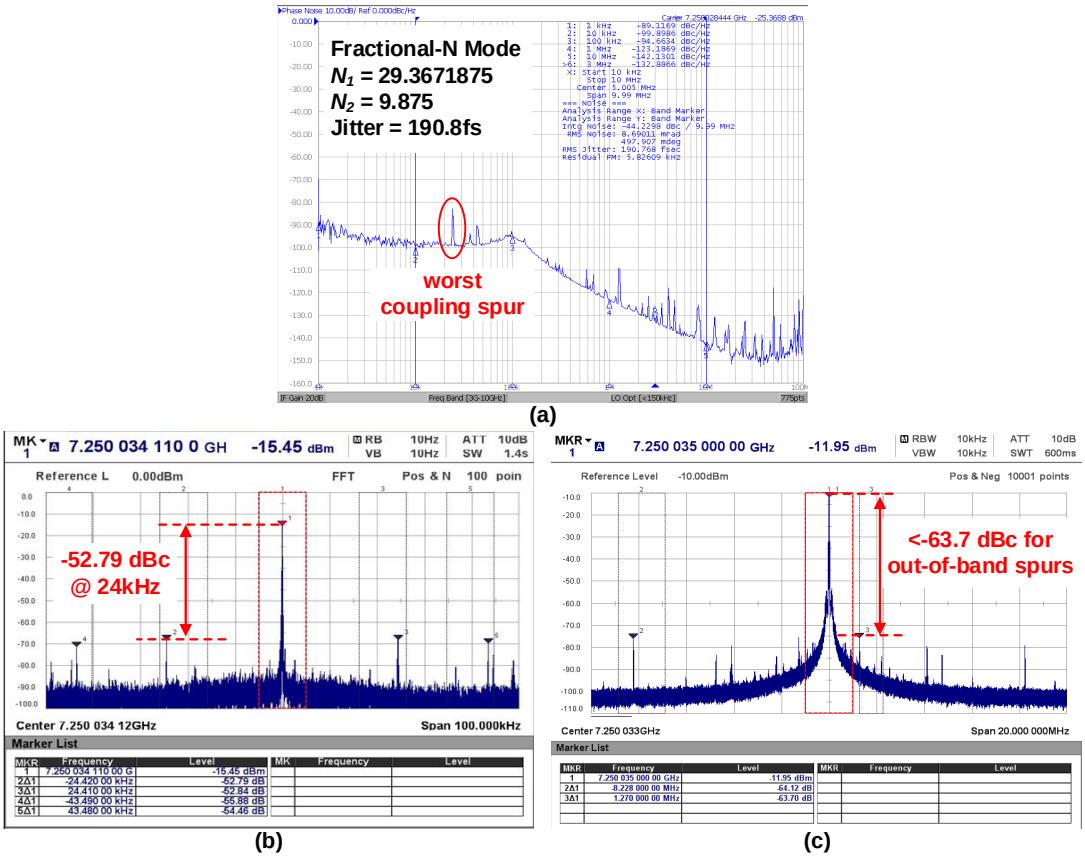


Figure 3.22: Measured (a) phase noise and (b),(c) spur performance at different offset frequencies of the cascaded PLL in a near-integer channel nearby 7.25 GHz.

parison. It can be seen in Fig. 3.24(a) that when N_1 of 29.001 (29 + 2^{-10}) and N_2 of 10 are adopted, the cascaded PLL generates a frequency of 7.25 GHz + 244 kHz. The worst fractional spur is measured to be -37.5 dBc, which is worse than simply elevating the previously measured -62.94 dBc MDLL spur level by $20\log_{10}(7.25/1.45)$ (resulting in -48.9 dBc). This implies that a more severe degradation caused by the inter-stage coupling can happen when a conventional cascaded PLL is utilized. The output spectrum with N_1 of 29.3681640625 and N_2 of 9.875 is shown in Fig. 3.24(b), where the output frequency is 7.25 GHz + 265 kHz. The cascaded PLL frequency is deliberately controlled to be close to the scenario in Fig. 3.24(a), with a frequency difference of around 21 kHz, which is limited by the FCW resolutions. It can be seen that the worst spur level can be less than -53 dBc when the two fractional FCWs are utilized.

The cascaded PLL is also measured with integer-N-fractional-N cascading scheme, which is shown in Fig. 3.25(a). N_1 of 29 and N_2 of 10.001 (10 + 2^{-10}) are utilized to generate a frequency of 7.25 GHz + 708 kHz. The measured worst fractional spur is -45.1 dBc at 354 kHz offset, which is generated by the DTC_2 working at a fractional

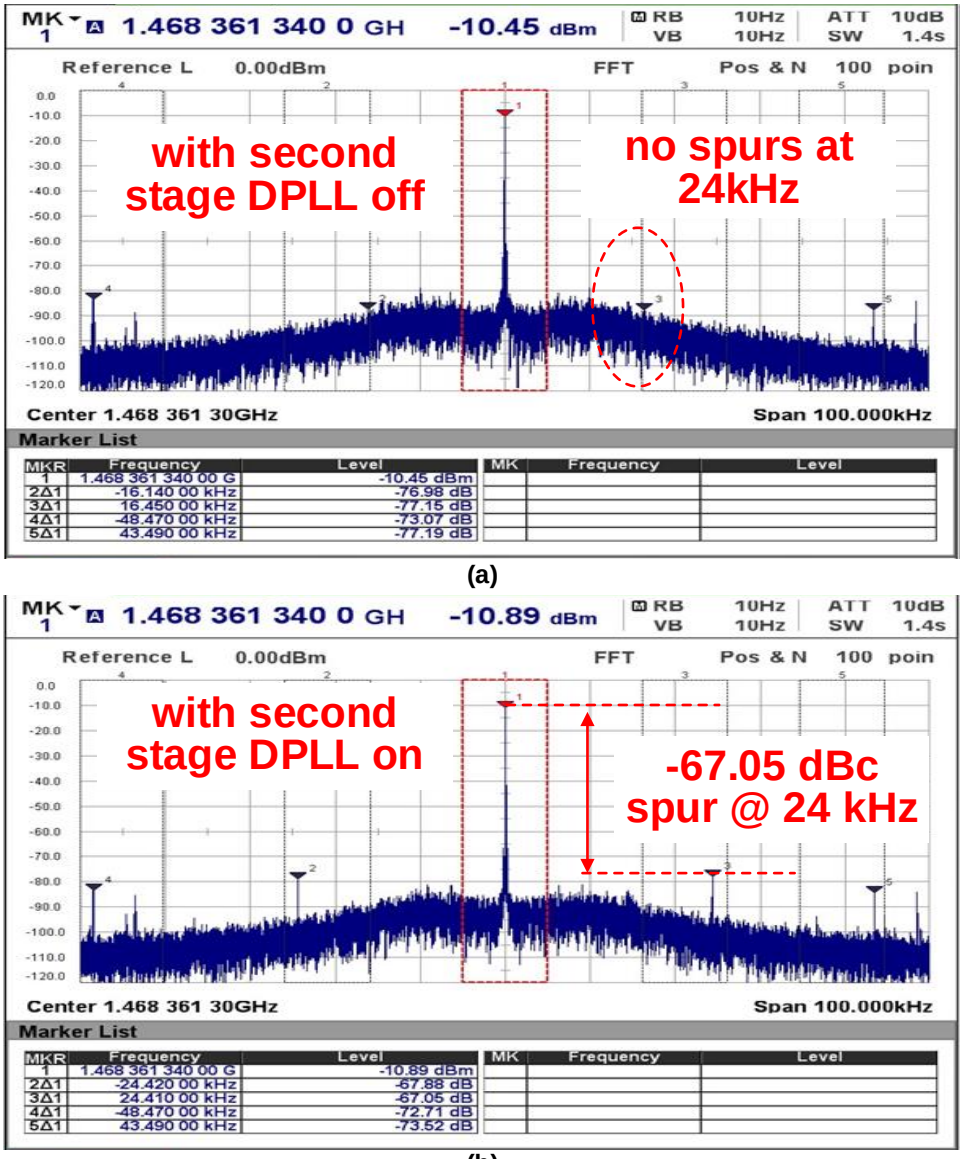
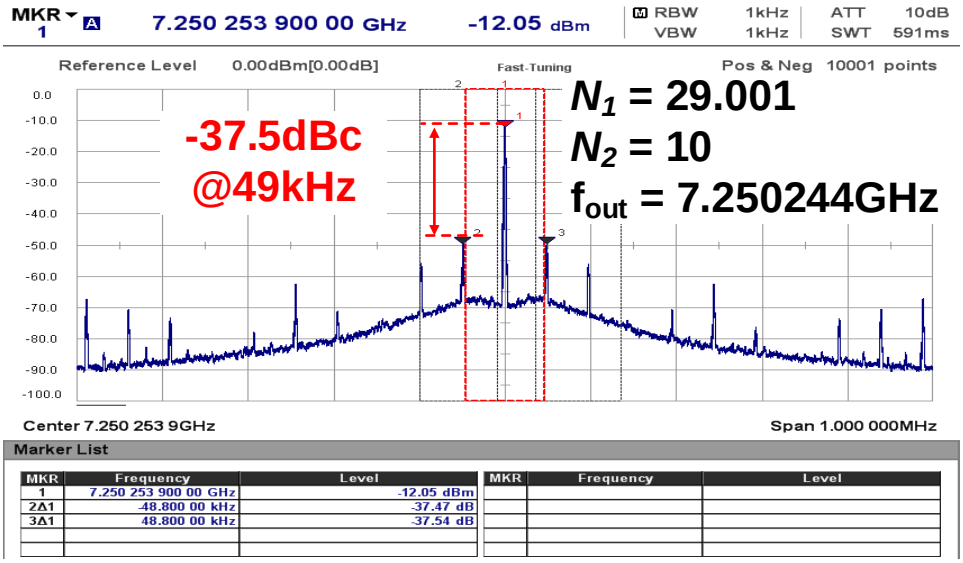


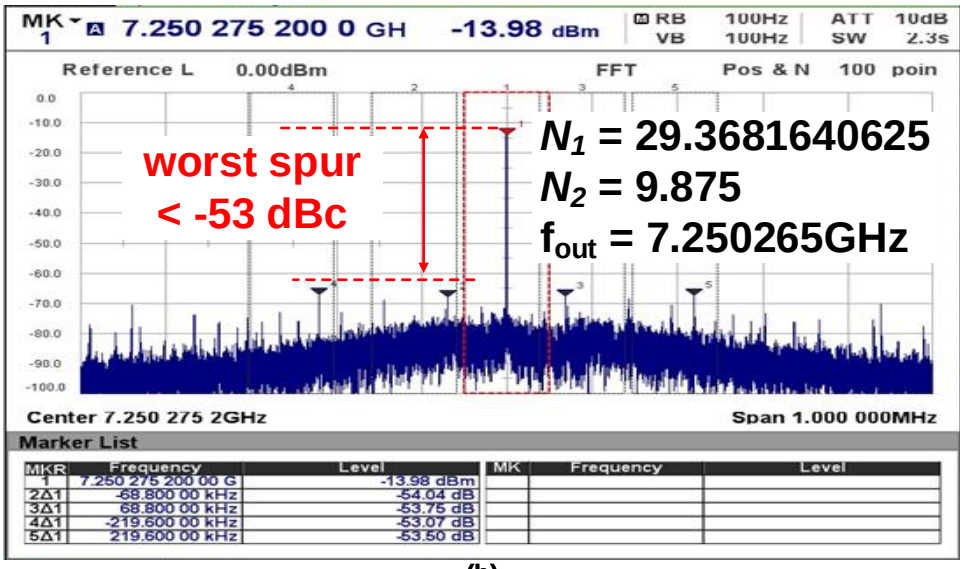
Figure 3.23: Measured spur performance with N_1 of 29.3671875 (a) before and (b) after turning on the second stage DPLL.

frequency of $29/4 \times 2^{-10} \times 50 = 0.354$ MHz. As a comparison, N_1 of 29.3583984375 and N_2 of 9.87890625 are used for generating an output frequency of 7.25 GHz + 722 kHz, which is close to the PLL frequency in Fig. 3.25(a). The measured spurs are all below -59.5 dBc, which is better than the conventional integer-N-fractional-N case.

For a fair comparison with conventional cascaded PLLs, the worst-case fractional spurs at near-integer channels across the target frequency range is measured. The results are summarized in Fig. 3.26. It can be seen that when the cascaded PLL is configured in the conventional fractional-N-integer-N scheme, the worst-case fractional spurs are



(a)

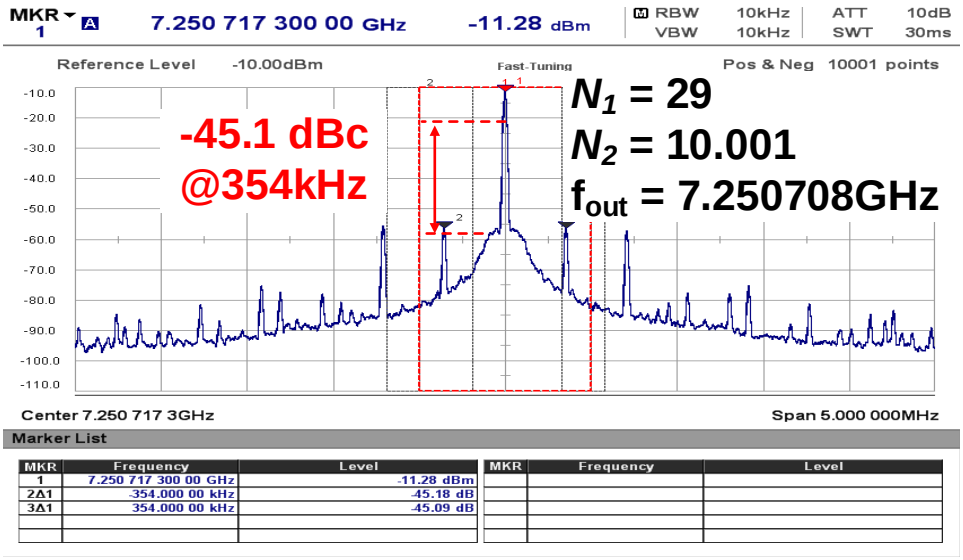


(b)

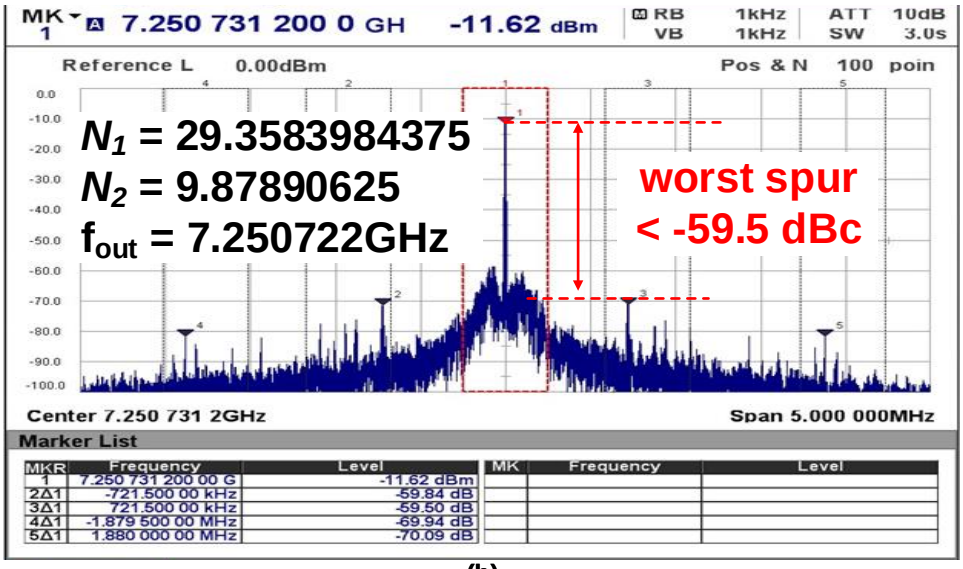
Figure 3.24: Fractional spur of the cascaded PLL when (a) N_1 = 29.001, N_2 = 10; (b) N_1 = 29.3681640625, N_2 = 9.875.

always larger than -37.8 dBc. It needs to be clarified that due to the limited fractional resolution of N_2, the worst case fractional spurs generated in integer-N-fractional-N mode cannot be located in-band. This results in a better worst-case fractional spur power of -46.7 dBc compared with the fractional-N-integer-N mode. On the other hand, thanks to the avoidance of near-integer N_1 and N_2, the worst-case fractional spurs in the proposed dual-fractional-N cascaded PLL can always be less than -52.79 dBc.

A comparison with other PLLs is shown in table 3.1, [22, 31, 33, 34, 39, 45–49]. The proposed cascaded PLL yields an integrated jitter of 191 fs with a power consumption of



(a)



(b)

Figure 3.25: Fractional spur of the cascaded PLL when (a) N_1 = 29, N_2 = 10.001; (b) N_1 = 29.3583984375, N_2 = 9.87890625.

14.2 mW. The FoM of the proposed PLL is -242.9 dB, which is in-line with recent PLLs using less than 100 MHz f_{ref}. Compared to other PLL architectures, the proposed PLL can avoid fractional spur degradation at near-integer output frequencies by combining two far-integer FCWs. When normalizing the fractional spur to 1 GHz, the proposed cascaded PLL can achieve one of the best fractional spur performance among DPLLs with less than 100 MHz f_{ref}. Further fractional spur suppression is possible by improving the isolation condition of the DTC_1, which can be achieved by the integration with on-chip LDOs or increasing the physical distance between the DTC_1 and the LCDCO. Moreover, for the

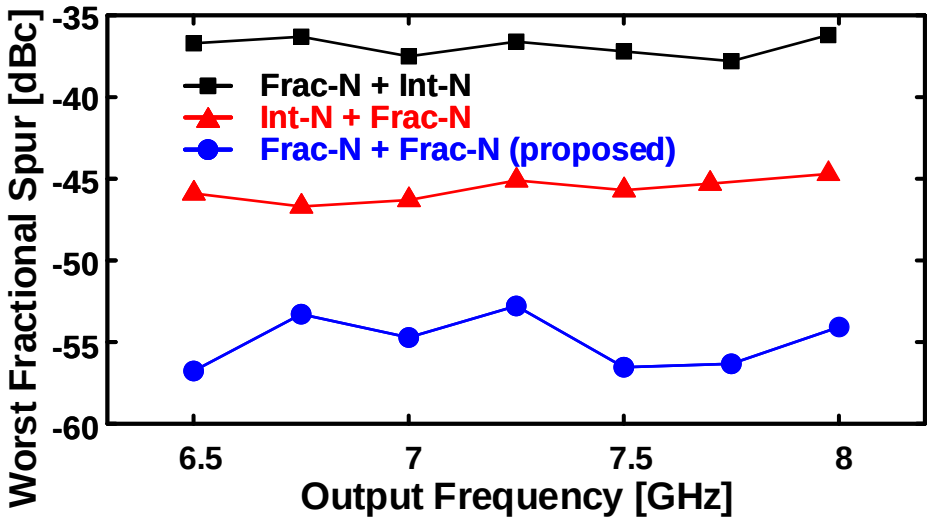


Figure 3.26: Measured worst-case fractional spur levels when the cascaded PLL is set to different cascading schemes at different near-integer channels.

precise loop bandwidth control in the second stage DPLL, which might be affected by the degraded BBPD gain when a near-integer channel is being synthesized, digital loop bandwidth calibration technique in [50, 51] can be readily applied.

3.5 Summary

In this chapter, a cascaded DPLL for fractional spur suppression is introduced. The cascaded DPLL employs two stages of fractional-*N* MDLL/PLL, such that the fractional spur degradation at near-integer channels can be avoided. This characteristic is achieved by carefully setting the two FCWs such that the fractional spurs generated in the two stages can be pushed to high frequencies, by which those spurs can be filtered by the low-pass transfer function of the PLL. It is worth mentioning that this proposed technique is not exclusive to the conventional dither or DPD-based fractional spur suppression techniques. Rather, those techniques can also be comnbined with the dual-fractional-*N* cascaded PLL when extremly low fractional spur level is required by the system specifications.

On the other hand, the cascaded DPLL can still be improved in the following aspects for further PN/ fractional spur performance improvement:

1. The DTC in the first stage is implemented to cover a wide delay range of $\approx$ 800 ps, which causes a potentially high phase noise. To mitigate this issue, the frequency of the first stage RO can be redesigned to be higher, *e.g.,* 5 GHz. In this way, the

required DTC_1 delay range can be 200 ps, which can benefit in a lower phase noise and INL amplitude.

2. The DTCs in the two stages are both prone to supply disturbance, which can come from the two oscillators, the output buffers, and the input reference buffer, *etc.* Meanwhile, the RO itself exhibit a poor supply pushing performance (K_{VDD} can be larger than 1 GHz/V). As a result, the isolation between two satges needs to be improved. For example, the ground and supplies of the two stages need to be separated, which can lead to a less inter-stage coupling and thus less spur/ PN degradation at the final output of the PLL.

3. Supply regulators such as low-dropouts (LDOs) can be integrated on-chip for generating clean supplies for different blocks. This method can generally improve the circuits robustness against noisy supplies. It needs to be mentioned that LDOs also contribute noise. As a result, they need to be implemented carefully in order not to degrade the PLL IPN. Moreover, other alternative methods might be adopted, which will be introduced in the next two chapters.

Table 3.1: Performance Comparison with Other PLL Structures.

	This Work	JSSC'23 Y. Jo	JSSC'12 D. Park	JSSC'17 L. Kong	JSSC'22 D. Yang	JSSC'23 M. Osada	JSSC'21 W. Wu	JSSC'23 D. Murphy	JSSC'23 Z. Gao	JSSC'23 S. Dartizio	JSSC'24 Q. Zhang
Structure	Cascaded Frac+Frac	Cascaded Frac+Sub-Int	Cascaded Int+Frac	Cascaded Int+Frac	Dual-Loop HM-PLL	Dual-Loop Dual-FB	SPLL	APLL	DPLL	DPLL	MDLL
Process	65nm	65nm	130nm	45nm	7nm	65nm	14nm	7nm	40nm	28nm	65nm
f_{out} [GHz]	6.5~8	0.6~7.7	2.9~4	2.3~2.6	25~28	2.9	6.2	4.66~5.22	2.56~4.1	9.25~10.5	1.5
f_{ref} [MHz]	50	150	50	22.6	74	40	76.8	79.96	40	250	50
Integrated Jitter [fs] Integration Range [Hz]	191 [10k~10M]	135 [1k~100M]	255 [100~40M]	1680 [10K~50M]	88 [10k~40M]	869 [1k~100M]	93.2 [10k~40M]	154 [10k~100M]	182 [10k~40M]	76.7 [10k~100M]	800 [10k~10M]
Ref. Spur [dBc]	-72.4	-77	-87	-70	-83	-65	-66	-70	-73.5	-70.5	-58
Frac. Spur [dBc]	-52.7	-51	-53.9	-52.5	-70**	-49	-66.4***	-60	-59	-71.9	-67
Frac. Spur Normalized to 1GHz [dBc]	-69.9	-68.1	-62.4	-60.1	-98.9**	-58.25	-82.2	-73.7	-67.5	-91.2	-70.52
Power [mW]	14.2	17.9	14.2	6.4	12.9	15.38	14.2	1.11	3.48	17.2	13.56
FoM* [dB]	-242.9	-244.9	-240.3	-227.4	-250	-229.4	-249.1	-255.8	-249.4	-250.6	-230.6
Core Area [mm^2]	0.48	0.64	0.26	0.03	0.24	0.112	0.31	0.21	0.31	0.33	0.23

*FoM = $20\log_{10}$(RMS Jitter/1s) + $10\log_{10}$(Power/1mW) **Ignoring coupling spurs ***Normalized to PLL frequency

Chapter 4

A DPD/Dither-Free DPLL

The cascaded dual-fractional-*N* DPLL introduced in the last chapter can avoid fractional spur degradation at near-integer channels by the combination of two far-integer FCWs. Note that although a ZOI PWL calibration was used to improve the first stage DTC linearity, it can be easily avoided by adopting a high-frequency RO in the first stage, which can reduce the required DTC delay range and the amplitude of the DTC INL. As a result, the potentially long time for the LUTs to update can probably be mitigated with this technique. On the other hand, no dithering is adopted in the cascaded dual-fractional-*N* DPLL, which can benefit in achieving an overall improvement in the DPLL IPN (recall in Chapter 2 that dithering only spread the spur power into a wider frequency range).

However, one more PLL is required in the cascaded dual-fractional-*N* DPLL. Considerably high power consumption is needed for the extra stage, which is the reason why the FoM is limited to -242.9 dB. Moreover, the on-chip isolation becomes important to achieve a better fractional spur and phase noise performance, which is hard to achieve when the chip area specification is tight.

To achieve extremly low fractional spur and low phase noise within limited chip area while avoiding the implementation of the time-consuming DPD, this cahpter presents a DPD/dither-free DPLL. The DPLL is based on two novel techniques: the cascaded fractional divider technique, and the pseudo-differential DTC (PD-DTC) technique.

4.1 Cascaded Fractional Divider

4.1.1 Cascaded Fractional Divider Concept

Despite the moderate FoM, a new yet important concept is hidden behind the the cascaded dual-fractional-*N* DPLL: the fractional spurs at near-integer channels can be suppressed if these spurs can be pushed to higher frequencies. This concept is also possible to be

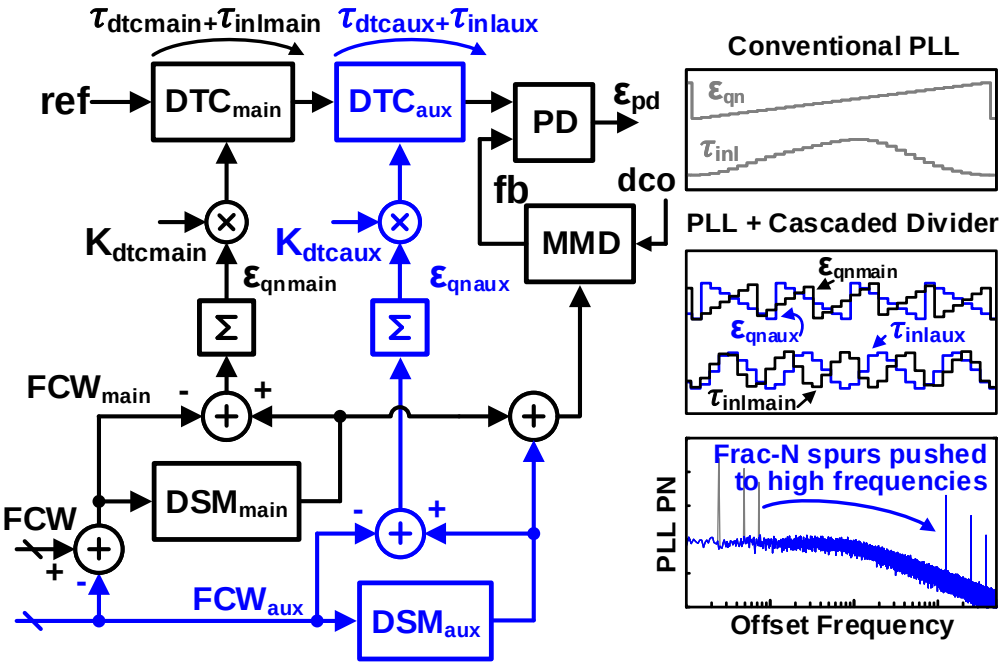


Figure 4.1: The schematic and operation of the proposed cascaded fractional divider technique.

realized within only one PLL. For example, in [52], an offset was added to the DSM of a charge pump (CP) PLL to shift the accumulated QN pattern to a higher frequency. However, the employed PD faced a wider input range because of the offset frequency, which resulted in a degraded PD linearity. Meanwhile, the mechanisms of the fractional spur generation by PD nonlinearity and DTC nonlinearity, which will be disclosed later, are different, hindering the direct application of this technique to a DPLL.

As shown in Fig. 4.1, a similar effect can be achieved by the proposed cascaded divider technique. With this technique, an auxiliary FCW_{aux} is subtracted from the original FCW to generate the FCW_{main}, which is the input of the DSM_{main}. In this way, the accumulated QN from the DSM_{main} (ε_{qnmain}) can be shifted to a frequency that is $FCW_{aux}f_{ref}$ higher than the original frequency. As a result, the pattern of the INL error from the DTC_{main}, which is used to cancel the ε_{qnmain}, can also be pushed to a higher frequency. However, by simply subtracting FCW_{aux} from the original FCW, the PLL output frequency will also be shifted to $FCW_{aux}f_{ref}$ away. For this reason, another auxiliary DSM_{aux} and DTC_{aux} pair is employed to compensate for this frequency drift. The INL error pattern from the DTC_{aux} repeats at a frequency of $FCW_{aux}f_{ref}$, thus will also be sufficiently filtered by the PLL. Note that the resolution of the FCW_{aux} needs not to be the

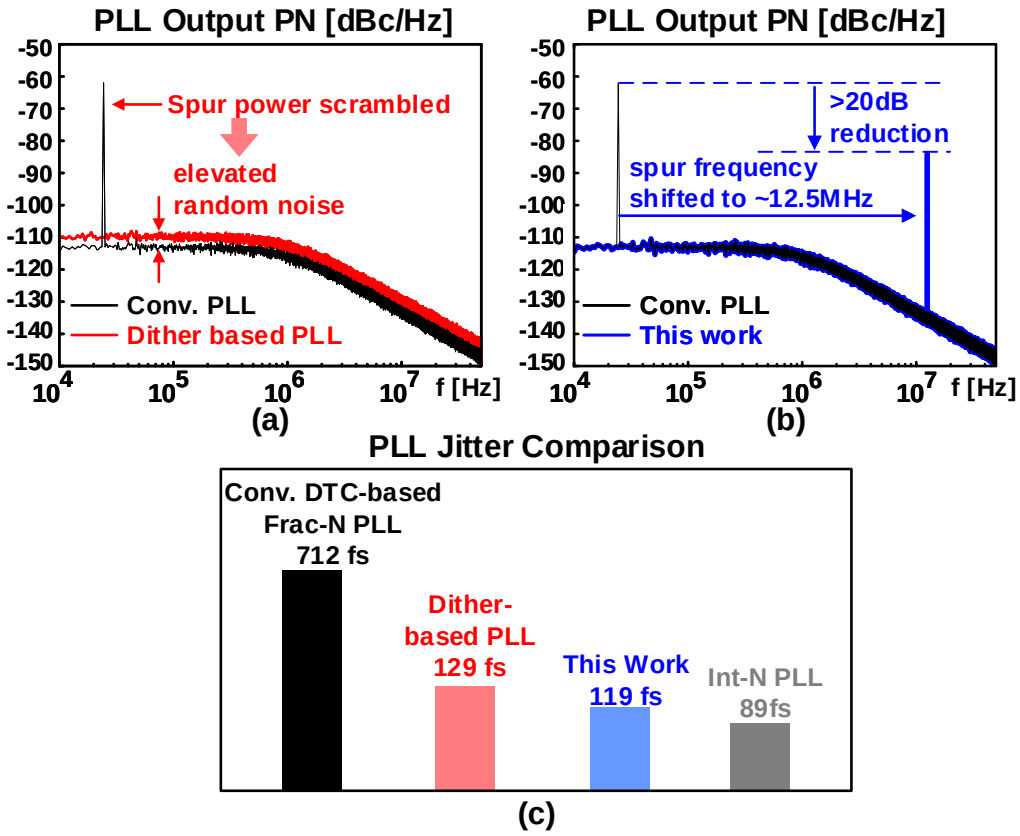


Figure 4.2: The simulated spectrum of a DTC-based PLL with (a) dithering technique, and (b) proposed cascaded divider technique; and (c) integrated jitter comparison of PLLs with different techniques

same as that of the original FCW. Rather, the FCW_{aux} is designed to be 3-bit in this work to simplify the design of the DTC control and gain calibration logic.

Fig. 4.2 (a), (b) show the simulation results of a DTC-based PLL before and after being applied with the conventional dithering technique and the proposed cascaded fractional divider technique, respectively. The simulations are carried out by passing the DTC nonlinearity, DCO noise, and reference noise through the transfer function of a type-II PLL [53]. In order to better show the difference between dithering technique and this work, the DSM is assumed to be of a first-order multistage noise-shaping (MASH-1) topology in the simulations, which results in a single fractional spur in the output spectrum. In the simulations, the DTC is assumed to exhibit a sine-shaped INL with 1 ps peak-to-peak amplitude (INL_{pp}), and the PLL output frequency is assumed to be near 7 GHz. It can be seen that with the dithering technique, the fractional spur can be effectively removed. However, the in-band random noise is elevated by around 4 dB because of the

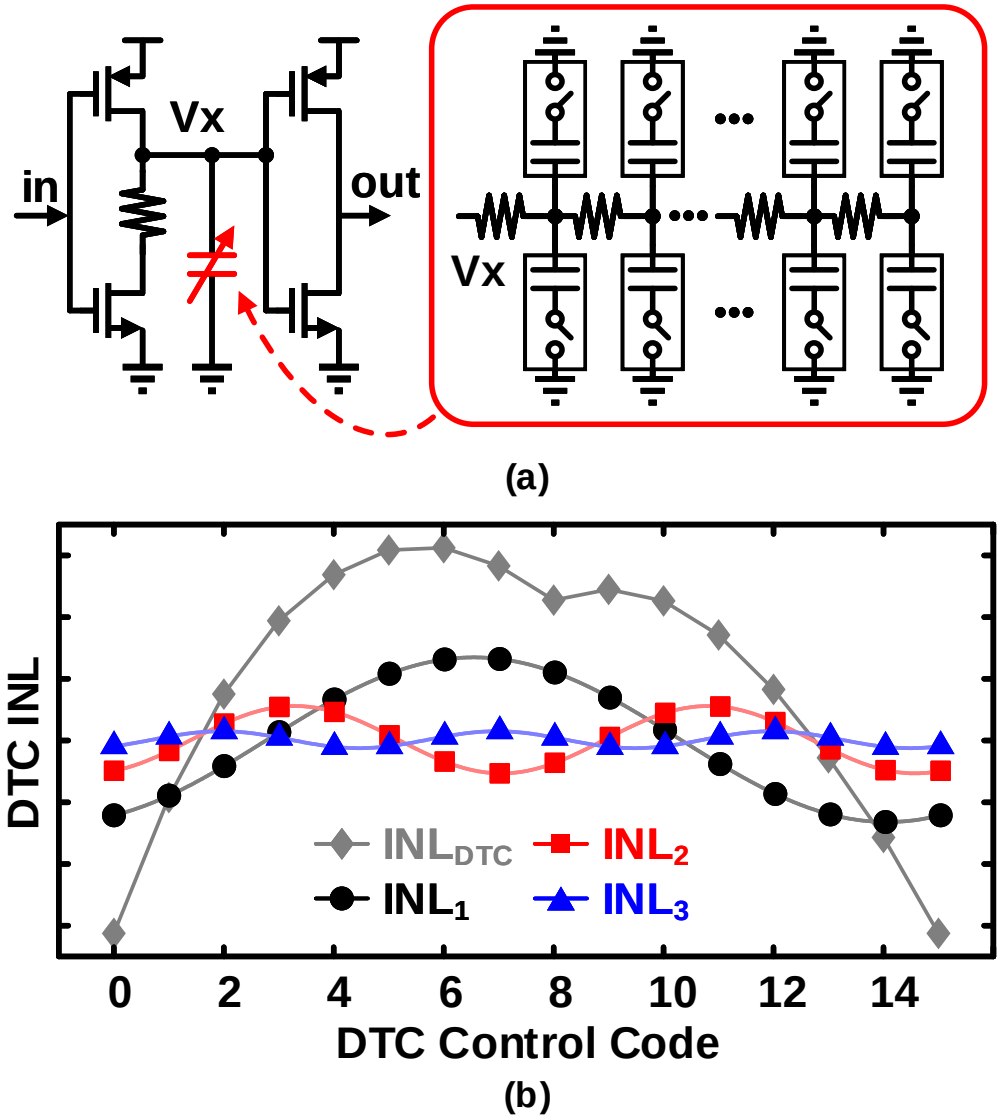


Figure 4.3: The (a) schematic and (b) INL profile of a variable slope DTC with layout-dependent parasitic resistance.

spreaded spur power. On the other hand, the fractional spur location can be pushed to be larger than 12.5 MHz with an FCW_{aux} of 1/8, leading to a more than 20 dB suppression in the fractional spur power with no elevated in-band phase noise in our proposed PLL topology. The integrated jitters of different PLL topologies are compared in Fig. 4.2 (c). It shows that without any distortion from DTC nonlinearity, the integrated jitter can be 89 fs in an integer-N PLL. The integrated jitter will be heavily degraded to 712 fs by the

fractional spur in fractional-N mode, which can be suppressed to 129 fs with the dithering technique. Nevertheless, thanks to the strong filtering strength on the high-frequency fractional spur, the integrated jitter can be suppressed even lower to 119 fs with the proposed cascade fractional divider technique.

4.1.2 DTC INL Decomposition

One may think of using an FCW_{ref} of 1/2 to further push the fractional spur frequency to $0.5f_{ref}$, just like the case in [52]. This will unfortunately not always result in the optimal fractional spur performance because of the high-order harmonic components from the τ_{inl}. To understand this, the profile of the DTC nonlinearity needs to be investigated.

Fig. 4.3 shows an example of the commonly used VS-DTC, where the delay is controlled by turning on or off different units of a capacitor bank. The nonlinearity of the VS-DTC comes mainly from the following three mechanisms:

1. The charging slope at the V_x node is different across different DTC control codes, which will generate a code-dependent delay at the comparator stage [17].

2. The physical distances between the V_x node and different unit switch-capacitor cells are different, which leads to a layout-dependent delay difference at the input stage [25].

3. The amount of the accumulated charge at the bottom plate of each capacitor cell depends on the switch on/off state in the previous reference cycle, leading to the memory effect and degraded DTC nonlinearity [54].

All the above-mentioned mechanisms contribute to the overall DTC INL (INL_{dtc}), which is shown in Fig. 4.3 (b) as a grey curve. For the convenience of analysis in this and the next section, INL_{dtc} can be represented by the following Fourier series:

$$\begin{aligned} INL_{dtc}[D_{ctrl}] &= \sum_i INL_i \\ &= \sum_i [a_i \cos(2\pi i \frac{D_{ctrl}}{2^m - 1}) + b_i \sin(2\pi i \frac{D_{ctrl}}{2^m - 1})], \end{aligned} \tag{4.1}$$

where INL_i is the i-th harmonic component of the DTC INL, m is the DTC number of bits, D_{ctrl} is the DTC control code. The first 3 INL harmonics, INL_1, INL_2, and INL_3, are also plotted in Fig. 4.3 (b) as black, red, and blue curves, respectively. It can be seen that, unlike the nonlinearity profile of a CP, which can be well approximated by a second or third-order polynomial [55], the harmonic components of the INL_{dtc} can be significantly

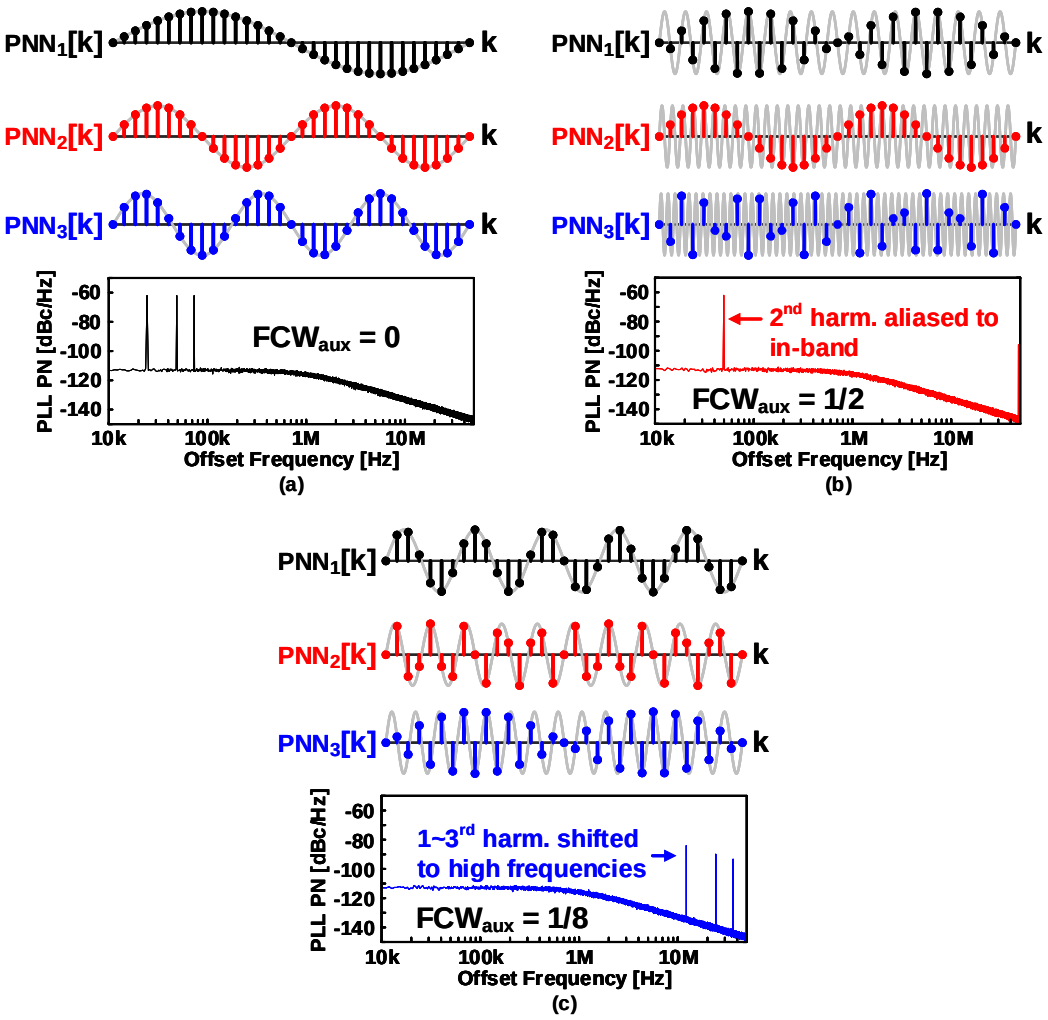


Figure 4.4: The simulated PLL spectrum with the FCW_{aux} of 0, 1/2, and 1/8, respectively.

different and more complicated depending on the specific topology and implementation of the DTC.

4.1.3 Optimal *FCW* Allocation

The optimal FCW_{aux} can be found by taking the previously analyzed INL_{dtc} profile into consideration. Because of the harmonic-rich nature of INL_{dtc}, it is not difficult to prove that when being mapped to ε_{qn}, the resulting periodical nonlinearity noise (*PNN*) of the DSM will also contain multiple harmonics [29, 55]. The *PNN* at the k-th reference cycle

can be expressed by:

$$\begin{aligned} PNN[k] &= \sum_j PNN_j[k] \\ &= \sum_j c_j \cos[2\pi j(\alpha + FCW_{aux})k + \varphi_j], \end{aligned} \tag{4.2}$$

where φ_j is the phase term that is related to the initial state of the DSM. Because the phase error information in a DPLL is handled in a discrete-time fashion[1, 35], each PNN_j can be further rewritten as:

$$PNN_j[k] = c_j \cos[2\pi k \cdot mod((\alpha + FCW_{aux})j, 1) + \varphi_j], \tag{4.3}$$

where *mod(·)* denotes the modulo operation.

Eq. (4.3) implies that the fractional spur frequency generated by the *j*-th harmonic component of the *PNN* will appear at an offset frequency of $mod((\alpha + FCW_{aux})j,1)\cdot f_{ref}$. For any integer $(FCW_{aux}\cdot j)$, the fractional spur will be aliased back to in-band, resulting in almost 0 suppression strength because of the low-pass PLL characteristic.

Fig. 4.4 shows the pattern of the first three terms of the *PNN* when different FCW_{aux}s are selected. The amplitudes of PNN_1, PNN_2, PNN_3 are assumed to be equal in Fig. 4.4, which will not affect the generality of the foregoing analysis. It can be seen from Fig. 4.4 (a) that when no FCW_{aux} is applied, the fractional spurs are located at αf_{ref}, $2\alpha f_{ref}$, $3\alpha f_{ref}$, respectively. When an FCW_{aux} of 1/2 is selected, the fractional spurs generated by PNN_1 and PNN_3 can be moved to higher frequencies, resulting in much smaller spur amplitudes. However, the fractional spur generated by PNN_2 remains at the same frequency as the case of a 0 FCW_{aux}. In order to obtain sufficient filtering strength for all the dominant harmonic components of the *PNN*, an FCW_{aux} of 1/8 is selected in this work for near-integer *FCW*s. As can be seen from Fig. 4.4 (c), the fractional spurs generated by the first three harmonic components of the *PNN* can all be moved beyond the PLL loop bandwidth. Moreover, an *FCW* mapping table as shown in Table 4.1 is utilized to ensure a consistent fractional spur level across different frequency channels.

4.2 Pseudo-Differential DTC

Stronger fractional spur suppression can be achieved by reducing the INL_{dtc} amplitude, which can be realized by either implementing high-linearity DTCs or utilizing the range-reduction technique [42]. However, recent high-linearity DTC topologies such as the constant-slope DTC (CSDTC) [18], or the inverse-constant-slope DTC (ICS-DTC) [22]

Table 4.1: FCW Mapping Table of the Cascaded Fractional Divider

FCW	FCW_{int}	FCW_{aux}	FCW_{main}
[N,N+1/8]	N-1	1/4	[3/4,7/8]
[N+1/8,N+1/4]	N-1	3/8	[3/4,7/8]
[N+1/4,N+3/8]	N-1	1/2	[3/4,7/8]
[N+3/8,N+1/2]	N-1	5/8	[3/4,7/8]
[N+1/2,N+5/8]	N	3/8	[1/8,1/4]
[N+5/8,N+3/4]	N	1/2	[1/8,1/4]
[N+3/4,N+7/8]	N	5/8	[1/8,1/4]
[N+7/8,N+1]	N	3/4	[1/8,1/4]

require extra bias currents, which increase the implementation complexity. On the other hand, further reducing the DTC range to *1/M* inevitably introduces *M* phase mismatches that need to be calibrated, which will cost extra PLL settling time [56]. In this section, we introduce a different way to reduce the INL_{dtc} amplitude by a PD-DTC.

It needs to be stated that the concept of using two DTCs was firstly proposed in [57] to cancel the common mode supply ripples. However, the effect of reducing INL was not reported in [57]. Recently, it was proposed in a patent [58] that a lower INL can be achieved by canceling out the nonlinearities which can be represented by even-order polynomials. Nonetheless, the detailed implementation, mismatch analysis, noise analysis and design considerations were not covered in [57], which will be the focus of this section. Another similar concept was presented in [59], where the time-domain differential operation was utilized to cancel the nonlinearities in a pair of phase interpolators.

4.2.1 Pseudo-Differential DTC Mechanism

With the PD-DTC technique, two identical DTCs (DTC_p and DTC_n) instead of one DTC are utilized to generate a relative delay to cancel the ε_{qn}, as depicted in Fig. 4.5 (a), (b). When the ε_{qn} becomes larger, the delay of the DTC_p (τ_{dtcp}) is tuned to be longer, while the delay of the DTC_n (τ_{dtcn}) is tuned to be shorter. In this way, the required delay ranges for DTC_p and DTC_n are both halved, which leads to lower INL amplitudes in the two

DTCs. Furthermore, the INLs of the two DTCs (INL_p and INL_n) can be expressed by the following two Fourier series:

$$INL_p[D_{ctrl}] = \sum_i [d_i \cos(2\pi i \frac{D_{ctrl}}{2^m - 1}) + e_i \sin(2\pi i \frac{D_{ctrl}}{2^m - 1})], \tag{4.4}$$

$$INL_n[D_{ctrl}] = \sum_i [d_i \cos(2\pi i \frac{D_{ctrl}}{2^m - 1}) - e_i \sin(2\pi i \frac{D_{ctrl}}{2^m - 1})]. \tag{4.5}$$

Note that the two INL profiles contain exactly the same even-symmetric components, which will cancel themselves due to the time-domain differential operation of the PD, and result in the following equivalent INL (INL_{diff}) profile:

$$INL_{diff}[D_{ctrl}] = \sum_i 2e_i \sin(2\pi i \frac{D_{ctrl}}{2^m - 1}). \tag{4.6}$$

The simulated INL_p, INL_n, and INL_{diff} are shown in Fig. 4.5 (c) as black, red, and blue curves, respectively, where the resistor of the DTC in Fig. 4.3 (a) is adjusted to control the $DTC_{p,n}$ delay ranges in the simulations. Due to the naturally low odd-symmetric INL components, the PD-DTC can achieve a much lower equivalent INL amplitude, which greatly relaxes the noise-power-linearity trade-off in conventional DTC designs.

4.2.2 Pseudo-Differential DTC Implementation

In order to balance the design complexity, chip area, and DTC INL characteristics, care must be taken when implementing the PD-DTC. As will be described in Section IV, the most significant bits (MSBs) from ε_{qnmain} and ε_{qnaux} are canceled by DTC_{main} and DTC_{aux}, respectively. However, if the DTC gain is controlled in the digital domain, considerably high hardware resources are required for the complicated multi-bit multiplication operations.

To this aim, a coarse-fine segment structure of the DTC is employed to cancel the ε_{qnmain}. The coarse stage of the single DTC branch is shown in Fig. 4.6 (a). The delay range of the DTC is controlled by passing the coarse DTC gain control code $K_{dtcmain}$ to a voltage mode digital-to-analog converter (DAC), which is used to control the bias voltage (V_b) of the active resistor (M_{p2}). A 10-pF capacitor is connected between the V_b node and the DTC supply to bypass the supply ripple, which might modulate the on-resistance of M_{p2}. In this way, a fine range resolution can be achieved in the coarse stage, which is sufficient to cancel all the most significant bits (MSBs) of the ε_{qnmain} without generating any residue QN. Note that because the $K_{dtcmain}$ is usually fixed for a given frequency channel, the nonlinearities from the DAC do not generate any influence on the DTC INL.

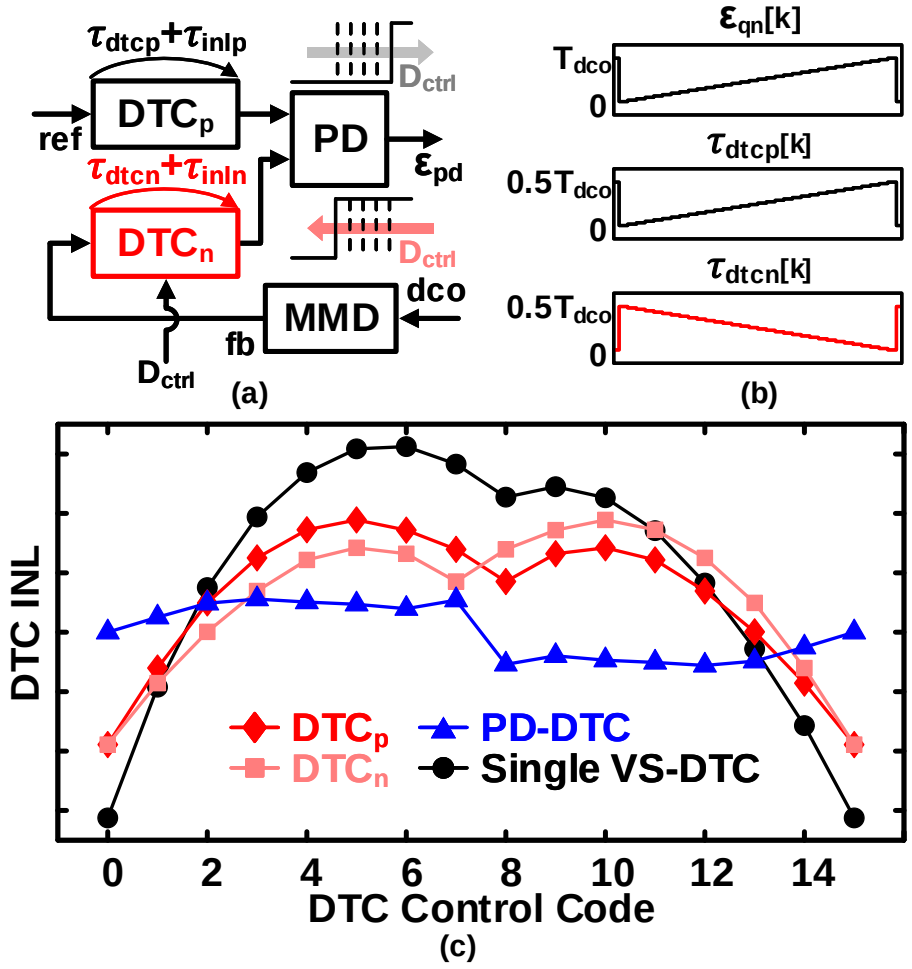


Figure 4.5: The concept of cancelling the even-symmetric INL components via a pseudo-differential DTC.

This allows a simple 10-bit R2R ladder implementation for the DAC, which is shown in Fig. 4.6 (c). The least significant bits (LSBs) of the ε_{qnmain} (ε_{qnfine}) are canceled by the fine DTC stage as shown in Fig. 4.6 (b), where the delay is controlled by a capacitor bank that loads a simple inverter. The fine DTC control code is generated by multiplying the fine DTC gain ($K_{dtcfine}$) with the ε_{qnfine}, which requires a much smaller number of bits in the multiplication operation compared to a conventional fully digital DTC gain control scheme [4].

It is possible to improve the PD-DTC resolution by controlling the delay codes of DTC_p and DTC_n (D_{ctrlp} and D_{ctrln}) separately. As shown in Fig. 4.6 (d), when D_{ctrl} increases by one, either the D_{ctrlp} is selected to be increased by 1 or the D_{ctrln} is selected

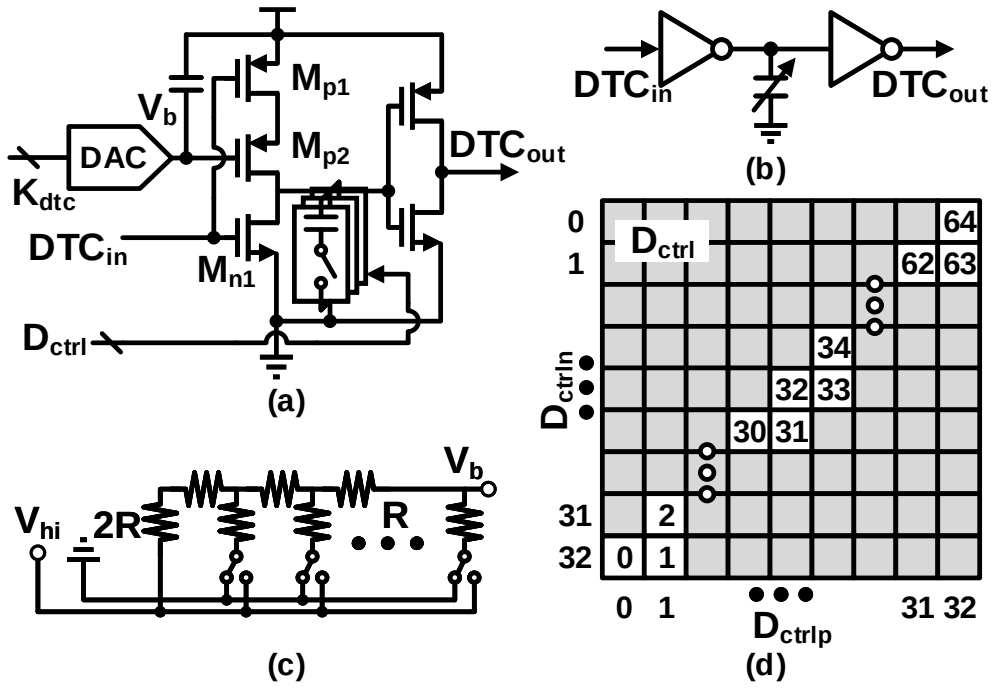


Figure 4.6: The schematics of (a) the single DTC branch of DTC_{main} and DTC_{aux}, (b) the single DTC branch of DTC_{fine}, (c) the R2R ladder DAC for the gain control of DTC_{main} and DTC_{aux}; and (d) the possible decoding scheme to improve the PD-DTC resolution.

to be decreased by 1. In this method, two (m-1)-bit DTCs can construct an m-bit PD-DTC. Nevertheless, it is worth mentioning that this improvement in the delay resolution is realized at the risk of worsening the INL_{diff}, which will be explained later in this section. For this reason, we only adopt this decoding scheme for the 6-bit DTC_{fine}, which will not degrade the INL too much because of the short delay range. The two branches of the 6-bit DTC_{main}, on the other hand, are controlled by the codes with inversed signs directly, which is the same for the 3-bit DTC_{aux}.

4.2.3 Mismatch Analysis

As mentioned earlier in this section, the mismatch between the two DTCs needs to be considered when implementing a PD-DTC. For the simplicity of analysis, the PD-DTC can be modeled as the circuits shown in Fig. 4.7 (a), where: R_p, stands for the on-resistance contributed by M_{p1} and M_{p2} in the DTC_p; C_{fixp} stands for the fixed-value capacitance at the comparator input node in the DTC_p, which is mainly contributed by the parasitic gate-to-source capacitance; C_0D_{ctrlp} stands for the capacitance of the capacitor bank in

the DTC_p. Similarly, R_n, C_{fixn}, and C_0D_{ctrln} stand for the corresponding variables in the DTC_n. The relative delay (τ_{diff}) generated by the PD-DTC can thus be expressed by:

$$\begin{aligned}\tau_{diff} &= \tau_{dtcp} - \tau_{dtcn} \\ &= R_pC_pln(\frac{V_{DD}}{V_{DD}-V_{thp}}) - R_nC_nln(\frac{V_{DD}}{V_{DD}-V_{thn}}) \\ &= \tau_{ofst} + \tau_{resp}D_{ctrlp} - \tau_{resn}D_{ctrln},\end{aligned} \tag{4.7}$$

where C_p = C_{fixp} + C_0D_{ctrlp} is the total capacitance at the DTC_p comparator input, C_n = C_{fixn} + C_0D_{ctrln} is the total capacitance at the DTC_n comparator input, τ_{ofst} = $R_pC_{fixp}ln(\frac{V_{DD}}{V_{DD}-V_{thp}})$-$R_nC_{fixn}ln(\frac{V_{DD}}{V_{DD}-V_{thn}})$ is a fixed term which will be nullified by the PLL, τ_{resp} = $R_pC_0ln(\frac{V_{DD}}{V_{DD}-V_{thp}})$ is the delay resolution of the DTC_p, τ_{resn} = $R_nC_0ln(\frac{V_{DD}}{V_{DD}-V_{thn}})$ is the delay resolution of the DTC_n, respectively.

As implied by Eq. (4.7), the mismatch between C_{fixp} and C_{fixn} contributes only to the τ_{ofst}, and thus will not degrade the INL_{diff} much. It worths mentioning that the mismatch between the delay offsets in DTC_p and DTC_n does cause the mismatch between the slope-induced nonlinearities in each DTC. This mismatch however, will only generate insignificant degradation on the INL_{diff}. On the other hand, any mismatches between R_p and R_n, or between V_{thp} and V_{thn} will result in the mismatch between the code-to-delay gains of the DTC_p and the DTC_n, which might degrade INL_{diff} heavily depending on the DTC decoding scheme, as will be shown below.

For the DTC decoding scheme shown in Fig. 4.6 (d), Eq. (4.7) can be re-written as Eq. (4.8) by replacing D_{ctrlp} and D_{ctrln} with $\lceil 0.5D_{ctrl} \rceil$ and $\lfloor 0.5D_{ctrl} \rfloor$, where $\lceil \cdot \rceil$ denotes the ceiling operation, $\lfloor \cdot \rfloor$ denotes the flooring function:

$$\begin{aligned}\tau_{diff}[D_{ctrl}] &= \tau_{ofst} + \tau_{resp}\lceil \frac{D_{ctrl}}{2} \rceil - \tau_{resn}\lfloor \frac{D_{ctrl}}{2} \rfloor \\ &= \tau_{ofst} + \hat{\tau}_{res}D_{ctrl} + \Delta\tau_{res}[D_{ctrl}].\end{aligned} \tag{4.8}$$

In Eq. (4.8), $\hat{\tau}_{res}$ = $\frac{\tau_{resp}+\tau_{resn}}{2}$ is the effective resolution of the PD-DTC, $\Delta\tau_{res}[D_{ctrl}]$ = $(-1)^{D_{ctrl}}.\frac{\tau_{resp}-\tau_{resn}}{2}$ is the term that represents the mismatch between the ideal and actual differential delays at D_{ctrl}. It can be seen that the sign of $\Delta\tau_{res}$ changes whenever D_{ctrl} increases by 1, which will generate a “sawtooth” pattern in the INL profile. It needs to be clarified that the decoding scheme in Fig. 4.6 (d) itself also creates the "sawtooth" pattern in the INL_{diff}, which is because of the interpolation between INL_p and INL_n. However, this will not degrade the INL_{diff} if the DTC_p and the DTC_n are perfectly matched. Fig. 4.7 (b) shows the 100-run Monte-Carlo simulation results of a PD-DTC with the decoding scheme in Fig. 4.6 (d). It can be seen that the mismatch between DTC_p and DTC_n causes

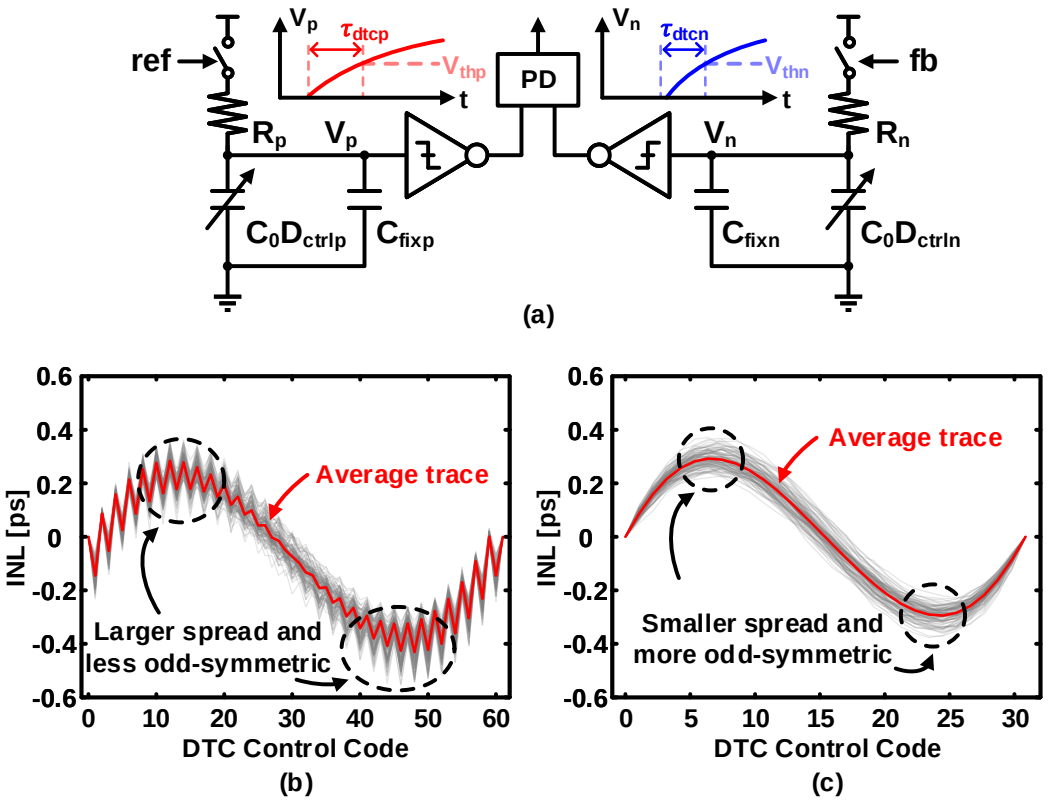


Figure 4.7: The (a) mismatch analysis model of PD-DTC; and the overlay of 100 Monte-Carlo simulations of the PD-DTC INL (b) with and (c) without the decoding scheme to extend the equivalent PD-DTC number-of-bits.

a larger spread in the INL profile, which further results in the worse degradation of the INL_{pp}. On the other hand, Fig. 4.7 (c) shows that in the implemented DTC_{main} where the decoding scheme in Fig. 4.6 (d) is not applied, a smaller INL spread and a smaller INL_{pp} can be expected.

4.2.4 Phase Noise Comparison with Single DTC

The PN difference between the single DTC and the PD-DTC is also necessary to be studied because the latter utilizes two DTCs which might contribute to more in-band PN. Although a direct noise analysis is tedious, the PN comparison between the single DTC and the PD-DTC could be easy because the jitter, *i.e.*, the PN of the DTC is related to only the amplitude of the noise voltage and the slew rate (SR) at the input node of the comparator stage [60]. For simplicity, we assume the nominal value of $V_{thp,thn}$ equals $0.5V_{DD}$, and represent the nominal values of $R_{p,n}$ and $C_{fixp,fixn}$ as R and C_{fix}, respectively. The SR

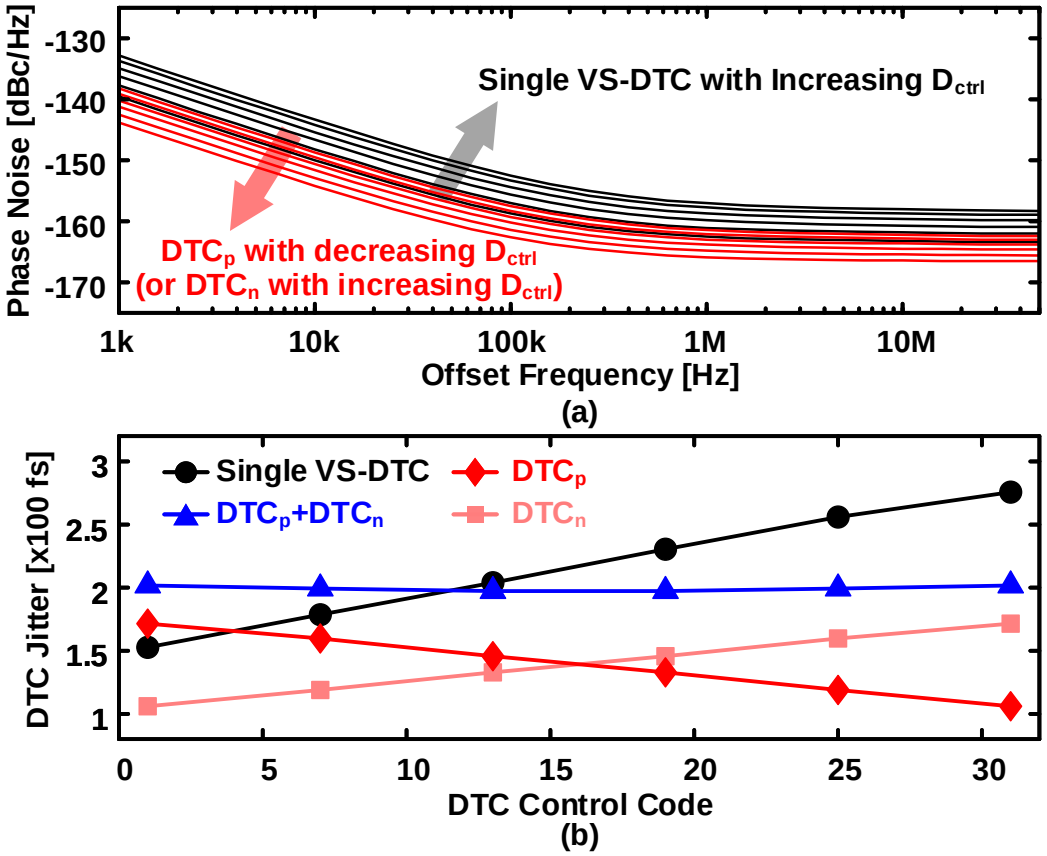


Figure 4.8: The simulated (a) phase noises of a single VS-DTC with 280 ps delay range and the two branch DTCs from a PD-DTC with the same differential delay range; and (b) the jitters contributed by the single VS-DTC and the PD-DTC.

at the time when V_p crosses $0.5V_{DD}$ can be calculated as $SR_p = \frac{V_{DD}}{2R(C_{fix}+D_{ctrl}C_0)}$. Similarly, for node V_n, we can derive $SR_n = \frac{V_{DD}}{2R(C_{fix}+(2^m-D_{ctrl})C_0)}$. The total jitter contributed by the PD-DTC ($\sigma^2{}_{diff}$) can then be expressed as:

$$\sigma^2_{diff} = \frac{\sigma^2_v}{SR^2_p} + \frac{\sigma^2_v}{SR^2_n} = \frac{4R^2\sigma^2_v}{V^2_{DD}} \cdot [(C_{fix}+D_{ctrl}C_0)^2 + (C_{fix}+(2^m-D_{ctrl})C_0)^2], \tag{4.9}$$

where $\sigma^2{}_v$ represents the overall voltage noise power contributed by the active resistor, switch transistor, *etc*.

Because the power consumption of the DTC is mainly determined by the total amount of charge dissipated at the capacitor in every cycle, a single VS-DTC with a capacitor

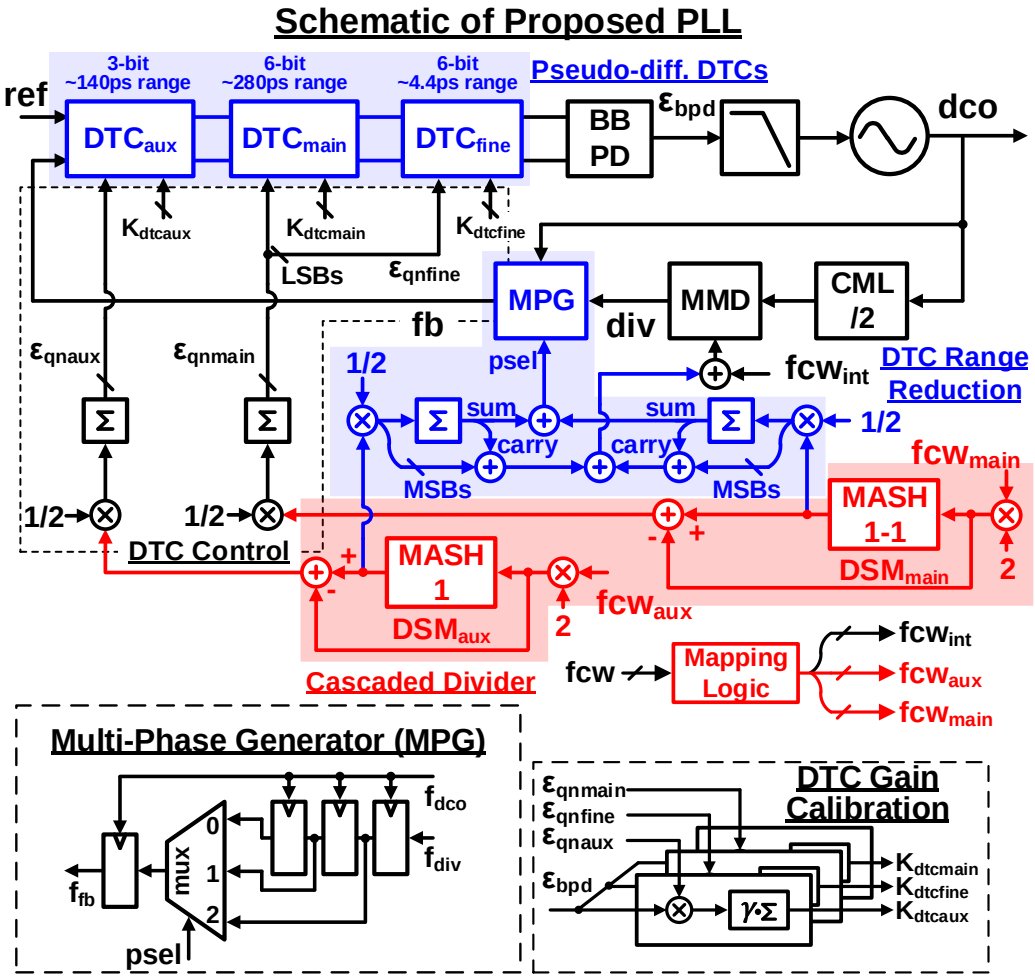


Figure 4.9: The implemented DPLL with the cascaded fractional divider, PD-DTCs, DTC range reduction, and LMS-based DTC gain calibrations.

bank, of which the unit capacitance is $2C_0$, is considered for a fair comparison. The SR of the single VS-DTC comparator input voltage when it crosses $0.5V_{DD}$ can be calculated as $SR_{se} = \frac{V_{DD}}{2R(C_{fix}+2D_{ctrl}C_0)}$. The jitter of the single VS-DTC can be expressed as:

$$\sigma_{se}^2 = \frac{\sigma_v^2}{SR_{se}^2} = \frac{4R^2\sigma_v^2}{V_{DD}^2} \cdot (C'_{fix} + 2D_{ctrl}C_0)^2, \tag{4.10}$$

where C'_{fix} is the fixed-value capacitance at the single VS-DTC comparator input node, which is usually different from C_{fix} due to the difference in the layout.

The difference between the PD-DTC and the single VS-DTC PN characteristics is thus revealed by Eq. (4.9) and (4.10): the PN power of the single VS-DTC increases

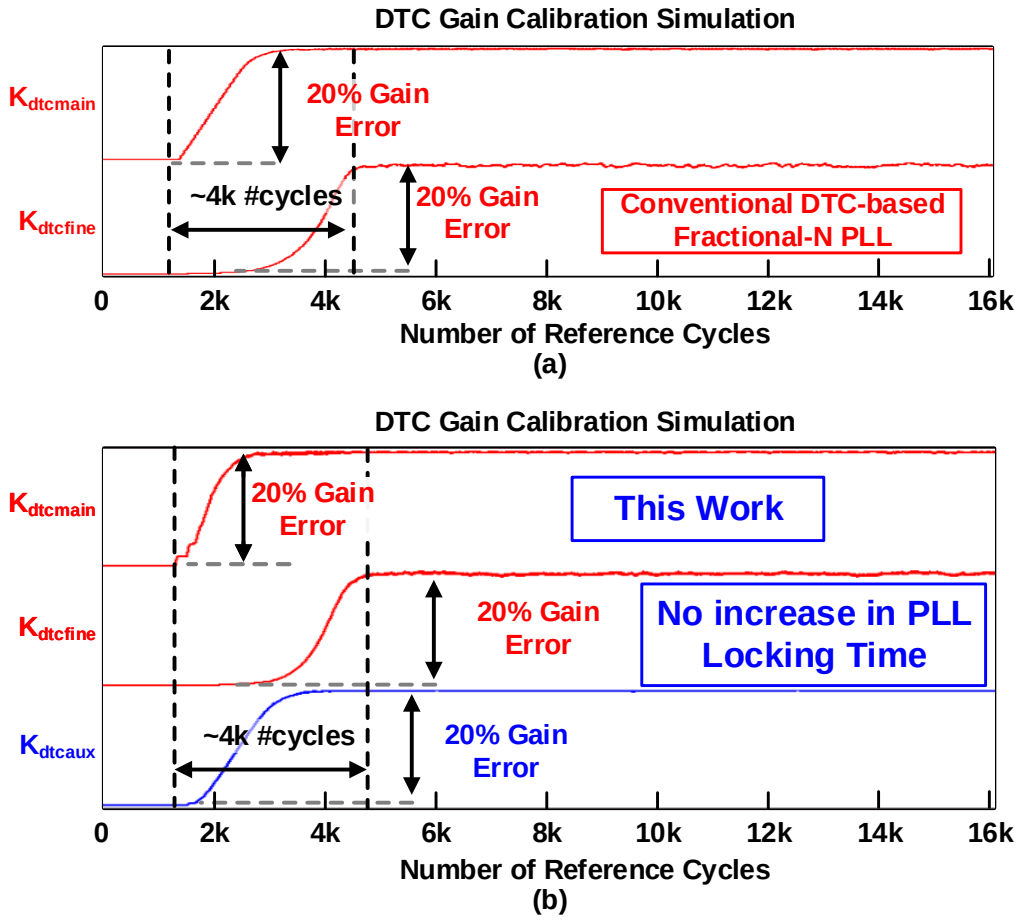


Figure 4.10: The simulated convergence processes of the DTC gain calibrations in (a) the conventional DTC-based fractional DPLL and (b) the proposed DPLL with a cascaded fractional divider and PD-DTCs.

monotonically with an increasing D_{ctrl}, while the PN power of the PD-DTC becomes lower when D_{ctrl} approaches the central value. As a result, the PN of the PD-DTC is not necessarily worse than that of the single VS-DTC when being applied with different delay control codes.

The post-layout simulations on the previously-mentioned DTC_{main} and a single VS-DTC with the same delay range of 280 ps are conducted to verify the above noise analysis. Fig. 4.8 (a) shows that with the increasing D_{ctrl}, the PN of the DTC_p in the PD-DTC increases and the PN of the DTC_n decreases. On the other hand, the PN of the single VS-DTC elevates with an increasing D_{ctrl}, which matches well with the predictions above. The jitters of different DTCs are also simulated across different DTC control codes, which are summarized and shown in Fig. 4.8. It can be seen that the jitter of the single VS-

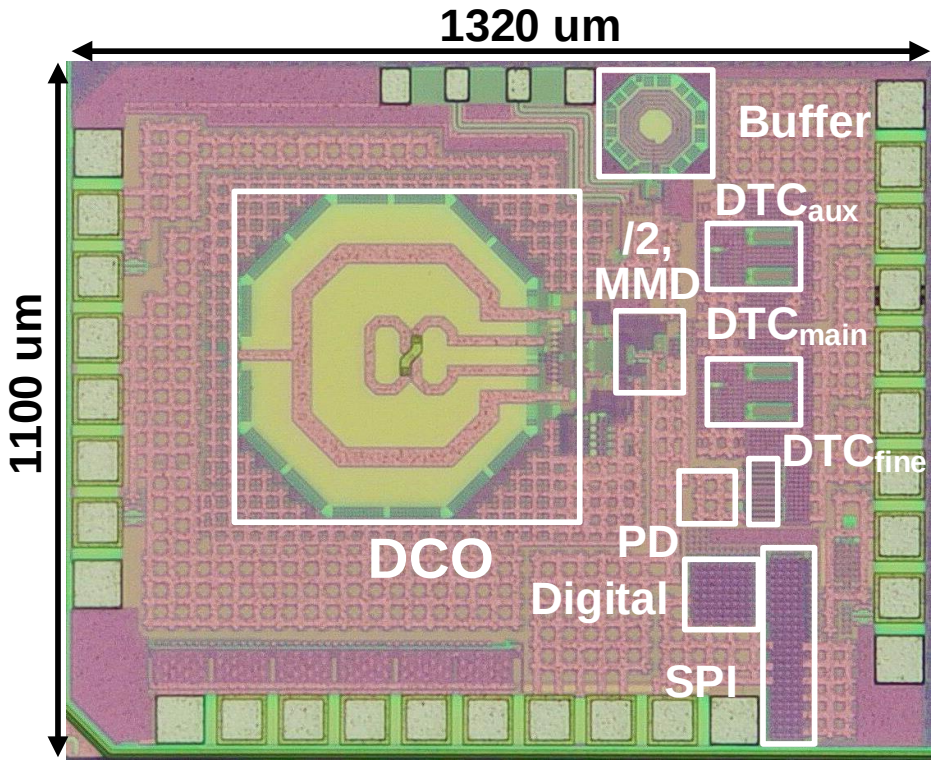


Figure 4.11: The die micrograph of the proposed DPD/dither-free DPLL.

DTC does increase monotonically with the D_{ctrl}, while the total jitter of the PD-DTC becomes lower when D_{ctrl} approaches the central code. The jitter of the single VS-DTC and the jitter of the PD-DTC are not the same at the central DTC control code because the difference between C'_{fix} and C_{fix} causes the difference in the minimum jitters, which "shifts" the jitter-D_{ctrl} curves vertically with different offsets. Moreover, for more than half of the DTC control codes, the jitter of the PD-DTC is lower than that of the single VS-DTC, implying on average no jitter degradation or even jitter improvement when a PD-DTC is used.

4.3 DPD/Dither-Free DPLL Implementation

The detailed schematics of the implemented DPLL utilizing the aforementioned cascaded fractional divider and PD-DTC techniques are shown in Fig. 4.9. A BBPD is utilized in the DPLL for reducing the power consunmption from the multi-bit TDC.

In order to ensure strong enough correlation between the BBPD output and DTC gain error such that the convergence of DTC gain calibration can be fast for near-integer FCWs,

one of the DSM should be implemented in at least second order. For simplicity, a MASH-1-1 DSM is used as the DSM_{main} in this work. It needs to be mentioned that the swap of MASH-1 and MASH-1-1 does not affect much the PLL performance. On the other hand, a MASH-1 DSM is used as the DSM_{aux} in order not to extend the required delay range of the DTC_{aux}, which might cause in-band PN degradation. The fractional resolution of DSM_{aux} is designed to be 3-bit for a better suppression of fractional spurs resulted from high-order *PNN*s. The fractional resolution of DSM_{main} is designed to be 15-bit for extending the PLL frequency resolution. Note that the swap of The 6-bit DTC_{main} and 6-bit DTC_{fine} with the structures described in Section-III are utilized to cancel the ε_{qnmain}. For the design simplicity, the 3-bit DTC_{aux} is implemented by reusing the DTC_{main} with the LSBs of the DTC control code tied to the ground. The delay range of the DTC_{aux} is around 140 ps.

The gains of the DTC_{main}, DTC_{fine}, and DTC_{aux} are all calibrated in the background by LMS-based calibrators [4]. The convergence process of the DTC gain calibration is shown in Fig. 4.10 (b). It shows that all the DTC gain calibrations can converge within 4 thousand reference cycles when the initial gain errors are both 20% away from the ideal values. In order to prove that no degradation in the DTC gain calibration time (and thus the PLL locking time) is generated in the implemented DPLL, the DTC gain calibrations of a conventional DTC-based DPLL is also simulated and shown in Fig. 4.10 (a). It can be seen that in the conventional DTC-based DPLL, the DTC gain calibrations take only slightly less than 4 tousand reference cycles to converge with the same initial gain errors, which is almost the same with the case of our proposed DPLL.

Because the DCO is working with an output frequency of 6.5-to-7.5 GHz, a by-2 divider based on the CML is used as a prescaler to avoid possible malfunctions in the MMD, which is the same as the previous cascaded dual-fractional-*N* DPLL. However, the required delay ranges of all the DTCs need to be doubled to cover the output period of the CML divider, which will cause in-band PN degradation of the DPLL. To mitigate this problem, the DTC range reduction technique in [42] is implemented. Furthermore, a multi-phase generator (MPG) is utilized to generate different MMD output phases from different DCO edges. It is worth mentioning that no phase mismatch calibration is required for the implemented DTC range reduction technique because the output of the MPG is retimed by the DCO clock, which yields a perfect 1 DCO period delay between the neighboring MPG output phases. The schematic of the MPG is also shown in Fig. 4.9.

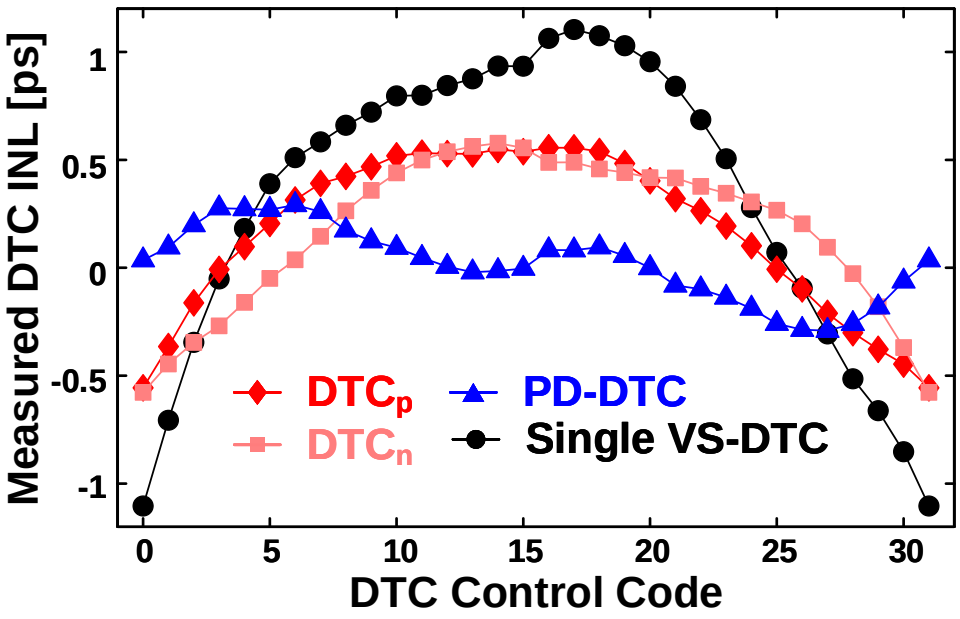


Figure 4.12: The measured INL of (a) the single VS-DTC with a 280 ps delay range and (b) the PD-DTC with a 280 ps differential delay range.

4.4 Measurement Results

This DPD/dither-free DPLL is implemented in 65-nm CMOS process. Fig. 4.11 shows the die micrograph of the DPLL, the core area is 0.23 mm^2. The reference frequency of the DPLL is 100 MHz, which is generated by a signal generator (Rhode&Schwarz SMA100A). The total power consumption of the DPLL is 8.89 mW, with the power breakdown as follows: the DTC_{main} consumes 0.67 mW, the DTC_{fine} consumes 0.5 mW, the DTC_{aux} consumes 0.58 mW, the DCO consumes 3.3 mW, the digital logic consumes 0.34 mW, the CML prescaler, MMD, BBPD, and other internal buffers consumes 3.5 mW.

4.4.1 DTC Nonlinearity Measurement

In order to validate the effect of the proposed PD-DTC, the nonlinearities of the PD-DTC and the single VS-DTC are measured with the method reported in [61]. When measuring the PD-DTC, the two inputs of the DTC_{main} are both connected to the 100 MHz reference directly, the DTC K_{main} is adjusted manually to match the differential delay range of the PD-DTC to twice the DCO period, *i.e.*, around 280ps. On the other hand, only one DTC branch of the DTC_{main} is used for the single VS-DTC INL measurement. In this scenario, the K_{main} is adjusted to match the delay range of the measured VS-DTC branch to around 280 ps.

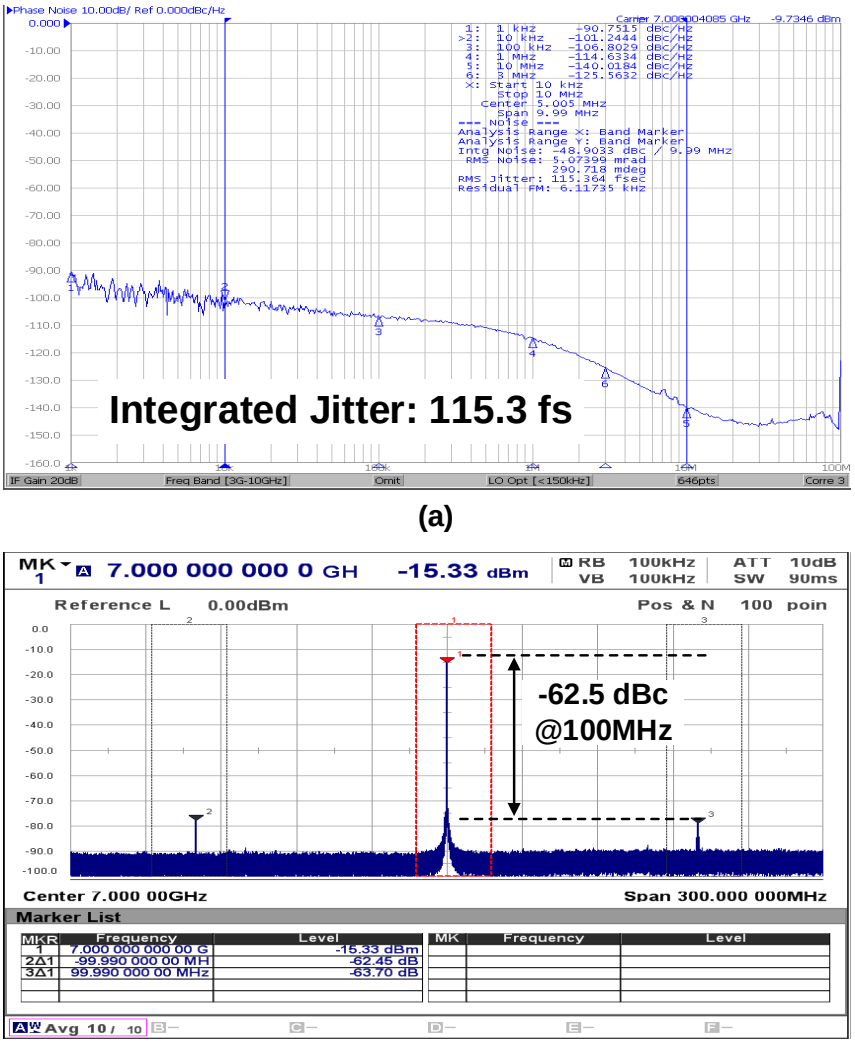
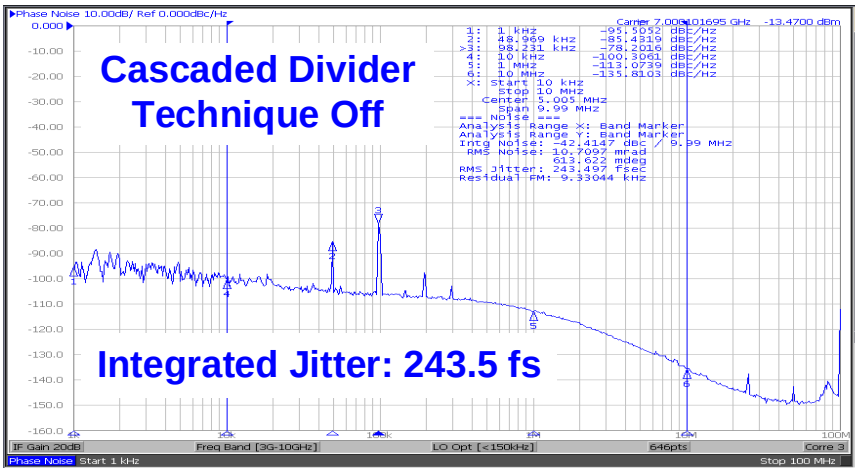
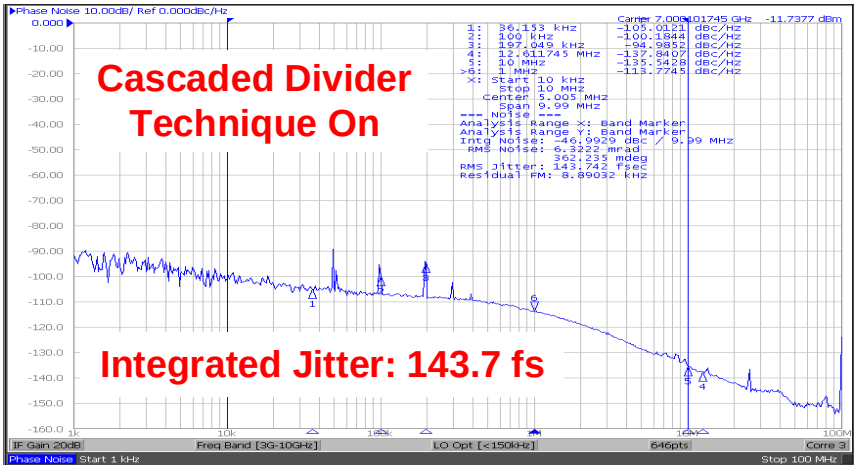


Figure 4.13: The measured (a) PLL phase noise spectrum and (b) reference spur level when the PLL output frequency is 7 GHz.

The measured INL profiles of the single VS-DTC and the PD-DTC are shown in Fig. 4.12. The INL_{pp} of the single VS-DTC is larger than 1.1 ps. Thanks to the halved delay range in each DTC branch of the PD-DTC, the INL_{pp} can be reduced to less than 600 fs. Moreover, an even lower differential INL_{pp} of less than 250 fs can be achieved. This corresponds to an improvement from 0.79% to 0.21% when being refferred to the whole DTC delay range, leading to a much lower fractional spur level when being applied to the PLLs.



(a)



(b)

Figure 4.14: The measured PLL phase noise spectrum (a) before and (b) after turning on the cascaded fractional divider technique at a near-integer channel near 7 GHz.

4.4.2 DPLL Measurement

The phase noise spectrum and reference spur level of the DPLL in an integer-N channel of 7 GHz is shown in Fig. 4.13. The DPLL exhibits an integrated jitter of 115.3 fs with an integration bandwidth of 10 kHz to 10 MHz. The reference spur level is measured to be -62.5 dBc.

The DPLL performances with and without the proposed cascaded divider technique are also measured at the fractional channel near 7 GHz. The measured fractional-N DPLL spectra are shown in Fig. 4.14. When the cascaded fractional divider technique is turned off, the DPLL integrated jitter is heavily degraded to 243.5 fs by the fractional spurs falling below the PLL bandwidth. When the cascaded fractional divider technique is

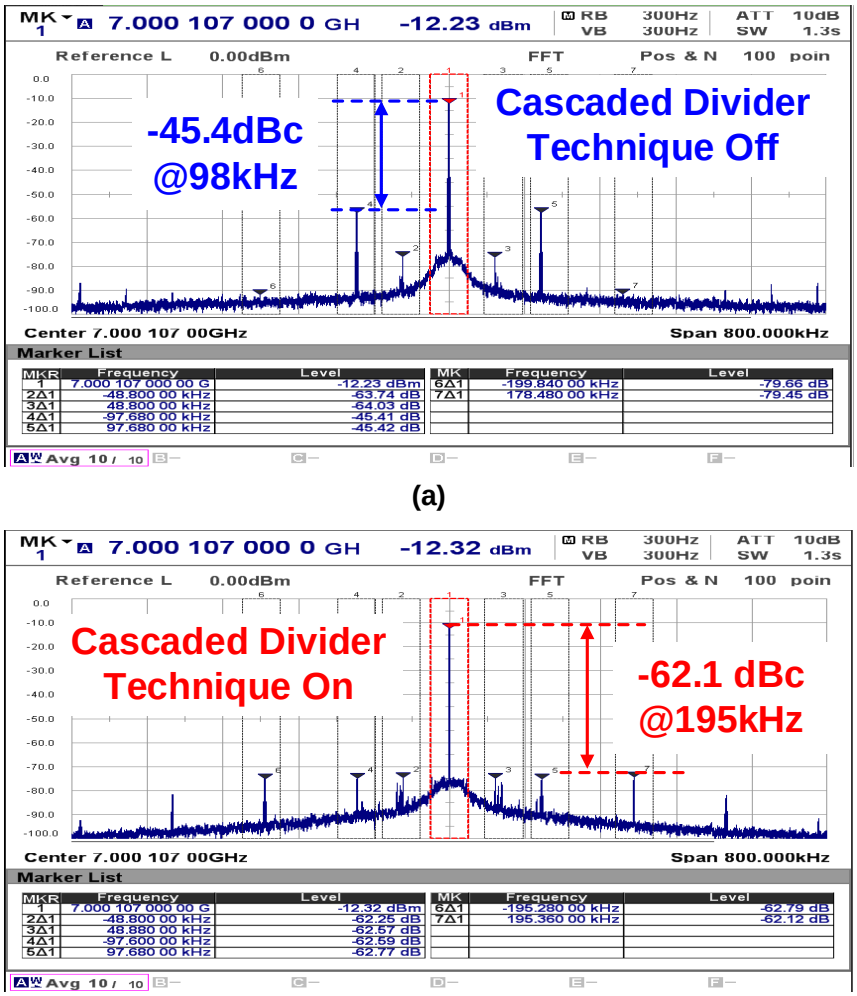


Figure 4.15: The measured PLL output spectrum (a) before and (b) after turning on the cascaded fractional divider technique at a near-integer channel near 7 GHz.

turned on, the *PNN* pattern can be pushed to a higher frequency, which is then filtered by the loop characteristics and leads to a much lower integrated jitter of 143.7 fs. The fractional spur levels before and after turning on the cascaded fractional divider technique are measured and shown in Fig. 4.15. It can be seen that before turning on the cascaded fractional divider technique, the worst fractional spur shows a level of -45.4 dBc with a 98 kHz offset frequency. After turning on the cascaded fractional divider technique, the worst fractional spur is located at 195 kHz offset frequency, showing an amplitude of -62.1 dBc. The fractional spur levels at different fractional-N channels near 7 GHz are also measured, which is shown in Fig. 4.16. It is observed that for the fractional spurs that fall below the PLL loop bandwidth, more than 15 dB suppression can be achieved

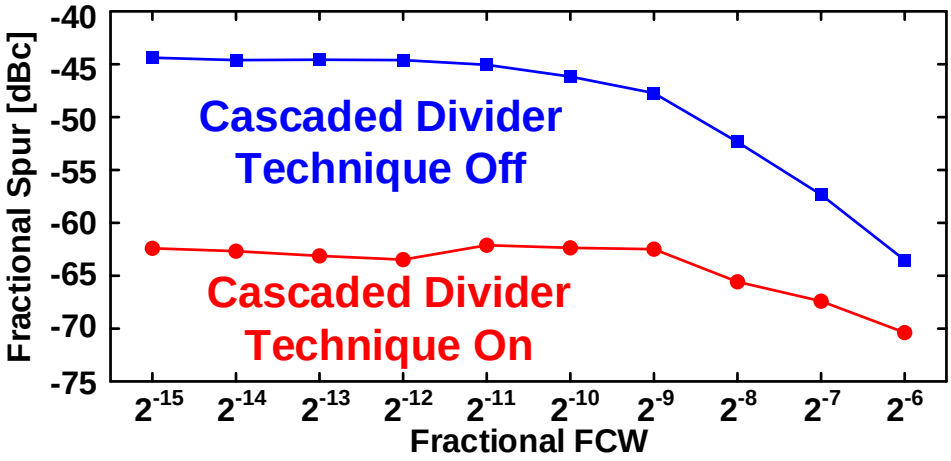


Figure 4.16: The measured worst-case fractional spur level acroos different fractional channels near 7 GHz.

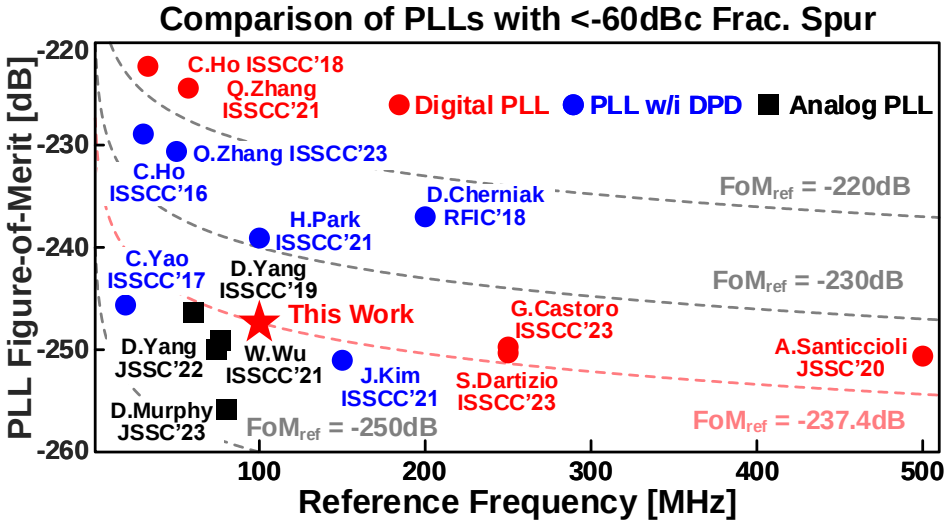


Figure 4.17: The comparison of PLLs with less than 60 dBc fractional spurs.

with the proposed cascaded fractional divider technique. The fractional spur suppression strength is limited by the substrate coupling and the high-order harmonic components of the *PNN*. Further fractional spur suppression can be achieved by improving the on-chip isolation conditions and applying careful layout techniques to reduce the high order harmonic components in the DTC INL, and thus *PNN*.

Table 4.2 summarizes the performance of recent PLLs [19, 22, 42, 49, 54, 62–65]. It can be seen that the DPLL in this work can achieve a very competitive performance,

especially the fractional spur performance, which is even better than some works with DPD. Fig. 4.17 shows a comparison of PLLs with less than 60 dB fractional spurs [25, 45, 48, 66–71]. Thanks to the cascaded fractional divider technique and the PD-DTCs, this DPLL can achieve a fractional spur suppression without any noise penalty below the PLL bandwidth, leading to an FoM_{ref} of -237.4 dB. Remarkably, without the implementation of any DPD technique, an FoM_{ref} of -237.4 dB can still be achieved by the proposed DPLL, implying an inherently superiority of the topology. If the PLL locking time constraints can be relieved, the DPD techniques introduced in chapter 2 can still be readily applied to this PLL, which can further benefit the fractional spur and phase noise suppression.

4.5 Summary

In this chapter, a 6.5-to-7.5 GHz DPD/dither-free DPLL in a 65-nm CMOS process is introduced. The presented DPLL demonstrates an integrated jitter of 143.7 fs at the near-integer channel when working with a 100 MHz reference frequency. The power consumption of the DPLL is 8.89 mW, which leads to an FoM of -247.4 dB. A worst-case fractional spur level of -62.1 dBc is achieved without the help of any dithering, which might cause the elevation of random noise. Meanwhile, no DPD on the DTC INL is utilized in the presented DPLL, guaranteeing no overhead in the PLL locking time. These excellent characteristics are achieved by exploiting:

1. A cascaded fractional divider technique which can shift the in-band fractional spurs to the out-of-band for being filtered by the PLL.

2. PD-DTCs with self-cancelled even-symmetric INL components, which greatly relaxes the noise-power-nonlinearity trade-off in the conventional DTCs by achieving a 0.21% INL_{pp} without much jitter overhead.

When compared with DPD-less DPLLs with less than -60 dBc fractional spurs, the presented DPLL can achieve the best FoM_{ref} of -237.4 dB.

Table 4.2: Comparison with Other Recent Fractional PLLs

	This Work	G. Castoro ISSCC'23	M. Mercandeli ISSCC'21	A. Santiccioli JSSC'20	S. Dartizio JSSCC'23	Z. Gao JSSC'23	J. Kim ISSCC'21	H. Liu JSSC'18	X. Gao ISSCC'16	W. Wu ISSCC'21
Process [nm]	**65**	28	28	28	28	40	65	65	28	14
Topology	**DPLL**	DPLL	DPLL	DPLL	DPLL	DPLL	DPLL	DPLL	DPLL	SPLL
Technique	**Cascaded Fractional Divider + PD-DTC**	Multi DTC	DTC Gain Calibration	Replica DTC + Retiming	ICS DTC + FCW Dither	TAU + DPD	VDAC + DPD	Isolated CS-DTC	Replica DTC+ Sampling TDC	DTC Range Reduction
w/i DPD?	**No**	No	No	No	No	Yes	Yes	No	No	No
Ref. Frequency [MHz]	**100**	250	250	500	250	40	150	26	40	76.8
PLL Frequency [GHz]	**6.5~7.5**	9.25~10.75	12.9~15.1	12.8~15.2	9.25~10.5	2.56~4.1	14~16	2.0~2.8	2.7~4.3	6.2
Fractional Spur [dBc]	**-62.1**	-60.3	-50.4	-61	-71.9	-59	-61	-56	-54	-66.4***
Integrated Jitter [fs]	**143.7**	77.1	107.6	66.2	76.7	182	104	530	159	93.2
Integration Bandwidth [Hz]	**10k~10M**	1k~100M	1k~100M	1k~100M	10k~100M	10k~40M	10k~30M	10k~10M	10k~40M	10k~40M
Reference Spur [dBc]	**-62.5**	-71.1	-73.2	-80.1	-70.5	-73.5	N/A	-72	-78	-70.5
Power [mW]	**8.89**	17.9	10.8	19.8	17.2	3.48	7.3	0.98	8.2	14.2
FoM* [dB]	**-247.4**	-249.7	-249.0	-250.6	-249.9	-249.4	-251.0	-246	-246.8	-249.1
FoM_{ref}** [dB]	**-237.4**	-235.8	-235.1	-233.6	-236.0	-243.4	-239.3	-241.85	-240.78	-240.2
Area [mm^2]	**0.23**	0.36	0.16	0.17	0.33	0.31	0.21	0.23	0.3	0.31

*$FoM = 10\log[(Power/1mW)(Jitter/1s)^2]$ **$FoM_{ref} = 10\log[(Power/1mW)(Jitter/1s)^2] + 10\log(f_{ref}/10MHz)$ ***Normalized to output frequency

Chapter 5

Building Block Design Techniques for Low-Fractional-Spur DPLLs

The cascaded dual-fractional-*N* DPLL and the DPD/dither-free DPLL introduced in chapter 3 and chapter 4 provide a different way to suppress the fractional spurs by pushing those spurs to high frequency. Consequently, a narrower loop bandwidth is preferred for those PLL topologies. Moreover, a high-purity and high-frequency reference source can cause a significant increase in the chip cost. When a less-clean reference source is utilized for the PLL, a wide loop bandwidth also leads to less suppression of the reference noise, *i.e.*, the PLL IPN will be degraded by the noisy reference.

Fig. 5.1 shows the simulated spectrum of the PLL output when different loop bandwidths are utilized. It can be seen although the reference noise and fractional spur can be suppressed with a narrower loop bandwidth, the DCO noise becomes stronger. Again, the optimum loop bandwidth should be selected such that the noise contribution from the reference path (*e.g.,* reference phase noise, fractional spur, TDC quantization noise, *etc.*) is equal to that from the DCO phase noise. If the DCO phase noise can be further improved, the loop bandwidth can be allowed to be narrower such that more reference noise can be filtered, and the fractional spur suppression effect can be stronger. Nevertheless, as the loop bandwidth becomes narrower, it is becoming increasingly difficult to suppress the phase noise contribution from DCO. This is because the DCO phase noise is dominated by the flicker noise, which features a 30 dB/dec roll-off rather than the thermal noise with a 20 dB/dec roll-off. This drives the need for the development of low-phase-noise oscillators, especially low-phase-noise LC oscillators for their noise superiority over the ring oscillator counterpart.

Another bottleneck in further suppressing the fractional spur is the on-chip isolation condition. Although a careful floorplan might benefit in achieving a good on-chip iso-

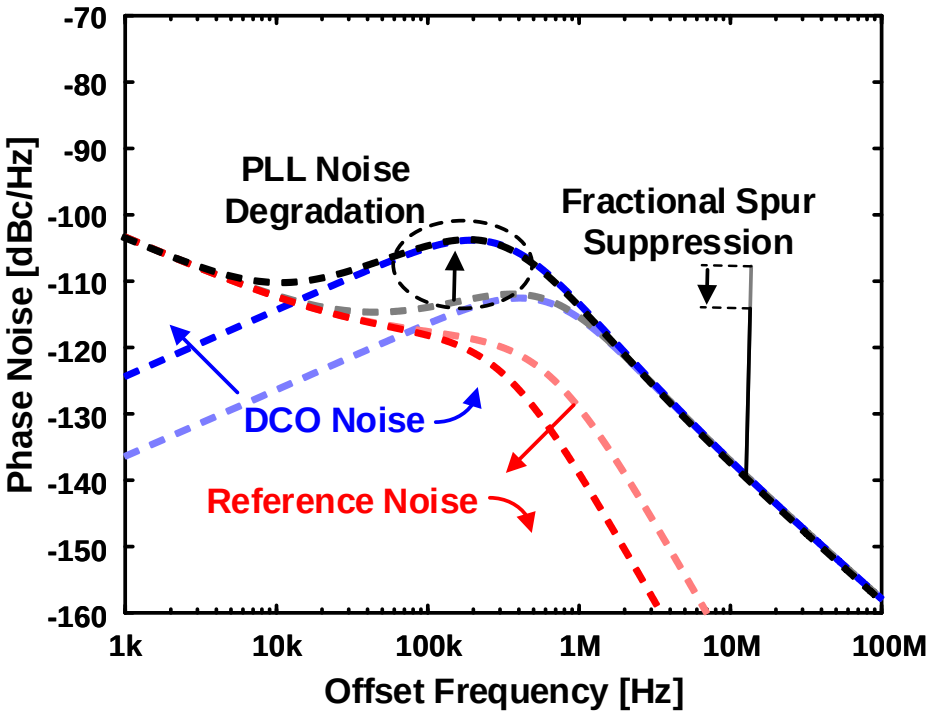


Figure 5.1: The PN spectrum of PLL with different bandwidths.

lation between different blocks, the guideline of how to achieve a good floorplan can sometimes be vague. This is because the disturbance to the DPLL can come from a lot of different sources. For example, when the DPLL is integrated in an SoC, the large transient current in the digital BB may generate strong ripples on the supply of DPLL even if a powerful LDO is utilized. On the other hand, the EM wave radiated from the high-power PA (or received by the antenna) can also be coupled to the supply of DPLL. Moreover, the DPLL itself is a mixed-signal system with multiple block circuits working at different frequencies. Cross-coupling also exists among those different blocks. To mitigate this problem, more robust topologies for the block circuits in DPLLs *i.e.,* TDC, DTC, and DCO, *etc.*, need to be developed.

To enable a narrow-band DPLL implementation and improve the overall DPLL robustness against supply disturbances, two novel block circuits will be presented shortly in this chapter: an LC oscillator which can achieve low flicker noise under nonideal decoupling networks, and a differential voltage-domain DSM QN cancellation block.

5.1 A Decoupling Network Q-Robust LC Oscillator

Numerous works have been conducted to reduce the VCO $1/f^3$ noise [44, 72–79]. One important technique to suppress the $1/f$ noise upconversion is to ensure high CM impedance at around twice the VCO frequency (f_{vco}) such that the noise current generated by the differential pair will not flow into the LC tank. In [44], the CM resonance was achieved by an extra LC tank inserted between the sources of the differential pair and the tail current source. Although the $1/f^3$ noise was effectively suppressed, the area overhead for the tail resonator was too large. Utilizing a two-turn inductor with carefully designed geometry, [73] realized differential-mode (DM) resonance at f_{vco} and CM resonance at $2f_{vco}$ within only one LC tank. Unfortunately the two-turn inductor introduced extra overlap area between metals at different layers, degrading the tank Q factor and the noise at $1/f^2$ region.

In [74], one transformer and a combination of differential and common-mode capacitor banks were exploited to achieve implicit CM resonance. Although excellent PN can be achieved in both $1/f^2$ and $1/f^3$ regions, the effect of implicit CM resonance is sensitive to the Q factor of the decoupling capacitor network, which might be bad when enough decoupling capacitors are not allowed by the tight area specification. In order to mitigate this issue, this section reports a VCO with a multi-tap transformer to avoid CM Q factor degradation caused by the nonideal decoupling network.

5.1.1 CM Q Factor Immunity against the Decoupling Network

Fig. 5.2 (a) shows the schematic and the equivalent CM impedance of the implicit CM resonance VCO in [74]. In real implementation, decoupling capacitors will be used to eliminate the supply/ground bouncing caused by the parasitic inductances and resistances from the bonding wires. Taking the decoupling capacitor into consideration, the equivalent CM impedance of the VCO in [74] can be expressed as:

$$Z'_{cm} = (s(1-k)L_{tk} + \frac{1}{sC_{de}} + R_{de}) || \frac{1}{sC_{cm}} || \frac{1}{sC_p}, \tag{5.1}$$

The L_{tk} in Eq.(5.1) is the inductance of one branch of the transformer, k is the coupling factor, C_{cm} is the CM capacitance, C_{de} is the decoupling capacitance, R_{de} is the parasitic resistance on the decoupling capacitor.

For frequencies near $2f_{vco}$, the impedance generated by C_{de} is negligible, thus Eq. (5.1) can be simplified as:

$$Z'_{cm} \approx (s(1-k)L_{tk} + R_{de}) || \frac{1}{sC_{cm}} || \frac{1}{sC_p}. \tag{5.2}$$

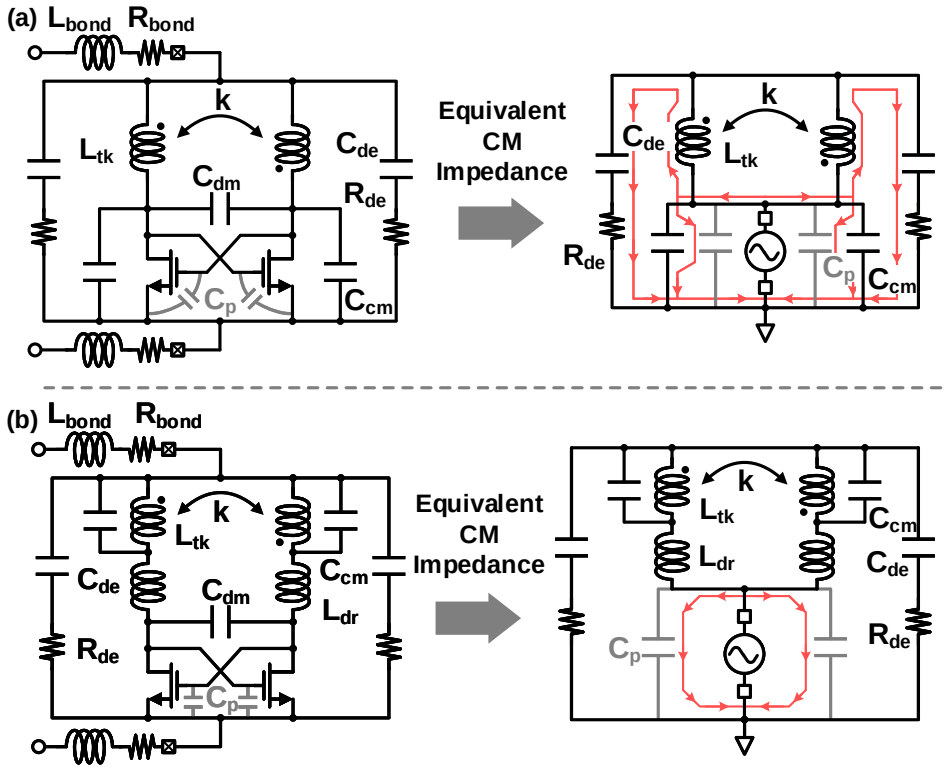


Figure 5.2: The schematics and equivalent CM impedances of (a) implicit-CM resonant VCO and (b) the proposed VCO.

It is implied from Eq. (5.2) that R_{de} from the decoupling network will directly affect the Q factor of the CM impedance.

Note that as explained in [75], the actual decoupling network also contains parasitic inductance. This inductance, however, is usually of very small value and thus will only be significant at high frequencies (*e.g.*, mmW). In the high-frequency scenario, $1/(sC_p)$ terms in the following equations should be replaced with sL_p correspondingly, which denotes the parasitic inductance. Nonetheless, R_{de} stays constant against varying frequencies, which means that the CM Q degradation is always happening for the VCO in [74]. As a result, the parasitic inductance on the decoupling network can be neglected in the foregoing analysis without affecting the effectiveness.

The proposed VCO is shown in Fig. 5.2 (b). In order to avoid the Q degradation of the CM impedance at around $2f_{vco}$, two inductors with an inductance of L_{dr} are inserted after the drain nodes of the differential pair. In this way, the implicit CM resonance tank can be "isolated" from the decoupling network. The equivalent CM impedance of the proposed

VCO can be derived as:

$$Z_{cm} = (sL_{dr} + s(1-k)L_{tk} || \frac{1}{sC_{cm}} + \frac{1}{sC_{de}} + R_{de}) || \frac{1}{sC_p}. \tag{5.3}$$

Because C_p is usually small, the above equation can be approximated as:

$$Z_{cm} \approx sL_{dr} + s(1-k)L_{tk} || \frac{1}{sC_{cm}} + \frac{1}{sC_{de}} + R_{de}. \tag{5.4}$$

Note thatC_p will actually introduce another pole to the CM impedance. However, the frequency of this pole will be above 20 GHz in real implementation, and thus will not affect the accuracy of this approximation.

It can be seen from Eq. (5.4) that R_{de} only adds a fixed value to the CM impedance. For L_{tk} and C_{cm} resonating at $2f_{vco}$, infinite CM impedance can be obtained. As a result, the Q factor of the CM impedance in the proposed VCO is less sensitive to the Q factor of the decoupling network (in real case, the CM impedance of the proposed VCO is finite, which will be limited by the Q factor of L_{tk} and C_{cm}).

5.1.2 DM Impedance Analysis

The DM impedance of the proposed VCO is also of interest, which can be expressed as:

$$\begin{aligned} Z_{dm} &= (sL_{dr} + s(1+k)L_{tk} || \frac{1}{sC_{cm}}) || \frac{1}{s2C_{dm}} || \frac{1}{sC_p} \\ &= \frac{s(L_{dr} + (1+k)L_{tk}) + s^3(1+k)L_{tk}L_{dr}C_{cm}}{1 + s^2\alpha + s^4\beta}, \end{aligned} \tag{5.5}$$

where $\alpha = (1+k)L_{tk}(C_{cm}+2C_{dm}+C_p)+L_{dr}(2C_{dm}+C_p)$, $\beta = (1+k)L_{tk}L_{dr}C_{cm}(2C_{dm}+C_p)$.

The above equation implies the existence of two zeros and two poles in the DM impedance of the proposed VCO, which may raise the concern about oscillation mode ambiguity. Fortunately, the oscillation mode ambiguity can be eliminated by the following two mechanisms:

1. In real implementation, the position of the high-frequency zero is placed close to the high-frequency pole such that the value of $|\ Z_{dm}\ |$ is much lower at the high-frequency pole compared to the value of $|\ Z_{dm}\ |$ at the low-frequency pole.

2. The Q factor of the LC tank is optimized for the low-frequency pole. For higher frequencies, tank Q factor will be significantly lower, which will further suppress the oscillation at the high-frequency pole.

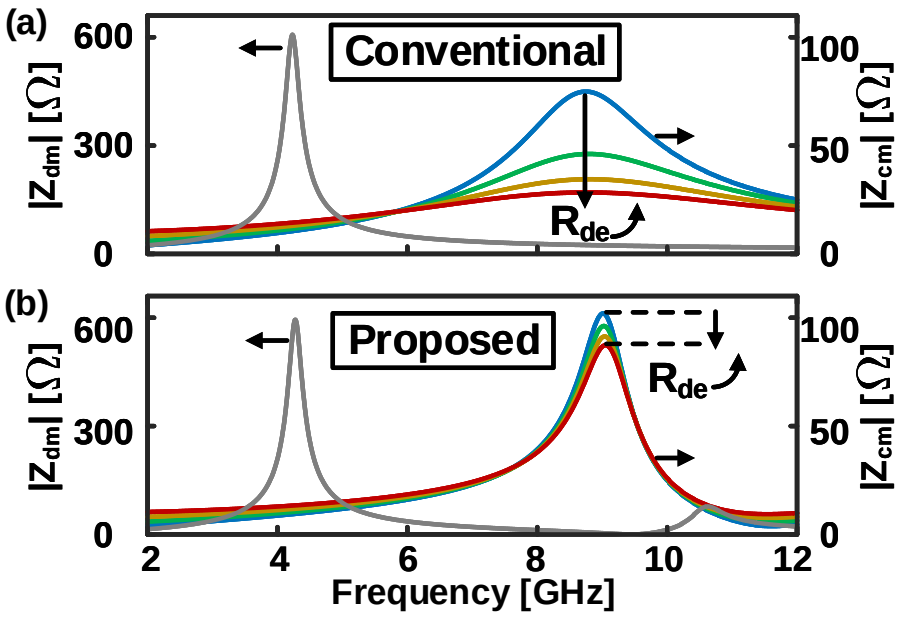


Figure 5.3: The simulated DM and CM impedance of the LC tank (a) in the conventional configuration, and (b) in the proposed configuration.

The DM impedance simulation of the proposed VCO is shown in Fig. 5.3 (b). It can be seen that $|Z_{dm}|$ at the high-frequency pole (around 11 GHz) is almost negligible compared to $|Z_{dm}|$ at the low-frequency pole (around 4.4 GHz), indicating no oscillation mode ambiguity.

5.1.3 PN Improvement under Low-Q Decoupling Network

Tank impedance and PN simulations are conducted to check the robustness of the proposed VCO against low-Q decoupling network. In the simulations, ideal C_{dm}, C_{cm}, and C_p are used. C_{de} is fixed at 30 pF, while R_{de} is swept from 5 Ω to 20 Ω (increased by 4 times). A multi-tap transformer, which will be disclosed in the next section, is used to implement L_{dr} and L_{tk} without much area overhead. The s-parameters of the transformer are also included in the simulations.

The tank impedance simulation result of the proposed VCO is shown in Fig. 5.3 (b). C_{dm} and C_{cm} are selected to match the peaks of $|Z_{dm}|$ and $|Z_{cm}|$ to f_{vco} and $2f_{vco}$, respectively. C_p = 60 fF is selected to mimic the parasitc capacitance from the layout. It can be seen that as R_{de} increases from 5 Ω to 20 Ω, the peak CM impedance decreases from 104 Ω to 77 Ω, corresponding to only 26% degradation. As shown in Fig. 5.4 (b),

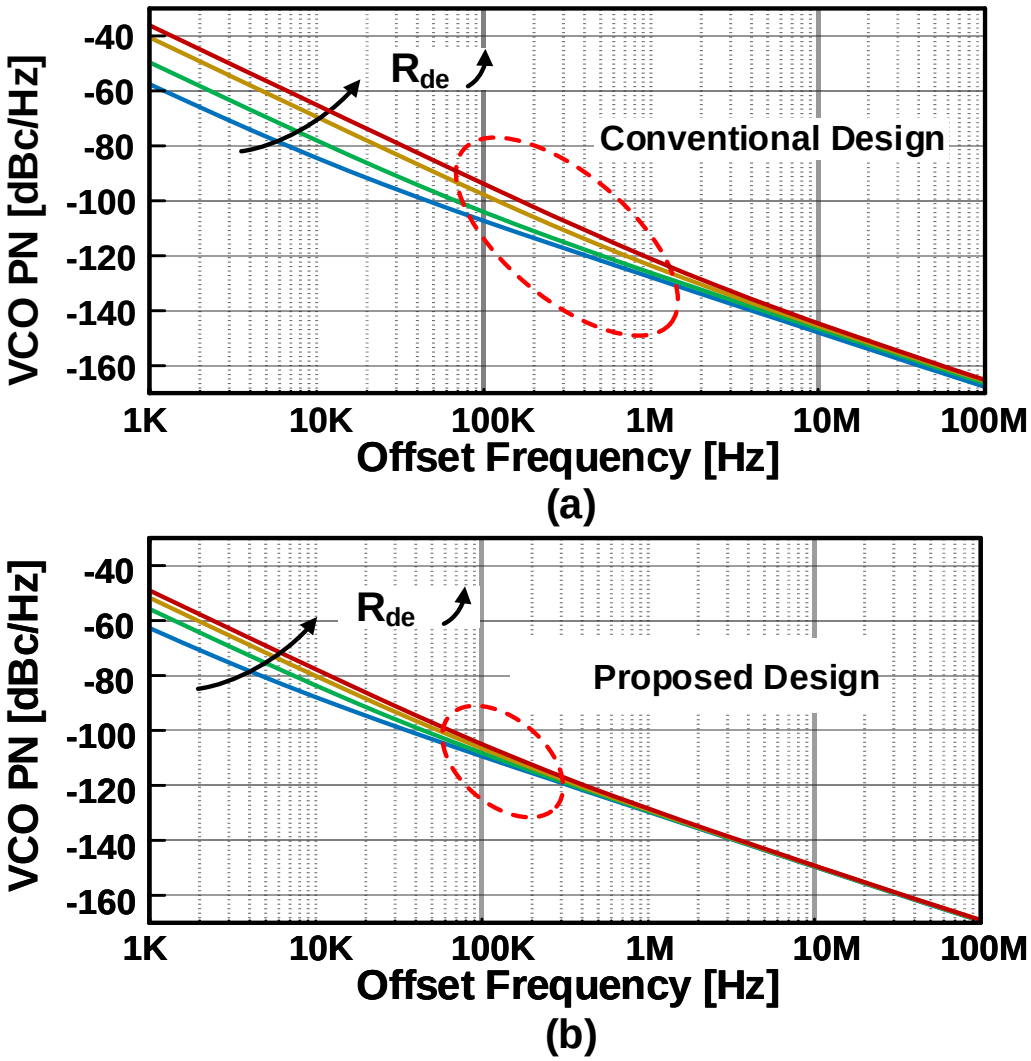


Figure 5.4: Simulated PN versus different R_{de} of (a) the conventional implicit CM resonance VCO and (b) the proposed VCO.

the PN of the proposed VCO is also simulated. It can be seen that the $1/f^3$ corner stays less than 200 kHz while R_{de} increases by 4 times.

Note that if C_{cm} is eliminated, and C_p is adjusted to construct the high CM impedance at $2f_{vco}$, the proposed VCO becomes equivalent to the conventional implicit CM resonance VCO. The tank impedance and VCO PN in this configuration are also simulated for a comparison. It is shown in Fig. 5.3 (a) that the peak CM impedance will be degraded from 86 Ω to 20 Ω, which is much worse than the CM impedance of the proposed design. As a result, the $1/f^3$ corner of the VCO is degraded from less than 100 kHz to larger than 1 MHz.

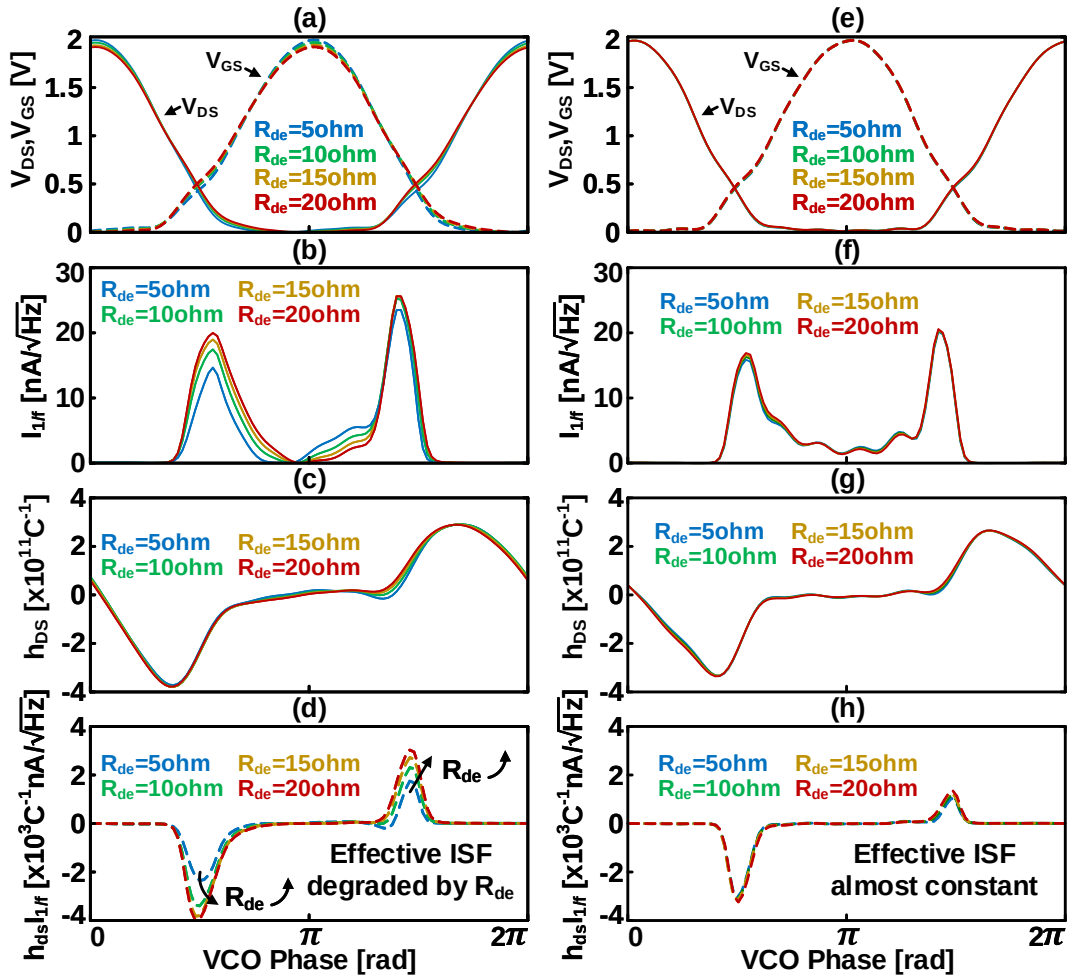


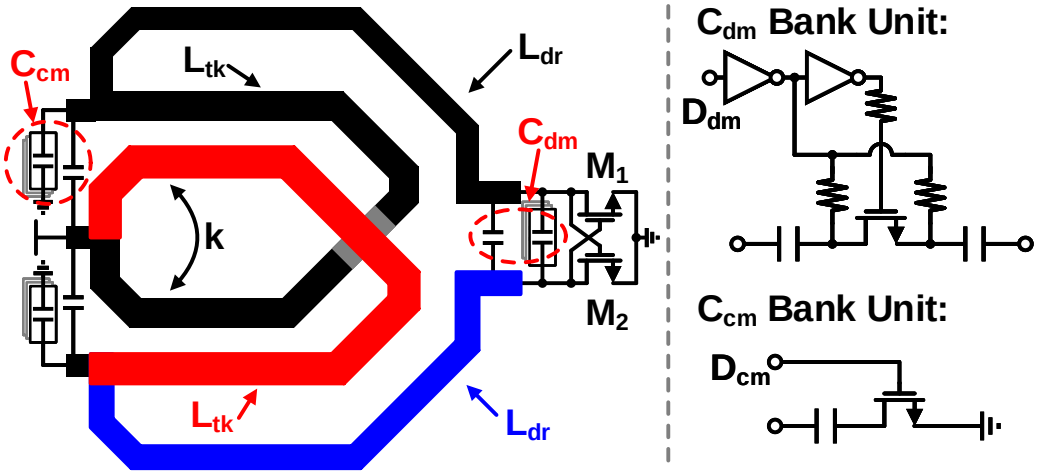
Figure 5.5: Simulated V_{DS}, V_{GS}, $I_{1/f}$, h_{DS}, $h_{DS}I_{1/f}$ of (a)-(d) the conventional implicit CM resonance VCO, and (e)-(h) of the proposed VCO.

The flicker noise upconversion mechanism is further investigated to evidence the effect of the proposed VCO. According to the theory of impulse sensitivity function (ISF) [80, 81], the VCO phase distortion $\phi(t)$ induced by the flicker noise current $I_{1/f}(t)$ at a certain frequency offset Δf can be calculated by:

$$\phi(t) = \int_{-\infty}^{t} h_{DS}(\tau) I_{1/f}(\tau) d\tau, \tag{5.6}$$

where $h_{DS}(t)$ is the non-normalized ISF, and $h_{DS}(t)I_{1/f}(t)$ is the effective non-normalized ISF.

The simulated drain-to-source voltage (V_{DS}), gate-to-source voltage (V_{GS}), $h_{DS}(t)$, $I_{1/f}(t)$ when Δf = 1 kHz, and $h_{DS}(t)I_{1/f}(t)$ of the conventional VCO and the proposed VCO



Key Elements	$M_{1,2}$	C_{cm}	C_{dm}	L_{dr}	L_{tk}	K
Design Parameters	58um/60nm	0.8~1.1pF	0.58~0.76pF	420pH	405pH	0.28

Figure 5.6: Detailed schematic and key design parameters of the proposed VCO.

are shown in Fig. 5.5 (a)-(d), and (e)-(h), respectively. It can be observed that the effective non-normalized ISF of the proposed VCO stays almost constant when R_{de} increases from 5 Ω to 20 Ω. On the other hand, the amplitude of the effective non-normalized ISF of the conventional implicit CM resonance VCO increases by almost two times when R_{de} increases from 5 Ω to 20 Ω. As a result, the flicker noise current will generate more phase disturbance in the conventional implicit CM resonance VCO, which is in agreement with the PN simulation result.

5.1.4 Implementation of the Proposed VCO

The detailed schematic of the proposed VCO with the above-mentioned multi-tap transformer and other key design parameters are shown in Fig. 5.6. The size of the NMOS differential pair is 58 um/ 60 nm. The capacitor bank of C_{cm} is designed to cover a range of 0.8 to 1.1 pF. The capacitor bank of C_{dm} is designed to cover a range of 0.58 to 0.76 pF. The L_{dr} is designed to be 420 pH. The two L_{tk}s are designed to be 405 pH with a coupling coefficient of 0.28. The switches in the capacitor banks are used as NMOSs in order to take advantage of low on-resistance. Although part of the CM current is still flowing through the C_{cm} bank to the ground, the CM Q degradation in the proposed VCO is negligible because the total amount of CM current flowing through the maximally 0.3 pF

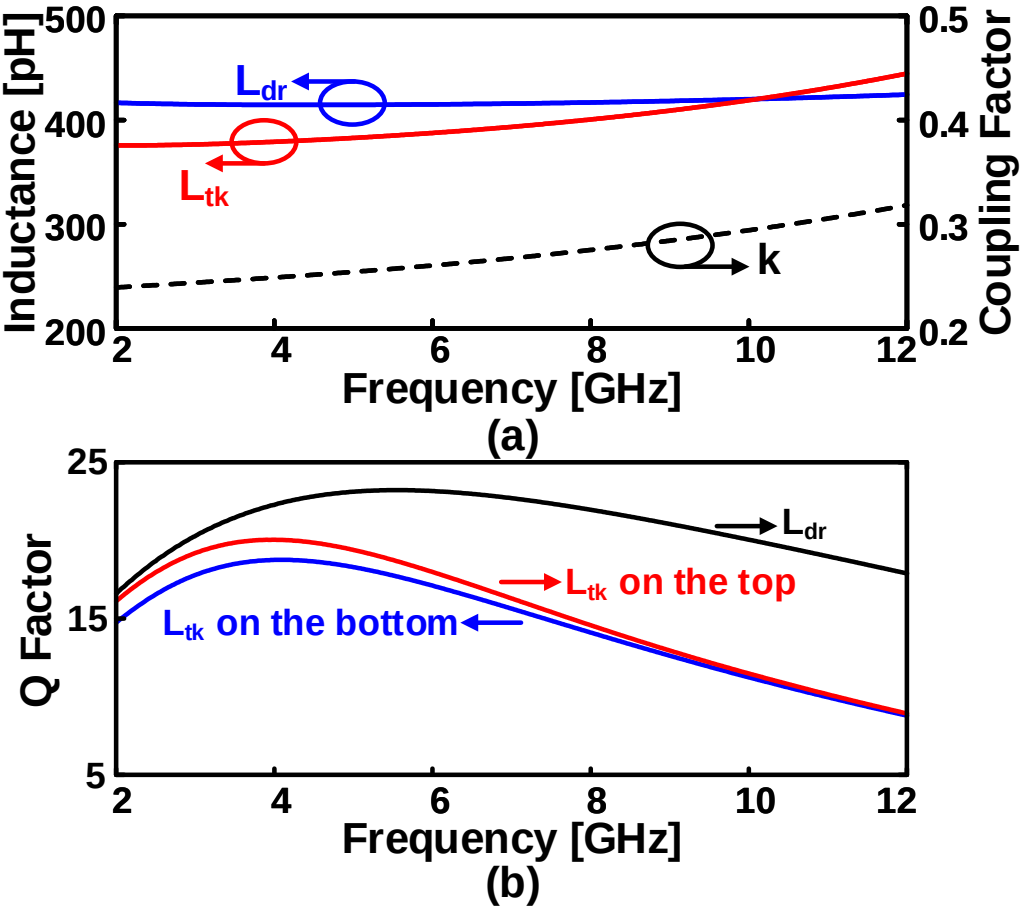


Figure 5.7: EM simulation results of the muti-tap transformer.

C_{cm} bank is limited. Besides, the CM current flows only locally through the decoupling network, leading to less loss on the parasitic resistance.

The geometries of the multi-tap transformer are optimized for achieving good Q factors within a limited die area. Note that for the target operation frequency, implementing L_{tk} and L_{dr} in the proposed multi-tap transformer leads to the minimum on-chip area. Nonetheless, for other frequency ranges, the two L_{dr}s might be implemented as two separate compact spirals for saving the die area. EM simulations are used to derive the inductance values of L_{tk} and L_{dr}, and the coupling factor. The simulation results are shown in Fig. 5.7 (a). For the VCO output frequency range, L_{tk} is around 405 pH, L_{dr} is around 420 pH. The coupling factor between the two L_{tk} branches is 0.28. The simulated Q factors of L_{tk} and L_{dr} are shown in Fig. 5.7 (b). It shows that the Q factor of L_{dr} at the VCO frequency range is around 23, while the Q factors of the two L_{tk}s are both around 13 at

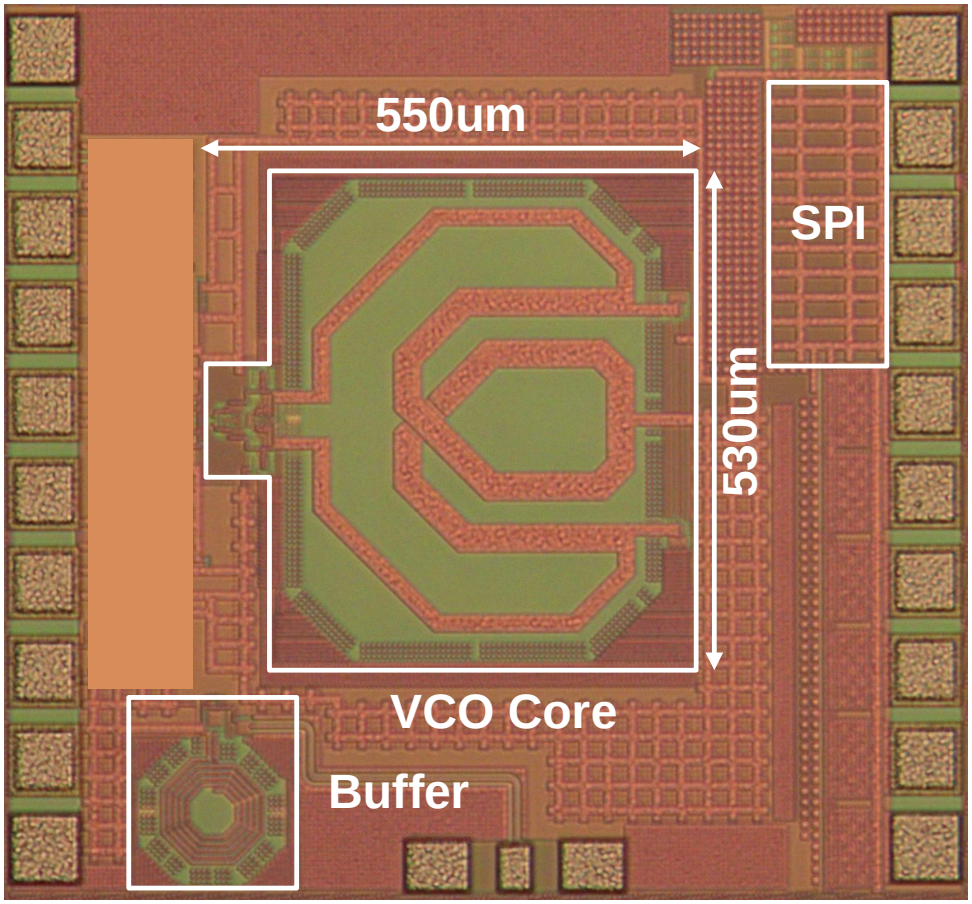


Figure 5.8: Chip photo of the implemented LC oscillator.

twice the VCO frequency range.

5.1.5 Measurement Results

A prototype of the proposed VCO is implemented on 65-nm CMOS process, which is shown in Fig. 5.8. The core area of the proposed VCO is 0.29 mm^2. When working under a 0.7 V supply voltage, the output frequency range of the proposed VCO is from 4.24 GHz to 4.8 GHz. The power consumption at the minimum output frequency (f_{min}) is 4.9 mW, while it is 4.2 mW at the maximum output frequency (f_{max}).

The measured PN spectra of the proposed VCO at f_{min} and f_{max} are shown in Fig. 5.9. At the minimum output frequency of around 4.24 GHz, the phase noise at 1 MHz frequency offset is measured to be -127.44 dBc/Hz. On the other hand, when the output frequency is fixed at the maximum frequency *i.e.,* 4.8 GHz, the phase noise at 1 MHz frequency offset is measured to be -126 dBc/Hz.

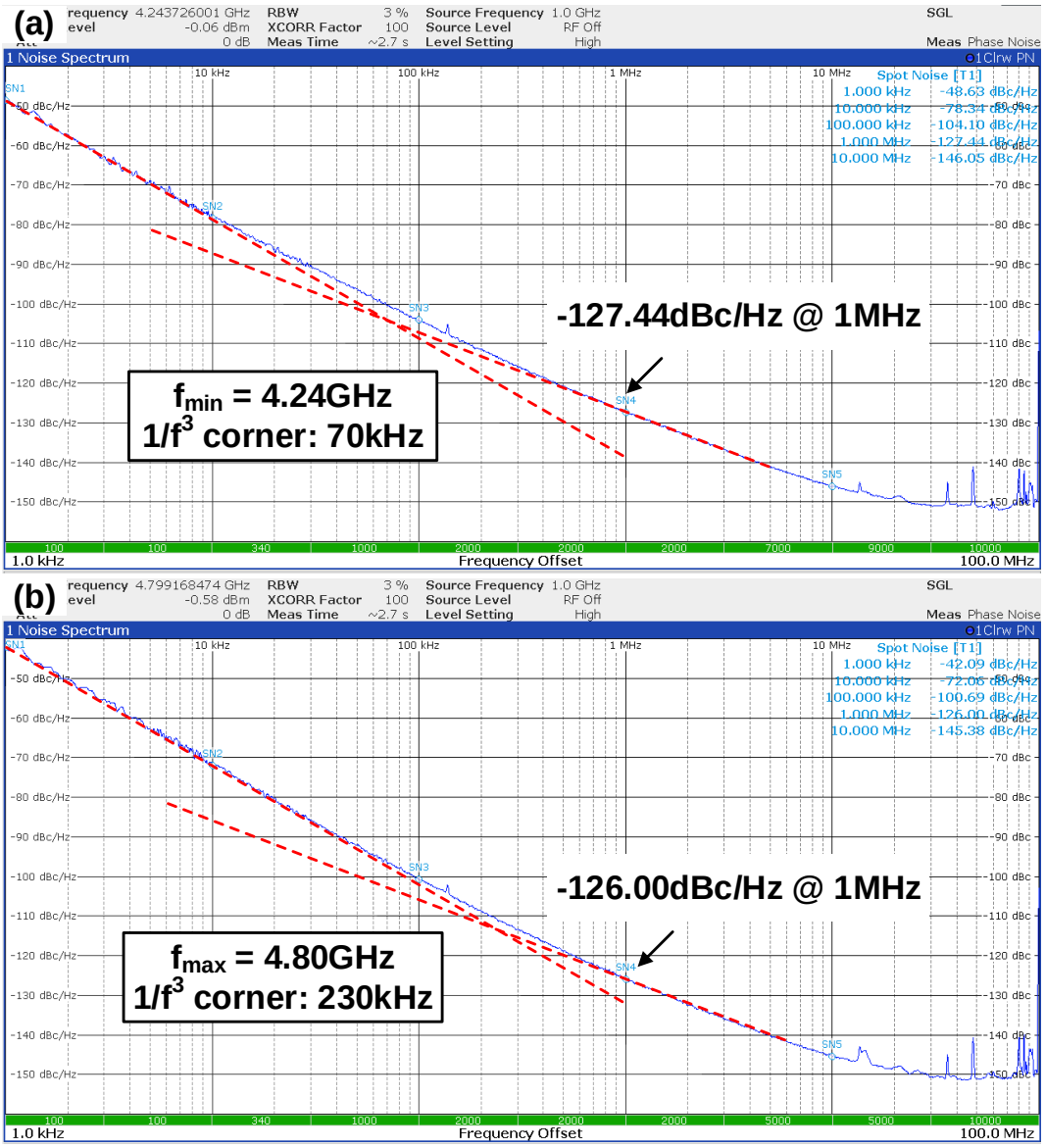


Figure 5.9: Measured VCO PN at (a) the minimum frequency of 4.24 GHz and (b) the maximum frequency of 4.80 GHz.

The measured $1/f^3$ corner, PN at 1 MHz f_{ofst}, and thermal region FoM across the VCO frequency range are shown in Fig. 5.10. It can be seen that the $1/f^3$ corner frequency increases with an increasing VCO output frequency. It achieves a lowest value of 70 kHz at the minimum VCO frequency, and the highest value of 230 kHz at the maximum VCO frequency. The reason can be mostly ascribed to the degraded tank quality factor at twice the VCO frequency, which can be evidenced by the EM simulation result in 5.7 (b). As a result of the increased $1/f^3$ corner frequency, the phase noise at 1 MHz f_{ofst} is also

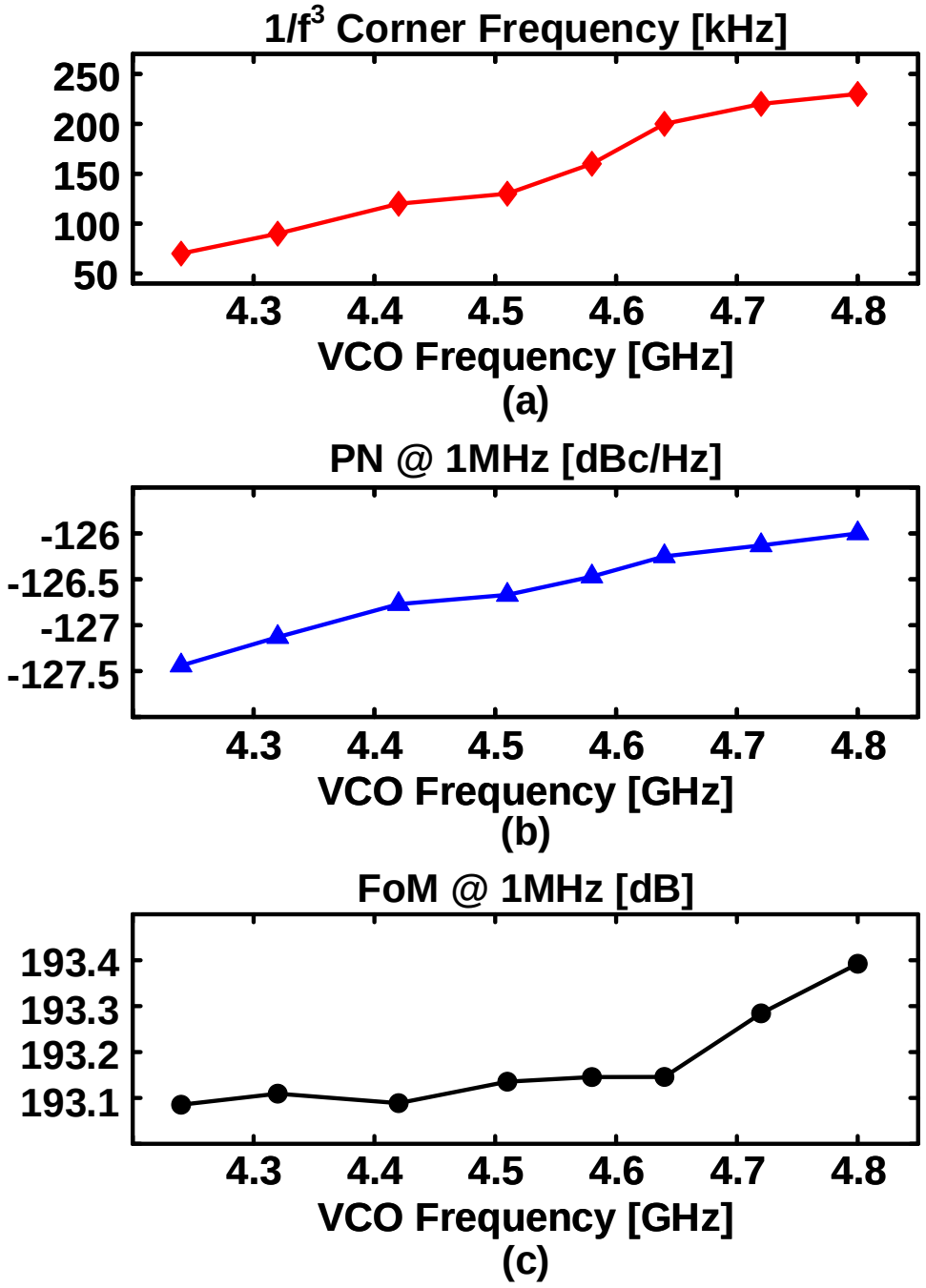


Figure 5.10: Measured VCO performance at different frequencies.

slightly degraded if the VCO frequency becomes higher. The FoM of the VCO on the other hand, does not change much across the VCO frequency range. Rather, a relatively higher FoM can be achieved at the maximum VCO frequency because of a slightly lower power consumption.

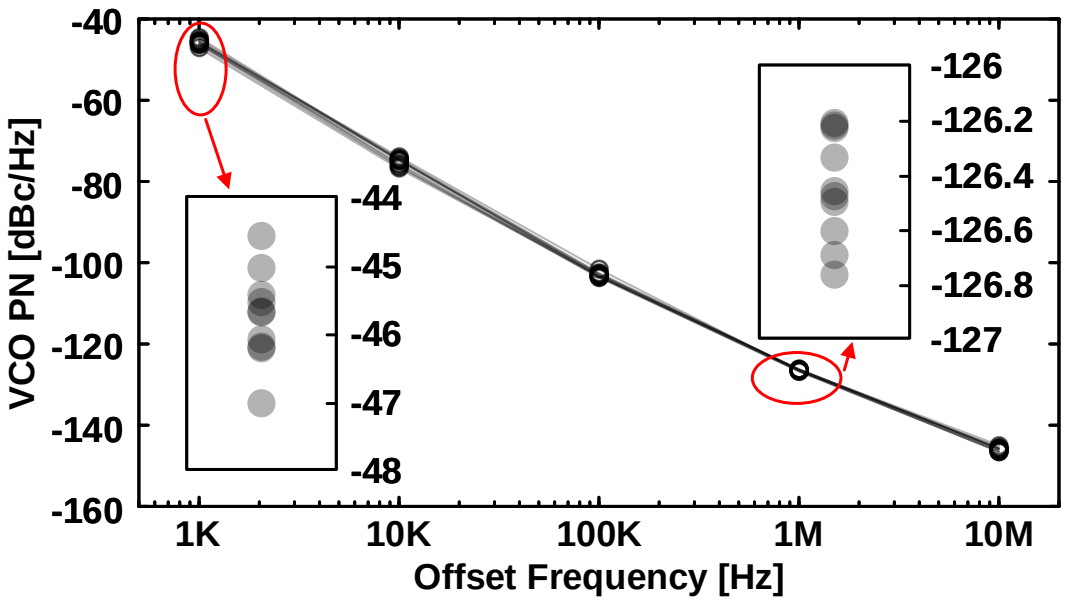


Figure 5.11: Measured VCO PN at different offset frequencies across 10 different chips (f_{vco} fixed at 4.4 GHz).

The supply pushing of the prototype at 4.4 GHz is measured to be 56 MHz/V, which is mainly limited by the parasitic varactors on the cross-coupled pair. Further supply pushing can be achieved by the adoption of an LDO on the VCO supply.

In order to verify the robustness of the proposed VCO against process variation, 10 different chips from one slot are measured. The measured phase noise from the 10 different chips at a frequency of 4.4 GHz are shown in Fig. 5.11. It can be seen that the performance variation across different chips is very limited. In the flicker noise region (at 1 kHz f_{ofst}), the VCO phase noise varies from -47 dBc/Hz to -44.5 dBc/Hz. In the thermal region (at 1 MHz f_{ofst}), the VCO phase noise varies from -126.8 dBc/Hz to -126.2 dBc/Hz.

A performance summary of recent low-flicker noise VCOs is shown in Table 5.1. Thanks to the proposed topology, the parasitic resistance in the decoupling network will not degrade the CM impedance at $2f_{vco}$, resulting in a low $1/f^3$ corner from 70 kHz to 230 kHz. Moreover, this robustness improvement does not require an extra passive elements on the chip, leading to a compact chip area. Meahwhile, there is only one metal cross-over in the proposed single-turn multi-tap transformer, which in turn benefits in a high Q factor of the LC tank. As a result, the thermal region VCO phase noise is also comparable to the existing low-flicker-noise LC oscillators.

Table 5.1: Comparison to Other Low Flicker Noise VCOs

	This Work	JSSC'17 D. Murphy	JSSC'16 M. Shahohammadi	ISSCC'21 H. Guo	SSCL'22 X. Lin
Topology	Implicit CM Resonance + Multi-tap XFMR	Implicit CM Resonance	Class-D/F2	Head Resonator	Class-D + PTV Inductor
Process	65nm	28nm	40nm	65nm	65nm
Supply Voltage [V]	0.7	0.9	0.5	0.4	0.35
Frequency [GHz] (Tuning Range)	4.24/4.80 (12.4%)	2.85/3.75 (27.3%)	3.3/4.5 (30.7%)	5/6.36 (23.9%)	3.68/4.44 (18.7%)
Phase Noise @ 1MHz [dBc/Hz]	-127.4/-126	-131/-127.5	-123.4/-119	-128.4/-125	-129.1/-124.8
Power [mW]	4.9/4.2	6.6	4.1/2.5	6.1/3.36	4.95/4.2
Thermal Region FoM* [dB]	193.1/193.4	192.5/192	187.6/188	195.1/196.9	194.9/194.2
$1/f^3$ Corner [Hz]	70k/230k	200k	60k/100k	90k/180k	230k/450k
Core Area [mm2]	0.29	0.15	0.24	0.24	0.12
Passives	1	1	1	2	1

*FoM = $-$ PN + $20\log_{10}(f_{vco}/f_{ofst}) - 10\log_{10}(P_{DC}/1mW)$

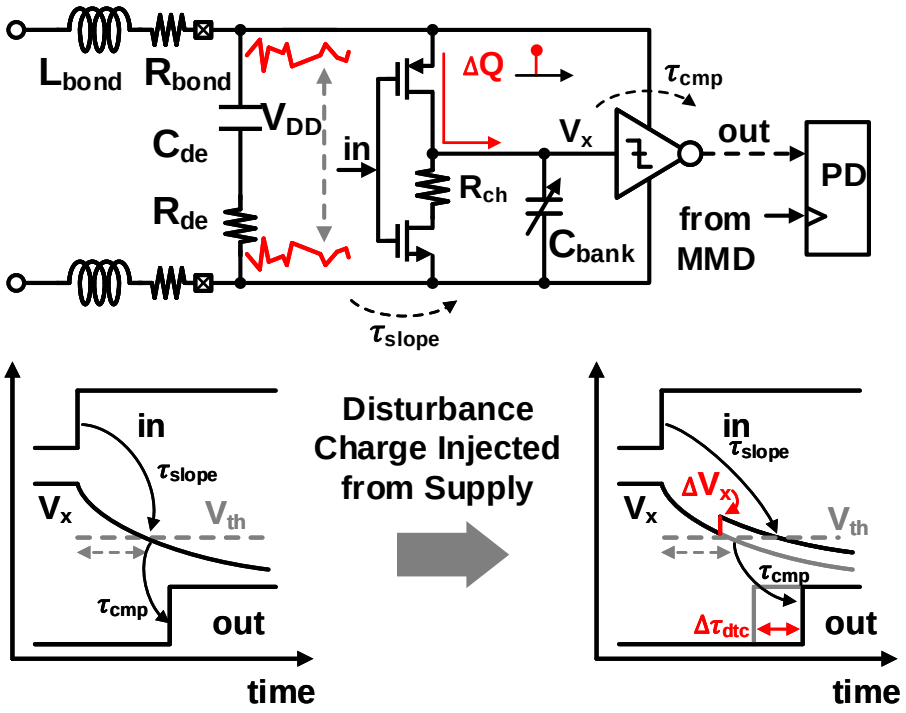


Figure 5.12: DTC INL degradation due to supply ripples.

5.2 Differential Voltage Domain DSM QN Cancellation Technique

5.2.1 Supply Seneitivity and Noise Penalty in DTC-based DPLLs

As mentioned earlier, current DTC topologies are generally prone to supply disturbances. This is because current DTC topologies require a comparator to recover the sharp transition edge at the output. The VS-DTC operation is shown in Fig. 5.12 as an example. When the rising edge comes at the input, the voltage at the V_x node starts to discharge from V_{DD}. When the VS-DTC is working with an ideal supply, the discharging process can be well described by the following equation:

$$V_x(t) = V_{DD} exp(\frac{-t}{R_{ch}C_{bank}}). \tag{5.7}$$

When V_x crosses V_{th}, a rising edge will be triggered at the DTC output, which is used for the PD to estimate the phase error of the DCO. It can be seen that the DTC

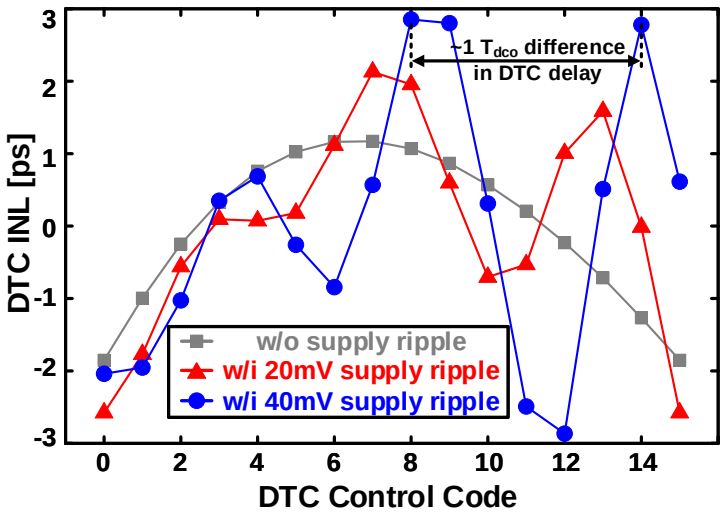


Figure 5.13: DTC INL degradation due to coupled DCO ripples.

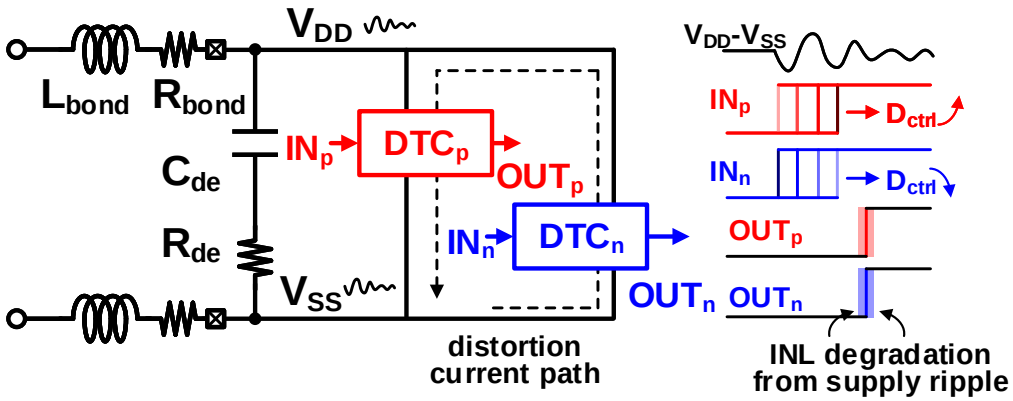


Figure 5.14: DTC INL degradation due to self-interference ripples.

delay is contributed by two parts: the delay generated by the RC slope generator τ_{slope} and the delay generated by the comparator τ_{cmp}. The slope generator delay can be easily calculated as:

$$\tau_{slope} = R_{ch}C_{bank}ln(\frac{V_{DD}}{V_{th}}). \tag{5.8}$$

When a disturbance charge of amount ΔQ is injected from the DTC supply before V_x reaches V_{th}, a corresponding voltage disturbance will be generated at the top plate of the

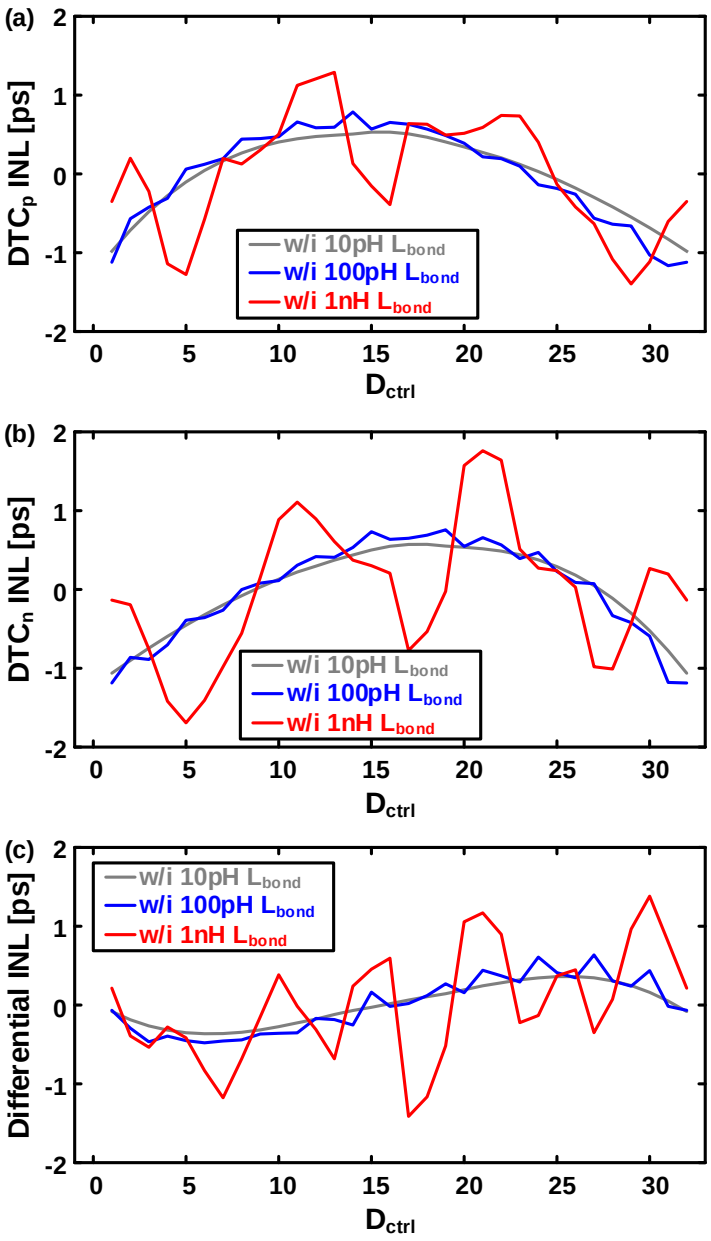


Figure 5.15: DTC INL degradation due to self-interference ripples.

charging capacitor C_{bank}. The voltage disturbance amplitude can be simply calculated as $\Delta V_x = \Delta Q/C_{bank}$. After the injection of disturbance charge, the ideal discharging trace will be shifted, which results in a shorter or longer τ_{slope}. The DTC delay error caused by ΔQ can be calculated by:

$$\Delta\tau_{dtc} \approx \Delta V_x / |\frac{dV_x(t)}{dt}|_{t=\tau_{slope}}| = \frac{\Delta Q}{C_{bank}} \frac{R_{ch}C_{bank}}{V_{th}} = \frac{\Delta Q R_{ch}}{V_{th}}. \quad (5.9)$$

Eq. (5.9) shows that the delay of VS-DTC is prone to supply distortion. The source of the supply distortion, however, may come from different mechanisms. For example, the EM wave radiated by the DCO might be coupled to the supply network of the DTC, noise current from the digital logics might cause the bouncing of substrate voltage, *etc.* An example is shown in Fig. 5.13, where the INL of a VS-DTC is simulated with DCO-frequency ripple on the suuply. The VS-DTC delay range is set to 400ps, while the DCO frequency is set to 7 GHz. It can be seen that the INL profile contains a component that repeats itself when DTC control code increases by around 5 to 6, which corresponds to one DCO period. Moreover, as the supply ripple amplitude increases to 40 mV, the DTC INL can be degraded to $\pm$3 ps, which is two times larger than the case where no supply ripple is injected.

Similar mechanisms also exist in DCO, PD, reference buffer, and output buffer, which lead to spur and noise performance degradation in the PLLs together. However, the suppression of this type of inter-block coupling spurs relies heavily on the physical distance between different blocks, the performance of supply regulators, the number of decoupling capacitors, and separating supplies according to operation frequencies. As a result, the suppression of those kind of spur or noise degradation is not in the scope of this thesis.

On the other hand, the DTC itself also injects disturbance current pulses to the supply network, which induces code-dependent ripples on the supply and thus memory effects in the DTC delay [54]. Similar to the effect of replica DTCs in [43] and [54], the PD-DTC introduced in Chapter 4 can partially convert code-dependent supply ripples to code-independent ripples. However, because the two DTCs are drawing current at the same time from the supply network, self-interference can still happen in either a pair of replica DTCs or a pair of PD-DTCs.

This effect is illustrated in Fig. 5.14. When the PD-DTC pair is implemented in a DPLL, the outputs of $\mathrm{DTC_p}$ and $\mathrm{DTC_n}$ should always align with each other given the DTC gain is properly calibrated. However, when the supply network is not ideal, the parasitic L_{bond} and C_{de} will be excited by the transient current flowing through the two DTCs, and exhibit damped oscillation. When the capacitor banks of the two DTCs are being charged together, distortion current can circulate between the two DTCs, which will further lead to variation in the charging speed and thus DTC delay/INL. It should be emphasized that this mechanism is different from the memory effect reported in [54]: even if the PD-DTC supply is fully settled before the arrival of its two inputs, the DTC

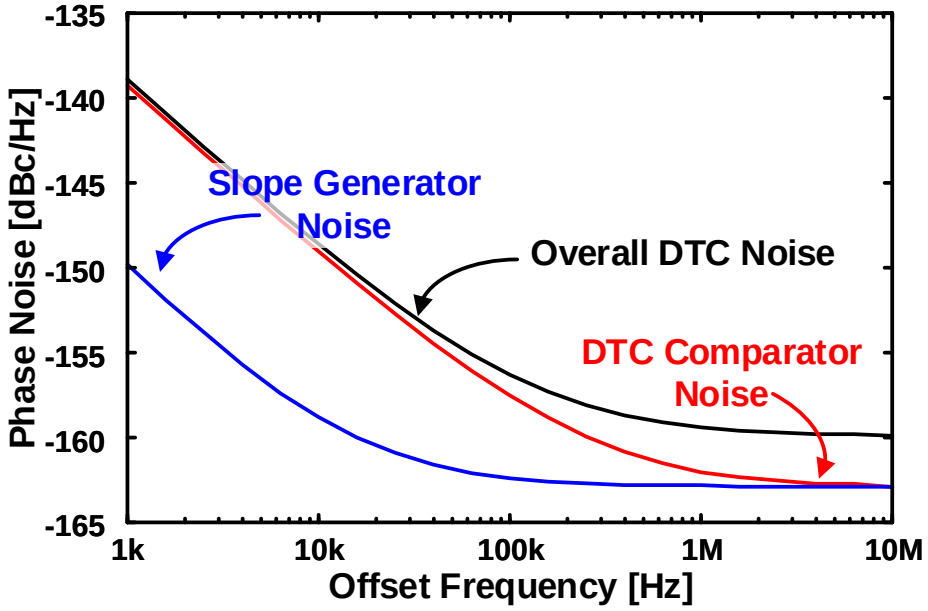


Figure 5.16: DTC phase noise breakdown.

delay/INL variation will still happen.

Fig. 5.15 shows the simulated INL of a pair of PD-DTCs with self-interference supply ripples. In the simulation, L_{bond} is selected between different values for controlling the amplitude of self-interference supply ripple, while R_{bond}, C_{de}, and R_{de} are fixed as 1 Ω, 100 pF, and 1 Ω, respectively. When L_{bond} becomes larger, the supply ripple amplitude also becomes larger, leading to a worse INL performance. The equivalent PD-DTC delay range is approximately 280 ps. It can be seen that when L_{bond} is 10 pH, almost no INL degradation happens in the PD-DTC pair, leading to a differential INL of $\pm$ 300 fs. However, when an L_{bond} of 1 nH is applied, the DTC INL is dominated by the ripple-induced delay variation, showing a peak amplitude of larger than 1.2 ps.

Despite the INL degradation when the DTC is working under a non-ideal supply, the comparator in the DTC also introduces considerable phase noise to the DTC output. Fig. 5.16 shows the noise breakdown of the VS-DTC in Fig. 5.12. It can be seen that the phase noise in the flicker noise region is mainly dominated by the noise from DTC comparator. This is because the input SR at the comparator input is usually low, which is limited by the DTC delay range and the deliberately increased fixed capacitance for achieving lower INL.

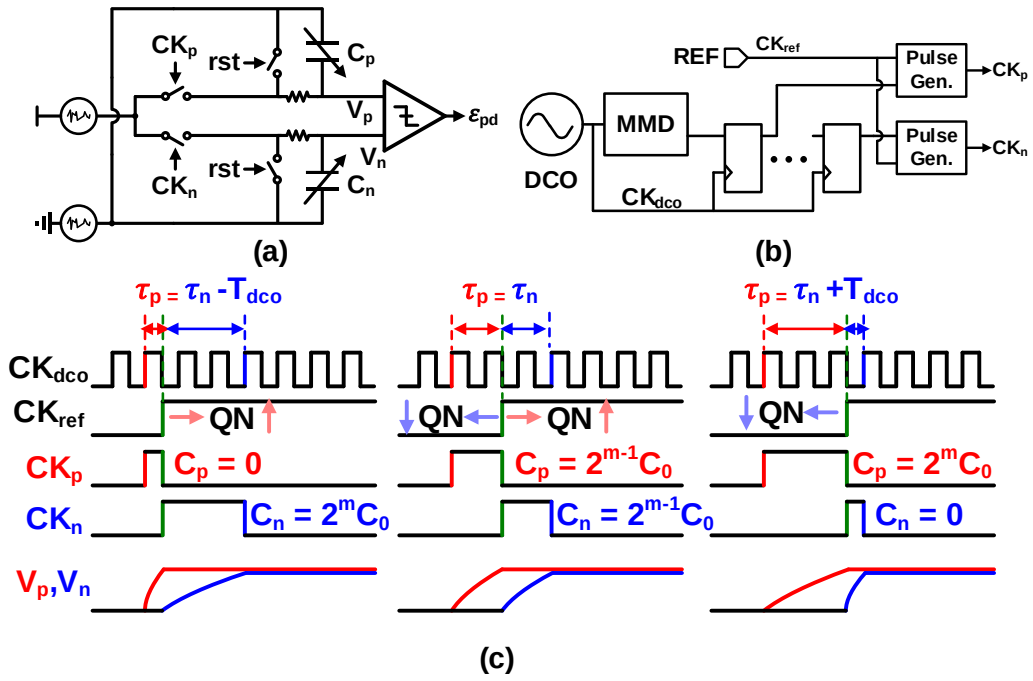


Figure 5.17: Concept of the VDQNC technique.

5.2.2 Voltage Domain DSM QN Cancellation Concept

One interesting fact can be observed from Fig. 5.12: the DPLL actually contains two consecutive comparators. The first comparator is the one utilized for recovering the sharp transition edge on the DTC output. The second comparator is the PD itself, where the phases of its two inputs are compared.

In order to eliminate the noise penalty caused by the DTC comparator, and in order to improve the DTC robustness against supply ripple, we proposed a voltage domain DSM QN cancellation (VDQNC) technique. The schematic of the proposed circuit is shown in Fig. 5.17 (a). The major difference between the VDQNC and the PD-DTC is that the comparators from the two DTCs are eliminated. Instead, a voltage comparator is utilized to compare the charged voltages at V_p and V_n. The charging window of capacitor banks C_p and C_n are controlled by the clock signals CK_p and CK_n, respectively. The generation of $CK_{p,n}$ is shown in Fig. 5.17 (b). The MMD output is retimed multiple times by the DCO signal, which is then utilized together with the CK_{ref} to generate the charging window.

The operation of the VDQNC is illustrated in Fig. 5.17 (c). When the DPLL is working in fractional-N mode, the phase difference between the MMD output and the reference will be changed by the DSM QN, which will affect the width of the charging

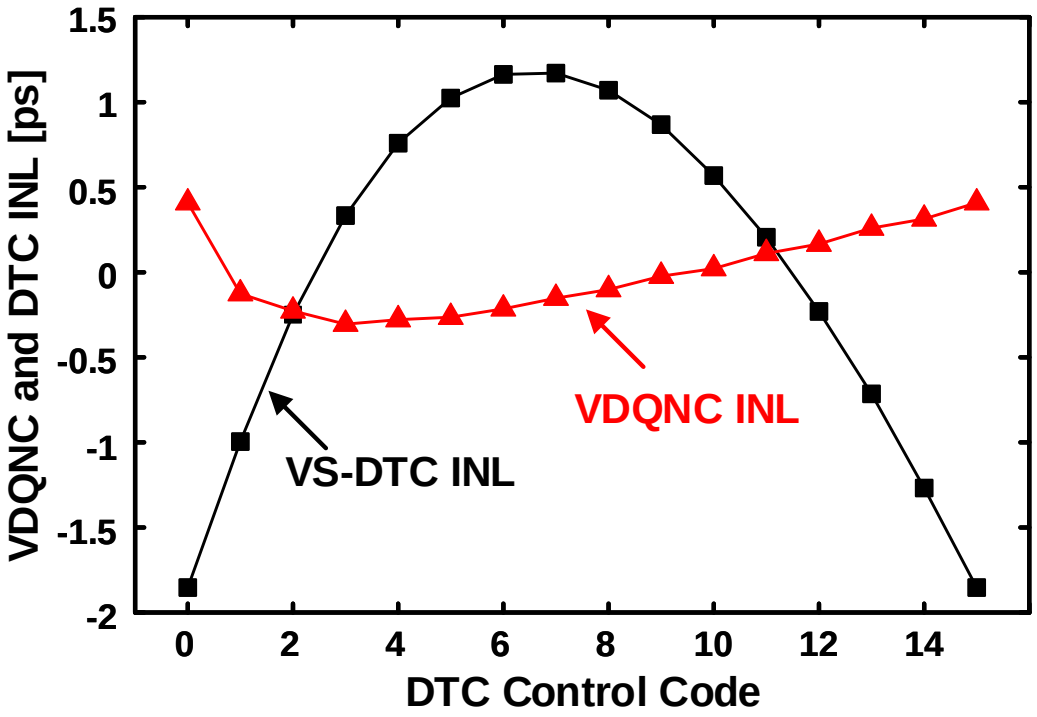


Figure 5.18: INL reduction effect in the VDQNC technique.

window $CK_{p,n}$. When the DSM QN becomes larger, the width of CK_p becomes larther, and the width of CK_n becomes narrower. The variation of the charging window width results in the difference between the final voltage of V_p and V_n in the corresponding reference cycle. Similar to a conventional VS-DTC, the DSM QN is cancelled by different C_p and C_n, such that the final voltage of V_p can be almost the same of V_n, which depends only on the DCO phase error at the same reference cycle.

Be cause the phase error is detected in voltage-domain, no slope-dependent nonlinearity is generated at the comparator, which leads to a suppression of INL compared to conventional DTC-based QN cancellation techniques. A comparison of the DTC INL with and without the nonlinear τ_{cmp} is shown in Fig. 5.18, where a more than 5-fold INL reduction can be observed.

Moreover, the proposed VDQNC is also less-sensitive to the self-interference supply ripple. This characteristic is illustrated in Fig. 5.19. When C_p is being charged, CK_p is high and CK_n is low, thus the distortion current will not flow through C_n. Similarly, when C_n is being charged, no distortion current will flow through C_p. Consequently, less INL degradation from the self-interference supply ripple can be expected in the proposed VDQNC. The equivalent INL of the VDQNC under different L_{bond}s is simulated for ver-

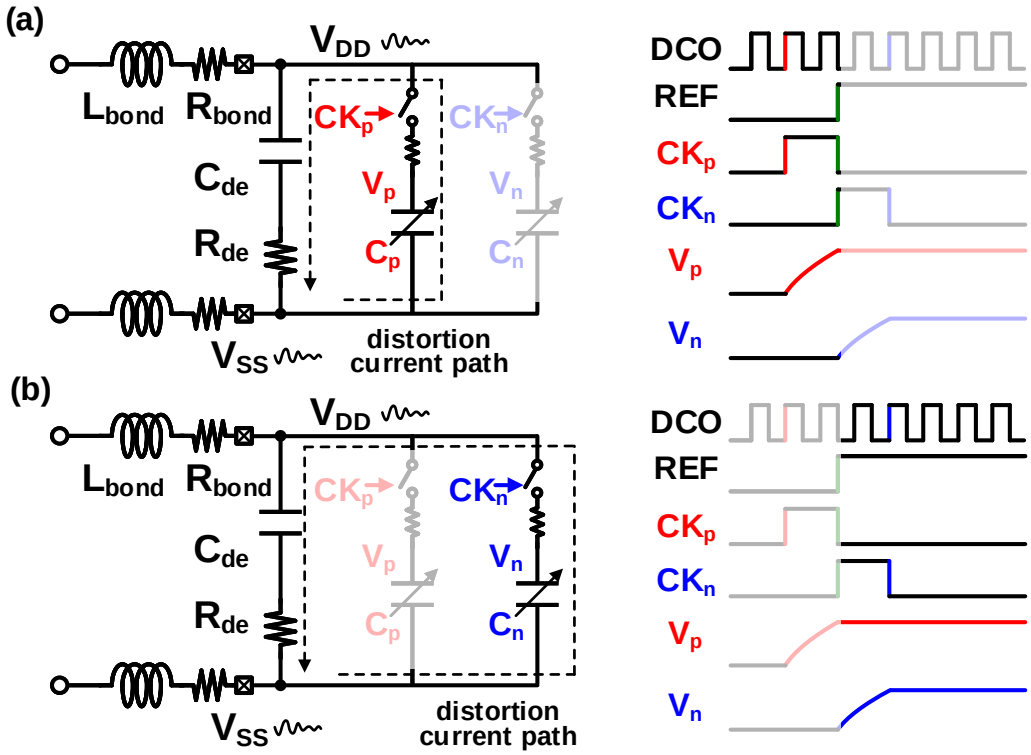


Figure 5.19: INL reduction effect in the VDQNC technique.

ifying the INL robustness. It can be seen in Fig. 5.20 that the equivalent INL amplitude stays almost constant when L_{bond} increases from 10 pH to 1 nH.

5.2.3 DPLL Implementation with Voltage Domain DSM QN Cancellation

A DPLL with the VDQNC technique is implemented, which is shown in Fig. 5.21. An LMS-based calibrator is used for estimating the digital-to-voltage gain of the VDQNC blcok. The MMD output is retimed with the DCO clock multiple times to generate the other internal clock signals for the VDQNC and the comparator to operate. A strong-arm latch is utilized for the comparator.

Event-driven simulations based on Verilog are used to check the phase noise and fractional spur performance of the proposed DPLL. The simulated PLL spectrum is shown in Fig. 5.22. It can be seen that a fractional spur reduction of 12 dB can be achieved thanks to the elimination of DTC comparator delay nonlinearity. Moreover, the integrated jitter from 10 kHz to 10 MHz bandwidth is improved from 160 fs to 95 fs.

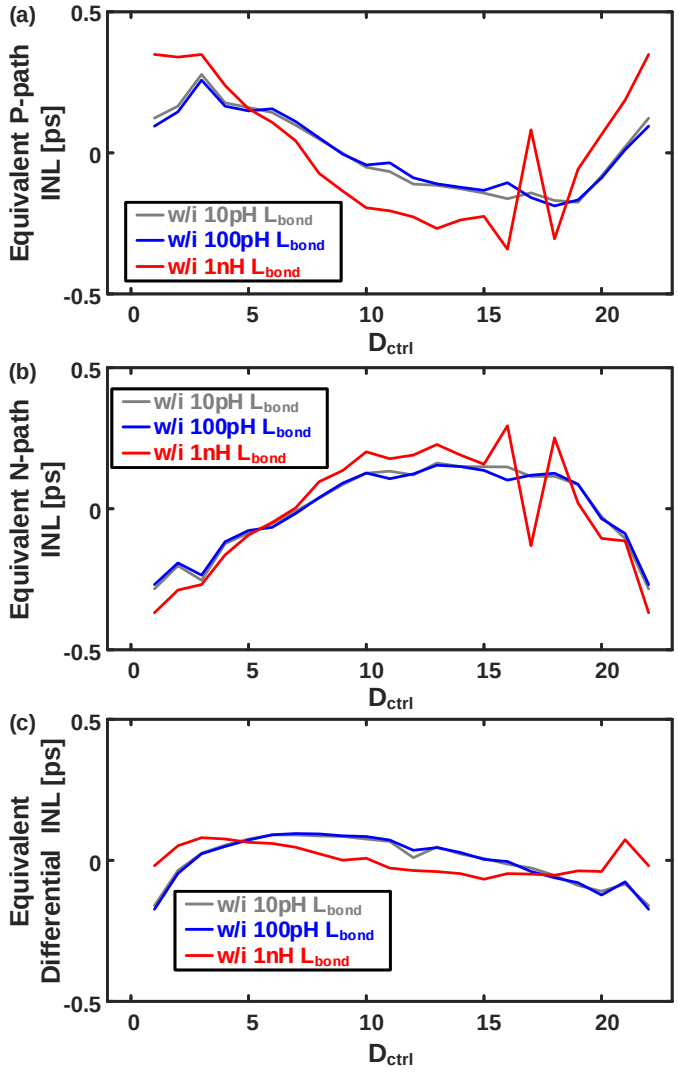


Figure 5.20: Avoidance of self-interference supply distortions in the VDQNC technique.

5.3 Summary

In this chapter, an LC oscillator with robust implicit CM resonance and a voltage domain DSM QN cancellation technique are proposed.

The LC oscillator can achieve a low flicker noise corner from 70 kHz to 230 kHz, and thus can benefit the design of a narrow-band PLL. Although the frequency of the proposed LC oscillator is from 4.24 GHz to 4.8 GHz, it can be readily modified such that the frequency can fit in the 6.5-to-8 GHz range. In combination with the DPD/dither-free DPLL, a stronger fractional spur suppression can be achieved by a narrower loop bandwidth without degrading the noise contribution from the DCO. Remarkably, the effect

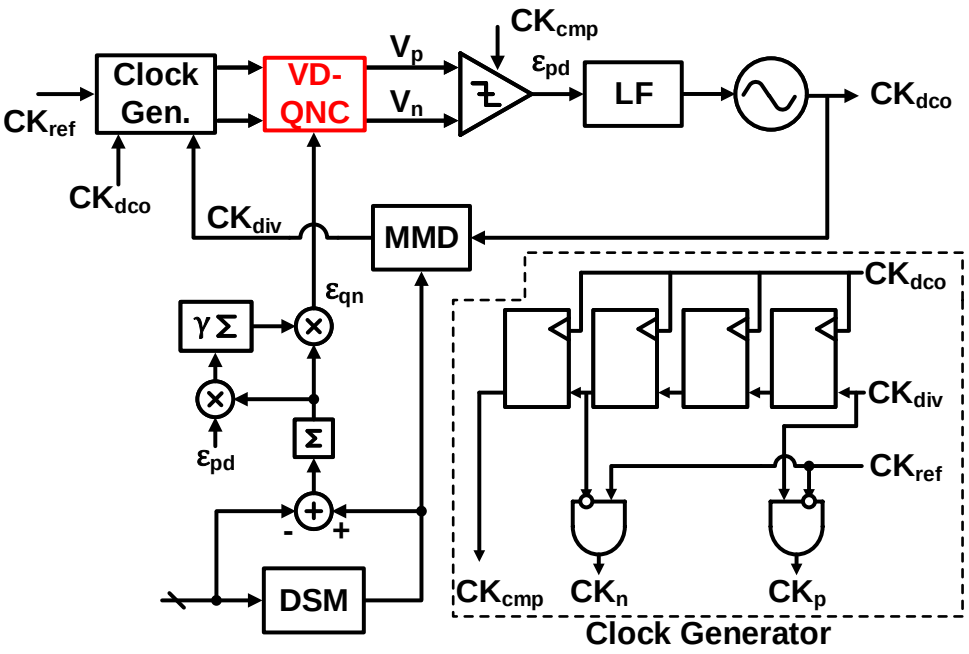


Figure 5.21: Topology of the VDQNC-based DPLL.

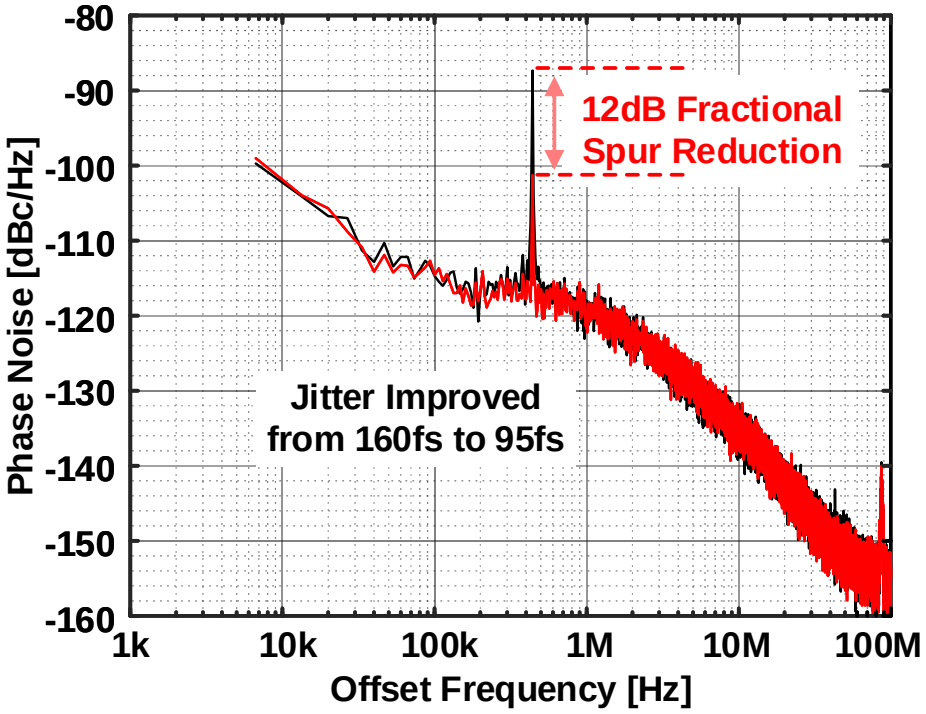


Figure 5.22: Simulated PN spectrum of the DPLL based on VDQNC.

of flicker noise suppression in the proposed LC oscillator shows less dependency on the decoupling network Q factor. Unlike the other conventional LC oscillators based on CM resonance at $2f_{vco}$, a low flicker noise corner can be expected in the proposed LC oscillator even with poorly designed decoupling network, which can potentially reduce the chip area wasted by on-chip decoupling capacitors.

The voltage domain DSM QN cancellation scheme eliminates the comparator in conventional DTC designs. Thanks to this feature, the noise penalty and supply sensitivity that are resulted by the DTC comparator can also be eliminated. Moreover, an inherently better INL can be achieved by the proposed voltage domain DSM QN cancellation technique. A 12 dB fractional spur reduction can be expected in the DPLL that is implemented with the proposed voltage domain DSM QN cancellation, which brings an integrated jitter improvement from 160 fs to 95 fs. Moreover, the differential output phases of the DCO can be exploitted (with calibration on the phase mismatch) to implement the cascaded fractional divider technique introduced in Chapter 4 for achieving a lower fractional spur level.

Chapter 6

Conclusion and Future Work

6.1 Conclusion

This thesis is devoted to present novel design techniques that can enable a low-fractional-spur and low-phase-noise DPLL for future wireless communication and FMCW radar systems.

As explained in chapter 1, the fractional spur suppression is a key factor in the future improvement of the wireless communication system data rate, as well as the improvement in the FMCW radar system accuracy. On the other hand, for the ease of integration with more and more powerful digital BB, DPLLs are preferred over the analog counterpart. However, the TDC utilized in DPLLs can introduce problems such as quantization error and mismatch-dependent nonlinearities. In order to improve the overall phase noise and spur performance, DTC-based DPLLs are attracting a lot of research interests. The bottleneck to further suppress the fractional spurs in DTC-based DPLLs is the nonlinearity from the DTCs.

Conventional techniques to mitigate the fractional spur and phase noise degradation from the DTC nonlinearities are reviewed in chapter 2. Those techniques can be roughly classified as the following three different types: 1) linear DTC topologies such as CS-DTC and ICS-DTCs; 2) DPD techniques that utilize LUTs to learn and compensate the shape of DTC INLs; 3) dithering techniques that randomize the periodical INL error such that the fractional spur power can be scrambled into wider frequency ranges. Nonetheless, different limitations exist for each of these techniques. Conventional linear DTC topologies need a precharging phase for proper operation, which limits their applications with high reference frequencies. DPD-based technique need considerable long calibration time for the LUTs to update. Dithering technique suppresses the fractional spur power at the cost of elevated random noise. Those limitations are driving the need of different PLL

and block circuit techniques for further fractional spur and phase noise suppression.

One different way to suppress the fractional spur is introduced in chapter 3, where a cascaded dual-fractional-*N* DPLL is proposed to combine different FCWs such that the fractional spurs can be pushed to high frequencies even in near-integer channels. Thanks to the high offset frequencies, the fractional spurs can be easily filtered by the second stage PLL. Careful FCW allocation can be applied to achieve the optimal fractional spur performance, which results in an as low as -63.7 dBc fractional spur.

Following the same idea, a DPD/dither-free DPLL is introduced in chapter 4. Compared to the cascaded dual-fractional-*N* DPLL, the DPD/dither-free DPLL can push the fractional spur to high frequencies without the need of an extra PLL, which can mitigate the degraded FoM in the cascaded dual-fractional-*N* DPLL. This is achieved with the newly proposed cascaded fractional divider technique, in which an extra DSM and DTC pair is utilized to achieve the FCW combination. Moreoever, a PD-DTC with self-cancelled even-symmetric nonlinearities is also introduced. The PD-DTC can achieve an INL reduction of around 4-fold without any noise penalty. Thanks to the two techniques introduced in chapter 4, the DPLL exhibits an FoM_{ref} of -237.4 dB, which is the best one at that time when compared to DPLLs with less than 60 dBc fractional spurs. Moreover, the DPLL shows a worst-case integrated jitter of 143.7 fs, which corresponds to a -47 dBc IPN. The target IPN performance of this thesis is thus achieved.

When being integrated with advanced process nodes such as FinFET CMOS process, more challenges will show up which might potentially limit the fractional spur and phase noise of DPLLs. The challenges mainly comes from two sides: 1) increasingly tight chip area specifiaction for limiting the fabrication cost; and 2) increasingly strong supply ripples which is caused by compact integration with other noisy block circuits. In order to ensure good phase noise and fractional spur performance even when the proposed DPLLs are migrated to the advanced process nodes, two circuit techniques are presented in chapter 5. The first one is an LC oscillator which can achieve robust implicit CM resonance even when the decoupling network Q factor is degraded due to limited on-chip area to implement sufficient decoupling capacitors. Featuring a flicker noise corner from 70 kHz to 230 kHz, a narrow bandwidth DPLL can be enabled by the proposed LC oscillator, which in turn will benefit in further fractional spur suppression. A voltage domain DSM QN cancellation technique is also proposed in chapter 5. By eliminating the comparator, which is necesssary in conventional DTC designs, the INL and phase noise performance of the DSM QN cancellation block can be improved. According to the simulation result, this technique can cause a 12 dB fractional spur suppression and a jitter improvement from 160 fs to 95 fs. Moreover, because of the differential operation of the proposed voltage domain DSM QN cancellation scheme, the INL degradation caused by supply ripples

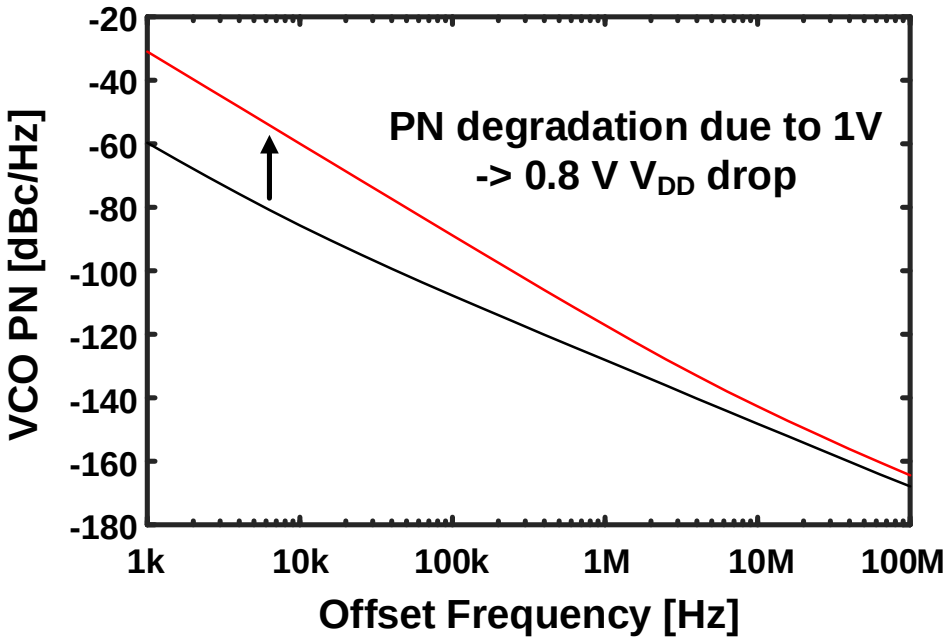


Figure 6.1: VCO PN degradation due to dropped supply voltage.

can also be expected to be suppressed.

Overall, the proposed techniques can be combined together such that a low-fractional-spur and low-phase-noise DPLL can be readily implemented in advanced process nodes where the chip area and supply ripples can affect the PLL performance negatively.

6.2 Future Works

6.2.1 Challenges on Advanced Process Nodes

As mentioned above, because of the need of stronger digital BB performance, advanced process nodes are highly desirable for moder SoC design. As a result, PLLs are required to be migrated to advanced nodes together with the digital BB. Unfortunately, the analog performance, especially the noise performance of transistor becomes worse as the transistor size becomes smaller. This poses a big challenge for both analog and digital PLL designers. For example, the flicker noise can easily degrade the output phase noise of a DTC.

Another challenge when migrating to the advanced node is the limited voltage headroom. Because of the thin oxide thickness which is necesssary for achieving smaller transistor size, the maximum supply voltage is usually lower in advanced process nodes.

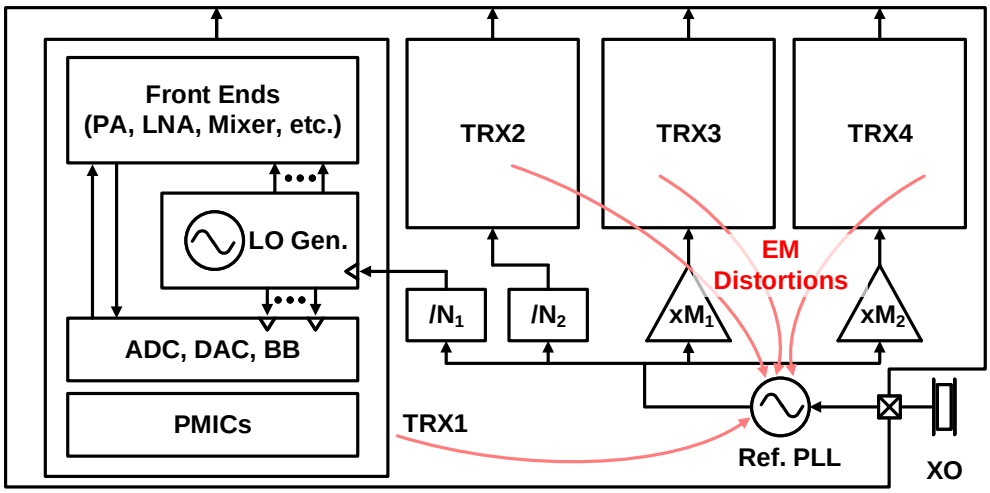


Figure 6.2: Clock synthesis for covering wider frequency bands.

On the other hand, the phase noise of the VCO is directly related to the oscillation amplitude, a lower supply voltage will cause severe noise penalty on the VCO side. The phase noise degradation caused by reduced supply voltage is shown in Fig. 6.1. It can be seen that for a conventional Class-B VCO, a PN degradation of 5 dB can happen in the thermal noise region when the supply voltage is dropped from 1 V to 0.8 V.

For the above reasons, new VCO topology and new DTC topology must be developed to avoid the noise penalty caused by the process scalling.

6.2.2 Higher Level of Integration

Modern cellular networks utilize multiple frequency bands from sub-GHz to mmW for maximizing the data rate, as shown in Fig. 6.2. Conventionally, different PLLs are designed for different frequency bands, taking the reference from another PLL that is driven by the XO.

Because all of the TRXs are driving power from the same power source (usually a battery), considerablly strong ripples will appear on the supplies of different block circuits. The nonlinear behavior in the block circuits will cause mixing and aliasing of the supply distortions, limiting the EVM of the TRX chain. Moreover, the inductors implemented for circuits such as PAs and LNAs will cause unwanted EM distortions. With the integration level becoming increasingly higher in modern SoCs, the noise penalty from the supply distortion and EM distortions can be increasingly strong.

On the other hand, the reference PLL usually employs an LC oscillator for achieving lower phase noise. The inductor from the LC oscillator is sensitive to the on-chip EM

distortions. As a result, when the EM distortions are coupled to the PLL by the VCO/DCO inductor, those distortions can cause noise fold-back and unwanted spurious tiones in the PLL output.

In order to mitigate the increasingly strong power and EM distortion, different PLL topologies are required. In particular, more digital circuits techniques can be exploitted such that the advantage of process scalling can be fully utilized.

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Appendix A

Publication List

A.1 Journal Papers

- **Dingxin Xu** *et al.*, "A VCO With Robust Implicit Common-Mode Resonance Against Nonideal Decoupling Network," in IEEE Solid-State Circuits Letters, vol. 7, pp. 171-174, 2024, doi: 10.1109/LSSC.2024.3399228.
- **Dingxin Xu** *et al.*, "A 6.5-to-8-GHz Cascaded Dual-Fractional-N Digital PLL Achieving -52.79-dBc Fractional Spur with 50-MHz Reference," in IEEE Journal of Solid-State Circuits, doi: 10.1109/JSSC.2024.3447021.
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A.2 International Conferences and Worshops

- **Dingxin Xu** *et al.*, "10.3 A 7GHz Digital PLL with Cascaded Fractional Divider and Pseudo-Differential DTC Achieving -62.1dBc Fractional Spur and 143.7fs Integrated Jitter," 2024 IEEE International Solid-State Circuits Conference (ISSCC), San Francisco, CA, USA, 2024, pp. 192-194, doi: 10.1109/ISSCC49657.2024.10454284.
- **Dingxin Xu** *et al.*, "A 6.5-to-8GHz Cascaded Dual-Fractional-N Digital PLL Achieving -63.7dBc Fractional Spurs with 50MHz Reference," 2023 IEEE Custom Integrated Circuits Conference (CICC), San Antonio, TX, USA, 2023, pp. 1-2, doi: 10.1109/CICC57935.2023.10121180.
- **Dingxin Xu** *et al.*, IEEE International Solid-State Circuits Conference (ISSCC) Student Research Preview, Feb. 2023.

A.3 Domestic Conferences and Workshops

- **Dingxin Xu**, Zheng Sun, Hongye Huang, 染谷 晃基, 白根 篤史, 岡田 健一, "A Time-Amplifier Gain Calibration Technique for ADPLL", 電子情報通信学会 ソサイエティ大会 (於 大阪大学), C-12-19, Sep. 2019.

A.4 Co-Authored Journals and Conferences

A.4.1 Journal Papers

- Huáng, Hóngyè, Bangan Liu, Zezheng Liu, **Dingxin Xu**, Yuncheng Zhang, Waleed Madany, Junjun Qiu *et al.* "A Fully Synthesizable Fractional-N MDLL With Energy-Efficient Ring-Oscillator-Based DTC of Large Tuning Range," in IEEE Solid-State Circuits Letters, vol. 7, pp. 54-57, 2024, doi: 10.1109/LSSC.2024.3352736.

- Zhang, Yuncheng, Zheng Sun, Bangan Liu, Junjun Qiu, **Dingxin Xu**, Yi Zhang, Xi Fu *et al.*, "A Time-Mode-Modulation Digital Quadrature Power Amplifier Based on 1-bit Delta–Sigma Modulator and Hybrid FIR Filter," in IEEE Journal of Solid-State Circuits, vol. 59, no. 4, pp. 993-1005, April 2024, doi: 10.1109/JSSC.2023.3349002.

- Qiu, Junjun, Zheng Sun, Bangan Liu, Wenqian Wang, **Dingxin Xu**, Hans Herdian, Hongye Huang *et al.*, "A 32-kHz-Reference 2.4-GHz Fractional-N Oversampling PLL With 200-kHz Loop Bandwidth," in IEEE Journal of Solid-State Circuits, vol. 56, no. 12, pp. 3741-3755, Dec. 2021, doi: 10.1109/JSSC.2021.3106514.

- Sun, Zheng, Hanli Liu, **Dingxin Xu**, Hongye Huang, Bangan Liu, Zheng Li, Jian Pang, Teruki Someya, Atsushi Shirane, and Kenichi Okada. "A Low-Jitter Injection-Locked Clock Multiplier Using 97-μW Transformer-Based VCO with 18-kHz Flicker Noise Corner." IEICE Transactions on Electronics 104, no. 7 (2021): 289-299.

- Zheng Sun, **Dingxin Xu**, Hongye Huang, Zheng Li, Hanli Liu, Bangan Liu, Jian Pang, Teruki Someya, Atsushi Shirane, and Kenichi Okada, "A Compact TF-based LC-VCO with Ultra-Low-Power Operation and Supply Pushing Reduction for IoT Applications," IEICE Transactions (accepted).

- Sun, Zheng, Hanli Liu, Hongye Huang, Dexian Tang, **Dingxin Xu**, Tohru Kaneko, Zheng Li *et al.*, "A 0.85mm2 BLE Transceiver Using an On-Chip Harmonic-Suppressed RFIO Circuitry With T/R Switch," in IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 68, no. 1, pp. 196-209, Jan. 2021, doi: 10.1109/TCSI.2020.3033540.

- Bangan Liu, Yuncheng Zhang, Junjun Qiu, Hongye Huang, Zheng Sun, **Dingxin Xu**, Haosheng Zhang, Yun Wang, Jian Pang, Zheng Li, Xi Fu, Atsushi Shirane, Hitoshi Kurosu, Yoshinori Nakane, Shunichiro Masaki, and Kenichi Okada, "A Fully-Synthesizable Fractional-N Injection-Locked PLL for Digital Clocking with Triangle/Sawtooth Spread-Spectrum Modulation Capability in 5-nm CMOS," in IEEE Solid-State Circuits Letters, vol. 3, pp. 34-37, 2020.

A.4.2 Conferences and Worshops

- Zhang, Yuncheng, Zheng Sun, Bangan Liu, Junjun Qiu, **Dingxin Xu**, Yi Zhang, Xi Fu *et al.*, "A Time-Mode-Modulation Digital Quadrature Power Amplifier Based on 1-bit Delta-Sigma Modulator and Transformer Combined FIR FIlter," 2023 IEEE Symposium on VLSI Technology and Circuits (VLSI Technology and Circuits), Kyoto, Japan, 2023, pp. 1-2, doi: 10.23919/VLSITechnologyandCir57934.2023.10185368.

- Qiu, Junjun, Wenqian Wang, Zheng Sun, Bangan Liu, Yuncheng Zhang, **Dingxin Xu**, Hongye Huang *et al.*, "A 32kHz-Reference 2.4GHz Fractional-N Nonuniform Oversampling PLL with Gain-Boosted PD and Loop-Gain Calibration," 2023 IEEE International Solid-State Circuits Conference (ISSCC), San Francisco, CA, USA, 2023, pp. 80-82, doi: 10.1109/ISSCC42615.2023.10067516.

- Sun, Zheng, **Dingxin Xu**, Junjun Qiu, Zezheng Liu, Yuncheng Zhang, Hongye Huang, Hanli Liu *et al.*, "A 0.25 mm2 BLE Transmitter with Direct Antenna Interface and 19% System Efficiency Using Duty-Cycled Edge-Timing Calibration," ESSCIRC 2021 - IEEE 47th European Solid State Circuits Conference (ESSCIRC), Grenoble, France, 2021, pp. 499-502, doi: 10.1109/ESSCIRC53450.2021.9567781.

- Zheng Sun, Hanli Liu, **Dingxin Xu**, Hongye Huang, Bangan Liu, Zheng Li, Jian Pang, Teruki Someya, Atsushi Shirane, and Kenichi Okada "A 78fs RMS Jitter Injection-Locked Clock Multiplier Using Transformer-Based Ultra-Low-Power VCO," IEEE European Solid-State Circuits Conference (ESSCIRC), Cracow, Poland, Sep. 2019.

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