

論文 / 著書情報
Article / Book Information

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Title(English)	A Study of Fractional Spur Suppression Techniques in Digital Phase-Locked Loops
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種別(和文)	論文要旨
Type(English)	Summary

(博士課程)
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論文要旨

THESIS SUMMARY

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要旨 (英文 800 語程度)

Thesis Summary (approx.800 English Words)

This paper titled "A Study of Fractional Spur Suppression Techniques in Digital Phase-Locked Loops" consists of six chapters in English.

In Chapter 1, "Introduction", the application of fractional DPLLs in modern wireless communication and radar systems are introduced. The importance of suppressing fractional spurs and phase noise in fractional DPLLs are also detailed.

In Chapter 2, "DTC-Based DPLLs and Fractional Spur Suppression Techniques", conventional DTC-based DSM QN cancellation technique is introduced, which is a key technique in mitigating fractional spurs. Other fractional spur suppression techniques such as linear DTC topologies, DPD-based techniques, and dither-based techniques are also introduced. The advantages and disadvantages of the above-mentioned techniques are discussed, which necessitates the development of new fractional spur suppression techniques.

Chapter 3, "A Cascaded Dual-Fractional-N DPLL for Fractional Spur Suppression", proposes a cascaded PLL topology where two stages are both working in fractional mode. Fractional spur degradation at near-integer channels can be avoided in the proposed cascaded PLL by carefully selecting the two FCWs such that the fundamental fractional spur frequencies can be pushed to higher frequency offsets and be filtered out by the low-pass loop characteristics. A segmented DTC with DPD with 0.05% full scale peak-to-peak INL and a low-phase-noise LCDCO are implemented for further fractional spur and phase noise improvement. The proposed cascaded PLL is implemented in 65nm CMOS and achieves a 190.8fs integrated jitter with -52.79dBc worst-case fractional spur, which is mainly limited by the inter-stage coupling. The mechanism of the inter-stage coupling is also discussed in this chapter, indicating a potentially better fractional spur performance can be achieved by improve the isolation between the LCDCO and the segmented DTC.

Chapter 4, "A DPD/Dither-Free DPLL", proposes a single-loop DPLL topology that can push the fractional spurs to out-of-band by a cascaded fractional divider technique. Compared to the cascaded PLL proposed in Chapter 3, an auxiliary DSM-DTC pair instead of an extra PLL is adopted to avoid the fractional spur degradation at near-integer channels, which leads to an inherently better jitter-to-noise trade-off. Moreover, a pseudo-differential DTC technique is proposed to cancel the strong even-symmetrical INLs in conventional variable-slope DTCs. The proposed DTC can achieve around 4-fold INL improvement compared to the conventional variable-slope DTC. Thanks to the two proposed techniques, the DPD/dither-free DPLL can achieve -62.1dBc fractional spur, 143.7fs integrated jitter, and an FoMref of -237.4dB.

In Chapter 5, "Block Circuits Design Techniques for Low-Fractional-Spur DPLLs", one novel LC oscillator and one voltage-domain DSM QN cancellation scheme are proposed to further enhance the fractional spur and phase noise performance. The proposed LC oscillator can achieve an implicit common-mode high impedance at twice the resonance frequency that is independent on the Q factor of decoupling network. Compared to the conventional implicit common-mode resonance VCO, the proposed VCO can maintain a low flicker noise when the decoupling capacitor area is limited. When being applied to the PLLs presented in Chapter 3 and 4, the loop bandwidth is enabled to be narrower for a stronger suppression on the fractional spur without degrading the overall integrated jitter. On the other hand, conventional DTC-based QN cancellation technique is prone to supply ripples and the noise/INL degradation caused by the comparator stage. In order to mitigate these issues, a voltage-domain QN cancellation technique is proposed. Because of the voltage-domain phase error detection in the proposed technique, no slope-dependent nonlinearity is generated during QN cancellation. The high differential slew rate at the comparator input can further suppress the comparator phase noise. Most importantly, unlike in the pseudo-differential DTC, there is no overlap between the charging windows of the comparators two inputs. This novel operation can further benefit in the reduction of

self-interference supply ripples, leading to less INL degradation when the PLL is working under nonideal supplies. The two proposed techniques in this chapter can be readily applied to the PLLs introduced in Chapter 3 and 4.

In Chapter 6, “Conclusion and Future Work”, the achievements of this paper are summarized. Future research directions for further improving the PLL spur and noise performance in advanced process nodes and compact SoCs are also discussed.

備考：論文要旨は、和文 2000 字と英文 300 語を 1 部ずつ提出するか、もしくは英文 800 語を 1 部提出してください。

Note : Thesis Summary should be submitted in either a copy of 2000 Japanese Characters and 300 Words (English) or 1copy of 800 Words (English).

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