論文 / 著書情報
Article / Book Information

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論 文 要 旨

THESIS SUMMARY

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要旨（英文 800 語程度）
Thesis Summary（approx.800 English Words ）

Routing has a significant impact on chip design and requires dedicated effort in each design style and situation. With recent technological advances, some types of advanced chips need to realize high connectivity demand in one direction, assumed horizontal direction in the dissertation, by utilizing limited routing resources. There are obstacles scattered throughout the chip, and the routing areas span horizontally between obstacles. It is preferred to complete routing nets by a single-trunk Steiner tree. Routing nets with various inherent widths by given limited areas needs the efficient use of areas.

An objective of the routing problem is to accomplish the routing to minimize routing resources used: especially, routing areas and wirelength. Efficient use of the available routing areas helps in reducing the overall size of the chip, which can lead to cost savings and improved yield in manufacturing. Shorter wirelength reduces signal delay and power consumption, and the wirelength reduction is crucial for improving the performance and efficiency of the chip. Therefore, while considering routing design constraints, the minimization of routing areas and wirelength plays a key role in the advanced chip design.

Routing algorithms to minimize routing resources have been investigated over several decades. However, existing algorithms cannot achieve efficient routing solutions in the scenario because they do not assume separated routing areas. Also, their solutions are complicated by dog-leg routing. To realize a high-performance chip design, research and development of algorithms to obtain efficient solutions for the scenario are necessary.

The dissertation proposes greedy heuristic algorithms to minimize routing areas and wirelength for the routing problem. Their proposed algorithms allocate trunks of nets to gaps on a gap-by-gap basis. The net priority, or allocation order of trunks of nets, affects the total routing areas used as well as the total wirelength. Since there is a trade-off between them, the dissertation develops an algorithm to use as small routing areas as possible first, followed by developing algorithms to minimize wirelength while maintaining the routing areas used.

First, the dissertation models the routing problem as gap channel routing (GCR) to standardize and clarify the problem. In GCR, various-width trunks of nets are allocated to separated routing areas, called gaps. The routing areas used correspond to the number of gaps used. The wirelength of a net depends on the y-coordinate at which the trunk is allocated. An optimal allocation of trunks often contains conflicts, and it is impossible to allocate all trunks to their optimal gaps in general since each gap has a limited capacity. Thus, to obtain efficient solutions, it is necessary to allocate the trunks while considering other trunks so that as many trunks as possible are routed to the optimal gap.

Second, the dissertation proposes a ceiling and packing algorithm (CAP) to minimize the number of gaps used. CAP allocates the trunk of a net repeatedly so that each gap is filled as much as possible by adopting an appropriate allocation order. CAP prioritizes wider trunks in allocation as first-fit-decreasing adopts in Bin-Packing while the allocation order changes flexibly based on allocated and unallocated trunks. The experimental results show that CAP achieves the least number of gaps used compared to conventional channel routing algorithms, Left-Edge and NLEA.

Finally, the dissertation proposes two algorithms: criticality-based ceiling and packing algorithm (CCAP) and Gap Swap-Flip (GSF) to minimize the wirelength with as small a number of gaps used as possible.

CCAP is a greedy heuristic algorithm that is conscious of congested gaps and determines the order of gaps and nets so that as many trunks as possible are allocated with the smaller wirelength as much as possible. CCAP is based on CAP and integrated congestion-aware gap order (CGO) and criticality-based net priority. CGO determines the order of the gaps to be routed so that as many nets as possible can be routed in small wirelength. Criticality-based net priority is a priority to routing a net whose wirelength will be smaller if it is routed to the current processing gap than to the remaining gaps. Incorporating them with CAP reduces the wirelength significantly while minimizing the increase in the number of gaps used. The evaluation results show that CCAP significantly reduced the wirelength by using almost the same number of gaps as CAP.

GSF is a post-processing algorithm, where given an initial allocation, GSF first reduces the wirelength outside gaps by swapping the allocation between two gaps and then reduces the wirelength inside a gap by reversing the allocation within the gap. It is possible to shorten the wirelength as much as possible without changing the number of gaps used.

Through the dissertation, the proposals obtain an efficient routing solution of GCR that is necessary to realize a high-performance chip design, and thus the dissertation contributes to these advanced chip designs.

備考 ： 論文要旨は、和文 2000 字と英文 300 語を 1 部ずつ提出するか、もしくは英文 800 語を 1 部提出してください。
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