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Scalable Millimeter-Wave MIMO Phased-Array Receiver Design with Area and Power Efficiency

by

Yi Zhang

A Ph. D. dissertation submitted in partial fullfillment of the requirements for the degree of

Doctor of Philosophy

in

Department of Electrical and Electronic Engineering

in the

School of Engineering

of

Institute of Science Tokyo

Supervised by

Prof. Kenichi Okada

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To my family,

Acknowledgment

Although more than six years have passed since I joined Okada Lab as a master's student, it feels as though the day I arrived in Tokyo in 2018 was not so long ago. The journey has been challenging, yet I feel fortunate to have had the opportunity to complete this period of study and research as a Ph.D. student at the Institute of Science, Tokyo.

This thesis owes its completion to the generous help and unwavering support of my fellow lab members, friends, my girlfriend, and my family. I would like to take this opportunity to express my heartfelt gratitude to all of them.

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Abstract

This dissertation presents the design and implementation of millimeter-wave (mmWave) phased-array receivers that are scalable to support additional frequency bands and MIMO streams while maintaining area and power efficiency, tailored for next-generation multiple-input multiple-output (MIMO) communication systems. The research addresses critical challenges such as power consumption, chip area constraints, and performance optimization by proposing novel architectural solutions and circuit techniques.

The dissertation begins by analyzing the requirements of mmWave phased-array receivers for next-generation communication systems and addresses these challenges by introducing two innovative receiver architectures: (1) a power-efficient multi-band phased-array receiver employing a harmonic-selection technique, and (2) an area-efficient time-division MIMO (TD-MIMO) phased-array receiver. The multi-band receiver leverages harmonic-selection filtering to achieve robust inter-band blocker rejection and seamless operation across multiple frequency bands, maximizing spectral utilization while minimizing power consumption. Meanwhile, the TD-MIMO phased-array receiver incorporates a hardware-sharing time-division multiplexing scheme, enabling high data throughput with minimal chip area expansion, ensuring scalability for future applications.

The proposed architectures are validated through experimental prototypes, demonstrating significant performance improvements. Furthermore, this dissertation explores the integration of the proposed techniques and presents a universal solution for next-generation mmWave receivers.

By offering scalable and efficient design methodologies, this work contributes to the advancement of future mmWave communication systems, laying the foundation for cost-effective, high-capacity receiver architectures that can adapt to evolving wireless communication demands.

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Chapter 1

Introduction

The discovery and study of electromagnetic waves have fundamentally transformed human communication. Wireless communication has become indispensable in daily life, advancing rapidly over the past few decades. Initially, it was primarily used for one-way radio broadcasting. The advent of multi-user mobile networks began with 1G in the 1980s, offering basic analog voice calls at speeds of 2.4 kbps. As shown in Fig. 1.1, subsequent generations of mobile communication brought exponential improvements. The transition to 2G in the 1990s introduced digital communication, enabling clearer voice calls and text messaging at data rates of up to 64 kbps.

The latest 5G technology marks a significant leap forward, delivering speeds up to

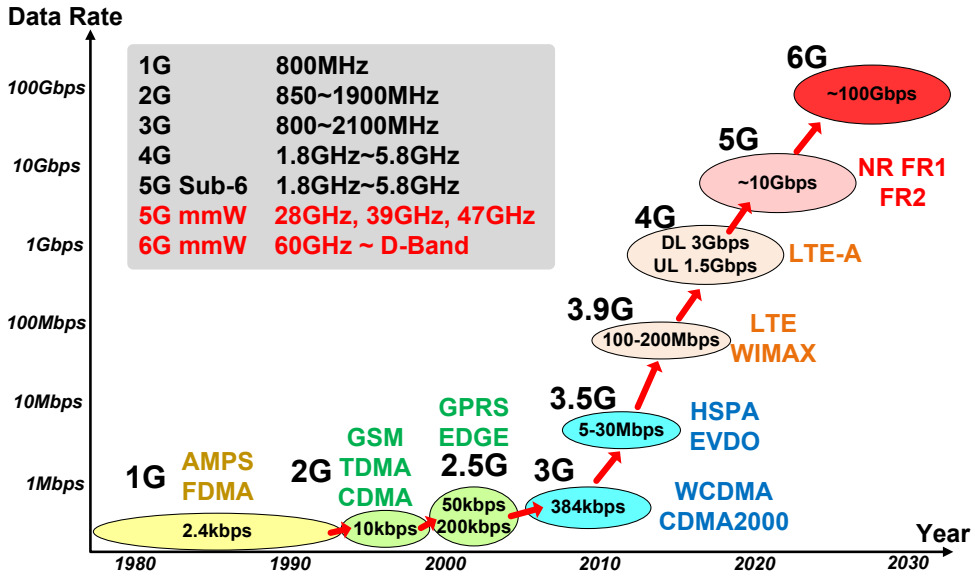


Figure 1.1: Typical wireless communication system.

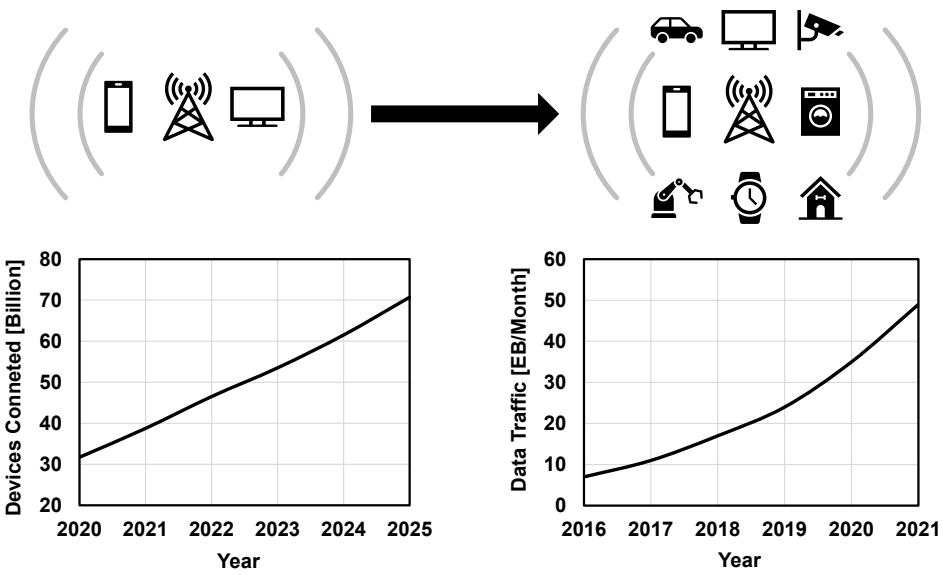


Figure 1.2: The exponential growth in data traffic volume

10 Gbps—nearly 100 times faster than 4G. It also reduces latency to just 1 millisecond compared to 30–50 milliseconds in 4G, making it ideal for real-time applications such as autonomous vehicles and virtual reality. Furthermore, 5G can connect millions of devices per square kilometer, fostering the rapid growth of the Internet of Things (IoT).

The evolution of communication systems continues steadily. By the late 20th century, wireless communication was mainly used for cell phone calls and TV/radio broadcasting. Advances in processor and wireless transceiver have since enabled wireless connectivity across a wide range of devices, including wearable gadgets, smart home appliances, and industrial equipment, as shown in Fig. 1.2. The number of connected devices is expected to exceed 70 billion by 2025, while global data traffic is projected to surpass 50 exabytes (EB) per month by 2021. This rapid growth is driven by the increasing demand for high-resolution video streaming, artificial intelligence (AI), and cloud services.

According to the Shannon-Hartley theorem (Eq. 1.1), the channel capacity C depends on the channel bandwidth BW and the signal-to-noise ratio (SNR) of the signal chain:

$$C = BW \log_2(1 + \frac{S}{N}) \tag{1.1}$$

However, both SNR and channel bandwidth are limited for most wireless applications. As data traffic increases, improving the wireless capacity of communication systems becomes essential. The microwave frequency spectrum (below 20 GHz) is already heavily

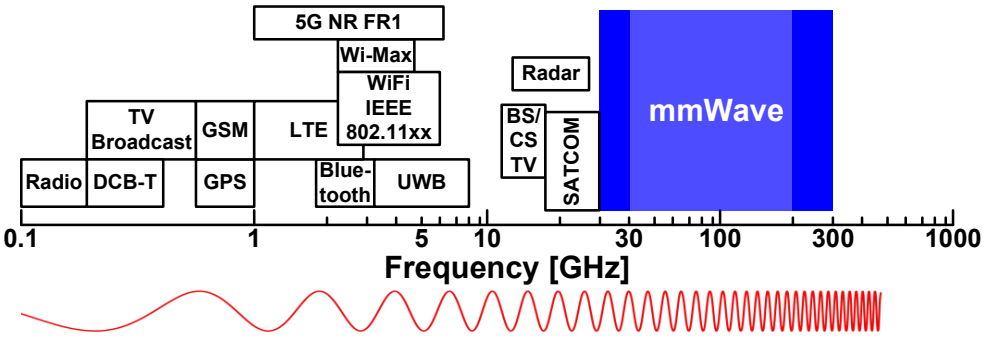


Figure 1.3: The spectrum resources allocation situation.

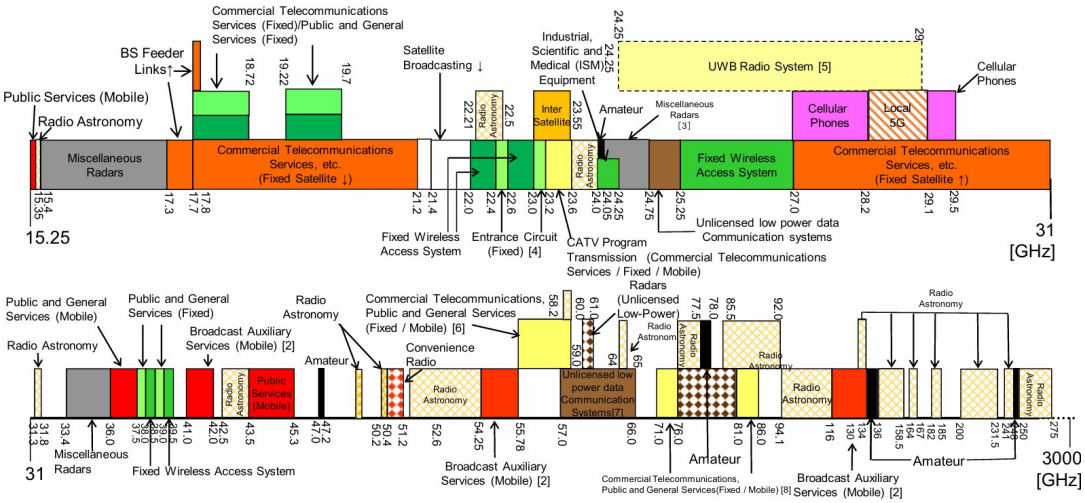


Figure 1.4: Current situation of millimeter-wave spectrum use in Japan.

utilized by existing standards, such as radio, TV broadcasting, GPS, WiFi, and LTE, as shown in Fig. 1.3. These lower frequency bands provide limited bandwidth and lack spatial multiplexing capabilities, which restrict achievable data rates and capacity. The crowded spectrum also creates challenges for maintaining high SNR performance. In contrast, the millimeter-wave (mmWave) band, spanning 20–300 GHz, offers abundant spectrum resources and allows for much larger bandwidth allocations. This expanded bandwidth is critical for supporting ultra-high-speed data rates and the demanding applications of next-generation communication systems. 5G NR FR2 and low-earth orbit (LEO) satellite communications have already adopted mmWave bands, with the spectrum for mmWave 5G shown in Fig. 1.4.

CMOS technology is well-suited for millimeter-wave (mmWave) applications, offer-

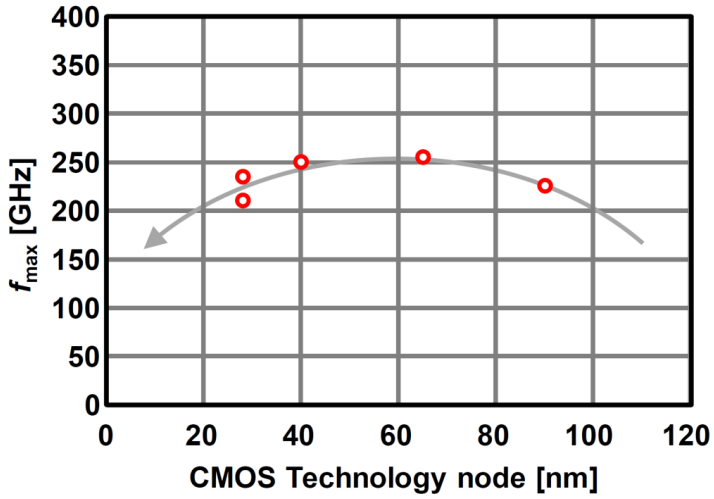


Figure 1.5: The maximum operating frequency of different CMOS technology node.

ing a practical and cost-effective solution. As shown in Fig. 1.5, the relationship between CMOS technology node size and maximum operating frequency $f_{\max}$ indicates that while smaller nodes typically support higher frequencies, the optimal $f_{\max}$ is achieved around the 40-65 nm range. The 65 nm CMOS node, in particular, combines low cost with high reliability and delivers $f_{\max}$ values above 200 GHz, making it more than sufficient for mmWave frequencies. This balance of performance and affordability makes it an ideal choice for developing high-performance mmWave systems without incurring excessive costs.

The shorter wavelength of mmWave frequencies enables spatial multiplexing, a key advantage over the microwave band. In the microwave range, omnidirectional antennas cause channel interference within the same area, limiting capacity utilization. To mitigate this, cellular base station layouts are used in microwave mobile communication networks, as shown in Fig. 1.6(a). In contrast, mmWave frequencies allow for chip-scale antenna arrays, enabling phased-array beamforming in compact devices, as illustrated in Fig. 1.6(b). This directional beamforming significantly expands wireless capacity by allowing more efficient radio resource allocation. Different channels can operate simultaneously without interference, and multiple targets can be communicated with simultaneously without requiring additional frequency bands.

As a solid information base for future super smart society, next-generation communication systems will inevitably expand into the mmWave band to achieve greatly enhanced wireless performance and further expands the boundaries of applications.

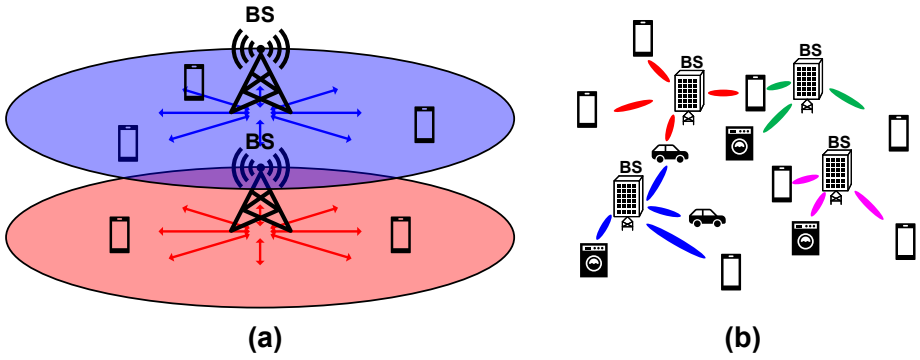


Figure 1.6: (a) Microwave cellular mobile communication network. (b) Millimeter-wave communication system utilizing spatial multiplexing.

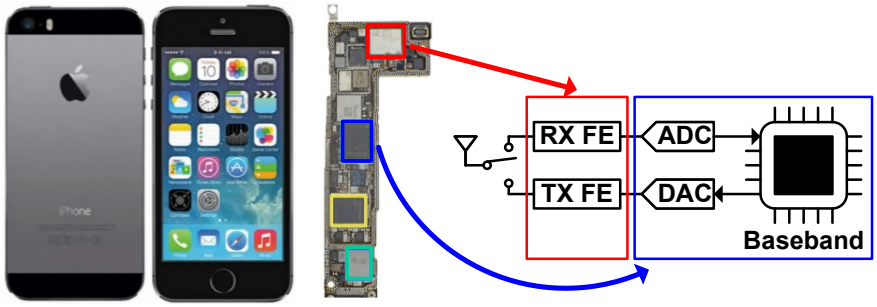


Figure 1.7: Typical wireless communication system in terminal devices.

1.1 Receivers in Wireless Communication Systems

Fig. 1.7 shows the components of a typical wireless communication system in terminal devices, where the digital data generated by the baseband from the transmitter (TX) side is first converted to analog signal by a digital-to-analog converter (DAC). This signal will then be up converted and power amplifier in the TX front-end (FE) before being transmitted into the air through the antenna module. On the receiver (RX) side, the electromagnetic wave captured by the antenna will be amplified, followed by the down-conversion to IF or baseband frequency and then be sampled by the analog-to-digital converter (ADC). In the end, the digitized data will be processed by the baseband to complete the communication. In modern portable devices, for example the iPhone 12 in the Fig. 1.7, the RX and TX front-end are separated designed with the digital baseband. While the performance requirement to the TX and RX are different due to their position in the signal chain, these

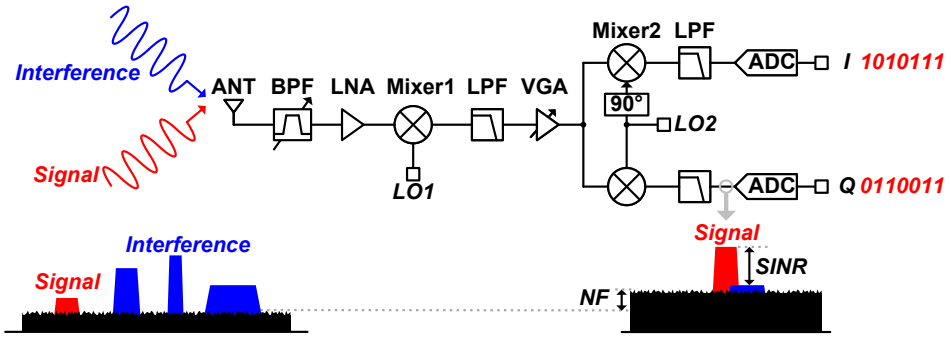


Figure 1.8: Detail block diagram of typical superheterodyne receiver.

thesis will focus on the design of receivers.

The block diagram of a typical receiver and its signal processing chain is shown in Fig. 1.8. The receiver starts with an antenna that captures not only the desired signal but also various environmental interferences. A band-pass filter (BPF) suppresses out-of-band interference, while a low-noise amplifier (LNA) amplifies the signal with minimal additional noise. In a superheterodyne architecture, the high-frequency RF signal is down-converted to an intermediate frequency (IF) by the first mixer (Mixer1) using a local oscillator (LO1). A variable gain amplifier (VGA) is then employed to optimize the dynamic range for signals of varying power levels. The IF signal is split and sent to a second mixer stage (Mixer2) for in-phase (I) and quadrature (Q) signal processing. A second local oscillator (LO2) ensures precise phase separation, and the resulting I/Q signals are digitized by ADCs. In contrast, a zero-IF architecture eliminates Mixer1, directly down-converting the RF signal to baseband using a high-frequency LO to avoid image signal issues.

The receiver's primary goal is to maintain a high signal-to-interference-plus-noise ratio (SINR) across a wide input power range. For weak signals, SINR is determined by the noise figure (NF), which quantifies the noise added by the receiver and impacts sensitivity. For strong signals and interference, SINR is limited by the linearity of amplifiers. In traditional single-element receivers, RF performance depends primarily on the element design itself. However, for multi-element phased-array receivers operating at millimeter-wave frequencies, overall performance mainly depends on system architecture and engineering considerations. Element design targets should align with system-level constraints to avoid overdesign and conserve resources.

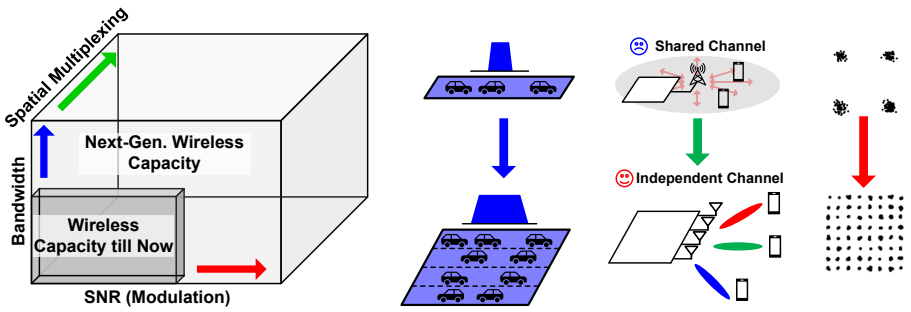


Figure 1.9: The exponential growth in data traffic volume.

1.2 The Demands for Next Generation Millimeter-Wave Receivers

To develop an optimized millimeter-wave receiver solution for next-generation communication systems, it is crucial to first identify the key demands. As shown in Fig. 1.9, the millimeter-wave spectrum enhances communication systems along three dimensions: (1) wider channel bandwidths that enable higher data rates; (2) reduced interference for improved signal-to-noise ratio (SNR), supporting higher-order modulation schemes and enhancing spectral efficiency; and (3) spatial multiplexing through beamforming, which increases spatial traffic capacity. To address these requirements, hardware solutions must incorporate innovative designs that support the performance and functionality required by next-generation systems.

As data traffic continues to grow, the total wireless capacity of next-generation communication systems must scale accordingly. This effort involves two critical aspects:

Enhancing Device-Level Data Rates: All terminal devices in the network must aim for higher data rates in next-generation communication systems. While this can theoretically be achieved by increasing channel bandwidth and SNR, as indicated by Eq. 1.1, practical limitations exist. Communication standards, such as 5G NR, impose constraints on modulation schemes and channel bandwidth. Over-engineering RF performance beyond these limits is often inefficient in terms of power and area. To overcome these challenges, multiple-input-multiple-output (MIMO) technology has become essential. By leveraging spatial multiplexing, MIMO bypasses bandwidth and SNR limitations to deliver higher data rates.

Efficient Wireless Resource Management: Even with increased theoretical channel capacity, efficient and intelligent wireless resource allocation is essential to fully realize

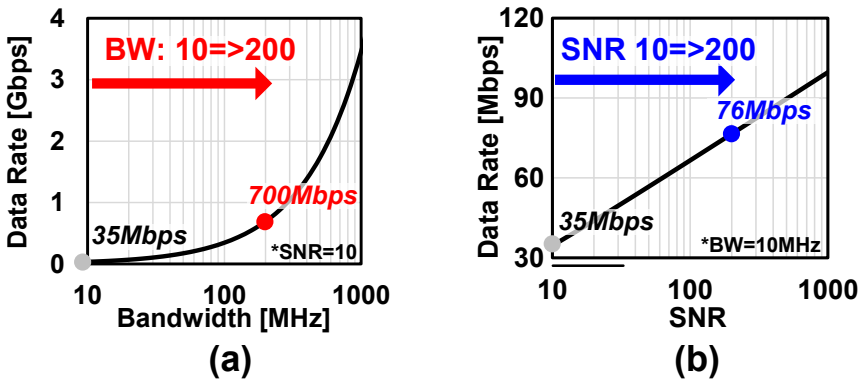


Figure 1.10: The exponential growth in data traffic volume.

the potential of next-generation systems. Advances in artificial intelligence (AI) enable the development of smart algorithms for resource management, which will play a critical role in future networks. However, millimeter-wave receivers must possess the necessary capabilities to support these advanced control mechanisms. Multi-band operation, in particular, provides exceptional flexibility for resource management, offering a robust solution to optimize system performance.

The following subsections provide a detailed discussion of these two aspects.

1.2.1 MIMO Towards Higher Data Rates

As shown in Fig. 1.10, data rates benefit more significantly from larger channel bandwidth than from higher SNR. This observation supports the adoption of the millimeter-wave band, which inherently provides abundant spectrum resources for wider bandwidths. While millimeter-wave frequencies experience greater free-space path loss, the resulting SNR degradation is less critical compared to the data rate advantage offered by the increased bandwidth. However, channel bandwidth is predefined by communication standards and cannot be expanded indefinitely due to competition among devices for spectrum allocation.

To overcome this limitation and achieve higher data rates, Multiple-Input Multiple-Output (MIMO) technology is essential. As illustrated in Fig. 1.11, traditional Single-Input Single-Output (SISO) systems are constrained to a single transmission channel. For example, in 5G NR FR2, the maximum modulation scheme (256-QAM) and channel bandwidth (400 MHz) limit the data throughput to 1.68 Gbps. In contrast, MIMO systems employ multiple transmit and receive antennas, enabling multiple spatial streams

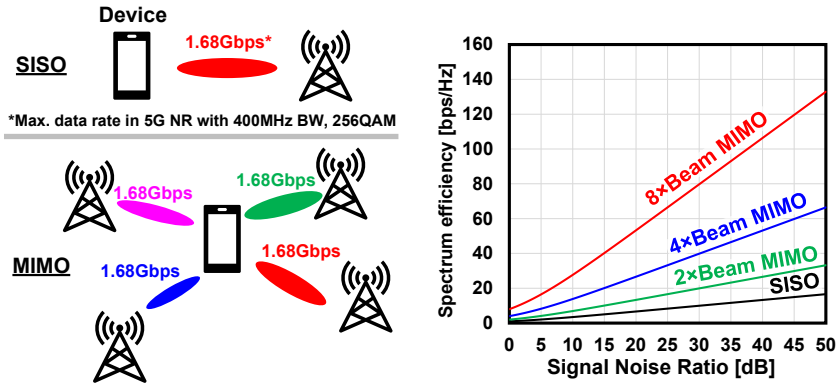


Figure 1.11: The exponential growth in data traffic volume.

to operate simultaneously and significantly increasing the total data rate. The equivalent channel capacity C of MIMO is given by:

$$C = NBW \log_2(1+SNR) \tag{1.2}$$

where N is the number of MIMO data streams connected to the device. The graph on the right highlights the advantage of MIMO in spectrum efficiency. While SISO systems show a modest increase in spectrum efficiency with higher SNR, MIMO systems exhibit exponential growth as the number of beams increases. For instance, a 4-Beam MIMO system can transmit four independent data streams concurrently, achieving four times the data rate of a SISO system, while maintaining the same modulation and bandwidth per stream. Digital processing-based MIMO is already widely used in microwave-band receivers. However, the omnidirectional transmission and reception of multiple MIMO streams in the microwave band spread energy across the entire space, unintentionally occupying spectrum resources of other devices and limiting the overall wireless capacity improvement. In contrast, MIMO in the millimeter-wave band can leverages spatial multiplexing through highly directional analog beamforming, effectively overcoming the constraints imposed by SISO systems. By efficiently utilizing spatial dimensions, millimeter-wave MIMO not only delivers higher data rates for individual devices but also optimizes spectrum usage across the network. This makes it a vital technology for addressing the growing demand for high-speed, high-capacity communication in next-generation systems.

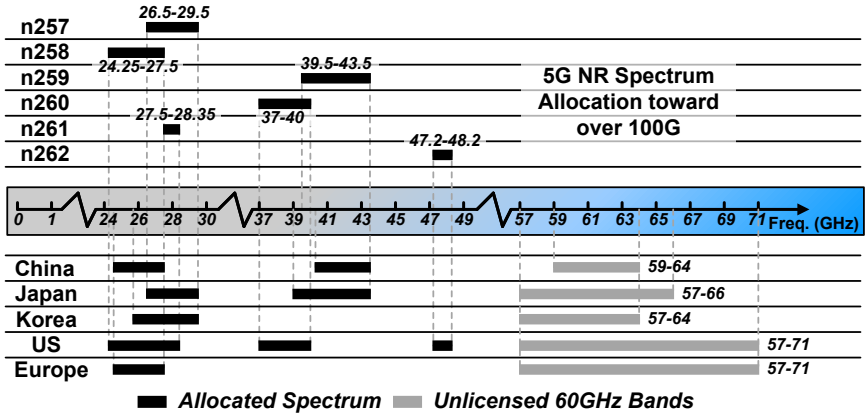


Figure 1.12: Latest 5G NR FR2 bands and global licensed/potential spectrum allocation for now and future.

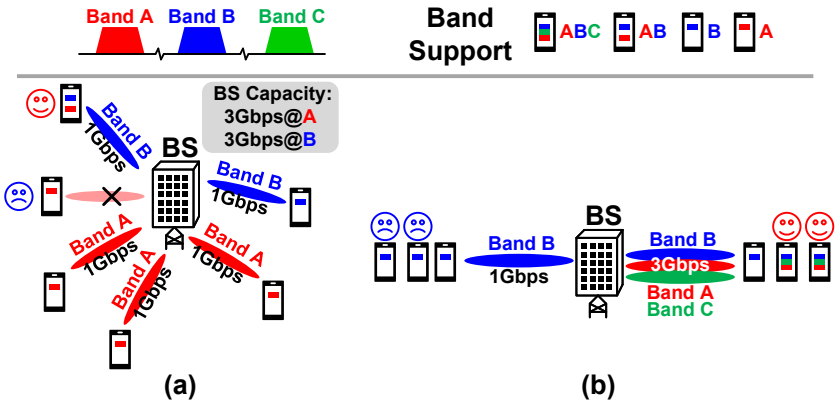


Figure 1.13: Wireless capacity utilization comparison with/without multi-band operation.

1.2.2 Multi-Band Communication Towards Higher Channel Utilization Efficiency

While spatial multiplexing and abundant spectrum resources promise large wireless capacity, channel utilization efficiency can still suffer due to unpredictable device connections and varying usage scenarios. This challenge becomes more prominent at millimeter-wave frequencies due to the far separated bands. For instance, the allocated and potential 5G NR millimeter-wave bands, as shown in Fig. 1.12, are distributed across a wide range, from 24 GHz to 71 GHz, to maximize available spectrum resources.

However, for optimal RF performance, millimeter-wave receiver ICs are typically de-

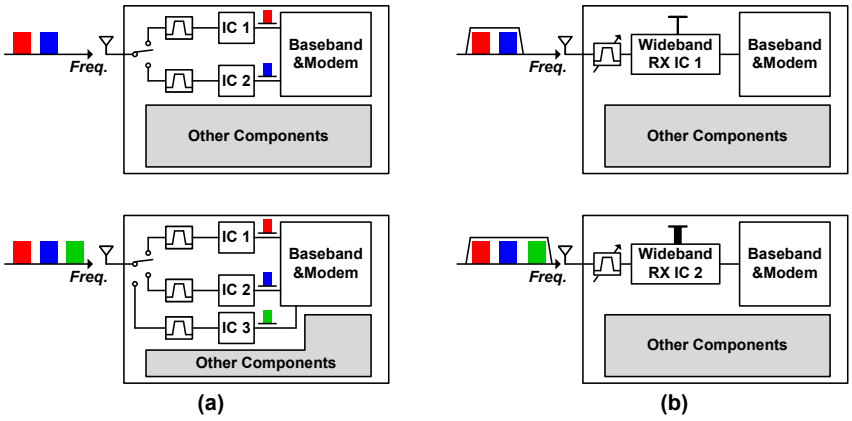


Figure 1.14: (a) Multiple front-end IC solution for multi-band operation. (b) Wide-band design solution for multi-band operation.

signed with limited bandwidth, restricting them to specific bands within a given standard. While single-band devices can achieve high data rates through MIMO, their inflexibility can lead to underutilized capacity and degraded overall system performance.

Fig. 1.13(a) illustrates a scenario where single-band devices supporting only Band A are unable to access the network due to full utilization of Band A's capacity, even though Band B remains underutilized. Devices supporting multiple bands, however, can dynamically switch to Band B and fully utilize the available resources, preventing capacity wastage and improving user experience.

Fig. 1.13(b) demonstrates another case where spatial multiplexing is limited for a group of devices in the same direction. Devices restricted to Band B are forced to share a single spatial beam, reducing individual data rates. Conversely, multi-band-capable devices can access separate bands (A, B, and C), enabling concurrent spatial streams and maximizing data throughput without interference.

Thus, multi-band operation is essential for next-generation receivers to enhance overall channel utilization efficiency, ensuring better adaptability and resource allocation in diverse scenarios while preventing capacity bottlenecks illustrated in Fig. 1.13.

1.2.3 Scalability in Communication System Evolution

As wireless communication standards evolve continuously across the globe, receivers designed for next-generation systems must possess scalability to accommodate new operating frequencies while maintaining area and power efficiency with minimal additional cost. Two conventional solutions for multi-band operation are illustrated in Fig. 1.14.

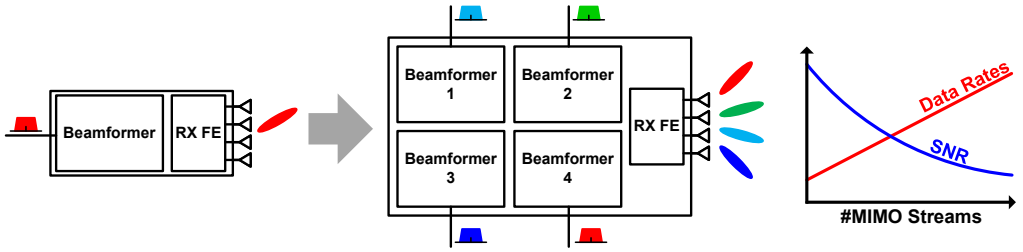


Figure 1.15: Conventional solution for millimeter-wave MIMO receiver.

The multi-IC solution shown in Fig. 1.14(a) achieves optimized RF performance and robust tolerance to inter-band interference by utilizing independent front-end RX ICs for each band. However, this approach is highly uneconomical and non-scalable. Adding support for new frequency bands requires additional ICs, along with redesigning the PCB and peripheral components, leading to increased costs and design complexity. Furthermore, this solution consumes valuable space needed by other components, posing challenges for small-form-factor devices. The wide-band solution in Fig. 1.14(b) eliminates the need for additional ICs when scaling to more bands. However, it still requires a full redesign for each extension, resulting in significant design overhead. Additionally, this approach consumes considerably more power, even when wideband signal reception is unnecessary. It is also more susceptible to inter-band interference, and power inefficiency worsens as the frequency range extends.

Similar scalability challenges arise with MIMO receivers. As shown in Fig. 1.15, conventional MIMO receivers use multiple beamformers with a shared aperture, tying the chip area directly to the number of supported MIMO streams. Scaling to support more MIMO streams in the future requires redesigning the receiver with a larger chip area. Moreover, while overall data rates improve, the SNR for individual beams degrades due to the shared-aperture design. This non-scalable approach is further constrained by the fixed signal chain design, optimized for the maximum number of MIMO streams. In real-world scenarios, MIMO receivers often only need to handle fewer streams or even a single beam, resulting in degraded performance when using a design over-optimized for maximum stream capacity.

In summary, the realization of multi-band and MIMO receivers for next-generation systems must achieve not only high performance but also excellent scalability. Receivers should maintain optimal area and power efficiency across diverse scenarios while being prepared for continuous system evolution with minimal design overhead and cost.

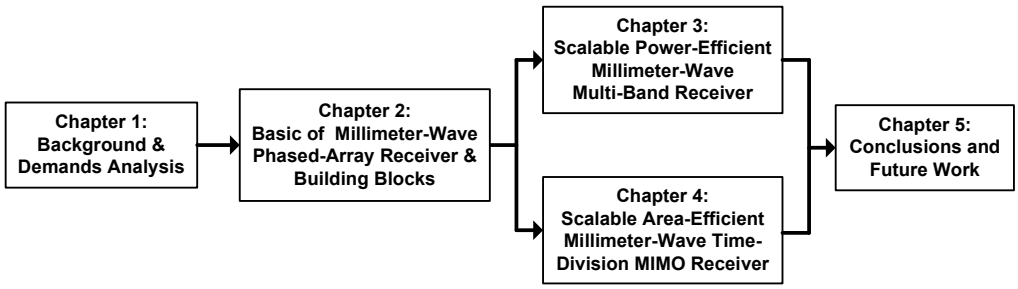


Figure 1.16: The organization of this thesis.

1.3 Thesis Objective and Organization

This thesis focuses on presenting novel architectures and design techniques for millimeter-wave phased-array receivers tailored to meet the demands of next-generation high-performance wireless communication standards. To address these requirements, both innovative receiver topologies and advanced building block circuit designs are essential.

The thesis is organized into five chapters, as illustrated in Fig. 1.16:

Chapter 2 provides an overview of the fundamentals of millimeter-wave phased-array receivers and their key components. It reviews existing receiver topologies and building block techniques, offering a detailed analysis of their strengths and limitations. This chapter serves as the foundation for the subsequent development of advanced phased-array receiver architectures discussed throughout the thesis.

Chapter 3 introduces a scalable and power-efficient solution for multi-band receivers. A 2-channel multi-band phased-array receiver prototype is presented, covering the full range of 5G NR bands. Measurement results validate its performance, demonstrating strong inter-band interference rejection and high power efficiency under various operating conditions, including worst-case scenarios. This chapter establishes the proposed architecture as a reliable and adaptable solution to address the challenges posed by congested spectrum environments, paving the way for future millimeter-wave communication systems.

Chapter 4 explores a novel scalable and area-efficient time-division MIMO (TD-MIMO) architecture that tackles the trade-offs between chip area and MIMO stream capacity in compact phased-array designs. A 4-stream, 8-element TD-MIMO phased-array receiver prototype is implemented, achieving a data rate of 9.6 Gbps with successful 64-QAM MIMO reception. This architecture demonstrates the highest reported area and spectral efficiency to date. With advancements in CMOS technology and further build-

ing block optimizations, the TD-MIMO architecture is positioned to support even more MIMO streams, setting new benchmarks for data rates in next-generation communication systems.

The final chapter concludes the thesis by summarizing the techniques introduced in Chapters 3 and 4. Additionally, it discusses the remaining challenges and outlines future research directions to further advance the development of millimeter-wave phased-array receivers.

Chapter 2

Millimeter-Wave Phased-Array Receivers and Blocks

Although millimeter wave bands greatly extends the channel capacity in wireless communication, its high frequency nature results in substantial propagation losses. Considering an isotropic transmitter (TX) and receiver (RX), as shown in Fig. 2.1, the free-space path loss can be described by the Friis transmission equation:

$$P_{RX} = P_{TX}\frac{A_{RX}}{4\pi d^2} \tag{2.1}$$

Here, P_{TX} and P_{RX} represent the transmitted and received power, respectively, while A_{RX} denotes the effective aperture (area) of the RX antenna, and d is the distance between the TX and the RX. In free space, electromagnetic waves propagate uniformly in all directions, causing the power density at a distance d from the TX to be inversely proportional to the surface area of a sphere with radius d. Consequently, the received signal power P_{RX} is directly proportional to the aperture of the RX antenna, A_{RX}. Although the energy spreading of the spherical wavefront is frequency-independent, the physical size of the antenna depends on the signal frequency. For a typical planar antenna, the aperture area is proportional to $\lambda^2/4\pi$, where λ represents the signal wavelength. Substituting this relationship into the Friis equation yields:

$$P_{RX} = P_{TX}(\frac{\lambda}{4\pi d})^2 = P_{TX}(\frac{c}{4\pi d f})^2 \tag{2.2}$$

The term $(\lambda/4\pi d)^2$ in Eq. 2.3 is referred to as the free-space path loss (FSPL), which is inversely proportional to the square of the carrier frequency. It should be noticed that the energy is actually lossless in the space and the effective loss at RX is just a result of power spreading. The FSPL is strictly a result of the fact that an isotropic receiver

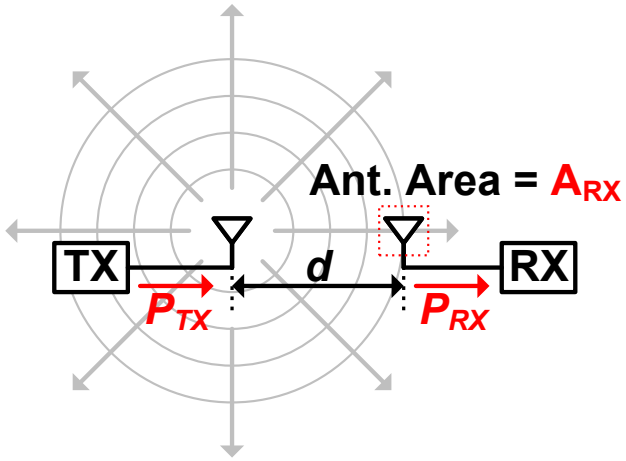


Figure 2.1: Free-space propagation with omnidirectional antennas

antenna aperture scales with frequency. Since the output power of a TX IC is constrained by CMOS technology and cannot be arbitrarily increased, the received signal power level is significantly weaker compared to lower microwave frequency with same distance d. In other word, the achievable communication distance at mmWave frequencies is also significantly shorter compared to lower microwave frequencies. For example, under the same P_{TX}, the maximum communication distance d for a 28 GHz signal is only 1/49 of the distance achievable at 4 GHz for the same bit error rate (BER) and modulation scheme. Compounding this issue, the saturated output power of a TX also decreases with increasing frequency due to technological limitations, further restricting communication range at mmWave bands.

However, the higher directivity of planar antennas in the millimeter-wave band partially compensates for the link gain loss. As illustrated in Fig. 2.2, the transmitted energy is concentrated within a narrower beam angle, while the receiver achieves higher gain for specific incident beam angles. Incorporating this additional antenna gain, the Friis transmission equation becomes:

$$P_{RX} = P_{TX} G_{TX} G_{RX} \left(\frac{\lambda}{4\pi d}\right)^2 \tag{2.3}$$

where G_{TX} and G_{RX} represent the antenna gains of the transmitter and receiver, respectively. Typically, planar antennas have a gain of only 5 to 10 dBi, which is insufficient

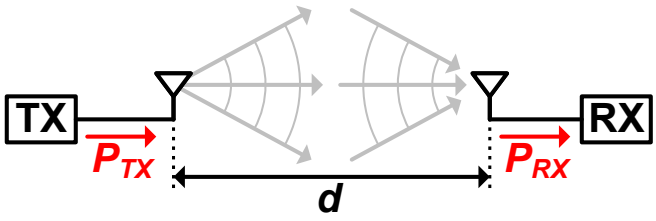


Figure 2.2: Free-space propagation with directional antennas

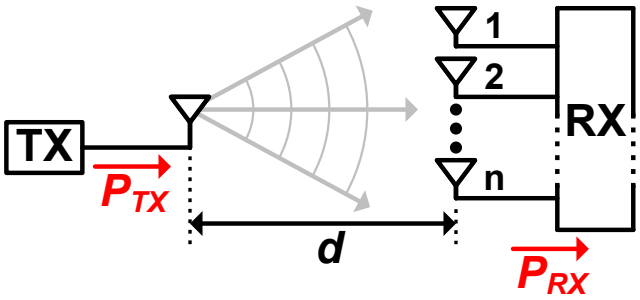


Figure 2.3: Free-space propagation with directional antennas

to compensate the significant FSPL in millimeter-wave band. To mitigate the reduction in P_{RX} at higher frequencies predicted by the Friis equation, a larger receiver antenna aperture is necessary. As depicted in Fig. 2.3, although antenna dimensions decrease with frequency, an array of antennas can be used to achieve a larger effective aperture, compensating for the increased FSPL more effectively than a single antenna. For an RX antenna array with n antennas, the Friis transmission equation becomes:

$$P_{RX} = P_{TX} G_{TX} n G_{RX} \left(\frac{\lambda}{4\pi d}\right)^2 \tag{2.4}$$

In fact, with the same equivalent receiving antenna aperture, the received power P_{RX} can be identical at both millimeter-wave and lower microwave frequencies. Moreover, if both the TX and RX have the same equivalent antenna apertures, the received power at millimeter-wave frequencies can even surpass that of microwave frequencies.

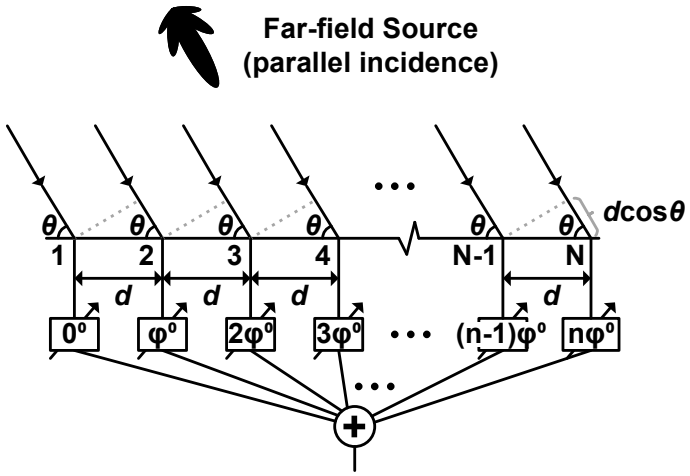


Figure 2.4: Phased-array mathematics

2.1 Phased-Array Calculations

When an antenna array is configured according to a specific geometric pattern, the signals received at each element interact and interfere with each other, producing unique and valuable characteristics. Such an array, composed of multiple receiving elements where each receives a copy of the same signal but with varying phase shifts, is known as a phased array. By electronically controlling the phase shifts, the direction of the received beam can be adjusted, which is also called beamforming. The versatile beamforming technique is applicable to both signal transmission and reception. In this thesis, however, the focus is on the phased-array receiver, which plays a crucial role in enhancing signal quality and achieving high directionality in millimeter-wave systems.

2.1.1 Beamforming and Beam Steering

For a far-field radiation source arriving at different incident angles, the wavefront phase at each antenna element in a phased-array receiver differs due to the varying path lengths. As a result, the combined signal power level varies with the incident angle, exhibiting a directional response. The mathematical model of a one-dimensional phased-array receiver with N elements is illustrated in Fig. 2.4.

In this model, all receiving elements are uniformly spaced with a distance d between adjacent elements. The angle of incidence of the signal relative to the antenna plane is denoted by θ, and the relative phase shift between adjacent elements is represented by φ.

The resulting interference pattern of the array, which depends on θ, is described by the Array Factor (AF):

$$\begin{aligned} AF(\theta) &= \sum_{n=1}^{N} e^{j(n-1)[kd\cos(\theta)+\varphi]} \\ &= \sum_{n=1}^{N} e^{j(n-1)\phi}, \phi = kd\cos(\theta)+\varphi \\ &= 1 + e^{j\phi} + e^{j2\phi} + \cdots + e^{j(N-2)\phi} + e^{j(N-1)\phi} \end{aligned} \tag{2.5}$$

or equivalently:

$$AF(\theta) = 1 + e^{j\phi} + e^{j2\phi} + \cdots + e^{j(N-2)\phi} + e^{j(N-1)\phi} \tag{2.6}$$

Here, $\phi = kd\cos(\theta)+\varphi$ is defined for simplicity in Eq. 2.5 and Eq. 2.6, where k is the wavenumber. To solve the resulting polynomial, the greatest common divisor of the coefficients is applied to both sides of Eq. 2.5. This manipulation yields the following equation:

$$AF(\theta)e^{j\phi} = e^{j\phi} + e^{j2\phi} + \cdots + e^{j(N-1)\phi} + e^{jN\phi} \tag{2.7}$$

By subtracting Eq. 2.7 from Eq. 2.6, the general term formula for AF can be derived as follow:

$$\begin{aligned} AF(\theta)(e^{j\phi}-1) &= e^{jN\phi} - 1 \\ AF(\theta) &= \frac{e^{jN\phi}-1}{e^{j\phi}-1} \\ &= e^{j\frac{N-1}{2}\phi}\left(\frac{\sin\frac{N\phi}{2}}{\sin\frac{\phi}{2}}\right) \end{aligned} \tag{2.8}$$

Finally, by changing the phase reference plane to the center of the array, Eq. 2.8 simplifies to:

$$AF(\theta) = \frac{\sin\frac{N\phi}{2}}{\sin\frac{\phi}{2}}, \phi = kd\cos(\theta)+\varphi \tag{2.9}$$

Eq. 2.9 shows that the array factor exhibits a sinc-shaped response in free space. Consequently, the maximum AF value occurs at $\phi = 0^\circ$, regardless of the value of d. The AF is symmetrical about $\phi = 0^\circ$, which serves as the central axis. The plot of the array factor versus the beam incident angle is commonly referred to as the beam pattern.

Fig. 2.5 presents the beam pattern of a one-dimensional, eight-element phased-array receiver with an antenna pitch of $\lambda/2$. When there is zero relative phase shift between

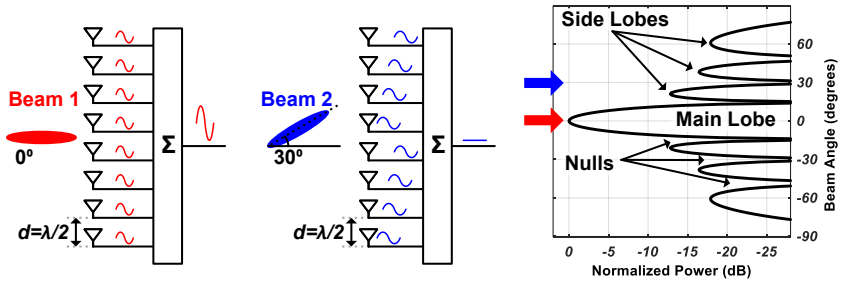


Figure 2.5: Beam pattern of phased-array receiver

elements, the received signals from beam 1 arriving at 0° incident angle are in-phase across all elements. This results in maximum beamforming gain after power combining, with the main lobe of the beam pattern centered at $\phi = 0°$. Conversely, Beam 2 arriving from 30° introduces a 90° relative phase difference between elements, leading to complete cancellation after power combining. This is reflected as a null in the beam pattern, providing effective spatial filtering of unwanted interference. There are also several side lobes in the beam pattern. Ideally, a phased array should achieve the narrowest possible main lobe and the lowest possible side lobes. With some calculation from Eq. 2.9, it can be proved that setting $d = \lambda/2$ optimizes the balance between a narrow main lobe and minimal side lobes. Reducing the antenna pitch broadens the main lobe, while increasing the pitch narrows it. However, an increased pitch introduces severe grating lobes due to spatial aliasing, which degrades performance.

By introducing an electronically controlled relative phase shift between adjacent elements, the beam pattern can be steered, allowing the main lobe to align with the desired incident angle. This process is known as beam steering. Fig. 2.6 shows the beam pattern of the phased-array receiver in Fig. 2.5, where a 90° relative phase shift between elements is applied using phase shifters. With this adjustment, the received signals from Beam 2, arriving at a 30° incident angle, become in-phase across all elements. In contrast, Beam 1, arriving at 0°, is eliminated after power combining due to the 90° relative phase difference between elements. Consequently, for this phased-array receiver, the main lobe of the beam pattern shifts to $\phi = 30°$, while 0° becomes a null in the pattern.

To further suppress the sidelobe and narrowing the mainlobe, a window function can be applied to the phased-array receiver. This operation is also called tapering, or amplitude weighting, which is a critical technique in phased-array receivers to optimize beam patterns by adjusting the gain or amplitude distribution across antenna elements. In receivers, tapering is implemented digitally or via analog attenuators, weighting signals

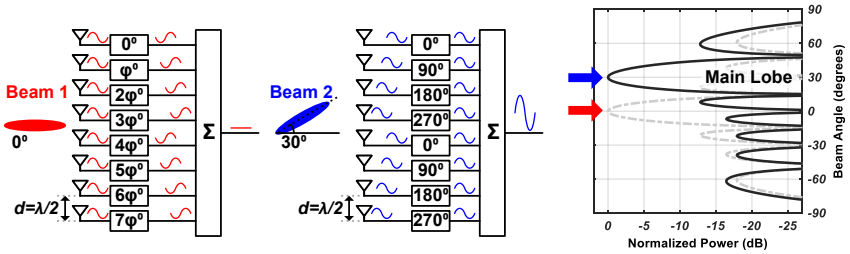


Figure 2.6: Beam steering of phased-array receiver

before beamforming. By applying a non-uniform amplitude profile—typically higher at the array center and tapered toward the edges—the receiver suppresses sidelobe levels, reducing interference from undesired directions. Common window functions (e.g., Hamming, Taylor, Chebyshev) shape this distribution, each offering distinct trade-offs between sidelobe suppression and mainlobe width. While lower sidelobes enhance interference rejection, they broaden the main beam, slightly reducing angular resolution. This balance is vital in applications like radar (clutter suppression) or communications (noise mitigation).

2.1.2 Array with True-Time Delays v.s. Array with Phase Shifter

As shown in Fig. 2.7 (a), for a beam arriving from an incident angle of θ°, the phase difference between adjacent receiving elements of the wavefront can be expressed as:

$$\Delta\varphi = \frac{2\pi d\cos\theta'}{\lambda} = \frac{2\pi d f\sin\theta}{c} = \frac{\omega d\sin\theta}{c} \tag{2.10}$$

where c is the speed of light. For a fixed antenna spacing d, the relative phase difference $\Delta\varphi$ between adjacent receiving elements varies with the signal frequency. In contrast, the relative travel distance difference between adjacent receiving elements remains constant across all frequencies, as shown in Fig. 2.7 (b). The corresponding time delay between adjacent receiving elements is given by:

$$\Delta t = \frac{d\cos\theta'}{c} = \frac{d\sin\theta}{c} \tag{2.11}$$

Since electromagnetic waves propagate at the same speed in free space, the relative inter-element time delay is frequency-independent. The phase and time delay characteristics of received signals in a phased-array receiver are summarized in Fig. 2.7 (c). To achieve precise beam steering toward a specific direction, different phase shift settings must be applied to the phased-array receiver for signals of varying frequencies. On the

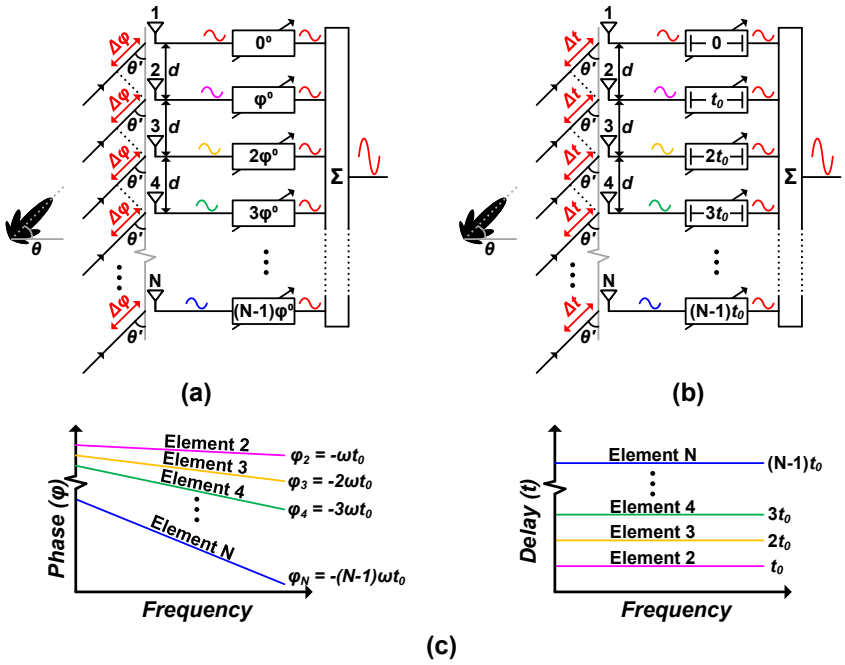


Figure 2.7: (a) Phased-array receiver with phase shifters. (b) Phased-Array receiver with true-time delays (c) Phase and time delay of received signals for beam arriving from $(90^\circ - \theta)$

other hand, accurate beam steering can be achieved for all frequencies using the same true-time delay settings. A phase shifter can be considered a narrowband approximation around the RF signal frequency. However, phased-array receiver using phase shifters suffer from frequency dispersion when handling wideband signals, as illustrated in Fig. 2.8 [4]. This dispersion causes uneven spectral reception and degrades signal quality, especially for beams arriving at large incident angles [1, 5, 6]. Moreover, the beam squinting effect becomes more significant with larger array size N since the narrower main lobe of the beam pattern amplifies the dispersion effects.

Although narrowband-phase-shifter-based phased-arrays suffer from beam squinting, they still dominate over TTD solutions due to practicality. Phase shifters offer compact, low-cost integration in CMOS/SiGe chips, critical for consumer mmWave systems such as 5G and Satcom. TTD eliminates squinting via frequency-independent delays but requires bulky analog delay lines or complex digital implementations, increasing size, power, and cost [5–8]. At mmWave frequencies, TTD's physical constraints (wavelength-scale delays) exacerbate design challenges. While squinting limits bandwidth, narrowband mmWave applications tolerate this trade-off for scalability and affordability. Thus,

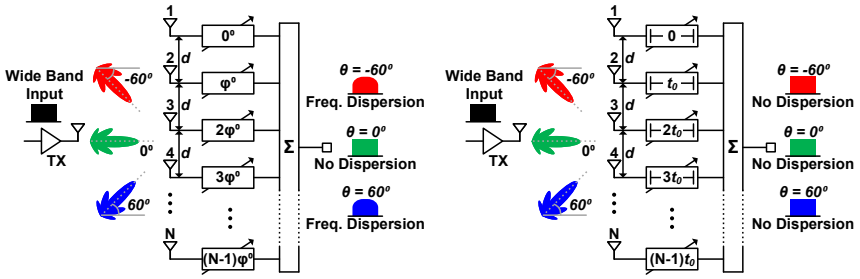


Figure 2.8: Frequency dispersion for wide-band signal in phased-array receiver

phase shifters remain favored, balancing performance with real-world feasibility in compact, high-volume systems.

2.2 Phased Array Architectures

Phased arrays can be implemented through various approach, categorized by where the beamforming operations are applied in the RX signal chain. These include digital beamforming through digital signal processing at the baseband stage, RF phase shifting at the RF front end, LO phase shifting in the frequency conversion stage, and IF (intermediate frequency) phase shifting at the intermediate signal processing stage. Each approach has unique advantages and limitations, presenting distinct trade-offs in complexity, linearity, area, and performance, making them suitable for specific application requirements.

2.2.1 RF Phase Shifting Beamforming

The placement of phase shifters and variable gain amplifiers (VGA) determines the categorization and performance of the phase-shifting architecture. Fig. 2.9 illustrates the block diagram of the RF phase-shifting architecture. In this design, phase shifting and power combining occur after the LNA but before the mixer. This approach requires only one mixer and baseband blocks for the receiver, significantly reducing chip area and power consumption, which is especially important for large-scale phased arrays in millimeter-wave systems. Additionally, interference from undesired directions is suppressed by the beam pattern after power combining, which alleviates the linearity requirements for the mixer and ADC. As a result, the RF phase-shifting architecture has become a widely adopted choice in millimeter-wave phased-array designs [1, 9–17].

However, RF phase shifters face significant challenges, particularly in millimeter-wave applications, due to their high operating frequencies. These challenges include

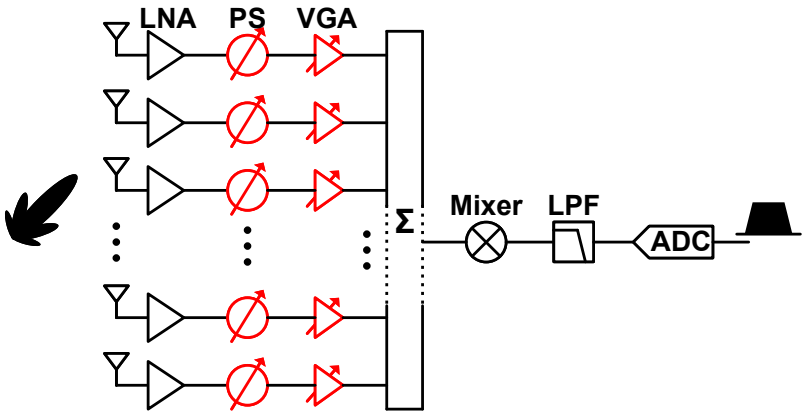


Figure 2.9: RF phase shifting architecture

phase/gain errors, bandwidth, and signal loss, which can degrade the beam controlling accuracy and SNR performance [1, 9–11]. Additionally, RF phase shifters must maintain high linearity to avoid becoming a bottleneck in the signal chain, ensuring they can handle strong signals without introducing excessive distortion or degrading signal quality. These demands highlight the critical role of RF phase shifters in meeting the stringent requirements of millimeter-wave phased-array systems.

2.2.2 IF Phase Shifting Beamforming

To mitigate performance degradation and reduce the design complexity associated with RF phase shifters, an alternative approach is to implement phase shifters and VGAs at the intermediate frequency (IF) stage within a superheterodyne architecture, as illustrated in Fig. 2.10. Since IF frequencies are typically much lower than RF frequencies, designing IF phase shifters is more straightforward and offers advantages such as reduced signal loss, improved phase and gain accuracy, enhanced bandwidth, and better linearity. For high-frequency bands such as W-band and D-band, IF phase shifting at a fixed IF avoids compromising beam control accuracy and SNR performance. The relatively lower operating frequency of the beamforming circuitry also enables the integration of advanced functionalities, such as autonomous spatial filtering (ASF) as demonstrated in [18], which are challenging to implement at W-band or higher frequencies.

However, the IF phase-shifting architecture introduces specific challenges. Each element in the array requires a mixer and an associated LO path, leading to bulky hardware and larger power consumption. Additionally, the LO distribution necessity for this archi-

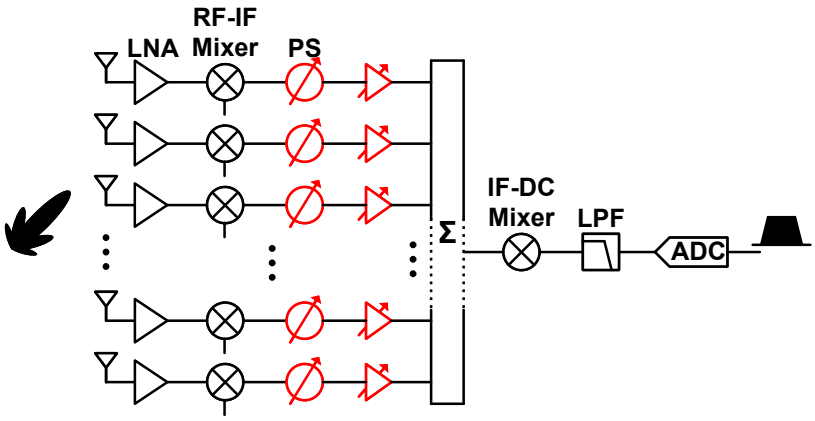


Figure 2.10: IF phase shifting architecture

tecture makes the layout design much more complicated. Moreover, since beamforming occurs after frequency conversion, the mixers are directly exposed to interference and blocking signals, potentially degrading performance. These limitations restrict the use of IF phase-shifting architectures to certain specialized applications.

2.2.3 LO Phase Shifting Beamforming

The pointing accuracy, null depth, and side lobe levels of a phased array receiver's beam pattern are highly dependent on the gain and phase errors of the phase shifters. In both RF and IF phase-shifting architectures, the phase shifters are part of the signal chain and must handle wideband signals over a large frequency range. Consequently, optimizing their gain and phase accuracy is not typically prioritized. While inter-element gain imbalances caused by gain variations during phase tuning can be partially compensated by VGAs, this compensation is limited by the tuning resolution and inherent phase errors of the VGAs.

A more effective approach to achieving precise beam control is to remove the phase shifters from the signal chain altogether. In the LO phase-shifting architecture, phase shifters are placed in the LO path, as illustrated in Fig. 2.11. Since the LO signal is a single-tone signal, the LO phase shifters do not require a flat broadband response. They only need to ensure sufficient LO signal amplitude to saturate the mixer's gate. This allows LO phase shifters to be fully optimized for resolution, coverage, and minimal phase error. Additionally, because the conversion gain (CG) remains constant once the LO swing saturates, gain errors in LO phase shifters are no longer a concern. As a result, LO phase-shifting architecture enables highly accurate beam control [2, 19–23]. The LO

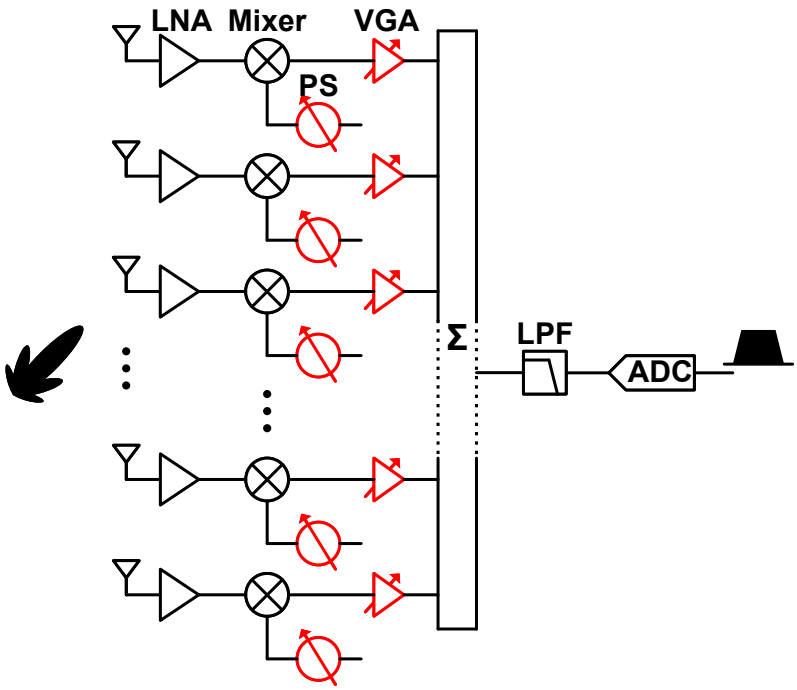


Figure 2.11: LO phase shifting architecture

phase-shifting architecture is also widely used in sub-THz phased arrays, as the frequency multiplier in such systems significantly reduces the required LO bandwidth and operating frequency for LO phase shifters [24–26]. However, similar to the IF phase-shifting architecture, the LO phase-shifting architecture requires independent mixers and LO paths for each antenna element. These complicated LO paths make it the bulkiest architecture among analog beamforming phased arrays.

2.2.4 Digital Beamforming

Digital beamforming (DBF), also known as baseband phase-shifting architecture, performs beamforming operations in the baseband and digital domain. Unlike analog beamforming, DBF directly downconverts the received signals at each antenna element, followed by analog-to-digital conversion (ADC) without phase shifters, as shown in Fig. 2.12. This approach offers the highest flexibility and precision by leveraging digital signal processing. DBF enables advanced features such as precise beam steering, null steering, multi-beam generation, and rapid reconfiguration, making it highly suitable for dynamic and complex communication environments [27, 28]. Therefore, it is widely used in sub-

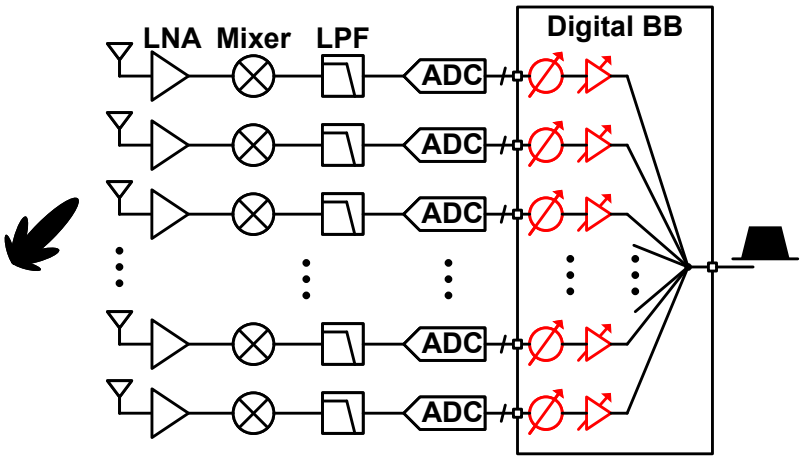


Figure 2.12: Digital beamforming (Baseband phase shifting) architecture

6GHz 5G communication system [29–31].

Despite its advantages, DBF has notable drawbacks, especially for millimeter-wave systems. One of the biggest challenges is the high power consumption and cost associated with the ADC and dedicated signal chain for each antenna element. At millimeter-wave frequencies, where arrays often have a large number of elements, this significantly increases hardware complexity and energy consumptions [32–34]. Furthermore, the wide signal bandwidths in millimeter-wave bands demand high sampling rates and resolutions from ADCs, which impose heavy burdens on data processing and storage. This necessitates high-speed interfaces and advanced digital processors, further increasing system complexity and cost [29, 33, 35, 36]. These challenges can make DBF less scalable for large millimeter-wave arrays.

2.2.5 Summary

In summary, RF phase-shifting architecture has become the preferred choice for millimeter-wave phased-array communication systems due to its ability to achieve excellent beam steering performance with minimal hardware complexity. Compared to alternative beamforming techniques such as IF and LO phase shifting, RF phase shifting offers a more direct and power-efficient approach to controlling the phase of incoming signals. This makes it particularly suitable for the stringent high-frequency and high-bandwidth requirements of millimeter-wave applications.

As illustrated in Fig. 2.13 and Fig. 2.14, a complete millimeter-wave phased-array re-

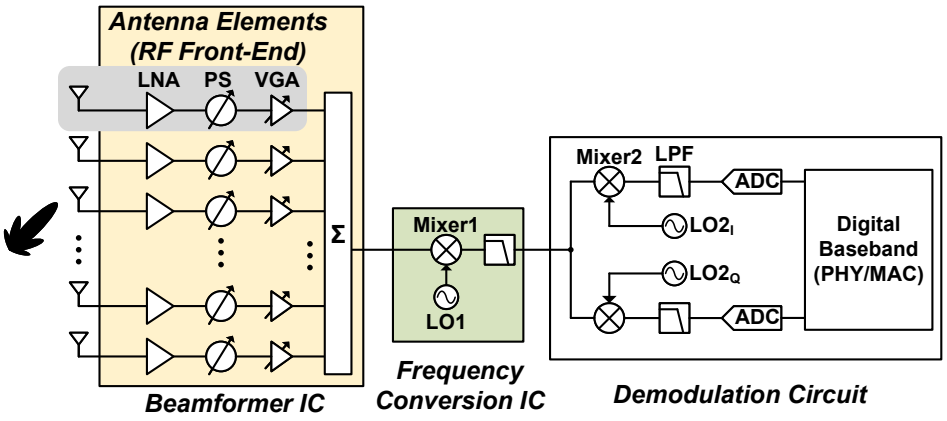


Figure 2.13: Typical IC layout of RF phase shifting phased-array receivers.

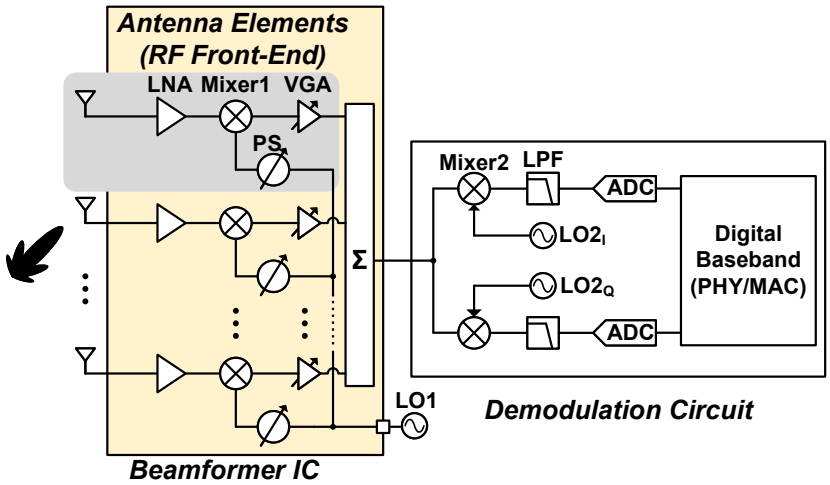


Figure 2.14: Typical IC layout of LO phase shifting phased-array receivers.

ceiver system is composed of several key functional components, including analog beamforming, frequency conversion, demodulation, and digital processing. In practical implementations, these functional blocks are typically designed as independent ICs to enhance design flexibility, simplify system integration, and facilitate easier maintenance and future upgrades. Among these components, the beamformer IC plays a pivotal role in determining the overall system performance, as it is responsible for the precise phase and amplitude steering of signals across the antenna array. Recent advancements in millimeter-wave receiver design have primarily focused on optimizing beamformer ICs, often excluding the

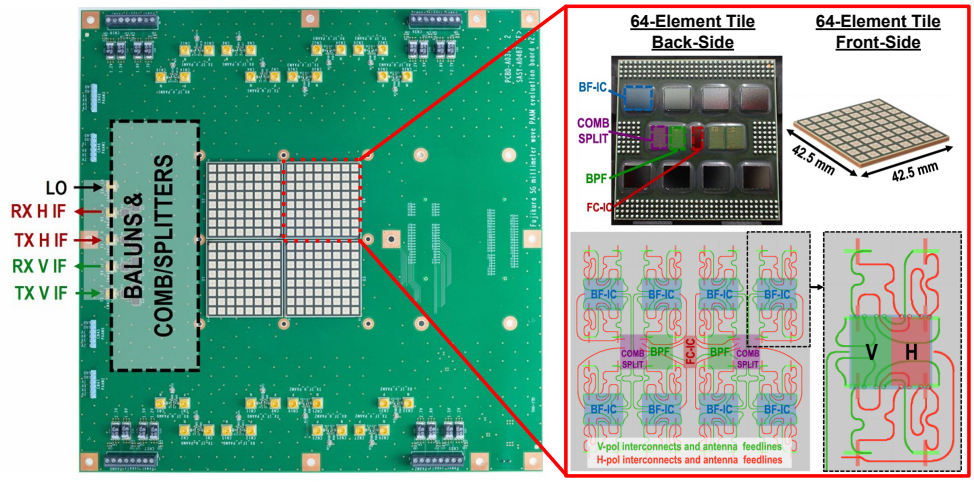


Figure 2.15: An example of 256-element millimeter-wave 5G phased-array module including multiple beamformer ICs and frequency-conversion IC [1].

demodulation function from the beamformer itself. Given the critical role of beamformers in phased-array systems, this thesis primarily concentrates on the beamformer design, emphasizing circuit techniques that enhance beam steering capabilities while minimizing power consumption and chip area.

To ensure high yield rates and simplify module design and packaging, the number of antenna elements integrated within a single beamformer IC is typically limited to 4 to 8 (e.g. 4 in [2, 11, 17] and 8 in [1]). However, achieving the required performance for millimeter-wave applications necessitates large-scale phased arrays. Consequently, millimeter-wave receiver systems often employ multiple beamformer ICs to form large planar arrays, introducing the challenge of efficient inter-chip connectivity. The RF phase-shifting beamformer architecture, as depicted in Fig. 2.13, offers a straightforward solution with a single-wire signal output, requiring only a single-layer power combining network for inter-chip connections [1, 10, 37, 38]. In contrast, the LO phase-shifting beamformer architecture, shown in Fig. 2.14, incorporates redundant and bulky LO paths for each antenna element, necessitating an additional inter-chip LO distribution network [2, 11, 17, 26]. Despite these challenges, LO phase-shifting remains a viable option due to its superior RF performance and the ability to implement specialized mixing functionalities.

An example of a large-scale 256-element millimeter-wave 5G phased-array module, featuring 32 beamformer ICs and 4 frequency-conversion ICs, is shown in Fig. 2.15, as presented in [1]. The layout on the right side of the figure provides a detailed illustration

of the interconnections among multiple ICs and the spatial arrangement of the antenna elements and chips. This modular design approach offers high scalability and flexibility, enabling the expansion of the array by simply adding more tiles. Furthermore, the separation of different functions into dedicated ICs allows for independent design and upgrades, making it highly advantageous for industrial applications.

2.3 Phase Shifters

As analyzed in previous sections, phase shifters are essential components in phased-array systems, playing a key role in determining the beamforming performance of the phased-array receiver. They can generally be categorized into passive and active types based on their operating principles and design. Passive phase shifters, such as switching-type phase shifters (STPS) and reflection-type phase shifters (RTPS), rely on reactive components like inductors, capacitors, and transmission lines to achieve phase adjustment without amplifying the signal. On the other hand, active phase shifters, such as vector-summing phase shifters (VSPS), incorporate amplifying elements to enable phase steering. Each type of phase shifter comes with its own advantages and limitations, and the choice of phase shifter depends on the specific requirements and trade-offs of the phased-array system.

2.3.1 Switch Type Phase Shifters

A typical switched-type phase shifter consists of cascaded phase-shifting units, each designed to introduce a specific phase shift by switching between discrete signal paths. As shown in Fig. 2.16, a standard single-ended 6-bit STPS is constructed using phase-shifting units with binary-weighted phase steps to minimize insertion loss. Each 1-bit phase-shifting unit utilizes RF switches to select between two signal paths, each providing a different phase delay. By carefully choosing the values of passive components, such as inductors or capacitors, in these signal paths, precise phase shifts can be achieved. STPS unit can be implemented in various configurations, including switched transmission lines, switched LC networks, and switched delay lines.

There are several ways to implement a STPS unit. Fig. 2.17(a) shows the schematic of a single-stage Π-type STPS unit along with its equivalent circuits when the control bias VC is set to 0V and the supply voltage (1V), respectively [39–41]. For millimeter-wave applications, a large bias resistor is necessary at the gate of the transistor switch to isolate the RF signal, thereby reducing insertion loss. In the phase delay state, transistor M1 is turned off and M2 is turned on, making the circuit behave like a low-pass filter. To achieve

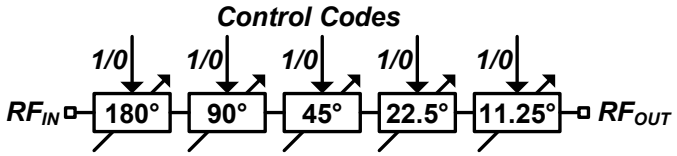


Figure 2.16: Switched-type phase shifter architecture

a desired phase shift φ, the values of the series inductor (L_S) and parallel capacitor (C_P) must be set as:

$$L_S = \frac{Z_0 \sin\varphi}{\omega_0} \qquad C_P = \frac{\tan\frac{\varphi}{2}}{\omega_0 Z_0} \tag{2.12}$$

where Z_0 is the input and output characteristic impedance of the unit, and ω_0 is the operating frequency. In the phase delay state, to prevent the parasitic capacitance C_{Para2} of the turned-off transistor M2 from affecting the phase shift, an inductor L_P is used to resonate with C_{Para2} at ω_0. The value of L_P is given by:

$$L_P = \frac{1}{{\omega_0}^2 C_{Para2}} \tag{2.13}$$

At the resonant frequency, the LC tank formed by C_{Para2} and L_P acts as an open circuit, ensuring minimal interference. In the bypass state, L_S resonates with $C_P/2$, resulting in zero phase shift. Consequently, the Π-type STPS unit achieves a phase difference of φ between two states. To enable compatibility with multi-stage cascades for finer resolution, transistors M1 and M2 are sized to maintain a characteristic impedance Z_0 of 50Ω in both the phase delay and bypass states.

Another design approach is the cross-coupled bridge T-type single-stage STPS unit, which is showed in Fig. 2.17(b) along with its equivalent circuits for both phase delay and bypass modes [40, 42–45]. In the phase delay mode, the series inductor (L_1) and the parasitic capacitance of transistor M2 (C_{Para2}) form a T-type low-pass filter, which introduces the desired phase shift. Similar to the calculations for the Π-type STPS unit, the values of (L_1) and C_{Para2} needed to achieve a phase shift of φ can be expressed as:

$$L_1 = \frac{Z_0 \tan\frac{\varphi}{2}}{\omega_0} \qquad C_{Para2} = \frac{\sin\varphi}{\omega_0 Z_0} \tag{2.14}$$

Here, C_{Para2} can be adjusted by appropriately sizing transistor M2 to achieve the required parasitic capacitance. In the bypass mode, to eliminate the phase shift introduced

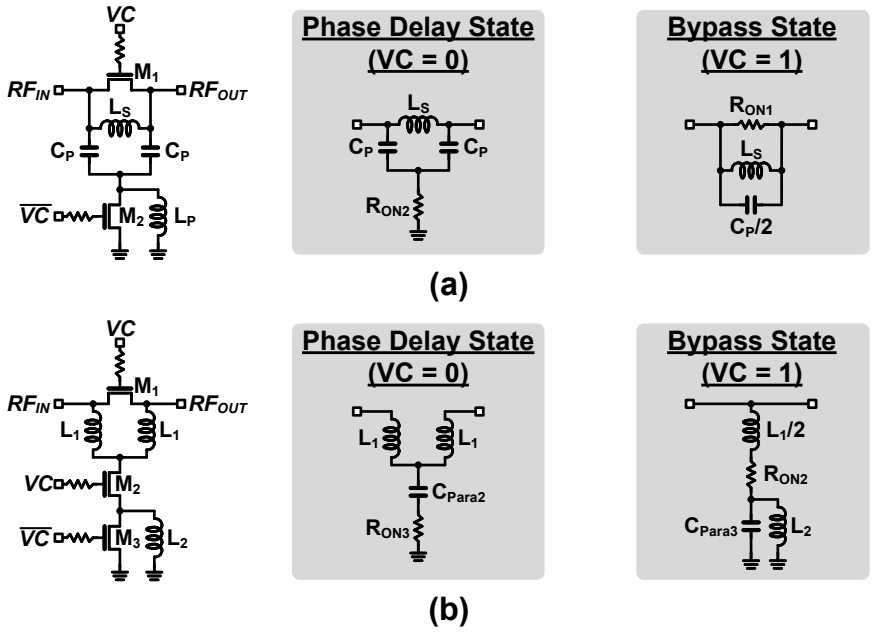


Figure 2.17: (a) Π-type STPS unit (b) T-type STPS unit

by L_1 and maintain the characteristic impedance of 50-Ω (Z_0), the values of (C_{Para3}) and L_2 must satisfy the following conditions:

$$C_{Para3} = \frac{2L_1}{{Z_0}^2} \qquad L_2 = \frac{1}{{\omega_0}^2 C_{Para3}} \tag{2.15}$$

The value of L_2 is determined after sizing transistor M3 to achieve the required parasitic capacitance C_{Para3}. This design ensures proper phase shift control in the delay mode while maintaining impedance matching and zero phase shift in the bypass mode.

In phased-array systems, maintaining low phase variation across the entire bandwidth is critical to ensure signal integrity during transmission. This characteristic, often described as group delay, directly impacts the system's performance. However, in the Π-type STPS unit, the passive network's order difference between the two modes results in different insertion phase slopes with respect to frequency. As a result, the desired phase difference φ can only be maintained over a narrow bandwidth. In contrast, the T-type STPS unit exhibits nearly identical insertion phase slopes for its two states, particularly at high frequencies. This leads to a relatively broadband and constant phase shift, minimizing the group delay deviation between the two modes. In other words, the T-type STPS unit offers lower group delay variation compared to the Π-type STPS unit, making

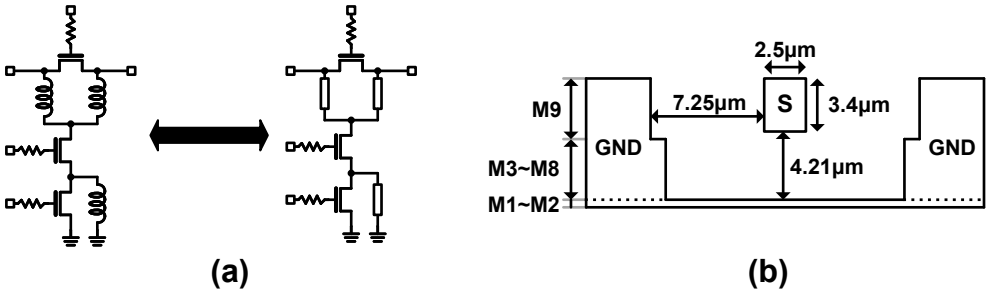


Figure 2.18: (a) Transmission line based STPS unit. (b) Cross-section structure of a typical on-chip CPW transmission line. [2]

it better suited for wideband applications [42, 43, 45]. As a result, T-type STPS units are increasingly favored in modern millimeter-wave phased-array receivers.

In millimeter-wave applications, the inductors in STPS units can be replaced with transmission lines implemented using on-chip coplanar waveguides (CPW) in CMOS technology, as shown in Fig. 2.18 (a) [43, 45]. Fig. 2.18 (b) provides an example of a 50-Ω CPW transmission line designed using 65nm CMOS technology [2]. These compact transmission lines not only save chip area but also offer greater flexibility in layout design. Additionally, using transmission lines helps mitigate isolation issues between inductors in adjacent units, further improving performance. The sequence of STPS units is another critical design consideration to minimize phase variation. The phase and impedance performance of STPS units are influenced by loading effects, which must be carefully managed. Typically, units with smaller phase shifts are placed at the center stages because they are more sensitive to mismatch and loading effects.

One of the key advantages of STPS is its ability to provide PVT (process, voltage, temperature) insensitive, accurate phase tuning for high-frequency applications, including millimeter-wave systems. Loss variation across different phase settings can be minimized by properly sizing the RF switches. Moreover, STPS units do not consume DC power and are compatible with digital control, making them well-suited for large-scale phased arrays. Their symmetrical design also supports bidirectional operation, allowing them to be shared between TX and RX paths. However, the performance of STPS is limited by insertion loss from the cascaded RF switches and the finite resolution of discrete phase steps, both of which can negatively impact system performance. The resolution of STPS involves a trade-off with insertion loss and chip area. Despite these challenges, switched-type phase shifters remain widely used in commercial analog beamforming systems due to their simple implementation, scalability, and robust PVT tolerance at high frequencies

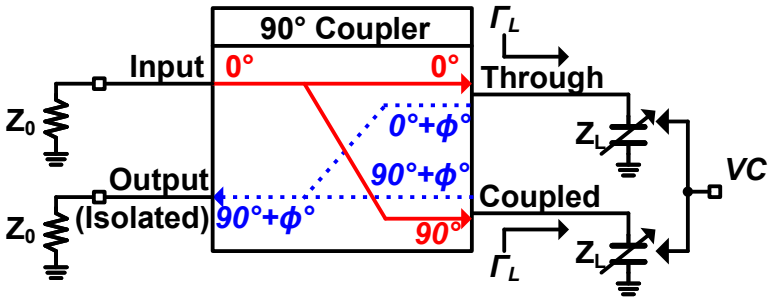


Figure 2.19: Schematic of typical reflection-type phase shifter.

[12–14, 16].

2.3.2 Reflection-Type Phase Shifters

Reflection-type phase shifters (RTPS) is another widely used passive phase shifter in phased-array systems. RTPS operates by reflecting the input signal off a variable impedance load, with the phase shift determined by the reactive properties of the load impedance. Fig. 2.19 shows the schematic of a typical RTPS, which includes an ideal 3-dB 90° quadrature coupler and two tunable loads. The quadrature coupler splits the input signal equally between the through port and the coupled port, introducing phase shifts of 0° and 90°, respectively. The reflected signals from the two ports are combined in phase at the isolated port, producing an output signal with the desired phase shift φ. The phase-shifting operation is governed by the reflection coefficient Γ_L, which is given by:

$$\Gamma_L = \frac{Z_L - Z_0}{Z_L + Z_0} \tag{2.16}$$

where Z_0 is the source impedance, and Z_L is the tunable load impedance connected to the through and coupled ports. The desired phase shift φ can then be expressed as:

$$\varphi = -90^\circ + \phi = \angle\Gamma_L = -90^\circ + 2\tan^{-1}(\frac{Z_L}{Z_0}) \tag{2.17}$$

The total phase shift range of an RTPS is determined by the tunable range of the load impedance:

$$\Delta\varphi = \angle\Gamma_{L,max} - \angle\Gamma_{L,min} = 2[\tan^{-1}(\frac{Z_{L,max}}{Z_0}) - \tan^{-1}(\frac{Z_{L,min}}{Z_0})] \tag{2.18}$$

To enhance the phase coverage of RTPS, it is crucial to maximize the load impedance tuning range. The tunable load can be implemented using variable capacitors, such as varactors or switched capacitor arrays, or using series/parallel LC tanks. For a purely capacitive load, the theoretical maximum phase shift range is limited to 180° (for C_{min} = 0 and $C_{max} = \infty$), which is impractical in actual circuits. In practical CMOS processes, the capacitance variation ratio C_{max}/C_{min} of on-chip varactors typically ranges from 2 to 3. This limits the phase shift range to a maximum 120° for a pure varactor and only 60° for an LC tank with the same capacitance variation ratio. Parasitic capacitances and non-ideal quality factors (Q) further restrict the effective phase shift range. The insertion loss of the RTPS depends on the load impedance Z_L and is given by:

$$IL = IL = 20\log|\Gamma_L| \tag{2.19}$$

Since the insertion loss varies as a function of the phase shift φ. maintaining $|\Gamma_L|$ as constant as possible across the tuning range of Z_L is critical. This can be achieved through careful impedance matching and the use of high-Q reactive components. While switched capacitor arrays can extend the capacitance tuning range compared to varactors, they come at the cost of reduced tuning resolution, increased parasitic capacitance, and degraded quality factor. These trade-offs must be carefully balanced in the design to optimize the phase shift range, step size, and insertion loss of the RTPS. [cite] Various approaches have been explored in previous research to improve the phase shift range of RTPS. High-order reactive networks have been shown to effectively extend the phase shift range [46–50]. [49] achieved a 360° phase shift range by cascading multiple RTPS stages, while [47, 48] utilized asymmetrical load impedances and separate control voltages for the two loads to realize a similar 360° range. However, these improvements often come at the cost of increased chip area, greater design and control complexity, or reduced phase resolution, making them less ideal for some applications.

In summary, RTPS provides high-resolution, continuous phase control in a compact form factor. The area efficiency of RTPS becomes even more advantageous at higher millimeter-wave frequencies, as the size of the coupler decreases with increasing operating frequency. Similar to STPS, the passive symmetrical design of RTPS enables bidirectional operation and high linearity, allowing it to be shared between the TX and RX paths. However, achieving a 360° phase shift range while maintaining these advantages remains a significant challenge. Additionally, at higher frequencies, parasitic effects increase the design complexity. Despite these limitations, RTPS continues to be a popular choice for compact and power-efficient phase shifters in modern beamforming applications.

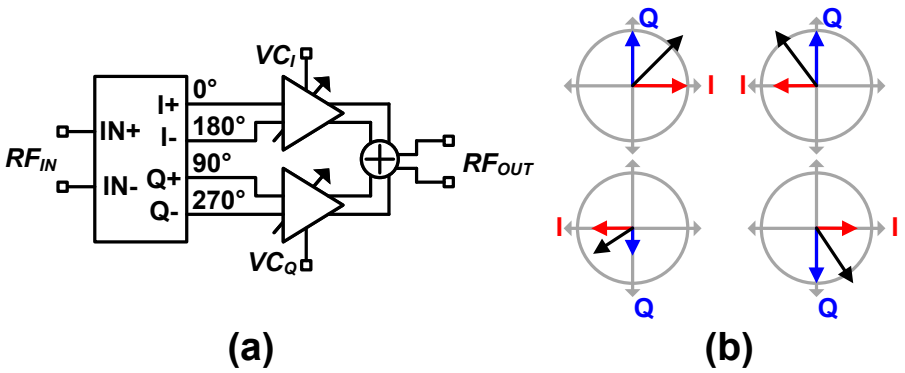


Figure 2.20: (a) Schematic of typical active vector-summing type phase shifter. (b) Phase map of VSPS with 360° phase shift coverage.

2.3.3 Vector-Summing Type Phase Shifters

As its name suggests, the vector-summing type phase shifter (VSPS) adjusts the phase by manipulating the amplitude and phase of orthogonal signal components. A typical VSPS structure is shown in Fig. 2.20 (a). The input signal is first split into two quadrature components (0° and 360°) using an in-phase/quadrature (I/Q) splitter. Each component is then independently amplified or attenuated through variable gain amplifiers (VGAs) to control their magnitudes. The adjusted signals are recombined at the output, resulting in a vector sum that achieves the desired phase shift. The output phase shift φ and gain A of the recombined signal can be expressed as:

$$Ae^{j\varphi} = G_I A_S e^{j0^\circ} + G_Q A_S e^{j90^\circ} \tag{2.20}$$

where G_I and G_Q are the adjustable gains of the in-phase and quadrature paths, respectively, and A_S represent the insertion loss of the I/) splitter. To realized a full 360° phase shift range, VSPS is typically designed with a fully differential structure. By swapping the polarity of G_I and G_Q, the output phase can cover all four quadrants, as illustrated in Fig. 2.20 (b). Through simple trigonometric analysis, the gain A and phase shift φ can be derived as:

$$A = A_S\sqrt{{G_I}^2 + {G_Q}^2} \qquad \varphi = \tan^{-1}(\frac{G_Q}{G_I}) \tag{2.21}$$

Here, the sign of G_I and G_Q determines the phase quadrant. The integrated VGAs allow the VSPS to provide continuous control of both phase and gain [11, 51–53]. To

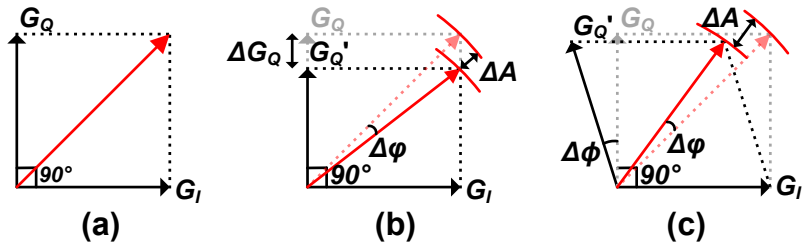


Figure 2.21: (a) Schematic of typical active vector-summing type phase shifter. (b) Phase map of VSPS providing 360° phase coverage.

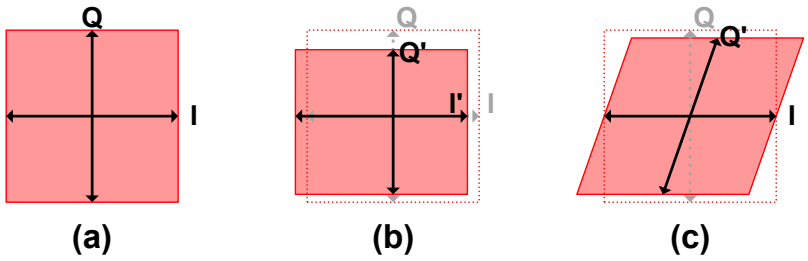


Figure 2.22: (a) Schematic of typical active vector-summing type phase shifter. (b) Phase map of VSPS with 360° phase shift coverage.

interface seamlessly with digital control systems without requiring additional digital-to-analog converters (DACs), digitally controlled amplifiers can be used [54–57]. However, this implementation sacrifices phase and gain tuning resolution. Alternatively, passive tunable attenuators can replace VGAs to achieve phase shifting, but their high insertion loss reduces the advantages of VSPS compared to STPS and RTPS. As a result, most VSPS designs are implemented as active phase shifters. The detail of VGAs and tunable attenuators will be discussed in following sub-section.

The I/Q splitter is critical to the overall performance of the VSPS. As illustrated in Fig. 2.21 and Fig. 2.22, any amplitude imbalance or phase mismatch introduced by the I/Q splitter under default VGA biasing conditions results in phase and gain errors. Additionally, these imperfections cause phase map distortions, affecting the achievable gain and phase coverage.

A commonly used parameter for characterizing I/Q splitter performance is the image rejection ratio (IRR). Originally, I/Q splitters were employed in superheterodyne Hartley

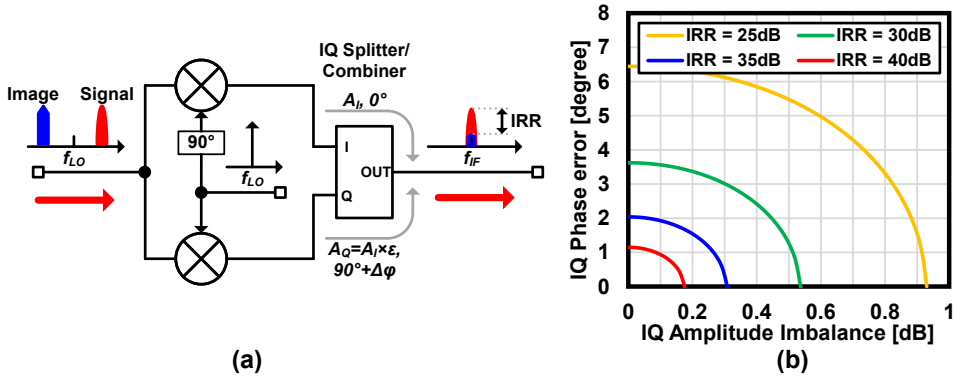


Figure 2.23: (a) IRR degradation caused by I/Q splitter/combiner error in Hartley receiver architecture. (b) IRR contour plot against IQ amplitude imbalance and phase error.

receivers, which rely on quadrature down-conversion to achieve image-free reception, as illustrated in Fig. 2.25(a) [58–60]. The IRR comprehensively indicates both I/Q amplitude imbalance and phase error, and can be expressed as:

$$IRR = \frac{1+\varepsilon^2+2\varepsilon\cos\Delta\varphi}{1+\varepsilon^2-2\varepsilon\cos\Delta\varphi} \approx \frac{4}{(\varepsilon-1)^2+(\Delta\varphi)^2} \tag{2.22}$$

Where ε is the I/Q amplitude imbalance (A_Q/A_I) and $\Delta\varphi$ is the I/Q phase error in radians. A perfect I/Q balance (i.e., $\varepsilon = 1$ and $\Delta\varphi = 0$) yields infinite image rejection. Figure 2.25(b) shows IRR contours as a function of amplitude imbalance and phase error. To achieve 30 dB of IRR, the allowed I/Q amplitude imbalance usually less than 0.25 dB, and the phase error must not exceed 3°.

To produce a full 360° phase shift, the outputs of the I/Q splitter must be differential. A conventional solution, shown in Fig. 2.24, employs a 3-dB 90° coupler followed by two baluns [57]. Although this approach supports a single-ended input and offers low insertion loss with broad operating frequency range, the coupler and baluns can be bulky, especially at lower frequencies. On-chip couplers also suffer performance degradation at lower bands (e.g., 5G NR FR3 operating from 8 to 24 GHz).

Another popular choice for I/Q splitting is the RC-based passive poly-phase filter (PPF). There are two main PPF topologies, as shown in Fig. 2.25 [59–62]. Type-I PPFs maintain I/Q orthogonality at all frequencies, but the I and Q amplitudes are equal only at the pole frequency $f_C = 1/(2\pi RC)$. In contrast, Type-II PPFs ensure equal I and Q amplitudes for all frequencies but achieve orthogonality only at f_C. The Type-II PPF is typically preferred due to its theoretically better (3-dB lower) insertion loss compared

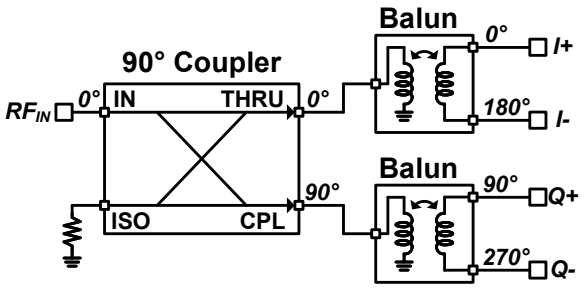


Figure 2.24: Schematic of conventional 90° coupler based I/Q splitter

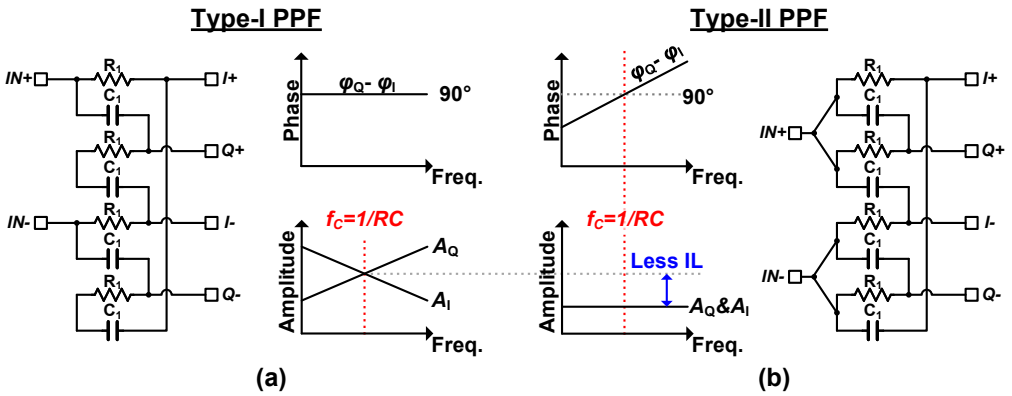


Figure 2.25: (a) Schematic of typical type-I passive RC poly-phase filter (PPF). (b) Schematic of typical type-II RC PPF

to Type-I [2, 11, 51, 52]. Because PPFs utilize only resistors and capacitors, they offer a compact core and simple impedance matching. However, the first-order RC-based filtering severely limits the operating bandwidth and incurs high insertion loss. Cascading multiple PPF stages can broaden the bandwidth but at the cost of higher insertion loss. Furthermore, on-chip resistor variations due to process-voltage-temperature (PVT) conditions can shift f_C from its intended value, which makes a calibration mechanism necessary [63].

To address the insertion loss and bandwidth limitations of RC PPFs, quadrature all-pass filters (QAFs) based on LC series resonators have been proposed, as shown in Fig. 2.26. By introducing an inductor into the network, the QAF provides higher-order filtering, reduces insertion loss, and broadens the bandwidth [64, 65]. Adjusting R_1 or adding

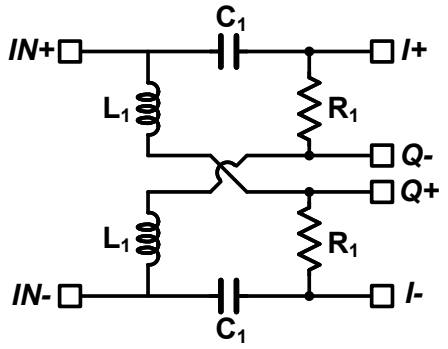


Figure 2.26: Schematic of typical quadrature all-pass filter.

series resistors allows control of the tank's quality factor, thereby make the bandwidth of QAF tunable. However, QAFs occupy larger chip areas, and careful layout design is required to mitigate coupling between inductors. Moreover, impedance matching for QAFs can be challenging, and their performance is sensitive to source and load impedances.

Recently, fully differential quadrature transformer-based I/Q splitters have gained popularity due to their robustness against PVT variations and wide-band operation, as illustrated in Fig. 2.27(a) [56, 66–68]. Replacing discrete inductors and capacitors with a one-inductor-footprint I/Q transformer creates a higher-order network with significantly reduced insertion loss and improved tolerance to capacitive and resistive loading. By cascading multiple stages (Fig. 2.27(b)), phase and amplitude mismatches can be further suppressed over a wide frequency range [66]. Simulation results (Fig. 2.27(c)) demonstrate that a three-stage transformer-based I/Q splitter can maintain nearly zero amplitude imbalance from 30 GHz to 60 GHz. Consequently, it can achieve over 35 dB of IRR across more than 100% relative bandwidth without requiring calibration (Fig. 2.27(d)). Although this solution is bulky, it is well-suited for high-precision, wide-band millimeter-wave designs due to its exceptional performance.

2.3.4 Summary

The advantages and limitations of the aforementioned phase shifters are summarized in Table 2.1. The selection of an appropriate phase shifter for phased-array system design depends on the specific application and required functionality. Passive phase shifters, with their inherent bidirectional operation, are particularly advantageous in time-division duplex (TDD) transceivers, where a single phase shifter can be shared between the TX

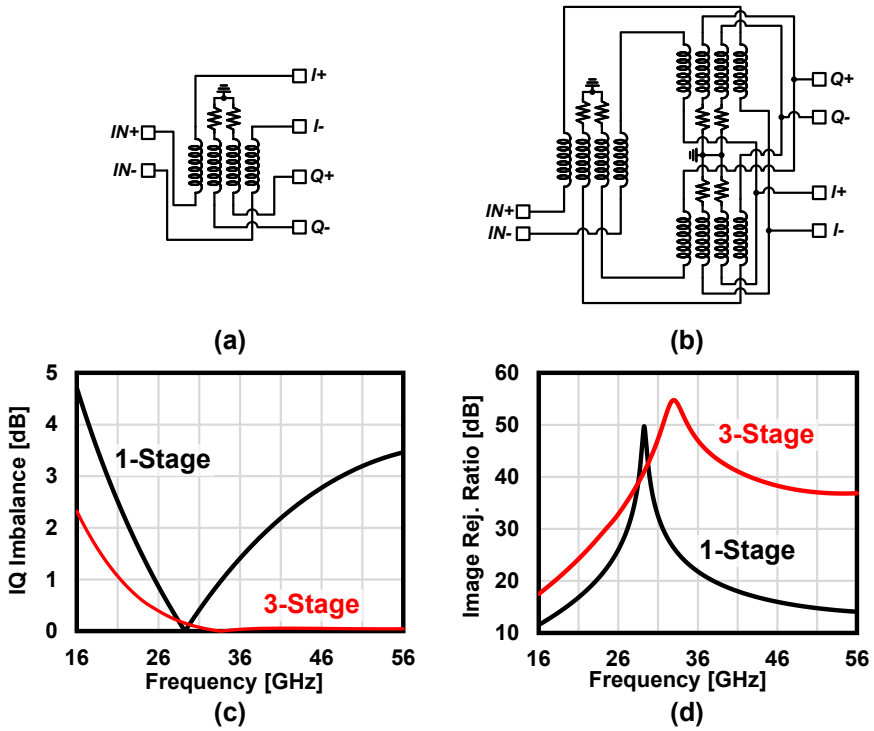


Figure 2.27: (a) Schematic of one-stage differential transformer-based I/Q splitter. (b) Schematic of cascaded 3-stage differential transformer-based I/Q splitter. (c) Simulated IQ amplitude imbalance against frequency. (d) Simulated IRR against frequency.

and RX paths to save chip area. On the other hand, active VSPS offer the largest phase and gain tuning range, making them suitable not only for phased-array systems but also for advanced functionalities, such as cross-polarization leakage cancellation in [69] and autonomous spatial filtering in [67]. In practice, different types of phase shifters can be combined to leverage their respective advantages. For example, a RTPS can be cascaded with coarse-step STPS units to achieve a passive phase shifter with both wide phase coverage and fine resolution.

2.4 Gain Control Unit

In receiver design, the gain control unit plays a critical role in maintaining optimal signal levels under varying operating conditions. It ensures that received signals are appropriately amplified or attenuated to maximize the system's dynamic range, minimize distortion, and accommodate fluctuations in input power levels. In phased-array receivers, the

Table 2.1: Performance Comparison of Phase Shifters

Architecture	Passive		Active
	STPS	RTPS	VSPS
Phase shift range	$\surd$	$\times$	$\surd\surd$
Phase resolution	$\times$	$\surd\surd$	$\surd$
Bi-directional	Yes	Yes	No
Insertion loss	$\times\times$	$\times$	$\surd$
Linearity	$\surd$	$\surd$	$\times$
Area	$\times$	$\surd$	Depends on I/Q splitter

gain control unit also compensates for gain mismatches between elements to achieve an ideal beam pattern and facilitates the application of tapering windows to enhance directivity as needed. Moreover, gain control units with switchable-polarization are necessary in VSPS. The gain control unit typically consists of variable gain amplifiers (VGAs) and variable attenuators, each performing distinct yet complementary functions. VGAs enable dynamic signal amplification, while variable attenuators manage signal reduction to prevent overloading and ensure linearity. In the following subsections, the design, implementation, and performance of VGAs and variable attenuators will be discussed in detail, emphasizing their essential roles in achieving high-performance phased-array receiver systems.

2.4.1 Variable Gain Amplifiers

The gain of an amplifier, A, is generally expressed as:

$$A = g_m(R_O \| Z_L) \tag{2.23}$$

where g_m is the transconductance, R_O is the output impedance of transistor, and Z_L is the load impedance. Consequently, the gain of a VGA can be controlled by tuning either g_m or R_O. A straightforward method to adjust g_m in an RF amplifier is by varying its bias voltage. Fig. 2.28 (a) shows a single-ended common-source stage VGA, where the gate bias voltage is controlled via a resistive digital-to-analog converter (RDAC) or capacitive digital-to-analog converter (CDAC) through a digital interface [70]. While this approach theoretically offers a wide gain tuning range, the gain becomes highly sensitive to PVT (process, voltage, and temperature) variations. Although digital compensation can address these variations, it introduces additional hardware overhead. On the other hand, Fig. 2.28(b) shows a differential pair VGA with its tail transistor biased by a current digital-to-analog converter (IDAC). In this design, the gate bias of the input pair is fixed

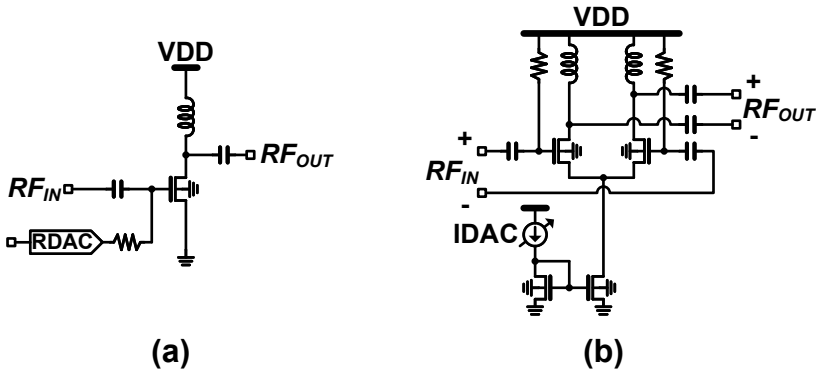


Figure 2.28: (a) Common-source stage VGA with DAC-controlled gate bias voltage. (b) Differential pair VGA with IDAC-controlled tail transistor current.

at VDD, and the g_m is controlled by the tail current. This approach provides a constant-g_m biasing scheme over PVT variations by using an IDAC with a proportional-to-absolute-temperature (PTAT) current source [71]. However, both the input capacitance C_{IN} and output resistance R_O of the input transistor in these two VGAs exhibit significant changes as g_m is tuned. These variations can introduce unpredictable phase shifts, potentially affecting the phase and gain response of adjacent blocks, such as the phase shifter.

A Gilbert cell can also be employed as a voltage-controlled VGA, as shown in the Fig. 2.29. In this configuration, the bottom differential pair, controlled by the differential voltage $V_C = V_{C1}$ - V_{C2}), steers the tail current between the two top transconductance-stage differential pairs. The small-signal gain of the Gilbert-cell-based VGA can be expressed as:

$$A = \frac{I}{4V_{OV}^2} V_C g_m (R_O \| Z_L) = \alpha (V_{C1} - V_{C2}) g_m (R_O \| Z_L) \tag{2.24}$$

where V_{OV} is the overdrive voltage of the input differential pair transistors, and I is the tail current of the Gilbert cell. From this equation, it is clear that the gain of the Gilbert-cell-based VGA is linearly proportional to the control voltage V_C. Besides, the output of Gilbert cell can be 180° flipped by applying a minus V_C. Furthermore, the output polarity of the Gilbert cell can be inverted by applying a negative V_C, These features make the Gilbert cell particularly suitable for VSPS [58]. Additionally, the complementary operation of the two top differential pairs ensures that the C_{IN} and R_O remain constant regardless of the control voltage V_C. This invariance is advantageous in maintaining predictable phase and gain responses in subsequent signal processing stages. However, despite its

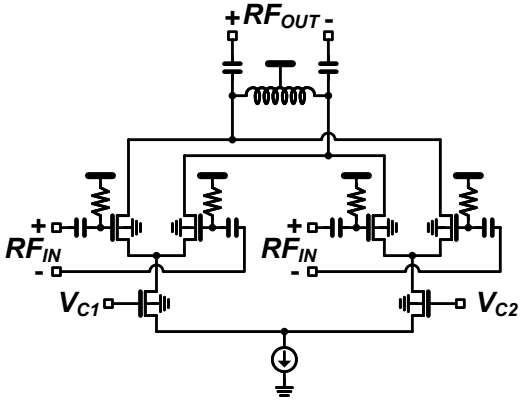


Figure 2.29: Schematic of Gilbert cell VGA.

excellent performance, the Gilbert cell consumes significant voltage headroom due to its cascode structure. In modern CMOS technologies, where the supply voltage is often limited to approximately 1V, the available headroom becomes insufficient for the proper operation of the Gilbert cell. As a result, Gilbert-cell-based VGAs are less commonly used in millimeter-wave CMOS systems, where low-voltage operation is critical.

Alternative solutions exist for realizing VGAs with invariant input capacitance C_{IN}. Fig. 2.30(a) shows a differential VGA with tunable output resistance [18, 67]. However, the low-pass resistive drain structure of this VGA makes it unsuitable for high-frequency operation, particularly in the millimeter-wave band. As a result, this type of VGA is typically used at lower intermediate frequencies or in baseband applications. In contrast, the current-steering VGA depicted in Fig. 2.30(b) incorporates a bandpass output network, making it well-suited for high-frequency operation. This design features a common-source input transistor, where the drain current is dynamically steered between the load and a bypass path controlled by the control voltage V_C [72–74]. By varying V_C, the effective resistance in the signal path is adjusted, thereby tuning the output amplitude. While this architecture is advantageous for low-voltage applications due to its simplicity and efficiency, it compromises with a narrower gain tuning range. However, in both VGA types, the variable output resistance R_O can affect subsequent stages that are sensitive to source impedance. This limitation makes them less suitable for applications requiring high precision or accuracy. Despite their benefits the variable output resistance R_O of both VGA types can adversely impact subsequent stages sensitive to source impedance. This drawback restricts their suitability for applications requiring high precision or accuracy.

For voltage-controlled VGAs, additional DACs are required, and some common con-

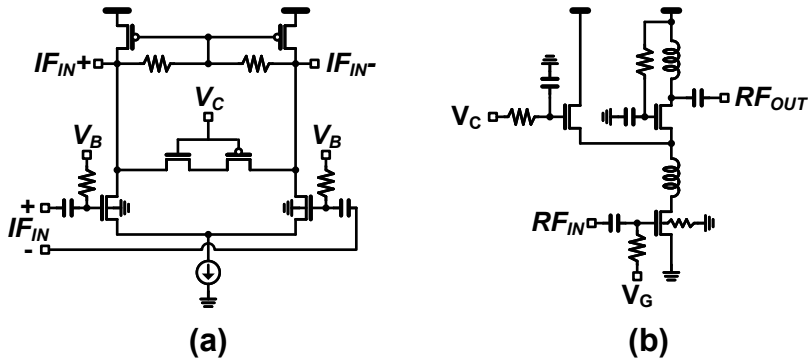


Figure 2.30: Schematics of two input impedance invariant VGAs: (a) VGA with tunable output impedance; (b) Current-steering VGA.

trol algorithms such as achieving linear-dB control become increasingly complex [53, 75, 76]. To better accommodate modern mixed-signal systems and facilitate advanced control logic, digital-controlled VGAs are commonly used in large-scale phased-array receivers. Fig. 2.31(a) illustrates a digital VGA composed of an array of g_m-cell units. Each unit is controlled by turning the tail transistor of a differential pair on or off, allowing precise gain adjustment through digital control. Similarly, the current-steering VGA can also be implemented as a digital-controlled VGA, as shown in Fig. 2.31(b). In this design, the current is not steered between the load and bypass path using an analog control voltage. Instead, both the load and bypass paths are divided into multiple unit arrays, and current is fully switched between the two paths in each unit based on digital control codes. To enhance area efficiency and reduce digital overhead, the units in digital-controlled VGAs are typically sized in binary-weighted configurations.

The digital controlling also allowing easier compensation to the variant C_{IN} and R_O. Fig. 2.32 shows a fully-compensated version of g_m-cell based digital VGA in Fig. 2.31(a) [15]. Another replica g_m-cell array but controlled by inverse controlled code is added to maintain a constant C_{IN}. Similary, a cross-coupled differential pair units array is added to output node to compensated the R_O variation due to the on-off of the g_m-cell array. While the C_{IN} and R_O variation is fully compensated, the circuit becomes bulky and power wasted. Also, the increasing parasitic introduced by the compensation units increase the loss and limit the operating frequency.

A more power- and area-efficient phase-invariant VGA solution with constant C_{IN} and R_O is illustrated in Fig. 2.33. In this design, the current from the input differential pair flows through an array of polarity selector units with predefined weight ratios, and the

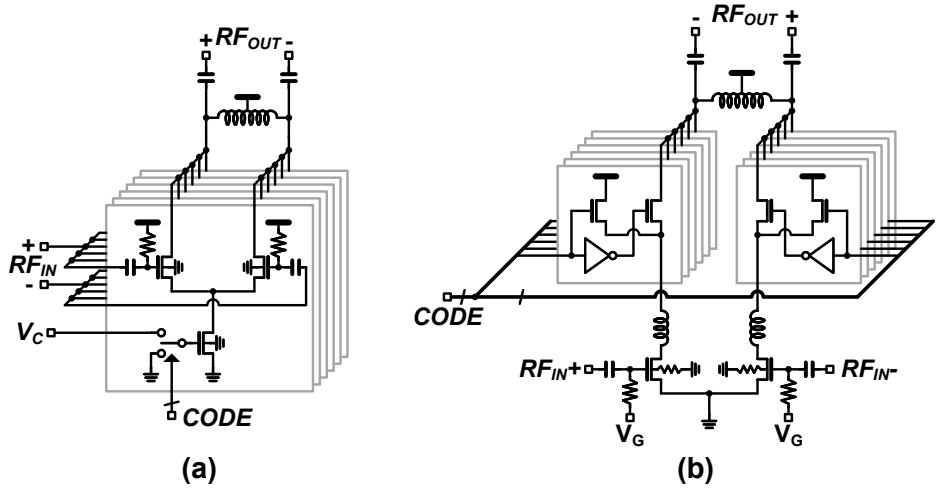


Figure 2.31: (a) VGA with switchable g_m-cell array. (b) Digital controlled pseudo-differential current steering VGA

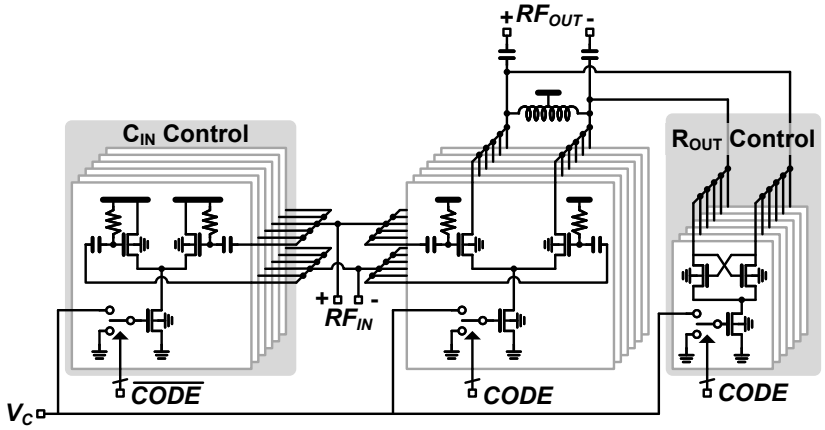


Figure 2.32: Schematic of phase-invariant VGA with Gm-cell units array.

signals are then combined at the output node. Gain adjustment is achieved by controlling the polarity of each unit in the array, enabling superposition and cancellation of signals from different units. The polarity selector units maintain a constant output impedance, effectively minimizing phase and gain variations across the tuning range [3, 55–57, 77, 78]. The design ensures that the overall DC current through the input differential pair remains constant, which also stabilizes the input capacitance C_{IN}. Although this operation reduces

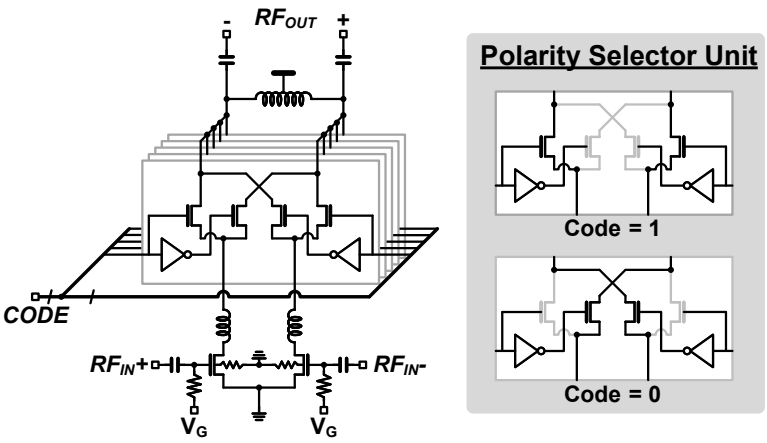


Figure 2.33: Schematic of phase-invariant VGA with polarity selector units array.

the gain tuning range by half, it introduces the capability to invert the output gain by 180°, making it particularly advantageous for applications requiring polarity selection and consistent performance. Unlike conventional digital current-steering VGAs, this solution maintains the same compactness while eliminating the issues of C_{IN} and R_O variation and the associated linearity degradation, ensuring superior reliability and precision.

2.4.2 Variable Attenuators

For RF receivers operating within a large dynamic range, attenuators are essential components to reduce the amplitude of strong signals while maintaining signal integrity. Unlike VGAs, attenuators based on passive networks do not suffer from linearity issues and maintain a wider operating bandwidth. Additionally, their symmetric design offers the ability of bidirectional operation. The three main types of passive attenuators are T-type, π-type, and Bridge-T-type, each with unique configurations and characteristics [79–81].

As shown in Fig. 2.34(a), the T-type attenuator consists of two series resistors R_S and one shunt resistor R_P, forming a "T"-shape structure. To achieve a desired attenuation A while maintaining the characteristic impedance Z_0, the corresponding resistor values are calculated as:

$$R_S = Z_0 \left[\frac{10^{\frac{A_{dB}}{20}} - 1}{10^{\frac{A_{dB}}{20}} + 1} \right]; \quad R_P = 2Z_0 \left[\frac{10^{\frac{A_{dB}}{20}}}{10^{\frac{A_{dB}}{10}} - 1} \right] \tag{2.25}$$

The T-type attenuator is simple and suitable for small attenuation values. However, its two series resistors introduce parasitics, limiting its high-frequency performance, espe-

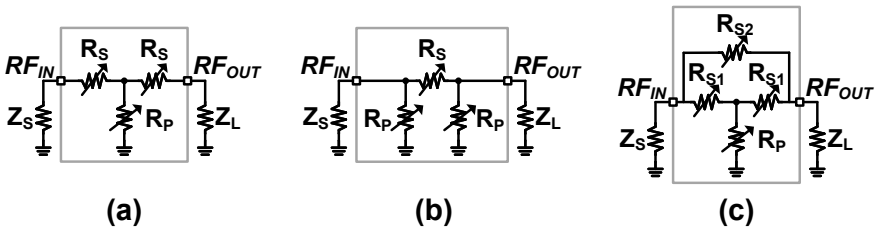


Figure 2.34: Schematic of basic (a) T-type attenuator, (b) π-type attenuator and (c) bridge-T-type attenuator.

cially at millimeter-wave frequencies. Additionally, impedance matching becomes sensitive to resistor variations, making it challenging to ensure accuracy under PVT variation, particularly for large attenuation values [81–84].

The π-type attenuator, shown in Fig. 2.34(b), consists of one series resistor R_S and two shunt resistors R_P, forming a "π"-structure. The resistor values for achieving a desired attenuation A with a characteristic impedance Z_0 are given by:

$$R_P = Z_0 \left[\frac{10^{\frac{A_{dB}}{20}} + 1}{10^{\frac{A_{dB}}{20}} - 1} \right]; \quad R_S = \frac{Z_0}{2} \left[10^{\frac{A_{dB}}{20}} - \frac{1}{10^{\frac{A_{dB}}{20}}} \right] \tag{2.26}$$

Compared to the T-type attenuator, the π-type attenuator offers better performance at higher frequencies and improved impedance matching, especially for larger attenuation values. However, the two shunt resistors result in greater DC power dissipation for the same attenuation level. Additionally, parasitic capacitance from the shunt resistors can impact attenuation accuracy and phase response [81, 83, 85, 86].

The Bridge-T-type attenuator, shown in Fig. 2.34(c), consists of two series resistors R_{S1}, one shunt resistor R_P, and an additional bridging resistor R_{S2} connecting the input and output ports, forming a symmetric bridge configuration. The resistor values for a desired attenuation A with a characteristic impedance Z_0 are:

$$R_{S1} = Z_0; \quad R_{S2} = Z_0 \left[10^{\frac{A_{dB}}{20}} - 1 \right]; \quad R_P = Z_0 \left[\frac{1}{10^{\frac{A_{dB}}{20}} - 1} \right] \tag{2.27}$$

The Bridge-T attenuator offers a wide attenuation range, which can be achieved through straightforward resistor adjustments. Its symmetrical structure ensures superior impedance matching between the input and output ports compared to T-type and π-type attenuators. Additionally, it exhibits reduced sensitivity to parasitic effects at high frequencies and delivers a more stable phase response, making it ideal for phase-sensitive applications such

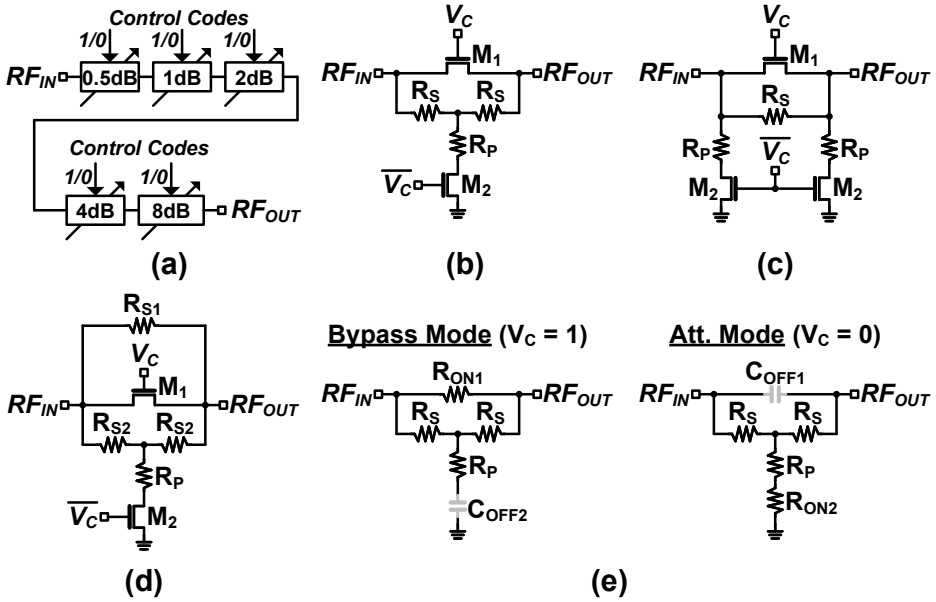


Figure 2.35: (a) A 5-bit digital attenuator with 0.5-dB resolution. (b) Digital attenuator units realization of T-type attenuator, (c) π-type attenuator and (d) bridge-T-type attenuator. (d) Bypass-mode and attenuation-mode equivalent circuit of T-type attenuator unit.

as phased-array systems [80, 85–88]. However, its increased complexity necessitates precise control over resistor values to ensure accurate attenuation and impedance matching. This sensitivity to PVT variations poses significant challenges in practical implementations. [84, 86]

In CMOS technology, particularly at higher frequencies, realizing tunable resistors can be challenging. When gate-voltage-controlled transistors are used as variable resistors, it is difficult to design an algorithm that reliably generates the appropriate control voltage to achieve the desired values for R_S and R_P across various attenuation levels. As a result, switching-type attenuators are widely adopted in RF receiver designs. Fig. 2.35(a) illustrates a typical 5-bit digital attenuator composed of binary-weighted attenuation units. Circuit implementations of switching-type T-type, π-type, and bridge-T attenuators are shown in Fig. 2.35(b)-(d). The operation principle is explained using the T-type unit in Fig. 2.35(e) as an example. In bypass mode, the signal flows through the turned-on transistor M_1. In attenuation mode, transistor M_1 is turned off, while transistor M_2 is turned on, forming the T-shaped topology. The attenuation step is defined by the values of R_S and R_P, while proper sizing of transistors M_1 and M_2 ensures that impedance and phase variations are minimized. However, in all three attenuator topologies, the transis-

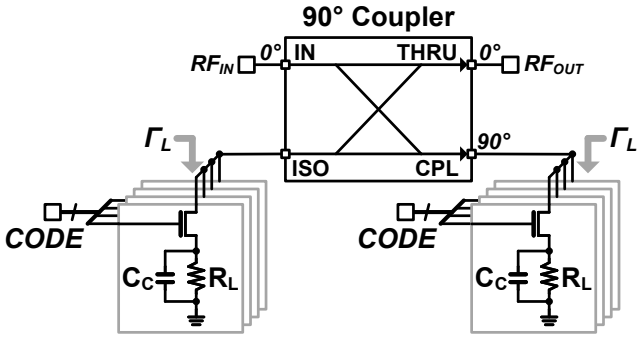


Figure 2.36: Schematic of 90° coupler-based fine-tuning attenuator.

tors introduce insertion loss, increasing the bypass mode loss and limiting the minimum achievable resolution of the digital attenuator. This makes it challenging to implement sub-degree tuning steps.

To address this limitation, a fine-tuning stage is often cascaded with the coarse attenuation units in a digital attenuator. Fig. 2.36 introduces a solution using a 90° coupler-based attenuator [84]. By adjusting the load impedance, the gain response of this circuit is expressed as:

$$S_{21,\text{att}} = \Gamma = \frac{R_L + Z_0}{R_L - Z_0} \tag{2.28}$$

Here, R_L is the load resistor in the unit, which can be implemented using either a voltage-controlled transistor or a switching resistor array. Since R_L can be tuned in very small steps, this solution achieves a high phase resolution, making it ideal for fine-grain attenuation control.

2.5 Summary

In this chapter, the fundamentals of millimeter-wave phased-array receivers and identifies the key challenges in their design are reviewed. By thoroughly examining the fundamental building blocks and architectures, the chapter lays the groundwork for devising precise solutions to meet the requirements of this thesis. The trade-offs inherent in various beamforming architectures are carefully analyzed to identify the most optimized approach for the research objectives. Additionally, as critical components of phased arrays, phase shifters and gain control units are evaluated in detail, with their respective advantages

and limitations summarized. The chapter concludes by highlighting the importance of compact, low-power designs to address the stringent demands of next generation wireless communication systems. These foundational analyses and insights serve as a guide for the subsequent development of advanced phased-array receiver designs throughout the thesis.

Chapter 3

Power-Efficient Millimeter-Wave Multi-Band Phased-Array Receiver

As discussed in Chapter 1, multi-band compatibility is essential for user devices to support global applications and cross-standard communication. To further enhance data rates and channel capacity, next-generation communication standards are continuously scaling toward higher frequencies. For example, Fig. 3.1 illustrates the frequency allocations for current 5G NR band allocation [89]. While the 28 GHz, 39 GHz, and 47 GHz bands have already been standardized for 5G, the growing demand for additional spectrum and higher channel capacity has brought the unlicensed 60 GHz band under consideration for the next phase of 5G communication standards. Although several narrowband millimeter-wave phased-array systems with competitive receiver performance have been published in recent years [2, 9–14, 16, 20, 35, 90–92], these designs cannot be directly extended to multi-band operation without relying on multiple IC solutions. To enable compact, low-cost user devices, several recent studies have demonstrated multi-band phased-array receivers capable of supporting multiple 5G NR FR2 bands with minimized system dimensions [18, 37, 67, 93–97]. However, these solutions suffer from high power consumption, which limits their practicality for portable devices. Furthermore, their operating frequency ranges remain constrained and are challenging to scale to higher frequency bands required by future communication standards. Multi-band operation also exposes receivers to more cluttered and rapidly changing electromagnetic (EM) environments. While enabling communication across multiple bands, current designs often experience significant performance degradation due to inter-band interference. Thus, next-generation receivers must adopt power-efficient and wideband architectures with sufficient rejection of inter-band blockers to ensure robust performance in complex EM environments.

To meet the demands of next-generation receivers, this thesis presents a power-efficient

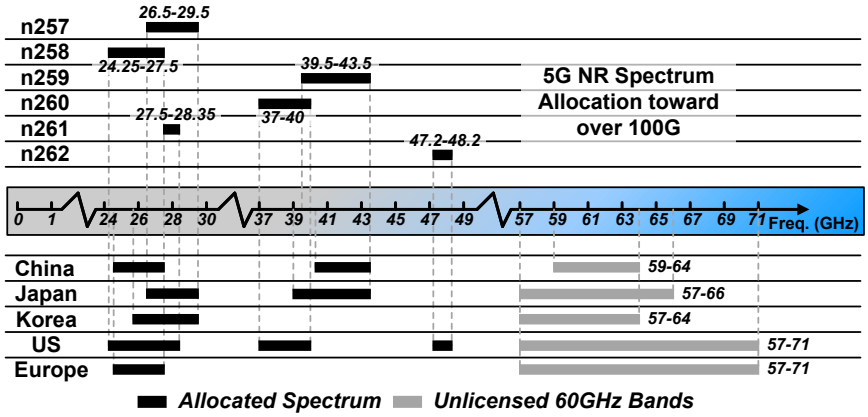


Figure 3.1: Latest 5G NR FR2 bands and global licensed/potential spectrum allocation for now and future.

multi-band receiver architecture implemented in CMOS technology. The proposed architecture addresses the limitations of conventional designs while ensuring compatibility with evolving communication standards. This chapter is organized as follows: Section 3.1 provides an overview of conventional multi-band phased-array receivers, highlighting their limitations and the challenges they face in meeting next-generation requirements. Section 3.2 introduces the proposed harmonic-selection technique, explaining its principles and advantages in enabling efficient multi-band operation. Section 3.3 outlines the system-level considerations for the proposed multi-band phased-array receiver, detailing how the architecture achieves improved performance and scalability. The circuit-level implementations is introduced in Section 3.4, providing a thorough explanation of the key components and design choices. Section 3.5 presents the measurement results. Finally, Section 3.7 concludes the chapter by summarizing the key findings and discussing potential directions for further optimization and improvement.

3.1 Conventional Multi-Band Receiver Architecture

Several previous research try to realize the multiband reception in different way. As shown in Fig. 3.2(a), conventional multi-band receiver based on the superheterodyne architecture achieves multi-band operation with wide-band signal path design [96, 97]. With relative high IF frequency, the images can be removed from the pass-band of the LNA. However, the operating bandwidth of the LO path will be proportional to the RF bandwidth. When the RF frequency coverage scales to 24-71GHz in order to support all 5G NR band, the LO fractional bandwidth achieves even 150% . The power consumption of both RF and

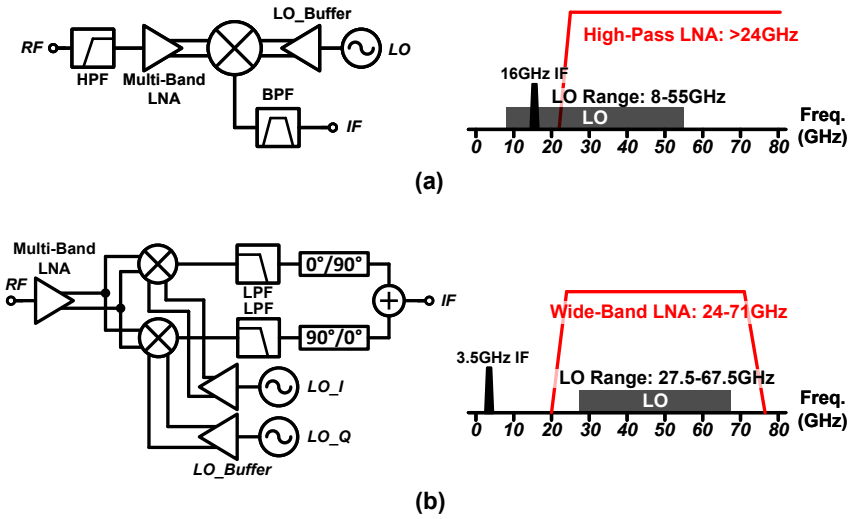


Figure 3.2: (a) Conventional multi-band receiver with wide-band path design. (b) Conventional multi-band receiver with Hartley architecture.

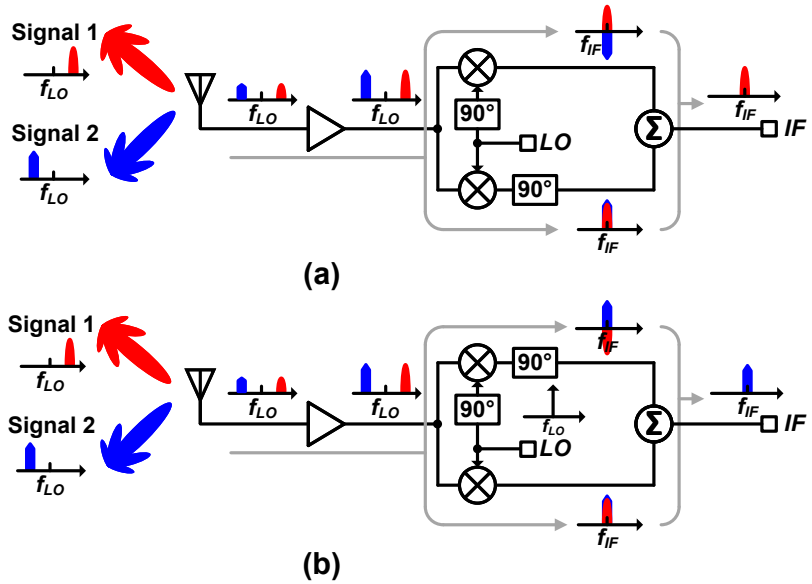


Figure 3.3: (a) Hartley receiver configured to select upper side band. (b) Hartley receiver configured to select lower side band.

LO will become incredibly large to guarantee the required conversion gain (CG). Moreover, the image frequency will also be inevitably overlapped with the pass-band of LNA even a high IF frequency is used. To tackle with this issue, Hartley architecture is adopted to provide additional full-band image rejection in multi-band receivers [67, 94], as shown

in Fig. 3.2(b). This design uses a quadrature LO and phase shifters to separate the desired signal from its image. This is caused by the inverse phase rotation for signal and image during phase shifting. Fig. 3.3 (a) shows how the Hartley receiver isolates upper side signal 1 (f_{LO}+f_{IF}) while suppressing lower side signal 2 (f_{LO}-f_{IF}), and Fig. 3.3 (b) demonstrates the reverse operation with a modified phase shifting configuration. Besides the improved image rejection, reconfigurable Hartley receiver with selectable side-band actually can reduce the LO frequency range [67], with the effect depending on IF frequency setting. However, a single multi-band LNA is still utilized in RF path to provide wide-band signal amplifying in Hartley receiver. The noise figure (NF) still degrade by around 3dB since the images are still located in the pass-band of the LNA.

Several prior studies have proposed various approaches for achieving multiband reception. As depicted in Fig. 3.2(a), the conventional multiband receiver, based on the superheterodyne architecture, utilizes a wideband signal path to enable multiband operation [96, 97]. By adopting a relatively high IF, this design effectively eliminates image frequencies from the LNA passband. However, the operating bandwidth of the LO path must scale proportionally with the RF bandwidth. To support 5G NR bands ranging from 24GHz to 71GHz, the LO fractional bandwidth reaches approximately 150%, resulting in significantly increased power consumption for both RF and LO paths to maintain the required conversion gain (CG). Additionally, even with a high IF frequency, the image frequency still overlaps a lot with the LNA passband.

To address these challenges, the Hartley architecture offers a promising solution by enabling full-band image rejection in multiband receivers, as shown in Fig. 3.2(b) [67, 94]. This architecture leverages a quadrature LO and phase shifters to distinguish the desired signal from its image through inverse phase rotation. Fig. 3.3(a) illustrates how the Hartley receiver isolates the upper sideband signal ($f_{LO} + f_{IF}$) while suppressing the lower sideband signal ($f_{LO} - f_{IF}$). Conversely, Fig. 3.3(b) demonstrates the reverse operation using a modified phase-shifting configuration. While reconfigurable Hartley receivers enhance image rejection and reduce LO frequency range requirements [67], their effectiveness depends on the IF frequency setting. However, a single multiband LNA is still employed in the RF path, amplifying wideband signals. Consequently, the noise figure (NF) degrades by approximately 3dB because the images remain within the LNA passband.

The wideband design illustrated in Fig. 3.2 is inherently not power-efficiency, particularly in multiband communication scenarios where the utilized bands distribute discretely and occupy only a small fraction of the spectrum. This inefficiency is explained in Fig. 3.4. Generally, the DC power consumption of the LO and RF paths, including bandpass amplifiers and buffers, scales with their bandwidth. For instance, although a bandwidth

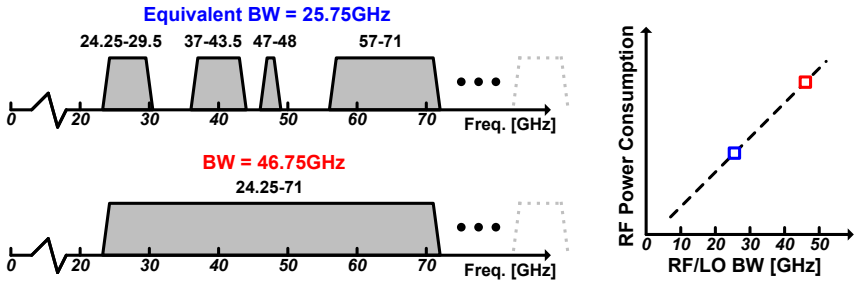


Figure 3.4: Power efficiency of multi-band receiver

of 24–71 GHz is necessary to consist all allocated and potential 5G NR bands, the actual equivalent bandwidth of these bands totals only 25.75 GHz. Nevertheless, a wideband design requires a 46.75 GHz bandwidth for both RF and LO paths, leading to substantially higher power consumption. Furthermore, extending a wideband design is challenging and often necessitates redesigning matching networks, along with further reduces power efficiency. This issue becomes worse at higher frequencies, where the bands are more spread out. Another issue for the wide-band signal chain is that it have to expose to the inter-band blocker without any rejection, unless employs tunable high quality out-of-chip band pass filter (BPF). A better solution is to use circuits that can select specific bands with narrower bandwidths. This approach improves power efficiency and makes it easier to adapt to future bands for next generation receivers. Also, adjustable narrow band design naturally have inter-band rejection.

3.2 Harmonic-Selection Technique

Current CMOS receivers exploit SAW filters as BPF to sufficiently attenuate large out-of-band blockers to prevent SNR degradation due to increase in noise and distortion. However, this kind of high-Q passive BPF at high frequency is impossible to be integrated with CMOS technology and has to be placed outside of the chip. To cover multiple bands across various standard, multiple SAW filters should be utilized which clearly increases cost and form factor. Therefore, it is desirable to have an integrated BPF with high selectivity and tunable center frequency for multi-band application. To address these requirement and prepare for the next generation receivers, a novel harmonic-selection technique is proposed in this thesis, which not only provide band selectivity with high inter-band rejection, but also can be scaled to support more bands at higher frequency.

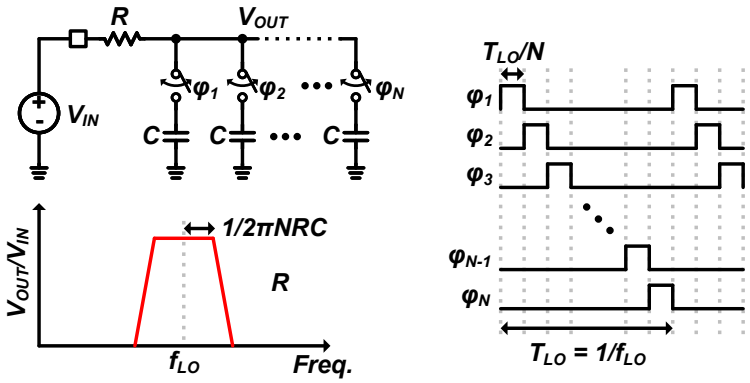


Figure 3.5: Conventional N-path filter.

3.2.1 Conventional N-Path Filter

To achieve high-selectivity bandpass filtering at high RF frequencies, the concept of modulation-based bandpass filtering was first introduced in the 1940s and 1950s [98**?**]. This technique shifts input signals to a desired low-frequency range using a mixer, followed by low-pass filtering to isolate the desired band. This architecture provided high selectivity and tunability while being compatible with CMOS processes, marking a significant breakthrough in RF design. Over time, the topology was simplified and evolved, replacing the mixer with multiple parallel time-modulated paths. This led to the development of the N-path filter, which emerged alongside advancements in CMOS technology. N-path filters provide reconfigurable bandpass filtering for RF and microwave frequencies. The operation principle of a conventional N-path filter is illustrated in Fig. 3.5. The core concept involves time-domain switching between multiple signal paths (the "N paths") that cyclically sample the input signal. This switching operation generates a bandpass response centered at a frequency f_{LO}, determined by the switching clock, with a bandwidth of $1/2\pi NRC$. This configuration enables precise frequency control through simple digital tuning.

Despite their advantages, N-path filters face significant challenges at millimeter-wave frequencies. The inherent parasitic effects of CMOS switches limit the achievable switching speeds, making square-wave modulation impractical at such high frequencies. Additionally, the switches introduce increased signal loss, further degrading performance. Nonetheless, N-path filters remain highly effective for tunable RF front-ends in sub-6 GHz applications, offering a compelling solution for reconfigurable filtering in this frequency range.

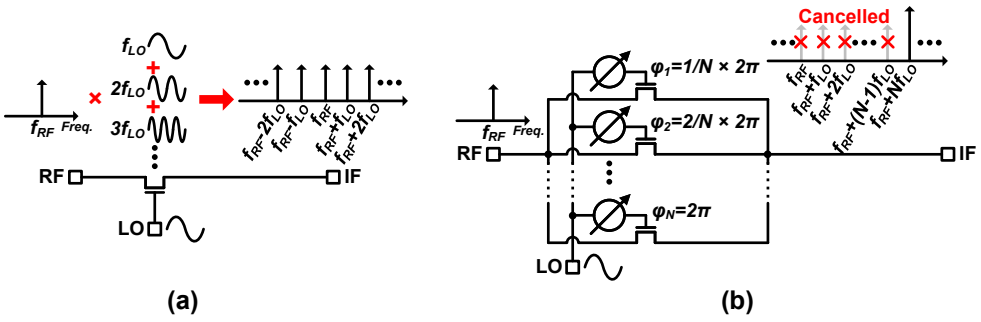


Figure 3.6: (a) Model of conventional transistor-based mixer. (b) Model of proposed harmonic-selection mixer.

3.2.2 Operation Principles of Proposed Harmonic-Selection Technique

The proposed harmonic-selection technique builds upon the principles of conventional N-path filtering, utilizing multi-path cancellation to achieve selectivity. Unlike traditional N-path filters, which operate at microwave frequencies with square-wave-driven switches, this approach is designed to function effectively at millimeter-wave frequencies by employing multi-path mixers driven by sinusoidal waveforms. This modification overcomes the limitations of conventional N-path filtering at higher frequencies. Fig. 3.6 (a) shows a basic transistor-based mixer. Due to the inherent nonlinearity of the mixing process, an RF signal applied to the transistor multipliers not only with the fundamental LO signal but also with higher-order harmonics of the LO, such as the 2^{nd}, 3^{rd} and beyond. Consequently, the down-converted IF signal contains many unnecessary mixing components. Actually, for conventional multi-band receiver with wide-band design, additional to the image, the high-order LO harmonic blockers may still within the RF operating frequency range, reducing the dynamic range. While LO harmonic interference is typically considered a limitation, it can be leveraged to enable band selectivity across a wide frequency range with low power consumption and high inter-band blocker rejection. To achieve this, A scalable harmonic-selection technique is introduced, depicted in Fig. 3.6(b). By applying a multi-phase LO to the mixer, the desired harmonic component can be selectively enhanced while suppressing others. Assume the receiver employs N mixing paths in the harmonic-selection receiver and they are driven by LO signals with N different phase. The resulting mixing components can be expressed by Eq. 3.1:

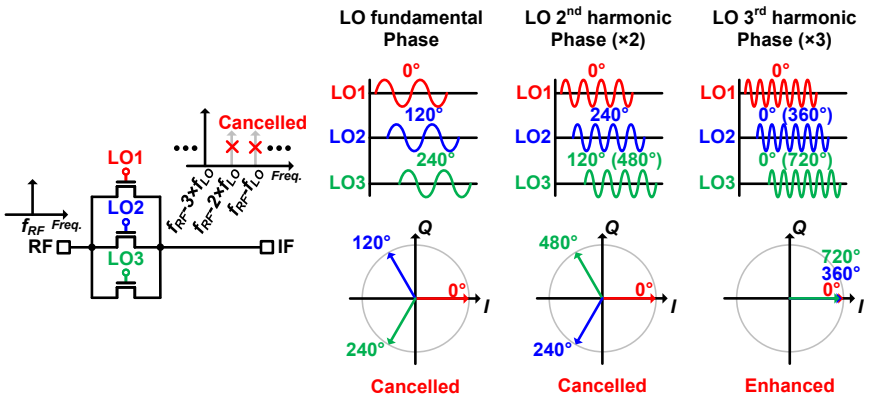


Figure 3.7: (a) Time-domain explanation when $N = 3$.

$$
\begin{aligned}
V_{\mathrm{IF}k\mathrm{th}} &= \frac{1}{2} A_{\mathrm{SIG}} A_{\mathrm{LO}} \sum_{i=1}^{N} \cos[(\omega_{\mathrm{RF}} \pm k\omega_{\mathrm{LO}}) + \frac{2ki\pi}{N}] \\
&= \frac{1}{2} A_{\mathrm{SIG}} A_{\mathrm{LO}} [\cos(\omega_{\mathrm{RF}} \pm k\omega_{\mathrm{LO}}) \sum_{i=1}^{N} \cos(\frac{2ki\pi}{N}) \\
&\quad - \sin(\omega_{\mathrm{RF}} \pm k\omega_{\mathrm{LO}}) \sum_{i=1}^{N} \sin(\frac{2ki\pi}{N})] \\
&= \begin{cases} 0, k < N \\ \frac{k}{2} A_{\mathrm{SIG}} A_{\mathrm{LO}} \cos(\omega_{\mathrm{RF}} \pm k\omega_{\mathrm{LO}}), k = N \end{cases}
\end{aligned}
\tag{3.1}
$$

Here, $V_{\mathrm{IF}k\mathrm{th}}$ represents the mixing component of the k-th LO harmonic. It can be found that only the N-th harmonic mixing component will be enhanced, while the other mixing components will be rejected by applying an N-phase LO with $2\pi/N$ phase interval. Fig. 3.7 shows an intuitive example of harmonic-selection mixer when $N = 3$ to explain the harmonic cancellation with LO time-domain waveform and phase map. With this feature, any mixing components generated by k-th (k<=N) order harmonic of the LO can be realized by applying an appropriate LO phase assignment to an k-path harmonic-selection mixer. This harmonic-selection technique effectively extends the receiver's operating frequency range without requiring a wideband LO, therefore minimize the power consumption. According to the equation, the harmonic-selection technique also provides rejections against the inter-band blockers generated by the unwanted harmonics. Collaborate with the LNA band-pass filtering and the Hartley receiver architecture, as shown in Fig. 3.8, the proposed technique can realize high inter-band blocker rejection with suppressed system NF and minimized power consumptions and can be easily scaled to support more

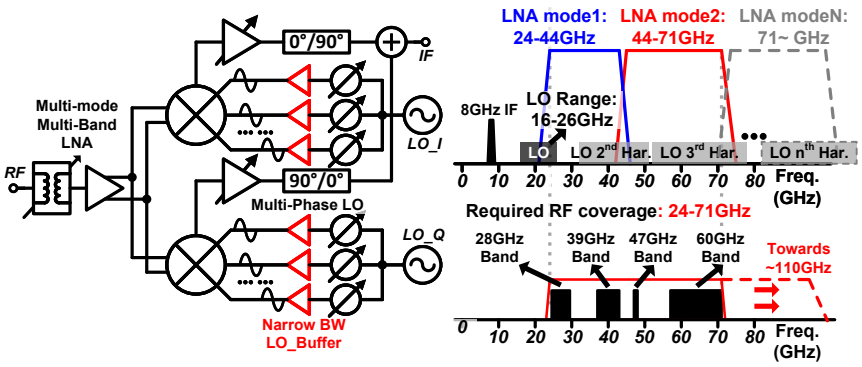


Figure 3.8: Power-efficient multi-band receiver architecture utilizing harmonic-selection technique.

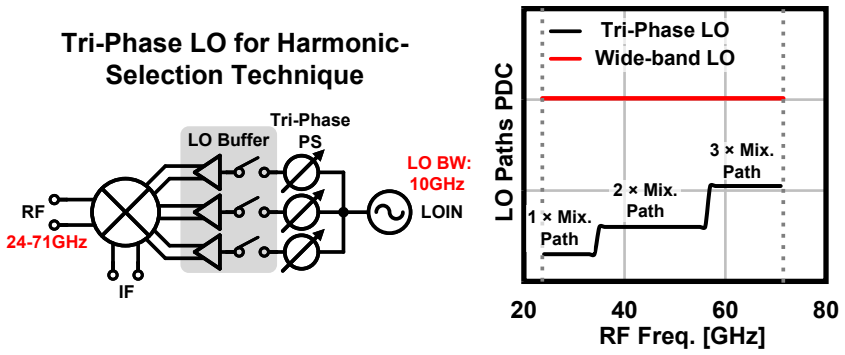


Figure 3.9: Power consumption of harmonic-selected mixer.

higher bands.

To achieve the required 24–71 GHz RF coverage for 5G NR, the proposed harmonic-selection technique utilizes only three mixing paths with a tri-phase LO assignment. This configuration reduces the required LO bandwidth to just 10 GHz, as shown in Fig. 3.9. While this approach significantly lowers the power consumption of each individual LO path, it does employ multiple LO paths for the down-conversion process. This might raise concerns about the overall power efficiency of using multiple LO paths. However, as derived in Eq. 3.1, the harmonic-selection mixer only activates k mixing paths to select the desired k-th harmonic mixing component. For example, as shown in Fig. 3.9, only one mixing path is active in the fundamental mode, and two paths are active in the second-harmonic mode. This selective activation ensures that lower power consumption is achieved at lower operating bands. In contrast, conventional wideband LO designs

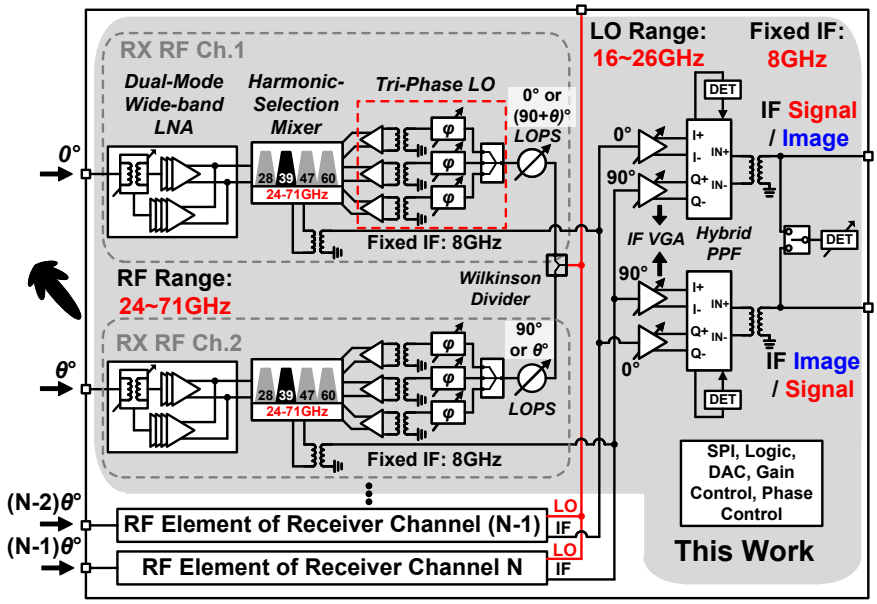


Figure 3.10: Block diagram of the proposed multi-band phased-array receiver with harmonic-selection technique.

consume a constant level of power regardless of the operating band. Although higher-order harmonic components are generally weaker due to the nonlinearity of the mixer, the proposed harmonic-selection technique compensates for this by leveraging multi-phase mixing paths. This results in a k-times CG for the k-th harmonic mixing component, as explained in Eq. 3.1, effectively mitigating the loss of higher-order harmonic mixing components. Consequently, the proposed approach achieves efficient RF coverage with minimized power consumption and maintains consistent performance across all operating bands.

3.3 System Considerations

3.3.1 Block Diagram

The block diagram of the proposed 24.25–71 GHz multi-band phased-array receiver, based on the harmonic-selection technique, is shown in Fig. 3.10. To meet the required RF frequency coverage, a tri-phase LO is employed to drive the mixer. With the proposed harmonic-selection technique, the LO frequency range is significantly reduced to 16–26 GHz. The IF frequency is fixed at 8 GHz, enhancing selectivity and minimizing interference from LO spurious signals and leakage. This narrowband IF design im-

proves tolerance to LO leakage, allowing the LO to be generated using a mature sub-6 GHz frequency synthesizer followed by a frequency multiplier [99–101]. The proposed receiver includes two channels on a single chip. Each channel comprises a dual-mode multi-band LNA, a harmonic-selection mixer driven by a tri-phase LO circuit, and an LO phase shifter. The LO phase-shifting architecture is used to enable precise beam steering across a wide frequency range [19, 20], with each channel supporting full 360° phase-shifting coverage. The dual-mode multi-band LNA is configurable to operate in either the 24–44 GHz or 44–71 GHz band, providing flexibility for different frequency ranges. The receiver also incorporates a configurable Hartley architecture for sideband selection and image rejection. While the phased-array system provides strong spatial selectivity, the Hartley architecture is specifically designed to handle cases where the desired and undesired signals arrive with identical phases. In this design, quadrature LO signals are generated by the LO phase shifters in the two receiver channels. Additionally, a hybrid-type poly-phase filter (PPF) is included in the IF stage to combine the received signals in quadrature. This integration ensures effective signal processing while maintaining the receiver's high performance across the full frequency range.

3.3.2 Frequency Plan

Based on the system implementation, the detailed frequency plan of the proof-of-concept harmonic-selection receiver is shown in Fig. 3.11. The receiver operates in four distinct modes, with frequency configurations of $F_{\mathrm{LO}} + F_{\mathrm{IF}}$, $2 \times F_{\mathrm{LO}} - F_{\mathrm{IF}}$, $2 \times F_{\mathrm{LO}} + F_{\mathrm{IF}}$, and $3 \times F_{\mathrm{LO}} - F_{\mathrm{IF}}$, corresponding to the 28 GHz, 39 GHz, 47 GHz, and 60 GHz bands, respectively. For the 28 GHz band operation, the harmonic-selection mixer is set to the fundamental-selected mode, and the LNA is configured to cover the 24–44 GHz range. In this mode, the Hartley architecture selects the upper sideband while rejecting the lower sideband. For the 39 GHz and 47 GHz band operations, the mixer operates in the 2^{nd}-harmonic-selected mode. Since the 39 GHz and 47 GHz bands are image frequencies of each other, the Hartley architecture distinguishes between them through its sideband selection capability. The LNA is set to the 24–44 GHz mode for the 39 GHz operation and to the 44–71 GHz mode for the 47 GHz operation, providing enough isolation to maximizes the IRR and minimizes the system NF. In the 60 GHz band operation, the harmonic-selection mixer operates in the 3^{rd}-harmonic-selected mode, and the LNA is configured to cover the 44–71 GHz range. The Hartley architecture selects the lower sideband in this mode. Across all four modes, the proposed receiver effectively selects the desired signal while rejecting unwanted inter-band blockers and image frequencies. This is achieved through the combined effects of the harmonic-selection technique, LNA

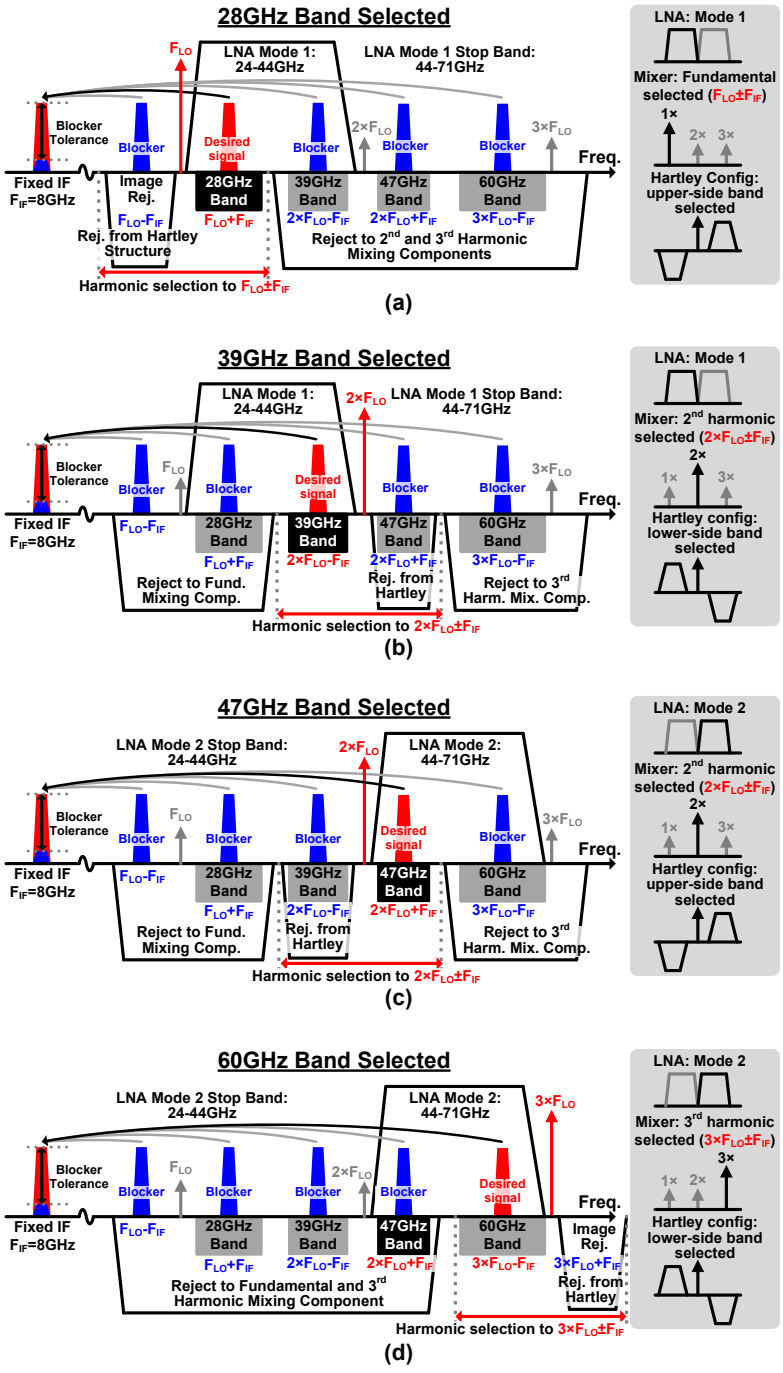


Figure 3.11: Frequency plan and inter-band blockers analysis of the proposed receiver on (a) 28GHz band mode, (b) 39GHz band mode, (c) 47GHz band mode, and (d) 60GHz band mode.

band-pass filtering, and the Hartley architecture.

In practical applications, non-idealities such as LO phase errors and phase offsets between desired and undesired signals may impact the performance of the Hartley or harmonic-selection operations. These effects will be analyzed in detail in the following section. However, the harmonic-selection technique, LNA band-pass filtering, and Hartley operation work synergistically to reject unwanted signals, ensuring robust receiver performance even in the presence of such mismatches.

3.4 Circuit Implementation

3.4.1 Harmonic-Selection Mixer and LO Paths

The proposed harmonic-selection technique significantly reduces the required LO frequency range while enabling efficient multi-band down-conversion. The operating principles of this technique for the fundamental-selected mode, 2^{nd} harmonic-selected mode and 3^{rd} harmonic-selected mode is explained in Fig. 3.12. The harmonic-selection mixer is driven by configurable tri-phase LO generation circuits and consists of three differential mixing paths. Each path is independently controlled by an LO signal with a specific phase assignment tailored to the desired mixing component. By applying LO signals with carefully assigned phases, the resulting mixing components in each path constructively enhance the desired harmonic while destructively canceling unwanted harmonics. Additionally, the mixer incorporates a differential-mode/common-mode selector based on a transformer at its output. Additional signal filtering and better matching can be therefore provided.

In the fundamental-selected mode, only two mixing paths are activated. The LO path to the closed mixing path is also turned down for saving power. The differential-mode output is selected in this mode and the proposed mixer now behaves as a conventional double-balanced mixer. The conversion gain of fundamental mixing component is enhanced by the double-balanced topology, while the unwanted 2^{nd} and 3^{rd} harmonic mixing components are rejected. The 2^{nd} harmonic-selected mode keeps the same LO phase assignment with the fundamental-selected mode. Nonetheless, the mixer output is switched to common-mode connection in this mode. Therefore, only the 2^{nd} harmonic mixing component is retained. The differential fundamental and 3^{rd} harmonic mixing components are cancelled. The balanced topology of fundamental- and 2^{nd} harmonic-selected modes can eliminate the LO leakage effectively. In the 3^{rd}-harmonic-selected mode, three mixing paths are fully activated and driven by tri-phase LOs with 120° phase difference. The fundamental and 2^{nd} mixing components are cancelled by the 120° interval tri-phase

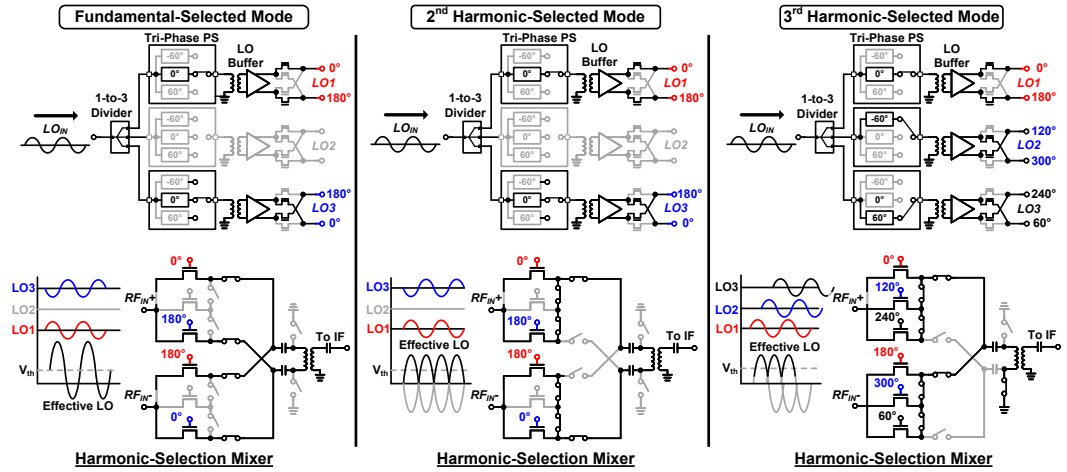


Figure 3.12: Operating principle of proposed harmonic-selection mixer with configurable tri-phase LO at each mode.

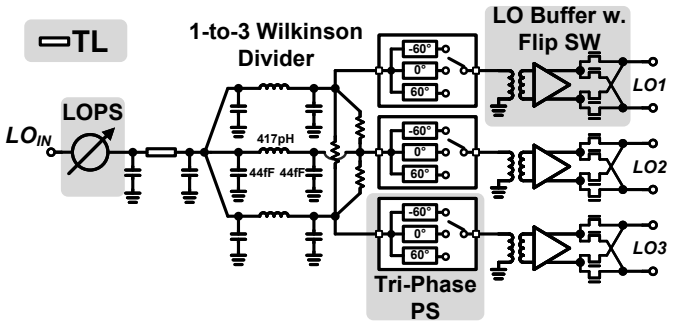


Figure 3.13: Block diagram of the tri-phase LO generation.

LO as analyzed in the previous section. The output connection of the mixer is switched to differential mode to further reject the common-mode 2nd harmonic mixing component. Therefore, the 3rd harmonic mixing component is finally preserved at the output.

In this work, the compact tri-phase LO generation is designed with low power consumption. The detailed circuit schematic of the LO is shown in Fig. 3.13. After the LO phase shifter for beamforming, the LO signal is divided into three paths by a compact 1-to-3 Wilkinson divider, which ensures isolations between each path. The bulky $\lambda/4$ wavelength transmission lines in Wilkinson divider are replaced by area-efficient *CLC* networks to significantly reduce the effective footprint [102, 103]. After that, a tri-phase phase shifter is employed in each path to realize the corresponding LO phase assignment for each harmonic-selection mode. As shown in Fig. 3.14(b), the proposed tri-phase

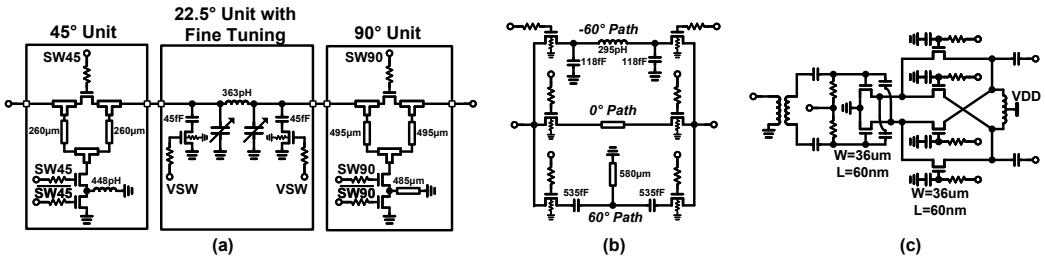


Figure 3.14: (a) Schematic of LO STPS, (b) tri-phase phase shifter, and (c) LO buffer with 180° flip switch.

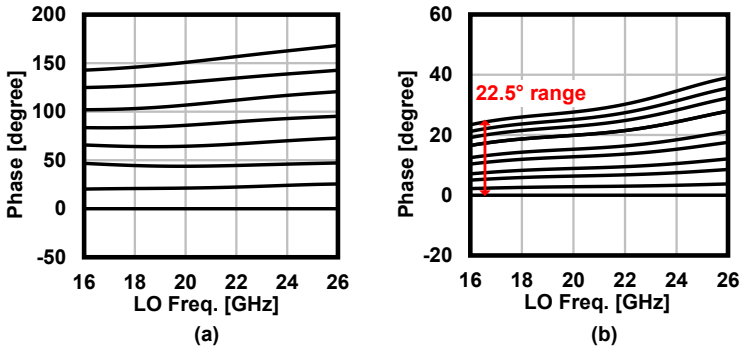


Figure 3.15: (a) Simulated relative phase response of the LO STPS. (b) Simulated relative phase coverage of the fine-tuning stage in LO STPS (tuned by 10-bit RDAC).

phase shifter consists of a -60° phase shifting path, a 60° phase shifting path, and a 0° through path. The -60° and 60° phase shifting are realized by a phase-lagging low-pass network and a phase-leading high-pass network, respectively, for a compact circuit area. A differential LO buffer with 180° phase-flipping function, as shown in Fig. 3.14(c), is inserted after the tri-phase phase shifter [104, 105]. Together with the tri-phase phase shifter, the phase assignment for all the operating mode could be generated with a minimized circuit overhead, as shown in Fig. 3.12. Transformer matching with capacitors are utilized in the LO buffers for broadening the operating bandwidth. Since the harmonic mixing is realized by the non-linearity of mixer rather than the harmonic distortion of LO buffer, the LO buffer consumes the same power on all operating modes, which is only around 7mW.

Fig. 3.14(a) shows the LO phase shifter for beamforming. With 4-bit phase resolution, the switching-type phase shifter (STPS) employed in this work consumes only 0.1mm^2 chip area, while achieving wide bandwidth and great linearity without additional power

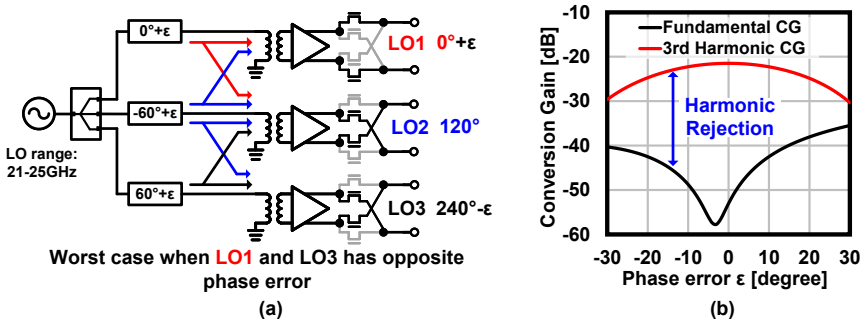


Figure 3.16: (a) LO paths with phase error on 3rd harmonic-selected mode. (b) Simulated mixer conversion gain and harmonic rejection degradation with LO error.

consumption. It consists of a 90° stage, a 45° stage and a 22.5° with fine-phase tuning. Along with the 180° phase-flipping function in the LO buffer, 360° phase coverage could be covered. The 45° and 90° stages in this work are designed with bridged-T architecture, which realize stable and precise phase shifting with small gain variation[41, 42, 106]. Nonetheless, the phase error is difficult to be eliminated in a wide LO frequency range. The simulated relative phase response of the STPS is shown in Fig. 3.15(a). The remaining phase error may cause LO I/Q mismatch and degrade the performance of Hartley receiver operation. Therefore, the 22.5° stage with CLC topology shown in Fig. 3.14(a) also plays the role of fine-tuning stage by employing varactors [43]. As shown in Fig. 3.15(b), the fine-tuning realizes at least 22.5° coverage, which is sufficient to compensate the LO phase error.

To evaluate the harmonic rejection performance of the proposed harmonic-selection mixer, a standalone test element group (TEG) consisting of only the harmonic-selection mixer and tri-phase LO generation circuitry was fabricated, as shown in Fig. 3.17. Measuring the entire receiver channel could lead to inaccurate harmonic rejection assessment, as contributions from the LNA and Hartley architecture may affect the results. Additionally, an IF VGA is integrated into the TEG with a bypass switch to facilitate evaluation.

In an actual circuit, the tri-phase LO may deviate from the desired phase due to the imperfect frequency characteristic of tri-phase LO generation and coupling between mixing paths. For fundamental- and 2nd harmonic-selected modes, mixing paths on two sides are selected to avoid coupling and keep circuit symmetrical. The phase error will only slightly degrade conversion gain (CG) with balanced mixer topology. This issue could be more obvious on 3rd harmonic-selected mode as shown in the Fig. 3.16(a). Nonetheless, the simulation result in a worst case in Fig. 3.16(b) shows that the harmonic-selection technique has a high tolerance to the phase error.

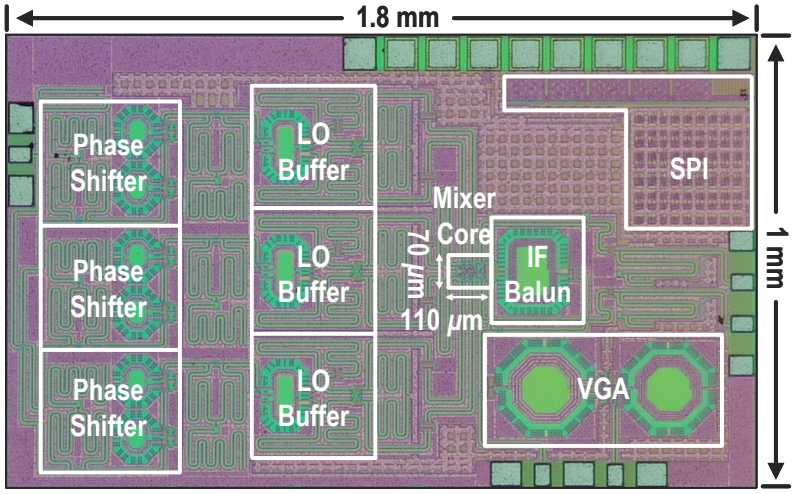


Figure 3.17: Chip micrograph of the TEG to validate the proposed harmonic-selection mixer.

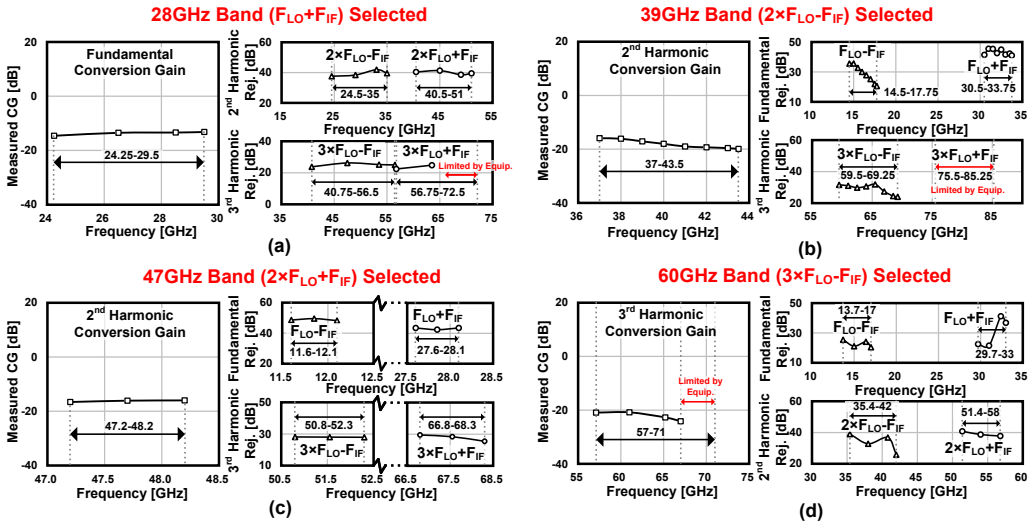


Figure 3.18: Measured CGs and harmonic rejections of the proposed mixer on (a) 28GHz band mode, (b) 39GHz band mode, (c) 47GHz band mode, and (d) 60GHz band mode.

The measured CG and harmonic rejections of the proposed harmonic-selection mixer along with the tri-phase LO are presented in Fig. 3.18. The IF frequency is fixed at 8GHz in this measurement. As shown in the figure, flat CG characteristic is obtained in all the harmonic-selection modes. More than 20-dB rejections to the undesired harmonic components are also achieved in each operating band by the proposed mixer. The conversion gain offset between each operating mode are less than 5dB, which can be compensated

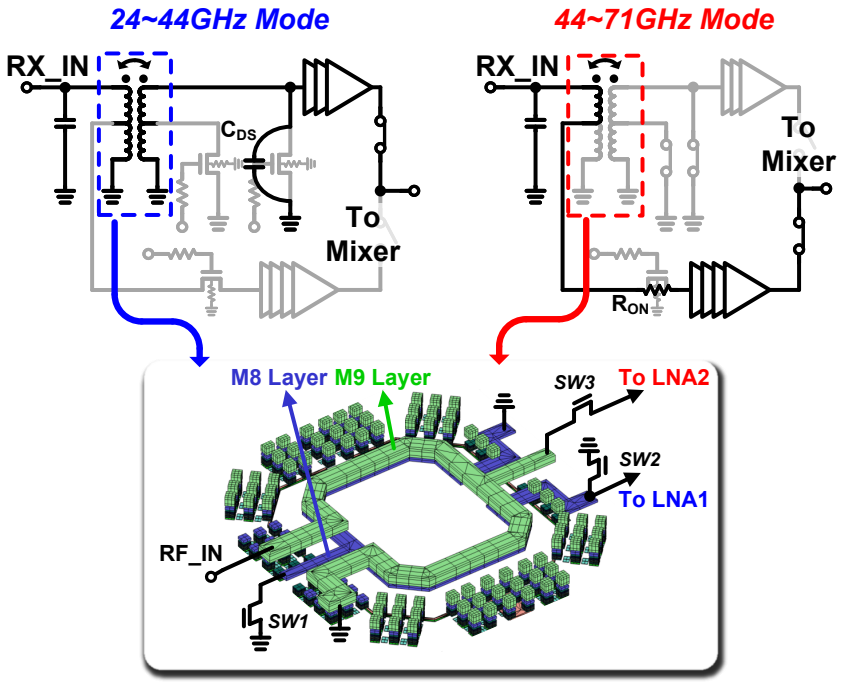


Figure 3.19: Operation explanation of dual-mode LNA at 24-44GHz mode and 44-71GHz mode with reconfigurable transformer.

by variable gain without causing a NF degradation. It should be noted that the rejections could be further improved by the LNA band-pass filtering and the Hartley receiver architecture.

3.4.2 Dual-Mode Multi-Band LNA

In recent years, although many attractive blocker rejection methods have been proposed, LNA is still the front line to undertake the impact from blockers. In conventional multi-band receivers, single LNA is designed with a wide-band frequency response to cover all the desired bands. The power consumption of the LNA will scale against the bandwidth for maintaining enough gain and linearity. The inter-band blocker rejection of such method is also limited due to the lack of band-pass filtering. In order to improve the power efficiency and inter-band blocker tolerance, a dual-mode multi-band LNA is proposed in this work as shown in Fig. 3.19. The proposed LNA consists of two LNA elements, which are the lower-band LNA covering 24-44GHz and the upper-band LNA covering 44-71GHz. The frequency coverage of the LNA elements is selected considering the system image rejection and the LNA circuit performance. With the help of the configurable

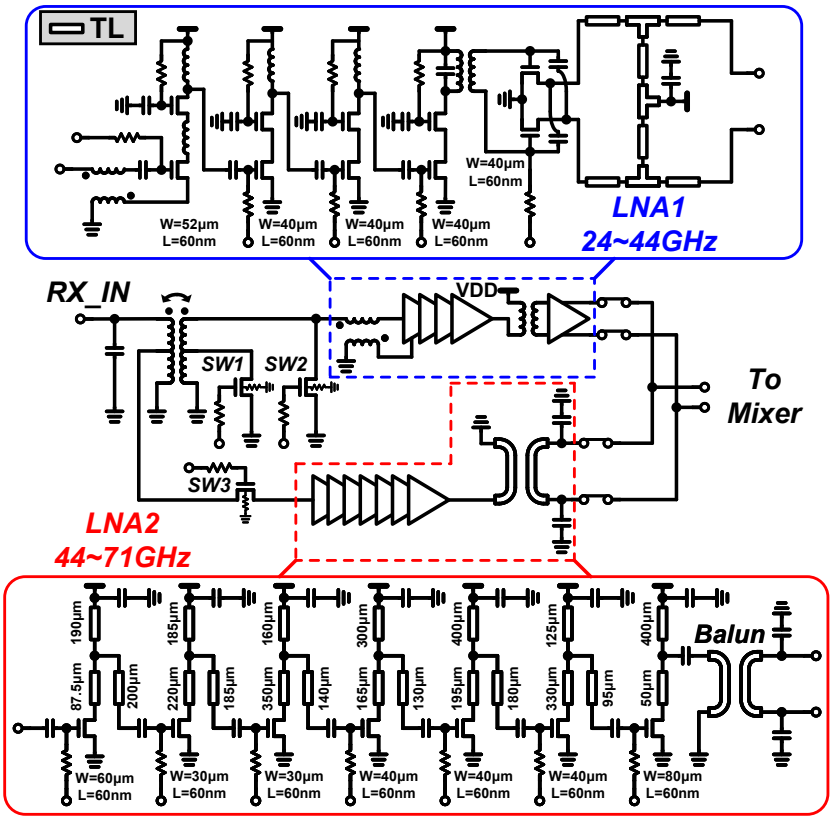


Figure 3.20: Block diagram of the proposed dual-mode wide-band LNA and its detailed core circuits.

matching network shared between two operating mode, the proposed dual-mode multi-band LNA structure takes a good balance between chip area and circuit performance. The band-pass filtering of the LNA also leads to high isolation between the fundamental and 3rd harmonic mixing components of the harmonic-selection mixer. The detailed compositions of the two LNA elements are also demonstrated in Fig. 3.20. The lower-band LNA employs four cascode stages to achieve high gain while maintaining a low NF [107]. The input stage is source degenerated with an inductor coupled and integrated with the input series inductor [108]. A compact footprint is realized with an improved matching and linearity. The upper-band LNA introduces seven common-source (CS) stages to ensure enough power gain. Transmission-line-based interstage matching is chosen to improve the area efficiency.

Typically, the required passive values for the matching is inversely proportional to the operating frequency. Based on this characteristic, a reconfigurable transformer is

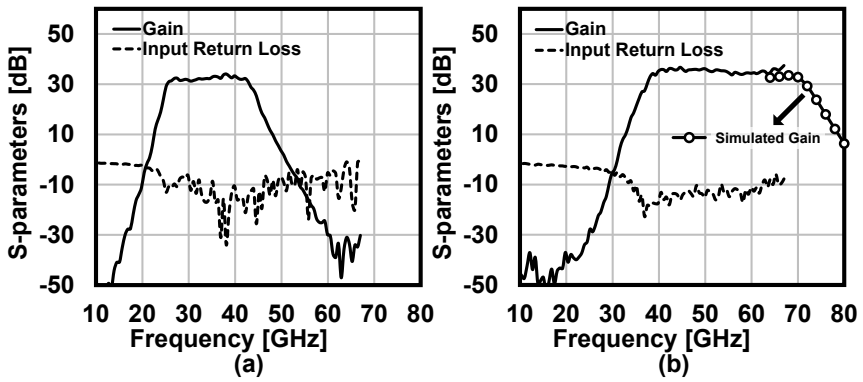


Figure 3.21: Measured frequency responses of a single proposed dual-mode multi-band LNA in (a) 24-44GHz mode and (b) 44-71GHz mode.

employed at the input to combine the two LNA elements. As shown in Fig. 3.19, the upper-band LNA is connected to the center tap of the primary coil. When the lower-band LNA is operating, the input transformer forms a high-order wide-band matching network with the C_{gs} from SW2 to cover 24-44GHz. During the operation of upper-band LNA, the secondary transformer coil will be grounded. The upper-band LNA will hence be matched with approximate half inductance value of the primary transformer coil. At the output side, the two LNA elements are combined with a single-pole-double-throw (SPDT) switch for better isolation.

A stand-alone dual-mode multi-band LNA is fabricated for on-wafer evaluation. The measured performance of the LNA in lower-band mode and upper-band mode are presented separately in Fig. 3.21. The -3dB bandwidth in lower-band and upper-band modes realize coverage of 24-44GHz and 44-71GHz, as expected. The measured gain of the proposed LNA in 24-44GHz mode and 44-71GHz mode are around 32dB and 35dB, respectively. During the measurement, The input return loss in both modes keep lower than -10dB in pass-band.

3.4.3 Hybrid-Type PPF with Self-Calibration

The IRR performance of multi-band receivers is essential due to their wide frequency coverage. The proposed receiver utilizes the Hartley receiver architecture to improve the image rejections. A 90°-shifted LO is used at adjacent channel, and -90° is again applied in IF PPF to realize the Hartley operation. The insertion loss (IL) of passive multi-stage PPFs increase significantly with more stages, which degrades the system conversion gain and NF. Therefore, a single-stage PPF is utilized in this work. Generally, the PPF topol-

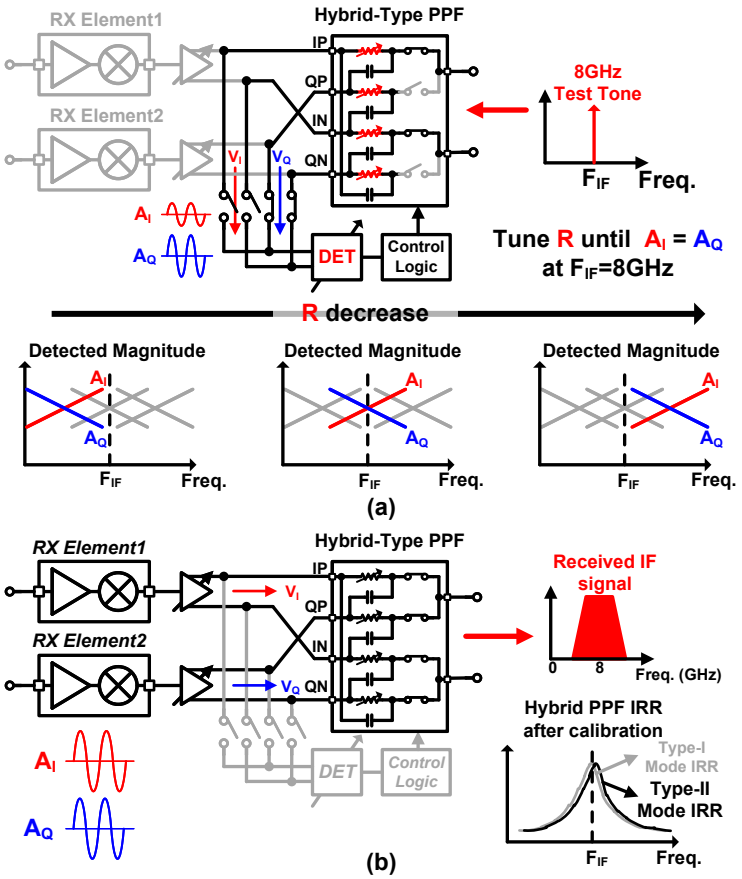


Figure 3.22: (a) Calibration of the hybrid-type PPF. (b) IF circuits configuration after IRR calibration at normal receiver operation.

ogy can be classified into type-I and type-II. As explained in Chapter 2, although both type exhibit a peak IRR at the pole frequency f_C, the IQ amplitude and phase relationship are reciprocal for these two type. Typically, Type-II PPF is preferred in conventional designs since its IL is 3-dB theoretically better than Type-I topology. However, regarding the IRR degradation caused by PVT variations, Type-II PPF generally requires complicated and bulky phase calibration [63, 93, 109]. The corresponding calibration accuracy is usually limited and the power consumption is usually high. On the contrary, the IRR of Type-I PPF can be easily calibrated by simple and high-accuracy magnitude detections. Therefore, this work introduces a hybrid-type PPF to achieve both accurate IRR calibration and low IL.

$$IRR_{\text{Type}-\text{I}} = IRR_{\text{Type}-\text{II}} = (\frac{f+f_C}{f-f_C})^2 \tag{3.2}$$

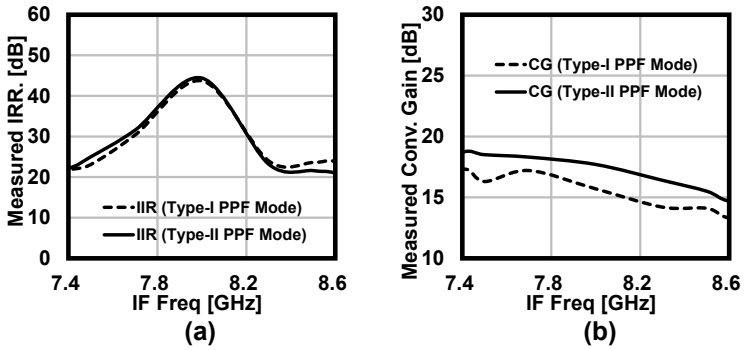


Figure 3.23: Measured system (a) IRR and (b) CG with the proposed hybrid-type PPF operating in type-I and type-II mode separately.

As explained in Eq. 3.2 [61, 62], Type-I and Type-II PPF have identical IRR with peak frequency located at $f_C = 1/2\pi RC$ when R and C values are the same. The hybrid-type PPF can be reconfigured between Type-I and Type-II topology while maintaining the same R and C values. The operation principle of the hybrid-type PPF is detailly explained in Fig. 3.22. The hybrid-type PPF will be first configured in Type-I mode for IRR calibration. An 8GHz test-tone signal is input from the IF output node, while the I and Q ports of the hybrid-type PPF are connected to a magnitude detector. The R value is tuned to calibrate the I/Q magnitude imbalance depending on the readout value of the detector. Since Type-I and Type-II PPFs share the same IRR peak frequency f_C, The proposed PPF will keep the calibrated R value and directly switches to Type-II mode. Lower IL during normal operation could be therefore achieved, as shown in Fig. 3.22(c). The f_C of the PPF is steered by tuning the R_{on} of a triode-region transistor. With the help of ADC, RDAC, and SPI interface integrated in the digital block, the hybrid PPF calibration can operate automatically. The measured IRRs of the proposed PPF in both Type-I mode and Type-II mode are shown in Fig. 3.23(a) after a calibration in Type-I mode. As demonstrated in the figure, the IRRs in Type-I and Type-II modes match with each other very well. As expected, Fig. 3.23(b) shows that the measured conversion gain achieves an 2-dB improvement with the proposed hybrid-type PPF operating in Type-II mode.

The proposed hybrid-type PPF is calibrated with an on-chip differential detector as shown in Fig. 3.24(a). The I/Q ports of the PPF shares one magnitude detector to avoid mismatch. The differential detector senses the input voltage by an input transconductance stage followed by a current rectifier. The rectified current is then amplified and filtered to generate a DC voltage $VOUT_{DC}$ [109]. Another detector is applied at the IF output node to

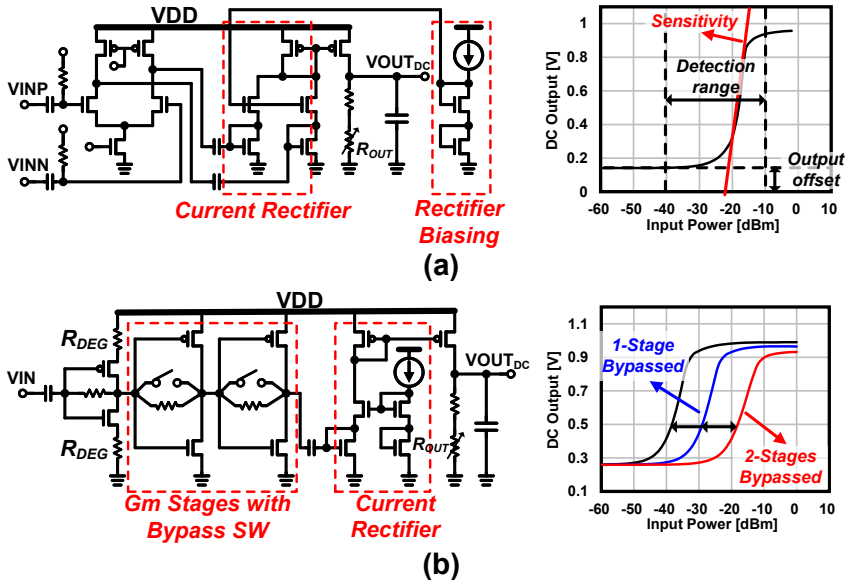


Figure 3.24: Schematic of (a) the proposed differential voltage detector for hybrid PPF calibration and (b) high-dynamic detector for IF power level detection.

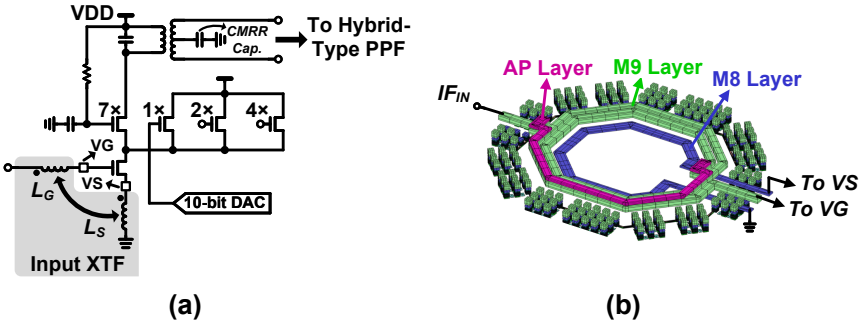


Figure 3.25: (a) Circuit schematic of the proposed 3-bit IF VGA. (b) The input XTF model of IF VGA.

indicate the output power of receiver, which is shown in Fig. 3.24(b). To extend the input dynamic range, multiple transconductance stages with bypass switches are introduced. Larger than 20-mV/dBm sensitivity can be achieved across 40-dB signal power range in the simulation.

An IF VGA is inserted between before PPF and mixer to provide variable gain and isolation. The detailed circuit of the proposed phase-invariant IF VGA is shown in Fig. 3.25(a). The IF VGA is designed based on the current-steering topology with 3-bit coarse

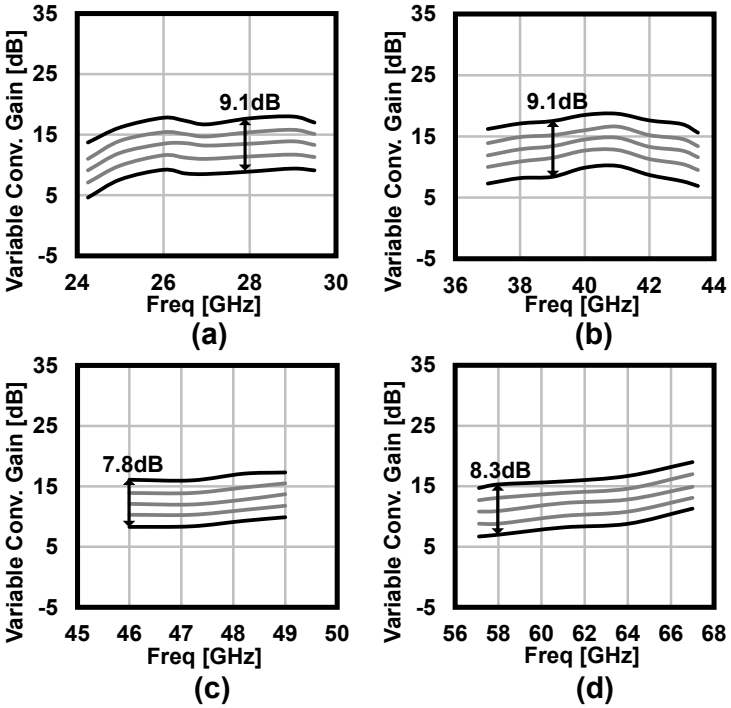


Figure 3.26: Measured receiver variable conversion gain on (a) 28GHz band mode, (b) 39GHz band mode, (c) 47GHz band mode, and (d) 60GHz band mode.

tuning and 10-bit fine tuning [74, 76]. The IF selectivity can be improved by IF VGA with a fixed IF frequency at 8GHz. A source degeneration inductor L_s is coupled and integrated with the input series inductor L_g as showed in Fig. 3.25(b) to realize improved matching with compact area [108]. A transformer with capacitors at center-tap are utilized at output of the VGA for providing matching with improved common-mode rejection ratio (CMRR). Fig. 3.26 demonstrates the measured normalized variable conversion gain of the proposed receiver in four operating mode. The IF frequency is fixed at 8GHz in measurement. During the measurement, the proposed VGA realized a 9-dB gain tuning range with 5G standard compatible bandwidth.

3.5 Measurement Result

The proposed two-channel multi-band phased-array receiver is fabricated with a 65-nm CMOS process. Fig. 3.27 shows the micrograph of the proposed chip. The chip size is 3.2mm$\times$1.4mm including 2-channel receiver element. Each element occupies 1.2-mm^2 core area while covering almost 50-GHz bandwidth. The single-path receiver character-

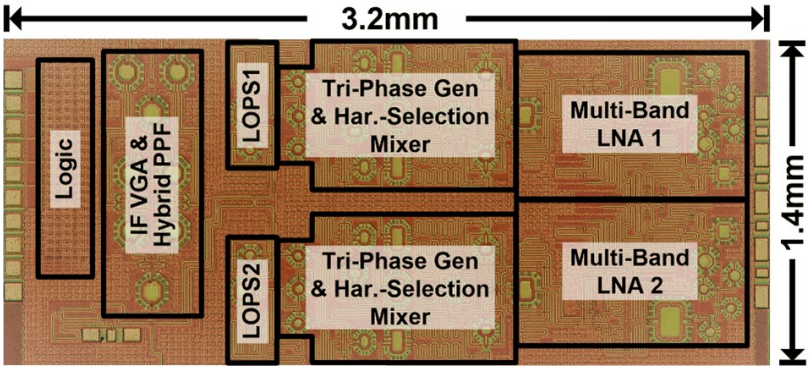


Figure 3.27: Chip micrograph of proposed 2-channel multi-band phased-array receiver.

Table 3.1: Power breakdown of single receiver channel of the proposed multi-band receiver at all operation modes.

Building Block	Dual-Mode Multi-band LNA	Harmonic-Sel. Mixer	Tri-Phase LO Gen.	IFVGA	P_{DC}/Path
28GHz Band Mode	20mW	0mW	12mW	4mW	36mW
39GHz Band Mode	17mW	0mW	11mW	4mW	32mW
47GHz Band Mode	35mW	0mW	12mW	4mW	51mW
60GHz Band Mode	50mW	0mW	21mW	4mW	75mW

istic is first on-wafer measured. Fig. 3.28 (a) demonstrates the overall CG of a single receiver path. The proposed phased-array receiver supports 24.25GHz to 71GHz operation covering all allocated spectrum in 5G NR FR2 with the help of the proposed harmonic-selection technique. Regarding a fixed IF frequency of 8GHz, the required LO coverage is only 16.25GHz to 26GHz to cover 24.25GHz to 71GHz operations. The measured CGs in four different operating modes are all around 15dB. Flat response is maintained in each mode with less than 2-dB variation. The IRRs in all four operating modes are measured with two receiver paths and shown in Fig. 3.28 (b). Owing to the Hartley receiver architecture and the band-pass filtering of LNA, the measured IRRs are always better than 52dB within all operating modes. Fig. 3.28 (c) presents the measured single-channel NF. The measured NFs are 3.6-8.0dB, 4.0-7.6dB, 5.3-6.8dB, and 4.9-6.7dB within 24.25-35GHz, 35-44GHz, 44-57GHz, and 57-67GHz, respectively. To be a reference, the measured NFs of the stand-alone LNA at 28GHz, 39GHz, 47GHz and 60GHz are 4.4dB, 4.7dB, 5.4dB, and 6dB, respectively. The measured input P1dB are shown in Fig. 3.28 (d). The achieved IP1dBs are -17.6dBm at 28GHz, -20.1dBm at 39GHz, -26.6dBm at 48GHz and -31.8dBm at 61GHz.

Selected Band	28GHz ($F_{LO}+F_{IF}$)	39GHz ($2\times F_{LO}-F_{IF}$)	47GHz ($2\times F_{LO}+F_{IF}$)	60GHz ($3\times F_{LO}-F_{IF}$)
LO Freq. Range	16-27GHz	21.5-26GHz	18-24.5GHz	21-25GHz

(a)

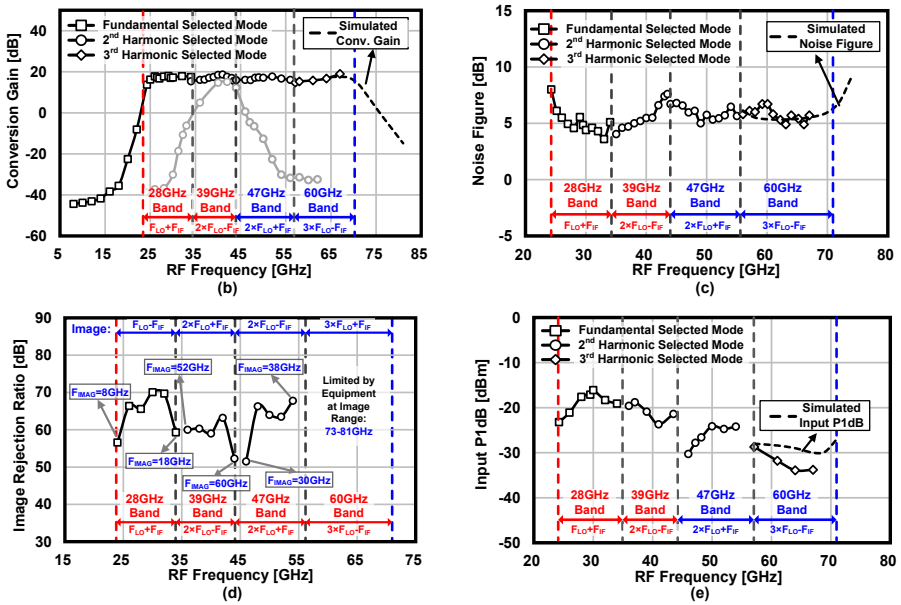
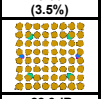
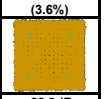


Figure 3.28: (a) Measured and simulated CG with single receiver channel. (b) Measured and simulated NF of single receiver channel. (c) Measured and simulated input P1dB of single receiver channel. (d) Measured IRRs of the proposed multi-band receiver at all operating bands.

The proposed receiver is then evaluated with 5G standard-compliant OFDMA-mode modulated signals. The OFDMA-mode modulated signals are generated by a Keysight VXG signal generator M9374B. For signals higher than 44GHz, an extra up-conversion mixer is adopted. The LO signal is generated by the Keysight signal generator E8275D. The received signals are analyzed by the Keysight oscilloscope UXR1102A. The measured EVMs and constellations over 24.25GHz to 71GHz with QPSK, 16QAM, 64QAM, and 256QAM modulations are listed in Table. 3.29. With the power consumption listed in Table. 3.1, this work achieves EVMs of -31.6dB at 24.25GHz, -33.4dB at 28GHz, -31.9dB at 39GHz, -32.5dB at 47.2GHz, -30.5dB at 60.1GHz, and -28.9dB at 71GHz with 64QAM modulation. In 256QAM modulation, the measured EVMs are -31.4dB at 24.25GHz. -33.5dB at 28GHz, -31.6dB at 39GHz, -32.4dB at 47.2GHz, -30.3dB at 60.1GHz, and -28.9dB at 71GHz.

As mentioned previously, multi-band receiver suffers from inter-band blockers. This work utilizes the harmonic-selection technique, LNA band-pass filtering, and Hartley receiver architecture to improve the rejections to inter-band blockers. In this work, the worst

Freq.			24.25GHz	28GHz	39GHz	47.2GHz	60GHz	71GHz
Mode			OFDMA	OFDMA	OFDMA	OFDMA	OFDMA	OFDMA
BW_c			400MHz	400MHz	400MHz	400MHz	400MHz	400MHz
Modulation*	QPSK (MCS4)	Const.						
		EVM (RMS)**	-32.0dB (2.5%)	-32.7dB (2.5%)	-32.1dB (2.5%)	-33.0dB (2.2%)	-30.9dB (2.8%)	-29.1dB (3.5%)
	16QAM (MCS10)	Const.						
		EVM (RMS)**	-31.8dB (2.6%)	-32.7dB (2.3%)	-32.1dB (2.5%)	-32.7dB (2.3%)	-30.7dB (2.9%)	-29.0dB (3.5%)
	64QAM (MCS19)	Const.						
		EVM (RMS)**	-31.6dB (2.6%)	-33.4dB (2.1%)	-31.9dB (2.5%)	-32.5dB (2.4%)	-30.5dB (3.0%)	-28.9dB (3.6%)
	256QAM (MCS27)	Const.						
		EVM (RMS)**	-31.4dB (2.7%)	-33.5dB (2.1%)	-31.6dB (2.6%)	-32.4dB (2.4%)	-30.3dB (3.1%)	-28.9dB (3.6%)

*5G NR MCS index table 2 for PDSCH is used. (Table 5.1.3.1-2 in 3GPP TS 38.214 V15.2.0).
**Measured EVMs are referred to the RMS magnitude.

Figure 3.29: Measured constellations and EVMs of proposed multi-band receiver at all bands.

blocker case happens when the blocker frequencies locate at the harmonic or image frequencies of the desired signals. In these conditions, the down-converted IF will be at the exactly same frequency as the desired signal, which cannot be removed by the IF band-pass filtering. In this work, the inter-band blockers are analyzed with four cases, which are at 28GHz, 39GHz, 47.2GHz, and 60.1GHz.

The rejections to harmonics and images in the above-mentioned four cases are first measured and shown in Table 3.31. This work achieves better than 36-dB rejections against the blockers located at the harmonic and image frequencies. The constellations and EVMs are also measured with inter-band blockers. The measurement setup for each operating mode is explained in Fig. 3.30. The Keysight VXG signal generator M9384B is utilized to generate the OFDMA-mode desired and blocker signals in 256QAM and 16QAM, respectively. For signals higher than 44GHz, an additional mixer is employed. The worst-case blocker frequency settings mentioned previously are applied in each case for convincing results. The measured EVMs and constellations are shown in Table. 3.32. Without the blockers, the proposed receiver demonstrates EVMs of -33.5dB, -31.1dB, -31.8dB, and -29.3dB at 28GHz, 39GHz, 47.2GHz, and 60.1GHz, respectively. With blockers on the same power level against desired signals, the measured EVMs are only slightly degraded to -33.3dB at 28GHz, -30.9dB at 39GHz, -31.6dB at 47.2GHz, and -28.5dB at 60.1GHz. The wide-band modulated 256-QAM signal is still supported with enough margin to meet the 5G NR standard.

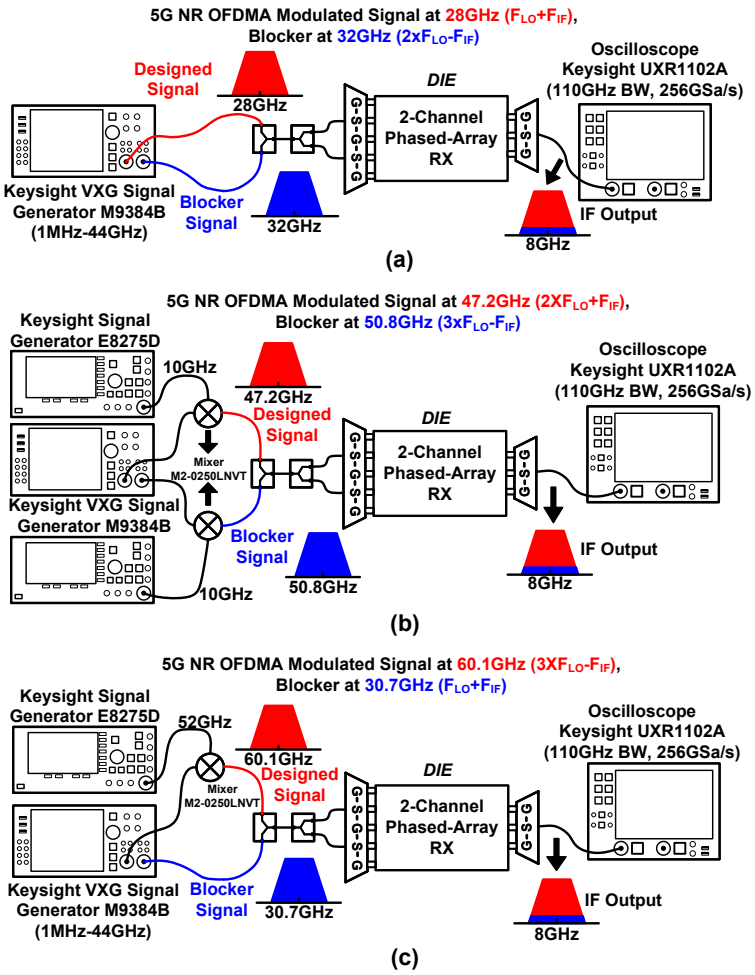


Figure 3.30: Measured constellations and EVMs of proposed multi-band receiver at all bands.

Case	Case 1	Case 2	Case 3	Case 4
Desired Signal Freq.	28GHz ($F_{LO}+F_{IF}$)	39GHz ($2\times F_{LO}-F_{IF}$)	47.2GHz ($2\times F_{LO}+F_{IF}$)	60.1GHz ($3\times F_{LO}-F_{IF}$)
Fundamental Blocker Rejection (dB) ($F_{LO}\pm F_{IF}$)	66@12GHz	58@15.5GHz 56@31.5GHz	68@11.5GHz 61@27.6GHz	64@14.7GHz 36@30.7GHz
2nd Harmonic Blocker Rejection (dB) ($2\times F_{LO}\pm F_{IF}$)	57@32GHz 58@48GHz	60@55GHz	59@31.2GHz	46@37.4GHz 43@53.4GHz
3rd Harmonic Blocker Rejection (dB) ($3\times F_{LO}\pm F_{IF}$)	63@52GHz NA*@68GHz	59@62.5GHz NA*@78.5GHz	50@50.8GHz 50@66.8GHz	NA*@76.1GHz
Blocker F_{IF} - Desired F_{IF}	0Hz	0Hz	0Hz	0Hz

*Limited by equipment operation range.

Figure 3.31: Measured inter-band blockers rejection in all bands.

	Case 1		Case 2		Case 3		Case 4	
Desired Signal Freq.	28GHz ($F_{LO}+F_{IF}$)		39GHz ($2\times F_{LO}-F_{IF}$)		47.2GHz ($2\times F_{LO}+F_{IF}$)		60.1GHz ($3\times F_{LO}-F_{IF}$)	
Desired Signal Mod.*	256QAM (MCS27) OFDMA Mode		256QAM (MCS27) OFDMA Mode		256QAM (MCS27) OFDMA Mode		256QAM (MCS27) OFDMA Mode	
Desired Signal BW_c	400MHz		400MHz		400MHz		400MHz	
Desired Signal Power	-39.1dBm		-45.3dBm		-41.9dBm		-37.0dBm	
Worst Case Blocker in EVM Measurement	32GHz ($2\times F_{LO}-F_{IF}$)		31.5GHz ($F_{LO}+F_{IF}$)		50.8GHz ($3\times F_{LO}-F_{IF}$)		30.7GHz ($F_{LO}+F_{IF}$)	
Blocker Modulation*	16QAM (MCS10) OFDMA Mode		16QAM (MCS10) OFDMA Mode		16QAM (MCS10) OFDMA Mode		16QAM (MCS10) OFDMA Mode	
Blocker BW_c	400MHz		400MHz		400MHz		400MHz	
Blocker Power Level**	0dBc		0dBc		0dBc		0dBc	
Constellation	without Blocker	with Blocker	without Blocker	with Blocker	without Blocker	with Blocker	without Blocker	with Blocker
								
EVM (RMS)	-33.5dB (2.2%)	-33.3dB (2.2%)	-31.1dB (2.8%)	-30.9dB (2.8%)	-31.8dB (2.6%)	-31.6dB (2.6%)	-29.3dB (3.4%)	-28.5dB (3.8%)

*5G NR MCS index table 2 for PDSCH is used. (Table 5.1.3.1-2 in 3GPP TS 38.214 V15.2.0).

**Measured EVMs are referred to the RMS magnitude.

Figure 3.32: Summarized constellations and EVMs of proposed receiver with worst-case 0-dBc inter-band blockers.

Table 3.2: Performance Comparison of Multi-Band Phased-Array Receiver

	This work				**UCSD [96]**		**Georgia Tech [67]**		**CMU [94]**		**UCSD [37]**
Process	65nm CMOS Bulk				22nm CMOS, FD-SOI		22nm CMOS, PD-SOI		65nm CMOS Bulk		0.18μm SiGe BiCMOS
Integration	LNA, Harmonic-Selection Mixer, LOPS, IF, LO				LNA, Mixer, IF, LO		LNA, Mixer, IF, LO		LNA, VSPS, Mixer, BB, LO		LNA, RFPS
Frequency	24.25 ~ 71GHz				20 ~ 44GHz		24.5 ~ 43.5GHz		27 ~ 38.75GHz		15 ~ 57GHz
Noise Figure (dB)	24.25 ~ 35GHz	35 ~ 44GHz	44 ~ 57GHz	57 ~ 71GHz**	20 ~ 44GHz		24.5 ~ 43.5GHz		27 ~ 29.75GHz	35 ~ 38.75GHz	15 ~ 57GHz
	3.6~8.0	4.0~7.6	5.3~6.8	4.9~6.7**	3.3~5		3.2~6.1		5.7~8.0*	8.5~10*	5.1~7.4
IP1dB* (dBm)**	28GHz	39GHz	48GHz	61GHz	20GHz	40GHz	28GHz	39GHz	28GHz	37GHz	40GHz
	-17.6	-20.9	-26.6	-31.8	-25*	-29.5*	-25	-27	-30	-23	-30*
Inter-Band Rej. Architecture	Harmonic Selection, Hartley RX				N/A		Hartley RX		Hartley RX		N/A
Inter-Band Rejection	Rejection to All Other Bands				N/A		Dual-Band Rej. to 28/39GHz		Dual-Band Rej. to 28/39GHz		N/A
	28GHz	39GHz	47.2GHz	60.1GHz	N/A		28GHz		28GHz/37GHz		N/A
	>57dB	>56dB	>50dB	>36dB	N/A		56dB		>35dB		N/A
Modulation w. Inter-Band Blocker	256QAM MCS27 OFDMA	256QAM MCS27 OFDMA	256QAM MCS27 OFDMA	256QAM MCS27 OFDMA	N/A		256QAM (SC mode only)		N/A		256QAM OFDMA
Blocker Level	0dBc	0dBc	0dBc	0dBc	N/A		0dBc		N/A		N/A
EVM w. Blocker	-33.3dB	-30.9dB	-31.6dB	-28.5dB	N/A		-29.2dB		N/A		N/A
P_{DC}/Path	36mW	32mW	51mW	75mW	70mW		60mW		77.5mW		180mW
Area/Path	1.2-mm^2				1.28-mm^2*		0.52-mm^2		0.55-mm^2		0.77-mm^2*

* Estimated from paper. ** Referred to peak constellation power. *** Measured without VGA.

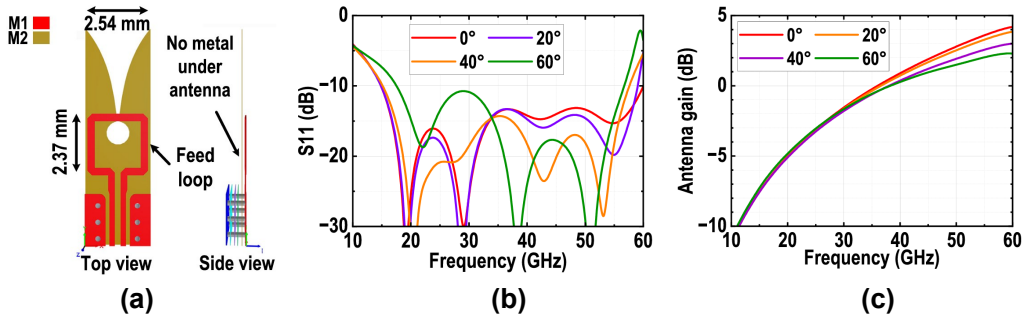


Figure 3.33: (a) Structure of a 15-55 GHz wideband Vivaldi antenna on PCB. (b) Simulated return loss of the Vivaldi antenna. (c) Simulated antenna gain of the Vivaldi antenna.

Table 4.5 compares this work with other state-of-the-art multi-band receivers designed for 5G NR FR2 [37, 67, 94, 96]. Thanks to the proposed harmonic-selection technique, this work supports 24.25GHz to 71GHz operation while maintaining over 36-dB inter-band blocker rejection. Each channel of the proposed receiver only consumes 36mW, 32mW, 51mW, and 75mW, when operating at 28GHz, 39GHz, 47.2GHz, and 60.1GHz, respectively. The proposed receiver can support ultra-wide-band operation with minimized power consumption and improved inter-band blocker rejections.

3.6 Multi-Band Antenna Designs

Wideband antennas are crucial in multi-band receiver systems to support multi-standard communication across various frequency bands. Although a PCB implementation of the proposed multi-band phased-array receiver prototype has not been conducted, it is essential to discuss antenna design considerations for future development. Among the numerous wideband antenna topologies, Vivaldi antennas are preferred due to their broadband characteristics, high gain, and compatibility with planar PCB designs, making them ideal for millimeter-wave communication and radar systems.

A typical wideband Vivaldi antenna is shown in Fig. 3.33(a). The Vivaldi antenna operates based on the principle of traveling waves propagating through a tapered slot structure, which gradually transforms the guided wave impedance to free-space impedance, enabling wide operational bandwidth. The example antenna in Fig. 3.33(a) is designed to operate within the 15–55 GHz range [38], featuring a tapered opening and a feed loop to improve impedance matching and radiation efficiency. The absence of metal beneath the antenna, as depicted in the side view, reduces interference and enhances radiation performance. The simulated return loss results in Fig. 3.33(b) demonstrate the antenna's ability

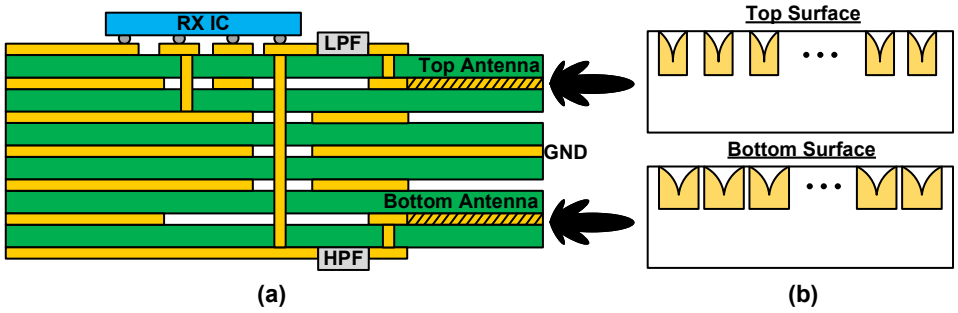


Figure 3.34: (a) The PCB stack configuration for double-side Vivaldi antenna array. (b) The Vivaldi antenna array with different setting on top and bottom surface.

to achieve good impedance matching across a wide frequency range at various beam-steering angles. Additionally, the antenna gain characteristics, shown in Fig. 3.33(c), indicate stable performance across the 10–60 GHz range, highlighting the antenna's capability to provide consistent directional gain across different frequencies. These features make the Vivaldi antenna an excellent candidate for multi-band receiver applications.

However, the bandwidth of a single Vivaldi antenna is still limited. The example shown in Fig. 3.33 does not fully cover the 24–71 GHz frequency range required by the 5G NR standard, let alone potential future bands. Another limitation arises from the fixed antenna pitch, which can introduce grating lobes at frequencies far from the optimal half-wavelength spacing of the antenna layout. Advancements in PCB manufacturing technology offer a promising solution—implementing Vivaldi antennas with different pitches on both sides of the PCB, as shown in Fig. 3.34. In this design, two parallel Vivaldi antenna arrays are optimized for different frequency ranges, effectively minimizing grating lobes caused by the aliasing effect of the fixed antenna pitch.

However, this type of design introduces additional challenges. Since two antennas are connected to a single LNA in parallel, the input matching characteristics significantly deviate from those of a traditional single-element design. Consequently, the LNA input matching conditions must be reconsidered and redesigned to ensure proper noise performance and maintain the sensitivity. A straightforward solution, such as employing a power combiner on the PCB, can resolve the matching issue. However, the inherent 3-dB insertion loss from the power combiner is entirely unacceptable, as it directly reduces the sensitivity. To address this issue without compromising efficiency, surface-mounted high-pass and low-pass filters can be integrated into the PCB, as shown in Fig. 3.34. These filters provide isolation between the two antennas, allowing each antenna and the LNA to maintain their original impedance characteristics without incurring additional insertion

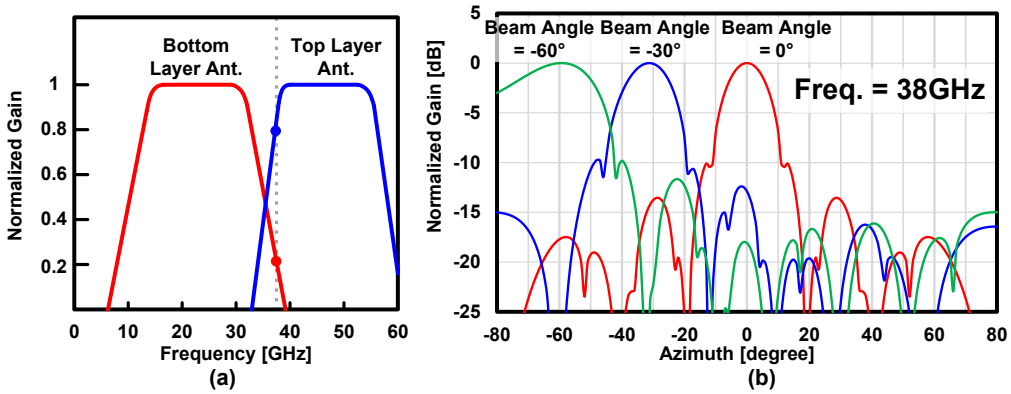


Figure 3.35: (a) Overlapped frequency response of dual-side Vivaldi antenna. (b) Simulated equivalent receiver beam pattern at 38GHz.

losses. Another crucial reason for employing non-overlapping frequency bands through filtering is to prevent pattern distortion due to antenna array design differences. The top- and bottom-layer Vivaldi antenna arrays exhibit distinct beam patterns due to their different antenna spacings. Specifically, for the high-frequency band array, the element spacing is less than half a wavelength ($d < \frac{\lambda}{2}$), while for the low-frequency band array, the spacing exceeds half a wavelength ($d > \frac{\lambda}{2}$). This difference results in unique sidelobe patterns and notch behaviors for each antenna array. Without proper frequency isolation, the passbands of the two antennas would inevitably overlap, as depicted in Fig. 3.35(a). At the transition frequency, beam pattern distortion can occur due to interference between the arrays. For example, at 38 GHz, while the high-band antenna operates, the low-band antenna still exhibits a normalized gain of approximately –8 dB. As shown in Fig. 3.35(b), this residual gain causes severe beam pattern glitches and unpredictable sidelobes, compromising the overall beamforming performance. By isolating the bands with high-pass and low-pass filters, the beam patterns remain stable, and the system achieves a clean transition between frequency bands, ensuring reliable directional performance and minimal interference.

A key drawback of on-PCB Vivaldi antenna arrays is their limitation to transmitting or receiving signals only in directions parallel to the PCB edge. While conventional patch antennas can easily achieve two-dimensional beam steering with planar arrays, edge-placed Vivaldi antennas cannot provide similar functionality within a single PCB layer. To overcome this limitation, two-dimensional phased arrays can be realized by stacking multiple PCBs, as demonstrated in Fig. 3.36. A recent work in [110] presents a stacked Vivaldi phased array implementation operating above 200GHz, where on-chip Vivaldi antennas and flexible PCBs are utilized to achieve extremely fine antenna pitch. Although

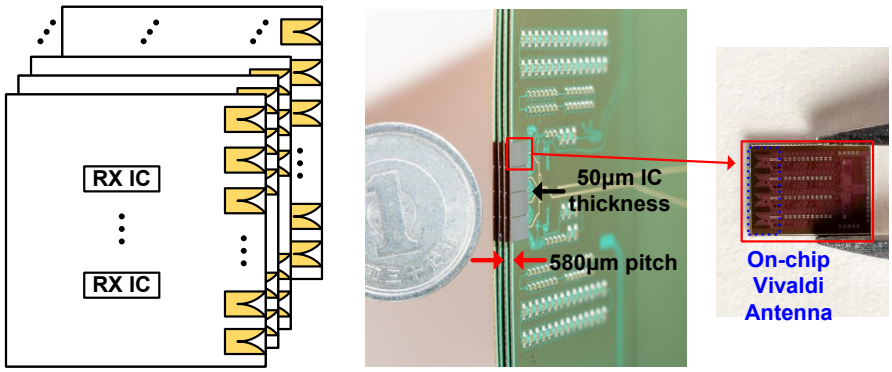


Figure 3.36: Two-dimension phased-array with wide-band Vivaldi antennas by stacking multiple PCBs.

phased array performance at such high frequencies is highly sensitive to PCB assembly mismatches, measurements have shown excellent beam patterns. For sub-100GHz applications, a two-dimensional Vivaldi antenna array implemented using stacked PCBs is a viable solution, offering enhanced performance and scalability for future multi-band phased-array receivers.

3.7 Summary

In this chapter, a novel harmonic-selection technique is introduced and validated through a two-channel multi-band phased-array receiver prototype. The receiver achieves a wide frequency coverage from 24.25 to 71 GHz, making it compatible with all existing 5G NR FR2 bands and the potential 60-GHz unlicensed band. By integrating a dual-mode multi-band LNA and a Hartley architecture, the proposed design achieves exceptional inter-band blocker rejections of 57 dB, 56 dB, 50 dB, and 36 dB at 28 GHz, 39 GHz, 47.2 GHz, and 60.1 GHz, respectively. This level of rejection ensures robust performance even in the presence of 0-dBc worst-case inter-band blockers. The receiver supports standard-compliant 400-MHz 5G NR modulated signals in 256-QAM with low power consumption per channel: 36 mW, 32 mW, 51 mW, and 75 mW at 28 GHz, 39 GHz, 47.2 GHz, and 60.1 GHz, respectively. The proposed energy-efficient and cost-effective harmonic-selection technique is well-suited for the multi-band operation solution of the evolving millimeter-wave communication standards, offering enhanced inter-band blocker rejection without compromising performance. The scalability of the proposed harmonic-selection technique, combined with the flexibility of the multi-mode LNA, enables compatibility with

higher frequencies without significant design complexity or additional power overhead. These features make the proposed receiver an ideal candidate for next-generation high-performance millimeter-wave systems, ensuring adaptability to future communication demands.

However, there are several areas where the proposed multi-band receiver can be further improved to enhance its performance:

1. Antenna Design: For a practical multi-band receiver, the antenna array must support operation across multiple frequency ranges. This requires careful design of the antenna array to ensure adequate bandwidth and efficiency at each frequency band, as well as corresponding PCB layout optimization to minimize signal loss and interference.

2. Background Calibration: The present foreground calibration method for the proposed hybrid-type PPF requires a test tone to be sent from the output port. This approach is inconvenient for practical use, as it interrupts normal operation and reduces communication time. By introducing automatic background calibration, the system could continuously compensate for PVT variations without interrupting operation, ensuring consistent performance during real-time communication.

Chapter 4

Area-Efficient Millimeter-Wave Time-Division MIMO Phased-Array Receiver

As discussed in Chapter 1, multiple-input multiple-output (MIMO) systems are essential for next-generation receivers to achieve higher data rates as operating frequencies continue to increase. At millimeter-wave frequencies, precise analog beamforming can be achieved with fully-on-chip phased arrays, enabling MIMO systems to leverage spatial multiplexing through beamforming. Extensive research has been conducted to develop power-efficient and high-performance MIMO receivers [1, 10, 11, 15, 16, 18, 33, 36, 67–69, 77, 78, 91, 93, 94, 111–118]. While millimeter-wave frequencies promise greater MIMO scalability than microwave bands, its small wavelength severely constrains the physical size of MIMO receiver ICs. As shown in Fig. 4.1(a), multi-chip phased arrays are common in millimeter-wave systems, with each IC typically designed to support 4 antenna elements to ensure symmetrical antenna connections with equal-length wires. The pitch of the antenna array matches the carrier frequency's half-wavelength, limiting the chip size for integration. For instance, at 50 GHz, the chip size must remain below 6 mm to avoid collisions. This constraint becomes even more restrictive when considering space for interconnect wiring. Although this situation is slightly more manageable at 28 GHz, future systems will operate at even higher frequencies, exacerbating this challenge.

Fig. 4.2 and Table 4.1 summarize recent MIMO receiver ICs. Many of these works are too large to fit within the physical constraints of a 2D multi-chip array at higher frequencies, such as 50 GHz. Furthermore, conventional MIMO architectures scale chip area with the number of MIMO streams, further limiting their ability to meet future requirements for higher data rates. The separation of MIMO streams in existing designs also

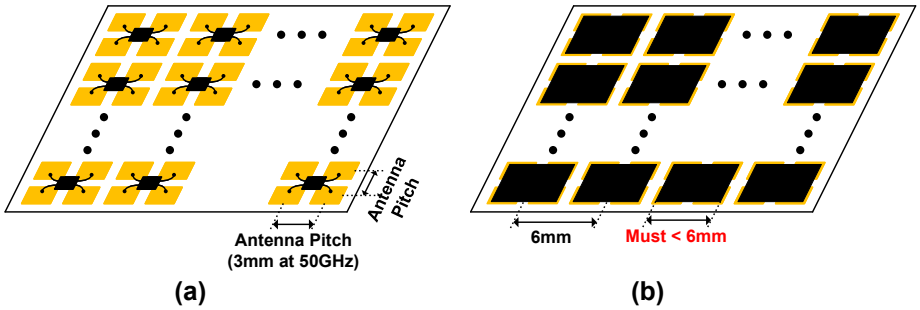


Figure 4.1: (a)Millimeter-wave large-scale 2D multi-chip phased-array SISO PCB. (b) Millimeter-wave large-scale 2D multi-chip phased-array MIMO PCB.

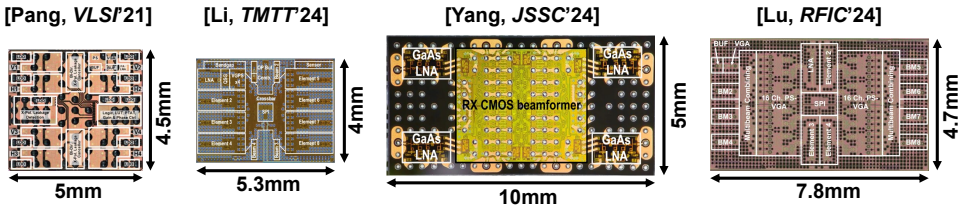


Figure 4.2: Chip micrograph and size of recent published MIMO phased-array receivers.

complicates multi-chip connections. Inter-chip connections for multiple MIMO streams require multi-layer PCBs with specialized designs to integrate the various combining networks. For instance, as shown in Fig. 4.3, a 12-layer PCB was designed for a 4-beam MIMO module in [3], significantly increasing cost and design complexity.

To address these challenges, this thesis proposes a Time-Division MIMO (TD-MIMO) architecture. This novel MIMO receiver design minimizes hardware requirements while remaining reconfigurable to support additional MIMO streams, enabling higher data rates without redesigning PCB or RF building blocks. Furthermore, TD-MIMO implements a single-wire chip connection for combining multiple MIMO streams, significantly reducing the difficulty of forming large-scale multi-chip phased arrays. This chapter is or-

Table 4.1: Summarization of recent millimeter-wave MIMO receivers

Reference	Architecture	#Streams	#Antenna	#RF Paths	Chip Size
J. Pang, *VLSI 21*	Fully-Connected	2	4	8	5mm × 4.5mm
Li, *TMTT 24*	Fully-Connected	4	8	32	5.3mm × 4mm
Yang, *JSSC 24*	Fully-Connected	4	4	16	10mm × 5mm
Lu, *RFIC 24*	Fully-Connected	4	4	32	7.8mm × 4.7mm
ADI ADAR3001	Fully-Connected	4	4	16	175mm^2

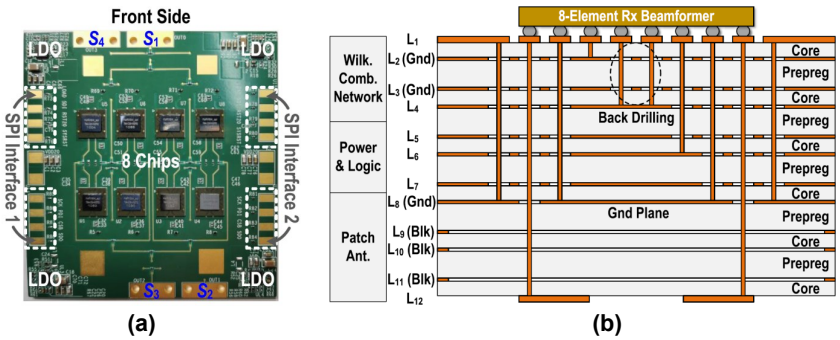


Figure 4.3: (a) PCB photograph of the 8-chips 64-element four-beam phased-array receiver module in [3]. (b) PCB stack up.

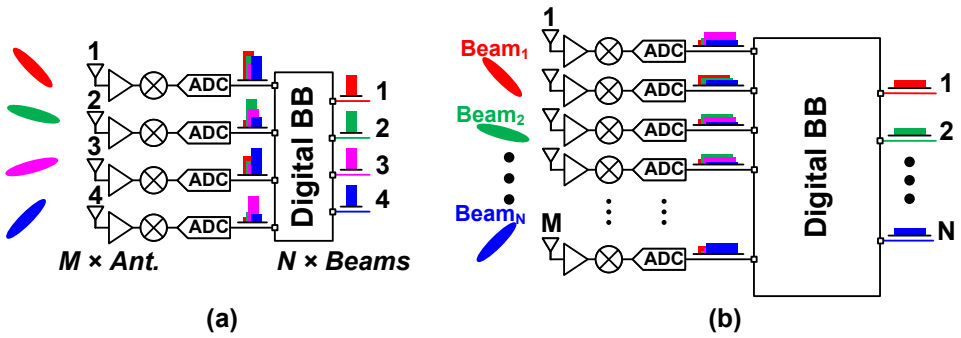


Figure 4.4: (a) Digital MIMO receiver at microwave. (b) Digital MIMO receiver at millimeter wave.

ganized as follows: Section 4.1 reviews conventional phased-array MIMO architectures. Section 4.2 provides a detailed analysis of the proposed TD-MIMO architecture and compares it with existing approaches. Section 4.3 describes the circuit design of the proposed receiver, while Section 4.4 presents on-wafer and over-the-air (OTA) measurements, including beam-switching speed and EVM with 5G NR modulated signals. Finally, Section 4.6 concludes the chapter and discusses potential improvements.

4.1 Conventional Phased-Array MIMO Receivers

4.1.1 Digital MIMO

Digital MIMO is an extension of digital beamforming that enables simultaneous communication across multiple spatial channels. This powerful signal processing technique uses multiple independent data streams to enhance spectral efficiency and capacity, making it a popular choice in sub-6 GHz 5G NR receivers. Figure 4.4(a) illustrates the architecture of a typical microwave 4-element digital MIMO receiver. In this design, each antenna element is connected to a dedicated signal chain, including an independent ADC for digitizing the received signals. When multiple signals arrive, each antenna element captures a portion of each signal. These signals are separated and processed in the digital baseband, which performs channel estimation, precoding, and decoding. This architecture offers exceptional flexibility, enabling dynamic adaptation to varying channel conditions and multi-user support.

However, implementing digital MIMO at millimeter-wave frequencies presents significant challenges. As shown in Fig. 4.4(b), the large bandwidths and low SNRs at millimeter-wave require ADCs with high sampling rates and resolutions, leading to significant power consumption and data processing overhead. Additionally, the digital overhead scales with both the array size M and the number of beams N. while $M \geq N$ is sufficient in microwave systems with fewer elements (e.g. $M = N = 4$ in Fig. 4.4 (a)), millimeter-wave systems typically require much larger arrays ($M \gg N$) to compensate for higher free-space path loss (FSPL). This results in a bulky digital baseband and increased complexity. Furthermore, multi-chip digital MIMO with a shared digital baseband becomes impractical due to the complicated wiring and the physical constraints imposed by the limited chip area, which is restricted by the smaller antenna pitch at millimeter-wave frequencies. These factors make fully digital MIMO unsuitable for millimeter-wave systems, where hybrid or analog MIMO architectures are preferred for their efficiency, scalability, and reduced overhead [15, 68, 115, 116, 119].

4.1.2 Partially-Connected MIMO

In contrast to digital MIMO, analog MIMO utilizes analog beamforming through phased arrays to separate multiple spatial streams before digital processing. Partially-connected MIMO, a subset of analog beamforming architectures, can be simply described as a combination of several SISO phased array receivers. In this architecture, each RF chain is exclusively connected to a distinct sub-array of antenna elements, enabling independent beamforming operations for each spatial beam, as shown in Fig. 4.5. This straightfor-

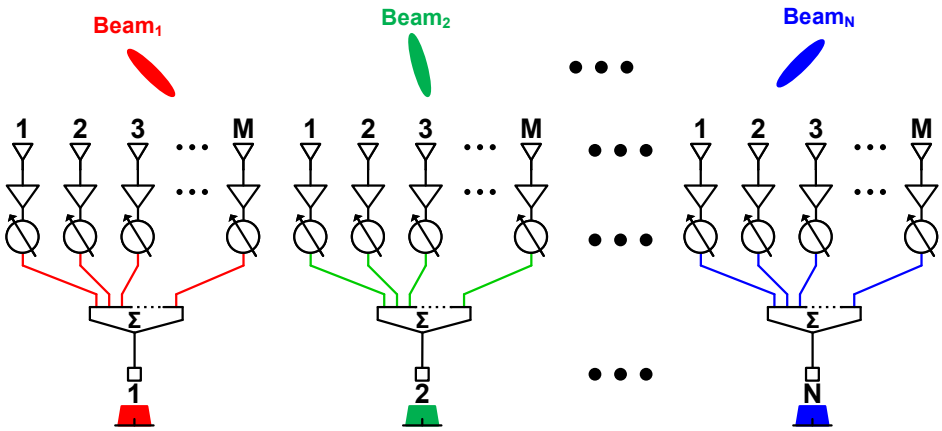


Figure 4.5: Partially-connected MIMO phased-array receiver architecture.

ward design makes partially-connected MIMO particularly suitable for millimeter-wave systems, where digital MIMO architectures face significant challenges as introduced before. One of the key advantages of analog beamforming-based MIMO is its ability to leverage spatial multiplexing for improved signal isolation between sub-arrays. By physically separating signal paths and associating them with distinct antenna groups, partially-connected MIMO inherently reduces interference, resulting in enhanced dynamic range and better RF performance.

However, partially-connected MIMO has notable limitations. Because antennas are not shared between RF chains, the architecture requires a larger form factor, making it less compact. Its scalability is constrained without adding additional hardware, increasing cost and package size. Despite these trade-offs, partially-connected MIMO remains an effective solution for millimeter-wave systems requiring simple and efficient analog beamforming.

4.1.3 Fully-Connected MIMO

Fully-Connected MIMO is an advanced analog beamforming architecture designed to maximize flexibility and performance in phased-array systems. Unlike partially-connected MIMO, where each RF chain is connected to a distinct sub-array of antennas, fully-connected MIMO shares the entire aperture among all sub-beamformers using variable phase shifters and amplitude controls. As shown in Fig. 4.6, the received signals at the antennas are evenly divided and routed to the RF signal chains of each sub-beamformer. One of the key advantages of fully-connected MIMO over partially-connected MIMO

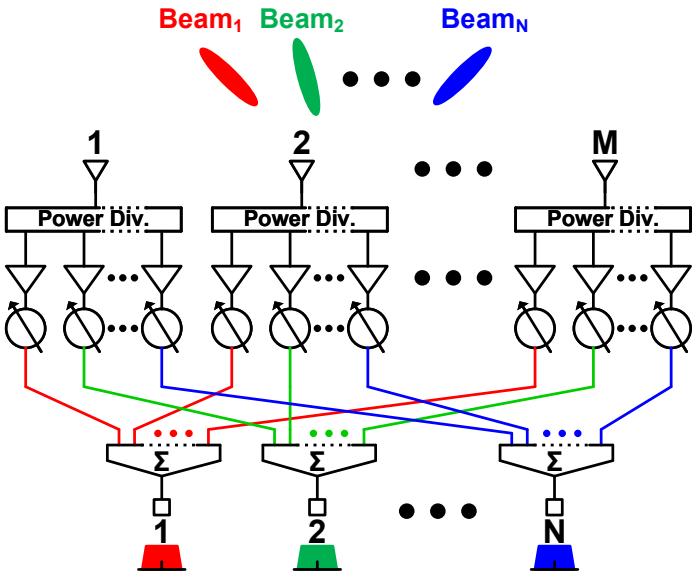


Figure 4.6: Fully-connected MIMO phased-array receiver architecture.

is its superior beamforming flexibility. With the same overall antenna package size, fully-connected MIMO leverages all antenna elements for each RF beamformer, achieving finer spatial control and enabling the formation of narrower beams with higher gain. This leads to improved spatial multiplexing, allowing the system to handle more users or streams simultaneously. Additionally, with the same sub-array size, fully-connected MIMO achieves a more compact form factor.

However, aperture sharing and power division in fully-connected MIMO degrade the SNR compared to a SISO phased array receiver with the same aperture. The fully-connected topology also introduces significant complexity, as the large number of interconnections requires extensive RF circuitry, increasing design challenges. The total number of RF chains must equal the product of the number of MIMO streams N and the array size M. As N increases, the wiring complexity and RF chain count scale proportionally, limiting scalability. This necessitates larger chip areas to accommodate additional MIMO streams. Similar to digital MIMO, the chip area is constrained by the antenna pitch in large-scale multi-chip arrays, especially at millimeter-wave frequencies. As a result, more than three MIMO streams have yet to be demonstrated for 2D arrays. Additionally, intra-chip connections for multi-chip fully-connected MIMO require multi-layer PCBs with specialized designs to integrate the multiple combining networks for each MIMO stream. As showed in Fig. 4.3, a 12-layer PCB is designed for 4-beam

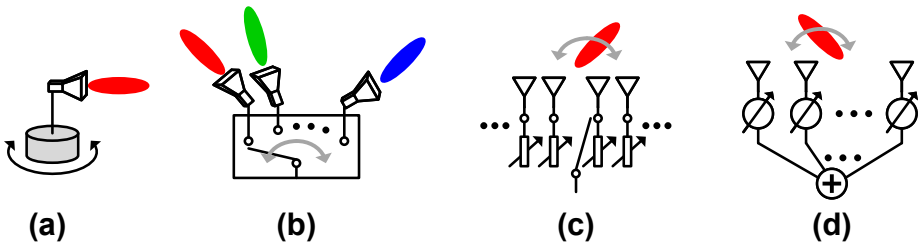


Figure 4.7: (a) Rotation of directional antenna. (b) Directional-antenna switching type. (c) Switching of passive parasitic antenna element. (d) Beamforming type.

MIMO module in [3], which greatly increases the cost and design difficulty. Despite these challenges, fully-connected MIMO remains popular in millimeter-wave communications and advanced radar systems due to its balance between module size and performance [15, 68, 115, 116, 119].

4.1.4 Time-Modulated Array

Conventional analog beamforming-based MIMO systems face a fundamental trade-off between chip area and the number of supported MIMO streams. Fully-connected MIMO architectures, with their predetermined power division and interconnection networks, suffer from unnecessary SNR degradation when fewer beams are utilized than the system's maximum capacity. Furthermore, the lack of scalability and flexibility in RF performance makes these traditional approaches less suitable for next-generation millimeter-wave receivers. A promising solution to address these challenges is hardware reuse, where antenna elements or beamformers can be shared among multiple MIMO streams, significantly improving area efficiency.

In microwave systems, such hardware multiplexing has already been explored. To better understand the potential of such approaches, it is useful to first examine the common methods for beam steering, as illustrated in Fig. 4.7. Beam steering techniques can be classified into four categories:

1. Mechanical Rotation (Fig. 4.7 (a)): This method, commonly used in radar systems, physically rotates the directional antenna to achieve beam steering. However, mechanical limitations result in slow response times, making it unsuitable for high-speed MIMO communications.

2. Antenna Switching (Fig. 4.7 (b)): In this approach, multiple antennas pointing in

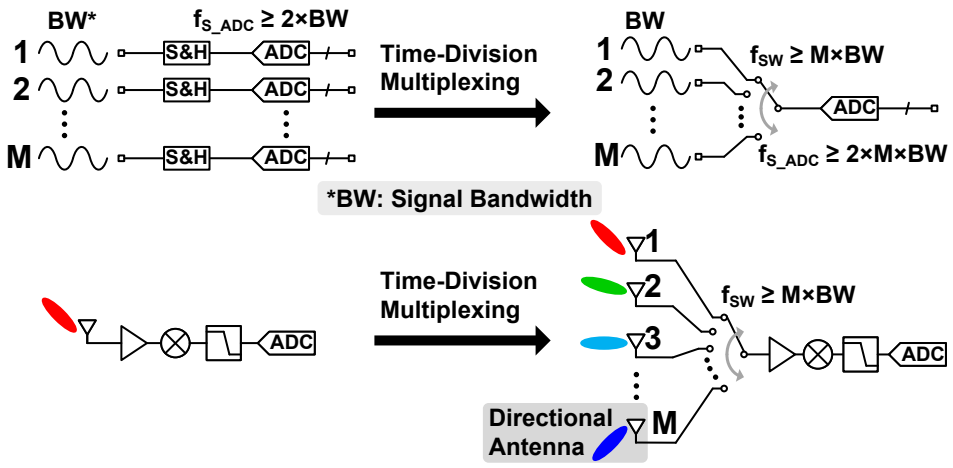


Figure 4.8: Time-division spatial multiplexing for MIMO receivers.

different directions are switched to achieve beam steering. This technique offers improved speed over mechanical methods but requires additional hardware.

3. Parasitic Element Switching (Fig. 4.7 (c)): Instead of switching between antennas, beam steering is achieved by dynamically adjusting the impedance and position of passive parasitic elements. This method provides compact and lightweight solutions while maintaining agility.

4. Beamforming-Based Steering (Fig. 4.7 (d)): Utilizing electronic phase shifting within an antenna array to achieve precise and dynamic beam steering, this approach is the most commonly used in modern communication systems.

High-speed switching techniques, such as those in Fig. 4.7 (b) and Fig. 4.7 (c), replace slow mechanical methods and open up new opportunities for circuit-level beamforming solutions.

To achieve scalable and area-efficient MIMO architectures, sampling and multiplexing techniques offer a viable solution. As shown in Fig. 4.8, time-division sampling, commonly used in ADC design, allows a single ADC to handle multiple input signals as long as the sampling rate satisfies the Nyquist criterion. This concept, when applied to MIMO receivers, enables the hardware sharing across multiple spatial beams without data loss. This architecture depicted in Fig. 4.8 is also called time-modulated array (TMA), leveraging time-division multiplexing at a Nyquist-rate switching frequency to dynamically allocate the RF front-end resources across multiple beams. This approach significantly reduces hardware complexity, requiring only a single RF chain after the time-modulated

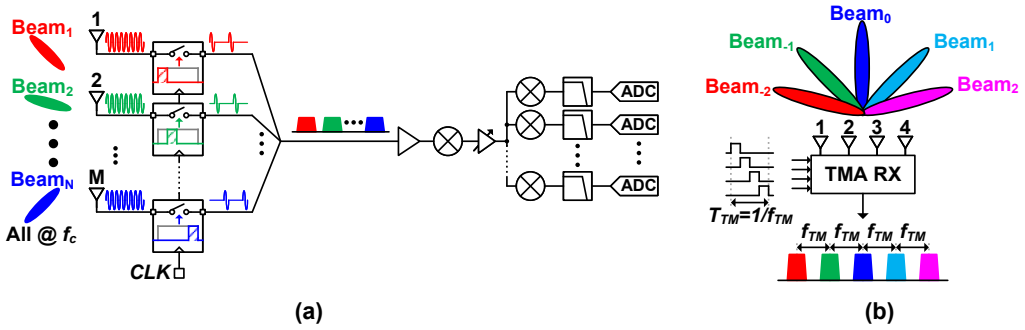


Figure 4.9: (a) Schematic of time-modulated array. (b) Spatial-to-spectrum mapping of time-modulated array.

switch array. The TMAs can be applied to both antenna switching and parasitic element switching system. the TMAs were first introduced in the 1960s [120, 121], but were initially limited by the challenges of achieving high-frequency time modulation. However, with advancements in CMOS technology, TMAs have gained renewed interest, even for millimeter-wave applications [113, 122–124].

The time and frequency domain characteristics of TMAs have been extensively studied in previous research. TMAs introduce time-domain modulation as an additional degree of freedom in phased arrays, enabling functionalities beyond the capabilities of traditional phased-array systems. As illustrated in Fig. 4.9(a), the periodic time-varying control signals applied to switches result in the redistribution of received signals into distinct spectral components, as shown in Fig. 4.9(b). The time modulation signal applied to the antenna elements can be expressed as:

$$a_n(t) = \sum_{m=-\infty}^{\infty} \beta_{n,m} e^{jm\omega_{\mathrm{TM}}t} \tag{4.1}$$

where $\beta_{n,m}$ represents the Fourier coefficients of the m-th harmonic of the time-modulation frequency $\omega_{\mathrm{TM}} = 2\pi/T_{\mathrm{TM}}$, and T_{TM} is the period of time modulation control signals. The array factor (AF) of a TMA, incorporating both time modulation and the spatial arrangement of antennas, can be expressed as:

$$\mathrm{AF}(\theta,t) = \sum_{m=-\infty}^{\infty} e^{j(\omega_c + m\omega_{\mathrm{TM}})t} \sum_{n=0}^{N-1} \beta_{n,m} e^{jknd\sin\theta} \tag{4.2}$$

where θ is the angle of arrival (AoA), k is the wavenumber, d is the element spacing, and ω_c is the carrier frequency. TMAs map signals from different directions θ to distinct harmonic frequencies, enabling multiple steerable beams using minimal hardware. For an

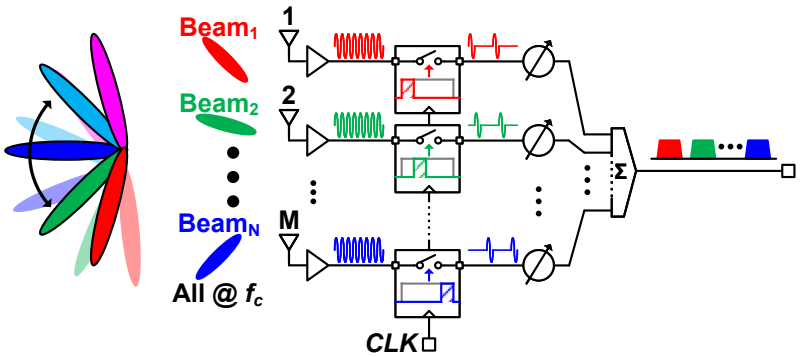


Figure 4.10: Schematic of a millimeter-wave TMA realizing full field-of-view coverage.

N-element TMA, N+1 beams can be generated, each corresponding to a unique harmonic frequency. This architecture requires only a single RF front-end after the time-modulated switch array, significantly reducing hardware complexity. The one-wire output simplifies integration into large-scale multi-chip arrays, significantly reducing wiring complexity.

However, TMAs have notable limitations. The spatial-spectral mapping fixes the beam pattern, allowing reception only from The N+1 directions determined. This means TMAs cannot adaptively steer beams to arbitrary directions. Besides, the insertion loss introduced by the switch array at high frequencies makes it unsuitable for millimeter-wave applications. At millimeter-wave frequencies, independent LNAs are necessary for each switch in TMAs to compensate the significant insertion loss. Fig. 4.10 shows a recent published TMA operates in millimeter wave [113]. While the additional phase shifters can rotate the entire beam pattern for full field-of-view (FOV) coverage , their practicality diminishes in complex and dynamic electromagnetic environments. A more critical issue is SNR degradation. Unlike conventional phased arrays that improve SNR with increasing array size, TMAs provide no beamforming gain and maintain the same SNR as a single-element receiver. Moreover, active components such as LNAs and VGAs operate continuously, even outside the duty cycle, reducing power efficiency. While analog beamforming MIMO improves the SNR proportionally with an increase in array size, TMAs can only increase the number of supported beams by enlarging the array size, without providing a corresponding SNR enhancement. These drawbacks highlight the challenges of employing TMAs in real-world millimeter-wave systems.

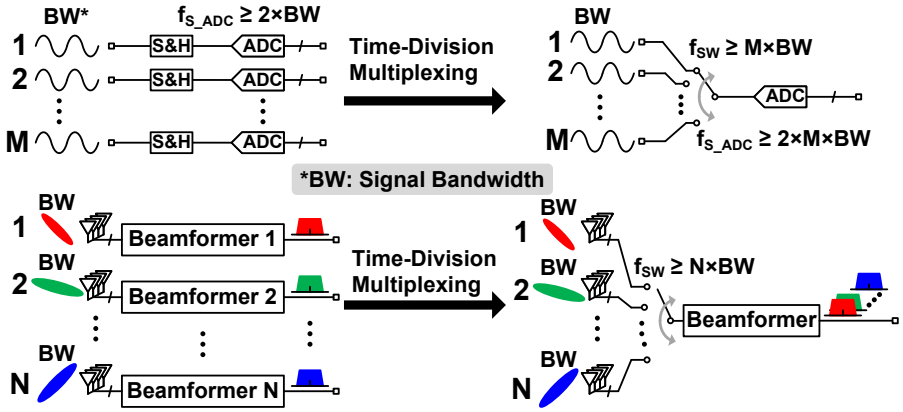


Figure 4.11: Time-division multiplexing of analog beamformer.

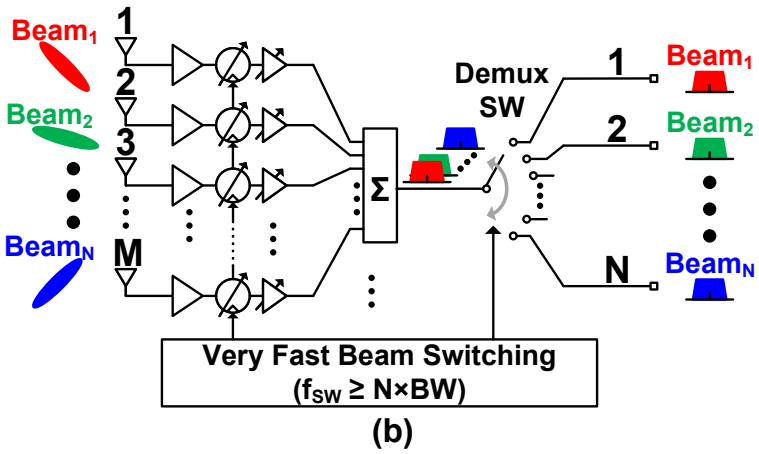


Figure 4.12: Proposed time-division MIMO phased array receiver architecture.

4.2 Proposed Time-Division MIMO

To address the need for area-efficient MIMO receivers, sampling-based hardware sharing can be applied. As illustrated in Fig. 4.11, time-division sampling allows each ADC to handle multiple input signals by alternating between them at a sampling rate that satisfies the Nyquist criterion. This time-division multiplexing approach significantly reduces the required number of ADCs. Since most communication standards operate with bandpass signals, applying Nyquist-rate sampling to a phased-array ensures no loss of information. Beyond ADC sharing, the analog beamformer can also be shared across multiple beams

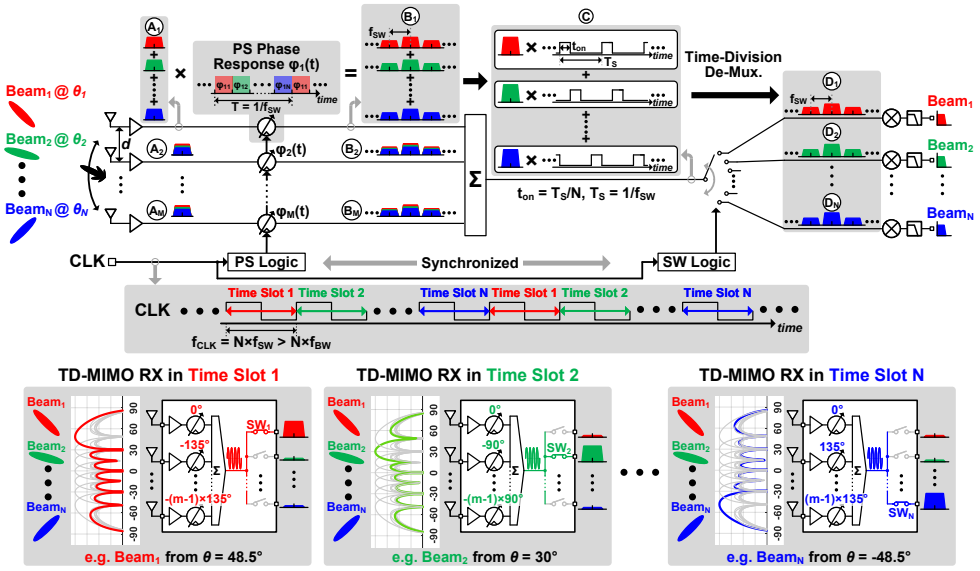


Figure 4.13: Explanation of the proposed TD-MIMO operation in both the time and frequency domains.

using time-division multiplexing at a Nyquist-rate switching frequency f_{SW}. This concept forms the proposed Time-Division MIMO (TD-MIMO) technique, as shown in Fig. 4.12. The proposed TD-MIMO maintains a constant number of RF signal paths, regardless of the number of MIMO streams, enabling a scalable solution without proportional hardware expansion. The detailed operational principles of TD-MIMO are analyzed in the following subsection, providing a comprehensive understanding of its implementation and advantages.

4.2.1 TD-MIMO Operation

The TD-MIMO architecture proposed in this work aims to enhance area efficiency. Instead of assigning a dedicated RX path to each MIMO stream, the TD-MIMO receiver shares the same RF element across all streams in different time slots. This is achieved through Nyquist-rate fast beam switching and synchronized TD-MIMO de-multiplexing. Fig. 4.13 provides an intuitive illustration of the TD-MIMO operation in both the frequency and time domains. The TD-MIMO receiver uses an external clock to control beam switching and synchronization. For example, in time slot 1, the PS phase configuration steers the pointed angle of arrival (AoA) to beam 1 at 48.5°. In time slot 2, the PSs are switched to a different phase configuration, shifting the pointing AoA to beam 2 at 30°. This process repeats across multiple time slots, and after reaching the last slot (time

slot N), the beam direction cycles back to beam 1. After beamforming, the TD-MIMO switch, synchronized with the beam-switching sequence, classifies and collects the beam-formed signals, directing each to its corresponding output port. In the frequency domain, the proposed TD-MIMO operation generates harmonics in the spectrum, while aliasing is avoided through Nyquist-rate oversampling. The required clock frequency to satisfy the Nyquist sampling theorem is $N \times f_{SW}$, where f_{SW} represent the signal bandwidth. For a 400 MHz f_{SW} (typical for 5G NR FR2), the beam switching period is as short as 2.5 ns. For simplification of calculations, we assume that the antenna element spacing d is set to $\lambda/2$, where λ represents the wavelength of the carrier signal. Considering a far-field source assumption, the angle of arrival θ_x of beam x (where $1 \leq x \leq N$) is considered identical across all antenna elements. Taking the first RF element as the reference phase plane, the combined received signal of all N beams at point A of y-th element (where $1 \leq y \leq M$) can be mathematically expressed as:

$$P_{A_y}(t) = \sum_{x=1}^{N} A_x e^{j(\omega_x t - y\frac{2\pi d}{\lambda}\cos\theta_x)} \quad = \sum_{x=1}^{N} A_x e^{j(\omega_x t - y\pi\cos\theta_x)} \tag{4.3}$$

In this equation, A_x and ω_x denote the amplitude and angular frequency of the signal originating from beam x, respectively. The received multi-beam signals then pass through the phase shifters, which apply a time-varying phase response modeled as $e^{j\varphi_y}(t)$. The phase response dynamically cycles through a set of discrete values, transitioning from φ_{y1} to φ_{yN} within each switching period $1/f_{SW}$, as illustrated in Fig. 4.13. The $e^{j\varphi_y}(t)$ can be expressed as the sum of N time-modulated constant phase responses, as Eq. 4.4:

$$\begin{aligned}
\varphi_y(t) &= \sum_{z=1}^{N} e^{j\varphi_{yz}} f_z(t) \\
&= \sum_{z=1}^{N} e^{j\varphi_{yz}} [\frac{1}{N} + \sum_{k=1}^{\infty} \frac{2}{k\pi} \sin(\frac{k\pi}{N}) \cos(\frac{2k\pi t}{T} - \frac{2k\pi z}{N})], \\
f_z(t) &= \begin{cases} 1, (k + \frac{z-1}{N})T \leq t \leq (k + \frac{z}{N})T, k \in \mathbb{Z} \\ 0, otherwise \end{cases}
\end{aligned} \tag{4.4}$$

where z represents the index of time slot (where $1 \leq z \leq N$). Here, z is used to represent the number of terms to distinguish it in the following equations. Although x and z share the same range of values, x represents the beam, while z represents the time slot in the time domain. The signals at point B, after undergoing time-variant phase shifting, can be expressed by Eq. 4.5:

$$P_{B_y}(t) = P_{A_y}(t)\varphi_y(t) = \sum_{x=1}^{N}\sum_{z=1}^{N} A_x e^{j(\omega_x t - y\pi\cos\theta_x + \varphi_{yz})}[\frac{1}{N} + \sum_{k=1}^{\infty}\frac{2}{k\pi}\sin(\frac{k\pi}{N})\cos(\frac{2k\pi t}{T} - \frac{2k\pi z}{N})] \tag{4.5}$$

Assuming the main lobe of all beams located at the null of all other beams, the beamformed signal at point C after power combining can be calculated as Eq. 4.6 when φ_{yx} is set equal to $y\pi cos\theta_x$.

$$\begin{aligned} P_C(t) &= \sum_{y=1}^{M} P_{B_y}(t) = \sum_{x=1}^{N} MA_x e^{j\omega_x t} f_x(t) \\ &= \sum_{x=1}^{N} MA_x cos(\omega_x t) f_x(t) \end{aligned} \tag{4.6}$$

After power combining, the beamformed signal for each beam is allocated to its corresponding time slot, while being suppressed in all other time slots. Intuitively, in the time domain, the signals at point C can be viewed as a sum of non-overlapping, periodically sampled beams (beam 1 through N), each with beamforming gain. The duty cycle of each sampled beam is $1/N$. To separate the signals from various beams in $P_C(t)$ and route them to their corresponding output ports, periodic windowed sampling functions with specific timing offsets are applied to the TD-MIMO switch to perform time-division de-multiplexing. The sampling function for beam x at output port x (where $1 \leq x \leq N$) is given by Eq. 4.7 as follows:

$$S_x(t) = f_x(t) = \frac{1}{N} + \sum_{k=1}^{\infty}\frac{2}{k\pi}\sin(\frac{k\pi}{N})\cos(\frac{2k\pi t}{T} - \frac{2k\pi x}{N}) \tag{4.7}$$

After the time-division de-multiplexing, the signal at point D to output port x (where $1 \leq x \leq N$) can be expressed by Eq. 4.8:

$$\begin{aligned} P_{D_x}(t) &= P_C(t)S_x(t) \\ &= [\sum_{z=1}^{N} MA_z cos(\omega_z t) f_z(t)] f_x(t) \\ &= MA_x cos(\omega_x t) f_x(t), \\ since\ f_z(t)f_x(t) &= \begin{cases} f_x(t), z = x \\ 0, z \neq x \end{cases} \end{aligned} \tag{4.8}$$

From Eq. 4.8, it is evident that all beams are fully separated and routed to their corresponding output ports without any crosstalk between different beams. The precondition

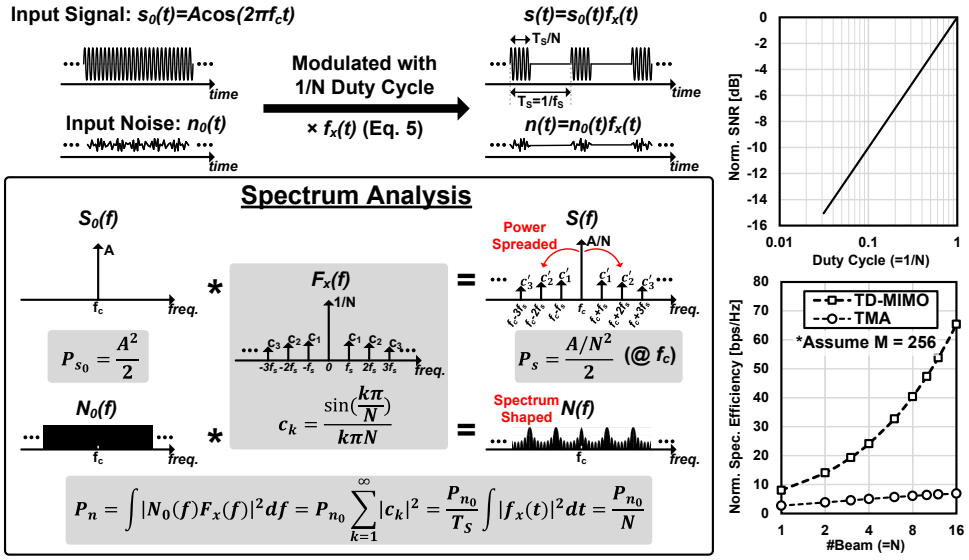


Figure 4.14: SNR analysis of duty cycle modulated RF signal.

for achieving this N-input N-output MIMO system is that all beams must be isolated. For a 1-D array with size of M, there are $M-1$ notches across the beam pattern, allowing a maximum of $M-1$ beams to be isolated from each other. The main lobe of the beam pattern to receive each beam is positioned at the nulls of the other beam patterns, ensuring that it does not receive signals from unintended beams. In modern millimeter-wave massive MIMO systems, the array size M is usually much larger than beam amount N, which ensures the feasibility of TD-MIMO.

The output signals of the proposed TD-MIMO receiver are time-modulated with a duty cycle of $1/N$. Similarly, the signals in the TMA also undergo a reduction in duty cycle. Fig. 4.14 illustrates the impact of this reduced SNR on the RF signal in both the time and frequency domains, which has also been discussed in [125]. Due to the spread spectrum effect introduced by time modulation, the signal power P_s at the operating frequency f_c experiences a degradation of $20\log N$ dB, while the full-band noise power P_n only decreases by $10\log N$ dB. Consequently, each beam suffers a $10\log N$-dB SNR loss during TD-MIMO operation. However, despite the SNR degradation, the overall spectral efficiency improves as the number of beams N increases. It is important to note that the spectral efficiency of TD-MIMO benefits from a larger array size M, while the TMA experiences only limited improvement due to degradation in its array factor, which will be analyzed in subsequent subsection. In practice, communication standards typically require a moderate SNR level for certain modulation schemes, making it advantageous to trade some excess SNR margin for higher data throughput.

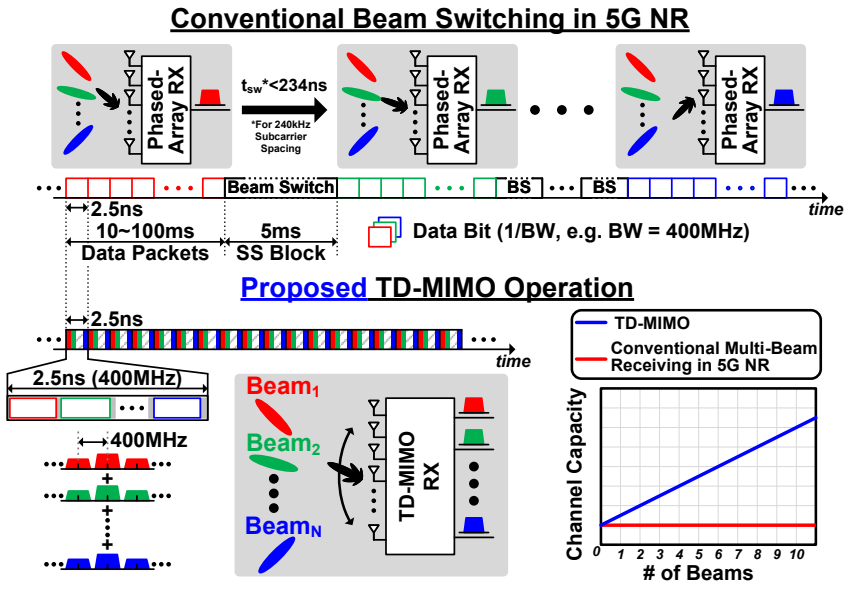


Figure 4.15: Data-bit level comparison between proposed TD-MIMO and conventional multi-beam communication with beam switching in 5G NR.

While the proposed TD-MIMO operation relies on very-fast beam switching, it fundamentally differs from conventional multi-beam communication based on existing standards. Fig. 4.15 compares the proposed TD-MIMO with beam-switching multi-beam communication in 5G NR. In 5G NR, beam switching occurs at the data packet level, with a single beam switch taking place within one signal synchronization block (SS block), resulting in only one switch in 5 ms [126]. To prevent inter-symbol interference, the beam transition time t_{SW} must be less than 80% of the cyclic prefix, which typically spans several hundreds nanoseconds [1, 28, 127]. Consequently, this form of multi-beam communication primarily increases the number of connected devices without enhancing effective channel capacity, as all beams share the same capacity. In contrast, TD-MIMO performs beam switching at the data-bit level. Each data bit from all beams is oversampled within a single data bit time (2.5 ns for a 400 MHz signal bandwidth), which allows the system's channel capacity to increase with the number of beams. Thus, the required t_{SW} must be very small. This Nyquist-rate beam switching makes TD-MIMO independent of any specific standard. By applying TD-MIMO operation, data throughput can be significantly improved across any communication standard.

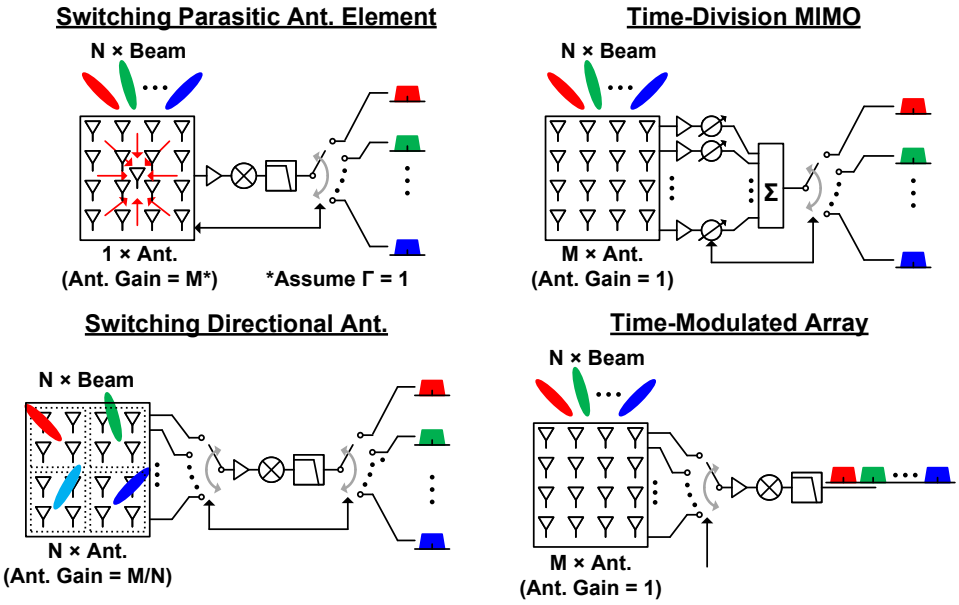


Figure 4.16: Multi-antenna MIMO receivers.

4.2.2 MIMO Phased-Array Receiver Comparison

In Section 4.1, various MIMO architectures that implement hardware multiplexing before the proposed TD-MIMO approach are introduced. A thorough comparison of these architectures is necessary to clarify their advantages and limitations. As discussed in Subsection 4.1.4, the block diagrams of switching parasitic antenna elements (PAE), switching directional antennas, TMA, and the proposed TD-MIMO are illustrated in Fig. 4.16. Conventional design of switching directional antennas and parasitic antenna elements, require specialized antenna designs. In contrast, beamforming does not impose such constraints and enables more efficient beam steering. However, for compact modules integrated with ICs, planar patch antennas on PCBs are often the only viable choice. Consequently, subarrays are used as an alternative to directional antennas. To optimize circuit area usage, time-division multiplexing is applied to both switching directional antennas and parasitic antenna elements. At any given time, only a single antenna receives signals in both the switching directional antenna and TMA solutions. For the switching directional antenna approach, antenna gain can be compensated by increasing the array size of the "directional antenna." However, the TMA solution lacks such compensation. In contrast, the parasitic antenna element method theoretically provides maximum antenna gain by leveraging all parasitic elements. However, for planar millimeter-wave antennas, the assumption of $\Gamma = 1$ is unrealistic. This results in unavoidable and significant antenna gain degradation

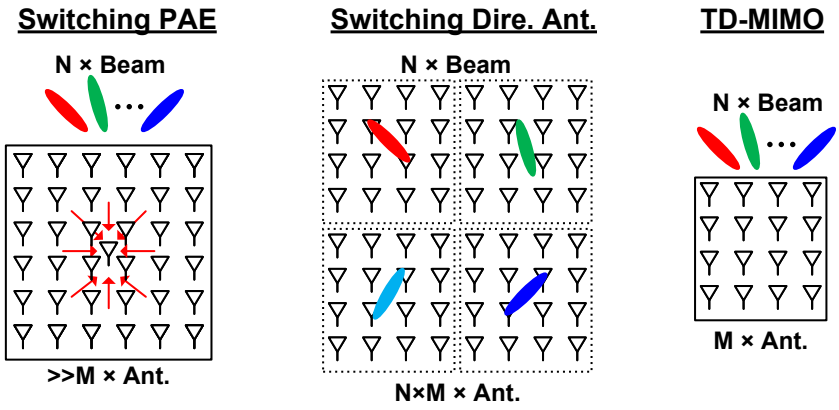


Figure 4.17: Hardware multiplexing MIMO receivers with same array factor.

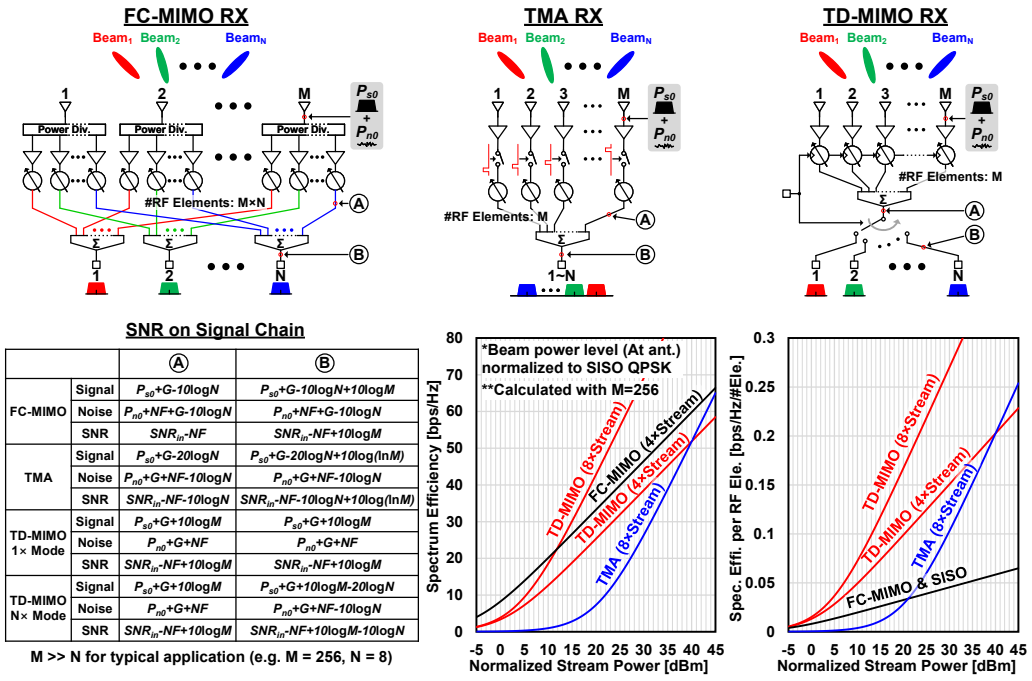
Table 4.2: Hardware cost comparison of hardware multiplexing MIMO receiver.

	#Antenna (Area)	#Beams	Array Factor	SNR
Switching PAE	$\gg$ M ($\Gamma \ll 1$ at mmW)	N	M	M/N
Switching Dire. Ant.	M × N	N	M	M/N
TMA	M	N	1	1/N
TD-MIMO	M	N	**M**	**M/N**

in the switching PAE solution.

To further illustrate the packaging size limitations of switching PAE [122] and switching directional antenna solutions [125] at millimeter-wave frequencies, Fig. 4.17 compares the required antenna arrays of these approaches with the proposed TD-MIMO architecture, ensuring all achieve the same array factor. When using subarrays as directional antennas, the switching directional antenna approach becomes excessively bulky. Furthermore, due to the inherently low Γ ($\ll 1$) of planar antennas at millimeter-wave frequencies, the switching PAE solution requires significantly more antennas to achieve an array factor comparable to that of TD-MIMO.

Table 4.2 summarizes the hardware costs of the different hardware-sharing MIMO receiver architectures. Despite employing hardware multiplexing, conventional switching PAE and switching directional antenna solutions fail to reduce module area effectively at millimeter-wave frequencies. In next-generation portable communication devices, both area and power budgets are strictly limited, preventing the allocation of excessive resources to wireless systems. Although, in theory, conventional solutions can be scaled to support more MIMO streams, they are impractical within the constraints of limited system budgets. As a result, they lack true scalability for supporting higher-order MIMO



		Ⓐ	Ⓑ
FC-MIMO	Signal	P_{s0}+G-10logN	P_{s0}+G-10logN+10logM
	Noise	P_{n0}+NF+G-10logN	P_{n0}+NF+G-10logN
	SNR	SNR_{in}-NF	SNR_{in}-NF+10logM
TMA	Signal	P_{s0}+G-20logN	P_{s0}+G-20logN+10log(lnM)
	Noise	P_{n0}+G+NF-10logN	P_{n0}+G+NF-10logN
	SNR	SNR_{in}-NF-10logN	SNR_{in}-NF-10logN+10log(lnM)
TD-MIMO 1× Mode	Signal	P_{s0}+G+10logM	P_{s0}+G+10logM
	Noise	P_{n0}+G+NF	P_{n0}+G+NF
	SNR	SNR_{in}-NF+10logM	SNR_{in}-NF+10logM
TD-MIMO N× Mode	Signal	P_{s0}+G+10logM	P_{s0}+G+10logM-20logN
	Noise	P_{n0}+G+NF	P_{n0}+G+NF-10logN
	SNR	SNR_{in}-NF+10logM	SNR_{in}-NF+10logM-10logN

Figure 4.18: Theoretical performance comparison between FC-MIMO, TMA, and proposed TD-MIMO receiver.

configurations. In contrast, the proposed TD-MIMO architecture achieves real scalability, enabling support for additional MIMO streams without increasing hardware complexity, making it a more viable solution for future wireless systems.

As a result, analog beamforming-based MIMO such as FC-MIMO, PC-MIMO and TD-MIMO remains the only practical solution for high-performance, large-scale millimeter-wave MIMO communication. The RF performance of the proposed TD-MIMO is compared with conventional analog beamforming MIMO receiver architectures, including fully-connected MIMO and time-modulated arrays, as shown in Fig. 4.18. Although both TD-MIMO and TMA experience SNR degradation due to reduced duty cycles, the non-overlapping duty cycles of each RF element in TMA lead to an additional degradation in array factor ($AF_{TMA} = 10\log(\ln M)$) compared to standard phased arrays. In contrast, the proposed TD-MIMO retains its array gain. Consequently, TMA becomes unsuitable for large array sizes due to severely degraded SNR. While FC-MIMO provides optimal SNR improvement for each beam through beamforming, its physical layout limits flexibility in adapting to various wireless scenarios. The power divider at the RF input in FC-MIMO introduces a constant $10\log N$ loss in array factor, fixed by the layout and unchangeable. Conversely, the proposed TD-MIMO allows for easy adjustment of N through different

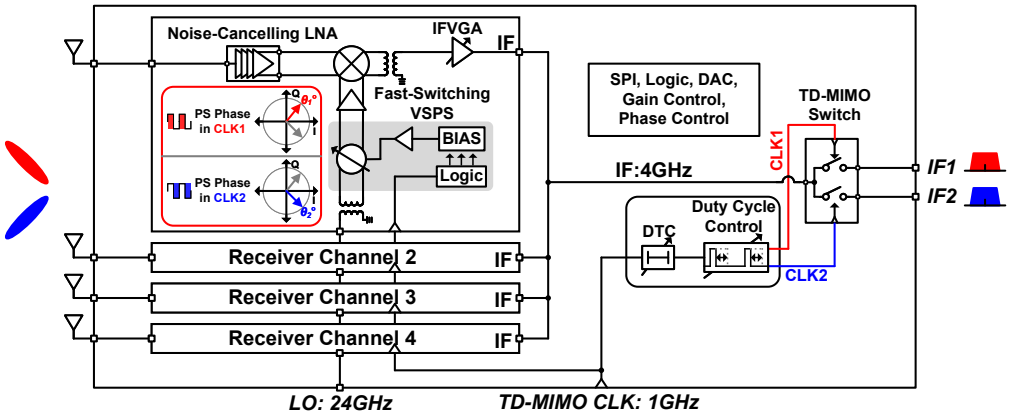


Figure 4.19: Block diagram of the initial version of TD-MIMO phased-array receiver operating at 28GHz.

beam-switching logic, enhancing sensitivity when operating with fewer beams. The spectrum efficiency per RF element of these MIMO receivers is also theoretically analyzed, assuming all beams have the same power level and that there are eight RF elements for simplicity. FC-MIMO achieves higher data rates by utilizing more RF elements, but its area efficiency remains the same a standard SISO phased-array receiver. On the contrary, both the proposed TD-MIMO and TMA significantly improve the spectrum efficiency without additional hardware overhead. However, the spectrum efficiency of the TMA is severely limited by its sensitivity degradation, while TD-MIMO achieves better spectrum efficiency with same beam due to less sensitivity loss. Furthermore, while the TD-MIMO receiver can achieve even higher spectrum efficiency by utilizing more concurrent beams, it can also be configured to improve sensitivity by reducing the number of beams. This flexibility makes the TD-MIMO receiver suitable for both high data rate and high sensitivity scenarios.

4.3 Circuit Implementation

4.3.1 Initial TD-MIMO Receiver Design

The block diagram of our first implementation of the TD-MIMO phased-array receiver is shown in Fig. 4.19. A key challenge in the TD-MIMO architecture is achieving a sufficiently high beam switching speed to ensure proper system operation. In the initial design, to achieve fast beam switching, compromises were made in terms of phase and amplitude

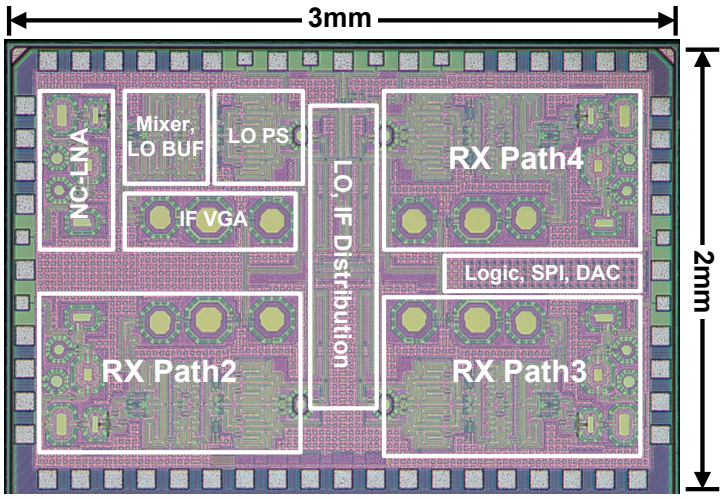


Figure 4.20: Chip micrograph of previous TD-MIMO phased-array receiver.

accuracy. To minimize beamforming performance degradation caused by gain and phase errors, an LO phase-shifting architecture was adopted. This choice allowed for fast beam switching with minimal errors and lower power consumption. In this design, digital-to-time converters (DTCs) were integrated to facilitate precise timing calibration, while Duty Cycle Control (DCC) units were introduced to generate non-overlapping timing signals, improving isolation between MIMO streams. Each antenna element (RF path) consists of a noise-canceling current-reuse LNA, a double-balanced mixer, a fast-switching LO VSPS, and an IF VGA. To demultiplex MIMO streams, a TD-MIMO switch and synchronized control circuit were implemented at the IF stage. The fabricated chip, shown in Fig. 4.20, was implemented using a 65nm CMOS process. Initial on-wafer measurements successfully demonstrated 2-stream MIMO reception, validating the feasibility of the TD-MIMO concept. However, several aspects required further improvement:

1. Building block performance: Both the noise-cancelling LNA and the fast-switching VSPS still require further enhancement to improve RF performance.

2. Over-the-air (OTA) verification: System-level validation with antennas and PCB design was necessary to fully assess real-world performance..

3. Scalability and efficiency limitations: The LO phase-shifting architecture introduced bulky LO distribution paths, which limited integration to only four antenna elements within a 3mm $\times$ 2mm area, undermining the area efficiency advantage of the TD-MIMO architecture.

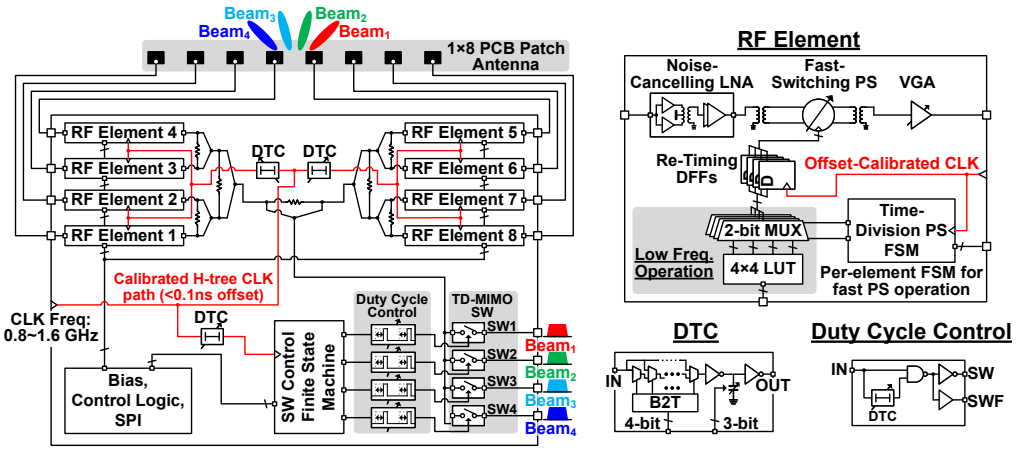
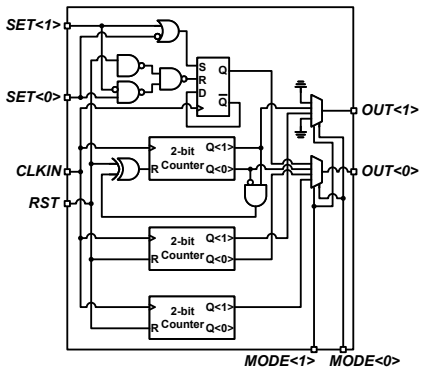


Figure 4.21: Block diagram of the updated TD-MIMO phased-array receiver.

4. Inter-chip complexity: The complex inter-chip LO distribution made the design unsuitable for large-scale multi-chip arrays, highlighting the need for a more scalable architecture.

4.3.2 Updated TD-MIMO Receiver Design

Building upon the insights gained from the initial design, extensive improvements were made to optimize the TD-MIMO phased-array receiver while retaining the fundamental system architecture. The block diagram of the updated 28-GHz TD-MIMO phased-array receiver is shown in Fig. 4.21. This enhanced version integrates eight antenna elements, significantly increasing system capacity while maintaining compactness and efficiency. To further improve power and area efficiency, RF phase-shifting architecture was adopted, offering better scalability for large multi-chip array systems. Compared to the LO phase-shifting approach in initial design, RF phase shifting reduces the complexity of inter-chip connections and allows for a higher level of integration within the same die area. Each RF element includes a noise-canceling current-reused LNA, a fast-switching PS, and a VGA. The control codes for the PS, enabling multiple beam configurations, are stored in a lookup table (LUT) and managed by a reconfigurable finite-state machine (FSM). As shown in Fig. 4.22(a), this FSM is designed to support various operation modes, ranging from SISO to 4-stream MIMO. The control codes for the corresponding beam are selected by the *OUT<1:0>* through the 2-bit multiplexer array. The truth table of the FSM for all operation mode is also provided in Fig. 4.22. After combining the signals with an 8-to-1 Wilkinson combiner, the beamformed signals from the eight elements are de-multiplexed



Mode	OUT<1:0>	f_{OUT}	MODE<1:0>	SET<1:0>
4-Stream	00 → 01 → 10 → 11 → 00	f_{CLK}	01	10
3-Stream	00 → 01 → 10 → 00	f_{CLK}	00	10
2-Stream	00 → 01 → 00	f_{CLK}	10	10
2-Stream	00 → 01 → 00	$\frac{f_{CLK}}{2}$	11	10
SISO	00	N/A	10	00
SISO	01	N/A	10	01

Figure 4.22: Circuit implementation and truth table of the proposed multi-mode time-division PS FSM.

by a 4-way TD-MIMO switch, synchronized with the beam switching performance. The time-domain beam switching and de-multiplexing operations for all modes are explained in detail in Fig. 4.23. Both the FSM and the TD-MIMO SW are driven by an external clock. The on-chip synchronization clock is distributed via a transmission-line-based H-tree network to each receiver element. Additionally, DTCs and DCC units are integrated for accurate timing calibration and enhanced stream-to-stream isolation, and a re-timing D-Flip-Flop (DFF) array is employed to synchronize beam switching timings with the offset-calibrated clock. Fig. 4.24 presents the circuit and measurement results of the proposed DTC and DCC unit. The DTC consists of a 4-bit path-selection coarse unit and a 3-bit variable-slope fine unit, balancing both area efficiency and resolution [128]. The DCC is implemented using a rising-edge delay generated by the DTC. The measured coarse and fine steps of the DTC are 30ps and 5ps, respectively, with a total range of 0.5ns. The measured duty cycle tuning range is 33% to 45% in 2-stream mode, and 12% to 21% in 4-stream mode.

4.3.3 Fast-Beam Switching

Both the beam-switching frequency and the beam-switching transition time are critical for enabling TD-MIMO operation. The beam-switching frequency must meet the Nyquist criterion, while a short transition time helps prevent sensitivity loss and degradation in EVM performance. Fig. 4.25 compares conventional beam switching technique with the proposed fast beam switching in this work. Conventional beam switching technique is usually utilized for UE scan in millimeter-wave communication since the narrow beamwidth for large-scale array. The beam-table-based beam switching stores the multi-beam phase-

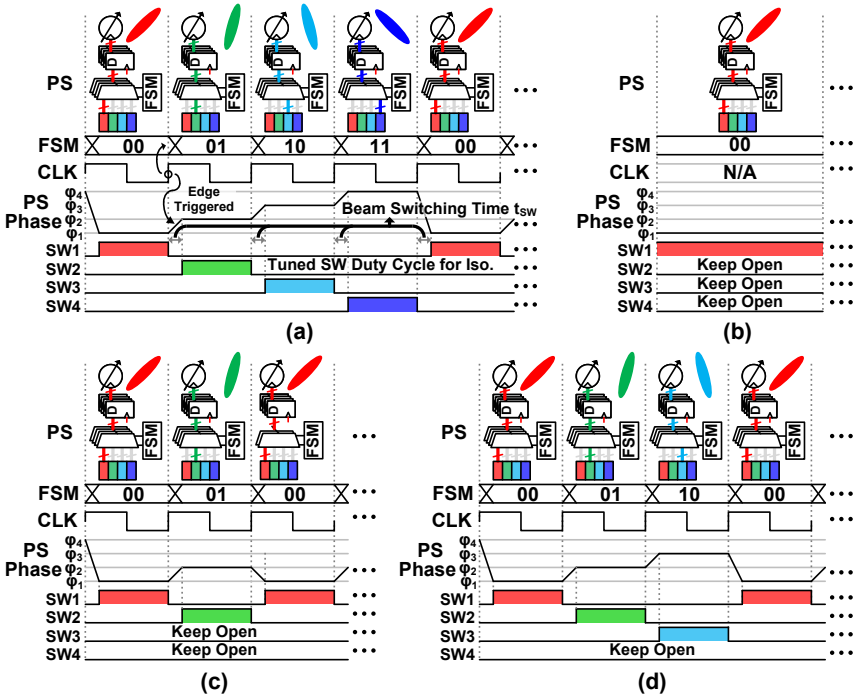
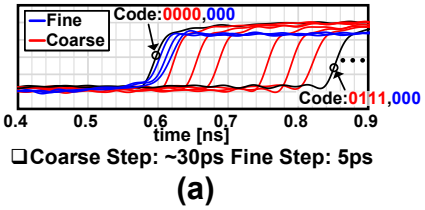


Figure 4.23: Beam switching logic in time-domain for (a) 4-streams MIMO mode, (b) SISO mode, (c) 2-stream MIMO mode, and (d) 3-stream MIMO mode



#MIMO Stream	SW Freq.	CLK Freq.	SW Duty Cycle Tuning Range
2×	0.4GHz (2.5ns)	0.8GHz	0.9ns – 1.15ns (33% - 45%)
4×	0.4GHz (2.5ns)	1.6GHz	0.3ns - 0.53ns (12% - 21%)

(b)

Figure 4.24: (a) Measured time-domain waveform of DTC. (b) Measured duty cycle tuning range.

settings in a LUT, reducing the data rate demands on the digital interface [117, 129]. However, the size of the LUT is constrained by the chip area. In [1], an on-chip calculator (OCC) replaces the beam table. The OCC can calculate the phase control code with the desired beam angle, hence supports much more beams than the beam-table-based beam switching without consuming large area. However, the beam-switching frequency in both beam-table-based and OCC beam switching is constrained by the digital interface. For typical millimeter-wave system technology, the distributed digital bus operates at less

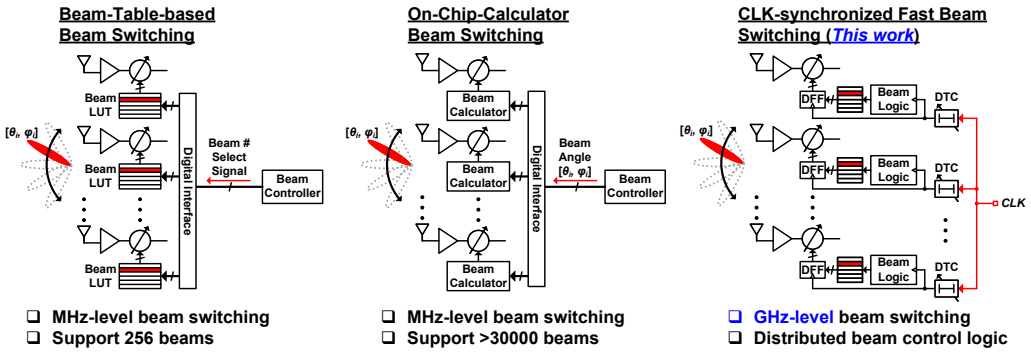


Figure 4.25: Comparison of conventional and proposed beam switching technique.

than 100 MHz. Additionally, the analysis in Sec. II-B demonstrates that the required beam transition time t_{SW} in 5G NR is far too short to meet the demands of TD-MIMO operation. In contrast, the proposed clock-synchronized beam-table-based fast beam switching eliminates the need for a high-speed digital interface. Each element includes a beam control FSM placed in close proximity to the LUT and PS. The GHz-level clock can be more easily distributed and calibrated in large systems compared to a digital interface, while the re-timing operation using the synchronized clock mitigates inter-element timing mismatches caused by the high-frequency operation of the beam control circuit.

Although the beam switching frequency is significantly improved by the proposed clock-synchronized fast beam switching technique, the beam transition time is influenced not only by the control circuit but also by the PS itself. Fig. 4.26 compares voltage-controlled PS (VCPS) and digital-controlled PS (DCPS) for fast switching applications. VCPS, including VGA-based vector-modulated PS (VMPS) and reflection-type PS (RTPS), are commonly used in phased arrays due to their high resolution and simple core circuitry. However, the analog biasing voltage is usually unable to quickly drive the large varactor or RF transistor in the PS. To achieve fast voltage switching, high-performance op-amp is required as a driver buffer. Nonetheless, the low supply voltage of advanced technologies limits the op-amp's gain bandwidth (GBW) and slew rate (SR), regardless its increasing power consumption. On the other hand, DCPS, such as switched-type PS (STPS), variable-delay transmission line (VDTL), and digital-controlled VMPS, use digital buffers to drive the RF switches in the PS. These digital buffers offer much higher power efficiency than analog voltage buffers and operate effectively with low supply voltages. The transient performance of voltage switching and digital code switching is also simulated and compared in Fig. 4.26. With a 1V supply and 2-mW P_{DC}, an op-amp optimized for GBW and SR achieves a switching transition time t_{SW} of 0.6ns when

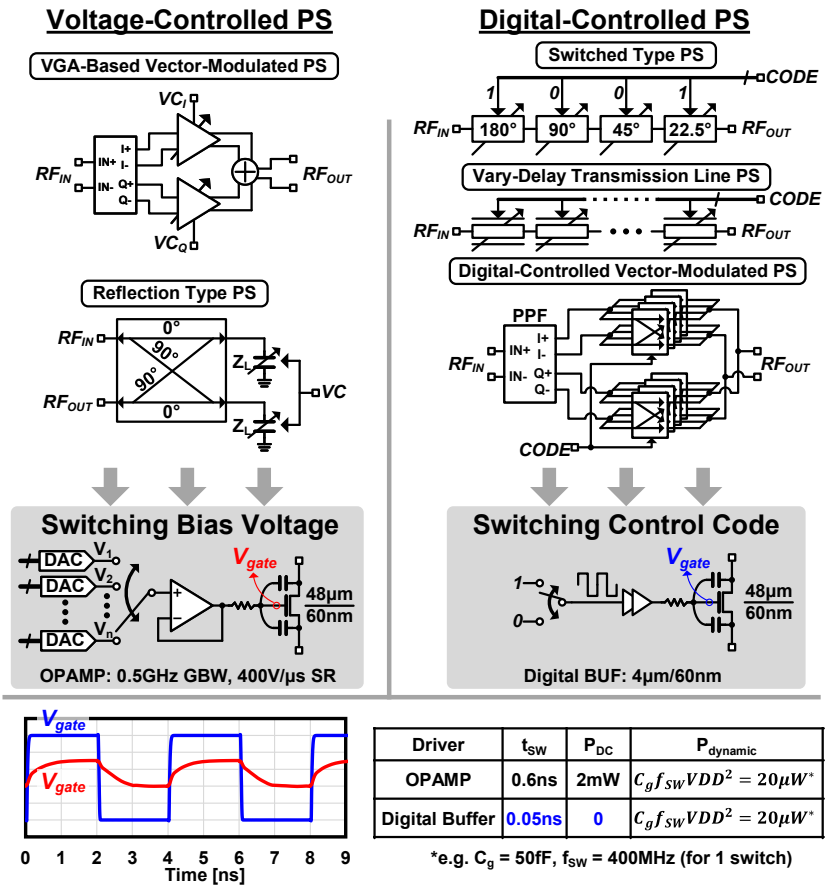


Figure 4.26: Transient performance analysis of voltage-controlled PS and digital-controlled PS

driving a 48μm/60nm transistor. Further increasing the P_{DC} of op-amp yields diminishing performance improvement, and it remains impractical to reduce the t_{SW} to 0.1-ns level. In contrast, a small digital buffer can switch the same transistor with a much faster t_{SW} of 0.05-ns. Moreover, the additional dynamic power dissipation from digital buffer can be negligible.

To further illustrate the limitations of the voltage-controlled approach, Fig. 4.27 (a) shows the circuit implementation of the fast-switching VSPS in the initial version of the TD-MIMO receiver. Due to the absence of a mixed-signal control module, a voltage-controlled PS was selected. The vector-summing architecture was adopted for its compact size and fine resolution capabilities. To enable fast beam switching, the control words of the I/Q VGAs for different beam settings were stored in separate RDACs (resistor digital-to-analog converters), with additional biasing buffers incorporated to accelerate

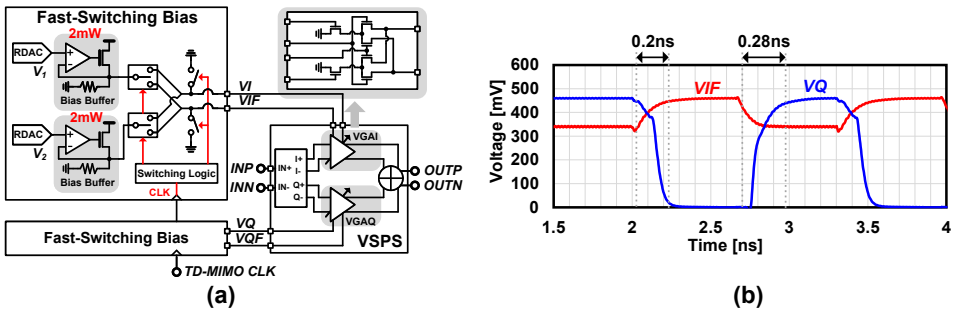


Figure 4.27: (a) The voltage-controlled VSPS in previous TD-MIMO receiver. (b) Simulated transient response of the biasing voltage.

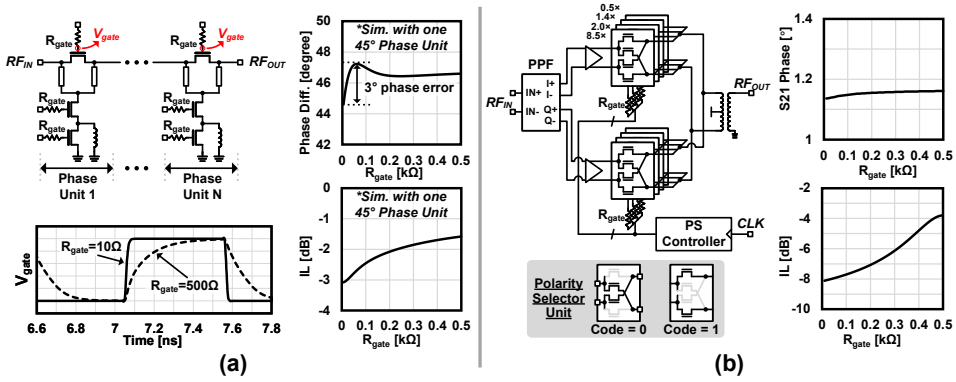


Figure 4.28: (a) The impact of SW gate biasing resistor in conventional STPS. (b) Proposed digital-controlled vector-modulated PS supporting fast switching in updated TD-MIMO receiver design.

the switching speed. To further optimize power consumption, a quadrant selector was employed, effectively reducing the number of required biasing buffers and RDACs by half. The measured switching speeds between the off-state and 45°-state were 0.2 ns and 0.28 ns, respectively, under a 24-GHz LO and a 400-MHz clock frequency, as shown in Fig. 4.27 (b). However, further reduction in switching transient time can only be achieved by increasing power and area allocation for the biasing buffer design, which poses a significant trade-off. Additionally, the voltage-controlled VSPS architecture is inherently susceptible to process, voltage, and temperature (PVT) variations, as well as device mismatches, which can severely impact beamforming accuracy and system performance.

In a DCPS, minimizing the RC time constant is crucial for achieving a shorter t_{SW}. While the transistor size cannot be too small in order to maintain RF performance, the

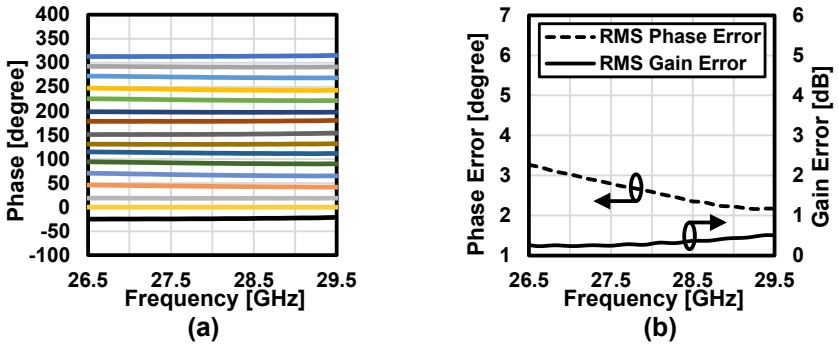


Figure 4.29: Measured (a) phase map and (b) phase and gain error of the proposed fast-switching vector-modulated PS.

large gate biasing resistor used in the switches can be eliminated for faster switching applications. A typical STPS is shown in Fig. 4.28(a) to analyze the impact of the gate biasing resistor R_{gate}. While reducing the R_{gate} can significantly shorten the t_{SW}, it also makes the phase response of the RTPS unit unstable and highly sensitive to R_{gate} when R_{gate} is small, due to the single-ended signal path. The STPS units are separated in layout due to their large area. The unavoidable long biasing wires introduce unpredictable parasitic R_{gate}, leading to substantial mismatches between units. Simulations show that R_{gate} variance causes a phase error of 3° for a single 45° unit. Additionally, the simulated insertion loss (IL) of the 45° unit increases due to lower impendence to ground. Given the series architecture, the cumulative phase error and insertion loss become significantly larger and more unpredictable. As a result, both STPS and VDTL are unsuitable for fast switching applications. To resolve the issues discussed above, this work employs a digital-controlled VMPS, as shown in Fig. 4.28(b). Two VM switch arrays are utilized to weight the IQ signals generated from a passive polyphase filter (PPF), enabling full 360° phase coverage with 22.5° phase step. Each array consists of 4-bit parallel polarity selector units with predefined weight ratios, producing normalized gains of ±1, ±0.92, ±0.707, ±0.38, and 0. The constant output impedance of the polarity selector unit minimizes phase and gain variations [56]. Since the VM switch arrays are compact and centralized, the digital buffers can be placed closed to each polarity selector unit, minimizing parasitic R_{gate}. The fully-differential signal path ensures stable phase response regardless of R_{gate}. Although the insertion loss increases, it is acceptable and not cumulative as in the STPS, allowing the removal of biasing resistors in the binary units to achieve a shorter t_{SW}. With the calibrated PPF [22], the measured RMS phase and gain error of the proposed phase shifter are showed in Fig. 4.29, with values of 2.5° and 0.4dB at 28GHz, respectively.

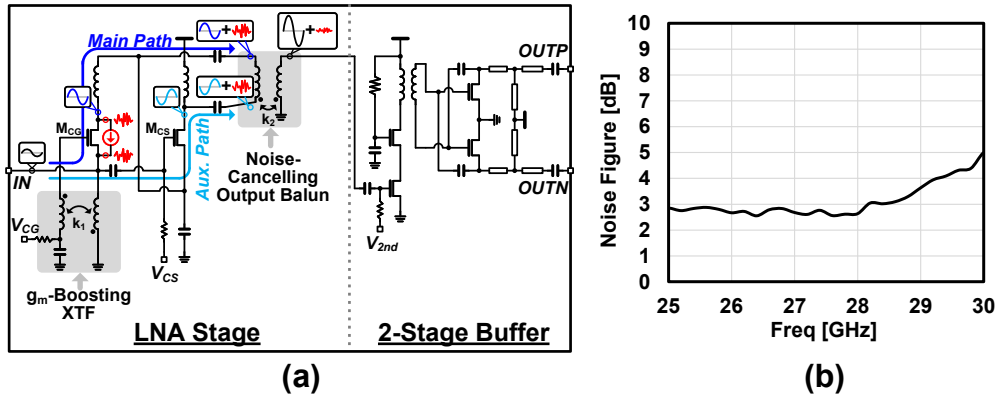


Figure 4.30: (a) Initial version of the proposed current-reused noise-cancelling LNA with g_m-boosting in previous TD-MIMO receiver. (b) Measured noise figure of noise-cancelling LNA.

4.3.4 Current-Reuse Noise-Cancelling LNA

As discussed in Section II, the sensitivity directly decides the RF performance of MIMO receivers. To address sensitivity challenges in the TD-MIMO receiver, the initial design incorporated an XTF-based low-noise amplifier (LNA) stage, shown in Fig. 4.30(a), utilizing a noise-cancelling technique to minimize the system NF. The noise-cancelling XTF cancels noise from the CG transistor in the main path by combining it with in-phase noise from the CS transistor in auxiliary path at the output side while strengthening the combined signal [130, 131]. To overcome noise-cancelling performance degradation due to CG stage gain at high frequencies, a g_m-boosting XTF is employed. Besides, the g_m-boosting effect on the input impedance allows smaller M_{CG} size while maintaining wideband 50-Ω input matching without high order network [132]. The g_m-boosting technique also reduces the power consumption of the CS stage while achieving relatively high total gain. Current-reuse technique is introduced to further reduce power consumption overhead from the CS stage. The inverted signal and in-phase noise from the CG main path and the CS auxiliary path are combined using an output balun. A two-stage buffer is added after the noise-cancelling LNA stage to enhance gain and suppress noise in the subsequent signal path. The output stage is designed as a differential CS stage to improve output linearity and optimize the connection to the mixer. As shown in Fig. 4.30 (b), the measured minimum NF is 2.5 dB at 27.5 GHz and remains below 3 dB across the 24.5 GHz to 28.5 GHz range.

Despite these advantages, the auxiliary CS stage in the initial design required a dedi-

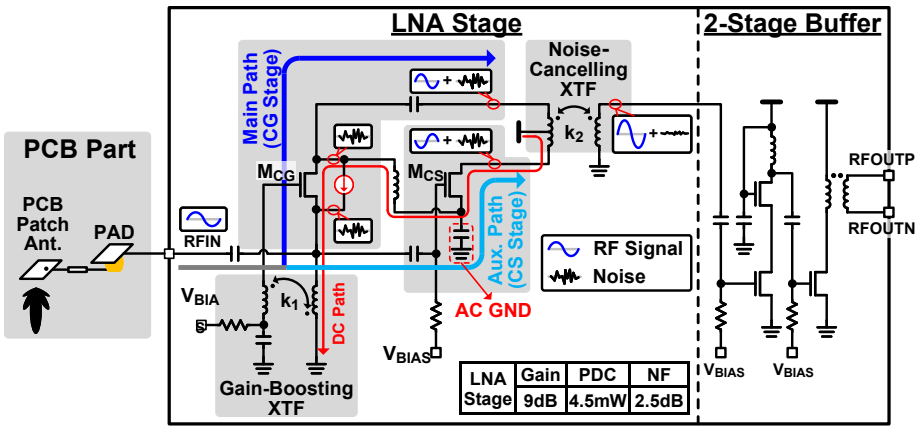


Figure 4.31: Circuit implementation of the proposed current-reused noise-cancelling LNA with g_m-boosting.

cated load inductor to connect to the supply voltage. This not only increased the overall chip area but also introduced additional noise due to parasitic effects. In the updated TD-MIMO phased-array receiver, the noise-cancelling LNA topology was further optimized, as depicted in Fig. 4.31. In the revised design, the CS and CG stages continue to share a common output balun. However, to further reduce chip area, the CS stage now utilizes the balun's center tap as the power supply connection. This modification significantly reduces the required layout area while maintaining the desired performance characteristics. A stand-alone version of the updated current-reused noise-cancelling LNA was fabricated and evaluated through on-wafer measurements. The results demonstrate a gain of 9 dB and an NF of 2.5 dB at 28 GHz, with a low power consumption of 4.5 mW. Compared to the initial design, the updated LNA achieves a consistently lower NF across a broader frequency range while achieving a smaller chip area, making it a highly area-efficient solution.

4.4 Measurement Results

The proposed chip TD-MIMO phased-array receiver is fabricated in a 65nm Bulk CMOS process. The chip micrograph is presented in Fig. 4.33. The proposed receiver only occupies a compact 3mm $\times$ 2mm area with eight RF elements. In the measurement, a standalone single RF element chip is used to evaluate RF performance. It achieves an 18-dB gain and 2.9-dB NF at 28GHz as shown in Fig. 4.34. The measured input P1dB of single RF element is -30dBm (Fig. 4.34(c)), which ensures sufficient dynamic range for

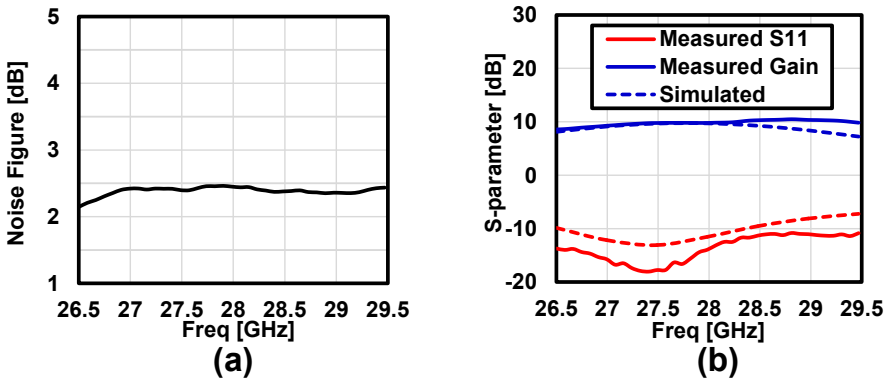


Figure 4.32: Measured (a) noise figure and (b) S-parameters of the proposed noise-cancelling LNA (without following 2-stage buffer).

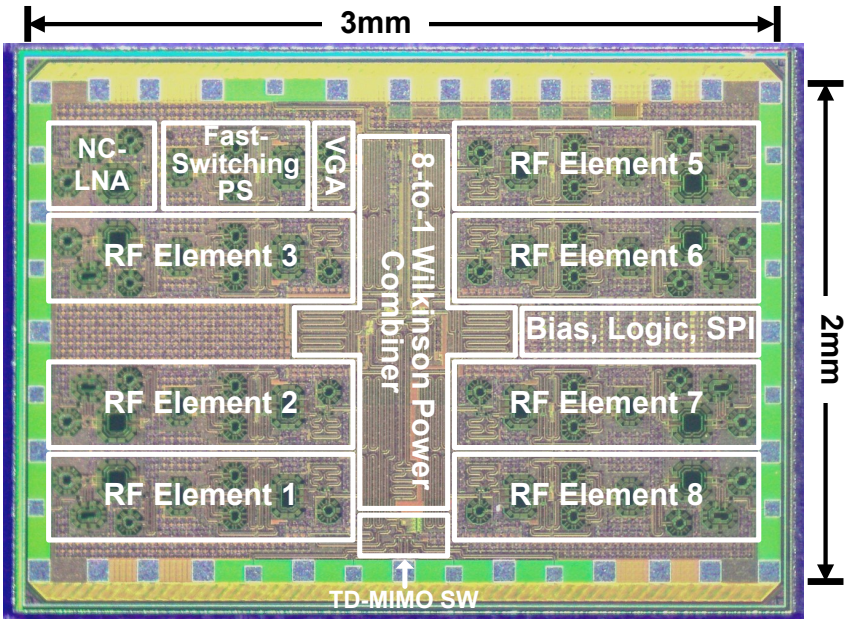


Figure 4.33: Chip micrograph.

millimeter-wave applications. The EVM versus input power of the single RF element are also evaluated using a 400-MHz bandwidth 5G standard-compliant modulated signal in OFDMA mode, depicted in Fig. 4.34(d).

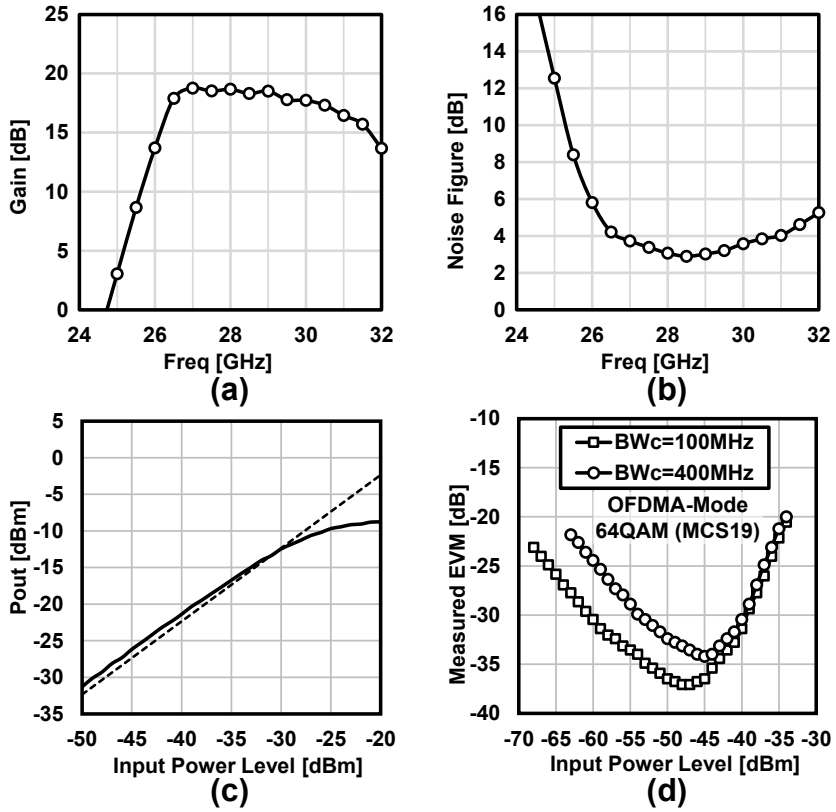


Figure 4.34: (a) Measured gain with single receiver channel. (b) Measured NF of single receiver channel. (c) Measured input P1dB of single receiver channel. (d) Measured Pout vs. Pin of single receiver channel.

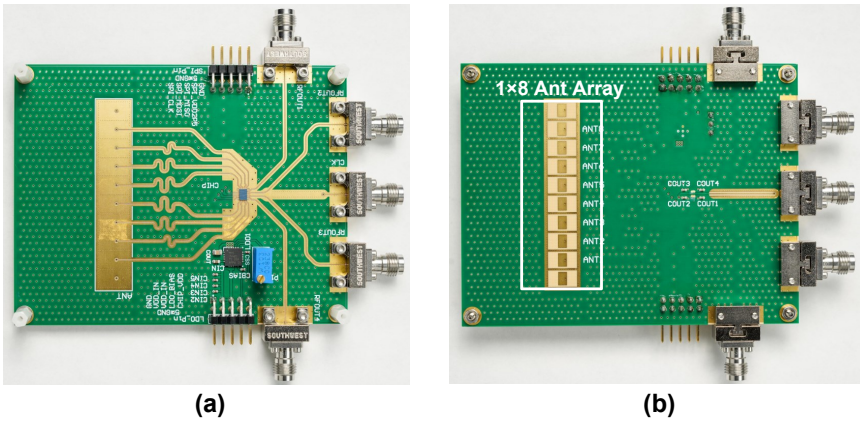


Figure 4.35: (a) Top side PCB photo. (b) Bottom side PCB photo.

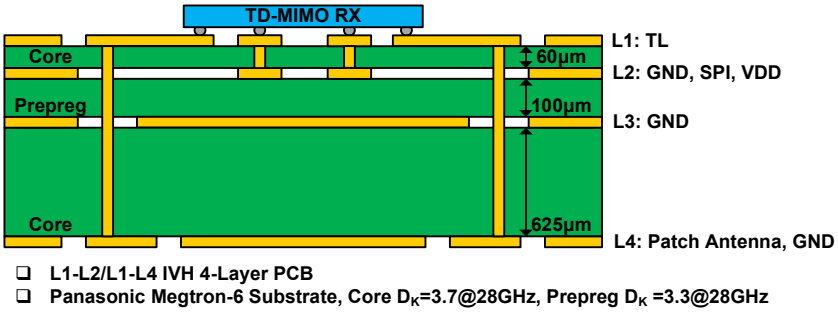


Figure 4.36: 4-Layer PCB stack configuration.

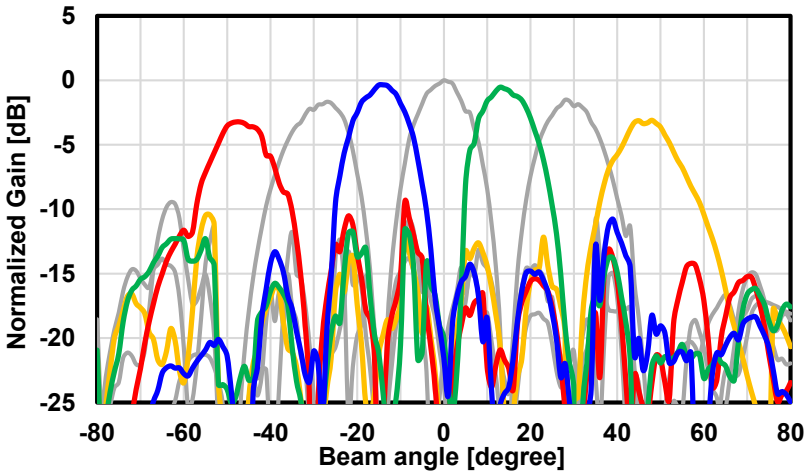


Figure 4.37: Measured beampattern of the proposed TD-MIMO receiver with PCB.

4.4.1 PCB Design

To perform over-the-air (OTA) communication and validate the TD-MIMO operation with an antenna array, the proposed TD-MIMO phased-array receiver is flip-chip assembled onto a PCB. The PCB features a 1×8 patch antenna array on its backside, as shown in Fig. 4.35. To ensure beam pattern precision, two dummy patch antennas are added on either side of the array. The PCB stack configuration is depicted in Fig. 4.36. This four-layer PCB employs L1-L2 blind vias, L1-L4 interstitial via holes (IVH), and uses a Panasonic Megtron-6 substrate. The measured beam patterns of the 1×8 element array in the azimuth plane are shown in Fig. 4.37, demonstrating a sidelobe level suppressed to -10 dB without tapering.

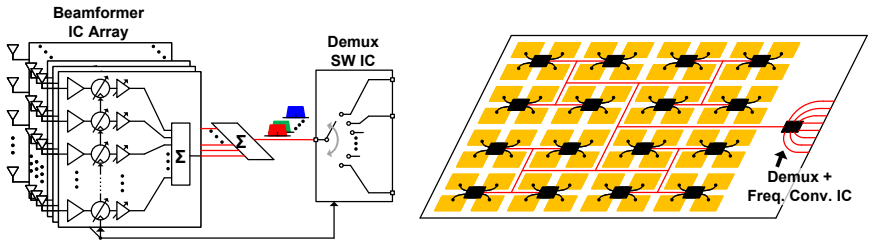
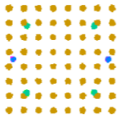
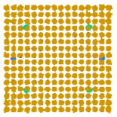


Figure 4.38: Large-scale multi-chip array solution for TD-MIMO.

Table 4.3: Measured SISO OTA constellations and EVMs of proposed TD-MIMO receiver.

Freq.	28GHz	28GHz	28GHz	28GHz
Modulation*	QPSK (MCS3)	16QAM (MCS10)	64QAM (MCS19)	256QAM (MCS27)
Mode	OFDM SISO	OFDM SISO	OFDM SISO	OFDM SISO
BW_c	400MHz	400MHz	400MHz	400MHz
Constellation				
EVM (RMS)	-34.4dB (1.91%)	-33.9dB (2.03%)	-33.8dB (2.05%)	-33.7dB (2.06%)

**5G NR MCS index table 2 for PDSCH (Table 5.1.3.1-2 in 3GPP TS 39.214 V16.1.0)

The TD-MIMO architecture allows for a simple single-wire inter-chip connection by separating the beamformer and de-multiplexer ICs, as illustrated in Fig. 4.38. After beamforming, all MIMO streams are time-division multiplexed, enabling them to share a single wire without mutual interference. Unlike conventional fully-connected MIMO systems, which require complex multi-layer PCBs, TD-MIMO only requires one additional PCB layer for routing the synchronization clock to each beamformer IC and the de-multiplexing switch IC. When the number of MIMO streams increases to meet future data rate demands, the PCB and beamformer IC remain unchanged. The only modification needed is replacing the de-multiplexing IC, making the TD-MIMO architecture highly scalable and ideal for next-generation high-performance receivers.

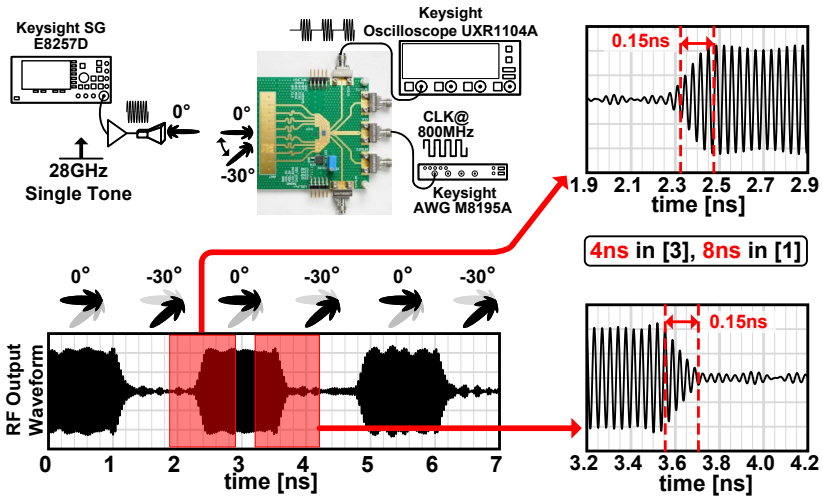


Figure 4.39: Measured beam switching time of proposed TD-MIMO receiver.

4.4.2 OTA Measurement Results

The OTA constellations and EVMs of the proposed receiver in SISO mode are measured using a 28GHz OFDM 5G modulated signal with 400-MHz bandwidth, transmitted from a horn antenna positioned at 0° azimuth. The results are summarized in Table 4.3, which shows the proposed receiver achieves a -33.7dB RMS EVM with 256QAM modulation. The beam switching speed of the proposed TD-MIMO receiver is then evaluated through OTA measurements. As explained in 4.39, the PCB is mounted vertically, with a horn antenna positioned directly in front of the antenna side at a 0° azimuth. A 28GHz continuous wave signal from a Keysight E8257D signal generator is fed to the horn antenna, while the TD-MIMO receiver is configured in 2-stream mode. The receiver's beam direction was periodically switched between 0° and -30° azimuth, driven by an external 800MHz clock generated from a Keysight AWG M8195A. The measured beam switching time is 0.15ns, significantly faster than previously reported results, such as 4ns in [117] and 8ns in [1].

The impact of sensitivity degradation caused by the TD-MIMO operation is evaluated through OTA measurements using a 400 MHz bandwidth, 64-QAM modulated signal (MCS17 in 5G NR OFDMA mode). Fig. 4.40(a) illustrates the measured RMS EVM across the duty cycle range, showing that the EVM degradation from the ideal value is limited to just 2.5dB at the worst-case scenario of 12% duty cycle, owing to the exceptionally fast beam switching speed. Although a 400 MHz switching frequency is the minimum requirement for a 400 MHz bandwidth modulated signal as dictated by the

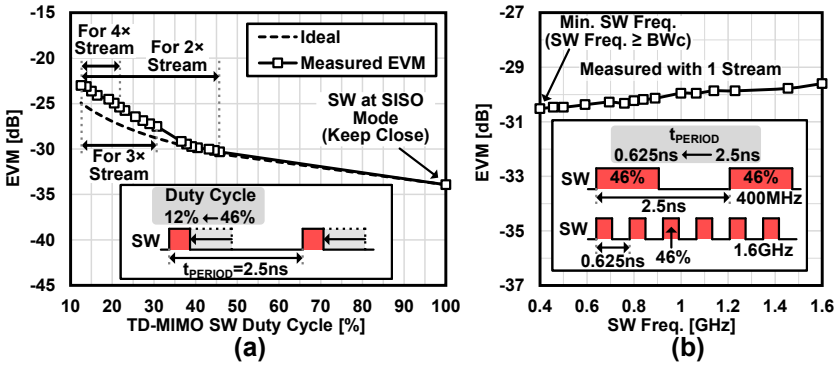


Figure 4.40: OTA measured EVMs vs. (a) TD-MIMO SW duty cycle and (d) switching frequency

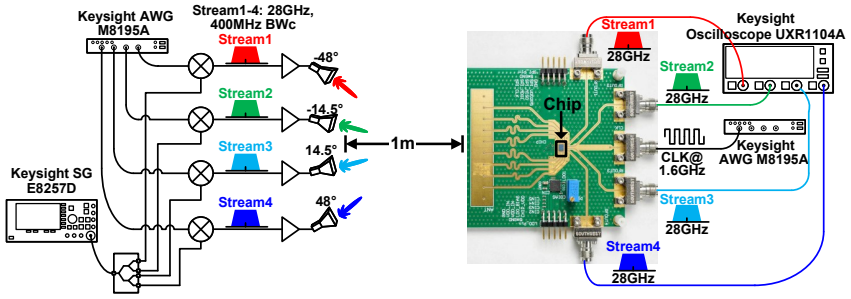
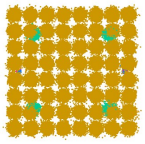
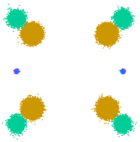
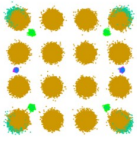
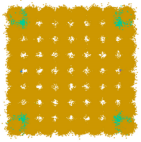


Figure 4.41: Equipment setup for MIMO constellations and EVMs measurement

sampling theorem, the RMS EVMs are also evaluated at higher switching frequencies, as shown in Fig. 4.40(b). The results indicate that EVM degradation at higher switching frequencies is negligible, confirming the TD-MIMO's capability to handle signals with larger bandwidths.

The equipments setup of multi-stream OTA measurement is shown in Fig. 4.41. EVMs are measured in both 2-stream and 4-stream MIMO modes of the proposed TD-MIMO receiver. In 4-stream mode, four 5G standard-compliant MIMO signals are generated using a Keysight M8195A AWG and transmitted from four horn antennas located at -48.5°, -14.5°, 14.5° and 48.5° azimuth. These beam directions are selected to ensure sufficient stream-to-stream isolation, as shown in the beam pattern in Fig. 4.37. For 2-stream mode, only two horn antennas positioned at -14.5° and 14.5° are used. The clock signal is generated by a second Keysight M8195A AWG, with both Keysight M8195A AWGs synchronized using a Keysight M8197A synchronization module. Constellations

Table 4.4: Measured MIMO OTA constellations and EVMs of proposed TD-MIMO receiver.

Mode	2×2 MIMO OTA	4×4 MIMO OTA		
Beam 1-4 Freq.	28GHz	28GHz	28GHz	28GHz
Beam 1-4 Modulation*	64QAM (MCS17) OFDMA Mode	QPSK (MCS4) OFDMA Mode	16QAM (MCS10) OFDMA Mode	64QAM (MCS17) OFDMA Mode
Beam 1-4 BW_c	400MHz	400MHz	400MHz	400MHz
CLK Freq.	800MHz	1.6GHz	1.6GHz	1.6GHz
Constellation**				
EVM (RMS)**	-25.7dB (5.2%)	-23.38dB (6.8%)	-23.32dB (6.8%)	-23.5dB (6.7%)

*5G NR MCS index table 1 for PDSCH is used (Table 5.1.3.1-1 in 3GPP TS 39.214 V16.1.0)
**Constellations and EVMs in TD-MIMO measurement are shown for 2/4 streams together (All layers).

and EVMs are measured by a Keysight UXR1104A oscilloscope. Remarkably, synchronization between the transmitter and receiver is unnecessary. The measured constellations and EVMs are summarized in Fig. 4.4. In 2-stream mode, the measured RMS EVM is -25.7dB in 64QAM modulation, with 800MHz clock frequency (400MHz SW frequency). In 4-stream mode, with 1.6GHz clock frequency (400MHz SW frequency), the measured RMS EVMs are -23.4dB, -23.3dB, and -23.5dB in QPSK, 16QAM, and 64QAM, respectively.

Table 4.5: Performance Comparison of MIMO Receivers

		This work	IBM [1]	Tokyo Tech [117]	CMU [15]	ZJU [116]	Georgia Tech [113]
Process		65nm CMOS	130nm SiGe	65nm CMOS	65nm CMOS	65nm CMOS	45nm SOI
Frequency		26.5 ~ 29.5GHz	24 ~ 30GHz	26.5 ~ 29.5GHz	25 ~ 30GHz	27.5 ~ 32GHz	26 ~ 33GHz
Noise Figure (SISO)		**2.9 ~ 3.4dB**	3.1 ~ 3.9dB	5dB (Min.)	7.3dB (Min.)	3.7 ~ 4.5dB	5.8 ~ 7.7dB
# Antennas (M)		M=8	M=8H+8V	M=4H+4V	M=8	M=8	M=4
# MIMO Streams (N)		**N=4**	N=1	N=2	N=2	N=2	[a]N=2
MIMO Architecture		**Time-Division MIMO**	N/A (N=1)	Fully-Connected MIMO	Fully-Connected MIMO	Fully-Connected MIMO	Time-Modulated Array MIMO
Maximum # MIMO Streams per RF path		**N**	N/A	1	1	1	[a]N+1
Array Factor		M	M	M	M	M	1
Area per Element (Area/M)		0.4mm^2	0.6mm^2	1.7mm^2	[b]0.4mm^2	2.6mm^2	0.9mm^2
PDC per Element (PDC/M)		28mW for SISO 32mW for 4×Stream	90mW (RX)	79mW (RX)	43mW	140mW	66mW
Area per Element per Stream (Area/M/N)		**0.1mm^2**	0.6mm^2	0.85mm^2	0.2mm^2	0.67mm^2	0.45mm^2
PDC per Element per Stream (PDC/M/N)		**8mW**	90mW	39mW	21mW	35mW	15mW
# RF Output Interface for Multi-Chip Array		[c]1	N	N	N	N	1
Beam Transition Time		**0.15ns**	8ns	4ns	N/A	N/A	N/A
Max. Measured MIMO Data Rates		**9.6Gbps**	6.4Gbps	6.4Gbps	N/A	N/A	0.8Gbps
5G NR Standard-Compliant MIMO	**# Streams**	**4×**	N/A	2×	N/A	N/A	2×
	MIMO Modulation	64QAM OFDMA Mode 400MHz BWc	N/A	64QAM SC-FDMA 400MHz BWc	N/A	N/A	16QAM SC 100MHz BWc
	EVM	-23.5dB	N/A	-25.2dB	N/A	N/A	-21.1dB

[a]Maximum two streams are evaluated for MIMO in this work. [b]Estimated from paper. [c]When Using separated TD-MIMO de-multiplexing switch.

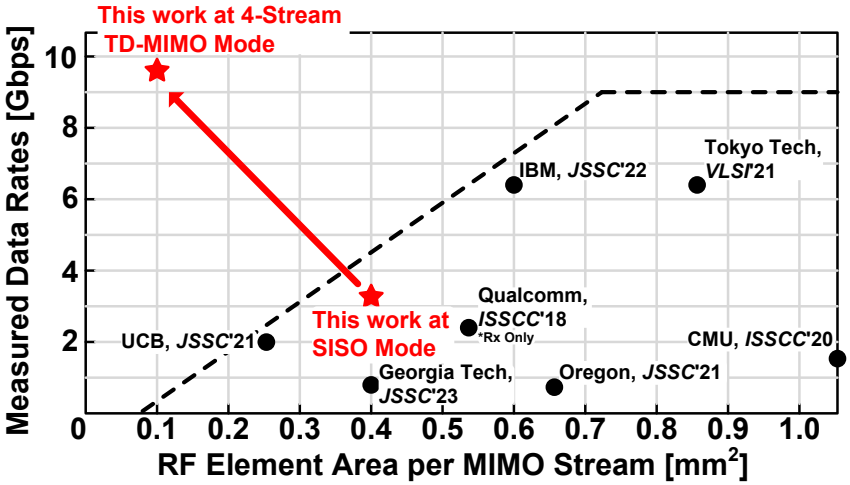


Figure 4.42: Data rates vs. RF element area per data stream of state-of-the-art millimeter-wave MIMO receivers

Table. 4.5 compares this work with other state-of-the-art millimeter-wave MIMO receivers [1, 15, 113, 116, 117]. Including the power consumption of the timing circuit, the PDC per element is 28mW on SISO mode and 32mW on 4-stream MIMO mode, respectively. The proposed TD-MIMO architecture shows large area and power advantage compared with other MIMO receivers. This work also shows the fastest beam-switching speed. Moreover, the proposed TD-MIMO receiver supports single-wire output, which benefits large-scale multi-chip arrays. Fig. 4.42 plots the data rates versus RF element area per data stream for millimeter-wave MIMO phased-array receivers, including this work [1, 12, 36, 111, 114, 117]. Among the listed MIMO receivers, this work achieves the highest data rates area efficiency in 4-streams MIMO mode.

4.5 Spectrum Aliasing of TD-MIMO

Fig. 4.43 categorizes and summarizes various blocker scenarios in phased-array receivers. In conventional receivers, the inherent band-pass filtering characteristics of the signal chain, combined with the spatial filtering capabilities of the beamformer, effectively suppress most interference. As a result, only blockers that share the same frequency and angle of arrival (Case 4) as the desired signal can directly interfere and significantly degrade the SNR. However, due to the limited linearity of the RF front-end, any strong blockers within the operational frequency range of the receiver can potentially compress the dynamic range, even if they do not coincide with the desired signal frequency. As

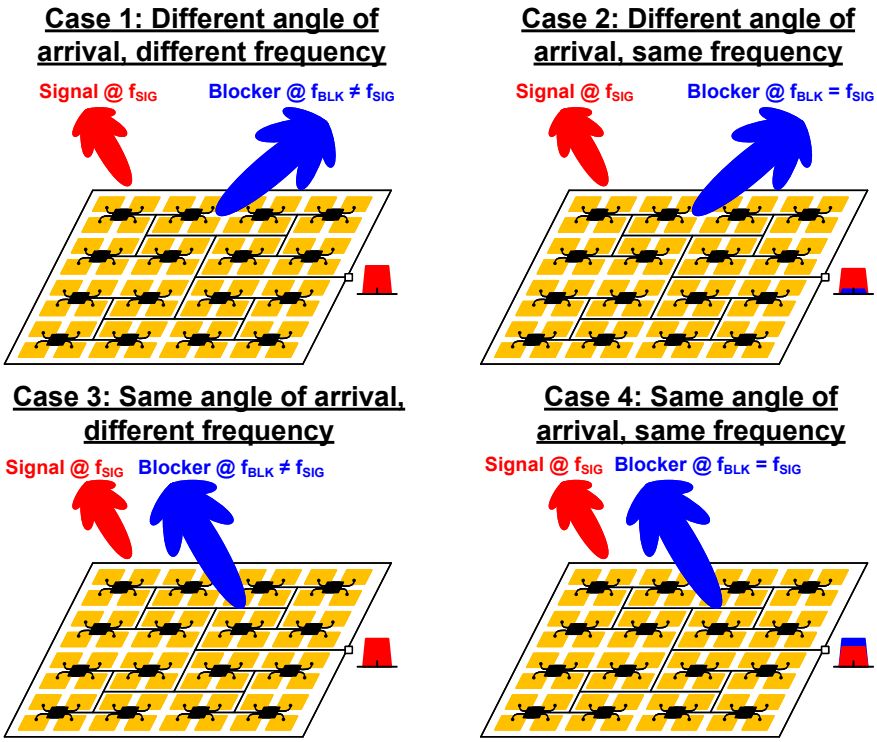


Figure 4.43: Blocker issue categorization for phased-array receivers

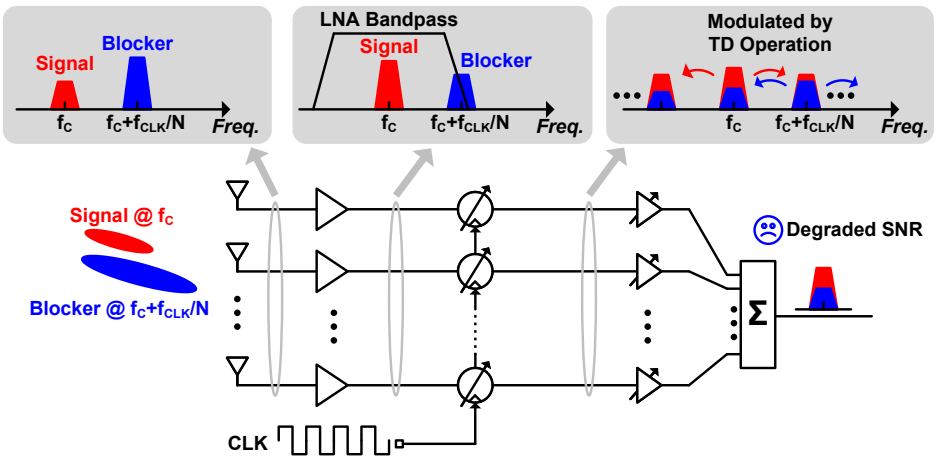


Figure 4.44: Blocker aliasing of proposed TD-MIMO receiver.

long as there is no spectral overlap, various mitigation techniques, such as filtering and linearization, can be employed to handle these blockers effectively.

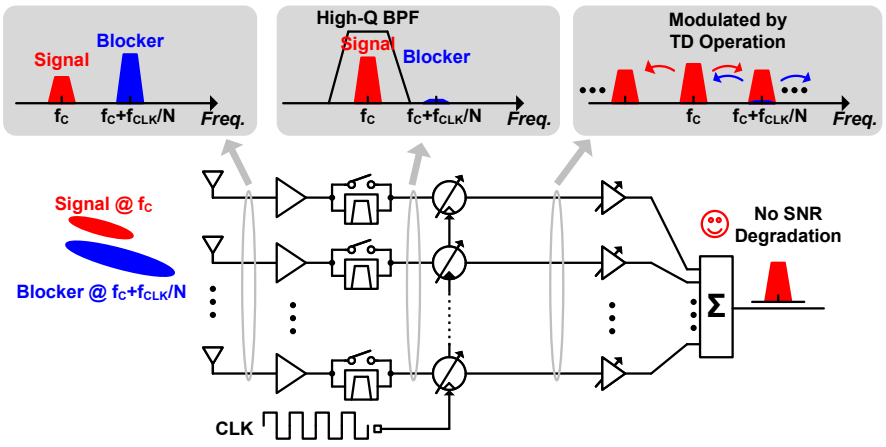


Figure 4.45: TD-MIMO receiver with high-Q anti-aliasing band pass filter.

In the proposed TD-MIMO phased-array receiver, the blocker issue becomes more severe due to the periodic beam-switching operation, which can be interpreted as a sampling and mixing process. The harmonics introduced by this switching process create significant interference challenges. Specifically, blockers appearing at harmonic frequencies of the form $f_C + f_{CLK}/N$ are folded back into the desired signal band at f_C, leading to substantial SNR degradation, as illustrated in the spectrum shown in Fig. 4.44. To achieve the required beam-switching speed, the signal chain bandwidth in the TD-MIMO receiver is designed to be relatively wide. Consequently, additional band-pass filtering may be necessary to mitigate harmonic blocker issues. Moreover, since aliasing occurs prior to power combining, the dispersion of the blocker signals, especially when they arrive from different directions, can further exacerbate SNR degradation. This unique challenge highlights the need for advanced filtering techniques and optimized switching strategies.

Despite the challenges posed by harmonic blockers, effective mitigation strategies can be implemented. As illustrated in Fig. 4.45, integrating a high-Q bandpass filter (BPF) into the signal chain before the switching phase shifter effectively attenuates harmonic blockers. While surface-mounted millimeter-wave BPF components are already widely used in industry, placing the filter on-chip after the LNA is preferable to minimize sensitivity loss. However, achieving a high-Q factor on-chip remains challenging due to trade-offs between out-of-band suppression and bandwidth, which limits the filter's ability to reject blocker signals. On the other hand, a possible solution is to increase the TD-MIMO switching frequency appropriately. In the proposed TD-MIMO receiver prototype

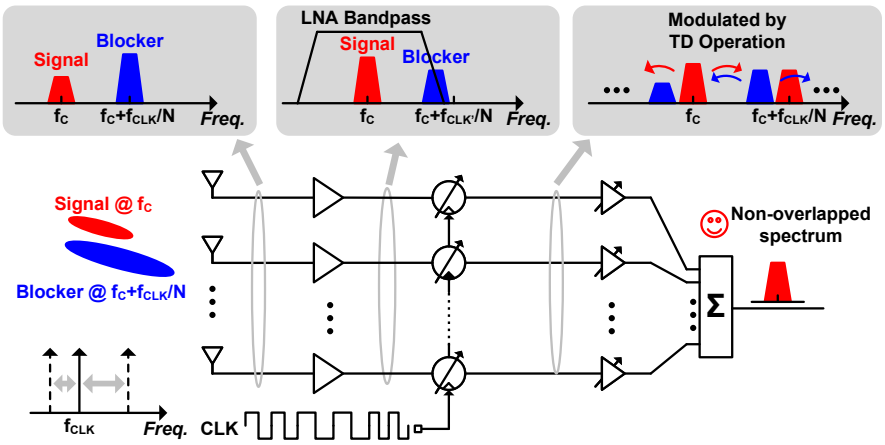


Figure 4.46: TD-MIMO receiver with adaptive hopping on TD operation frequency.

presented in this chapter, a beam-switching frequency exceeding 2 GHz is feasible. By further optimizing the phase shifter design and transitioning to a more advanced CMOS technology node, an even higher switching frequency can be achieved. This relaxes the bandwidth requirements of the on-chip BPF, making its integration more practical. Additionally, the BPF can be designed with a bypass switch to minimize SNR degradation when harmonic blockers are absent.

Another approach is to dynamically adjust the TD-MIMO operation frequency to avoid harmonic blockers, as showed in Fig. 4.46. When a blocker at a harmonic frequency is detected, the system hops the driving clock frequency, ensuring that the blocker no longer aligns with the harmonic frequencies of the desired signal. For example, if the desired signal is located at f_C and the original driving clock frequency is f_{CLK}, blockers at f_C+f_{CLK}/N (where N represents the number of MIMO beams) can introduce spectral aliasing. By shifting the driving clock frequency to $f_{CLK'}$, the modulated blockers are displaced from their original positions, effectively preventing spectral aliasing and eliminating SNR degradation due to spectral overlap. A major advantage of this method is that it requires no modifications to the RF signal chain, thereby minimizing RF performance degradation.

4.6 Summary

A novel time-division MIMO (TD-MIMO) architecture is introduced in this chapter, demonstrated through a 28-GHz 4-beam, 8-element TD-MIMO phased-array receiver

prototype fabricated in 65nm CMOS. The prototype achieves 64-QAM 4×4 MIMO reception with an RMS EVM of -23.5 dB in over-the-air (OTA) measurements. By utilizing four 5G NR data streams over a 400 MHz channel bandwidth, this architecture delivers high performance while maintaining the same number of RF elements as a single-input single-output (SISO) receiver. Fast-switching phase shifters with a beam-switching speed of 0.15 ns ensure high sensitivity and scalability to support additional MIMO streams. This scalability enables the design of power- and area-efficient MIMO receivers. The proposed TD-MIMO architecture is well-suited for next-generation high-data-rate receivers, facilitating larger MIMO beam configurations and very large-scale phased arrays while maintaining excellent power and area efficiency.

However, there are several areas where the proposed TD-MIMO phased-array receiver can be further improved to enhance its performance:

1. Linearity Improvement: Enhancing the linearity of the LNA and phase shifters to extend the dynamic range, enabling support for higher-order modulation schemes during MIMO operation.

2. Higher Switching Frequency: Revising the phase shifters to support higher switching frequencies, increasing adaptability to more MIMO streams or larger bandwidth.

3. Blocker Tolerance: Introducing non-uniform sampling or dithering in PS and MIMO switch control to mitigate harmonic blocker issues.

4. Automatic Timing Calibration: Implementing automatic inter-element timing calibration to significantly reduce synchronization preset effort.

Chapter 5

Conclusion and Future Work

5.1 Conclusion

This thesis is devoted to present novel architecture and design techniques of millimeter-wave phased-array receiver prepared for next generation high performance wireless communication standards.

This thesis focuses on millimeter-wave receiver ICs, a critical component of advanced communication systems. Chapter 1 introduces the background and evolution of communication systems, followed by an analysis of their applications and the demands of next-generation communication systems. The evolution of communication systems is explored in two dimensions in this thesis: achieving higher data rates for inter-device communication and increasing overall data traffic capacity across the network. MIMO technology is considered as essential for achieving higher data rates, while multi-band operation is considered crucial for expanding overall data traffic capacity. In line with the requirements of next-generation communication systems, scalable multi-band and MIMO techniques with high power and area efficiency are deemed indispensable. This thesis delves into the development and discussion of these techniques, providing insights and solutions to meet the demands of future communication networks.

Chapter 2 reviews the fundamentals of millimeter-wave phased-array receivers and identifies the key challenges in their design. By thoroughly examining the fundamental building blocks and architectures, the chapter lays the groundwork for devising precise solutions to meet the requirements of this thesis. The trade-offs inherent in various beamforming architectures are carefully analyzed to identify the most optimized approach for the research objectives. Additionally, as critical components of phased arrays, phase shifters and gain control units are evaluated in detail, with their respective advantages and limitations summarized. The chapter concludes by highlighting the importance of

compact, low-power designs to address the stringent demands of next generation wireless communication systems. These foundational analyses and insights serve as a guide for the subsequent development of advanced phased-array receiver designs throughout the thesis.

To address the multi-band operation demands outlined in Chapter 1, Chapter 3 presents a scalable and power-efficient solution for multi-band receivers. Conventional millimeter-wave multi-band receivers are first reviewed, revealing significant limitations: they are not only power-inefficient but also lack scalability to accommodate higher frequency bands without extensive redesign. These shortcomings highlight the need for innovative approaches to meet the evolving requirements of modern communication systems. In response, the proposed harmonic-selection technique provides a transformative solution. This technique enables power-efficient reception of multi-band signals within a limited bandwidth while intrinsically rejecting inter-band interference. Its scalability ensures adaptability for future frequency bands without requiring substantial modifications. To validate the effectiveness of this approach, a 2-channel multi-band phased-array receiver prototype is developed, designed to comprehensively cover all 5G NR bands. Measurements confirm its exceptional performance, demonstrating robust rejection of inter-band blockers and maintaining high power efficiency across various operating conditions, including worst-case scenarios. This advancement establishes the proposed receiver architecture as a highly reliable and scalable solution for increasingly congested spectrum environments. It not only addresses current challenges but also positions the design as a foundation for future millimeter-wave communication systems, ensuring sustained performance and adaptability in a rapidly evolving technological landscape.

To address the high data rate demands of point-to-point communication in next-generation systems, Chapter 4 introduces a novel time-division MIMO (TD-MIMO) architecture. This scalable solution effectively balances the trade-offs between chip area and MIMO stream capacity, making it well-suited for compact phased-array designs. A comparative analysis of conventional MIMO phased-array receivers presented in Chapter 4 reveals their poor scalability and limited compatibility with multi-chip systems. In contrast, the proposed TD-MIMO architecture facilitates the development of cost-effective, large-scale multi-chip arrays with a simplified single-wire inter-chip connection. This approach minimizes hardware costs and streamlines design modifications to accommodate additional MIMO streams in future applications.To validate the proposed design, a 4-stream, 8-element TD-MIMO phased-array receiver prototype was implemented. Over-the-air (OTA) measurements using a PCB setup demonstrated successful 64-QAM MIMO reception across four streams, achieving a data rate of 9.6 Gbps—marking the highest reported area and spectral efficiency to date. Furthermore, the TD-MIMO architecture is

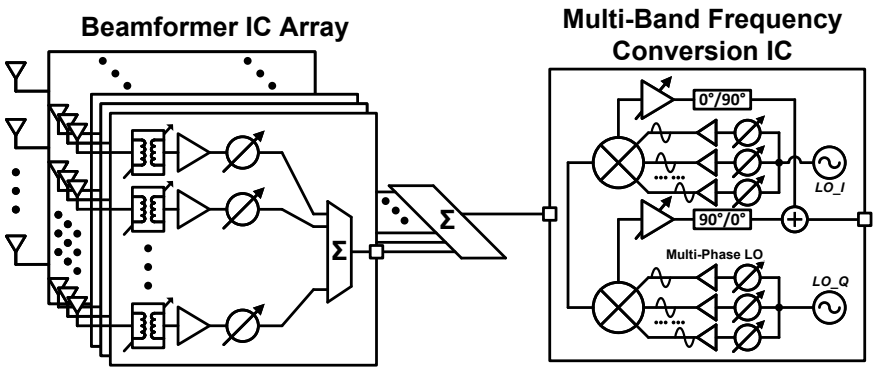


Figure 5.1: Area-efficient multi-band solution for large-scale multi-chip array.

extendable to phased-array transmitters, offering potential improvements in uplink communication. With continuous advancements in CMOS technology and further optimization of key circuit building blocks, the TD-MIMO architecture is well-positioned to scale further, setting new benchmarks for data rates and efficiency in next-generation wireless communication systems.

The efforts presented in this thesis represent a significant advancement in realizing the potential of millimeter-wave phased-array receivers, providing a comprehensive framework for addressing the critical challenges of scalability and efficiency in next-generation communication systems. As millimeter-wave technology continues to advance, the methodologies and findings outlined in this research are expected to serve as a foundational reference for the development of future wireless communication systems.

Notably, the proposed scalable multi-band architecture and the innovative TD-MIMO architecture are complementary in their development. Together, they offer a universal solution for millimeter-wave receivers, effectively tackling the pressing challenges of spectrum efficiency, scalability, and adaptability. By integrating these architectures, future communication systems will be well-equipped to handle the demands of increasingly complex and high-capacity networks, ensuring reliable and efficient operation in the evolving technological landscape.

5.2 Future Works

5.2.1 Area-Efficient Multi-Band Receiver

As discussed in the previous chapters, a large-scale multi-chip receiver array is essential for next-generation communication systems to achieve superior RF performance and

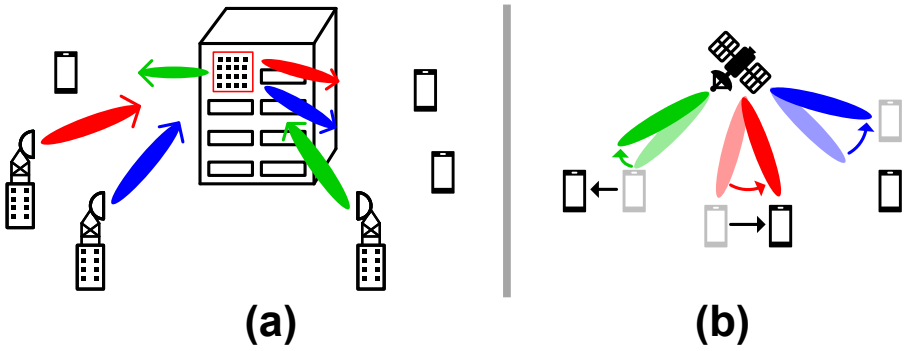


Figure 5.2: (a) Reflected-type time-division MIMO relay array. (b) TD-MIMO transceiver with real-time background fast-beam tracking.

enhanced functionality. The proposed multi-band receivers in this thesis rely on LO phase-shifting architectures to alleviate the bandwidth and linearity demands on phase shifters. However, these architectures require dedicated mixers and LO paths for each antenna element, significantly reducing area efficiency. This limitation becomes particularly problematic for the proposed harmonic-selection technique, which demands a larger multi-phase LO generation circuit. Additionally, the complex inter-chip LO distribution inherent to LO phase-shifting architectures further hinders their scalability in multi-chip applications.

Recent advancements in ultra-wideband passive networks, such as fully differential quadrature transformer-based I/Q splitters (as shown in Fig. 2.27 and discussed in Chapter 2), offer a promising alternative to realize passive multi-band phase shifters. Furthermore, studies on massive arrays with low phase resolution have demonstrated the feasibility of passive phase shifters for accurate beam control [133]. Phase shifters with low-resolution can be implemented in a low-insertion-loss, ultra-wideband design, enabling an RF phase-shifting architecture for multi-band receivers. By adopting this new technique, the proposed multi-band receiver architecture can transition to an RF phase-shifting design, allowing for a more area-efficient multi-chip layout. As illustrated in Fig. 5.1, the RF beamformer with multi-band phase shifters can be separated into a dedicated chip for multi-chip integration, while the harmonic-selection mixer and LO generation circuits are consolidated into an independent frequency conversion IC.

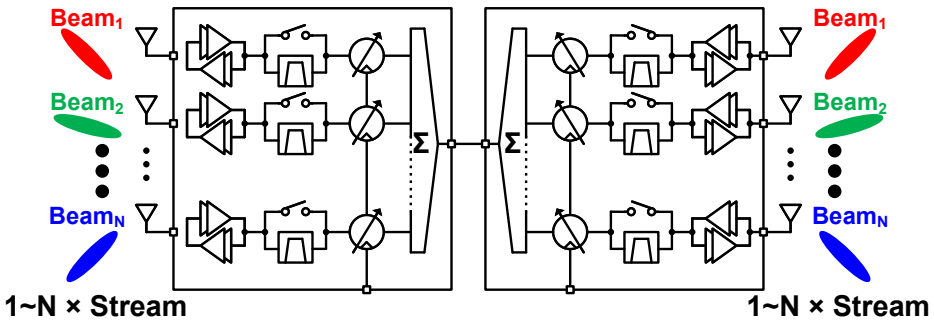


Figure 5.3: Block diagram of bi-directional relay transceiver with TD-MIMO architecture.

5.2.2 Time-Division Multiplexing in More Application

The time-division multiplexing based on Nyquist-rate fast beam switching in the proposed TD-MIMO architecture enables its application in advanced systems. Relays, which play a critical role in modern communication systems by extending coverage and improving signal quality, act as intermediate nodes retransmitting signals between the source and destination—especially in areas with poor direct connectivity, such as urban environments. As shown in Fig. 5.2 (a), the TD-MIMO architecture is well-suited for relay systems due to its strong support for large-scale multi-chip arrays. Its compact size and scalability make it a cost-effective and highly adaptable solution. Additionally, the lossless fast beam switching in TD-MIMO can extend beyond communication applications to target tracking. Fig. 5.2 (b) illustrates a concept of a TD-MIMO transceiver with real-time fast beam tracking.

Let's take a closer look at these concepts. A relay is a network element that receives, processes, and retransmits signals to facilitate communication between distant or obstructed nodes. In millimeter-wave communication, relay technology is essential for extending coverage and mitigating signal blockages caused by high path loss and obstacles. By forwarding signals between the transmitter and receiver without requiring direct line-of-sight, relays enhance link reliability and reduce power consumption. Fig. 5.3 illustrates the block diagram of the proposed bi-directional TD-MIMO relay array. The system features a shared IC design for both the TX and RX sides, significantly reducing design complexity and overhead. The TD-MIMO operation maximizes the number of supported user devices in relay while minimizing hardware costs. The single-wire connection architecture enhances modular design flexibility and simplifies array scalability, removing traditional barriers.

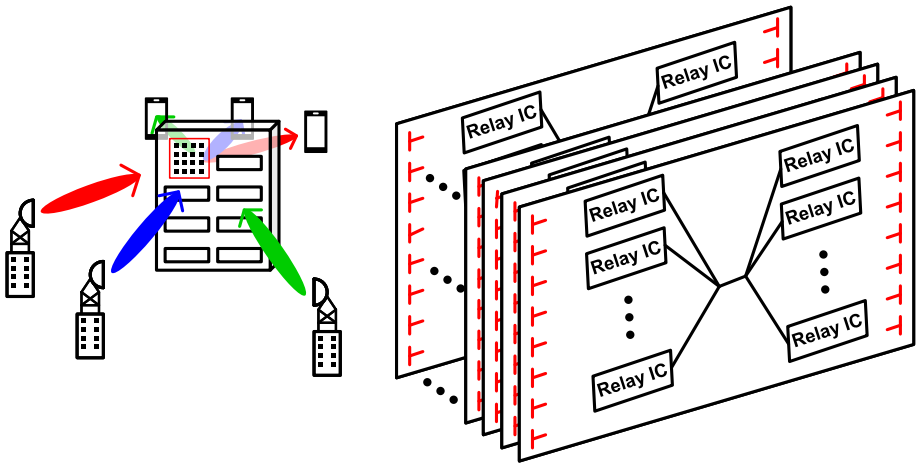


Figure 5.4: The PCB design and transmissive-type relay

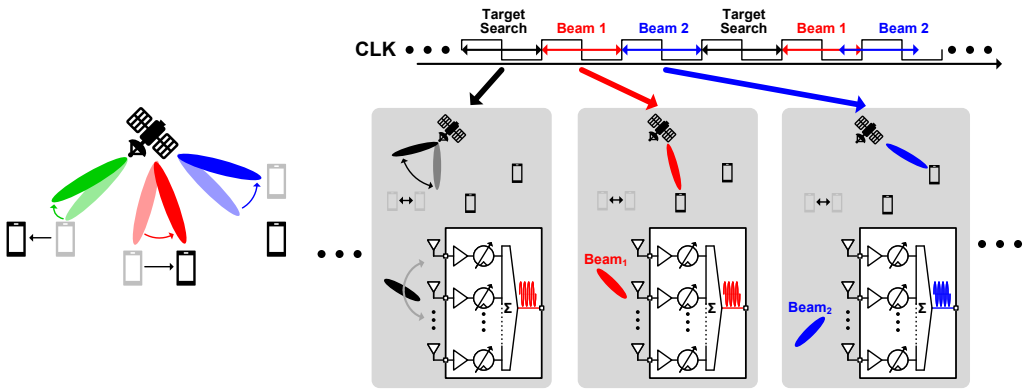


Figure 5.5: Operation principle of the transceiver combining sensing and communication with TD-MIMO operation.

The reconfigurable TD-MIMO operation adapts to varying target locations and user demands, which are often unpredictable in relay applications. In contrast, conventional MIMO relays based on FC-MIMO architectures lack the flexibility to accommodate dynamic user requirements. Furthermore, with side-located antenna arrays on both ends, as shown in Fig. 5.4, the transmissive-type relay can be efficiently implemented without the need for complex module designs. The TX-RX shared IC architecture also simplifies PCB wiring and layout, further reducing design complexity and enhancing manufacturability.

The integration of communication and sensing functionalities has become a key focus

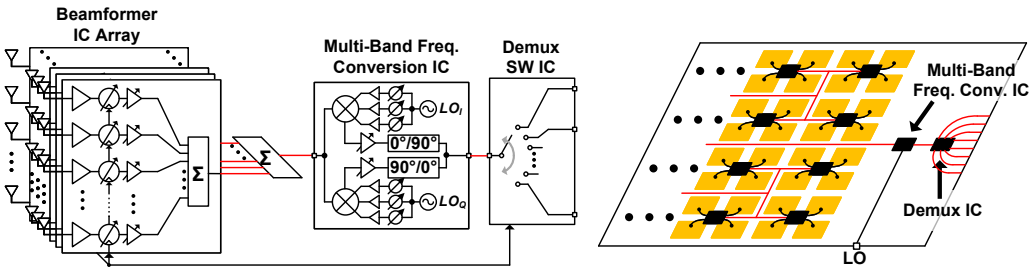


Figure 5.6: Scalable solution for next generation receiver with modular design.

in the advancement of millimeter-wave applications, enabling efficient spectrum utilization and enhanced situational awareness. The proposed TD-MIMO architecture is particularly well-suited for the seamless fusion of communication and sensing due to its dynamic beam allocation capability. By reserving specific time slots within the TD-MIMO operation for beam searching, the system can continuously sense and track moving targets in real time by adjusting beam directions dynamically.

As illustrated in Fig. 5.5, the TD-MIMO transceiver cyclically alternates between target search and communication beams, ensuring uninterrupted data transmission while simultaneously scanning the environment for new objects or changes in target positioning. For example, with a data channel bandwidth of 400 MHz, the beam switching rate reaches a minimum of 400 MHz, allowing the transceiver to scan up to 400 million directions per second. This high-speed scanning capability provides rapid and accurate environmental awareness, making it ideal for applications such as automotive radar, industrial automation, and smart infrastructure.

Unlike conventional beam-scanning systems that require dedicated sensing intervals—causing interruptions to communication and resulting in lower data rates—the TD-MIMO operation enables concurrent beam tracking and communication. This ensures continuous data transmission without sacrificing throughput, thus optimizing both connectivity and situational awareness. Moreover, the reconfigurable nature of TD-MIMO allows it to flexibly adapt to varying operational scenarios, dynamically allocating resources based on real-time sensing requirements and communication demands.

5.2.3 Scalable Modular Receiver for Next-Generation Communication System

As discussed in previous chapters, both multi-band and MIMO operation are essential for next-generation receivers. The proposed multi-band architecture, based on the harmonic-

selection technique, and the TD-MIMO architecture can be seamlessly combined to form a universal receiver solution for future communication systems. This integrated solution achieves power- and area-efficient high data rate communication, ensures global compatibility, and maximizes channel utilization efficiency across the entire system. The block diagram of this universal design is shown in Fig. 5.6. By incorporating RF phase-shifting architecture into the multi-band receiver, the multi-band harmonic-selection mixer and MIMO de-multiplexing switches can be modularized into an independent IC. This modular design separates the analog beamformer front end from other functional blocks, enabling flexible upgrades to multi-band and MIMO capabilities with minimal design overhead and cost. Additionally, RF performance can be enhanced by simply increasing the size of the multi-beamformer array without impacting the functionality of the multi-band and MIMO modules.

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Appendix A

Publication List

A.1 Journal Papers

- **Yi Zhang** *et al.*, "A Power-Efficient CMOS Multi-Band Phased-Array Receiver Covering 24–71-GHz Utilizing Harmonic-Selection Technique With 36-dB Inter-Band Blocker Tolerance for 5G NR," in IEEE Journal of Solid-State Circuits, vol. 57, no. 12, pp. 3617-3630, Dec. 2022, doi: 10.1109/JSSC.2022.3214118.

- **Yi Zhang** *et al.*, "A 2.5dB Noise Figure 28GHz Current-Reused Noise-Cancelling LNA with g_m-Boosting in 65nm CMOS for Millimeter-Wave MIMO Applications," in IEICE Electronics Express, Early Access, Jan. 2025.

A.2 International Conferences and Worshops

- **Yi Zhang** *et al.*, "A 28GHz 4-Stream Time-Division MIMO Phased-Array Receiver Utilizing Nyquist-Rate Fast Beam Switching for 5G and Beyond," 2024 IEEE Symposium on VLSI Technology and Circuits (VLSI Technology and Circuits), Honolulu, HI, USA, 2024, pp. 1-2, doi: 10.1109/VLSITechnologyandCir46783.2024.10631537.

- **Yi Zhang** *et al.*, "28GHz Phase Shifter with Temperature Compensation for 5G NR Phased-array Transceiver," 2021 26th Asia and South Pacific Design Automation Conference (ASP-DAC), Tokyo, Japan, 2021, pp. 7-8.

- **Yi Zhang** *et al.*, "A 28GHz Bi-direction Transceiver with Temperature Compensation," IEEE International Conference on Integrated Circuits, Technologies and Applications (ICTA), Zhuhai, China, 2021, pp. 80-81

- **Yi Zhang** *et al.*, IEEE International Solid-State Circuits Conference (ISSCC) Student Research Preview, Feb. 2024.

A.3 Domestic Conferences and Workshops

- **Yi Zhang** *et al.*, "Temperature-Compensated Active Phase Shifter for 28GHz Phased-Array Transceiver," IEICE Society Conference, C-12-1, Sep. 2020.
- **Yi Zhang** *et al.*, "A 39GHz Bi-direction Phased-Array Transceiver with Temperature," IEICE Society Conference, C-12-27, Sep. 2021.
- **Yi Zhang** *et al.*, "A Hybrid-Type Passive Polyphase Filter with High Image Rejection and Low Insertion Loss," IEICE Society Conference, C-12-18, Sep. 2022.
- **Yi Zhang** *et al.*, "A Self-Locked Duty Cycle Control Cell with 40% Tuning Range for Clock Distribution Network," IEICE General Conference, Hiroshima, C-12-42, Mar. 2024.

A.4 Co-Authored Journals and Conferences

A.4.1 Journal Papers

- Jian Pang, Zheng Li, Xueting Luo, Joshua Alvin, Rattanan Saengchan, Ashbir Aviat Fadila, Kiyoshi Yanagisawa, **Yi Zhang** *et al.* "A CMOS Dual-Polarized Phased-Array Beamformer Utilizing Cross-Polarization Leakage Cancellation for 5G MIMO Systems," in IEEE Journal of Solid-State Circuits, vol. 56, no. 4, pp. 1310-1326, April 2021, doi: 10.1109/JSSC.2020.3045258.
- Yuncheng Zhang, Zheng Sun, Bangan Liu, Junjun Qiu, Dingxin Xu, **Yi Zhang**, Xi Fu *et al.*, "A Time-Mode-Modulation Digital Quadrature Power Amplifier Based on 1-bit Delta–Sigma Modulator and Hybrid FIR Filter," in IEEE Journal of Solid-State Circuits, vol. 59, no. 4, pp. 993-1005, April 2024, doi: 10.1109/JSSC.2023.3349002.
- Jian Pang, Zheng Li, **Yi Zhang** *et al.*, "A Compact 28 GHz Bi-Directional Power-Combined Antenna Interface in WLCSP for 5G and B5G Transceivers," in IEEE Solid-State Circuits Letters, vol. 6, pp. 149-152, 2023, doi: 10.1109/LSSC.2023.3279136.
- Zheng Li, Jian Pang, **Yi Zhang** *et al.*, "A 39-GHz CMOS Bidirectional Doherty Phased-Array Beamformer Using Shared-LUT DPD With Inter-Element Mismatch

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- Dingxin Xu, Zezheng Liu, Yifeng Kuai, Hongye Huang, Yuncheng Zhang, Zheng Sun, Bangan Liu, Wenqian Wang, Yuang Xiong, Junjun Qiu, Madany Waleed, **Yi Zhang** *et al.*, "A DPD/Dither-Free DPLL Based on a Cascaded Fractional Divider and Pseudo-Differential DTCs Achieving a -62.1-dBc Fractional Spur," in IEEE Journal of Solid-State Circuits, doi: 10.1109/JSSC.2024.3477498.

A.4.2 Conferences and Workshops

- Yuncheng Zhang, Zheng Sun, Bangan Liu, Junjun Qiu, Dingxin Xu, **Yi Zhang**, Xi Fu *et al.*, "A Time-Mode-Modulation Digital Quadrature Power Amplifier Based on 1-bit Delta-Sigma Modulator and Transformer Combined FIR FIlter," 2023 IEEE Symposium on VLSI Technology and Circuits (VLSI Technology and Circuits), Kyoto, Japan, 2023, pp. 1-2, doi: 10.23919/VLSITechnologyandCir57934.2023.10185368.

- Xi Fu, Yun Wang, Dongwon You, Xiaolin Wang, Ashbir Aviat Fadila, **Yi Zhang** *et al.*, "A 3.4mW/element Radiation-Hardened Ka-Band CMOS Phased-Array Receiver Utilizing Magnetic-Tuning Phase Shifter for Small Satellite Constellation," 2022 IEEE International Solid-State Circuits Conference (ISSCC), San Francisco, CA, USA, 2022, pp. 90-92, doi: 10.1109/ISSCC42614.2022.9731557.

- Jian Pang, Zheng Li, Xueting Luo, Joshua Alvin, Kiyoshi Yanagisawa, **Yi Zhang** *et al*. "A Fast-Beam-Switching 28-GHz Phased-Array Transceiver Supporting Cross-Polarization Leakage Self-Cancellation," 2021 Symposium on VLSI Circuits, Kyoto, Japan, 2021, pp. 1-2, doi: 10.23919/VLSICircuits52068.2021.9492496.

- Jian Pang, **Yi Zhang** *et al*. "A Power-Efficient 24-to-71 GHz CMOS Phased-Array Receiver Utilizing Harmonic-Selection Technique Supporting 36dB Inter-Band Blocker Rejection for 5G NR," 2022 IEEE International Solid-State Circuits Conference (ISSCC), San Francisco, CA, USA, 2022, pp. 434-436, doi: 10.1109/ISSCC42614.2022.9731619.

- Zheng Li, Jian Pang, **Yi Zhang** *et al*. "A 39-GHz CMOS Bi-Directional Doherty Phased-Array Beamformer Using Shared-LUT DPD with Inter-Element Mismatch Compensation Technique for 5G Base-Station," 2022 IEEE Symposium on VLSI Technology and Circuits (VLSI Technology and Circuits), Honolulu, HI, USA, 2022, pp. 98-99, doi: 10.1109/VLSITechnologyandCir46769.2022.9830274.

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- Dongfan Xu, Minzhe Tang, **Yi Zhang** *et al*. "A 24–71-GHz Tri-Mode Mixer Using Harmonic Selection for Multi-Band 5G NR," 2024 IEEE International Symposium on Circuits and Systems (ISCAS), Singapore, Singapore, 2024, pp. 1-4, doi: 10.1109/ISCAS58744.2024.10558040.
- Dingxin Xu, Zezheng Liu, Yifeng Kuai, Hongye Huang, Yuncheng Zhang, Zheng Sun, Bangan Liu, Wenqian Wang, Yuang Xiong, Junjun Qiu, Madany Waleed, **Yi Zhang** *et al.*, "10.3 A 7GHz Digital PLL with Cascaded Fractional Divider and Pseudo-Differential DTC Achieving -62.1dBc Fractional Spur and 143.7fs Integrated Jitter," 2024 IEEE International Solid-State Circuits Conference (ISSCC), San Francisco, CA, USA, 2024, pp. 192-194, doi: 10.1109/ISSCC49657.2024.10454284.