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Pham Nam Hai,[1,a)] Takanori Shirokura,[2,b)] and Nguyen Huynh Duy Khang[3]

AFFILIATIONS

[1]Department of Electrical and Electronic Engineering, Institute of Science Tokyo, 2-12-1 Ookayama, Meguro, Tokyo 152-0033, Japan
[2]Institute of Innovative Research, Institute of Science Tokyo, 4259 Nagatsuta-cho, Midori-ku, Yokohama, Kanagawa 226-8503, Japan
[3]Department of Physics, Ho Chi Minh City University of Education, 280 An Duong Vuong Street, District 5, Ho Chi Minh City 738242, Vietnam

[a)]**Author to whom correspondence should be addressed:** pham.n.ab@m.titech.ac.jp
[b)]**Present address:** National Institute of Technology, Numazu College.

ABSTRACT

We propose an architecture for the suppression of magnetic domain wall shift error in 3D magnetic domain wall memory, which utilizes the spatially modulated perpendicular magnetic anisotropy (PMA) of magnetic layers that are deposited on the side walls of multilayers of different oxide materials. We experimentally identified the oxide material candidates for such implementation and found that CrO_x can generate the largest PMA while GdO_x generates the smallest PMA of Pt/Co/Pt multilayers. Our proposed architecture can be a key to realizing 3D magnetic domain wall racetrack memory with low bit-shift error.

I. INTRODUCTION

3D magnetic domain wall (or racetrack) memory is expected to be the next-generation storage-class non-volatile memory because it does not require a stair-case structure as in the case of 3D NAND flash memory.[1] In 3D magnetic domain wall (MDW) memory, the magnetic layers are deposited vertically on the sidewalls of the deep vertical wells. The magnetic domains, which store data bits, are moved up and down by a driving current, which exerts spin-transfer-torque (STT) or spin–orbit-torque (SOT) on the MDWs. One of the major challenges in 3D MDW memory is how to suppress the shift error of MDWs due to variations in domain wall driving current density, pulse width, as well as domain wall velocity.[2] While there are several techniques to suppress shift error in 2D MDW memory such as local doping,[3–5] local alloying,[6,7] notching,[8–12] shaping[13–15] of the racetrack, etc., such techniques are difficult to implement in a 3D structure.

In this work, we propose an architecture to suppress MDW shift error that can be implemented in 3D, utilizing the spatially modulated perpendicular magnetic anisotropy (PMA) of magnetic nanowires that are induced by neighboring oxide layers. We then experimentally identified the oxide material candidates to realize such a structure. Finally, we verified our technique using micromagnetic simulations. Our proposed structure can be a key to realizing 3D MDW racetrack memory with low bit-shift error.

II. ARCHITECTURE OF OUR 3D MAGNETIC DOMAIN WALL MEMORY

Figure 1(a) shows the schematic structure of our proposed 3D MDW memory. In this structure, the 3D racetracks are deposited on the sidewalls of multilayers of different oxide materials. These oxide layers induce different PMA constant K_u of the magnetic layers. The areas of the magnetic layers with low K_u on top of oxide B (gray) correspond to magnetic bit sites, while the areas with high K_u on top of oxide A (green) generate domain wall pinning sites at their boundaries. At the bottom of the well, there is a writer for writing magnetic bit data and a reader for reading out the magnetic bit data. As shown later by micromagnetic simulations, MDWs can be stopped at the boundaries between the low K_u and high K_u areas. Thus, sequences of a short pulse with a high current for depinning MDWs from the boundaries and a long

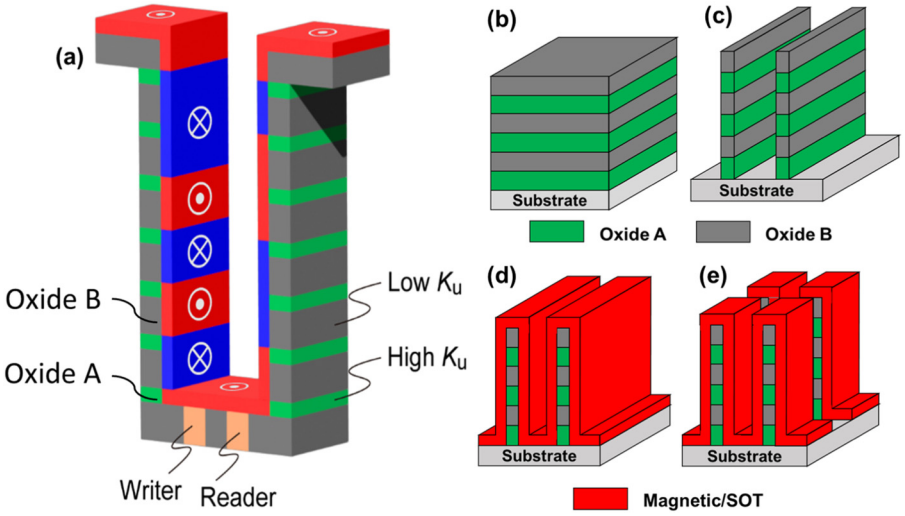

FIG. 1. (a) Schematic structure of our proposed 3D MDW memory. (b)–(e) Manufacturing process flow of such a 3D MDW memory.

pulse with a low current for moving the MDWs away from the boundaries will allow precise shifting of MDWs in 3D MDW memory. Figures 1(b)–1(e) show the manufacturing process of such a 3D MDW memory. First, multilayers of oxides A and B are deposited on the top of a substrate using conventional physical vapor deposition techniques. Here, the substrate can embed writers and readers for the 3D MDW memory (not shown). Then, long fin structures of the oxide multilayers are formed by reactive ion etching. In 3D-NAND flash memory, it is known that SiO_2/poly-Si, SiN/poly-Si, or SiO_2/SiN multilayers can be deposited up to several ~100 pairs and vertical holes with very high aspect ratio can be etched with little notching. Thus, it is essential to develop a reactive ion etching technique with two reactive gases that have very high selectivity between the two oxide materials so that the FIN structure with little notch can be realized. Next, magnetic and optional SOT layers can be deposited by chemical vapor deposition or atomic layer deposition to form 3D magnetic/SOT multilayers on the long fin structures including their surfaces and sidewalls.[16,17] Finally, the long fins are etched again to form 3D MDW memories.

III. INVESTIGATION OF MATERIAL CANDIDATES

We then investigated the material candidates for such implementation. For this purpose, we deposited stacks of oxide buffer/Pt (0.8 nm)/Co (0.8 nm)/Pt (0.8 nm)/cap on surface-oxidized Si substrates, as shown in Fig. 2(a). For the oxide buffer, we used NiO or MgO deposited by sputtering from ceramic targets and GdO_x or CrO_x deposited by reactive sputtering from metallic targets with $Ar + O_2$ gas. All the oxide layers were deposited at room temperature. Thus, we expect that these oxide buffer layers are amorphous, although MgO may be crystallized. Local clusters of hexagons from amorphous materials can mimic a pseudo-crystalline (111) surface, whose nearest atomic distance may match or mismatch with that of the Pt(111)/Co(0001) system. Since the PMA of the Pt/Co/Pt system strongly depends on the degree of Pt(111)/Co(0001) texture,[18,19] an amorphous buffer with the nearest atomic distance matched with that of Pt(111) can yield a higher degree of Pt(111)/Co(0001) texture and stronger PMA than that with mismatched one. Since there is no reliable literature data for the studied amorphous oxide materials, we assume the bonding lengths in their amorphous oxides are close to those in their crystalline oxides and compare the bond length of Pt–Pt (2.77 Å) with that of Ni–O (2.09 Å) and Mg–O (2.11 Å) in their well-known rock salt NiO/MgO crystal structure, Cr–O (1.99 Å) in its tetragonal CrO crystal structure, and Gd–O (2.33 Å) in its zinc-blende GdO crystal structure.[20] We find that triple of the Cr–O bond length (5.97 Å) is closest to double of the Pt-Pt length (5.54 Å), while that of the Gd–O length (6.99 Å) is farthest and those of Ni–O (6.27 Å) and Mg–O (6.33 Å) are in between. Thus, we expect that the Pt(111) interface would match best with CrO_x, while it would match worst with GdO_x.

Figures 2(c)–2(j) show the normalized anomalous Hall resistance R_{ANE} of Pt/Co/Pt deposited on top of the GdO_x, NiO, MgO, and CrO_x buffer layer, respectively, measured with an out-of-plane and an in-plane magnetic field in Hall bar devices, from which we measured the coercive force H_C as well as the PMA field H_k of the Pt/Co/Pt multilayers. Figure 2(b) summarizes H_k and H_C of these stacks. A clear correlation between H_C and H_k was observed. Importantly, we found that CrO_x generates the largest PMA with $H_k = 6.4$ kOe, while GdO_x generates the smallest PMA with $H_k = 1$ kOe, as expected. Thus, GdO_x/NiO, NiO/MgO, or MgO/CrO_x pairs can be utilized for the low-K_u/high-K_u inducing mutilayers of the fin structures, while Pt/Co/Pt can be utilized as the magnetic multilayers for the proposed structure in Fig. 1. We note that since these oxides are amorphous, similar modulation of PMA can be expected when the Pt/Co/Pt multilayers are deposited on the sidewalls of the fins. The most important technical challenge of Pt/Co/Pt deposition on the sidewalls of the fins is the use of the atomic layer deposition (ALD) method to grow multilayers of Pt and Co. Recently, high-quality ALD-Pt and sputtered Co with PMA has been studied.[17] On the other hand, PMA and domain-wall motion of ALD-Co on a sputtered Pt seed layer have been also demonstrated.[21] Thus, we expect that full ALD-Pt/Co/Pt with PMA can be realized for use in our architecture.

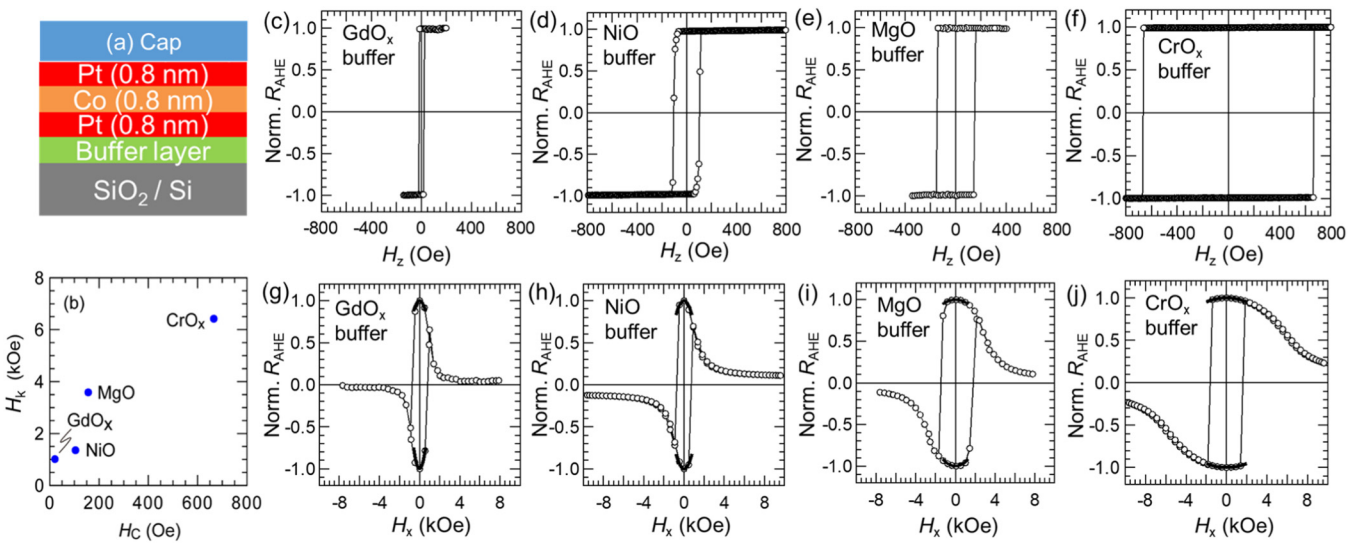

FIG. 2. (a) Schematic stacking structure for evaluation of the PMA of Pt/Co/Pt trilayers deposited on various oxide buffer layers. (b) Coercive force H_C and PMA field H_k of the Pt/Co/Pt trilayers deposited on GdO_x, NiO, MgO, and CrO_x buffer layer, estimated from the normalized anomalous Hall resistance R_{AHE} measured with (c)–(f) an out-of-plane and (g)–(j) an in-plane magnetic field, respectively.

IV. OPERATION OF WRITER AND READER

Next, we discuss the operation of writers and readers at the bottom of 3D MDW memory. Figure 3 shows the schematic view of the bottom of a single 3D MDW memory. The substrate embeds three components: a writer with a hard ferromagnetic (FM) layer for writing magnetic domains by spin injection through a thin tunnel barrier, a reader for reading magnetic domains, and a non-magnetic (NM) electrode located between the writer and the reader. The length of the bottom is assumed to be at least the length of one full bit in the nanowire. The length of the writer is half of a bit length. For data writing, a writing current is applied between the writer and the NM electrode, as shown in Fig. 3(a). Since the width of the writer is only a half of the bit length, a magnetic domain with a half-length is generated, which we call a "half-bit." Next, a shift pulse current is injected into the nanowire to shift the newly generated "half-bit" magnetic domain toward the reader position. The pinning site near the reader provides the precise position control of the shift operation so that the half-bit magnetic domain sits on the top of the reader for verification, as shown in Fig. 3(b). Finally, a short but high depinning pulse and a long but low shift pulse are applied to expand the half-bit to a full-bit, as shown in Fig. 3(c). At this stage, the writing operation finishes.

We note that because the Pt(111) underlayer is very thin (0.8 nm or thinner), it can allow spin injection for writing.

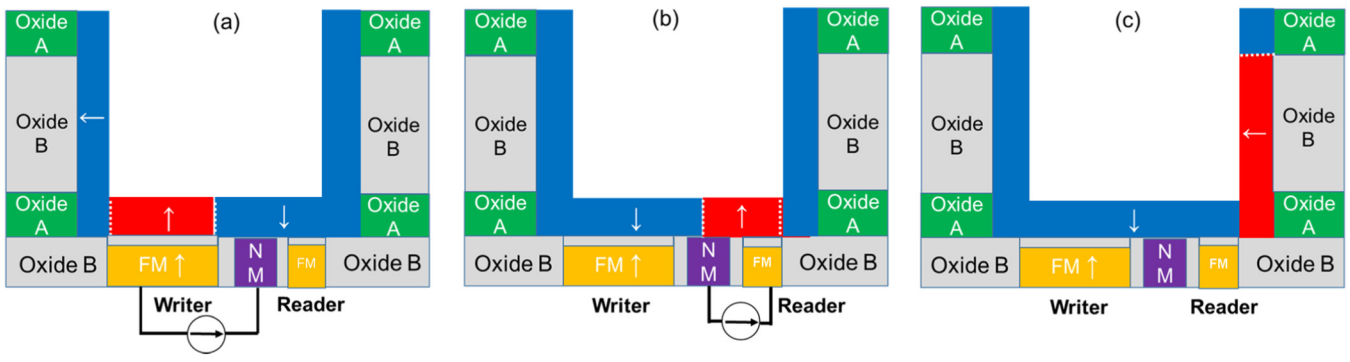

FIG. 3. Operation of writers and readers at the bottom of 3D MDW memories. (a) Half-bit injection, (b) half-bit verification, and (c) full-bit expansion.

Indeed, we have demonstrated magnetization switching by the spin–orbit-torque effect on Pt (0.8 nm)/Co(0.8 nm)/Pt (0.8 nm) in contact with the topological semimetal YPtBi.[22] Another example is SOT switching in BiSb/Pt (0.8 nm)/Fe (1 nm).[23] Therefore, it would be possible for writing in a "contact mode," i.e., via spin injection by either STT from an FM layer or SOT from an NM layer.

For reading, we can also use the "contact mode." Since the very thin Pt allows spin transport, when a spin-polarized current is injected from a reference FM layer to the nanowire, there should be a TMR effect. Indeed, TMR was observed in Co(001) (200 Å)/Cu (001) (0–20 Å)/AlO_x (18 Å)/$Ni_{80}Fe_{20}$ (100 Å), where a Cu layer is inserted between the Co and the AlO_x layer.[24]

For the contact mode spin-injection writer via the STT effect and the spin-detection reader via the TMR effect, their oxide tunnel barriers are the same as the bottom oxide material. In general, the oxide material for low K_u areas may not be the best tunnel barrier material for the contact-mode writer and reader, although MgO is possible when using MgO for the low K_u sites and CrO_x for the high K_u sites.

Alternatively, we can also use the "non-contact mode" for writing and reading, similar to the Oersted field writer and the TMR reader in a hard disk drive (HDD). Here, the Oersted field is generated by coils wrapped around a write head. In modern HDD, the write head can write data to areas as small as ~20 nm. Thus, it would be able to write data to the nanowire by an Oersted field-writer similar to those in HDD. For non-contact mode reading, a full-stack TMR reader can be placed below the racetrack, and the reader senses the stray field of the domain above. Because the stray field is perpendicular to the plane, a Hall effect device placed below the domain can also be used as a reader.

V. MICROMAGNETIC SIMULATION

We now use micromagnetic simulation to demonstrate that our architecture is indeed helpful for the precise position control of MDW. For that purpose, we simulate the domain wall motion after half-bit writing for verification and full-bit expansion, as described in Fig. 3. Figure 4 shows the simulation results for a 50 nm wide × 500 nm long magnetic wire using the mumax3 simulator.[25] For simplicity, we simulate the domain wall motion in this straight wire, rather than the U-shape wire at the bottom of the real 3D MDW memory. Here, the left half area at x = 100–250 nm of the straight wire in Fig. 4 corresponds to the bottom part of the U-shape wire in Fig. 3, while the left-most area at x = 0–100 nm and the right half area at x = 250–500 nm of the wire in Fig. 4 represent the left and the right vertical parts of the U-shape wire in Fig. 3. Three high K_u sites (K_{u2} sites) are positioned at x = 50–100 nm, 250–300 nm, and x = 450–500 nm. We assume the magnetization $M = 1000$ emu/cc, the film thickness $t_{FM} = 1.2$ nm, the magnetic anisotropy constant $K_{u1} = 1.0 \times 10^6$ J/m^3 for the low K_u sites and $K_{u2} = 1.5 \times 10^6$ J/m^3 for the high K_u sites, the Landau–Lifshitz damping constant $\alpha = 0.15$, the non-adiabaticity of spin-transfer-torque $\xi = 0.1$,[26] and the spin-polarization $P = 0.65$. The simulation started at $t = 0$ ns with an initial domain $m_z = -1$ located at x = 100–200 nm, representing a "half-bit" injected by a writer. Next, current $J_1 = 0.7 \times 10^8$ A/cm^2 was injected to drive the domain by STT for $t = 0$–3 ns. As shown in the left panels of Fig. 4, as soon as the current was injected, the domain started to move toward the middle K_{u2} site with a speed of 25 nm/ns. The domain head reached the middle K_{u2} site at $t = 2$ ns and was stopped at the left boundary of the middle K_{u2} site. The tail of the domain continued to move until $t = 3$ ns, at that the domain size shrank by 25%. However, it would take 4 ns for the domain size to fully shrink, so

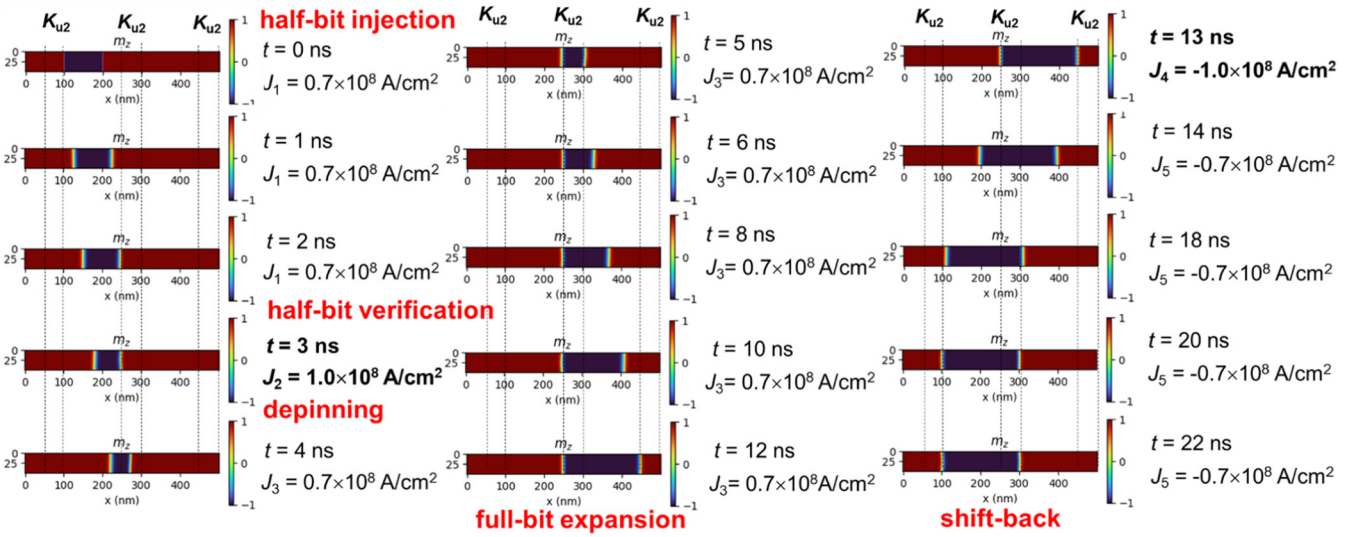

FIG. 4. Micromagnetic simulation of half-bit shift, depinning, full-bit expansion, and shift-back with 1 ns depinning pulses of ±1.0 × 10^8 A/cm^2, when $K_{u1} = 1.0 \times 10^6$ J/m^3 and $K_{u2} = 1.5 \times 10^6$ J/m^3.

we have a large margin not to accidentally eliminate the half-bit. At this point, the domain would sit on the top of the reader's position for verification by the reader. Next, a higher current $J_2 = 1.0 \times 10^8$ A/cm^2 was applied at $t = 3$–4 ns to depin the domain head from the boundary of the middle K_{u2} site. At $t = 4$ ns, the head of the domain entered the internal of the middle K_{u2} site. Finally, a lower current $J_3 = 0.7 \times 10^8$ A/cm^2 was applied at $t = 4$–12 ns to expand the half-bit to a full-bit. As seen in the middle panels of Fig. 4, the tail of the domain reached the middle pinning site at $t = 5$ ns and stopped further moving, while the head of the domain continued to move toward the right pinning site until $t = 12$ ns. At $t = 12$ ns, the half-bit expanded to a full-bit. Thus, the K_{u2} sites are very important and useful for precise control of the domain wall motion.

To see the backward motion of the domain, a reverse sequence of 1 ns ($t = 13$–14 ns) depinning pulse $J_4 = -1.0 \times 10^8$ A/cm^2 and 9 ns ($t = 14$–23 ns) shift-pulse $J_5 = -0.7 \times 10^8$ A/cm^2 was applied as shown in the right column of Fig. 4. Because the domain walls were not pinned in the reverse direction, the intended depinning pulse J_4 simply shifted the domain backward with a higher speed of about 50 nm/ns. Therefore, the domain walls took only 4 ns ($t = 14$–18 ns) of the J_5 shift pulse to reach the right boundary of the left and middle K_{u2} sites, and they stood still for the remaining duration ($t = 18$–22 ns) of the J_5 pulse.

At the end of the shift-back operation, the domain walls are pinned at the right boundary of the K_{u2} sites. Thus, the half-bit shift to the right direction cannot be performed correctly in this situation. To solve this problem, information of the last bit-shift direction of the 3D racetrack can be stored in a one-bit meta data (i.e., "1" for the right direction and "0" for the left direction). Before performing the writing and half-bit shift, a controller reads the meta data to learn the last bit-shift direction. If the meta data bit is "1," the controller can perform writing immediately. However, if the meta data bit is "0," the controller will move the racetrack to the left for 1-bit length, then move it to the right for 1 bit-length. This step makes sure that all the domain walls are pinned at the correct boundaries of the K_{u2} areas, so that the writing and half-bit shift can be performed correctly. Alternatively, one can also design a racetrack bottom area with two readers: one in the left and the other in the right of the writer. If the meta data bit is "1"/"0," the half-bit will be shifted to the right/left, and the right/left reader will be used for verification, respectively.

Next, to examine the margin of the depinning pulse current density, we perform the simulation for the same wire but increase the depinning pulse J_2 to 1.8×10^8 A/cm^2. The simulation results are shown in Fig. 5. We observe that after the depinning pulse J_2, the head wall moved over the middle K_{u2} site, while the tail wall reached the left boundary of the middle K_{u2} site. Consequently, the domain expansion finished at $t = 10$ ns, which is 2 ns faster than the previous case. Nevertheless, all operations were achieved as expected. This result demonstrates the large margin for selecting the depinning current density when K_{u2} is 1.5×10^6 J/m^3.

Next, we performed simulations for the nanowire with higher $K_{u2} = 3.5 \times 10^6$ J/m^3. Figures 6 and 7 show the simulation results with a 1 ns depinning pulse $J_2 = 2.7 \times 10^8$ and 2.9×10^8 A/cm^2, respectively. For both cases, depinning was successful. When $J_2 = 2.7 \times 10^8$ A/cm^2, full-bit expansion finished at $t = 10$ ns. However, when $J_2 = 2.9 \times 10^8$ A/cm^2, full-bit expansion finished at about $t = 8$ ns. With higher K_{u2} of 3.5×10^6 J/m^3, the small change of $\Delta J_2 = 0.2 \times 10^8$ A/cm^2 accounts for the change of full-bit expansion time $\Delta t = 2$ ns, which is smaller than $\Delta J_2 = 0.8 \times 10^8$ A/cm^2 for the previous case of $K_{u2} = 1.5 \times 10^6$ J/m^3. Therefore, we conclude that while higher K_{u2} provides better margin (less error) for pinning, it leads to a lower margin of depinning current density.

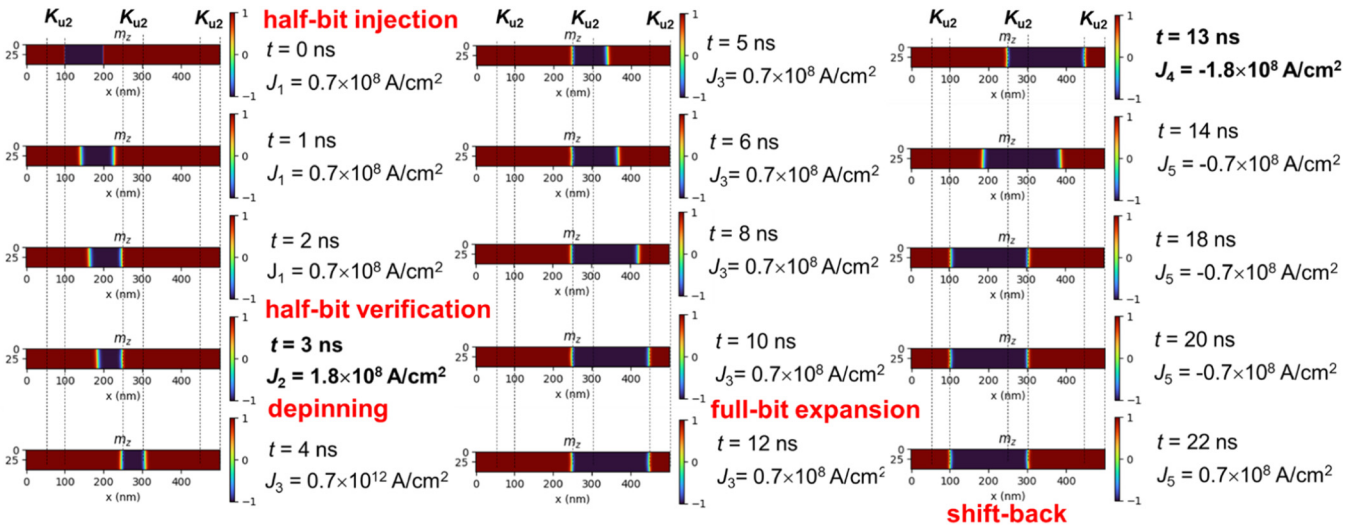

FIG. 5. Simulation of half-bit shift, depinning, full-bit expansion, and shift-back with 1 ns depinning pulses of $\pm 1.8 \times 10^8$ A/cm^2, when $K_{u1} = 1.0 \times 10^6$ J/m^3 and $K_{u2} = 1.5 \times 10^6$ J/m^3.

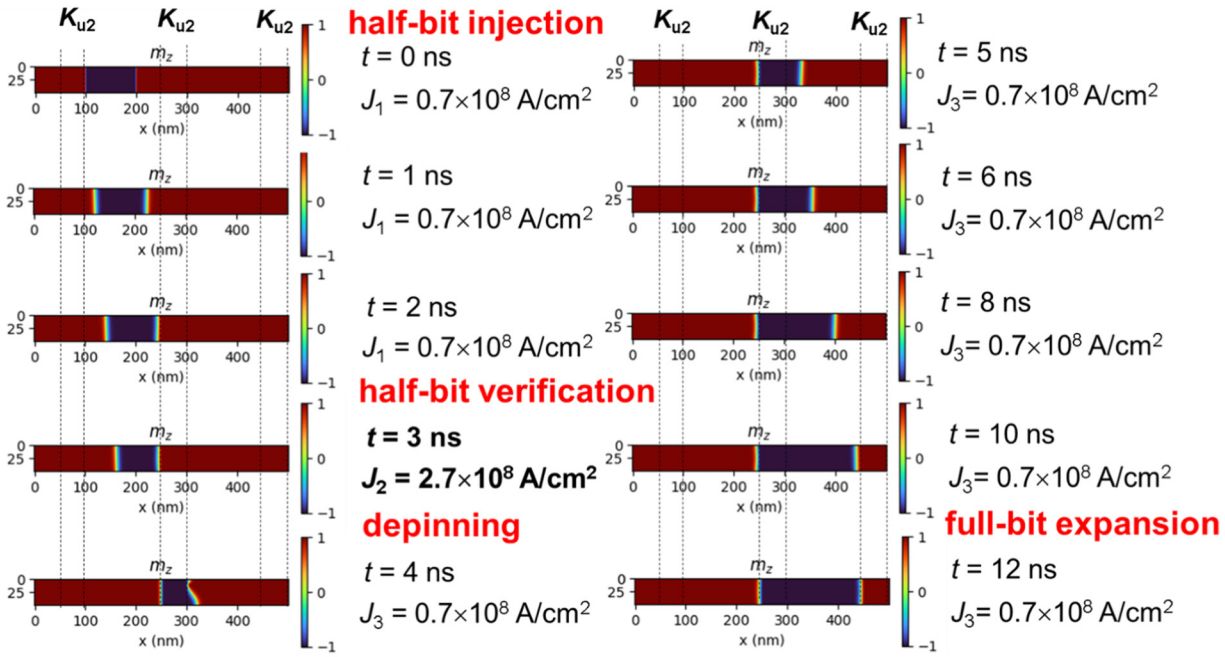

FIG. 6. Simulation of half-bit shift, depinning, and full-bit expansion with a 1 ns depinning pulse of 2.7 × 10^8 A/cm^2, when K_{u1} = 1.0 × 10^6 J/m^3 and K_{u2} = 3.5 × 10^6 J/m^3.

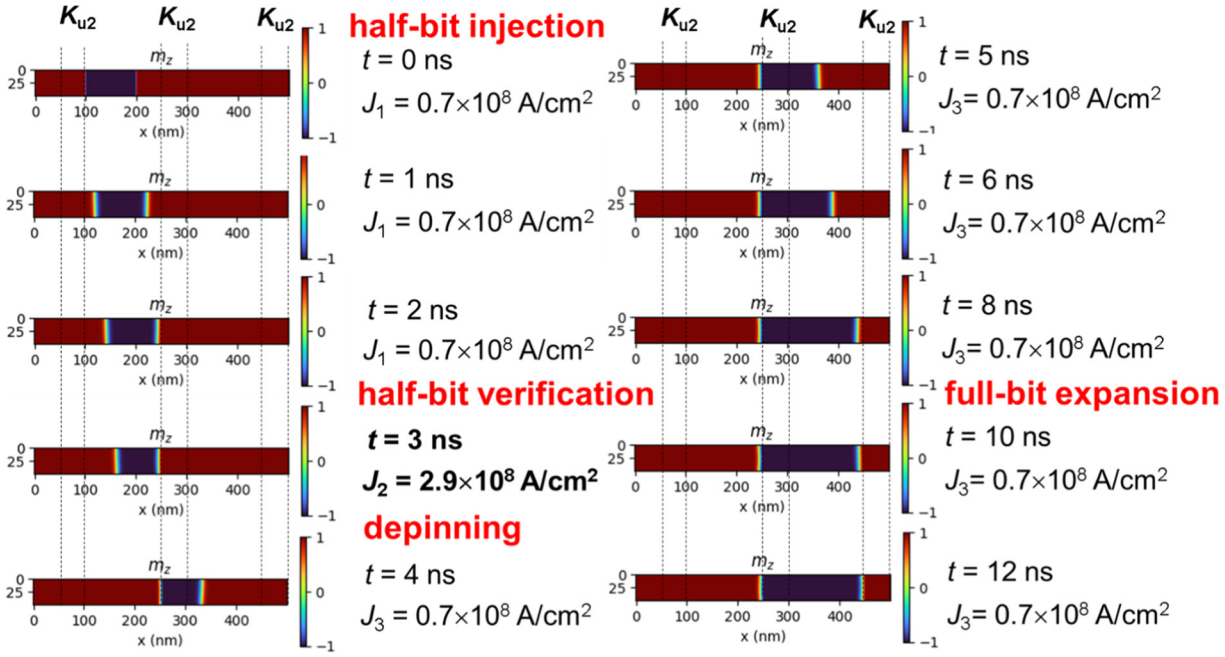

FIG. 7. Simulation of half-bit shift, depinning, and full-bit expansion with a 1 ns depinning pulse of 2.9 × 10^8 A/cm^2, when K_{u1} = 1.0 × 10^6 J/m^3 and K_{u2} = 3.5 × 10^6 J/m^3.

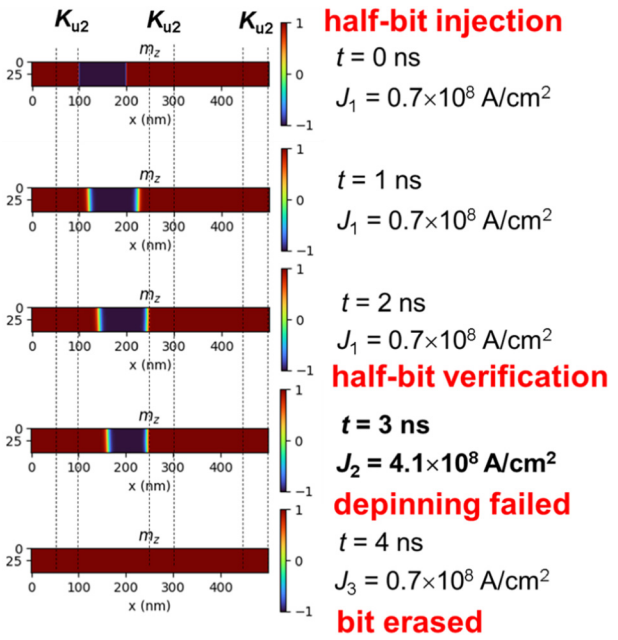

FIG. 8. Simulation of half-bit shift and failed depinning with a 1 ns depinning pulse of 4.1×10^8 A/cm^2, when $K_{u1} = 1.0 \times 10^6$ J/m^3 and $K_{u2} = 6.4 \times 10^6$ J/m^3, which results in the written half-bit mistakenly erased.

The lower margin of depinning current density is equivalent to the increasing uncertainty of the bit-shift time. If suppression of the uncertainty of the bit-shift time by the pinning effect of the K_{u2} sites is not enough, we need to increase the bit-length (i.e., the length of the K_{u1} sites). The optimum K_{u2} value for the lowest bit-shift error depends on the nature of the uncertainty (spread) of the K_{u2} value in real devices.

Finally, we performed simulations for the nanowire with very high $K_{u2} = 6.4 \times 10^6$ J/m^3. Figures 8–10 show the simulation results for a 1 ns depinning pulse $J_2 = 4.1 \times 10^8$, 4.12×10^8, and 4.15×10^8 A/cm^2, respectively. When $J_2 = 4.1 \times 10^8$ A/cm^2, the head wall could not be depinned from the boundary, resulting in the written half-bit erased as shown in Fig. 8. When $J_2 = 4.12 \times 10^8$ A/cm^2, the depinning and full-bit expansion were successful, as shown in Fig. 9. However, when $J_2 = 4.15 \times 10^8$ A/cm^2, both the head wall and the tail wall were depinned, resulting in the full-bit expansion error. In other words, the margin of J_2 is less than 0.1×10^8 A/cm^2. Thus, we conclude that when K_{u2} is much higher than K_{u1}, the depinning current density margin is impractically small.

Although our simulations were performed for a single magnetic wire in which the MDWs are driven by STT, we expect the same precise control of MDWs in our structure by SOT in magnetic or synthetic antiferromagnets/SOT multilayers,[27–31] which can drive the domain wall more efficiently than the STT technique.

Finally, we note that further simplification of the bottom of the MDW memory in Fig. 3 is possible by eliminating the reader

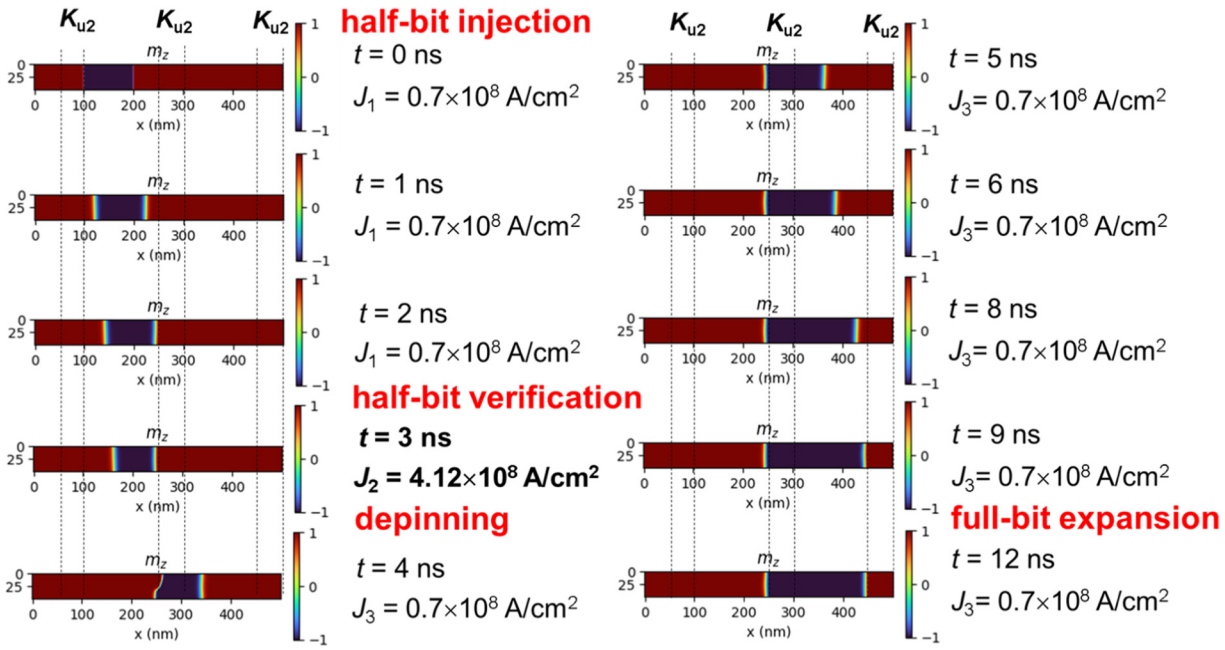

FIG. 9. Simulation of half-bit shift, depinning, and full-bit expansion with a 1 ns depinning pulse of 4.12×10^8 A/cm^2, when $K_{u1} = 1.0 \times 10^6$ J/m^3 and $K_{u2} = 6.4 \times 10^6$ J/m^3.

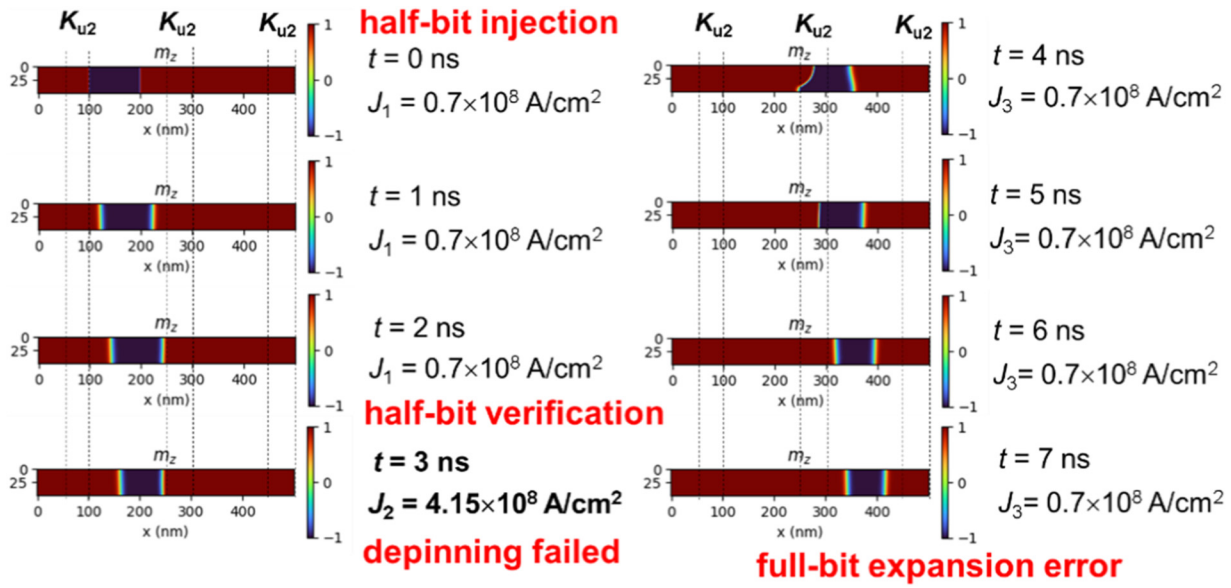

FIG. 10. Simulation of half-bit shift, failed depinning, and full-bit expansion error with a 1 ns depinning pulse of 4.15×10^8 A/cm^2, when $K_{u1} = 1.0 \times 10^6$ J/m^3 and $K_{u2} = 6.4 \times 10^6$ J/m^3.

and using the writer for both writing and reading/verification. However, having a reader near the corner is useful for detecting whether the half-bit is accidentally erased by the J_1 pulse or not and provides a further redundancy for the writing operation. Furthermore, by separating the writer and the reader, we can use different technologies for the writer and the reader, for example, Oersted field-writer and Hall-effect reader.

VI. CONCLUSION

In conclusion, we have proposed an architecture for the suppression of MDW shift error in 3D by utilizing the spatially modulated PMA of magnetic layers deposited on the sidewalls of multilayers of different oxide materials. We experimentally identified the oxide material candidates for such implementation and found that CrO_x can generate the largest PMA while GdO_x generates the smallest PMA of Pt/Co/Pt multilayers. We then confirmed the half-bit shift, pinning, depinning, full-bit expansion, and shift-back operations in our architecture by micromagnetic simulation. Our proposed architecture can be a key to realizing 3D MDW racetrack memory with low bit-shift error.

ACKNOWLEDGMENTS

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AUTHOR DECLARATIONS

Conflict of Interest

The authors have no conflicts to disclose.

Author Contributions

Pham Nam Hai: Conceptualization (lead); Funding acquisition (lead); Project administration (lead); Resources (lead); Supervision (lead); Validation (lead); Visualization (equal); Writing – original draft (lead); Writing – review & editing (lead). **Takanori Shirokura:** Data curation (equal); Formal analysis (equal); Investigation (equal); Methodology (equal); Visualization (equal). **Nguyen Huynh Duy Khang:** Data curation (equal); Formal analysis (equal); Investigation (equal); Methodology (equal); Visualization (equal).

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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